Muhammad Hassan Tahir

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PROFESSIONAL SUMMARY

Semiconductor process and device engineer with over three years of experience in epitaxy, thin-film deposition, and device characterization for high-performance architectures. Expert in DOE-driven process integration and wafer-level characterization, enabling the transition of R&D innovations into scalable manufacturing. Proficient in optimizing CMOS/BJT-related fabrication steps and advanced metrology to improve device responsivity and thermal stability.

EDUCATION

University of South Carolina — **Columbia, SC**
MS Electrical Engineering — *July 2022 – July 2025*

Lahore University of Management Sciences — **Lahore, Pakistan**
BS Chemistry — *July 2018 – July 2022*

EXPERIENCE

Process Engineering — **January 2025 - Present**
Kyma Technologies — *Raleigh, NC*

- Optimized HVPE and MOCVD growth recipes using Design of Experiments (DOE) to improve film uniformity and run-to-run repeatability by 25%.
- Scaled manufacturing workflows to increase wafer throughput by 1.5× and reduce cycle time by 30% for AlGaN and ultra-wide bandgap films.
- Delivered >20 epi wafers for 10 kV-class device development, ensuring high crystal quality through rigorous AFM and XRD characterization.
- Partnered with DOE, AFRL, and DOD on β-Ga_2O_3 development, providing experimental data for 3+ federal technical reports.

Entrepreneurial Lead — **April 2024 – December 2024**
National Science Foundation — *Columbia, SC*

- Secured $50K NSF I-Corps grant and spearheaded customer discovery at industry conferences to validate market needs for wide-bandgap architectures.
- Analyzed power electronics adoption barriers to develop a data-driven commercialization roadmap and pivot product designs for market applications.
- Established a startup and filed a patent for β-Ga_2O_3 based deep-UV detectors while applying for SBIR/STTR commercialization grants.

Graduate Research Assistant — **July 2022 – July 2023**
University of South Carolina — *Columbia, SC*

- Optimized deep-UV β-Ga_2O_3/4H-SiC diodes by tuning growth conditions and Si co-doping to enhance responsivity, breakdown voltage, and thermal stability.
- Investigated interface dynamics in MOCVD-grown thin films and HFETs using C–V profiling and SKPM to characterize dielectric integration.
- Investigated interface and defect dynamics in MOCVD-grown $(Al_{1-x}Ga_x)_2O_3$ and GaN/AlGaN HFETs using SKPM and C–V profiling for dielectric integration.

PUBLICATION AND PATENTS

- M. U. Jewel, S. R. Crittenden, **M. T. Hassan**, et al., "Surface properties of MOCVD grown $(Al_{1-x}Ga_x)_2O_3$ thin films on c-plane sapphire via SKPM," AIP Advances, vol. 14, no. 12, 2024.
- N. J. Nipa, K. Fu, **M. T. Hassan**, et al., "Effect of growth conditions on β-Ga_2O_3 diodes on 4H–SiC," IEEE MDTS Conference, 2025.
- **M. T. Hassan**, et al., "β-Ga_2O_3 Diodes on 4H–SiC for <254 nm Switching/Detection," GOX Conference 2025
- Indium/silicon delta co-doped beta-gallium oxide for better performing devices. USC Patent ID No. 1771. The inventors are I. Ahmad, N. J. Nipa, **M. T. Hassan**.

TECHNICAL SKILLS

Semiconductor Fabrication: ALD, MOCVD, PECVD, PVD, RIE, ALE, ICP, CCP, Oxidation, Diffusion, Ion Implantation

Imaging & Microscopy: SEM, EDS/EDX, TEM, Optical Microscopy, AFM (Surface Roughness Optimization)

Spectroscopy: XRD, XRR, XRF, XPS, UV-Vis, FTIR, Raman Spectroscopy

Chemical & Qualitative Analysis: TGA, AFM, DSC, GC, LC/HPLC, GCMS, SIMS, Lithography.

Electrochemical & Durability: C–V/I–V Profiling, LSV, RDE, EIS, ADT.

Software & Data Analysis: MATLAB, Tableau, OriginPro, JMP, Minitab, DOE (Design of Experiments), Weibull Analysis, MS Office.