

**Define Clock**

Enter parameters below to force the signal to an alternating pattern (clock). Assignments made from within HDL code or any previously applied constant or clock force will be overridden

Signal Name:

Value Radix:

Leading Edge Value:

Trailing Edge Value:

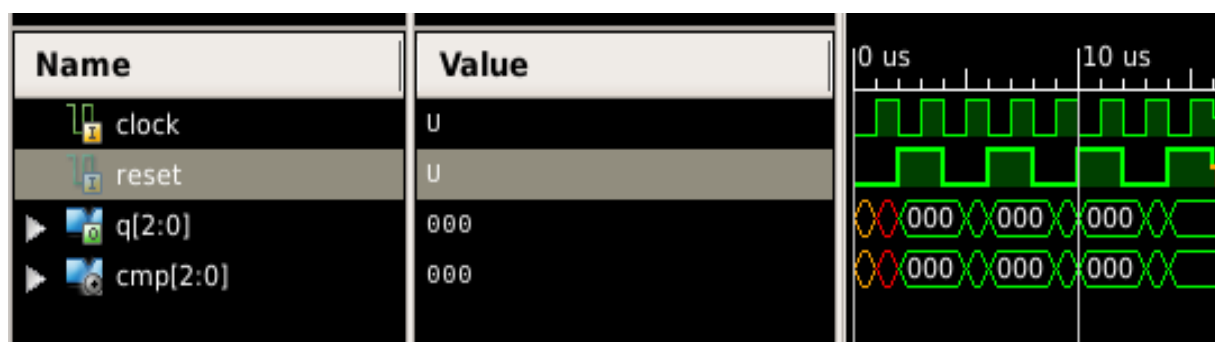
Starting at Time Offset:

Cancel after Time Offset:

Duty Cycle (%):

Period:

Leading Edge Value :	Valeur de bord d'attaque : 'départ'	قيمة الحافة الرائدة
Trailing Edge Value :	Valeur du bord de fuite : 'fin'	قيمة الحافة الخلفية
Starting at Time Offset :	À partir du décalage horaire :	
Cancel after Time Offset :	Annuler après le décalage horaire	
Duty Cycle (%) :	Cycle d'utilisation (%) :	
Period	Période	



$$2 * T_{clock} = T_{reset}$$

$$2 * 2us = 4us$$

will be overridden

Signal Name:

Value Radix:

Leading Edge Value:

Trailing Edge Value:

Starting at Time Offset:

Cancel after Time Offset:

Duty Cycle (%):

Period:

will be overridden

Signal Name:

Value Radix:

Leading Edge Value:

Trailing Edge Value:

Starting at Time Offset:

Cancel after Time Offset:

Duty Cycle (%):

Period:

Signal Name:

Value Radix:

Leading Edge Value:

Trailing Edge Value:

Starting at Time Offset:

Cancel after Time Offset:

Duty Cycle (%):

Period:

Signal Name:

Value Radix:

Leading Edge Value:

Trailing Edge Value:

Starting at Time Offset:

Cancel after Time Offset:

Duty Cycle (%):

Period:

