The University of Azad Jammu & Kashmir, Muzaffarabad

Lab Title:
Verification of Basic Logic Gates and Their Truth Tables

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Course Title: Computer Architecture and Logic Design

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Lab Objective:

The objective of this lab is to study, design and verify the functionality of basic logic gates (AND, OR, NOT, NAND, NOR, XOR) and their truth tables using Electronic Workbench.

Apparatus:

The apparatus used for this lab:

- Virtual power supply
- Virtual breadboard
- ICs: 7400, 7402, 7404, 7408, 7432, 7486.
- Virtual connecting wires
- Simulation software: Electronic Workbench (EWB)

Theory:

Logic gates are digital circuits with one output and one or two inputs. Different logic gates are AND, OR, NOT, NAND, NOR, XOR. They work according to certain logic.

1. AND Gate:

➔ Logic equation. Y = A.B

The output of AND gate is logic 1 when both the inputs A and B are at high logic.

2. OR Gate:

➔ Logic equation. Y = A+B.

The output of OR gate is logic 1 when either one of the inputs A or B or both the inputs are logic 1.

3. NOT Gate:

➔ Logic equation. Y = $\bar{A}$.

The output of NOT gate is a complement of the input.

4. NAND Gate:

➔ Logic equation. Y = ~(A.B) or Y= (A.B)'

The output of the NAND gate is high logic or logic 1 when one of the inputs or both the inputs are low level.

5. NOR Gate:

➔ Logical equation. Y = A+B.

The output of NOR gate is true when both the inputs are low.

6. X-OR Gate:

➔ Logic equation. Y=AB+AB.

The output of the XOR gate is true when both inputs are complemented by each other.

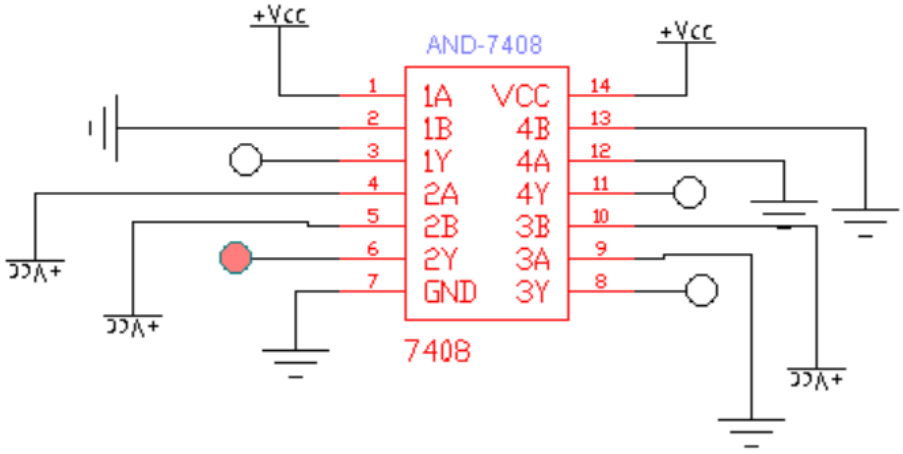
Procedure:

The following procedure was followed for simulating each logic gate:

1. I selected the relevant IC according to the gate I was simulating.
2. I attached ground to port 7 and voltage to port 14.
3. Different input combinations and various probes for output were attached on the remaining ports.
4. Truth tables were filled based on the output displayed (Probe lighted up when the output was HIGH)
5. Screenshots of all working circuits were taken for documentation/ lab report.

Observations:

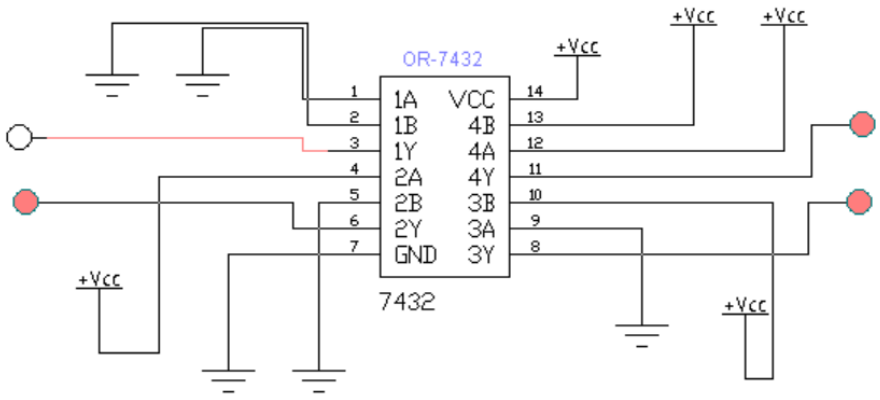
1. **AND- 7408**



Truth Table:

A	B	Y=A*B
0	0	0
0	1	0
1	0	0
1	1	1

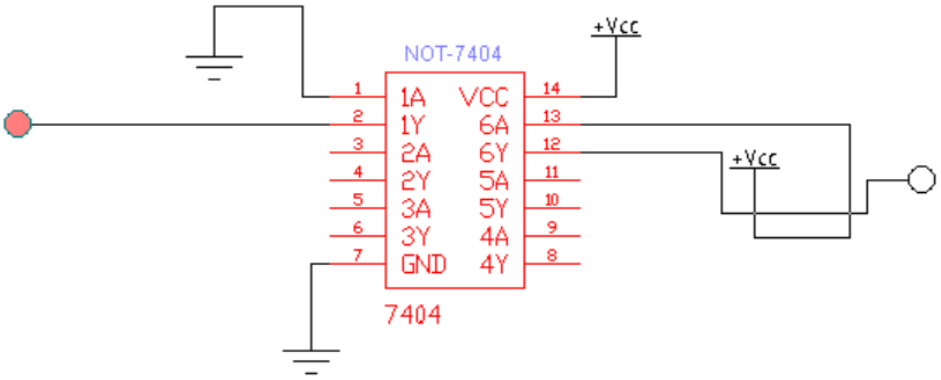
2. OR- 7432



Truth Table:

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

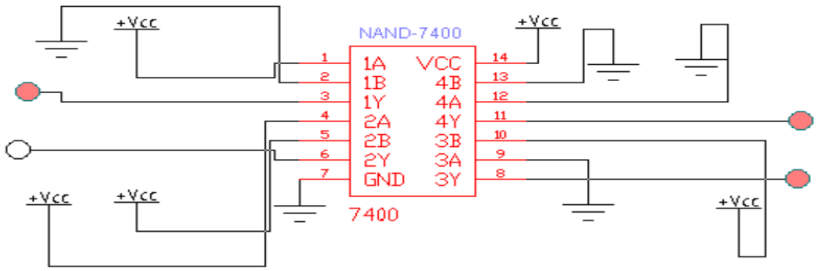
3. NOT- 7404



Truth Table:

A	Y= $\bar{A}$
0	1
1	0

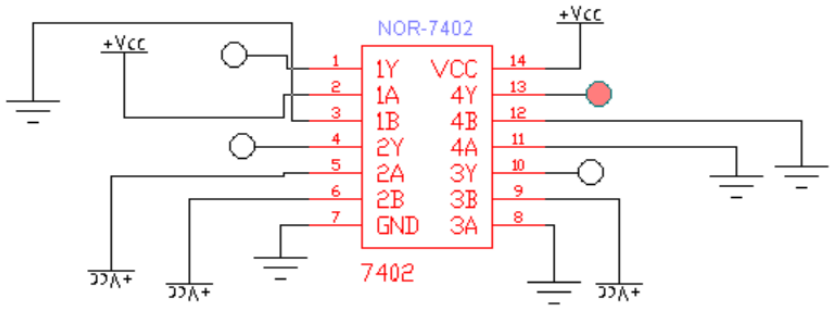
4. NAND- 7400



Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

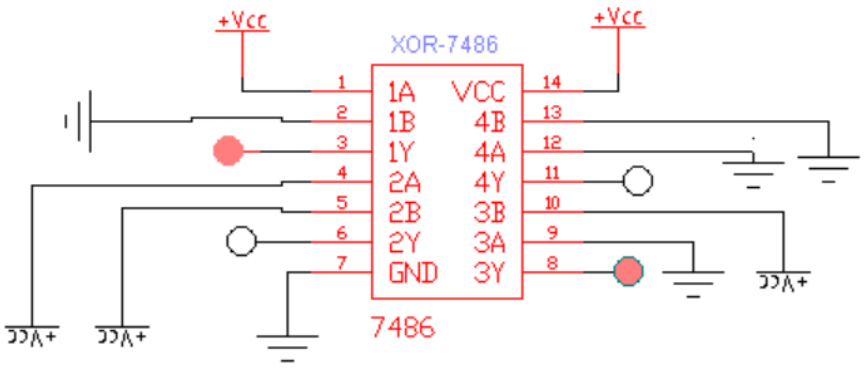
5. NOR- 7402



Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

6. XOR- 7486



Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Conclusion:

In this lab, the fundamental behavior of basic logic gates **(AND, OR, NOT, NAND, NOR, XOR)** was successfully verified using virtual simulation in Electronics Workbench. The truth tables for each gate were constructed and matched the theoretical expectations, demonstrating the functionality of digital logic circuits.

This lab helped students including me understand how logical gates form the circuits of digital electronics and their application in circuit design.