Multi-Frequency Impedance Transformers for Frequency-Dependent Complex Loads

Yun Liu, Yongjiu Zhao, Shaobin Liu, Yonggang Zhou, and Yao Chen

***Abstract*—In this paper, a general synthesis method is proposed for the design of multi-frequency impedance transformers (MFITs) for arbitrary frequency-dependent complex loads (FDCLs) by adopting the concept of multi-frequency inverters (MFIs). An MFI, which is placed between two susceptance blocks, is constructed with a transmission line and two-side multi-frequency susceptances (MFSs), whose values at multiple frequencies are independently specified. By merging neighboring susceptances, we get a very simple Pi-shaped topology of MFITs, which in theory has no limitation on the number of matching frequencies. The MFS blocks are realized with one or more parallel shunt stubs, providing needed susceptance values at several specified frequencies. A genetic algorithm is used in extracting the circuit parameters of the parallel stubs. Several dual-, triple-, and quad-frequency impedance transformers for FDCLs are designed for illustrating the design methods. Experiment and simulation results are compared with good agreement, validating the feasibility of the theory. The designed impedance transformers are concise in circuit and compact in dimensions.**

***Index Terms*—Frequency-dependent complex load (FDCL), multi-frequency impedance transformer (MFIT), multi-frequency inverter (MFI).**

I. Introduction

IMPEDANCE transformers are basic building blocks for microwave components, such as power amplifiers, power splitters, and antennas. Recently, as more and more wireless communication standards and wireless applications are proposed, systems and circuits are required to work simultaneously on several frequency bands. Thus, the research on multi-frequency impedance transformers (MFITs) has raised much attention.

Although many MFITs have been presented in the recent decade, a majority of the studies deal with dual-frequency problems. Dual-frequency impedance transformers (DFITs) were first realized between two real impedances using cascaded two sections of commensurate lines [1], L-shaped network of transmission lines [2], and Pi-shaped network [3].

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A more general problem is to realize DFITs for frequency-dependent complex loads (FDCLs). Thus, a lot of new topologies and methods are generated [4]–[13]. In [4], three transmission lines are cascaded for realizing the DFIT for the FDCL. As an alternative to [4], two sections of transmission lines and a two-section shunt stub are cascaded with the shortcoming of large dimensions [5]. A T-shaped DFIT is then proposed with simplified structure and compacter dimensions [6]. In [7], the DFIT is enriched with a dc-block function by adopting coupled lines. A generalized DFIT for two complex impedances is realized with four sections of transmission lines [8]. The above distributed dual-frequency transformers often have two or more sections of transmission lines or coupled lines, and thus are large in length.

Dual-frequency offset-lines that are realized with symmetric T-shaped [9] or Pi-shaped networks [10], [11] can directly function as DFITs between real impedances, and they can be used to construct DFITs for FDCLs by adding a section of transmission line and a stub [10] or a T-shaped dual-band stub [11] at the expense of high circuit complexity and large dimensions.

Lumped circuits always have smaller dimensions compared to distributed networks, and are much easier to be integrated into RF integrated circuits (RFICs). By means of frequency transformations, a lumped network can realize dual-frequency impedance matching between real load and real source [12]. For FDCLs, three topologies are proposed for dual-frequency matching according to different dual-frequency allocations of a load in a Smith chart [13].

Only a limited number of MFITs are presented to operate on more than two frequencies [12], [14]–[16], but they are not for FDCLs or not analytically designed. Successive frequency mappings are adopted in [12] for quad-frequency impedance matching between real impedances. In [14], a lumped triple-frequency impedance transformer between two real impedances is realized by extending the design concepts of [13]. Two sections of coupled lines are cascaded to form a quad-frequency impedance transformer between real impedances, but only three frequencies are independent [15]. MFITs containing multi-section transmission lines are designed for FDCLs using particle swarm algorithm (PSA), a fully optimizing method [16].

Although there is possibility to increase the number of matching frequencies by cascading the structures of [1]–[8] with more sections of transmission lines or stubs, the difficulty will dramatically rise in analytically extracting the circuit parameters. Moreover, even if analytical design methods can be developed, some restriction conditions as used in [1]–[8] must be adopted to simplify the synthesis problems, resulting in redundant topologies.

It seems possible to develop triple- or quad-frequency offset-lines by extending the concepts and topologies of [9]–[11], but

perhaps at the expense of very high complexity in circuit. In addition MFITs containing the multi-frequency offset-lines for arbitrary FDCLs will be even larger.

Unlike most of the above topologies that only treat impedance matching at a fixed number of frequencies (commonly two frequencies), we present a general and concise topology of MFIT that, in theory, is suitable for an arbitrary number of frequencies. A simple synthesis method is established by adopting the concepts of multi-frequency inverters (MFIs) and multi-frequency susceptances (MFSs). The possible number of matching frequencies can be continually increased by adding a limited number of circuits to the MFS blocks.

II. Synthesis Theory of Multi-Frequency Impedance Transformers

A. Topology of the MFITs

Fig. 1(a) gives the topology of the MFIT, which includes a J inverter block and two susceptances jB_1 and jB_2. Here, Z_l is a FDCL. The J inverter is to form the inverse of the load admittance, and it works at multiple frequencies with the J value varies,

$$J(f_i) = J_i, \qquad i = 1 : N. \tag{1}$$

Here, f_i is the ith frequency at which impedance matching is demanded, and N is the number of matching frequencies. By parallel connecting a susceptance jB_1 to the load, we get an input impedance as Z_l', and across the inverter, we get

$$Y_{\text{in}}'(f_i) = J_i^2 Z_l'(f_i), \qquad i = 1 : N. \tag{2}$$

$Y_{\text{in}}'(f_i)$ must have a real part as Y_0, which is the characteristic admittance at the input port, thus we have

$$\text{Re}\left(Z_l'(f_i)\right) = \frac{Y_0}{J_i^2}, \qquad i = 1 : N. \tag{3}$$

The imaginary part of $Y_{\text{in}}'(f_i)$ should be compensated with jB_2 for impedance matching, thus,

$$B_2(f_i) = -\text{Im}\left(J_i^2 Z_l'(f_i)\right), \qquad i = 1 : N. \tag{4}$$

In the literature, a J inverter can be realized with a $\lambda/4$ transmission line or a Pi or T shaped lumped network [17], and always works at a single frequency with limited bandwidth. Fig. 1(b) gives a realization of the so-called MFI, which consists of a transmission line and two susceptance blocks. Here, the J values at the matching frequencies are not restricted to be equal. The transmission line has an electrical length θ, which is proportional to frequency. Each of the two susceptance blocks has specified susceptances at multiple frequencies, and here we call them multiple-frequency susceptances (MFSs). The jB_c block will be merged into neighboring circuits and is not needed to be realized directly, and thus incur circuit simplicity and dimension reduction. Due to the equality at N working frequencies, the left and right circuits of Fig. 1(b) have equal $ABCD$ matrices at all the matching frequencies, and we have (5), shown at the bottom of this page.

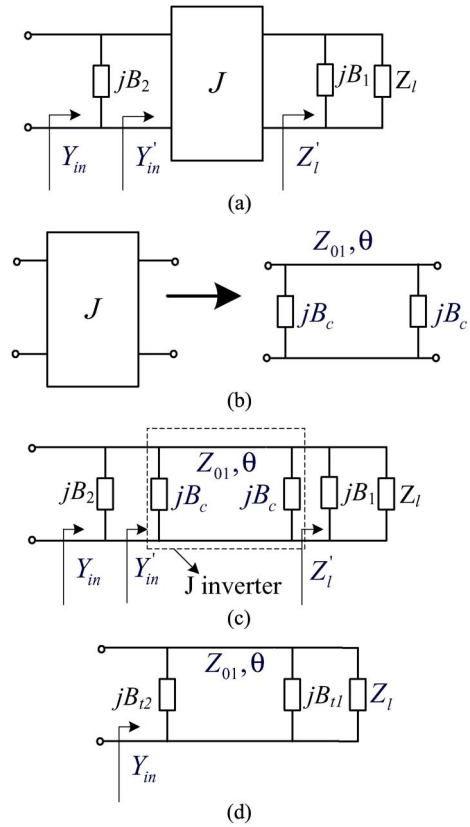

Fig. 1. Topologies of the MFITs. (a) General topology of MFIT. (b) J inverter implementation. (c) Detailed topology of MFIT. (d) Simplified topology of MFIT.

Here, θ_i is the electrical length at f_i, and B_{ci} is the value of B_c at f_i. From (5), we get the following three equations:

$$\begin{cases} \cos\theta_i - B_{ci} Z_{01} \sin\theta_i = 0 & \text{(6-1)} \\ Z_{01} \sin\theta_i = \dfrac{1}{J_i} \qquad i = 1 : N. & \text{(6-2)} \\ 2B_{ci}\cos\theta_i + \sin\theta_i / Z_{01} - B_{ci}^2 Z_{01}\sin\theta_i = J_i & \text{(6-3)} \end{cases}$$

$$\begin{aligned} \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ jB_{ci} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_i & jZ_{01}\sin\theta_i \\ \dfrac{j\sin\theta_i}{Z_{01}} & \cos\theta_i \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jB_{ci} & 1 \end{bmatrix} \\ &= \begin{bmatrix} \cos\theta_i - B_{ci}Z_{01}\sin\theta_i & jZ_{01}\sin\theta_i \\ j\left(2B_{ci}\cos\theta_i + \sin\theta_i/Z_{01} - B_{ci}^2 Z_{01}\sin\theta_i\right) & \cos\theta_i - B_{ci}Z_{01}\sin\theta_i \end{bmatrix} \\ &= \begin{bmatrix} 0 & \dfrac{j}{J_i} \\ jJ_i & 0 \end{bmatrix}, \qquad i = 1 : N \end{aligned} \tag{5}$$

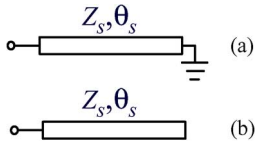

Fig. 2. Stubs for realizing MFS for DFITs.

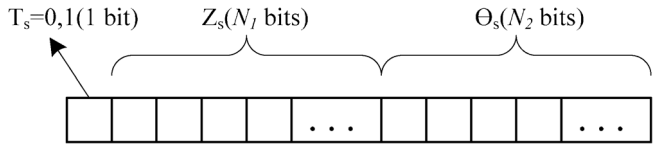

Fig. 3. Chromosome representation of a stub.

When the length and characteristic impedance of the transmission line are given, we obtain

$$\begin{cases} B_{ci} = \dfrac{\cot\theta_i}{Z_{01}} & \text{(7-1)} \\ J_i = \dfrac{1}{(Z_{01}\sin\theta_i)} & \text{(7-2)} \end{cases} \qquad i = 1:N.$$

If the jB_c circuit block can provide the needed susceptances given in (7-1) at the frequencies, the right two-port network in Fig. 2(b) will equal to an MFI with the J values given in (7-2).

We can replace the J inverter of Fig. 1(a) with Fig. 1(b) and get the circuit of the MFIT as shown Fig. 1(c).

We can now rewrite (3) as

$$\mathrm{Re}\,(Z_l'(f_i)) = Z_{01}^2\sin^2\theta_i Y_0, \qquad i = 1:N. \tag{8}$$

As we know,

$$\mathrm{Re}\,(Z_l'(f_i)) = \frac{G_l(f_i)}{G_l^2(f_i)+(B_l(f_i)+B_1(f_i))^2} \le \frac{1}{G_l(f_i)} \qquad i = 1:N \tag{9}$$

Here, G_l and B_l are the real and imaginary parts of Y_l. We have

$$Z_{01}^2\sin^2\theta_i Y_0 \le \frac{1}{G_l(f_i)}, \qquad i = 1:N. \tag{10}$$

Thus, Z_{01} must be chosen with the restriction

$$Z_{01} \le \min_{i=1:N}\sqrt{\frac{1}{G_l(f_i)Y_0\sin^2\theta_i}}. \tag{11}$$

In the design of an MFI, the electrical length θ and characteristic impedance Z_{01} can be chosen with certain freedoms, and manual selection of θ and Z_{01} are recommended for achieving different circuit larger matching bandwidths. After Z_{01} and θ are selected, we can find J_i and B_{ci} from (7), and in addition, derive the value of $B_1(f_i)$ from (9),

$$B_1(f_i) = \pm\sqrt{\frac{G_l(f_i)}{Z_{01}^2\sin^2\theta_i Y_0} - G_l^2(f_i) - B_l(f_i)}, \qquad i = 1:N. \tag{12}$$

There are two possible values for $B_1(f_i)$, and in addition, two values for $B_2(f_i)$ according to (4),

$$\begin{aligned} B_2(f_i) &= -\mathrm{Im}\left(\frac{1}{jB_1(f_i)+Y_l(f_i)}\cdot\frac{1}{(Z_{01}^2\sin^2\theta_i)}\right) \\ &= \pm Y_0\sqrt{\frac{1}{G_l Z_{01}^2\sin^2\theta_i Y_0}-1}, \qquad i = 1:N. \end{aligned} \tag{13}$$

Thus, more freedom can be found for MFIT design.

By merging the neighboring susceptances, the circuit of Fig. 1(c) can be simplified as shown in Fig. 1(d), and the values of B_{t1} and B_{t2} at f_i are

$$\begin{aligned} B_{t1}(f_i) &= B_1(f_i) + B_c(f_i) \\ &= \pm\sqrt{\frac{G_l(f_i)}{Z_{01}^2\sin^2\theta_i Y_0} - G_l^2(f_i) - B_l(f_i)} + \cot\theta_i/Z_{01}, \\ &\qquad i = 1:N \end{aligned} \tag{14}$$

and

$$\begin{aligned} B_{t2}(f_i) &= B_2(f_i) + B_c(f_i) \\ &= \pm Y_0\sqrt{\frac{1}{G_l Z_{01}^2\sin^2\theta_i Y_0} - 1} + \cot\theta_i/Z_{01}, \\ &\qquad i = 1:N. \end{aligned} \tag{15}$$

Different selection of $B_1(f_i)$ and $B_2(f_i)$ will result in different circuit synthesis results for jB_{t1} and jB_{t2}, and in addition, affects the matching bandwidths.

B. Synthesis of Dual-Frequency Susceptance Circuits

Now the task is to synthesize the MFS blocks of jB_{t1} and jB_{t2}, enforcing they provide needed values computed with (14) and (15).

For dual-frequency cases with $N = 2$, we use a single shunt stub to realize an MFS. The stub may be short circuited or open circuited, as shown in Fig. 2(a) and (b).

The susceptance of a stub is

$$\begin{cases} B_s(f_i) = Y_s\tan\theta_s(f_i) & \text{open-circuited} \quad \text{(16-1)} \\ B_s(f_i) = -Y_s\cot\theta_s(f_i) & \text{short-circuited.} \quad \text{(16-2)} \end{cases}$$

A genetic algorithm [18] can be developed for extracting the circuit parameters including the stub type, characteristic impedance Z_s, and electrical length θ_s.

For implementing the genetic algorithm, the parameters of a stub should be encoded with a section of binary data, which is also called a chromosome, as shown in Fig. 3. Here, T_s is 1 bit with two value choices of 0 or 1, representing the stub is short or open circuited. Z_s and θ_s are encoded with N_1 bits and N_2 bits, respectively. As an inverse decoding procedure, Z_s and θ_{s11} can be computed from the corresponding bits, de-normalized to be within practical value ranges. In our design, we set $N_1 = N_2 = 10$.

Fig. 4 gives a flow graph for the synthesis of a dual-frequency MFS using a genetic algorithm. It starts by randomly generating a population of chromosomes, which represents stubs with different parameters. The fitness of each chromosome evaluates the differences between the stub susceptances and the goals

$$\text{fitness} = \frac{1}{\sum\limits_{i=1,2}|B_s(f_i) - B_t(f_i)|}. \tag{17}$$

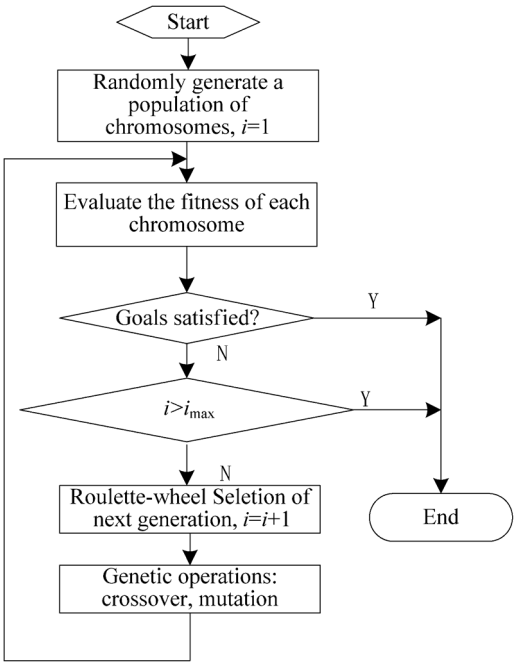

Fig. 4. General flowchart of genetic algorithm.

The best individual with highest fitness will be checked whether the optimization goals can be met.

A Roulette-wheel strategy will then be applied for selecting the father chromosomes of the next generation if the goals are not satisfied by any chromosome of the current generation. The chance that a chromosome can be selected is proportional to its fitness value. Following this is the genetic operations, including crossover operations between every two chromosomes and mutation operations on the individuals in respect of a certain ratio. The best chromosome is directly copied into the next generation, ensuring the best one of the next generation is not worse than that of the current generation. After the new generation is generated, the fitness of each new chromosome will be evaluated. The iteration procedure will not end until the best chromosome satisfies all goals, or until the allowable maximum generation number is reached.

C. Synthesis of Triple- and Quad-Frequency Susceptance Circuits

As impedance matching is required at more frequencies, we need more circuit freedoms for the design of MFSs. For triple- and quad-frequency cases, it is necessary to parallel combine two stubs for providing needed susceptances since two stubs can afford four design freedoms. The combinations of two stubs can be classified into three types, which are: 1) open–open; 2) open–short; and 3) short–short, as shown in Fig. 5.

For each type of these combinations, the susceptance is

$$\begin{cases} B_s(f_i) = Y_{s1}\tan\theta_{s1}(f_i) + Y_{s2}\tan\theta_{s2}(f_i) & \text{OO} \quad (18\text{-}1) \\ B_s(f_i) = Y_{s1}\tan\theta_{s1}(f_i) - Y_{s2}\cot\theta_{s2}(f_i) & \text{OS} \quad (18\text{-}2) \\ B_s(f_i) = -Y_{s1}\cot\theta_{s1}(f_i) - Y_{s2}\cot\theta_{s2}(f_i) & \text{SS.} \quad (18\text{-}3) \end{cases}$$

To design a triple- or a quad-frequency MFS, we also use a genetic algorithm to get the parameters, including stub types and Z_{s1}, θ_{s1}, Z_{s2}, and θ_{s2}. It is possible to include some analytical computations into the design of an MFS for decreasing

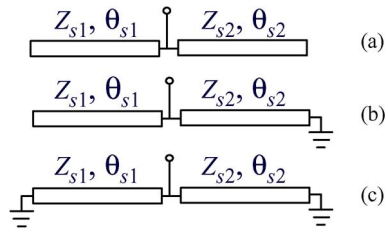

Fig. 5. Combined stubs for realizing MFS for triple-frequency impedance transformers. (a), Open–open (OO) type. (b) Open–short (OS) type. (c) Short–short (SS) type.

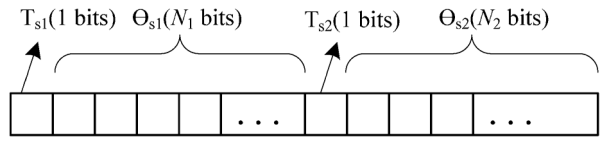

Fig. 6. Chromosome that represents a parallel connection of two stubs.

the number of unknowns. Here, Z_{s1} and Z_{s2} are not necessary to be treated as direct unknowns since they can be analytically computed if the stub types and electrical lengths are initially set in a chromosome, as shown in Fig. 6. Here, $N_1 = N_2 = 10$.

As an example, if we use an open-open stub combination to realize a triple-frequency susceptance block whose susceptances are $B(f_1)$, $B(f_2)$, and $B(f_3)$, we have

$$\begin{cases} Y_{s1}\tan\theta_{s1}(f_1) + Y_{s2}\tan\theta_{s2}(f_1) = B(f_1) & (19\text{-}1) \\ Y_{s1}\tan\theta_{s1}(f_2) + Y_{s2}\tan\theta_{s2}(f_2) = B(f_2). & (19\text{-}2) \end{cases}$$

For given θ_{s1} and θ_{s2}, we can solve the values of Y_{s1} and Y_{s2} from (19-1) and (19-2) as

$$\begin{cases} Y_{s1} = \frac{B(f_1)\tan\theta_{s2}(f_2) - B(f_2)\tan\theta_{s2}(f_1)}{\tan\theta_{s1}(f_1)\tan\theta_{s2}(f_2) - \tan\theta_{s1}(f_2)\tan\theta_{s2}(f_1)} & (20\text{-}1) \\ Y_{s2} = \frac{B(f_1)\tan\theta_{s1}(f_2) - B(f_2)\tan\theta_{s1}(f_1)}{\tan\theta_{s2}(f_1)\tan\theta_{s1}(f_2) - \tan\theta_{s1}(f_1)\tan\theta_{s2}(f_2)}. & (20\text{-}2) \end{cases}$$

Since the susceptance of the circuit at f_3 is demanded to be $B(f_3)$, the fitness function can be set as

$$\text{fitness} = \frac{1}{|B(f_3) - Y_{s1}\tan\theta_{s1}(f_3) - Y_{s2}\tan\theta_{s2}(f_3)|}. \quad (21)$$

Similarly, we can list the equations to compute Y_{s1}, Y_{s2} and fitness in (22) and (23) for the cases of open–short or short–short circuits individually.

For open–short cases,

$$\begin{cases} Y_{s1} = \frac{B(f_1)\cot\theta_{s2}(f_2) - B(f_2)\cot\theta_{s2}(f_1)}{\tan\theta_{s1}(f_1)\cot\theta_{s2}(f_2) - \tan\theta_{s1}(f_2)\cot\theta_{s2}(f_1)} & (22\text{-}1) \\ Y_{s2} = \frac{B(f_1)\tan\theta_{s1}(f_2) - B(f_2)\tan\theta_{s1}(f_1)}{-\cot\theta_{s2}(f_1)\tan\theta_{s1}(f_2) + \tan\theta_{s1}(f_1)\cot\theta_{s2}(f_2)} & (22\text{-}2) \\ \text{fitness} = \frac{1}{|B(f_3) - Y_{s1}\tan\theta_{s1}(f_3) + Y_{s2}\cot\theta_{s2}(f_3)|}. & (22\text{-}3) \end{cases}$$

For short–short cases,

$$\begin{cases} Y_{s1} = \frac{B(f_1)\cot\theta_{s2}(f_2) - B(f_2)\cot\theta_{s2}(f_1)}{-\cot\theta_{s1}(f_1)\cot\theta_{s2}(f_2) - \cot\theta_{s1}(f_2)\cot\theta_{s2}(f_1)} & (23\text{-}1) \\ Y_{s2} = \frac{B(f_1)\cot\theta_{s1}(f_2) - B(f_2)\cot\theta_{s1}(f_1)}{-\cot\theta_{s2}(f_1)\cot\theta_{s1}(f_2) + \cot\theta_{s1}(f_1)\cot\theta_{s2}(f_2)} & (23\text{-}2) \\ \text{fitness} = \frac{1}{|B(f_3) + Y_{s1}\cot\theta_{s1}(f_3) + Y_{s2}\cot\theta_{s2}(f_3)|}. & (23\text{-}3) \end{cases}$$

An evolutional procedure will result in the most suitable θ_{s1} and θ_{s2}, and the stub types as well. The characteristic admittances Y_{s1} and Y_{s2} can then be computed.

We also use two parallel stubs to realize a quad-frequency MFS whose susceptance at four frequencies are $B(f_1)$, $B(f_2)$, $B(f_3)$, and $B(f_4)$. Similar design steps for triple-frequency

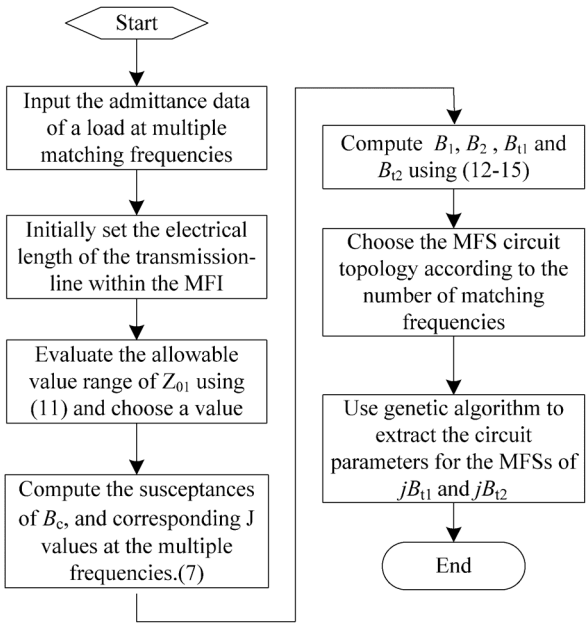

Fig. 7. Design graph of a MFIT.

MFSs can be adopted, except that we must simultaneously evaluate the values of both $B_s(f_3)$ and $B_s(f_4)$ in the fitness function. For different types of stub combinations, we have different fitness functions as follows:

$$\begin{cases} \text{fitness}=\dfrac{1}{\sum_{i=3,4}|B(f_i)-Y_{s1}\tan\theta_{s1}(f_i)-Y_{s2}\tan\theta_{s2}(f_i)|} & \text{OO} \quad (24\text{-}1) \\ \text{fitness}=\dfrac{1}{\sum_{i=3,4}|B(f_i)-Y_{s1}\tan\theta_{s1}(f_i)+Y_{s2}\cot\theta_{s2}(f_i)|} & \text{OS} \quad (24\text{-}2) \\ \text{fitness}=\dfrac{1}{\sum_{i=3,4}|B(f_i)+Y_{s1}\cot\theta_{s1}(f_i)+Y_{s2}\cot\theta_{s2}(f_i)|} & \text{SS.} \quad (24\text{-}3) \end{cases}$$

For impedance matching at more than four frequencies, we can parallel connect more than two stubs or use stepped-impedance stubs to afford more design freedoms for realizing corresponding MFSs.

For the convenience of implementation, a summarized design graph for MFITs is given in Fig. 7.

III. Design Examples and Results

A. DFITs

To give design examples following the theory above, we firstly construct an FDCL, as shown in Fig. 8. It consists of a transmission line that is terminated by a resistor. The real and imaginary parts of the load admittance are plotted in Fig. 8.

Dealing with the FDCL, we give the design steps for a DFIT with the frequencies of $f_1 = 1$ GHz and $f_2 = 2.05$ GHz.

As can be computed, the load impedances and admittances at the two frequencies are (the units ohm and siemens are omitted)

$$Z_l(f_1) = 14.42 - \text{j}21.54 \quad Z_l(f_2) = 9.4 + j6.03$$
$$Y_l(f_1) = 0.0215 + \text{j}0.0321 \quad Y_l(f_2) = 0.0754 - j0.0483.$$

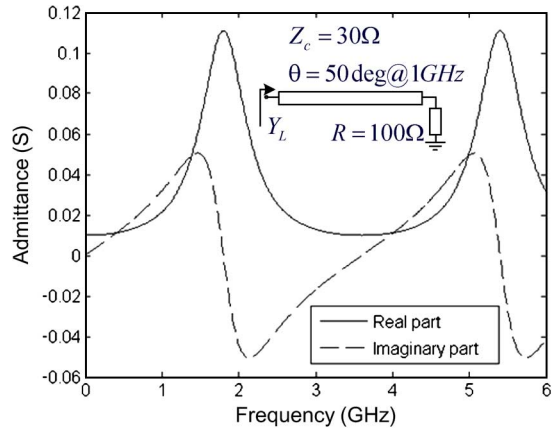

Fig. 8. Admittance of a constructed FDCL.

Step 1: Design of the Dual-Frequency Admittance Inverter: We always have a certain freedom in choosing the length of the transmission line, and here we initially set

$$\theta_2 = \frac{\pi}{2}.$$

Correspondingly we have

$$\theta_1 = \frac{\pi}{2}\frac{f_1}{f_2} = 0.7662.$$

For the means of multi-frequency impedance matching, Z_{01} must be set within a frequency range according to (11),

$$Z_{01} \le \min_{i=1:2}\sqrt{\frac{1}{G_l(f_i)Y_0\sin^2(\theta(f_i))}} = 25.75\ \Omega$$

and we can select a value as $Z_{01} = 25.75\ \Omega$.

For constructing a dual-frequency J inverter, two jB_c blocks are included with the values computed with (7-1),

$$B_c(f_1) = 0.0403 \quad B_c(f_2) = 0.$$

Together with this, we computed the equalized J values at f_1 and f_2 with (7-2),

$$J_1 = 0.06 \quad J_2 = 0.0388.$$

Step 2: Calculation of jB_1, jB_2, jB_{t1}, and jB_{t2}: After the parameters of the dual-frequency J inverter are determined, we need to decide the susceptances of jB_1 and jB_2 in Fig. 1(a). For achieving $Y'_{\text{in}}(f_i)$ with the real part as Y_0, B_1 should be computed according to (12), which results in two solutions at each frequency, and we choose

$$B_1(f_1) = -0.0859 \quad B_1(f_2) = 0.0483.$$

Correspondingly, for compensating the imaginary part of $Y'_{\text{in}}(f_i)$, B_2 is therefore computed with (13),

$$B_2(f_1) = -0.0502 \quad B_2(f_2) = 0.$$

TABLE I
STUB PARAMETERS FOR jB_{t1} AND jB_{t2} OF A DUAL-FREQUENCY IMPEDANCE TRANSFORMER ($f_1 = 1$ GHz AND $f_2 = 2.05$ GHz)

Circuit block	Stub type	Characteristic Impedance	Electrical Length@1GHz
jB_{t1}	Short	13.1 Ω	59.44 Degree
jB_{t2}	Short	104.8 Ω	43.9 Degree

TABLE II
DESIGN DATA OF THREE DFITS

No.	1	2	3
f_1(GHz)	1	1	1
f_2(GHz)	2.05	2.7	3.3
$Z_{01}(\Omega)$	25.75	52.2	68.52
$\theta@f_2$ (degree)	90	90	90
$B_{t1}(f_1)$	-0.0456	-0.032	-0.0288
$B_{t1}(f_2)$	0.0483	0.0278	0.0081
Stub type for jB_{t1}	Short	Open	Open
$Z_{s1}(\Omega)$	13.1	22.2	66.1
$\theta_{s1}@f_1$ (degree)	59.44	145	117.8
$B_{t2}(f_1)$	-0.0099	0.021	0.005
$B_{t2}(f_2)$	0	0	0
Stub type for jB_{t2}	Short	Short	Short
$Z_{s2}(\Omega)$	104.8	83.9	201.7
$\theta_{s2}@f_1$ (degree)	43.9	100	136.4

With (14) and (15), we can merge jB_c and jB_1 into jB_{t1}, and jB_c and jB_2 into jBt_2, resulting in the following values:

$$B_{t1}(f_1) = -0.0456 \quad B_{t1}(f_2) = 0.0483$$
$$B_{t2}(f_1) = -0.0099 \quad B_{t2}(f_2) = 0.$$

Step 3: Circuit Synthesis of MFSs of jB_{t1} and jB_{t2}: Open and short stubs are candidates to realize jB_{t1} and jB_{t2} of Fig. 1(d). The stub type, together with characteristic impedance and electrical length, are extracted via a genetic algorithm, whose fitness function is given in (17). Since the number of unknowns and optimization goals are only two, the extraction of the parameters for a MFS block can be completed in 1 s. The resulted parameters are listed in Table I.

Following the same steps, we designed two other DFITs with different matching frequencies, and we list the design data of all the three designs in Table II.

Fig. 9 gives the simulated $S11$ of all three DFITs. We can see each plot has two reflection zeros at the required frequencies with certain matching bandwidths.

Fig. 10 compares the simulated and measured results of the 1-GHz/2.05-GHz design. The impedance matching circuit, as shown in Fig. 11, is fabricated on a Rogers 4003 substrate with a dielectric constant of 3.38 and a thickness of 0.508 mm. The measured plot matches the simulated one well, except for small frequency differences. The 10-dB matching bandwidths are 157 and 574 MHz.

B. Triple-Frequency Impedance Transformers

In regard to the same FDCL, we can design triple-frequency impedance transformers. For $f_1 = 1$ GHz, $f_2 = 1.8$ GHz, and $f_3 = 3$ GHz, we give similar design steps for explanation.

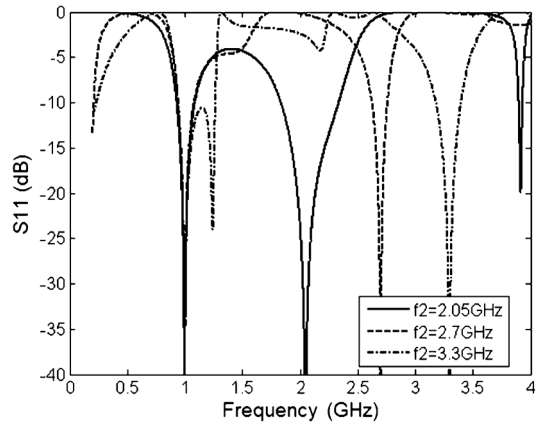

Fig. 9. Simulated $S11$ of three DFITs. ($f_1 = 1$ GHz).

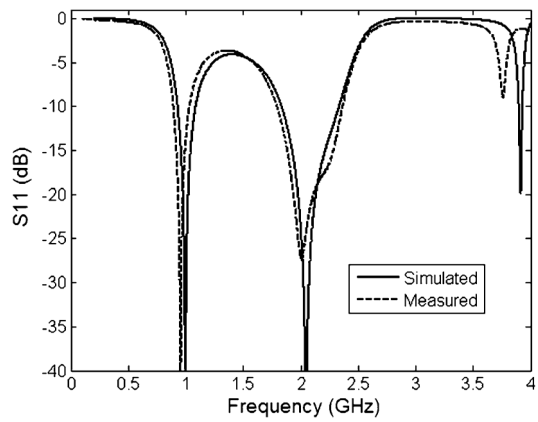

Fig. 10. Compared measured and simulated $S11$ of a DFIT. $f_1 = 1$ GHz, $f_2 = 2.05$ GHz.

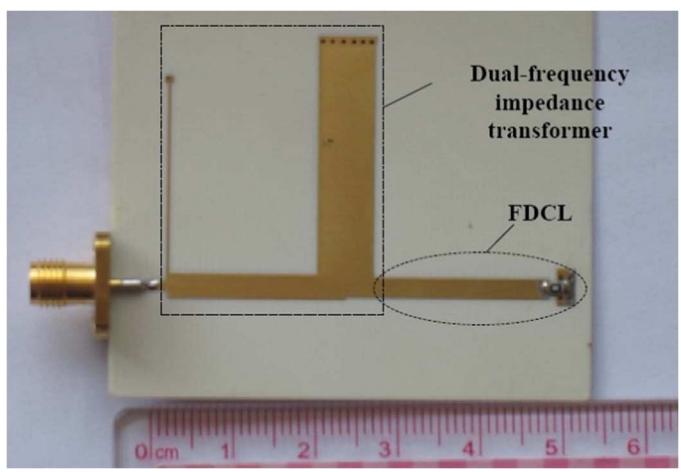

Fig. 11. Photograph of a DFIT: $f_1 = 1$ GHz, $f_2 = 2.05$ GHz.

Firstly, the impedances and admittances of the load at the three frequencies can be given as follows:

$$Z_l(f_1) = 14.42 - j21.54; Z_l(f_2) = 9.0$$
$$Z_l(f_3) = 28.3465 + j37.2$$
$$Y_l(f_1) = 0.0215 + j0.0321 \quad Y_l(f_2) = 0.1111$$
$$Y_l(f_3) = 0.0129 - j0.017.$$

TABLE III
STUB PARAMETERS FOR jB_{t1} AND jB_{t2} OF A TRIPLE-FREQUENCY IMPEDANCE TRANSFORMER (1 GHz/1.8 GHz/3 GHz)

Circuit block	Stub type	Characteristic Impedance	Electrical Lengths@1GHz
jB_{t1}	Short	65.5 Ω	90.535 Degree
	Short	87.6	15.2 Degree
jB_{t2}	Open	64.6 Ω	35.6 Degree
	Short	73.5	40.5 Degree

TABLE IV
DESIGN DATA OF THREE TRIPLE-FREQUENCY IMPEDANCE TRANSFORMERS

No.	1	2	3
f_1(GHz)	1	0.9	0.9
f_2(GHz)	1.8	3.5	2.4
f_3(GHz)	3	5.2	3.5
$Z_{01}(\Omega)$	26.22	25.79	45.25
$\theta@f_3$(degree)	90	110	135
$B_{t1}(f_1)$	-0.042	-0.0278	-0.0268
$B_{t1}(f_2)$	0.0277	0.0405	0.0533
$B_{t1}(f_3)$	-0.0108	-0.0583	-0.0094
Stub types for jB_{t1}	Short/short	Open/short	Short/open
Z_{s1}/Z_{s2} for $jB_{t1}(\Omega)$	65.5/87.6	23.35/45.83	37.6/121.7
$\theta_{s1}/\theta_{s2}@f_1$ for jB_{t1}(degree)	90.5/15.16	7.07/33.38	57.1/40.6
$B_{t2}(f_1)$	-0.0048	-0.0101	-0.0035
$B_{t2}(f_2)$	0.0277	0.0643	0.0119
$B_{t2}(f_3)$	-0.043	-0.0141	-0.0239
Stub types for jB_{t1}	Open/ short	Open/ short	Short/ Short
Z_{s1}/Z_{s2} for $jB_{t2}(\Omega)$	64.6/73.5	75.38/137	156.8/22
$\theta_{s1}/\theta_{s2}@f_1$ for jB_{t2}(degree)	35.6/40.6	20.13/26	18.3/109.1

In constructing a multi-frequency J inverter, we initially set the electrical length of the transmission line as

$$\theta(f_3) = \frac{\pi}{2}.$$

A proper characteristic impedance is then selected as

$$Z_{01} = \min_{i=1:3} \sqrt{\frac{1}{G_l(f_i) Y_0 \sin^2(\theta(f_i))}} = 26.22\ \Omega.$$

As the parameters of the connecting lines are given, jB_c must have the susceptances at the three frequencies as

$$B_c(f_1) = 0.0661 \quad B_c(f_2) = 0.227 \quad B_c(f_3) = 0.$$

The resulted MFI has the J values at the frequencies as

$$J_1 = 0.0763 \quad J_2 = 0.0471 \quad J_3 = 0.0381.$$

Following a similar method, we obtain

$$B_{t1}(f_1) = -0.042 \quad B_{t1}(f_2) = 0.227 \quad B_{t1}(f_3) = -0.0108$$
$$B_{t2}(f_1) = -0.0048 \quad B_{t2}(f_2) = 0.0277 \quad B_{t2}(f_3) = -0.043.$$

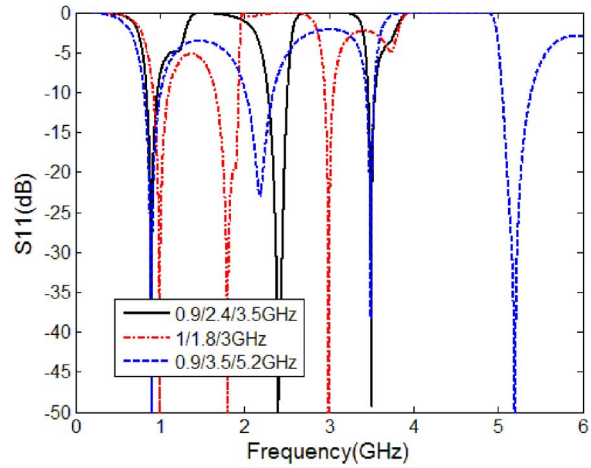

Fig. 12. Simulated $S11$ of three triple-frequency impedance transformers.

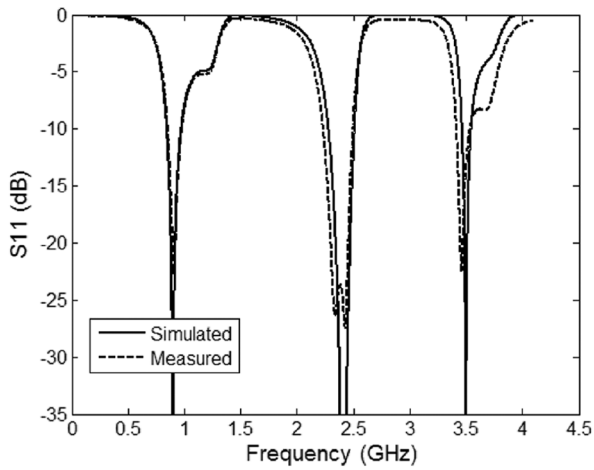

Fig. 13. Comparison betwee measured and simulated $S11$ of a triple-frequency impedance transformer ($f_1 = 0.9$ GHz, $f_2 = 2.4$ GHz, and $f_3 = 3.5$ GHz).

By adopting the genetic algorithm, we achieve the synthesized circuit parameters of the combined stubs for jB_{t1} and jB_{t2}, as listed in Table III.

Together with the above example, we give the data of three designs of triple-frequency impedance transformers, which have different matching frequencies. The data are given in Table IV.

Fig. 12 gives the simulated $S11$ plots of all three impedance transformers. Fig. 13 compares the simulated and measured $S11$ response of the 0.9/2.4/3.5-GHz triple-frequency impedance transformer. The 10-dB matching bandwidths are 127, 264, and 120 MHz. The experimental circuit is also fabricated on a Rogers 4003 substrate with a thickness of 0.508 mm, as shown in Fig. 14.

C. Quad-Frequency Impedance Transformers

Dealing with the same load, we give the design procedure of a quad-frequency impedance transformer whose four matching frequencies are specified as $f_1 = 0.9$ GHz, $f_2 = 1.7$ GHz, $f_2 = 2.4$ GHz, and $f_3 = 3.5$ GHz. The load impedances and

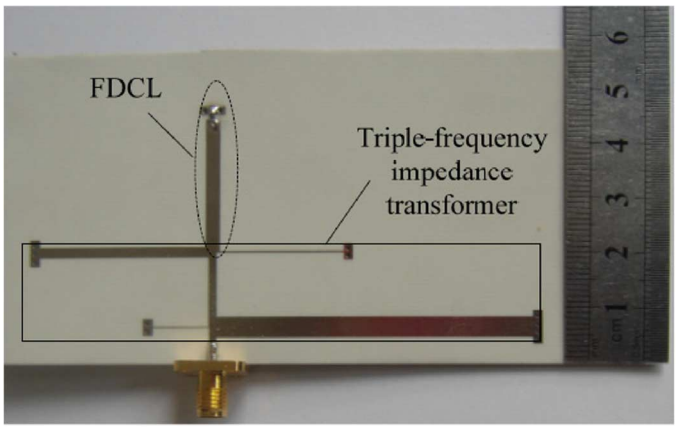

Fig. 14. Photograph of a triple-frequency impedance transformer: $f_1 = 0.9$ GHz, $f_2 = 2.4$ GHz, and $f_3 = 3.5$ GHz.

admittances at the four frequencies can be listed as follows:

$$Z_l(f_1) = 16.5138 - j25.0459 \quad Z_l(f_2) = 9.0626 - j2.3868$$
$$Z_l(f_3) = 11.6506 + j15.302 \quad Z_l(f_4) = 92.867 + j24.4581$$
$$Y_l(f_1) = 0.0183 + j0.0278 \quad Y_l(f_2) = 0.01032 + j0.0272$$
$$Y_l(f_3) = 0.0315 - j0.0414 \quad Y_l(f_4) = 0.0101 - j0.0027.$$

As a first step, we must choose the electrical length θ and characteristic impedance Z_c of the transmission line, which is a part of the multi-frequency J inverter. In practical design, we manually tried several different sets of θ and Z_c and compared the computed circuit parameters of the stubs and matching bandwidths, resulting in a relatively good selection (not "globally optimal") of electrical length given as follows:

$$\theta(f_4) = \frac{3\pi}{4}.$$

Considering the impedance matching at four frequencies, Z_c must satisfy

$$Z_{01} \le Z_{01\max} = \min_{i=1:4} \sqrt{\frac{1}{G_l(f_i) Y_0 \sin^2(\theta(f_i))}} = 24.177\ \Omega.$$

Here, we choose $Z_{01} = Z_{01\max} * 0.7 = 16.9\ \Omega$, which is also an "optimal" value selected from several tried values. To construct multi-frequency J inverters, the values of B_c are

$$B_c(f_1) = 0.0853 \quad B_c(f_2) = 0.0268 \quad B_c(f_3) = -0.0027$$
$$B_c(f_4) = -0.0591.$$

The J values can be computed as

$$J(f_1) = 0.1038 \quad J(f_2) = 0.0649 \quad J(f_3) = 0.0591$$
$$J(f_4) = 0.0836.$$

Correspondingly the values of B_1 and B_2 at the four frequencies should be

$$B_1(f_1) = -0.1255 \quad B_1(f_2) = 0.0781 \quad B_1(f_3) = -0.0258$$
$$B_1(f_4) = 0.0611$$
$$B_2(f_1) = -0.1065 \quad B_2(f_2) = 0.0204 \quad B_2(f_3) = -0.0427$$
$$B_2(f_4) = 0.1161.$$

TABLE V
STUB PARAMETERS FOR jB_{t1} AND jB_{t2} OF A QUAD-FREQUENCY IMPEDANCE TRANSFORMER (0.9 GHz/1.7 GHz/2.4 GHz/3.5 GHz)

Circuit block	Stub type	Characteristic Impedance	Electrical Lengths@0.9GHz
jB_{t1}	Open	94.07 Ω	45.11 Degree
	Short	42.33 Ω	24.91 Degree
jB_{t2}	Short	74.98 Ω	40.8 Degree
	Short	33.58	79.07 Degree

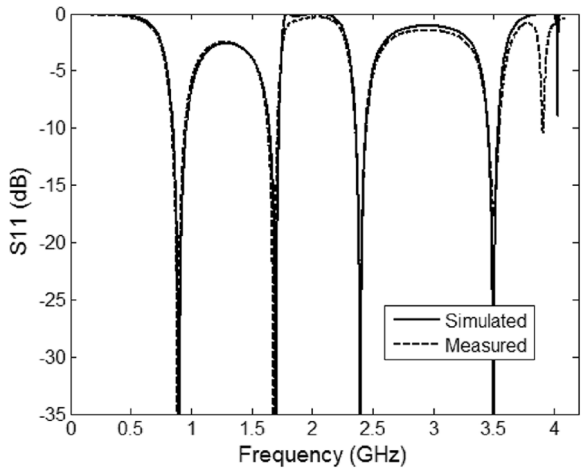

Fig. 15. Comparison between measured and simulated $S11$ of a quad-frequency impedance transformer ($f_1 = 0.9$ GHz, $f_2 = 1.7$ GHz, $f_3 = 2.4$ GHz, and $f_4 = 3$ GHz).

By merging the neighboring susceptances, we get

$$B_{t1}(f_1) = -0.0402 \quad B_{t1}(f_2) = 0.1049; B_{t1}(f_3) = -0.0258$$
$$B_{t1}(f_4) = 0.002$$
$$B_{t2}(f_1) = -0.0212 \quad B_{t2}(f_2) = 0.0472 \quad B_{t2}(f_3) = -0.0453$$
$$B_{t2}(f_4) = 0.057.$$

We use parallel stubs to realize the quad-frequency susceptance blocks of jB_{t1} and jB_{t2}, and the stub parameters are extracted using genetic algorithm and listed in Table V.

Fig. 15 gives the comparison of the measured and simulated $S11$ responses, and good agreement is achieved, showing good matching around the four frequencies. The 10-dB matching bandwidths are 110, 82, 92, and 85 MHz. The circuit is also fabricated on a Rogers 4003 substrate, as shown in Fig. 16.

Since the real and imaginary parts of the load impedance, as shown in Fig. 8, are not fully independent, we give a more arbitrary FDCL example in Fig. 17, consisting of an ATF54143 transistor [19]. The real and imaginary parts of load impedance Z_l are plotted in Fig. 18.

Again, to realize impedance matching for the load at four frequencies of $f_1 = 0.9$ GHz, $f_2 = 1.7$ GHz, $f_3 = 2.4$ GHz, and $f_4 = 3.5$ GHz, we firstly list the load impedances as follows:

$$Z_l(f_1) = 19.8 - j33.1 \quad Z_l(f_2) = 16.4715 + j0.9483$$
$$Z_l(f_3) = 21.1447 + j17.5625 \quad Z_l(f_4) = 48.515 + j39.48.$$

Following a similar procedure, we get a design of a quad-frequency impedance transformer, as shown in Fig. 17, and the parameters are listed in Table VI. We can find the simulated $S11$

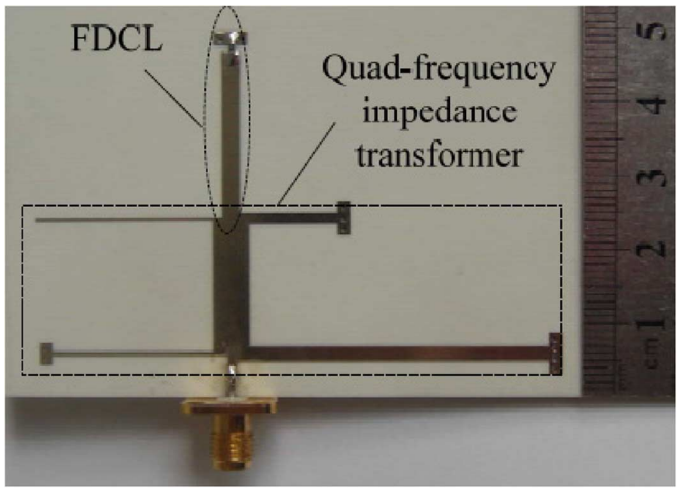

Fig. 16. Photograph of a quad-frequency impedance transformer: $f_1 = 0.9$ GHz, $f_2 = 1.7$ GHz, $f_3 = 2.4$ GHz, and $f_4 = 3.5$ GHz.

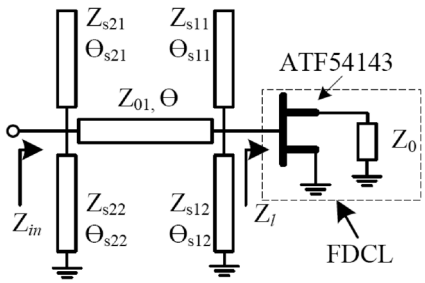

Fig. 17. Topology of a quad-frequency impedance transformer: $f_1 = 0.9$ GHz, $f_2 = 1.7$ GHz, $f_3 = 2.4$ GHz, and $f_3 = 3.5$ GHz (ATF54143 is biased with $V_{\rm ds} = 4.9$ V, $V_{\rm gs} = 0.37$ V and $I_{\rm ds} = 1.95$ mA).

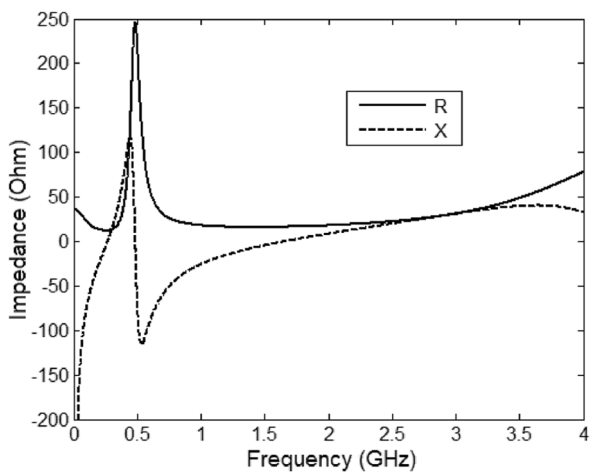

Fig. 18. Plots of load impedance Z_l of Fig. 17.

of this transformer in Fig. 19. The 10-dB matching bandwidths are 103, 90, 140, and 153 MHz.

D. Discussions

Some discussions are given based on the above design examples and the performance comparison between this work and the references, as listed in Table VII.

As a main advantage over the other techniques, this work gives a general design method of MFITs for FDCLs with no limitation in theory on the number of matching frequencies. To demonstrate this, a number of dual-, triple-, and quad-frequency design examples have been given. Moreover, it is able to increase matching frequencies by parallel combining more stubs, or by using stepped impedance stubs with more sections.

TABLE VI
CIRCUIT PARAMETERS OF A QUAD-FREQUENCY IMPEDANCE TRANSFORMER OF FIG. 17

Z_{01}	23.94 Ω	θ @f_4	160 Degree
Z_{s11}	64.51 Ω	θ_{s11}@f_1	39.1 Degree
Z_{s12}	49.62 Ω	θ_{s12}@f_1	35.27 Degree
Z_{s21}	71.8 Ω	θ_{s21}@f_1	40.2 Degree
Z_{s22}	82.23 Ω	θ_{s22}@f_1	24.11 Degree

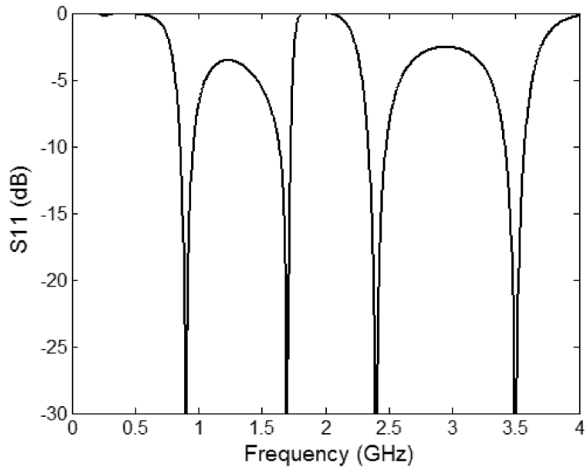

Fig. 19. Simulated $S11$ of a quad-frequency impedance transformer for the FDCL shown in Fig. 16.

TABLE VII
PERFORMANCE COMPARISON BETWEEN THE PROPOSED MFITs AND OTHER TECHNIQUES

Ref	Num. of Freq.	Load type	Num. of TLs	Max. freq. ratio of Examples	Design method*
This work	2/3/4	FDCL	3/5/5	3.3/5.7/3.9	A+O
[1]	2	Real	2	2	A
[2]	2	Real	2	2.7	A
[3]	2	Real	3	2	A
[4]	2	FDCL	3	2.3	A
[5]	2	FDCL	4	2.5	A
[6]	2	FDCL	3	2	A
[7]	2	FDCL	3	2.2	A
[8]	2	FDCL	4	2.9	A
[9]	2	Real	3	2	A
[10]	2	FDCL	5	2.4	A
[11]	2	FDCL	6	1.78	A
[12]	2/4	Real	N/A	2/8	A
[13]	2	FDCL	N/A	5	A
[14]	3	Real	N/A	3	A
[15]	4	Real	4	4.2	A
[16]	4	FDCL	4	4	O

*: "A" denotes analytical method, "O" denotes optimizing method.

The matching frequencies can be specified in a very wide range provided that the load impedances at the frequencies are not purely imaginary. As listed in Table VII, the maximum ratios between the matching frequencies of the dual-, triple-, and quad-frequency design examples are 3.3, 5.7, and 3.9, respectively.

As another important advantage, the technique provides concise and compact designs. In realizing a DFIT for FDCLs, this technique uses three sections of transmission lines, less than the designs of [5], [7], [10], and [11]. Moreover, in realizing the triple- and quad-frequency impedance transformers, we only add two stubs. Since the designed MFITs have only one section of transmission line in length, they are much shorter compared with many other solutions.

It is necessary to note that there are two reasons for the bulky dimensions of the designs of [10] and [11]. Firstly, dual-frequency offset lines are restricted to have the same identical characteristic impedance at two frequencies, and in fact, are redundant in function in realizing DFITs for FDCLs. Unlike this, dual-frequency inverters with no constraint to the identical J values are used in this work, resulting in less and simpler circuits. The MFIs have the same Pi-shaped topology, as shown in Fig. 1(b) for different numbers of frequencies, while we cannot find a general topology for multi-frequency offset lines. Secondly, the merging technique of circuits based on the so-called MFS concept is used in this work, minimizing the number of circuits, while in [10] and [11], different parts of the DFITs are separately designed and simply cascaded, with no circuit merging of parallel shunt parts. The two reasons are also why the topologies and design techniques of [10] and [11] cannot be easily extended for the design of MFITs with more matching frequencies.

We cannot easily compare the matching bandwidths between different works because the loads are quite different from each other, but as shown in the measured plots, the 10-dB matching bandwidths of the designed transformers in this paper are all larger than 80 MHz, always satisfying the RX or TX bandwidth requirement of any popular communication system, such as GSM900 and DCS1800. As we can observe, the matching bandwidths do vary very much for different loads and designs.

Besides the specified matching frequencies, in theory the transformers can realize impedance matching at any other frequencies if (14) and (15) can be satisfied by the designed branch circuits, such as stubs or combined parallel stubs. This is why there appear unexpected matching dips in the $S11$ plots of Figs. 9, 10, 12, and 15.

Moreover, large matching bandwidths could be obtained if the susceptance plots of the branch circuits over the frequency bands agree well with those generated from (14) and (15). We cannot simply control the matching bandwidths since practical loads differ from each other very much, but we have the chance to get optimal designs. Firstly, as the values of θ and Z_{01} vary, we will get new jB_{t1} and jB_{t2} from (14) and (15), together with new synthesis results of branch circuits, and it is possible to get better agreement between susceptance plots, and thus, larger matching bandwidths. Secondly, if θ, Z_{01}, jB_{t1}, and jB_{t2} are given, we also have design freedoms in synthesizing the branch circuits when the number of parameters is larger than the matching frequencies. For example, in designing triple-frequency susceptance circuits, we have three goal susceptance values, but four parameters of θ_{s1}, θ_{s2}, Z_{s1}, and Z_{s2}. Beside these, it is helpful to add some new circuits, and therefore, new design freedoms to the branch circuits for tuning the susceptance plots over the matching bands at the expense of larger dimensions.

By the way, we can observe from the design (Tables I–VI) that the characteristic impedances of the transmission lines and stubs are within a realizable range, guaranteeing practical implementation. Unrealizable characteristic impedances always can be avoided by choosing suitable values of θ and Z_{01}, which lead to realizable design.

It is unavoidable that practical difficulty will rise for the design of an MFIT as more matching frequencies are demanded, but impedance matching could be expected to be realized at ten or even more frequencies with parallel-stub MFSs, considering the aspects of circuit layout and parameter extraction. Five-stub MFSs will be used as N reaches ten, thus, the average angle between every two nearest lines (including the main transmission line and the stubs) will be about 52°, which will not deteriorate the matching performance very much as the characteristic impedances of the stubs or transmission line are not very low. Moreover, the junction effects of the MFSs can be compensated by slightly tuning related circuit parameters with the aid of electromagnetic (EM) simulation tools. We are fortunate that the numbers of practical unknowns and optimization goals are both reduced to $N/2$ in the genetic algorithm approach for parameter extraction of a parallel-stub MFS since enough analytical procedures are included into the algorithm. This can be explained by the described synthesis procedures of quad-frequency MFSs in Section II-C. Therefore, for $N = 10$, we only have five unknowns and five goals in designing an MFS, and the genetic algorithm could be expected to converge in reasonable time. The left five unknowns or parameters can be analytically computed after this.

The use of stepped-impedance stubs for MFSs will ease the layout of practical circuits, especially when N is becoming larger, but will also lead to an increased number of practical unknowns and increased difficulty in extracting the circuit parameters.

IV. Conclusions

A general topology and design theory has been proposed for MFIT design for FDCLs. Thanks to the adoption of MFIs, the method can be used to design MFITs, which can work on more than two frequencies. The MFS blocks are realized with stubs or combined structure of stubs. Several dual-, triple-, and quad-frequency impedance transformers are designed with the simulated and measured $S11$ plots compared. The matching frequencies can be increased by adding complexity to the MFS circuits.

The circuits are concise and compact with short length. The many design freedoms provide various possible designs, thus optimal matching bandwidths can be obtained and unrealizable designs can be avoided.

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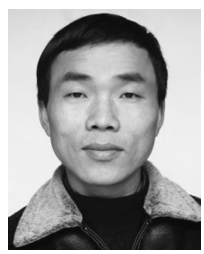

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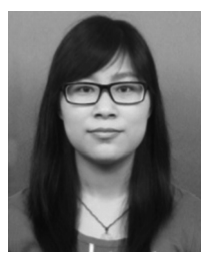

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