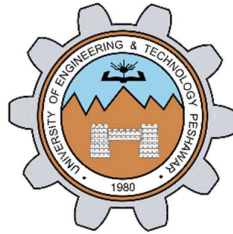


SR AND D FLIP FLOPS

LAB # 9



Fall 2023

CSE-202L Digital Logic Design Lab

Group Members:

Ahsan Raza (22PWCSE2099)

Hassan Zaib Jadoon (22PWCSE2144)

Mutahhar Fayyaz (22PWCSE2176)

Submitted to:

Dr. Rehmat Ullah Khattak

February 17, 2024

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

LAB # 9

SR AND D FLIP FLOPS

Flip-Flop:

The basic 1-bit digital memory circuit is known as flip-flop. It can store either 0 or 1. Flip-flops are classified according to the number of inputs.

SR Flip Flop:

An SR flip-flop, also known as a Set-Reset flip-flop, is a fundamental building block in digital electronics. It is a type of sequential logic circuit that stores one bit of data. The name "SR" stands for Set and Reset, which are the two fundamental operations it can perform.

The SR flip-flop typically has two inputs: Set (S) and Reset (R). When the Set input is activated (set to logic 1), the output of the flip-flop becomes 1, or "set". Conversely, when the Reset input is activated (set to logic 1), the output becomes 0, or "reset". Both inputs are usually active-low, meaning that they are triggered when set to logic 0.

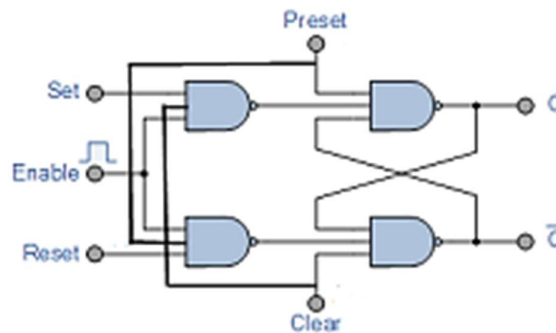


Figure 1: Logic Diagram

S	R	E	P	C	Q(t+1)
X	X	X	0	1	set
X	X	X	1	0	reset
X	X	0	1	1	No change
0	0	1	1	1	No change
0	1	1	1	1	Reset
1	0	1	1	1	Set
1	1	1	1	1	Indeterminate state

Table 1: Truth Table

D FLIP FLOP:

A D flip-flop, also known as a data or delay flip-flop, is another type of sequential logic circuit commonly used in digital electronics. It stores one bit of data and is often used for data storage, synchronization, and edge detection.

The D flip-flop has a single data input (D) and two control inputs: clock (CLK) and reset (often labeled as CLR or RESET). The behavior of a D flip-flop is such that the output (Q) reflects the value of the data input (D) at the moment the clock signal transitions from low to high (rising edge).

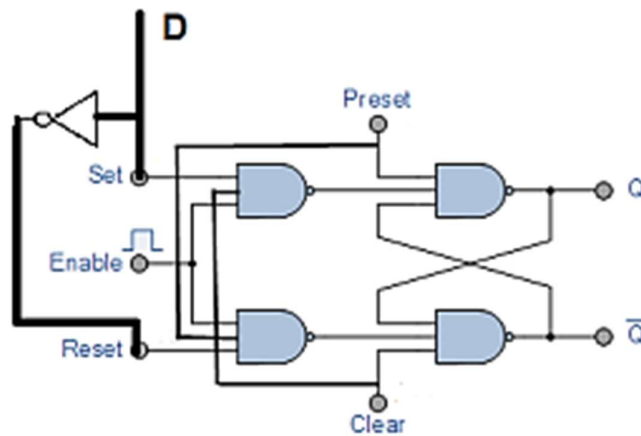


Figure 2:Logic Diagram

D	E	P	C	Q(t+1)
X	X	0	1	set
X	X	1	0	reset
X	0	1	1	No change
0	1	1	1	Reset
1	1	1	1	set

Table 2: Truth Table