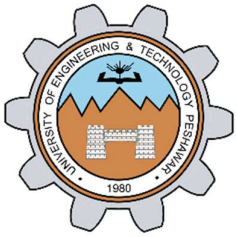
JK AND T FLIP FLOPS

LAB # 10



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CSE-202L Digital Logic Design Lab

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LAB # 10

JK AND T FLIP FLOPS

JK Flip Flop:

A JK flip-flop is a type of sequential logic circuit that is widely used in digital electronics for various applications such as frequency division, data synchronization, and memory storage. It has two inputs, labeled J (set) and K (reset), along with a clock input (CLK) and an optional asynchronous clear (CLR) input. The behavior of a JK flip-flop is similar to that of an SR flip-flop, but it addresses the problem of the undefined state present in SR flip-flops when both inputs are active simultaneously.

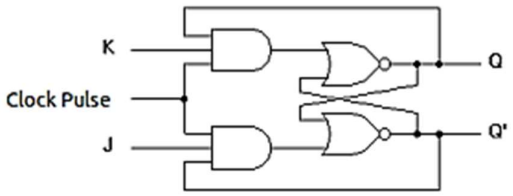

Figure 1:Logic Diagram

CP	**J**	**K**	**Q**(t+1)
0	X	X	No Change
1	0	0	No Change
1	0	1	Reset
1	1	0	Set
1	1	1	Toggle

Table 1: Truth Table

T Flip Flop:

A T flip-flop, also known as a toggle flip-flop, is a type of sequential logic circuit that is commonly used in digital electronics. It has a single input, labeled T (toggle), along with a clock input (CLK). The T flip-flop toggles its output state (Q) each time the clock signal transitions from low to high (rising edge) if the T input is set to 1.

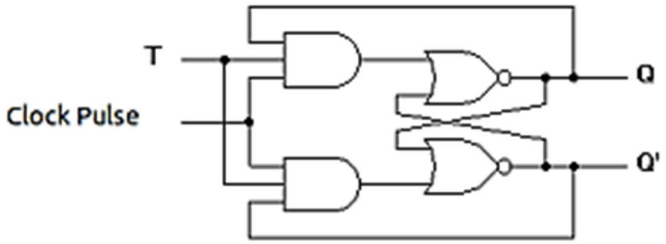

Figure 2: Logic Diagram

CP	**T**	**Q**(t+1)
0	X	No Change
1	0	No Change
1	1	Toggle

Table 2: Truth Table