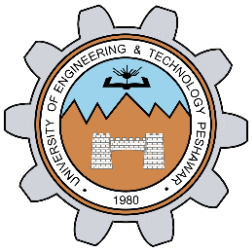
INTRODUCTION TO THE BASIS OF DIGITAL LOGIC GATES

LAB # 01



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CSE-202L: Digital Logic Design Lab

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LAB 01:

INTRODUCTION TO THE BASIS OF DIGITAL LOGIC GATES

Introduction:

Digital logic gates are the fundamental building blocks of digital circuits. These gates perform logical operations on one or more binary inputs and produce a single binary output, which is either 0 or 1. Understanding the behavior and functionality of these gates is essential for designing and analyzing complex digital systems.

Types of Digital Logic Gates

1. AND Gate:

Definition: An AND gate produces a high output (1) only when all its inputs are high (1). Otherwise, the output is low (0).

Truth Table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2. OR Gate:

Definition: An OR gate produces a high output (1) when at least one of its inputs is high (1). It produces a low output (0) only when all inputs are low (0).

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT Gate:

Definition: A NOT gate, also known as an inverter, produces the opposite binary state as its input. It converts 1 to 0 and 0 to 1.

Truth Table:

A	Y
0	1
1	0

4. NAND Gate:

Definition: A NAND gate is a combination of an AND gate followed by a NOT gate. It gives the opposite output of the AND gate.

Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR Gate:

Definition: A NOR gate is a combination of an OR gate followed by a NOT gate. It produces the opposite output of the OR gate.

Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

6. XOR Gate:

Definition: An XOR gate (exclusive OR) produces a high output (1) when the number of high inputs is odd.

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

EXPERIMENT

NOT GATE:

Figure:

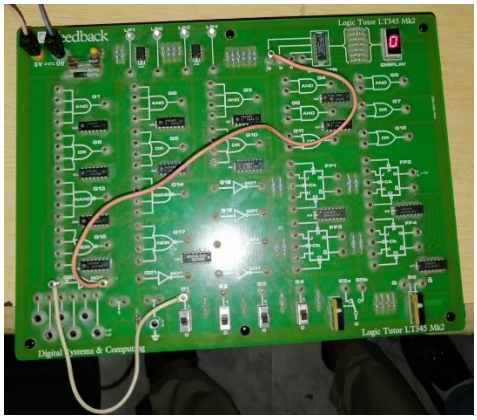

Figure 1: NOT Gate

Table:

Table 1: Truth Table for NOT Gate

A (High/Low)	Y (Volts)	Y (High/Low)
Low	4.85	High
High	0.08	Low

AND OR GATES:

Figures:

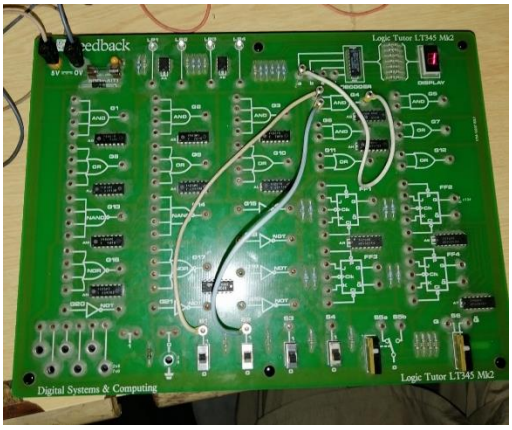

Figure 2: AND Gate

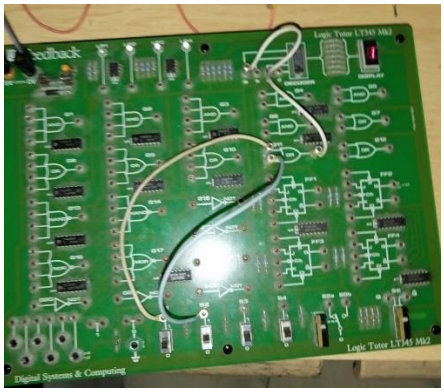

Figure 3: OR Gate

Table:

Table 2: Truth Table for AND & OR Gates

A (H/L)	B (H/L)	AND2 (V)	AND2 (H/L)	OR2 (V)	OR2 (H/L)
L	L	0.09	Low	0.09	Low
L	H	0.10	Low	4.79	High
H	L	0.09	Low	4.83	High
H	H	4.72	High	4.88	High

NAND, NOR, & XOR GATES

Figures:

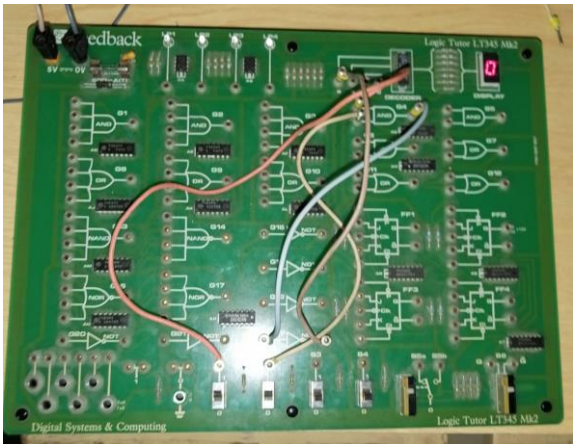

Figure 4: NAND Gate

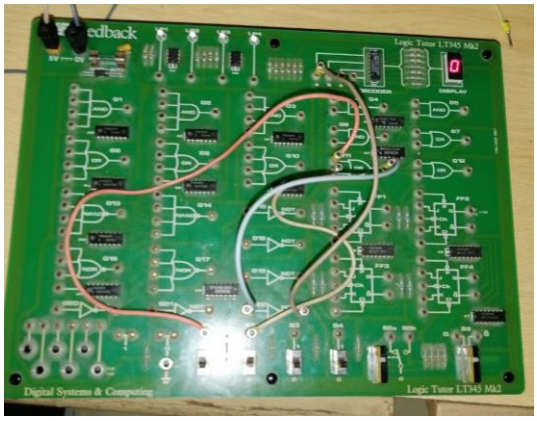

Figure 5: NOR Gate

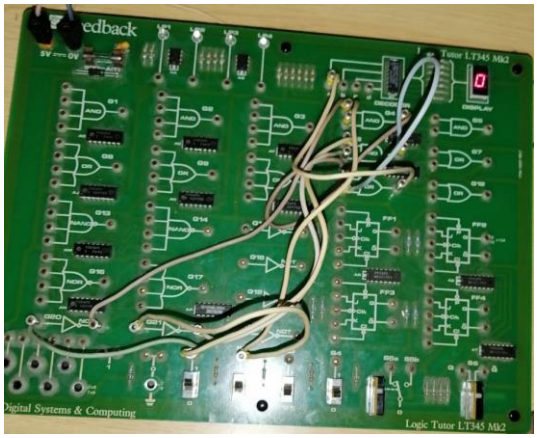

Figure 6: XOR Gate

Table:

Table 3: Truth Table for NAND, NOR, & XOR Gates

A (H/L)	B (H/L)	NAND2 (V)	NAND2 (H/L)	NOR2 (V)	NOR2 (H/L)	XOR2 (V)	XOR2 (H/L)
L	L	4.82	High	0.11	Low	0.095	Low
L	H	4.81	High	0.10	Low	4.94	High
H	L	4.74	High	0.09	Low	4.87	High
H	H	0.08	Low	4.74	High	0.09	Low