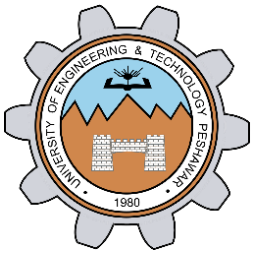
LAB # 07



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Registration Number: 22pwcse2144, 22pwcse2099, 22pwcse2176
Section: A

"On my honor, as a student of the University of Engineering and Technology, I have neithergiven nor received unauthorized assistance on this academic work."

Submitted to:

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Objectives of lab:

1. Design and construct a Decoder and an Encoder using logic gates.
2. Verify the truth tables of the Decoder and Encoder circuits using logic gates.
3. Understand the functionality of a Decoder and Encoder as a multiple-input, multiple-output logic circuit.

Theory:

Decoder:

A Decoder is a logic circuit converting coded input to coded output with a one-to-one mapping. It accommodates multiple inputs and produces multiple outputs, allowing 2^n possible output values. The block diagram illustrates 'n' inputs resulting in 2^n potential outputs.

Encoder:

An Encoder is the inverse of a Decoder, generating binary code corresponding to input values. It consists of 2^n input lines and 'n' output lines.
In this experiment, an octal to binary Encoder with eight inputs and three outputs was employed, assuming only one input has a value of one at any given time.

Components Required:

- Two 7410, 3 I/P NAND gate
- Three 7432, 2 I/P OR gate
- 7404 hex inverters

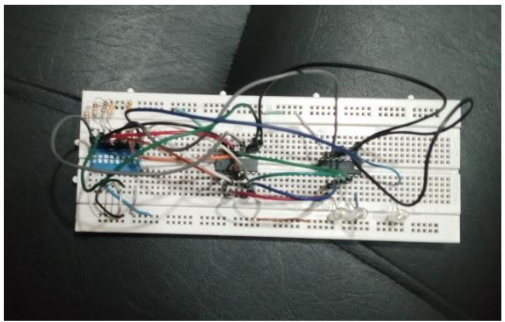
Procedure:

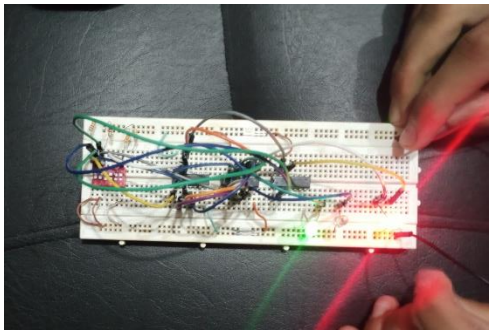
1. Establish connections based on the provided circuit diagrams.
2. Input logical values as specified in the circuit diagrams.
3. Observe the output and validate against the predefined truth tables.

Design a 3x8 Decoder using two 2x4 Decoders (74LS139).

To design a 3x8 Decoder using two 2x4 Decoders, connect the enable inputs of the second decoder to the complement of the enable input of the first decoder. The inputs of the second decoder are connected to the same input lines as the first decoder, and the outputs of both decoders are combined to form the final 3x8 Decoder.

Practical Diagram:





Figures:

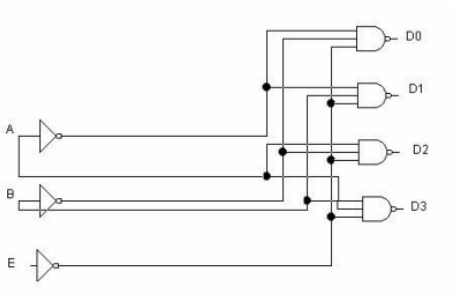


Figure1: Decoder

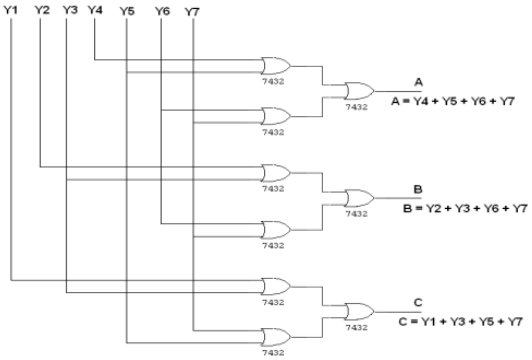


Figure: Encoder