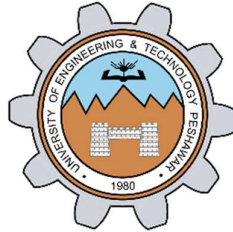


ADDER AND SUBTRACTOR

LAB # 05



Fall 2023

CSE-202L: Digital Logic Design Lab

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LAB NO. 05:

ADDER AND SUBTRACTOR

Objectives of lab:

- To design and construct half and full adder and subtractor.
- Verify the truth tables.

Components:

- Power Supply
- Breadboard. ICs 7408 (quad 2-input AND gate)
- 7432 (quad 2-input OR gate)
- 7404 hex inverter
- DIP Switch
- LED's

Half Adder:

A half adder is a fundamental digital circuit that adds two single-bit binary numbers to produce the sum and the carry.

$$S = A \oplus B$$

$$C = A \cdot B$$

Truth Table:

| A | B | Sum (S) | Carry (C) |
|---|---|---------|-----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Full Adder:

A full adder can handle three inputs: two operands (A and B) and a carry input (Cin), producing a sum output (S) and a carry output (Cout).

$$S=A\oplus B\oplus C_{in}$$

$$C_{out}=(A\cdot B)+C_{in}(A\oplus B)$$

Truth Table:

| A | B | C _{in} | Sum (S) | C _{out} (C _{out}) |
|---|---|-----------------|---------|--------------------------------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

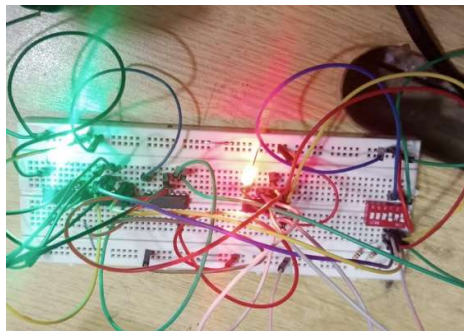


Figure 1: Full Adder

Half Subtractor:

A half subtractor is a combinational logic circuit that subtracts two single-bit binary numbers and computes both the difference (D) and the borrow (Borrow) output.

$$D=A\oplus B$$

$$\text{Borrow}=A'\cdot B$$

Truth Table:

| A | B | Difference (D) | Borrow (Borrow) |
|---|---|----------------|-----------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Full Subtractor:

It's an extension of the half subtractor, capable of handling three inputs: minuend bit (A), subtrahend bit (B), and borrow input

$$D = A \oplus B \oplus \text{Bin}$$

$$\text{Borrow} = (A \cdot B) + (A \cdot \text{Bin}) + (B \cdot \text{Bin})$$

Truth Table:

| A | B | Bin | Difference (D) | Borrow (Borrow) |
|---|---|-----|----------------|-----------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

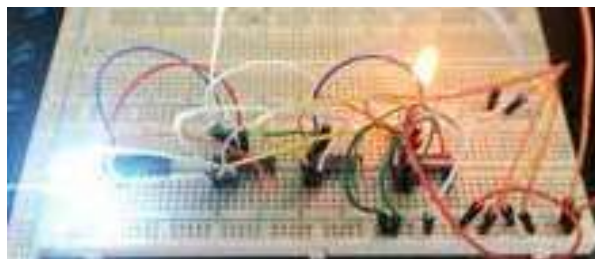


Figure 2: Full subtractor