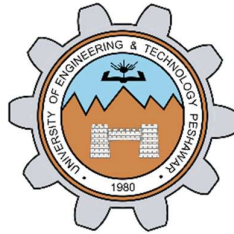# MULTIPLEXER AND DEMULTIPLEXER

LAB # 8

Fall 2023

CSE-202L Digital Logic Design Lab

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LAB # 8

MULTIPLEXER AND DEMULTIPLEXER

OBJECTIVES

- Create and build the Multiplexer and DeMultiplexer.

- Use simple logic gates to verify their truth tables.

COMPONENTS REQUIRED

- Two 7411, 3 I/P AND gates

- 7432, 2 I/P OR gate

- 7404, hex inverter

MULTIPLEXER:

Transmitting a large number of information units over a limited number of channels or lines is known as multiplexing. A combinational circuit known as a digital multiplexer is used to pick binary data from one of several input lines and route it to a single output line. A collection of selection lines determines which input line gets selected. The selection of an input is determined by the bit combination of n selection lines and n input lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.
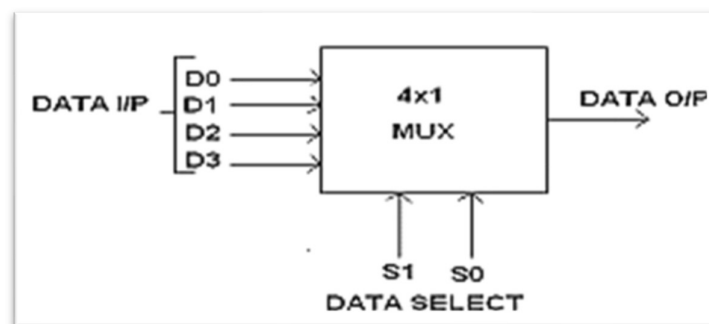

Figure 1:BLOCK DIAGRAM FOR 4x1 MULTIPLEXER

FUNCTION TABLE:

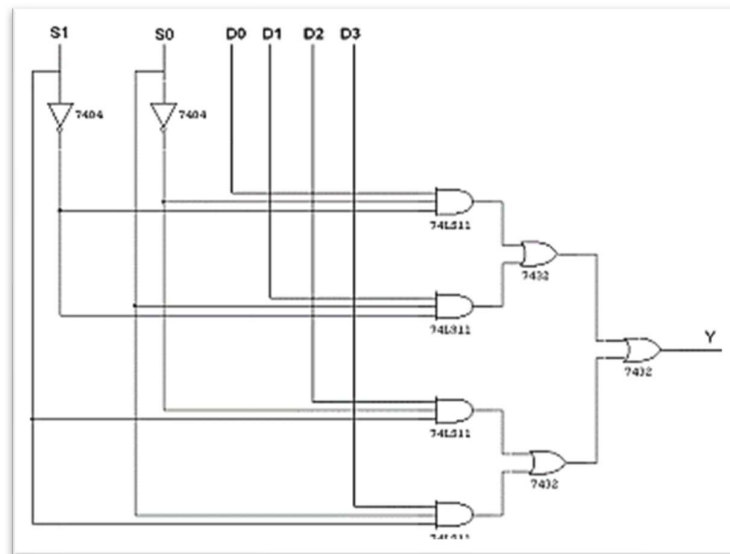| S1	S0	OUTPUT Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Figure 2:CIRCUIT DIAGRAM FOR 4x1 MULTIPLEXER

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It distributes data to a predetermined number of output lines from one line. The demultiplexer is sometimes referred to as a data distributor as a result. A demultiplexer can also be employed as a decoder.

In the 1x4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.
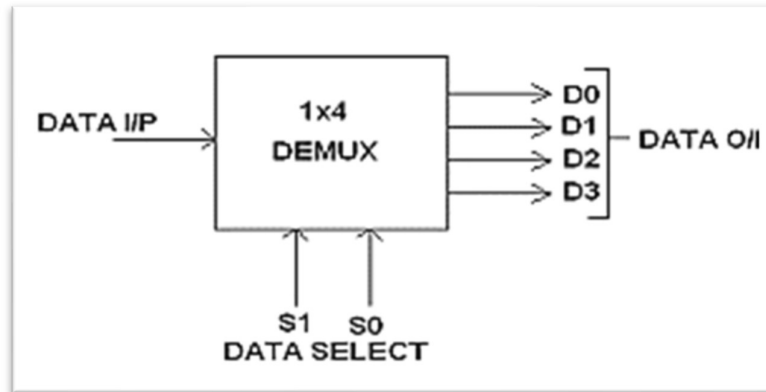
Figure 3:BLOCK DIAGRAM FOR 1x4 DEMULTIPLEXER

FUNCTION TABLE:

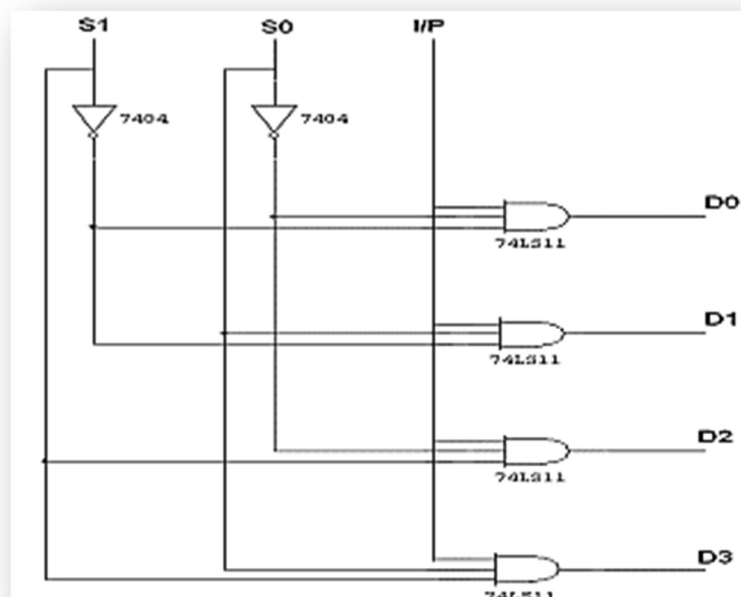| S1	S0	OUTPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Figure 4:LOGIC DIAGRAM FOR DEMULTIPLEXER