

LAB NO 09



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CSE-304L Computer Organization and Architecture Lab

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Introduction to MODELSIM and Gate-Level Modeling

Objectives:

- Introduction to MODELSIM software.
- Understanding the usage of MODELSIM for gate-level modeling and simulations.

MODELSIM:

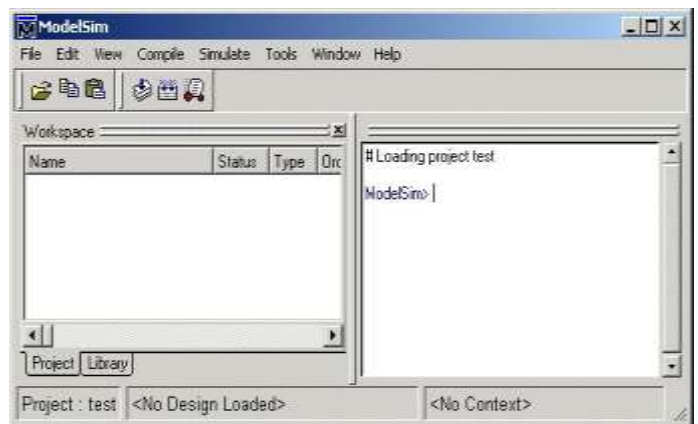
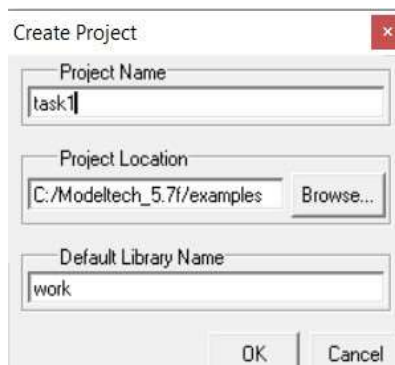
MODELSIM is a powerful simulation tool used for simulating designs written in VHDL or Verilog HDL. It allows users to visualize, debug, and test designs efficiently. The interface is user-friendly, providing an environment for both beginners and advanced users in hardware description language simulation.

How to Use MODELSIM:

Step 1: Creating a New Project

1. **Select** File > New > Project from the main window to create a new project. The **Create Project** dialog will appear, which includes the following options:
 - **Project Name:** Specify the name of your new project.
 - **Project Location:** Choose the directory where the .mpf file will be stored.
 - **Default Library Name:** Assign a working library name, typically left as "work."
2. Click **OK** to finalize the project creation. A blank **Project** tab will appear in the workspace, along with the **Add Items to the Project** dialog.

The name of your current project will be displayed at the bottom left corner of the **Main window**.



Step 2: Adding Items to the Project

In the **Add Items to the Project** dialog, there are several options:

- **Create New File:** Create new VHDL, Verilog, Tcl, or text files for your design.
- **Add Existing File:** Add an existing file to the project.
- **Create Simulation:** Define the source files and simulation configurations.
- **Create New Folder:** Organize your project files by creating folders.

To create a new file:

1. **File Name:** Enter the name for your new file.
2. **Add File as Type:** Choose the type of file (VHDL, Verilog, TCL, or text).

3. **Folder:** Choose the folder within the project where the file should be placed.

Click **OK**, and the Source window will open with an empty file, listed in the **Project** tab.

To add an existing file:

1. **File Name:** Browse and select the file you want to add.
2. **Add File as Type:** Select the file type (the default type is based on the file extension).
3. **Folder:** Specify the folder for the file.

You can choose whether to reference the file from its current location or copy it into the project directory.



Step 3: Compiling the Files

In the **Project** tab, files that have not been compiled are marked with a question mark. To compile the files:

1. Select **Compile > Compile All** or right-click the file in the **Project** tab and choose **Compile > Compile All**.

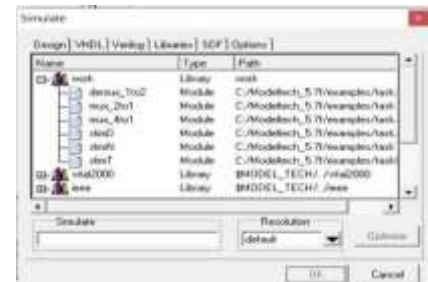
Once compiled, you can expand the **work** library in the **Library** tab to view the compiled design units.

Step 4: Simulating the Design

To simulate a design:

1. Double-click or right-click the design unit and select **Simulate**.
2. A new tab will appear showing the structure of the active simulation.

You can then add signals to the **Wave** window and run the simulation for a specified time. This allows you to analyze the results and verify the behavior of your design.



Program: Example for the module instantiation

