

EI331 COURSE PROJECT

By: Wang Haoxuan

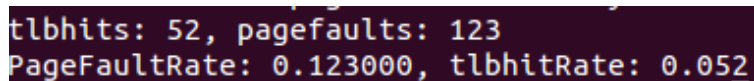
Instructor: Wu ChenTao

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I. PROJECT 8: DESIGNING A VIRTUAL MEMORY MANAGER

A. Introduction

This project consists of writing a program that translates logical to physical addresses for a virtual space. The whole structure is similar to the real structure in computer memory except that the memory and disk address are stored in a file. TLB and page table are requested to be implemented in this project. The algorithms in this program include demand paging, managing a TLB, and a page-replacement. At last, we would calculate the percentage of page faults TLB hit rate. The result is as follows:



```
tlbhits: 52, pagefaults: 123
PageFaultRate: 0.123000, tlbhitRate: 0.052
```

FIG. 1: Result for the Experiment

B. Implementation Details

In the program, we first construct a 2-D array to represent physical memory (256 by 256), a page table of size 256, a TLB page size of 16 and TLB frame num of 16. The transformation from logical address to physical address is quite simple, we just read from the .bin file to find such corresponding pairs. The difficulty lies in arranging the page table and the TLB. We adopted the FIFO method for the page replacement as well as TLB replacement.

There are few details to mention. The page size and the frame size are the same, thus we do not really have to care about the free page spaces as well as whether there is enough space left in the page table for the replacement of pages.

Also, the data in the .bin file is randomly placed in order, thus the time continuous and space continuous features are not significant. In this way, we do not expect high TLB hit rate, and the table fault rate is acceptable. Code is shown in the *code* file.