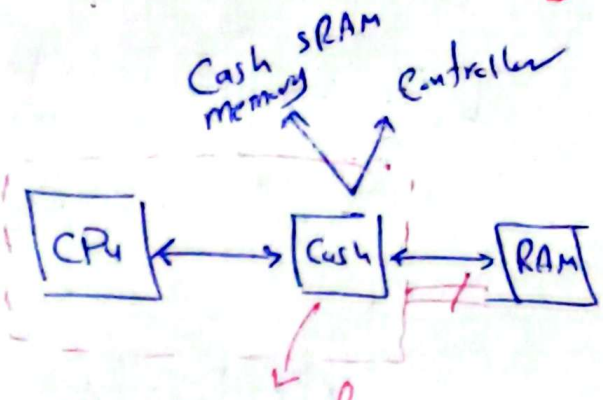
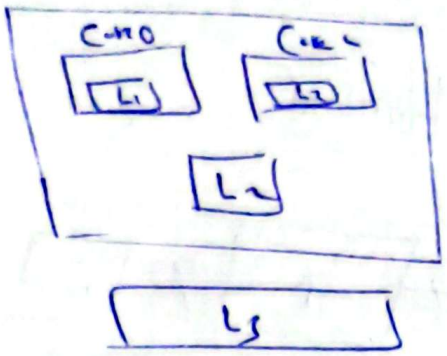
MCU - Architecture

Cashe memory → sRam



Read Block of memory

Hit miss



L1, L2, L3 : Cashe levels

* Cashe Coherence :- any change is updated within all cashes

$$\text{Hit ratio} = \frac{\#\text{hits}}{\#\text{total}}$$

FPU & mpu & mmu

FPU → Floating Point unit

Module deals with Floats

mpu → memory Protection unit

CPU ↔ Cash ↔ mPU ↔ Ram → Ranges

mmu → memory managment unit

APP → 8 GB

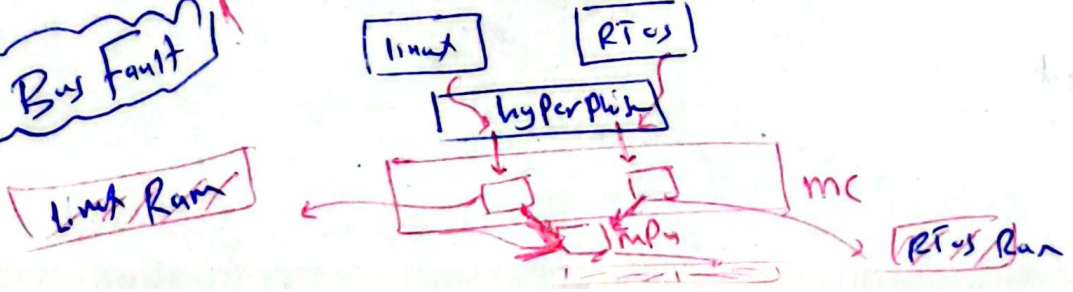
mP → mMu

Ram 1GB

only socket of 1GB

HDD

1. Bus Fault



I/O ⇒ interfacing

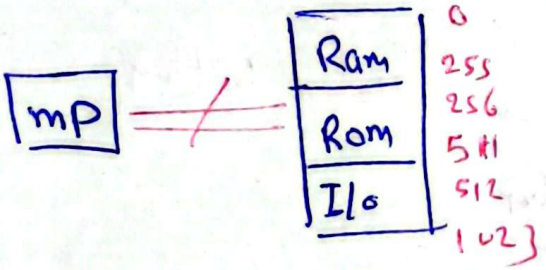
Bus set
- data
  - Rom & I/o — uni direct
  - Ram — Bidiration
- Address — uni direction
- Control — uni direction

Archecture

Von-neuman (PC)

memory mapped

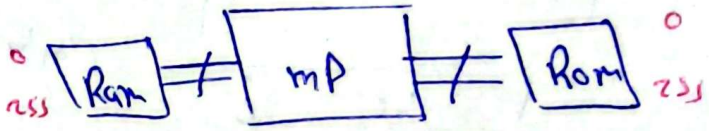
one memory system



* Can't Call Ram & Rom at Same time *

Harvard (MC)

Port mapped

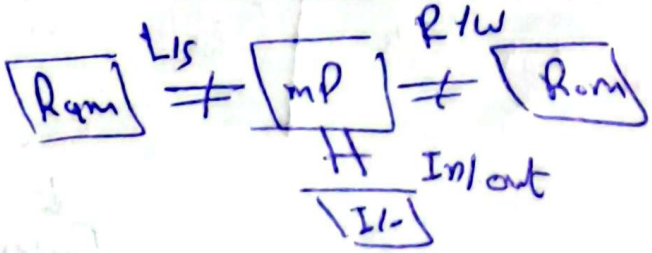


Software For Sam addrs

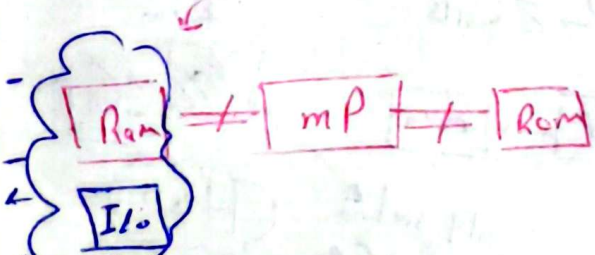
- Ram — Assembly: load/Store (C-lang)
- Rom — R\W

I/O (harvard)

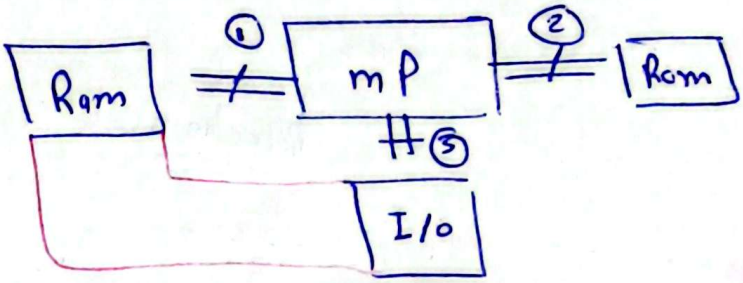
Port mapped



Memory mapped



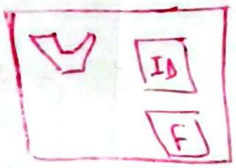
C-lang → load/store



Bus set 1: C-lang LIS

Bus set 3: Assembly I/O

PiPeline



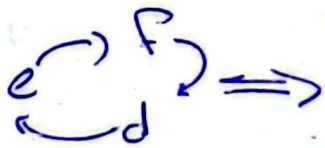
f d e
f d e
f d e
f d e
f d e

Cisc & Von-neumen → Can't support

Risc & Harvard only

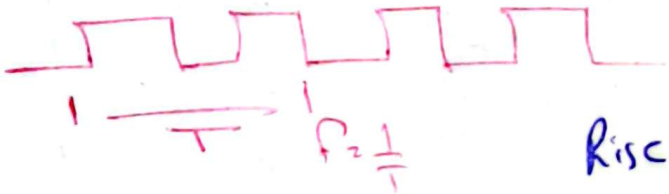
1-cycle

Inst



⟹ Clock

↳ square wave



$f = \frac{1}{T}$

Risc → inst. → 1 Cycle

8 mHz → 8 mIPs

Clock Systems

electrical

Rc - oscillator

Cost ↓ (↓)

Acc ↓

Settling time ↑

وقت الاستقرار

Noise:

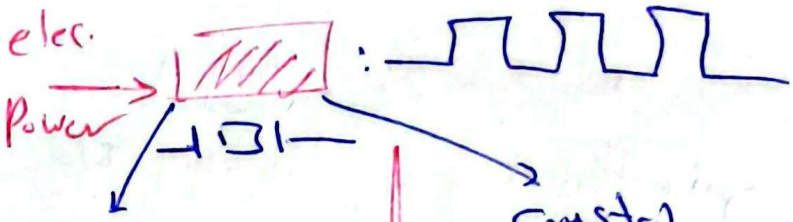
Temp X R↑

EmI X

Vibration ↓

Mechanical

material



Ceramic Resonator

Cost ~

Acc ~

Settling ~

Temp ↓

EmI ↓

Vib. X

Crystal oscillator

Cost ↑

Acc ↑ (↓)

Settling ↓ (↓)

Temp ↓

EmI ↓

Vib X

I/o interfacing

↓

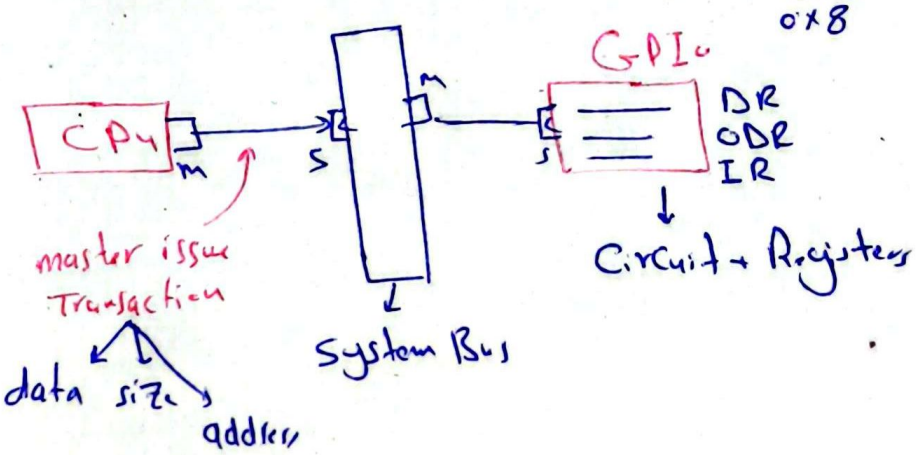
memory mapped → Ranges

GPIo

↓

Range = (Base + offset)
0x0 ↘ Register 0x0, 0x4, 0x8

digital design



Specs [TRM]

Bus Bridges