CSE271 Section 2
Introduction to Digital Systems

Lecture 31

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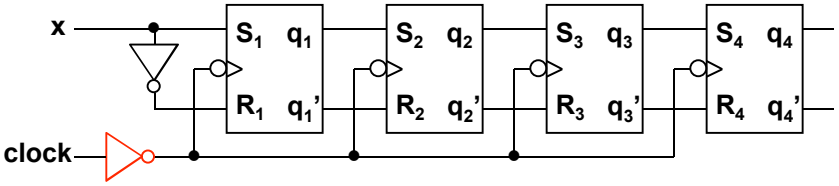
Shift Registers

- A register is a collection of flip flops, with a common name and a common clock.
- Shift register -- data moves one place to the right on each clock or shift input.

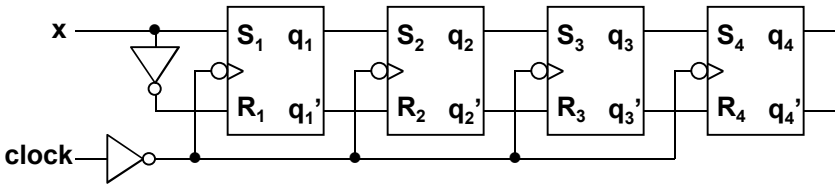


Red NOT gate

- Leading-edge triggered shift register
- Circuit presents a load of 1 to the clock, rather than a load of 4.

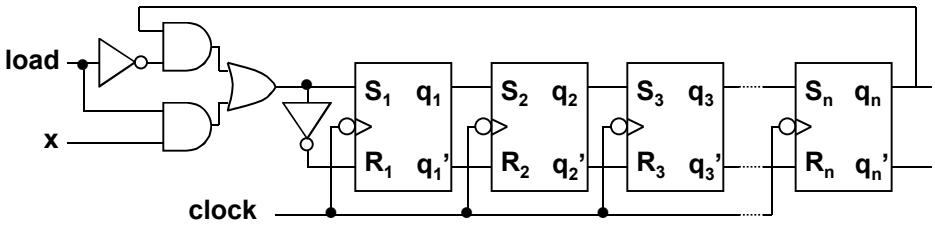
Serial-in Serial-out Shift Register

Only 1 bit (at left) may be loaded into the register at a time and only 1 bit (at right) may be read.



x	1	0	1	1	1	0	1	1	1	1	0	0	0		
q_1	0	1	0	1	1	1	0	1	1	1	1	0	0	0	
q_2	0	0	1	0	1	1	1	0	1	1	1	1	0	0	0
q_3	0	0	0	1	0	1	1	1	0	1	1	1	1	0	0
q_4	0	0	0	0	1	0	1	1	1	0	1	1	1	1	0

Application: Shift Register Storage



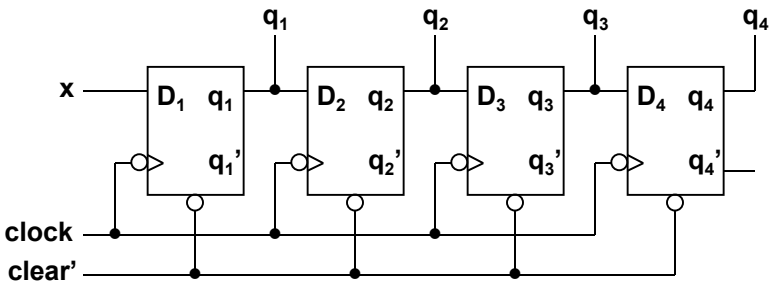
When load=0, the data circulate around the n flip flops.

Data is available only at q_n, once every n clock cycles.

When load=1, x can be stored into q_1.

To initialize register to all 0's, we can let x=0 and load=1 for n clock cycles.

Serial-in Parallel-out Shift Register



D flip flop implementation.

We can initialize the register using clear' input.

Application: input port from modem
(converting serial data to parallel data).

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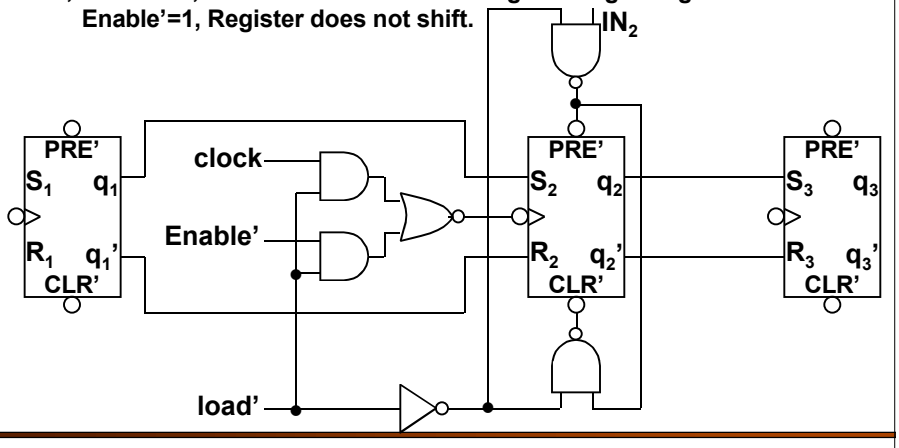
Parallel-in Serial-out Shift Register

If load'=0, IN_2=0, then PRE'=1 and CLR'=0, q_2=0. (static loading)
IN_2=1, then PRE'=0 and CLR'=1, q_2=1.
If load'=1, Enable'=0, then clock is inverted and go through. Register shifts.
Enable'=1, Register does not shift.



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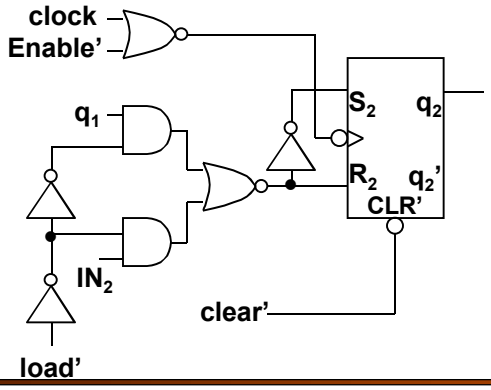
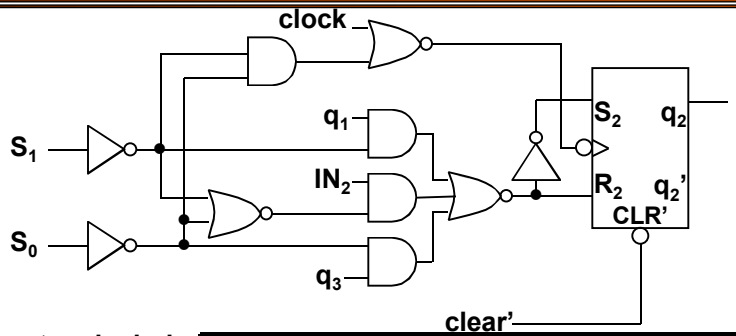
Parallel-in Serial-out Shift Register

There is an independent active low static clear.
When Enable'=0, clock is inverted and go through.
When Enable'=0 and load'=0, IN_2 is stored into q_2.
When Enable'=0 and load'=1, q_1 is shift into q_2.



Load is done synchronously.

Right/Left Shift Register



Most computers include both left/right shift and rotate instructions. Right/left shift register can shift the stored bits in both directions.

	Clear'	S_0	S_1	q_1^*	q_2^*	q_3^*	q_4^*
Static clear	0	X	X	0	0	0	0
Hold	1	0	0	q_1	q_2	q_3	q_4
Shift left	1	0	1	q_2	q_3	q_4	LS
Shift right	1	1	0	RS	q_1	q_2	q_3
Load	1	1	1	IN_1	IN_2	IN_3	IN_4

Application of Right/Left Shift Register

- Typically used in ALU for better performance
  - Multiplied by 2 can be done by one-bit shifting left.
    - 4*2: 0100 shift left one bit and get 1000 (8).
  - Divided by 2 can be done by one-bit shifting right.
    - 4/2: 0100 shift right one bit and get 0010 (2).