Hatim Kanchwala

BORN ON 7ᵀᴴ FEBRUARY 1995 IN INDORE, INDIA

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AUSBILDUNG

Apr. 2019 – Sept. 2022 *Aachen, Germany*	**M. Sc. Electrical Engineering, Information Technology and Computer Engineering** *RWTH Aachen University* *Abschlussnote 2,1* Field-Programmable Gate Array based Real-Time Control and Simulation
July 2014 – May 2018 *Bihta (Patna), India*	**B. Tech. Electrical Engineering** *Indian Institute of Technology Patna* *Abschlussnote 7.32 / 10* Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation

BERUFSERFAHRUNG

M. Sc. Thesis "Field-Programmable Gate Array based Real-Time Control and Simulation"

Apr. 2021 – Dec. 2021
Aachen, Germany

IEK-10, Forschungszentrum Jülich & Institute for Automation of Complex Power Systems

- Developed design using soft-core microprocessors to rapidly prototype control-loop algorithms for FPGA-based real-time simulators of power systems and to allow independent formulation of power system and control-loop models.
- Introduced *control* and *data-logger* soft-cores, each based on MicroBlaze soft-core microprocessor from Xilinx and implemented on Xilinx Virtex Ultrascale+ VCU118 board, respectively dedicated to running control algorithms at switching frequency and logging simulation data at each time step.
- Conceptualised heterogenous architecture using multiple and dedicated soft-core microprocessors, enabling hierarchical control-loop systems and fine-grained administration of real-time simulation.
- Assembled final work product using combination of proprietary Xilinx IPs from Vivado IP Integrator, HLS modules of power systems generated from ORTiS, self-authored Verilog RTL modules and binaries for soft-core microprocessor using Xilinx SDK.

Student Intern

Oct. 2020 – Feb. 2021
Remote

IEK-10, Forschungszentrum Jülich

- Implemented power sytems models using open-source code-generation tool ORTiS targeted toward High-Level Synthesis for RTL co-simulation and real-time simulation on an FPGA. Extended HLS models with memory-mapped AXI4 register interface. Verified hardware models on Xilinx Virtex-7 VC707 FPGA board using remote debugging.
- Developed Makefile pipeline on Linux for ORTiS code generation, Vivado High-Level Synthesis, Vivado IP Integrator and FPGA bitstream generation stages.

Student Assistant

May 2019 – Sept. 2020
Aachen, Germany

Institute for Automation of Complex Power Systems, E.ON Energy Research Centre

- Integrated Xilinx FPGA development boards into VILLAS co-simulation platform by designing an architecture built on top of Aurora 8B/10B serial protocol from Xilinx, thereby providing a consistent interface between CPU, over PCIe, and real-time simulators, over physical fibre link.
- Engineered Tcl-Makefile system of scripts to simplify file management of multiple source types and binary files and streamline project management using revision control systems. Developers could utilise system to collaborate on version-agnostic local toolchains and significantly reduce commit and check-out sizes.
- Implemented memory-mapped AXI4 register interface wrapper around Aurora 8B/10B by extending corresponding Xilinx Baremetal drivers in C/C++.

Senior Research Fellow

May 2018 – Nov. 2018
Control and
Instrumentation Lab, IIT
Patna, India

"Underwater Target Motion Analysis with Passive Sensors"

- Implemented advanced filters, like Distributed Extended Kalman Filter, Shifted Rayleigh Filter, Particle Filter with compound proposals, Particle Filter with MCMC, and Regularised Particle Filter, for the Bearings-only Tracking problem in MATLAB.
- Simulated performance of these filters on actual field manoeuvres provided by sponsor, and prepared comparative study as measured by time, resource and computational complexities, and target tracking accuracy.
- Concluded that Shifted Rayleigh Filter outperforms other filters in terms of computational complexity while still being superior at tracking target.

Aug. 2017 – May 2018 *IIT Patna, India*	**B. Tech. Thesis	Nominated for Best B. Tech. Thesis award from Dept of Electrical Engineering** *"Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"*

- Designed and implemented a parallel architecture of Sigma-point Kalman filtering algorithms on an FPGA by independently conceptualised parallel routine for Cholesky decomposition in $\mathcal{O}(N)$ time complexity.
- Further optimised resource usage of parallel Cholesky decomposition architecture for maximum processor utilisation to achieve $\mathcal{O}\left(\frac{1}{4}N^2\right)$ resource complexity, as compared to $\mathcal{O}\left(\frac{1}{2}N^2\right)$ resource complexity of state-of-the-art.
- Implemented parallel architectures using Verilog HDL and Xilinx Vivado on Xilinx Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards, making use of open-source floating-point IPs and Xilinx Vivado IPs.
- Presented final work product to the professors of the department and was one of only two students to receive unanimous 10 / 10 grade from cohort of 50 candidates.

May 2017 – Aug. 2017 *Google Summer of Code* *2017*	**Student Developer, "EDSAC Museum on FPGA"	Presented at ORConf 2017 digital design conference** *Free and Open Source Silicon Foundation*

- Built Verilog model of historic EDSAC computer from original but incomplete documentation in collaboration with members of "The EDSAC Replica Project" team (TNMOC, Bletchley Park, UK).
- Programmed and simulated EDSAC architecture and ISA on myStorm Lattice iCE FPGA board using open-source toolchains, like Yosys and iverilog.
- Coordinated with team of younger students in UK to build hardware imitation of EDSAC memory delay line, teleprinter and paper tape reader.
- Demonstrated final work product at ChipHack 2017 workshop and presented at ORConf 2017 digital design conference in Hebden Bridge, UK, for which full sponsorship was received.

Feb. 2016 – Aug. 2016 *Google Summer of Code* *2016*	**Student Developer, "Read/Write Multiple Status Registers and Lock/Unlock Memory on SPI Chips"** *Coreboot (Flashrom)*

- Designed unified abstraction of multiple status registers in SPI Flash-memory chips to provide consistent interface between flashrom and diverse chip manufacturers.
- Programmed routines to lock/unlock memory space governed by status registers, handle configuration bits, access/lock OTP memory areas, and automatically generate memory protection maps.
- Developed CLI to expose these features, and tested infrastructure using Raspberry Pi and Teensy development board.
- Liaised with Sales Executive of GigaDevie from China to arrange for engineering samples and add support for GigaDevice SPI chips.

KENNTNISSE

Programmierung	Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS
Software	Xilinx Vivado & HLS, MATLAB, Simulink, RSCAD, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, LaTeX, gnuplot
Hardware	Xilinx Virtex & Zynq SoC, Digilent Nexys4 DDR, RTDS NovaCor, Raspberry Pi, Arduino, PIC Microcontroller
Sprachen	English (*TOEFL 114/120*), Deutsch (*B1*), Hindi (*native*)

EXTRACURRICULAR ACTIVITIES

Faiz al-Mawaid al-Burhaniyah (FMB)
Aachen, Germany
Volunteer
June 2021 – Apr. 2022

- Co-founded Aachen chapter of FMB and led team of volunteers with vision to provide home-cooked and healthy meals to students in and around Aachen at least once a week.
- Organised meal distribution drives on festive occasions, especially Ramadan, to celebrate cultural identity and increase community engagement.
- Co-developed low-cost, sustainable standard operating model to make community effort scalable and reproducible at other locations.

Training and Placement Cell
IIT Patna, India
Assistant Head Coordinator, Dept of Electrical Engineering
Apr. 2017 – Apr. 2018

- Selected by class majority to represent students of Dept of Electrical Engineering.
- Led team in designing placement brochures and helped arrange on-campus placement sessions, tests and interviews.

Startup Relations, Entrepreneurship Club
IIT Patna, India
Coordinator
Apr. 2016 – Apr. 2017

- Led Startup Relations department and served as mentor to early-stage on-campus startups to help develop business plans, choose investor strategies and network with advisors.
- As part of Core Committee, oversaw the organisation of E-Week 2017, the annual national-level event of Entrepreneurship Club.
- Delivered presentations as part of In-house Mentorship Lecture series based on individual technical and business experience in early-stage startups.

Task Manager
Apr. 2015 – Apr. 2016

- Recruited volunteers and helped organise pitching events, workshops and guest talks.
- Assisted in establishing panel of early investors and mentors for on-campus startups.