Hatim Kanchwala

Pre-final Year • Undergraduate • Electrical Engineering • Indian Institute of Technology Patna
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INTERESTS

Computer Organisation & Architecture • Embedded Systems Design • Adaptive Filters • Neural Networks • Entrepreneurship

SKILLS

PROGRAMMING

C/C++ • Assembly • Verilog • JavaScript • Python • HTML/CSS • LaTeX • Shell • Java • Scala

SOFTWARE

GNU/Linux • git/GitHub • MATLAB • Simulink • Xilinx ISE • Multisim • Synopsys • Pyxis • MPLAB IDE • Proteus • NumPy/SciPy • Eclipse IDE

HARDWARE

Xilinx Spartan FPGA • PIC Microcontroller • TMS320 DSP Chip • Arduino • 8051 Microcontroller • Raspberry Pi • Teensy

LANGUAGES

English • Hindi • Gujarati • Marathi • Urdu • Arabic

EDUCATION

INDIAN INSTITUTE OF TECHNOLOGY PATNA

B. Tech. in Electrical Engineering
2014 - 2018 • Bihta (Bihar), India
CPI: 7.59 / 10.0 (upto 5th semester)

PROJECTS

FPGA IMPLEMENTATION OF NLMS ADAPTIVE FILTERING ALGORITHM FOR SIGNAL ENHANCEMENT

FEB. 2017 - PRESENT • hatimak/zephyr
Adviser - Dr Yatendra Kumar Singh

- Implementing Normalized Least Mean Squares (NLMS) adaptive filtering algorithm to extract desired audio from corrupted signal with additive autoregressive noise.
- Prototyping on Xilinx Spartan-3E FPGA in Verilog HDL, with focus towards optimised placing and routing.
- Investigating performance gain by FPGA over typical DSP chip (TMS320).

8085 INSTRUCTION SET ARCHITECTURE PROTOTYPE ON FPGA WITH BASIC PIPELINING

JAN. 2017 - PRESENT • hatimak/marineford
Adviser - Dr Kailash Chandra Ray

- Implementing Intel 8085 microprocessor ISA on Xilinx Spartan-3E FPGA in Verilog HDL. Developing ASM testbenches to investigate performance gain due to pipelining.

FLASHROM

FEB. - AUG. 2016

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FINGERPRINT BASED REMOTE ATTENDANCE SYSTEM

JAN. - OCT. 2015 • hatimak/den-den-mushi

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MINI PROJECTS

8085 INSTRUCTION SET ARCHITECTURE PROTOTYPE ON FPGA WITH BASIC PIPELINING

JAN. 2017 - PRESENT • hatimak/marineford
Guide - Dr Kailash Chandra Ray

- Implementing Intel 8085 microprocessor ISA on Xilinx Spartan-3E FPGA in Verilog HDL. Developing ASM testbenches to investigate performance gain due to pipelining.

FULL-CUSTOM DESIGN OF RING OSCILLATOR

NOV. 2016 • hatimak/ring-osc

- Designed core layout of ring oscillator using AMI05 (0.5 µm) CMOS Technology in Pyxis (Mentor Graphics), and verified output of back annotated simulation.

COURSEWORK

UNDERGRADUATE

Digital Electronics & Microprocessors
Embedded Systems
VLSI Design
Semiconductor Devices & Circuits
Analog Integrated Circuits
Digital Signal Processing
Control Systems
Communication Systems
Electromagnetic Theory
Electronic Instrumentation
Electrical Power Systems
Electrical Machines
Linear Algebra
Probability & Random Processes
Algorithms & Data Structures

MOOC

Machine Learning
Principles of Valuation: Risk & Return
Principles of Valuation: Time Value of Money

EXPERIENCE

AFICIONADO VENTURES • Backend Engineer

Startup • FEB. 2016 - OCT. 2016 • Gurugram (Haryana), India

- Purchasing platform connecting restaurants and vendors - helping restaurants procure better quality raw ingredients and products at competitive prices from extensive & diverse collection of vendors.
- Designed asset-light reactive scalable backend architecture for marketplace platform. Used MeteorJS for server, MongoDB for data storage, GitHub for code collaboration, Heroku for web app hosting, mLab for database hosting, and Cordova for cross-platform mobile apps.
- Implemented MVP-stage marketplace platform with bilingual search to look up products in English/Hinglish. Started work on machine learning engine for vendor inventory prediction and predictive restaurant purchase order generation. Proposed and prototyped conversational UX via messaging bot, in lieu of app interfaces.

WEAVE • Co-founder & Product Developer

Startup • JUNE 2015 - DEC. 2015 • Patna (Bihar), India

- Implemented basic prototype of Model Generator in JavaScript - based on user input data and features, Model Generator builds 3D NURBS model of user's body using weighted combination of precomputed basis models.
- Developed model of Cloth Physics Engine that emulates dyanmics for clothes fitted on generated NURBS model - users can try clothes virtually.
- Despite garnering client & investor interest, startup failed because product-market fit was not right.

EXTRACURRICULAR

COORDINATOR, STARTUP RELATIONS • Entrepreneurship Club, IIT Patna

APR 2015 - PRESENT

- Serving as on-campus mentor to early stage startups, helping entrepreneurs develop business plan, choose investor strategy, and network with domain experts.
- Responsible for building connections with startups and investors, and building investor panel for on-campus startups.
- Part of Core Committee for E-Club's flagship annual event, E-Week. Responsible for organizing guest talks, workshops and pitching event in collaboration with Incubation Centre, IIT Patna.