

# Hatim Kanchwala

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## Ausbildung

Apr. 2019 – Sept. 2022  
Aachen, Deutschland

### M. Sc. Elektrotechnik, Informationstechnik und Technische Informatik

RWTH Aachen Universität

Abschlussnote 2,1

- Masterarbeit "Field-Programmable Gate Array basierte Echtzeitregelung und -simulation"

Juli 2014 – Mai 2018  
Bihta (Patna), Indien

### B. Tech. Electrical Engineering

Indian Institute of Technology Patna

Abschlussnote 7.32 / 10 (indische) = 2,1 (deutsche)

- Bachelorarbeit "Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"

## Berufserfahrung

Apr. 2021 – Dez. 2021  
Aachen, Deutschland

### Masterarbeit "Field-Programmable Gate Array basierte Echtzeitregelung und -simulation"

Institut für Energie- und Klimaforschung (IEK-10) am Forschungszentrum Jülich GmbH

- Developed design using soft-core microprocessors to rapidly prototype control-loop algorithms for FPGA-based real-time simulators of power systems and to allow independent formulation of power system and control-loop models.
- Introduced *control* and *data-logger* soft-cores, each based on MicroBlaze soft-core microprocessor from Xilinx and implemented on Xilinx Virtex Ultrascale+ VCU118 board, respectively dedicated to running control algorithms at switching frequency and logging simulation data at each time step.
- Konzipierte eine heterogene Architektur mit mehreren speziellen Soft-Core-Mikroprozessoren, die hierarchische Regelkreissysteme und eine detailliertere Verwaltung der Echtzeitsimulation ermöglicht.
- Assembled final work product using combination of proprietary Xilinx IPs from Vivado IP Integrator, HLS modules of power systems generated from ORTiS, self-authored Verilog RTL modules and binaries for soft-core microprocessor using Xilinx SDK.

Okt. 2020 – Feb. 2021  
Home Office

### Praktikant

Institut für Energie- und Klimaforschung (IEK-10) am Forschungszentrum Jülich GmbH

- Implementierte Stromnetzmodelle mit dem Open-Source-Code-Generierungstool ORTiS, das auf High-Level-Synthese für RTL-Co-simulation und Echtzeitsimulation auf einem FPGA ausgerichtet war.
- Erweiterte HLS-Modelle mit memory-mapped AXI4-Register-Interface. Verifizierte Hardware-Modelle auf Xilinx Virtex-7 VC707 FPGA-Board mit Remote-Debugging.
- Entwickelte Makefile-Pipeline unter Linux für ORTiS-Code-Generierung, Vivado High-Level Synthesis, Vivado IP Integrator und FPGA-Bitstream-Generierung.

Mai 2019 – Sept. 2020  
Aachen, Deutschland

### Studentische Hilfskraft

Institute for Automation of Complex Power Systems, E.ON Energy Research Centre

- Integrierte Xilinx-FPGA-Boards in die VILLAS-Cosimulations-Plattform durch den Aufbau einer Architektur auf dem seriellen Aurora 8B/10B-Protokoll.
- Entwickelte ein Tcl-Makefile-System mit Skripten zur Automatisierung der Design-Generierung und Bitstream-Kompilierung.
- Entwickelte Bare-Metal-Driver-Programme in C/C++ für FPGA-Firmware.

Mai 2018 – Nov. 2018  
IIT Patna, Indien

## Senior Research Fellow

“Underwater Target Motion Analysis with Passive Sensors”,  
Naval Physical & Oceanographic Laboratory (DRDO), Ministry of Defence, Govt of India

- Implementierte fortgeschrittene Tracking-Filter in MATLAB für das Bearings-only Tracking-Problem.
- Simulierte die Leistung von modernen Filtern anhand realer Manöverdaten der indischen Marine und erstellte eine vergleichende Studie.
- Concluded that Shifted Rayleigh Filter outperforms other filters in terms of computational complexity while still being superior at tracking target.

Aug. 2017 – Mai 2018  
IIT Patna, Indien

## Bachelorarbeit “Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation”

Control and Instrumentation Lab

- Designed and implemented a parallel architecture of Sigma-point Kalman filtering algorithms on an FPGA by independently conceptualised parallel routine for Cholesky decomposition in  $O(N)$  time complexity.
- Further optimised resource usage of parallel Cholesky decomposition architecture for maximum processor utilisation to achieve  $O(\frac{1}{4}N^2)$  resource complexity, as compared to  $O(\frac{1}{2}N^2)$  resource complexity of state-of-the-art.
- Implemented parallel architectures using Verilog HDL and Xilinx Vivado on Xilinx Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards, making use of open-source floating-point IPs and Xilinx Vivado IPs.
- Presented final work product to the professors of the department and was one of only two students to receive unanimous 10 / 10 grade from cohort of 50 candidates. Nominated for Best B. Tech. Thesis award from Dept of Electrical Engineering.

Mai 2017 – Aug. 2017  
Google Summer of Code  
2017

## Studentischer Softwareentwickler

Free and Open Source Silicon Foundation, “EDSAC Museum on FPGA”

- Built Verilog model of historic EDSAC computer from original but incomplete documentation in collaboration with members of “The EDSAC Replica Project” team (TNMOC, Bletchley Park, UK).
- Programmed and simulated EDSAC architecture and ISA on myStorm Lattice iCE FPGA board using open-source toolchains, like Yosys and iverilog.
- Coordinated with team of younger students in UK to build hardware imitation of EDSAC memory delay line, teleprinter and paper tape reader.
- Demonstrated final work product at ChipHack 2017 workshop and presented at ORConf 2017 digital design conference in Hebden Bridge, UK, for which full sponsorship was received.

Feb. 2016 – Aug. 2016  
Google Summer of Code  
2016

## Studentischer Softwareentwickler

Coreboot (Flashrom), “Read/Write Multiple Status Registers and Lock/Unlock Memory on SPI Chips”

- Entwickelte eine einheitliche Abstraktion von Statusregistern in SPI Flash-Speicherchips von verschiedenen Chip-Herstellern.
- Programmierte Functions zum Sperren/Entsperren von Speicherplätzen, zum Umgang mit Konfigurationsbits und zur automatischen Generierung von Speicherschutzmaps.
- Entwickelte CLI, um neue Funktionen bereitzustellen, und testete die Infrastruktur mit Raspberry Pi und Teensy-Development-Board.
- Kontaktaufnahme mit dem Verkaufsleiter von GigaDevice aus China, um Engineering-Probe-Chips zu besorgen und Unterstützung für diese Chips einzuführen.

## Kenntnisse

<b>Programmierung</b>	Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS				
<b>Software</b>	Xilinx Vivado & HLS, MATLAB, Simulink, RSCAD, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, L <sup>A</sup> T <sub>E</sub> X, gnuplot				
<b>Hardware</b>	Xilinx Virtex & Zynq SoC, Digilent Nexys4 DDR, RTDS NovaCor, Raspberry Pi, Arduino, PIC Microcontroller				
<b>Sprachen</b>	English	Hearing C2	Reading C2	Speaking C2	Writing C2
	Deutsch	Hören B1	Lesen B2	Sprechen B1	Schreiben B1
	Hindi	Muttersprache			

## Ehrenamtliches und sonstige Tätigkeiten

*Juni 2021 – Apr. 2022*  
*Aachen, Deutschland*

### **Freiwilliger**

*Faiz al-Mawaid al-Burhaniyah (FMB)*

- Co-founded Aachen chapter of FMB and led team of volunteers with vision to provide home-cooked and healthy meals to students in and around Aachen at least once a week.
- Organised meal distribution drives on festive occasions, especially Ramadan, to celebrate cultural identity and increase community engagement.
- Co-developed low-cost, sustainable standard operating model to make community effort scalable and reproducible at other locations.

*Apr. 2017 – Apr. 2018*  
*IIT Patna, Indien*

### **Assistant Head Coordinator, Dept of Electrical Engineering**

*Training and Placement Cell*

- Selected by class majority to represent students of Dept of Electrical Engineering.
- Led team in designing placement brochures and helped arrange on-campus placement sessions, tests and interviews.

*Apr. 2016 – Apr. 2017*  
*IIT Patna, Indien*

### **Coordinator**

*Startup Relations, Entrepreneurship Club*

- Led Startup Relations department and served as mentor to early-stage on-campus startups to help develop business plans, choose investor strategies and network with advisors.
- As part of Core Committee, oversaw the organisation of E-Week 2017, the annual national-level event of Entrepreneurship Club.
- Delivered presentations as part of In-house Mentorship Lecture series based on individual technical and business experience in early-stage startups.

*Apr. 2015 – Apr. 2016*  
*IIT Patna, Indien*

### **Task Manager**

*Startup Relations, Entrepreneurship Club*

- Recruited volunteers and helped organise pitching events, workshops and guest talks.
- Assisted in establishing panel of early investors and mentors for on-campus startups.

## **Referenzen**

### **Univ.-Prof. Dr.-Ing. Andrea Benigni**

*Deputy*

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### **Steffen Vogel, M. Sc.**

*Team Simulation Infrastructure and HPC*

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