Hatim Kanchwala

Pre-final Year • Undergraduate • Electrical Engineering • Indian Institute of Technology Patna
A-437, Boys' Hostel, IIT Patna, Amhara Village, Bihta, Bihar, India - 801118
(+91) 966 5154 719 • hatim@hatimak.me, hatim.ee14@iitp.ac.in • hatimak.me • hatimak • hatimak

INTERESTS

Computer Organisation & Architecture • Embedded Systems Design • Adaptive Filters • Neural Networks

EDUCATION

INDIAN INSTITUTE OF TECHNOLOGY PATNA

B. Tech. in Electrical Engineering
2014 — 2018
Bihta (BR), India
CPI: 7.59 / 10.0 (upto 5th semester)

DEOGIRI COLLEGE

Higher Secondary
2011 — 2013
Aurangabad (MH), India

NATH VALLEY SCHOOL

Primary & Secondary
2001 — 2011
Aurangabad (MH), India

SKILLS

PROGRAMMING

C/C++ • Assembly • Verilog • JavaScript • Python • Java • Scala • Shell • HTML/CSS • LaTeX

SOFTWARE

GNU/Linux • git/GitHub • MATLAB • Simulink • Xilinx ISE • Multisim • Synopsys • Pyxis • MPLAB IDE • Proteus • NumPy/SciPy • Eclipse IDE

HARDWARE

Xilinx Spartan FPGA • PIC Microcontroller • TMS320 DSP Chip • Arduino • 8051 Microcontroller • Raspberry Pi • Teensy

LANGUAGES

English • Hindi • Gujarati • Urdu • Marathi • Arabic

EXPERIENCE

AFICIONADO VENTURES • Backend Engineer

Startup • FEB. 2016 — OCT. 2016 • Gurugram (HR), India

- Purchasing platform helping restaurants procure better quality produce from competitive collection of vendors.
- Designed reactive backend architecture - MeteorJS server, MongoDB database, Heroku/mLab web app hosting, and Cordova for cross-platform mobile apps.
- Implemented MVP-stage marketplace platform with bilingual search to look up products in English/Hinglish. Prototyped conversational UX via messaging bot.
- Started work on vendor inventory and restaurant demand prediction models.

ENHANCE FLASHROM WITH FEATURES TO READ & WRITE MULTIPLE STATUS REGISTERS AND LOCK & UNLOCK MEMORY SPACE • Google Summer of Code 2016 student with Coreboot

Open-source • FEB. 2016 — AUG. 2016 • hatimak/flashrom

- Designed multiple status registers model to abstract chip diversities across manufacturers into single consistent interface.
- Developed rutines to lock/unlock memory space governed by bits in status register(s), handle configuration bits, and automatically generate BP range table for some chips.
- Added functionality to access/lock OTP memory areas.
- Developed CLI to expose new infrastructure. Tested on physical GigaDevice SPI chips using Raspberry Pi (over SPI bus), and Teensy.

WEAVE • Co-founder & Product Developer

Startup • JUNE 2015 — DEC. 2015 • Patna (BR), India

- Implemented prototype in JavaScript to build NURBS model of user, using input features and weighted combination of precomputed basis models.
- Developed algorithm to emulate dyanmics for clothes on NURBS model - users can try clothes virtually.
- Despite garnering client & investor interest, startup failed because product-market fit was not right.

PROJECTS

FPGA IMPLEMENTATION OF NLMS ADAPTIVE FILTERING ALGORITHM FOR SIGNAL ENHANCEMENT

Research • FEB. 2017 — PRESENT • hatimak/zephyr
Adviser: Dr Yatendra Kumar Singh

- Implementing Normalized Least Mean Squares (NLMS) adaptive filtering algorithm to extract desired audio from signal corrupted with additive autoregressive noise.
- Prototyping on Xilinx Spartan-3E FPGA in Verilog HDL, with focus towards optimised placing and routing.
- Investigating performance gain by FPGA over typical DSP chip (TMS320).

COURSEWORK

UNDERGRADUATE

Embedded Systems
VLSI Design
Digital Electronics & Microprocessors
Semiconductor Devices & Circuits
Analog Integrated Circuits
Digital Signal Processing
Control Systems
Communication Systems
Electromagnetic Theory
Electronic Instrumentation
Electrical Power Systems
Electrical Machines
Linear Algebra
Probability & Random Processes
Algorithms & Data Structures

MOOC

The Hardware/Software Interface
Machine Learning
Game Theory
Valuation: Risk & Return
Valuation: Time Value of Money

BIOMETRIC ATTENDANCE SYSTEM SUITABLE FOR ECONOMIC AND LOW-POWER LIMITED-CONNECTIVITY REMOTE DEPLOYMENT

JAN. 2015 — OCT. 2015

- Developed code to interface 8051 (Atmel AT89S51) with fingerprint reader (R305) and GSM/GPRS module (SIM900A) over serial port via multiplexer.
- Developed human interface using 16×2 LCD and keypad.
- Post biometric authentication, attendance data is transmitted by SIM900A via SMS to server. Fingerprints stored locally only.
- Developed firmware in C and ASM. Microcontroller operations simulated in Proteus.

MINI PROJECTS

8085 INSTRUCTION SET ARCHITECTURE PROTOTYPE ON FPGA WITH BASIC PIPELINING

FEB. 2017 — PRESENT • hatimak/marineford
Adviser: Dr Kailash Chandra Ray

- Implementing Intel 8085 microprocessor ISA on Xilinx Spartan-3E FPGA in Verilog HDL. Developing ASM testbenches to profile performance delta due to pipelining.

IMPLEMENTATION OF VIOLA-JONES OBJECT DETECTION FRAMEWORK

JAN. 2017 — PRESENT • hatimak/vj-goggles
Adviser: Dr Mahesh H. Kolekar

- Implementing algorithm proposed in paper by P. Viola and M. Jones in MATLAB and on TMS320 DSP chip.

FULL-CUSTOM DESIGN OF RING OSCILLATOR

NOV. 2016 • hatimak/ring-osc
Adviser: Dr Kailash Chandra Ray

- Designed core layout of ring oscillator using AMI05 (0.5 µm) CMOS Technology in Pyxis (Mentor Graphics), and verified output of back annotated simulation.

POSITIONS

COORDINATOR, STARTUP RELATIONS • Entrepreneurship Club, IIT Patna

APR. 2016 — PRESENT

- Serving as on-campus mentor to early stage startups, helping them develop business plan, choose investor strategy, and network with advisers.
- Building connections with startups and investors with vision to form investor panel for on-campus startups.
- Delivered presentations as part of In-house Lecture series conducted by E-Club.

TASK MANAGER, STARTUP RELATIONS • Entrepreneurship Club, IIT Patna

APR. 2015 — APR. 2016

- Part of Organising Committee for E-Club's flagship annual event, E-Week. Organised guest talks, workshops and pitching event.

VOLUNTEER, STARTUP RELATIONS • Entrepreneurship Club, IIT Patna

AUG. 2014 — APR. 2015