

Hatim Kanchwala

📅 07.02.1995
🏠 Engelbertstraße 12, 52078 Aachen, Germany
📞 +49 176 45 9995 53
✉ hatim@hatimak.me
🌐 <https://www.linkedin.com/in/hatimak>



Education

Apr. 2019 – Sept. 2022
Aachen, Deutschland 🇩🇪

M. Sc. Elektrotechnik, Informationstechnik und Technische Informatik

RWTH Aachen Universität

Final Grade 2,1

- Masterarbeit "Field-Programmable Gate Array basierte Echtzeitregelung und -simulation"

Juli 2014 – Mai 2018
Bihta (Patna), Indien 🇮🇳

B. Tech. Electrical Engineering

Indian Institute of Technology Patna

Final Grade 7.32 / 10 (indische) = 2,1 (deutsche)

- Bachelorarbeit "Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"

Experience

Apr. 2021 – Dec. 2021
Aachen, Germany 🇩🇪

M. Sc. Thesis "Field-Programmable Gate Array based Real-Time Control and Simulation"

Institute of Energy and Climate Research (IEK-10), Forschungszentrum Juelich GmbH

- Developed design with soft-core microprocessors to rapidly prototype control-loop algorithms for FPGA-based real-time simulators.
- Introduced control and data-logger soft-cores dedicated to running control algorithms at switching frequency and logging simulation data.
- Conceptualised heterogeneous architecture of multiple dedicated soft-core microprocessors, enabling hierarchical control-loop system designs.
- Implemented digital design based on soft-core MicroBlaze microprocessor from Xilinx on Virtex Ultrascale+ VCU118 board.

Oct. 2020 – Feb. 2021
Remote 🌐

Intern

Institute of Energy and Climate Research (IEK-10), Forschungszentrum Juelich GmbH

- Implemented power systems models using High-Level Synthesis designs for RTL co-simulation and real-time simulation on FPGA.
- Extended HLS models with memory-mapped AXI4 register interface. Verified hardware models on Virtex-7 VC707 FPGA board using remote debugging.
- Developed Makefile pipeline on Linux for ORTIS code generation, Vivado High-Level Synthesis, Vivado IP Integrator and FPGA bitstream generation stages.

May 2019 – Sept. 2020
Aachen, Germany 🇩🇪

Student Assistant

Institute for Automation of Complex Power Systems, E.ON Energy Research Centre

- Integrated Xilinx FPGA boards into VILLAS co-simulation platform by designing an architecture built on top of Aurora 8B/10B serial protocol.
- Engineered Tcl-Makefile system of scripts to automate design generation and bitstream compilation.
- Developed bare-metal driver programs in C/C++ for FPGA firmware.

May 2018 – Nov. 2018
IIT Patna, India 🇮🇳

Senior Research Fellow

"Underwater Target Motion Analysis with Passive Sensors",

Naval Physical & Oceanographic Laboratory (DRDO), Ministry of Defence, Govt of India

- Implemented advanced tracking filters in MATLAB for the Bearings-only Tracking problem.
- Simulated performance of modern filters on real field manoeuvre data from Indian Navy, and prepared comparative study.
- Concluded Shifted Rayleigh Filter outperforms other filters in terms of computational complexity and tracking accuracy.

Aug. 2017 – May 2018

IIT Patna, India 

B. Tech. Thesis “Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation”

Control and Instrumentation Lab

- Designed and implemented a parallel architecture of Sigma-point Kalman filtering algorithms on FPGA.
- Conceptualised novel parallel routine for Cholesky matrix decomposition; improvement from $O(N^3)$ to $O(N)$ time complexity.
- Optimised resource usage of Cholesky decomposition architecture for double utilisation at same processor count.
- Implemented parallel designs in Verilog HDL using Vivado and open-source IPs on Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards.

May 2017 – Aug. 2017

Google Summer of Code
2017

Student Developer

Free and Open Source Silicon Foundation, “EDSAC Museum on FPGA”

- Built Verilog model of historic EDSAC computer from original but incomplete documentation in collaboration with experts from The National Museum of Computing, UK.
- Programmed and simulated EDSAC architecture and ISA on myStorm Lattice iCE FPGA board using open-source toolchains, like Yosys and iverilog.
- Coordinated with team of students in UK to build hardware imitation of EDSAC memory delay line, teleprinter and paper tape reader.
- Demonstrated final work product at ChipHack 2017 workshop and presented at ORConf 2017 digital design conference in Hebden Bridge, UK.

Feb. 2016 – Aug. 2016

Google Summer of Code
2016

Student Developer

Coreboot (Flashrom), “Read/Write Multiple Status Registers and Lock/Unlock Memory on SPI Chips”

- Designed unified abstraction of multiple status registers in SPI Flash-memory chips across diverse chip manufacturers.
- Programmed routines to lock/unlock memory areas, handle configuration bits, and automatically generate memory protection maps.
- Developed CLI to expose new features, and tested infrastructure using Raspberry Pi and Teensy development board.

Skills

Programming	Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS				
Software	Xilinx Vivado & HLS, MATLAB, Simulink, RSCAD, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, L ^A T _E X, gnuplot				
Hardware	Xilinx Virtex & Zynq SoC, Digilent Nexys4 DDR, RTDS NovaCor, Raspberry Pi, Arduino, PIC Microcontroller				
Languages	English	Hearing C2	Reading C2	Speaking C2	Writing C2
	Deutsch	Hören B1	Lesen B2	Sprechen B1	Schreiben B1
	Hindi	native			

Volunteering

June 2021 – Apr. 2022

Aachen, Germany 

Volunteer

Faiz al-Mawaid al-Burhaniyah (FMB)

- Co-founded Aachen chapter of FMB and led team of volunteers with vision to provide home-cooked and healthy meals to students in and around Aachen at least once a week.
- Organised meal distribution drives on festive occasions, especially Ramadan, to celebrate cultural identity and increase community engagement.
- Co-developed low-cost, sustainable standard operating model to make community effort scalable and reproducible at other locations.

Apr. 2017 – Apr. 2018

IIT Patna, India 

Assistant Head Coordinator, Dept of Electrical Engineering

Training and Placement Cell

- Selected by class majority to represent students of Dept of Electrical Engineering.
- Led team in designing placement brochures and helped arrange on-campus placement sessions, tests and interviews.

Apr. 2016 – Apr. 2017


IIT Patna, India 

Coordinator

Startup Relations, Entrepreneurship Club

- Led Startup Relations department and served as mentor to early-stage on-campus startups to help develop business plans, choose investor strategies and network with advisors.
- As part of Core Committee, oversaw the organisation of E-Week 2017, the annual national-level event of Entrepreneurship Club.
- Delivered presentations as part of In-house Mentorship Lecture series based on individual technical and business experience in early-stage startups.

Apr. 2015 – Apr. 2016

IIT Patna, India 

Task Manager

Startup Relations, Entrepreneurship Club

- Recruited volunteers and helped organise pitching events, workshops and guest talks.
- Assisted in establishing panel of early investors and mentors for on-campus startups.

References

Univ.-Prof. Dr.-Ing. Andrea Benigni

Deputy

Institut für Energie- und Klimaforschung,

Forschungszentrum Jülich GmbH

 +49 2461 61 85523

 a.benigni@fz-juelich.de

Steffen Vogel, M. Sc.

Team Simulation Infrastructure and HPC

Institute for Automation of Complex Power Systems,

E.ON Energy Research Centre, RWTH Aachen Universität

 +49 241 80 49577

 stvogel@eonerc.rwth-aachen.de