Hatim Kanchwala

Pre-final Year • Undergraduate • Electrical Engineering • Indian Institute of Technology Patna
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EDUCATION

INDIAN INSTITUTE OF TECHNOLOGY PATNA
B. Tech. in Electrical Engineering
2014 — 2018
Bihta (BR), India
CPI: 7.59 / 10.0 (upto 5th semester)

DEOGIRI COLLEGE
Higher Secondary
2011 — 2013
Aurangabad (MH), India

NATH VALLEY SCHOOL
Primary & Secondary
2001 — 2011
Aurangabad (MH), India

SKILLS

PROGRAMMING
C/C++ • Assembly • Verilog • JavaScript • Python • Java • Scala • Shell • HTML/CSS • LaTeX

SOFTWARE
GNU/Linux • MATLAB • Simulink • git/GitHub • Xilinx ISE • Multisim • Synopsys • Pyxis • MPLAB IDE • Proteus • NumPy/SciPy • Eclipse IDE

HARDWARE
Xilinx Spartan FPGA • PIC Microcontroller • TMS320 DSP Chip • Arduino • 8051 Microcontroller • Raspberry Pi • Teensy

LANGUAGES
English • Hindi • Gujarati • Urdu • Marathi • Arabic

INTERESTS

Computer Organisation & Architecture • Reconfigurable Computing • Embedded Systems Design • Networked Control Systems

EXPERIENCE

GOOGLE SUMMER OF CODE • Developer with Free and Open Source Silicon Foundation
"EDSAC Museum on FPGA"
Open-source • MAY 2017 — PRESENT

- Replicating EDSAC architecture and ISA on myStorm FPGA board using Verilog HDL and Yosys.
- Designing and implementing standard communication protocol for external extensible I/O interfaces.
- Developing assembler to debug, build and load instructions onto FPGA board.

AFICIONADO VENTURES • Backend Engineer
Startup • FEB. 2016 — OCT. 2016 • Gurugram (HR), India

- Purchasing platform helping restaurants procure quality produce from competitive collection of vendors.
- Designed reactive backend architecture - MeteorJS server, MongoDB database, Heroku/mLab web app hosting, and Cordova for cross-platform mobile apps.
- Implemented MVP-stage marketplace platform with bilingual search for products in English/Hinglish.
- Prototyped conversational UX via messaging bot.

GOOGLE SUMMER OF CODE • Developer with Coreboot (Flashrom)
"Enhance Flashrom with features to read & write multiple status registers and lock & unlock memory space"
Open-source • FEB. 2016 — AUG. 2016 • hatimak/flashrom

- Designed multiple status registers model to abstract chip diversities across manufacturers into single consistent interface.
- Developed routines to lock/unlock memory space governed by bits in status register(s), handle configuration bits, and automatically generate memory protection maps for some chips.
- Added functionality to access/lock OTP memory areas.
- Developed CLI to expose new infrastructure. Tested on physical GigaDevice SPI chips using Raspberry Pi (over SPI bus), and Teensy.

WEAVE • Co-founder & Product Developer
Startup • JUNE 2015 — DEC. 2015 • Patna (BR), India

- Implemented prototype in JavaScript to build NURBS user model, using input features and weighted combination of precomputed basis models.
- Developed algorithm to emulate dynamics for clothes on NURBS model - users can try clothes virtually.
- Despite garnering client & investor interest, startup failed because product-market fit was not right.

COURSEWORK

UNDERGRADUATE

Embedded Systems
VLSI Design
Digital Electronics & Microprocessors
Semiconductor Devices & Circuits
Analog Integrated Circuits
Digital Signal Processing
Control Systems
Communication Systems
Electromagnetic Theory
Electronic Instrumentation
Electrical Power Systems
Electrical Machines
Linear Algebra
Probability & Random Processes
Algorithms & Data Structures

MOOC

The Hardware/Software Interface
Machine Learning
Game Theory
Valuation: Risk & Return
Valuation: Time Value of Money

PROJECTS

FPGA IMPLEMENTATION OF NLMS ADAPTIVE FILTERING ALGORITHM FOR SIGNAL ENHANCEMENT

Course project • FEB. 2017 — APR. 2017
Adviser: Dr Yatendra Kumar Singh

- Implemented Normalized NLMS adaptive filtering algorithm to extract desired signal from that corrupted with additive autoregressive noise.
- Prototyped on Xilinx Spartan-3E FPGA in Verilog HDL.

FULL-CUSTOM DESIGN OF RING OSCILLATOR

Course project • NOV. 2016
Adviser: Dr Kailash Chandra Ray

- Designed core layout of ring oscillator using AMI05 (0.5 µm) CMOS Technology in Pyxis (Mentor Graphics).

BIOMETRIC ATTENDANCE SYSTEM SUITABLE FOR ECONOMIC AND LOW-POWER LIMITED-CONNECTIVITY REMOTE DEPLOYMENT

JAN. 2015 — OCT. 2015

- Interfaced 8051 (Atmel AT89S51) with fingerprint reader (R305) and GSM/GPRS module (SIM900A) over serial port, via multiplexer.
- Developed user interface using 16×2 LCD and keypad.
- Developed firmware in C and ASM. Microcontroller operations simulated in Proteus.

POSITIONS

ASSISTANT HEAD COORDINATOR

Training and Placement Cell, IIT Patna
APR. 2017 — PRESENT

COORDINATOR, STARTUP RELATIONS

Entrepreneurship Club, IIT Patna
APR. 2016 — APR. 2017

- Served as on-campus mentor to early stage startups, helped develop business plan, choose investor strategy and network with advisers.
- Part of Core Committee for E-Club's annual event, E-Week. Organised guest talks and In-house sessions.
- Delivered presentations as part of In-house Lecture series conducted by E-Club.

TASK MANAGER, STARTUP RELATIONS

Entrepreneurship Club, IIT Patna
APR. 2015 — APR. 2016

- Building connections with startups and investors with vision to form investor panel for on-campus startups.
- Part of Organising Committee for E-Club's annual event, E-Week. Organised guest talks, workshops and pitching event.

VOLUNTEER, STARTUP RELATIONS

Entrepreneurship Club, IIT Patna
AUG. 2014 — APR. 2015