Hatim Kanchwala

Pre-final Year • Undergraduate • Electrical Engineering • Indian Institute of Technology Patna
A-437, Boys' Hostel, IIT Patna, Amhara Village, Bihta, Bihar, India - 801118
(+91) 966 5154 719 • hatim@hatimak.me, hatim.ee14@iitp.ac.in • hatimak.me • hatimak • hatimak

INTERESTS

Computer Organisation & Architecture • Embedded Systems Design • Adaptive Filters • Neural Networks

SKILLS

PROGRAMMING

C/C++ • Assembly • Verilog • JavaScript • Python • Java • Scala • Shell • HTML/CSS • LaTeX

SOFTWARE

GNU/Linux • git/GitHub • MATLAB • Simulink • Xilinx ISE • Multisim • Synopsys • Pyxis • MPLAB IDE • Proteus • NumPy/SciPy • Eclipse IDE

HARDWARE

Xilinx Spartan FPGA • PIC Microcontroller • TMS320 DSP Chip • Arduino • 8051 Microcontroller • Raspberry Pi • Teensy

LANGUAGES

English • Hindi • Gujarati • Urdu • Marathi • Arabic

EDUCATION

INDIAN INSTITUTE OF TECHNOLOGY PATNA

B. Tech. in Electrical Engineering
2014 — 2018
Bihta (BR), India
CPI: 7.59 / 10.0 (upto 5th semester)

DEOGIRI COLLEGE

Higher Secondary
2011 — 2013
Aurangabad (MH), India

NATH VALLEY SCHOOL

Primary & Secondary
2001 — 2011
Aurangabad (MH), India

PROJECTS

FPGA IMPLEMENTATION OF NLMS ADAPTIVE FILTERING ALGORITHM FOR SIGNAL ENHANCEMENT

Research • FEB. 2017 — PRESENT • hatimak/zephyr
Adviser: Dr Yatendra Kumar Singh

- Implementing Normalized Least Mean Squares (NLMS) adaptive filtering algorithm to extract desired audio from corrupted signal with additive autoregressive noise.
- Prototyping on Xilinx Spartan-3E FPGA in Verilog HDL, with focus towards optimised placing and routing.
- Investigating performance gain by FPGA over typical DSP chip (TMS320).

ENHANCE FLASHROM WITH FEATURES TO READ/WRITE MULTIPLE STATUS REGISTERS AND LOCK/UNLOCK MEMORY SPACE

Google Summer of Code 2016 with Coreboot
Open-source • FEB. — AUG. 2016 • hatimak/flashrom

- Designed multiple status registers model that abstracts chip diversities across manufacturers into single consistent interface, while retaining identities of special bits in status registers.
- Designed Block Protection model allowing flashrom to lock/unlock memory space governed by bits in status register(s). Developed routines to handle additional configuration bits and generate block protect range table for given Flash chip. Multiple chips share block protect range table definitions to make efficient use of memory. Added functionality to access/lock OTP memory areas.
- Developed CLI to expose new infrastructure. Tested on physical GigaDevice SPI chips using internal dummy programmer, Raspberry Pi (over SPI bus), and Teensy.
- Planned to add support for configuration registers and for access protection in non-SPI chips.

BIOMETRIC ATTENDANCE SYSTEM SUITABLE FOR ECONOMIC AND LOW-POWER REMOTE DEPLOYMENT

JAN. — OCT. 2015

- Hardware prototype comprised 8051 microcontroller (Atmel AT89S51), fingerprint reader (R305), GSM/GPRS module (SIM900A), 16×2 LCD and keypad.
- 8051 interfaces with R305 and SIM900A over serial port via multiplexer. 16×2 LCD and keypad provides control of device. Initial setup requires enrolling fingerprints into R305 internal memory. Post biometric authentication, attendance data is transmitted by SIM900A via SMS or over GPRS to central server depending on connectivity at remote station. Fingerprints stored locally only.
- Developed firmware in C and ASM. Microcontroller operations simulated in Proteus.

MINI PROJECTS

8085 INSTRUCTION SET ARCHITECTURE PROTOTYPE ON FPGA WITH BASIC PIPELINING

FEB. 2017 — PRESENT • hatimak/marineford
Adviser: Dr Kailash Chandra Ray

- Implementing Intel 8085 microprocessor ISA on Xilinx Spartan-3E FPGA in Verilog HDL. Developing ASM testbenches to investigate performance gain due to pipelining.

COURSEWORK

UNDERGRADUATE

Digital Electronics & Microprocessors
Embedded Systems
VLSI Design
Semiconductor Devices & Circuits
Analog Integrated Circuits
Digital Signal Processing
Control Systems
Communication Systems
Electromagnetic Theory
Electronic Instrumentation
Electrical Power Systems
Electrical Machines
Linear Algebra
Probability & Random Processes
Algorithms & Data Structures

MOOC

The Hardware/Software Interace
Machine Learning
Game Theory
Valuation: Risk & Return
Valuation: Time Value of Money

IMPLEMENTATION OF VIOLA-JONES OBJECT DETECTION FRAMEWORK

JAN. 2017 — PRESENT • hatimak/vj-goggles
Adviser: Dr Mahesh H. Kolekar

- Implementing object detection algorithm proposed in paper by P. Viola and M. Jones in MATLAB and on TMS320 DSP chip.

FULL-CUSTOM DESIGN OF RING OSCILLATOR

NOV. 2016 • hatimak/ring-osc
Adviser: Dr Kailash Chandra Ray

- Designed core layout of ring oscillator using AMI05 (0.5 µm) CMOS Technology in Pyxis (Mentor Graphics), and verified output of back annotated simulation.

EXPERIENCE

AFICIONADO VENTURES • Backend Engineer

Startup • FEB. 2016 — OCT. 2016 • Gurugram (HR), India

- Purchasing platform connecting restaurants and vendors - helping restaurants procure better quality raw ingredients and products at competitive prices from extensive & diverse collection of vendors.
- Designed reactive scalable backend architecture for marketplace platform. Used MeteorJS for server, MongoDB for data storage, Heroku/mLab for web app hosting, and Cordova for cross-platform mobile apps.
- Implemented MVP-stage marketplace platform with bilingual search to look up products in English/Hinglish. Started work on machine learning engine for vendor inventory prediction and predictive restaurant purchase order generation. Proposed and prototyped conversational UX via messaging bot, in lieu of app interfaces.

WEAVE • Co-founder & Product Developer

Startup • JUNE 2015 — DEC. 2015 • Patna (BR), India

- Implemented basic prototype of Model Generator in JavaScript - based on user input, Model Generator builds 3D NURBS model of user's body using weighted combination of precomputed basis models.
- Developed model of Cloth Physics Engine that emulates dyanmics for clothes fitted on generated NURBS model - users can try clothes virtually.
- Despite garnering client & investor interest, startup failed because product-market fit was not right.

EXTRACURRICULAR

COORDINATOR, STARTUP RELATIONS • Entrepreneurship Club, IIT Patna

APR. 2015 — PRESENT

- Serving as on-campus mentor to early stage startups, helping entrepreneurs develop business plan, choose investor strategy, and network with domain experts.
- Responsible for building connections with startups and investors, and building investor panel for on-campus startups.
- Part of Core Committee for E-Club's flagship annual event, E-Week. Responsible for organizing guest talks, workshops and pitching event in collaboration with Incubation Centre, IIT Patna.