



Hatim Kanchwala

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EDUCATION

2019 – 2021	RWTH Aachen University , M.Sc. IN ELECTRICAL ENGINEERING, INFORMATION TECHNOLOGY AND COMPUTER ENGINEERING	PRESENT	Aachen, Germany
2014 – 2018	Indian Institute of Technology Patna , B.TECH. IN ELECTRICAL ENGINEERING	CPI 7.32 / 10	Bihta (Patna), India
2011 – 2013	Deogiri College , CLASS XII MAHARASHTRA HIGHER SECONDARY CERTIFICATE	82.33%	Aurangabad, India
2001 – 2011	Nath Valley School , CLASS X CENTRAL BOARD OF SECONDARY EDUCATION	GPA 10 / 10	Aurangabad, India

EXPERIENCE

STUDENT ASSISTANT

Aachen, Germany

Institute for Automation of Complex Power Systems, E.ON Energy Research Centre

May 2019 – PRESENT

- Working on integrating FPGAs into a distributed real-time power-hardware-in-loop simulation system.

SENIOR RESEARCH FELLOW

Control and Instrumentation

“Underwater Target Motion Analysis with Passive Sensors”

Lab, IIT Patna

Supervisor: Dr Shovan Bhaumik, Sponsor: Naval Physical & Oceanographic Laboratory (DRDO)

May 2018 – Nov. 2018

- Implemented advanced filters for Bearings-Only Tracking problem - Distributed Extended Kalman Filter, Shifted Rayleigh Filter, Particle Filter with Unscented Kalman Filter and Shifted Rayleigh Filter proposals, Particle Filter with MCMC, and Regularised Particle Filter.
- Simulated performance of these filters on actual field manoeuvres provided by sponsor, and prepared a comparative study. Shifted Rayleigh Filter outperforms other filters in terms of computational complexity while still being superior at tracking target.

B.TECH. THESIS | NOMINATED FOR THE BEST B.TECH. THESIS AWARD FROM DEPT OF ELECTRICAL ENGINEERING

“Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation”

IIT Patna

Supervisor: Dr Shovan Bhaumik

Aug. 2017 – May 2018

- Developed parallel architecture of Sigma-point filtering algorithms like UKF, CKF, etc.
- Designed and implemented on FPGA a parallel architecture to compute the Cholesky decomposition of a positive-definite matrix in $\mathcal{O}(N)$ time complexity.
- Further optimised resource usage of parallel Cholesky decomposition architecture for maximum processor utilisation to achieve $\mathcal{O}(\frac{1}{4}N^2)$ resource complexity, as compared to $\mathcal{O}(\frac{1}{2}N^2)$ resource complexity of state-of-the-art.
- Using parallel Cholesky architecture, formulated and implemented linear time complexity matrix inverse routine to compute covariance inverses required by sigma-point filtering algorithms.
- Implemented Gaussian RNG based on CDF Inversion method using FPGA amenable LUT-SR Uniform RNG.
- Implemented all the parallel architectures using Verilog HDL and Xilinx Vivado on Xilinx Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards. Made use of open-source floating-point IP and several Xilinx Vivado IP.

STUDENT DEVELOPER, “EDSAC MUSEUM ON FPGA” | PRESENTED AT ORCONF 2017, HEBDEN BRIDGE, UK

Free and Open Source Silicon Foundation

Google Summer of Code 2017

Mentor: Dr Jeremy Bennett

May 2017 – Aug. 2017

- Built a model of EDSAC from original, albeit incomplete documentation, and from correspondences with members of “The EDSAC Replica Project” team (TNMOC, Bletchley Park, UK).
- Replicated EDSAC architecture and ISA on myStorm Lattice iCE FPGA board using Verilog HDL and open-source toolchain Yosys.
- Designed and implemented modified-UART communication protocol for external extensible I/O interfaces.
- Helped a team of students in UK build hardware reproduction of EDSAC memory delay line, teleprinter and paper tape reader.
- Final work product used at ChipHack 2017 workshop and presented work at ORConf 2017 conference during Wuthering Bytes festival in Hebden Bridge, UK.

Coreboot (Flashrom)

Feb. 2016 – Aug. 2016

- Designed multiple status registers model to abstract chip diversities across manufacturers into single consistent interface.
- Developed routines to lock/unlock memory space governed by bits in status registers, handle configuration bits, and automatically generate memory protection maps for some chips.
- Added functionality to access/lock OTP memory areas.
- Developed CLI to expose new infrastructure. Tested on physical GigaDevice SPI chips using Raspberry Pi and Teensy.

SUMMER INTERN

New Delhi, India

Aficionado Ventures

May 2016 – July 2016

- Aficionado was a startup helping restaurants procure quality produce from competitive collection of vendors.
- Designed reactive backend architecture - MeteorJS server, MongoDB database, Heroku/mLab web hosting, and Cordova for cross-platform mobile apps.
- Implemented MVP-stage marketplace platform from scratch with bilingual search for products in English/Hinglish.
- Worked with business team to conduct market research on restaurants and vendors.

PROJECTS

Implementation of Normalised LMS Adaptive Filtering Algorithm for Signal Enhancement on Raspberry Pi

Design Lab, IIT Patna

Supervisor: Dr Yatendra Kumar Singh

Feb. 2017 – Apr. 2017

- Implemented normalised LMS adaptive filtering to extract desired signal from that corrupted with autoregressive noise.
- Prototyped on Raspberry Pi Model 3.

Full-Custom Design of Ring Oscillator

VLSI Design Lab, IIT Patna

Supervisor: Dr Kailash Chandra Ray

Nov. 2016

- Designed core layout of ring oscillator using AMI05 (0.5 um) CMOS Technology in Pyxis Layout (Mentor Graphics).

Biometric Attendance System Suitable for Economic and Low-power Limited-connectivity Remote Deployment

Innovation Centre, IIT Patna

Jan. 2015 – Oct. 2015

- Interfaced Atmel AT89S51 8051 microcontroller with R305 fingerprint reader and SIM900A GSM/GPRS module over serial port via multiplexer.
- Developed user interface using 16 × 2 LCD and keypad.
- Developed firmware in C and ASM. Microcontroller operations simulated in Proteus.

ACHIEVEMENTS

2018	Nominated for Best B.Tech. Thesis award , Dept of Electrical Engineering	IIT Patna
2017	Received full sponsorship to present “EDSAC Museum on FPGA” at ORConf 2017 open-source digital design conference	Hebden Bridge, UK
2014	Secured All India Rank 4997 (99.6156th percentile) in JEE Advanced , All India Joint Entrance Exam	Pune, India
2010	Received silver medal , International Informatics Olympiad 2010	New Delhi, India
2010	Secured rank 25 and received gold medal in the final round , 9 th National Cyber Olympiad	New Delhi, India
2008	Secured rank 156 in the final round , 7 th National Cyber Olympiad	Aurangabad, India
2006	Secured rank 196 in the final round , 5 th National Cyber Olympiad	Aurangabad, India

SKILLS

Programming	Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS
Software	Xilinx Vivado, MATLAB, Simulink, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, \LaTeX , gnuplot, Mentor Graphics
Hardware	Xilinx Virtex & Zynq-7000 SoC, Digilent Nexys4 DDR, Raspberry Pi, Arduino, PIC Microcontroller, TMS320 DSP Chip
Languages	English (TOEFL 114/120), German (A1), Hindi (native)

POSITIONS

Assistant Head Coordinator, Dept of Electrical Engineering

IIT Patna

Training and Placement Cell

Apr. 2017 - Apr. 2018

- Designed placement brochures for IIT Patna and Dept of Electrical Engineering.
- Helped arrange and coordinate placement sessions, tests and interviews.

Coordinator, Startup Relations*IIT Patna***Entrepreneurship Club***Apr. 2016 - Apr. 2017*

- Served as on-campus mentor to early stage startups, helped develop business plan, choose investor strategy and network with advisers.
- Part of Core Committee for Entrepreneurship Club's annual event, E-Week. Organised guest talks and In-house sessions.
- Delivered presentations as part of In-house Lecture series conducted by Entrepreneurship Club.

Task Manager, Startup Relations*IIT Patna***Entrepreneurship Club***Apr. 2015 - Apr. 2016*

- Worked towards building connections with startups and investors with vision to form investor panel for on-campus startups.
- Part of Organising Committee for Entrepreneurship Club's annual event, E-Week. Organised guest talks, workshops and pitching event.