

# Hatim Kanchwala

Birth date: 07.02.1995

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## Education

**Apr. 2019 – Sept. 2022**

Aachen, Germany

**M.Sc. Electrical Engineering, Information Technology and Computer Engineering**

*RWTH Aachen University*

Final Grade 2,1

- Thesis “Field-Programmable Gate Array based Real-Time Control and Simulation”

**July 2014 – May 2018**

Bihta (Patna), India

**B. Tech. Electrical Engineering**

*Indian Institute of Technology Patna*

Final Grade 7.32 / 10

- Thesis “Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation”

## Experience

**Apr. 2021 – Dec. 2021**

Aachen, Germany

**M.Sc. Thesis “Field-Programmable Gate Array based Real-Time Control and Simulation”**

*Institute of Energy and Climate Research (IEK-10), Forschungszentrum Juelich GmbH*

- Developed design with soft-core microprocessors to rapidly prototype control-loop algorithms for FPGA-based real-time simulators.
- Introduced control and data-logger soft-cores dedicated to running control algorithms at switching frequency and logging simulation data.
- Conceptualised heterogeneous architecture of multiple dedicated soft-core microprocessors, enabling hierarchical control-loop system designs.

**Oct. 2020 – Feb. 2021**

Remote

**Intern**

*Institute of Energy and Climate Research (IEK-10), Forschungszentrum Juelich GmbH*

- Implemented power systems models using High-Level Synthesis designs for RTL co-simulation and real-time simulation on FPGA.
- Extended HLS models with memory-mapped AXI4 register interface. Verified hardware models on Virtex-7 VC707 FPGA board using remote debugging.
- Developed Makefile pipeline on Linux for ORTIS code generation, Vivado High-Level Synthesis, IP Integrator and FPGA bitstream generation stages.

**May 2019 – Sept. 2020**

Aachen, Germany

**Student Assistant**

*Institute for Automation of Complex Power Systems, E.ON Energy Research Centre*

- Integrated Xilinx FPGA boards into VILLAS co-simulation platform by designing an architecture built on top of Aurora 8B/10B serial protocol.
- Engineered Tcl-Makefile system of scripts to automate design generation and bitstream compilation.
- Developed bare-metal driver programs in C/C++ for FPGA firmware.

**May 2018 – Nov. 2018**

IIT Patna, India

**Senior Research Fellow**

*“Underwater Target Motion Analysis with Passive Sensors”,*

*Naval Physical & Oceanographic Laboratory (DRDO), Ministry of Defence, Govt of India*

- Implemented advanced tracking filters in MATLAB for the Bearings-only Tracking problem.
- Simulated performance of modern filters on real field manoeuvre data from Indian Navy, and prepared comparative study.

Aug. 2017 – May 2018  
IIT Patna, India

## B. Tech. Thesis “Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation”

Control and Instrumentation Lab

- Designed and implemented a parallel architecture of Sigma-point Kalman filtering algorithms on FPGA.
- Conceptualised novel parallel routine for Cholesky matrix decomposition; improvement from  $O(N^3)$  to  $O(N)$  time complexity.
- Optimised resource usage of Cholesky decomposition architecture for double utilisation at same processor count.

May 2017 – Aug. 2017  
Google Summer of Code 2017

## Student Developer

Free and Open Source Silicon Foundation, “EDSAC Museum on FPGA”

- Built Verilog model of historic EDSAC computer from original but incomplete documentation in collaboration with experts from The National Museum of Computing, UK.
- Designed and implemented modified-UART communication protocol to support external embedded I/O interfaces.

Feb. 2016 – Aug. 2016  
Google Summer of Code 2016

## Student Developer

Coreboot (Flashrom), “Read/Write Multiple Status Registers and Lock/Unlock Memory on SPI Chips”

- Designed unified abstraction of multiple status registers in SPI Flash-memory chips across diverse chip manufacturers.
- Programmed routines to lock/unlock memory areas, handle configuration bits, and automatically generate memory protection maps.
- Developed CLI to expose new features, and tested infrastructure using Raspberry Pi and Teensy development board.

## Skills

Programming	Verilog, C/C++, Python, Assembly, Java, Tcl, JavaScript, Shell, HTML/CSS					
Software	Xilinx Vivado & HLS, MATLAB, Simulink, git/GitHub, RSCAD, NI LabVIEW, GNU/Linux, gdb, Verilator, yosys, L <sup>A</sup> T <sub>E</sub> X, gnuplot, OpenCV					
Hardware	Xilinx Virtex & Zynq SoC, Digilent Nexys4 DDR, RTDS NovaCor, Lattice FPGA, Raspberry Pi, Arduino, PIC Microcontroller					
Languages	English	Listening C2	Reading C2	Speaking C2	Writing C2	TOEFL 114 / 120
	Deutsch	Hören B1	Lesen B2	Sprechen B1	Schreiben B1	
	Hindi	native				

## Volunteering

June 2021 – Apr. 2022  
Aachen, Germany

## Volunteer

Faiz al-Mawaid al-Burhaniyah (FMB)

- Co-founded Aachen chapter of FMB and led team of volunteers to provide home-cooked and healthy meals to students in and around Aachen at least once a week.
- Organised meal distribution drives on festive occasions, especially Ramadan.

Apr. 2016 – Apr. 2017  
IIT Patna, India

## Coordinator

Startup Relations, Entrepreneurship Club

- Served as department leader and offered mentorship to early-stage on-campus startups.
- Oversaw the organisation of annual national-level event E-Week 2017.
- Delivered lectures as part of In-house Mentorship series.

## References

Univ.-Prof. Dr.-Ing. Andrea Benigni  
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Institut für Energie- und Klimaforschung,  
Forschungszentrum Jülich GmbH  
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