

# Hatim Kanchwala



BORN ON 7<sup>TH</sup> FEBRUARY 1995 IN INDORE, INDIA

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## EDUCATION

### RWTH Aachen University

Aachen, Germany

M.Sc., ELECTRICAL ENGINEERING, INFORMATION TECHNOLOGY AND COMPUTER ENGINEERING

Sept. 2022

Thesis: "Field-Programmable Gate Array based Real-Time Control and Simulation"

Final Grade 2,1

### Indian Institute of Technology Patna

Bihta (Patna), India

B.Tech., ELECTRICAL ENGINEERING

May 2018

Thesis: "Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"

Final Grade 7.32 / 10

Achieved a national rank of 4997 (99.6156<sup>th</sup> percentile) in the Common Merit List of the Joint Entrance Exam (JEE) from among 1.36 million students to secure a study place at the Indian Institute of Technology Patna

## EXPERIENCE

### M.Sc. THESIS | "FIELD-PROGRAMMABLE GATE ARRAY BASED REAL-TIME CONTROL AND SIMULATION"

### IEK-10, Forschungszentrum Jülich and Institute for Automation of Complex Power Systems

Aachen, Germany

Supervisors: Univ.-Prof. Dr.-Ing. Andrea Benigni, Steffen Vogel, M. Sc., Dr.-Ing. Lukas Razik

Apr. 2021 – Dec. 2021

- Designing soft-core processor based on Xilinx MicroBlaze for control of real-time FPGA-based simulation of power systems.

### STUDENT INTERN

### IEK-10, Forschungszentrum Jülich

Jülich, Germany

Supervisor: Dr.-Ing. Lukas Razik

Oct. 2020 – Feb. 2021

- Worked on ORTIS toolchain for High-level Synthesis of power systems design.
- Performed several RTL and FPGA real-time simulations.
- Implemented data triggering to collect and transfer simulation data points.

### STUDENT ASSISTANT

### Institute for Automation of Complex Power Systems, E.ON Energy Research Centre

Aachen, Germany

Supervisor: Steffen Vogel, M. Sc.

May 2019 – Sept. 2020

- Worked on integrating FPGAs into the VILLAS co-simulation platform.
- Developed support wrapper modules for Aurora 8B10B IP cores.

### SENIOR RESEARCH FELLOW

Control and Instrumentation

### "Underwater Target Motion Analysis with Passive Sensors"

Lab, IIT Patna

Supervisor: Dr Shovan Bhaumik, Sponsor: Naval Physical & Oceanographic Laboratory (DRDO)

May 2018 – Nov. 2018

- Implemented advanced filters for the Bearings-only Tracking problem - Distributed Extended Kalman Filter, Shifted Rayleigh Filter, Particle Filter with compound proposals, Particle Filter with MCMC, and Regularised Particle Filter.
- Simulated the performance of these filters on actual field manoeuvres provided by the sponsor, and prepared a comparative study as measured by time, resource and computational complexities, and target tracking accuracy. Concluded that Shifted Rayleigh Filter outperforms other filters in terms of computational complexity while still being superior at tracking the target.

### B.TECH. THESIS | NOMINATED FOR THE BEST B.TECH. THESIS AWARD FROM DEPT OF ELECTRICAL ENGINEERING

### "Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"

IIT Patna

Supervisor: Dr Shovan Bhaumik

Aug. 2017 – May 2018

- Designed and implemented a parallel architecture of Sigma-point Kalman filtering algorithms on an FPGA by independently conceptualised a parallel routine to the Cholesky decomposition of a positive-definite matrix in  $\mathcal{O}(N)$  time complexity.
- Further optimised resource usage of parallel Cholesky decomposition architecture for maximum processor utilisation to achieve  $\mathcal{O}(\frac{1}{4}N^2)$  resource complexity, as compared to  $\mathcal{O}(\frac{1}{2}N^2)$  resource complexity of state-of-the-art.
- Implemented the parallel architectures using Verilog HDL and Xilinx Vivado on the Xilinx Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards, making use of open-source floating-point IPs and Xilinx Vivado IPs.
- Presented the final work product to the professors of the department and was one of the only two students to receive a unanimous 10 / 10 grade out of a cohort of 50 students.

**Free and Open Source Silicon Foundation**

Google Summer of Code 2017

*Mentor: Dr Jeremy Bennett*

May 2017 – Aug. 2017

- Built a Verilog model of the historic EDSAC computer from original but incomplete documentation in collaboration with members of "The EDSAC Replica Project" team (TNMOC, Bletchley Park, UK).
- Programmed and simulated the EDSAC architecture and ISA on the myStorm Lattice iCE FPGA board using open-source toolchains, like Yosys and iverilog.
- Coordinated with a team of younger students in the UK to build a hardware imitation of the EDSAC memory delay line, teleprinter and paper tape reader.
- Demonstrated the final work product at the ChipHack 2017 workshop and presented at the ORConf 2017 digital design conference in Hebden Bridge, UK, for which full sponsorship was received.

**STUDENT DEVELOPER, "READ/WRITE MULTIPLE STATUS REGISTERS AND LOCK/UNLOCK MEMORY ON SPI CHIPS"**

Google Summer of Code 2016

**Coreboot (Flashrom)**

Feb. 2016 – Aug. 2016

- Designed a unified abstraction of multiple status registers in an SPI Flash-memory chip to provide a consistent interface across diverse chip manufacturers.
- Programmed routines to lock/unlock memory space governed by status registers, handle configuration bits, access/lock OTP memory areas, and automatically generate memory protection maps for a selection of chips. Developed a CLI to expose these features, and finally tested the infrastructure using a Raspberry Pi and a Teensy development board.
- Liaised with a Sales Executive of GigaDevice from China to arrange for engineering samples and add support for GigaDevice SPI chips.

**SKILLS****Programming** Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS**Software** Xilinx Vivado & HLS, MATLAB, Simulink, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, L<sup>A</sup>T<sub>E</sub>X, gnuplot, Mentor Graphics**Hardware** Xilinx Virtex & Zynq SoC, Digilent Nexys4 DDR, Raspberry Pi, Arduino, PIC Microcontroller, TMS320 DSP Chip**Languages** English (TOEFL 114/120), German (B1), Hindi (native)**EXTRACURRICULAR ACTIVITIES****Coordinator, Startup Relations**

IIT Patna

*Entrepreneurship Club*

Apr. 2016 - Apr. 2017

- Served as on-campus mentor to early stage startups, helped develop business plan, choose investor strategy and network with advisers.
- Part of Core Committee for Entrepreneurship Club's annual event, E-Week. Organised guest talks and In-house sessions.
- Delivered presentations as part of In-house Lecture series conducted by Entrepreneurship Club.

**Task Manager, Startup Relations**

IIT Patna

*Entrepreneurship Club*

Apr. 2015 - Apr. 2016

- Worked towards building connections with startups and investors with vision to form investor panel for on-campus startups.
- Part of Organising Committee for Entrepreneurship Club's annual event, E-Week. Organised guest talks, workshops and pitching event.