Hatim Kanchwala

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Education

Apr. 2019 – Sept. 2022
Aachen, Deutschland

M. Sc.Elektrotechnik, Informationstechnik und Technische Informatik
RWTH Aachen Universität
Final Grade 2,1

- Masterarbeit "Field-Programmable Gate Array basierte Echtzeitregelung und -simulation"

Juli 2014 – Mai 2018
Bihta (Patna), Indien

B. Tech.Electrical Engineering
Indian Institute of Technology Patna
Final Grade 7.32 / 10 (indische) = 2,1 (deutsche)

- Bachelorarbeit "Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"

Experience

Apr. 2021 – Dec. 2021
Aachen, Germany

M. Sc. Thesis "Field-Programmable Gate Array based Real-Time Control and Simulation"
Institute of Energy and Climate Research (IEK-10), Forschungszentrum Juelich GmbH

- Developed design using soft-core microprocessors to rapidly prototype control-loop algorithms for FPGA-based real-time simulators of power systems and to allow independent formulation of power system and control-loop models.
- Introduced *control* and *data-logger* soft-cores, each based on MicroBlaze soft-core microprocessor from Xilinx and implemented on Xilinx Virtex Ultrascale+ VCU118 board, respectively dedicated to running control algorithms at switching frequency and logging simulation data at each time step.
- Conceptualised heterogenous architecture using multiple and dedicated soft-core microprocessors, enabling hierarchical control-loop systems and fine-grained administration of real-time simulation.
- Assembled final work product using combination of proprietary Xilinx IPs from Vivado IP Integrator, HLS modules of power systems generated from ORTiS, self-authored Verilog RTL modules and binaries for soft-core microprocessor using Xilinx SDK.

Oct. 2020 – Feb. 2021
Remote

Intern
Institute of Energy and Climate Research (IEK-10), Forschungszentrum Juelich GmbH

- Implemented power sytems models using open-source code-generation tool ORTiS targeted toward High-Level Synthesis for RTL co-simulation and real-time simulation on an FPGA.
- Extended HLS models with memory-mapped AXI4 register interface. Verified hardware models on Xilinx Virtex-7 VC707 FPGA board using remote debugging.
- Developed Makefile pipeline on Linux for ORTiS code generation, Vivado High-Level Synthesis, Vivado IP Integrator and FPGA bitstream generation stages.

May 2019 – Sept. 2020
Aachen, Germany

Student Assistant
Institute for Automation of Complex Power Systems, E.ON Energy Research Centre

- Integrated Xilinx FPGA boards into VILLAS co-simulation platform by designing an architecture built on top of Aurora 8B/10B serial protocol.
- Engineered Tcl-Makefile system of scripts to automate design generation and bitstream compilation.
- Developed bare-metal driver programs in C/C++ for FPGA firmware.

May 2018 – Nov. 2018
IIT Patna, India

Senior Research Fellow
"Underwater Target Motion Analysis with Passive Sensors",
Naval Physical & Oceanographic Laboratory (DRDO), Ministry of Defence, Govt of India

- Implemented advanced tracking filters in MATLAB for the Bearings-only Tracking problem.
- Simulated performance of modern filters on real field manoeuvre data from Indian Navy, and prepared comparative study.
- Concluded that Shifted Rayleigh Filter outperforms other filters in terms of computational complexity while still being superior at tracking target.

Aug. 2017 – May 2018
IIT Patna, India

B. Tech. Thesis "Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation"

Control and Instrumentation Lab

- Designed and implemented a parallel architecture of Sigma-point Kalman filtering algorithms on an FPGA by independently conceptualised parallel routine for Cholesky decomposition in $O(N)$ time complexity.
- Further optimised resource usage of parallel Cholesky decomposition architecture for maximum processor utilisation to achieve $O(\frac{1}{4}N^2)$ resource complexity, as compared to $O(\frac{1}{2}N^2)$ resource complexity of state-of-the-art.
- Implemented parallel architectures using Verilog HDL and Xilinx Vivado on Xilinx Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards, making use of open-source floating-point IPs and Xilinx Vivado IPs.
- Presented final work product to the professors of the department and was one of only two students to receive unanimous 10 / 10 grade from cohort of 50 candidates. Nominated for Best B. Tech. Thesis award from Dept of Electrical Engineering.

May 2017 – Aug. 2017
Google Summer of Code 2017

Student Developer

Free and Open Source Silicon Foundation, "EDSAC Museum on FPGA"

- Built Verilog model of historic EDSAC computer from original but incomplete documentation in collaboration with experts from The National Museum of Computing, UK.
- Programmed and simulated EDSAC architecture and ISA on myStorm Lattice iCE FPGA board using open-source toolchains, like Yosys and iverilog.
- Coordinated with team of students in UK to build hardware imitation of EDSAC memory delay line, teleprinter and paper tape reader.
- Demonstrated final work product at ChipHack 2017 workshop and presented at ORConf 2017 digital design conference in Hebden Bridge, UK, for which full sponsorship was received.

Feb. 2016 – Aug. 2016
Google Summer of Code 2016

Student Developer

Coreboot (Flashrom), "Read/Write Multiple Status Registers and Lock/Unlock Memory on SPI Chips"

- Designed unified abstraction of multiple status registers in SPI Flash-memory chips across diverse chip manufacturers.
- Programmed routines to lock/unlock memory areas, handle configuration bits, and automatically generate memory protection maps.
- Developed CLI to expose new features, and tested infrastructure using Raspberry Pi and Teensy development board.

Skills

Programming Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS

Software Xilinx Vivado & HLS, MATLAB, Simulink, RSCAD, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, LaTeX, gnuplot

Hardware Xilinx Virtex & Zynq SoC, Digilent Nexys4 DDR, RTDS NovaCor, Raspberry Pi, Arduino, PIC Microcontroller

Languages

English	*Hearing* C2	*Reading* C2	*Speaking* C2	*Writing* C2
Deutsch	*Hören* B1	*Lesen* B2	*Sprechen* B1	*Schreiben* B1
Hindi	native			

Volunteering

June 2021 – Apr. 2022
Aachen, Germany

Volunteer

Faiz al-Mawaid al-Burhaniyah (FMB)

- Co-founded Aachen chapter of FMB and led team of volunteers with vision to provide home-cooked and healthy meals to students in and around Aachen at least once a week.
- Organised meal distribution drives on festive occasions, especially Ramadan, to celebrate cultural identity and increase community engagement.
- Co-developed low-cost, sustainable standard operating model to make community effort scalable and reproducible at other locations.

Apr. 2017 – Apr. 2018
IIT Patna, India

Assistant Head Coordinator, Dept of Electrical Engineering

Training and Placement Cell

- Selected by class majority to represent students of Dept of Electrical Engineering.
- Led team in designing placement brochures and helped arrange on-campus placement sessions, tests and interviews.

Apr. 2016 – Apr. 2017
IIT Patna, India

Coordinator
Startup Relations, Entrepreneurship Club

- Led Startup Relations department and served as mentor to early-stage on-campus startups to help develop business plans, choose investor strategies and network with advisors.
- As part of Core Committee, oversaw the organisation of E-Week 2017, the annual national-level event of Entrepreneurship Club.
- Delivered presentations as part of In-house Mentorship Lecture series based on individual technical and business experience in early-stage startups.

Apr. 2015 – Apr. 2016
IIT Patna, India

Task Manager
Startup Relations, Entrepreneurship Club

- Recruited volunteers and helped organise pitching events, workshops and guest talks.
- Assisted in establishing panel of early investors and mentors for on-campus startups.

References

Univ.-Prof. Dr.-Ing. Andrea Benigni
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Institut für Energie- und Klimaforschung,
Forschungszentrum Jülich GmbH
Phone : *+49 2461 61 85523*
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Steffen Vogel, M. Sc.
Team Simulation Infrastructure and HPC
Institute for Automation of Complex Power Systems,
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