Hatim Kanchwala

BORN ON 7TH FEBRUARY 1995 IN INDORE, MADHYA PRADESH, INDIA

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Education

2019 – 2022	**RWTH Aachen University**, M.Sc. in Electrical Engineering, Information Technology and Computer Engineering	Grade 2,1	*Aachen, Germany*
2014 – 2018	**Indian Institute of Technology Patna**, B.Tech. in Electrical Engineering	CPI 7.32 / 10	*Bihta (Patna), India*
2011 – 2013	**Deogiri College**, Class XII Maharashtra Higher Secondary Certificate	82.33%	*Aurangabad, India*
2001 – 2011	**Nath Valley School**, Class X Central Board of Secondary Education	GPA 10 / 10	*Aurangabad, India*

Experience

Master Thesis | "Field-Programmable Gate Array based Real-Time Control and Simulation"

IEK-10, Forschungszentrum Jülich and Institute for Automation of Complex Power Systems — *Aachen, Germany*

Supervisors: Univ.-Prof. Dr.-Ing. Andrea Benigni, Steffen Vogel, M. Sc., Dr.-Ing. Lukas Razik — *Apr. 2021 – Dec. 2021*

- Designing soft-core processor based on Xilinx MicroBlaze for control of real-time FPGA-based simulation of power systems.

Student Intern

IEK-10, Forschungszentrum Jülich — *Jülich, Germany*

Supervisor: Dr.-Ing. Lukas Razik — *Oct. 2020 – Feb. 2021*

- Worked on ORTiS toolchain for High-level Synthesis of power systems design.
- Performed several RTL and FPGA real-time simulations.
- Implemented data triggering to collect and transfer simulation data points.

Student Assistant

Institute for Automation of Complex Power Systems, E.ON Energy Research Centre — *Aachen, Germany*

Supervisor: Steffen Vogel, M. Sc. — *May 2019 – Sept. 2020*

- Worked on integrating FPGAs into the VILLAS co-simulation platform.
- Developed support wrapper modules for Aurora 8B10B IP cores.

Senior Research Fellow — *Control and Instrumentation Lab, IIT Patna*

"Underwater Target Motion Analysis with Passive Sensors"

Supervisor: Dr Shovan Bhaumik, Sponsor: Naval Physical & Oceanographic Laboratory (DRDO) — *May 2018 – Nov. 2018*

- Implemented advanced filters for Bearings-Only Tracking problem - Distributed Extended Kalman Filter, Shifted Rayleigh Filter, Particle Filter with Unscented Kalman Filter and Shifted Rayleigh Filter proposals, Particle Filter with MCMC, and Regularised Particle Filter.
- Simulated performance of these filters on actual field manoeuvres provided by sponsor, and prepared a comparative study. Shifted Rayleigh Filter outperforms other filters in terms of computational complexity while still being superior at tracking target.

B.Tech. Thesis | Nominated for the Best B.Tech. Thesis award from Dept of Electrical Engineering

"Hardware Architecture of a Family of Sigma-Point Kalman Filters for Bayesian Estimation" — *IIT Patna*

Supervisor: Dr Shovan Bhaumik — *Aug. 2017 – May 2018*

- Developed parallel architecture of Sigma-point filtering algorithms like UKF, CKF, etc.
- Designed and implemented on FPGA a parallel architecture to compute the Cholesky decomposition of a positive-definite matrix in $\mathcal{O}(N)$ time complexity.
- Further optimised resource usage of parallel Cholesky decomposition architecture for maximum processor utilisation to achieve $\mathcal{O}(\frac{1}{4}N^2)$ resource complexity, as compared to $\mathcal{O}(\frac{1}{2}N^2)$ resource complexity of state-of-the-art.
- Using parallel Cholesky architecture, formulated and implemented linear time complexity matrix inverse routine to compute covariance inverses required by sigma-point filtering algorithms.
- Implemented Gaussian RNG based on CDF Inversion method using FPGA amenable LUT-SR Uniform RNG.
- Implemented all the parallel architectures using Verilog HDL and Xilinx Vivado on Xilinx Zynq-7000 ZC702 and Digilent Nexys4 DDR FPGA boards. Made use of open-source floating-point IP and several Xilinx Vivado IP.

Student Developer, "EDSAC Museum on FPGA" | Presented at ORConf 2017, Hebden Bridge, UK

Free and Open Source Silicon Foundation *Google Summer of Code 2017*

Mentor: Dr Jeremy Bennett *May 2017 – Aug. 2017*

- Built a model of EDSAC from original, albeit incomplete documentation, and from correspondences with members of "The EDSAC Replica Project" team (TNMOC, Bletchley Park, UK).
- Replicated EDSAC architecture and ISA on myStorm Lattice iCE FPGA board using Verilog HDL and open-source toolchain Yosys.
- Designed and implemented modified-UART communication protocol for external extensible I/O interfaces.
- Helped a team of students in UK build hardware reproduction of EDSAC memory delay line, teleprinter and paper tape reader.
- Final work product used at ChipHack 2017 workshop and presented work at ORConf 2017 conference during Wuthering Bytes festival in Hebden Bidge, UK.

Student Developer, "Read/Write Multiple Status Registers and Lock/Unlock Memory on SPI Chips" *Google Summer of Code 2016*

Coreboot (Flashrom) *Feb. 2016 – Aug. 2016*

- Designed multiple status registers model to abstract chip diversities across manufacturers into single consistent interface.
- Developed routines to lock/unlock memory space governed by bits in status registers, handle configuration bits, and automatically generate memory protection maps for some chips.
- Added functionality to access/lock OTP memory areas.
- Developed CLI to expose new infrastructure. Tested on physical GigaDevice SPI chips using Raspberry Pi and Teensy.

Summer Intern *New Delhi, India*

Aficionado Ventures *May 2016 – July 2016*

- Aficionado was a startup helping restaurants procure quality produce from competitive collection of vendors.
- Designed reactive backend architecture - MeteorJS server, MongoDB database, Heroku/mLab web hosting, and Cordova for cross-platform mobile apps.
- Implemented MVP-stage marketplace platform from scratch with bilingual search for products in English/Hinglish.
- Worked with business team to conduct market research on restaurants and vendors.

Projects

Biometric Attendance System Suitable for Economic and Low-power Limited-connectivity Remote Deployment *Innovation Centre, IIT Patna* *Jan. 2015 – Oct. 2015*

- Interfaced Atmel AT89S51 8051 microcontroller with R305 fingerprint reader and SIM900A GSM/GPRS module over serial port via multiplexer.
- Developed user interface using 16 × 2 LCD and keypad.
- Developed firmware in C and ASM. Microcontroller operations simulated in Proteus.

Achievements

2018	**Nominated for Best B.Tech. Thesis award**, Dept of Electrical Engineering	*IIT Patna*
2017	**Received full sponsorship to present "EDSAC Museum on FPGA" at ORConf 2017 open-source digital design conference**	*Hebden Bridge, UK*
2014	**Secured All India Rank 4997 (99.6156th percentile) in JEE Advanced**, All India Joint Entrance Exam	*Pune, India*
2010	**Received silver medal**, International Informatics Olympiad 2010	*New Delhi, India*
2010	**Secured rank 25 and received gold medal in the final round**, 9th National Cyber Olympiad	*New Delhi, India*
2008	**Secured rank 156 in the final round**, 7th National Cyber Olympiad	*Aurangabad, India*
2006	**Secured rank 196 in the final round**, 5th National Cyber Olympiad	*Aurangabad, India*

Skills

Programming	Verilog, C/C++, Python, Assembly, JavaScript, Java, Shell, HTML/CSS
Software	Xilinx Vivado, MATLAB, Simulink, NI LabVIEW, GNU/Linux, git/GitHub, gdb, Verilator, LaTeX, gnuplot, Mentor Graphics
Hardware	Xilinx Virtex & Zynq-7000 SoC, Digilent Nexys4 DDR, Raspberry Pi, Arduino, PIC Microcontroller, TMS320 DSP Chip
Languages	English (*TOEFL 114/120*), German (*A2*), Hindi (*native*)