Off-Spec notes

These notes are comprised of various speculations on recently discovered processor cores, such as the Andes A25 processor. They are not necessarily draft candidates for a future Bunch of Wire spec, pull request, nor even an implementation of one. They are more rambling thoughts with poor or bad math that has not been verified. Nonetheless, they are an essential supplement to considering Bunch of Wires processors that could be integrated with memory, radio, and other D2D connections, as this chiplet design takes a holistic system approach to power consumption and design.

Bunch of Wires spec is 0.25-1 pJ/bit. Converted into bytes, that's 2pJ-8pJ/byte and possibly 1W= 1 J/second= 8 Terabit/s. Some specs (not BoW) claim as low as 0.2pJ/bit. Whether running it at fast speeds (1Ghz,etc) facilitates the efficiency is unclear, but its likely that running each wire at 1Megahertz instead of 1 gigahertz will in closer to 1000x less milliwatts except when things like impedance and leakage play a role under 600mV. But also:

2nJ-8nJ/Kilobyte
2uJ-8uJ/Megabyte
2mJ-8mJ/Gigabyte

Also, I found that there is a half splice mode for low data rates, which only requires 8 data wires plus 2 for clock, instead of 16+2. It's unclear whether there are any benefits to using 8 if there are other benefits at 16 for keeping the mHz low(could hinder leakage or increase it)

Assuming that is all true, 8 wires could run at 2MHz and transmit 16MHz, or 32MHz at DDR clock rate, and 32Mbps or 64Mbps on 16 wires. With 8MB of RAM chip, that would be like flushing the entire address space in one second (but likely needs faster, 50ns to run smoothly.) A nano second is 5% of a microsecond, and a microsecond is a millionth of a second (I can see why they use GHz).

But when the RAM size is only 8MB, that might not matter much, plus it doesn't need to flush everything.

I am not sure how much wattage that is, but as the Ambiq Micro has 576uA for a 96Mhz processor (6uA/mHz), 8uJ/Megabyte x 32 = 256uJ, or 256uW ÷ 0.7Volts (with is the spec of BoW)~365uA.

Seems pretty close to that. I think they chose 0.7V because its the closest they could get without needing special memory cells under 600mV...(as mentioned in the semis engineering article "NTV gets a boost").

Even at 0.7V it might be possible to keep the consumption down to levels that doesn't consume milliwatts but it seems a lot harder. Still, it'd be interesting to see something around 30Mhz cruise on a 386-like processor or RISC based with 0.7V and see if it can maintain around 1mW. The Andes A-25 32-bit RISC-V processors include MMUs and are rated for 20uW/Mhz, which means it consumes
100uW @ 5MHz
500uW at 25MHz
1mW at 50MHz
2mW at 100MHz
10mW at 500MHz
and 20mW at 1000MHz. But I don't know if that includes RAM. Still, seems competitive with Ambiq (considering it has a MMU!)

By comparison, the MicroMagic RISC-V 64-bit processor unveiled in December of 2020 was claimed to have reached 10mW at 350mV at 1GHz. The Andes A25 runs between 0.81V-.9V, possibly accounting for twice the power consumption, as 20uW x1000 MHz is 20mW.

Whether it is possible to underclock the A25 processor from 1Ghz to 50 or 100MHz while maintaining 0.8V or 0.7V and 20uW/MHz remains to be seen. The Dynamic power unit (uW/MHz) could refer to the average consumption, and may be less “MIPS/watt” efficient at lower speeds.

Andes also offers a pre-integrated Platform for the A25:
A25 with AE350 Platform: Pre-integrated A25, PLIC, Debug Module, plus AXI/AHB Platform

Whether this contains all the I/O necessary to interface with other peripherals, such as nB-IoT wireless radios and the like is unclear, but having sufficient wiring capable of reaching modem speeds needed for 128Kbps, for example, may need 1Mbit wire (or bunch of wires – x8 or x16 @ 64Kbps or 128Kbps each, for example). Qorvo’s new QM55011, for example, which operates at 2.5V and can transmit around 127Kbps D/l and 158.5Kbps U/l, like Quectl’s BC660KGLAA-I03-SNASA. Can it use IoT? Sure. Can it browse the web? Why not? Surf like it’s 1999.