Project name (max. 100 characters) The Autarkic Standard for Integrated Chiplets (The ASIC)

Abstract: Can you explain the whole project and its expected outcome(s).

Energy autarkic hardware is an emerging design principle in devices such as IoT and wearables. General purpose processors with energy autarkic system design have yet to be commercialized. Energy autarky enables energy independence at the portable level, with solar panels on phones and laptops, but also other power sources. Energy autarky treats energy similar to zero-trust computer security, thus does not expect reliable access to energy grids. The design methodology of energy-autarkic hardware necessitates some of the most leading edge technologies, such as near-threshold voltage processors (sub 30nm nodes, ultra-low refresh (<10fps for low priority notification apps) low-power displays with non-emissive backlights, ultralow power nbIoT/LTE modems with advanced idle states such as eDRX, heterogeneous chiplets, Libre EDA tools, and low power microkernels. The integration of extremely specific power limits for all hardware components ensures mobile devices can operate even at 100% CPU utilization, without a net decrease in lithium ion capacitance.

Have you been involved with projects or organisations relevant to this project before? And if so, can you tell us a bit about your contributions?

I have been active in an e-ink advocacy forum called EI2030, in 2021, and maintain contacts with community members interested in alternatives to non-emissive displays such as e-paper and reflective displays.
https://alexsoto.dev/static/ei2030/2021-04-25/slides.html#/4
https://alexsoto.dev/slides.html

My contributions are primarily informational web search-based using publicly available information:
https://hackaday.io/project/177716-the-libre-autarkic-laptop

A directory of links:
https://github.com/EI2030/Low-power-E-Paper-OS/blob/master/Hyperlinks%20and%20Scratchpad.md

Compare your own project with existing or historical efforts.

This project was started for the single purpose of establishing an ultra power low-power alternative to the National Science Foundation (U.S)-funded and Dutch Ministry of Economic Affairs-funded Protean Supersensor:

https://protean.systems/
https://protean.systems/supersensor_sensys22.pdf

The reason this project has an advantage is that Protean's SuperSensor is an energy efficient platform, but it is not as low power as possible, nor does it specifically address general purpose applications such as voice and text applications. A power-first approach latter opens up more opportunities for even more low-cost and more interoperable hardware standards, including NLNET funded projects such as LibreEDA and LibreSoC, LibreSilicon, LibreCellular, LibreSiP. Additionally, this project can help bridge the Digital Divide.

Another difference with SuperSensor, is that its capacitor-only based design, rather than lithium-ion capacitor based design, uses complex adaptive power management for intermittent computing. While

batteryless computing is certainly a novel and ideal platform to strive towards, the current implementation requires a large effort in re-writing kernel and application thread management around an entirely persistent state system (non-volatile).

In contrast, lithium-ion capacitors appear to allow for a continuous discharge of battery, albeit slightly less efficient than capacitors, but do not require extensive rewriting the existing power management states that have been developed for embedded linux and RTOSes. Capacitors, on the other hand require frequent recharges, for short powered tasks.

This project aims achieve a simpler set of goals than the Protean, namely just the first and third, with a different appoach in the third (from p.4):

"Our goal is to (i) provide multiple hardware options in terms of computing modalities, peripherals, and harvesting technologies, (ii) enable energy efficient inference applications, (iii) provide resilient runtime support for managing program state and memory across power failures,
and (iv) allow rapid development and testing of different configurations of machine learning models."

Re: (i) I agree with multiple hardware options- add ons, modular designs - both at the EDA stage and post-SoC level
Re: (ii) Inference is a ML technology and not a priority for voice/text technologies
Re: (iii) I agree with power management, but I do not agree with debatably complex systems. For example, PWM is a low cost power management system. MPPT tracking is more expensive, thus alternative power saving techniques include porting the most energy efficient applications (often legacy-based) over feature rich applications. This system does not necessairily use PWM, but is an example where low cost alternatives may not significantly affect efficiency and still provide excellent autarkic system capabilities

It is unclear if Protean system seeks to define battery free devices as ones excluding any lithium, to support a purist view. Lithium ion capacitors (LICs) contain only a small amount of lithium at the anodes. Furthermore, it seems like conventional operating systems (RTOS, linux) can run on LICs. They are duty-free, and can be shipped anywhere in the world that is legal to do so. Furthermore, tantalum, a conflict mineral, is present in some capacitors, thus lithium free capacitors are not necessarily sourced more ethically than capacitors containing trace amounts of lithium.
https://www.electronicdesign.com/technologies/components/article/21799667/conflict-minerals-and-the-tantalum-capacitor-supply-chain

Explain what the requested budget will be used for?

The first expenditure is to hire a computer engineer to draft the open standard for a modular, "Chiplet-based System In a Package." This would involve defining interposer framework for chiplets that connect solar panel power management systems, integrated circuits, lithium ion capacitors, as well as the instruction set architectures that can support either a heterogeneous carrier board, or monolithic versatile system on a chip for general purpose computing. Thus, the funding request is to identify a specialist who can identify the electrical requirements to develop a VLSI or glue-logic based ICs for solar-integrated system on a package.

While I have identified some of the lowest-power components commercially available over the course

of two years, a specialist or specialists would be needed to identify electric wiring standards for energy generation, storage, memory, and display, using a unified autarkic thermal power limit. Thus the TDP establishes the framework for the VLSI, while the engineer defines the ratio of each component's TDP to maintain a continuous operation. As capacitors are unable to provide a continuous discharge, lithium ion capacitors appear to offer both continuous discharge, similar to a battery, as well as a long cycle life.

A tentative list of leading components:

1. Solar Power & Battery Management
https://www.tindie.com/products/jaspersikken/solar-harvesting-into-lithium-ion-capacitor/
https://www.powerfilmsolar.com/products/development-kits/solar-development-kit

2. Microcontroller & Memory
https://ambiq.com/apollo4/ 5uA/Mhz

3. Linux/RTOS software development--EPOC/EKA2? https://en.wikipedia.org/wiki/EKA2
https://en.wikipedia.org/wiki/EPOC_(operating_system)
QNX microkernel http://www.qnx.com/news/pr_2471_2.html

4. E-paper/Reflective Display driver
https://www.youtube.com/watch?v=BD4At2-e87E SHARP Memory in Pixel 4.4" RLCD LPM044M141A
between 250uW and 2mW:
https://os.mbed.com/media/uploads/JDI_Mbed_Team/lineup_from_draft_rev3_jdi_gr_mip_reflective_color_lcd_and_standard_products_20180219-3.pdf

The cost of these devices, while more expensive than a mass-produced components, are essential to demonstrating proof-of-concept userspace applications. The solar Gameboy prototype from 2020 is another proof of concept autarkic device, although its intermittent design leaves a lot remaining for practical use. https://www.freethegameboy.info/

Another difference from the Protean system is that this system is designed to use as little power as possible, rather than prioritizing efficient management of power. The difference is subtle, as low-tech hardware components and software can sometimes be repurposed in a novel or hybrid system. The project understands the need for high tech components, but also does not place emphasis only on novel solutions. In other words, legacy software/ hardware components may be preferred over newer components, since the power consumption may be less. The interoperability of the chiplet design ideally provides the most options for either.

What are significant technical challenges you expect to solve during the project, if any?)

Significant challenges include porting EKA2 kernel and uClinux to Ambiq Apollo4 under 2MB of RAM, developing a general purpose display controller compatible with memory-in-pixel displays, developing an interoperable interposer that supports various low power antennas, such as LPWA BC660K-GL NB2
https://www.quectel.com/product/lpwa-bc660k-gl-nb2, integrating a PMIC such as Epeas' AEM10941 or TI BQ24650/25570. While these components are not necessary for an autarkic standard, they convey the essence of what makes this platform's autarkic capabilities possible. The sum of the parts is less

than the whole, because Moore's Law has never allowed for a convergence of high-tech components to be integrated in such a manner before that is able to generate a net increase in energy storage, like the recently established fusion power. Screening for low-power components is a pre-condition for autarkic design. As the most power-intensive components have been identified (display, wireless, and memory), the sum of all the parts have been shown to consume less than the square area of a small solar panel (50mmx50mm, or much larger can fit a laptop). Thus, as long as the sum of the parts' consumption is less than the average capture of soar irradiance, there can be a net increase in energy storage. Strategies to allow at least one charging session per day can help create a buffer from low “battery” levels for the LIC in low-light conditions.

Ambiq Apollo4 5uA/mhz at 192Mhz: 960uA
4.4" Japan Display <3mW
Quectel lpwa-bc660k-gl-nb2:
"Power Consumption (Typical) : 800 nA @ PSM 0.11 mA @ Idle (DRX = 2.56 s) 0.038 mA @ Idle (eDRX = 40.96 s, PTW = 10.24 s)"
“67 mA @ Connected Tx 0 dBm 330 mA @ Connected Tx 23 dBm"

"LICs combine many advantages of Li-ion batteries and supercapacitors making it a perfect choice for batteryless IoT applications.

The AEMLIC is a 15x20mm board with the AEM10941 Solar Harvesting IC from E-peas. It efficiently converts solar panel energy into LIC charge, it even works with indoor light. It has a regulated output that is enabled when the LIC has sufficient charge, and a low voltage warning that informs the user of impending shutdown when the LIC runs low. It easily integrates in other projects because of the castellated via's, and when soldered onto 0.1' pitch headers it fits in a bread board."

"The AEMLIC charges the capacitor up to 3.78V and the output is enabled down to 2.49V. If your application draws 30mA from the 3.3V output, then it will run for: 250F(3.78V-2.49V)90%/0.03A= 10750s = 2.7 hrs. A display that runs at less than 9mA and an MCU that runs at 1mA could thus last over 8 hrs (not counting inputs or wireless).

While the AEMLIC is designed for IoT, I believe the system is ideal for batteryless phones, because systems today can be built using low power microcontrollers (a precedent is the Mudita Cortex M7), and low power LTE modem: (BC660K-GL has Max. 127Kbps downlink / 158.5Kbps uplink: 127Kbps would be more than enough speed for a realtime SIP Phone and text application)

https://en.wikipedia.org/wiki/Bit_rate#Other_audio (minimum is 450 bits/sec, recommends 1.2kbit/s for Codec 2)

700 bit/s – lowest bitrate open-source speech codec Codec2, but barely recognizable yet, sounds much better at 1.2 kbit/s
800 bit/s – minimum necessary for recognizable speech, using the special-purpose FS-1015 speech codecs
2.15 kbit/s – minimum bitrate available through the open-source Speex codec
6 kbit/s – minimum bitrate available through the open-source Opus codec
8 kbit/s – telephone quality using speech codecs
32–500 kbit/s – lossy audio as used in Ogg Vorbis)

Indoor Series

LL200-3-37

1000 lux:
1.089mW
0.419mA
2.6V

200 lux:
0.166mW
0.079mA
2.1V

Classic Application
ONP1.2-12x24

100% Sun
4mW
3.33mA
1.2V

25% Sun
0.9mW
0.7mA
1.2V

https://www.powerfilmsolar.com/products/development-kits/solar-development-kit (TI BQ25570 PMIC)

EPEAS-CAPXX
Indoor Series
LL200-2.4-37

1000 lux:

0.462mW
0.220mA
2.1V
200 lux:

0.07W
0.044mA
1.6V
Classic Application
MPT2.4-21

100% Sun

32mW
14.2mA

2.4V
25% Sun

7.7mW
3.2mA
2.4V

https://www.powerfilmsolar.com/products/development-kits/solar-development-kit-with-e-peas-pmic-cap-xx-supercapacitors

My estimate is that as long as the display is able to use less than 2mW, a conservative estimate would be that the phone could produce a net charge of 1mW with an idle display. The microcontroller uses less than 1mW. In low light conditions, the refresh rates could be reduced to 1fps or even switch to a bistable display such as epaper (having both, of course would increase the cost).

Another long-term goal is depending less on the ARM-ecosystem and adopting a libre-soc capable of sub 40nm nodes (e.g. Skywater is at 90nm, TSMC/Intel/Samsung may be able to license foundry space for a RISC-V using near threshold voltage tooling)

Companies such as Ventana appear to offer advanced RISC-V designs using disaggregated chiplets, thus potentially decreasing the cost to purchase or license IP components for a potentially interoperable hetergeneous chiplet, using otherwise Libre standards.

Describe the ecosystem of the project, and how you will engage with relevant actors and promote the outcomes?

Over the past two years, I have been engaging with companies and universities in this project. However, one of the hurdles appears to be that some institutions are more likely to collaborate with other institutions. With businesses, there is also the marketability component. Thus businesses will not have much interest to collaborate unless they can establish a return on investment. Thus, one of the reasons this project could benefit from NLNet is sponsorship and recognition by a major institution. The liaison for this outreach can be you.

If funded, I would immediately seek someone who would be interested in drafting a specification for a chiplet, so that someone in each specialty, such as solar power management (at Epeas or TI) can be in contact with a systems designer, and a display controller developer, can work on a low power driver for memory in pixel. I would also need a kernel developer working with the display developer, as those would be closely integrated. Companies such as Bootlin, Konsulko, have offered to port linux to Ambiq Apollo4. In 2021 Bootlin quoted around 60 thousand Euros. This figure has likely increased. Symbian's EKA2 kernel, according to its developer, Dennis May, is compatible with Cortex M4 (from Chapter 17 in Jane Sales Symbian programming textbook). Since these technical challenges are far beyond my expertise, I am probably not the best person to consult or mediate contact. However, there is a lot of existing source code that is freely available online, such as Symbian, and it may be worthwhile to reuse existing codebase rather than rewrite entirely new operating systems and kernels.