A Heuristic Method for Designing Solar Circuits

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***Abstract* – "Solar circuits" is a nomenclature for a photovoltaic panel, power manager, and microprocessor integrated on a System on a Chip that meet a predefined thermal design power envelope and volumetric design envelope for energy and space-constrained mobile devices such as cell phones, tablets, and laptops. The emerging market of Internet of Things, for over two decades, has prioritized interfaceless devices to either operate within extreme energy budgets or to rely on remote clients/terminals for offloading compute-intensive tasks. An emphasis on designing with energy generation and integration with interfaces in solar circuits expands the accessibility of IoT and mobile computers to developing markets as well as solutions requiring a "local first" design ethos. Solar circuit design will be contextualized within the precedent of Software Defined Hardware to specify an autonomous or batteryless capability requirement that utilizes energy harvesting or energy scavenging to meet "just enough" application needs. Furthermore, setting limits on system power consumption allows a solar circuit to serve as a proxy or "litmus test" for measuring (and subsequently demonstrating) the progress of Moore's Law within solar constraints. Performance of general purpose microprocessors that can be solar powered in mobile form factors is estimated to be consistently 25-30 years behind (in MIPS/W/mm^2) leading edge chips such as AMD Instinct and Apple A17. A number of heuristic methods are described in this paper to estimate the solar circuit requirements (in transistors, memory, and OPS) to run general purpose operating systems such as Microsoft Windows 95 and Linux 5.1 in modern, commercially viable process nodes, such as Global Foundries 22nm FD-SOI, TSMC's 22 and 12nm ULL, or Intel's 16nm FF– processes that all utilize low leakage.**

Index Terms – Solar power, microprocessors, Thermal Design Power (TDP), Software Defined Hardware (SDH)

INTRODUCTION

Microprocessors in recent decades have undergone major shifts in energy profiles to achieve performance gains after the decline of Dennard's scaling in 2006 with the development of parallel processing, dark silicon, and dynamic voltage and frequency scaling (DVFS). While multi-core consumer and HPC systems still rely on transistor scaling to see gains in certain performance, setting limits to upgrade paths for operating systems and software reliant on future hardware upgrades offers sustainable solutions towards software as an appliance (e.g software that may require little to no maintenance)[1].

Existing efforts to develop software appliances rests partly on a concept called "good enough computing" or "just enough operating system" (JeOS)[2][3][4][5]. Formulated in 2009, the term saw usage in the late oughts and early 2010s during the netbook era but also the Intel Core i-series & AMD Athlon processor generation that led to significant gains in desktop performance. An earlier term (or plea), "lean computing," originated in the 1990s after an observation by Niklaus Wirth, who stated that software is getting slower more rapidly than hardware is becoming faster[6].

The concept of "good enough" computing suggests that containerized applications, whether as a software appliance, may not require a major hardware upgrade for several generations of software versions/ feature additions. The proposition that hardware can outlast both applications and operating systems is not rooted in business strategy, but consumer economics. There are often unrelated feature additions that serve as an impetus for hardware upgrades. For example, designing hardware to last longer, or be more adaptable to newer operating system requirements can be difficult due to the unpredictability of hardware security features that ensure official compatibility (such as TPM 2.0 modules for Windows 11 support on motherboards that support it).

HEURISTIC METHODS TO CALCULATE MIPS/W/MM^2

I. Solar computing precedents- calculators and the Pentium

The first demonstration of efficient process node shrinkage coupled with solar power was in the 1970s, when SHARP released the first solar powered calculator- the EL-8026[9]. In 2011, Intel demonstrated a solar powered Pentium, capable of running linux, Quake, and Windows 95[10]. Using transistor count as a proxy for Dennard's scaling, a heuristic method can be applied to a 3nm node as the current leading edge node to estimate the power consumption of a square millimeter of die space. The Apple A17 processor, which in 2024 holds the best in class title for transistor density, is reported to contain over 183,000,000 transistors in 1mm^2. Using this figure, logic and memory can be approximated based on the number of transistors typically

required for CPU, SRAM/cache, and DRAM. Logic and DRAM can use as little as 1 transistor/ce, whereas SRAM may use up to 6-10T per cell. Furthermore, due to the breakdown of Dennard's scaling, a 3nm chip may not be expected to utilize 100% of a square millimeter at any given time due to heat constraints and thermal runaway prevention. Thus the dark silicon utilization of a square millimeter die space may not represent a 1:1 scaling of concentrated power scaling. Nonetheless, using a 10T/1C ratio of SRAM for a processor, cache gates can be powered down to conserve power and thus heat. Using this approximation, a Pentium II Dixon is said to use 13 million transistors for 256KB cache (~6T/C), and 27 million transistors overall†‡. Assuming 156,00,000 transistors would be remaining for DRAM, or a combination of large caches and extra power saving modes, a 1mm^2 die would be expected to support up to 16MB of DRAM using 1T/1C (16MB is equal to 134 million bits) [22]. As 64MB is 536,870,912 bits, a 3nm node would require 4mm^2 die space using A17's process node technology (a max of 732 million transistors, using 183m x 4 as an estimate in 2mm x 2mm squares). Windows XP, which was released in 2001, had a 64MB RAM requirement, as did Ubuntu 4.04, one the first mainstream releases of a linux desktops[11][12]. Since transistor density may prohibit 100% utilization of transistor power for long periods of time, the DRAM cache may be limited to 64MB if 1T/1TC to provide adequate heat dissipation.

By adapting this heuristic for transistor scaling, leading edge nodes may be able to be designed to run general purpose processors within 1mm^2 of die space, which can correlate to a power consumption of less than 10 milliwatts. Dennard's scaling can be compared to the 6 million transistor Claremont (a Pentium P54C in both 32nm and 22nm that used 147mm^2) in 2011 and 2012 at ISCCC, demonstrated by Intel, which was said to consume between 2mW-10mW from 10-60MHz (and up to 915MHz using higher consumption)[13]. By tracing the die space scaling along with transistor count, one can make the estimate that leading edge nodes can be designed to solar power microprocessor technologies from as recent as 18 years (1993-2011), but more practically, 25-30 years with mature process nodes that may be commercially viable. For example, while the 2011 Claremont used level shifters to offer three modes of speed, a fixed speed Pentium might only require 3.1 million transistors as in the original P54C. The node shrink from 32nm to 3nm in 2024 might not suggest a proportional 10x reduction in power consumption, but at the very least, that a 27.4 million transistor Pentium II might be able to fit in the same 147mm^2 die space of the 2011 Claremont (this large die space was said to support the the motherboard compatibility, rather than intrinsic requirements of the chip itself). Using that heuristic, one might be able to reason that approximately 7/8ths of 147mm^2 die space can be reserved for embedded DRAM (eDRAM), or extra SRAM to utilize up to 128MB of RAM. Whether or not this would fit in a 4mm^2 or 8mm^2 die space (for 128MB/1,073,741,824 bits) depends on the actual density of 3nm chips. Prior efforts to integrate graphics have shown similar density increases[14]. This heuristic example will be the basis for additional examples in this paper. The power consumption of a 3nm Pentium II may be analogized to the 60MHz Claremont, but the measurement of system power consumption to include solar powerable 32nm RAM was never tested for the ISSCC 2011 nor 2012 conference. Therefore, this heuristic analogy can serve as the estimate for a future test.

TABLE I

Processor	Transistor count	Year	Designer	Process (nm)	Area (mm^2)	Transistor density ($tr./mm^2$)
Pentium (32-bit, 16 KB of caches)	3,100,000	1993	Intel	800 nm	294 mm^2	10,500
Pentium II Mobile Dixon (32-bit, caches)	27,400,000	1999	Intel	180 nm	180 mm^2	152,000
Pentium 4 Northwood (32-bit, large cache)	55,000,000	2002	Intel	130 nm	145 mm^2	379,000
Apple A17	19,000,000,000 [187]	2023	Apple	3 nm	103.8 mm^2	183,044,315

FIGURE I

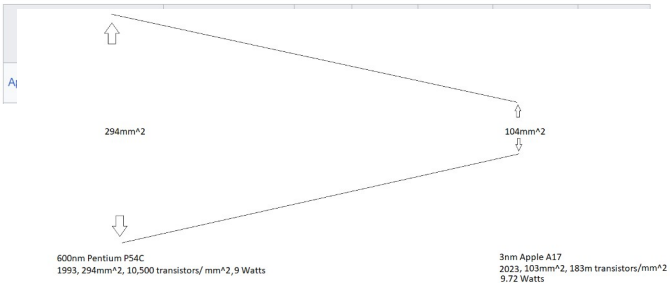

TABLE 2
PREDICTED SCALING AND SYSTEM REQUIREMENTS FOR SOLAR-CAPABLE CIRCUITS

RAM (MB)	Operating System	Processor	Process Node (nm)	Power Consumption (mW)
8*	Windows 95	PENTIUM 1 60MHZ	32	10
64	Windows XP	PENTIUM II 233MHZ	3	10
64	Ubuntu 4.04	PENTIUM II 233MHZ	3	10
512	DSL 2024	PENTIUM IV HT 3GHZ	0.5**	10

*off chip, untested in Claremont
** projected 5 Angstrom process node in 2037 [15]

According to Table 2, Dennard's scaling is projected to proportionally allow roughly equal consumption of the 2011 Intel Claremont with a 3nm Pentium II, with the added benefit of on-chip DRAM (at 3T/1C or less) in quantities of

†256KB is equal to 2,048,000 bits[21]
‡ According the PIV Northwood, 256KB cache utilizes approximately 13 million transistors[16]

64MB or less. In other words, if Intel chip designers ported the PII Dixon processor, a 27 million transistor chip to 3nm, an additional 65 million eDRAM transistors would be expected to fit the same die space that was previously measured to power an Apple A17 chip with a 181 million transistor/mm^2 density and is expected to consume 10 milliwatts, using the number of transistors: 19 billion divided by reported power consumption of the chip, 9,700 milliwatts, to reach 1.958 million transistors per mW (Figure 1). However, since the A17 is clocked between 1GHz-3.6 GHz, a 233MHz PII at 3nm would not be expected to consume the nearly 10 milliwatts per 20 million transistors, but rather, 100-180 million transistors per 10 milliwatts at approximately 1/10th the speed (233Mhz/2.5GHz). Also, since the the A17 uses ARM v8.6 architecture, comparing it to x86 Pentium I & II OPS is not exact and may not run correctly beyond speeds they were designed for. A projected power consumption estimate is also made for a 5A (5 Angstroms, following Intel's 18A & 14A nomenclature) process node, using an early Pentium IV Northwood with Hyperthreading as CMOS scaling is still expected to progress in the next two decades before transitioning to more economical or efficient computers, such as graphene, photonics, or quantum computing[16]. The 2002 Northwood, with 55 million transistors, first appeared on the 130nm node, which was new at the time. It featured a 512KB cache, which increased the transistor count from 42 million to 55 million. A 1/6th reduction in node size from 3nm to 0.5nm may allow approximately 6x more die space for the 512MB RAM requirements of modern operating systems utilizing linux kernel 5.1 (for example, DSL 2024 averages 90-120MB of RAM in idle, and is significantly less resource demanding than Lubuntu, which briefly recommended RAM requirements as high as 2GB in 2018 [17][18]. Toolkit OSes, such as Tiny Core Linux, utilize as little as 64MB-128MB RAM on a P5-75 [19][20].

II. "Good Enough" Transistor Density as a MIPS proxy

Common desktop applications such as e-mail, web browsing, and multimedia are increasingly capable of utilizing lower thermal design envelopes in systems that minimize support for advanced software packages or platforms. However, system designers may not prefer to sacrifice a "one stop shop" performance target to support only the most essential applications or lightweight interfaces for the highest portability. Systems that limit multimedia and compute intensive software can extend battery life and communication times for highly mobile users. Projections of energy consumption in Table II are rough estimates of past, current, and future manufacturing capabilities, but are not expected to be far off the mark. With that said, software and operating system designers may want to plan product development for chips that can fully support not only mobile versions, but "solar mobile" versions of packages or dependencies that are optimized for limited recharging. This approach can maximize accessibility via portable, modular, and interoperable software products.

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