Current-mode Temperature Compensation for a Differential Logarithmic Amplifier in 180nm BiCMOS

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***Abstract*—This paper presents a new approach for the temperature compensation of a diode-based logarithmic amplifier used in on-chip power measurement circuitry. The output voltages of the amplifier are first converted into current domain. Then, the temperature compensation is realized using a translinear circuit and a PTAT current source. As most millimeter-wave systems on chip already contain a PTAT current generator, and the temperature compensation uses only devices readily available in commercial BiCMOS technologies, the presented approach is viable for many different designs. Simulation results of the compensation circuit together with an exemplary log amp show cancellation of the temperature dependence between −40 °C and 125 °C with a dynamic range of 50 dB.**

***Index Terms*—Logarithmic amplifier, temperature compensation, translinear circuit.**

I. Introduction

The logarithmic amplifier (log amp) is a basic building block of analog signal processing when dealing with exponential sensor characteristics. Sensors such as photo diodes or power detectors have outputs with large dynamic ranges. Therefore, either high-quality analog-digital converters (ADC) are needed to process these output signals or a compression stage has to be placed in front of the ADC.

This compression can be realized by a logarithmic amplifier based on inverting the exponential characteristic of a pn diode [1], also called a logarithmic converter. An inherent problem of this approach is that the resulting output voltage is linearly dependent on temperature. A temperature-dependent offset at the log amp output can easily be removed through digital calibration by measuring the output voltage with the input switched off and subtracting it from the measurement results. However, the slope of the log amp's input-output characteristic also depends heavily on temperature and is significantly harder to calibrate digitally. Therefore, temperature-compensating circuitry usually has to follow a logarithmic amplifier.

A proven method achieving this temperature compensation is to feed the log amp's output to an amplifier whose gain is set by temperature-dependent resistors [2]. With these resistors, the gain can then be designed in way that it cancels the log amp's temperature dependence. The obvious disadvantage of this approach is that precision resistors with a suitable temperature behavior have to be available to the circuit designer. This is usually not the case for standard CMOS and BiCMOS processes.

Other approaches rely on the I-V characteristic of a MOS transistor in linear region [3], [4]. In first-order approximation, the drain current in this region is proportional to the product of gate-source and drain-source voltage. By, for example, applying the log amp output at the drain and designing a bias circuit providing a gate-source voltage linearly dependent on temperature in an opposite way, the circuit can be sized so that both temperature dependences cancel in the drain current. The draw-backs of these approaches usually lie in the difficulty of keeping the transistor firmly biased in linear region under all operating conditions. Furthermore, modern submicron technologies suffer from non-ideal transistor characteristics deteriorating the circuit's linearity performance.

In this paper, we present a current-mode temperature compensation scheme for a differential log amp adapted from [5] that will be used for compressing the output range of a millimeter-wave power detector. The output voltage of the logarithmic amplifier is first converted into a single-ended current. A PTAT current is then used to remove the temperature dependence of the log amp slope using a translinear multiplier.The rest of the paper is organized as follows: First, the logarithmic amplifier and its temperature characteristic are briefly discussed. The following sections present the V-I conversion and temperature compensating blocks. Finally, simulation results are shown before the paper concludes.

II. Logarithmic Amplifier

The log amp used as base for this work was adapted from [5]. Its schematic is shown in Fig. 1. To understand the circuit's function, MOS transistors $M_{1,2}$ with the resistors R_l at their sources can be interpreted as source followers linearly turning the input voltages V_{in} and V_{ref} into the currents I_l^+ and I_l^-. The cascode transistors $M_{3,4}$ together with the load $M_5 - M_8$ ensure a high impedance at the output nodes. Through current mirrors $M_{9,11}$ and $M_{10,12}$, $I_{t,l}$ and $I_{t,r}$ can be used to compensate process induced static offsets in the

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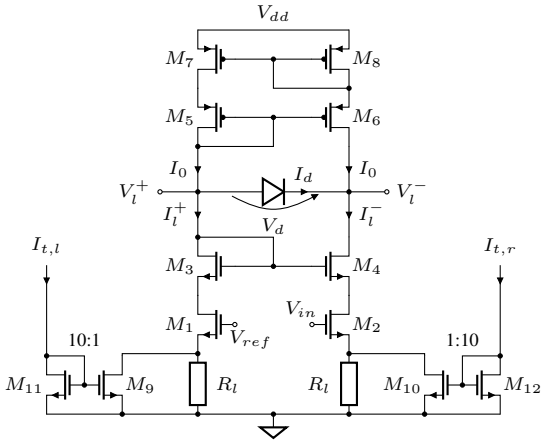


Figure 1: Schematic of the log amp used for evaluating the temperature compensation scheme

output voltages V_l^+ and V_l^-.

When V_{in} rises while V_{ref} stays constant, a difference current $I_d = (I_l^+ - I_l^-)/2$ flows through the diode. This results in a differential output voltage

$$V_l^+ - V_l^- = V_d \approx V_T \cdot \log \frac{I_d}{I_s}, \tag{1}$$

with the thermal voltage $V_T = kT/q$ ($\approx 26\,\mathrm{mV}$ at $300\,\mathrm{K}$), and the reverse saturation current I_s.

The temperature dependence of the output voltage V_d stems from $V_T\,(T)$ and $I_s\,(T)$. In the following, our main concern will be the compensation of the V_T term as it directly influences the slope characteristic of the log amp output. As explained above, other temperature related offsets will be removed digitally in the final system.

III. V-I Conversion

Fig. 2a shows the schematic of the V-I conversion block. The output voltages of the log amp are applied to the non-inverting terminals of the operational amplifiers, realized as two-stage Miller-compensated opamps with pMOS input pairs. The opamps force these voltages over the resistors R resulting in two currents $I^+ = V_l^+/R$ and $I^- = V_l^-/R$. The advantage of this I-V conversion approach over techniques relying on linear-region MOSFETs [4], despite the higher power and area consumption, lies in its good linearity as most BiCMOS processes for analog applications include at least one type of quality resistor. Furthermore, these resistors typically show linear temperature behavior which is removed in the temperature cancellation block.

Transistors $M_3 - M_6$ together with $M_{1,2}$ can be interpreted as a folded-cascode stage. In this circuit it is used as a current differential amplifier [6]. Currents I^+ and I^- are fed into the low-impedance nodes at the sources of $M_{3,4}$. Through the current-mirroring action of $M_{5,6}$, the nodal equation at the source of M_4 reads

$$I_b + I^+ = I_D + I^- \;\Rightarrow\; I_D = I_b + I^+ - I^-. \tag{2}$$

As can be seen from (2), the output current of the differential current amplifier I_D is the difference of I^+ and I^- offset by the biasing current I_b. This current I_b makes sure that there is always a current flowing in the branches of the amplifier therefore preventing any switch-on distortion. Since the current mirror can be designed to be very accurate, the linearity of the differential to single-ended conversion provided by this V-I converter is superior to similarly complex solutions based on voltage amplifiers.

The current mirrors $M_7 - M_{10}$ and $M_{11} - M_{14}$ converting I_D into the V-I converter's output current I_{VI} ensure that the voltage at the drain of M_4 is sufficiently high. As the input voltage V_l^- lies around half the supply voltage of $3.3\,\mathrm{V}$, this voltage has to be high enough to ensure that M_2 and M_4 can operate in saturation. If the current I_D is directly fed into the temperature compensation block in Fig. 2b, the voltage at the drain of M_4 is two base-emitter voltages high and therefore too low. By using the cascode current mirror, the voltage drop over M_7 and M_9 automatically assumes a value such that all transistors operate in saturation.

IV. Temperature Compensation Block

The schematic of the temperature compensation block is shown in Fig. 2b. Its operation principle is based on a translinear loop [7]. Using Kirchhoff's voltage law on the base-emitter voltages of $Q_1 - Q_4$ yields

$$V_{BE1} + V_{BE2} = V_{BE3} + V_{BE4} \tag{3}$$

$$V_T \log \frac{I_{VI}}{I_s} + V_T \log \frac{I_{b1}}{I_s} = V_T \log \frac{I_{PTAT}}{I_s} + V_T \log \frac{I_o}{I_s} \tag{4}$$

$$\frac{I_{VI}}{I_s} \cdot \frac{I_{b1}}{I_s} = \frac{I_{PTAT}}{I_s} \cdot \frac{I_o}{I_s}. \tag{5}$$

Assuming well-matched transistors, the temperature-dependent terms V_T and I_s cancel in (5). Solving for I_o, we find for the temperature-independent output current

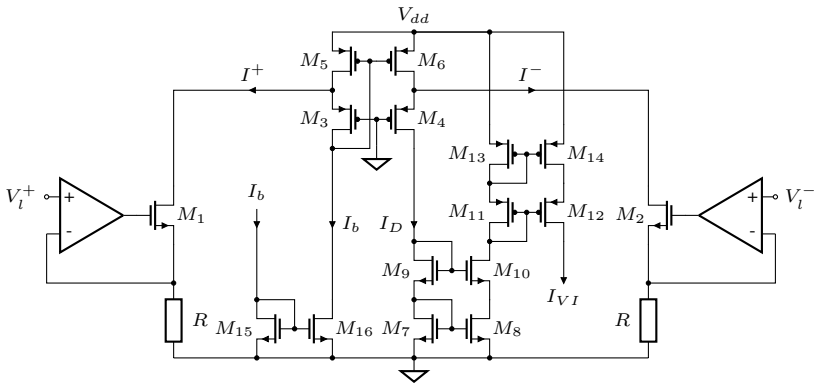
$$I_o = I_{b1} \frac{I_{VI}}{I_{PTAT}}. \tag{6}$$

With I_{b1} being a bias current constant over temperature, and I_{VI} being PTAT because of (1), the temperature-dependence of I_{VI} can be compensated by an additional PTAT current I_{PTAT} according to (6). As most modern systems already include PTAT current sources for biasing purposes, compensating the log amp's linear temperature characteristic with the proposed circuit becomes an exercise of finding the optimal PTAT slope.

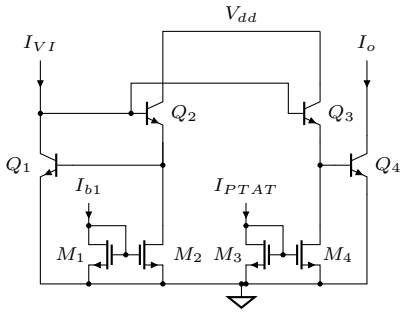
V. Simulation Results

The proposed temperature compensation scheme has been implemented in NXP's internal $180\,\mathrm{nm}$ SiGe BiCMOS technology [8]. The circuit area (without the logarithmic amplifier) is estimated to be approximately $0.09\,\mu\mathrm{m}^2$ of which the largest part is occupied by the two operational amplifiers. The resistors are realized in polysilicon, and have values of $R_l = 100\,\mathrm{k}\Omega$ and $R = 80\,\mathrm{k}\Omega$, respectively.

To verify the circuit's operation in the targeted temperature range for automotive applications between $-40\,^\circ\mathrm{C}$ and $125\,^\circ\mathrm{C}$,



(a) V-I converter



(b) Temperature compensation block

Figure 2: V-I converter with differential current amplifier and the translinear loop-based temperature compensation block

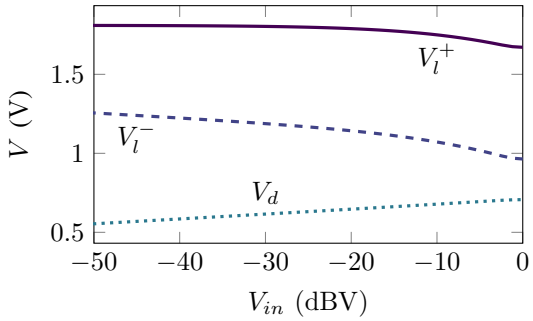


Figure 3: Output voltages of the log amp at room temperature

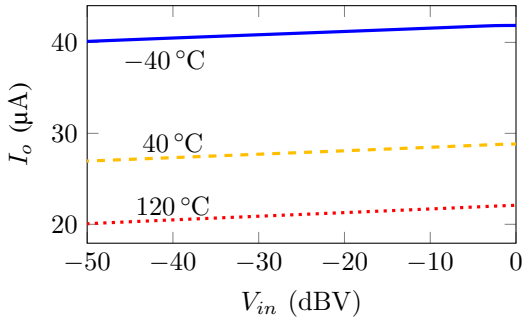


Figure 5: Temperature-compensated output current

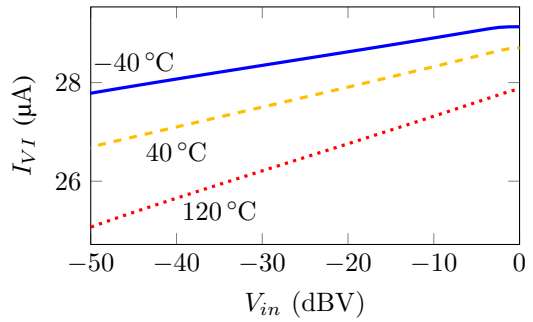


Figure 4: Single-ended output current of the V-I converter for three different temperatures

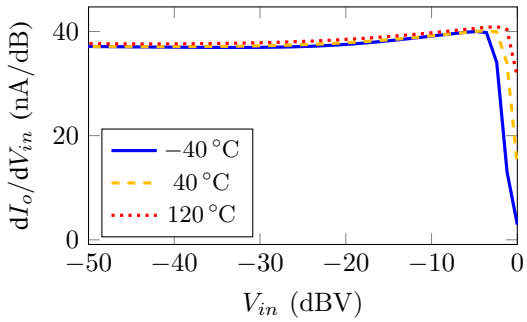


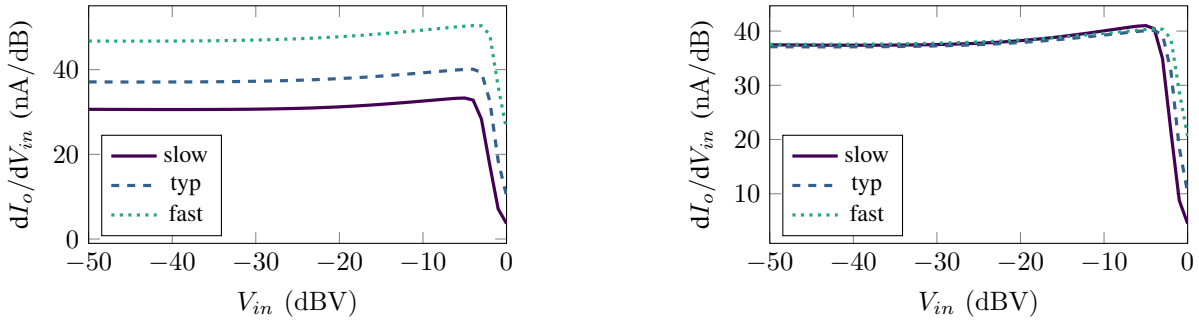
Figure 6: Slopes of the I_o-V_{in} curves from Fig. 5

extensive simulations have been performed. The temperature compensation circuitry draws about 0.9 mA from a 3.3 V supply under nominal conditions.

The simulated output voltages of the log amp at room temperature are shown in Fig. 3. Already at an input voltage of approximately −20 dBV, the single-ended output voltages begin to deviate significantly from their ideal characteristic: V_l^+ stops being constant, and V_l^- changes its slope. However, these nonidealities cancel in the differential output voltage V_d. To preserve the dynamic range of the logarithmic amplifier, the temperature compensation scheme should not introduce any distortion for high input voltages. Because of this, the highly linear topology with an operational amplifier was chosen as input stage for the V-I converter in Fig. 2a.

Fig. 4 depicts the curves of the V-I converter's output current at −40 °C, 40 °C, and 120 °C. The linearity of the differential log amp output voltage V_d is reproduced in I_{VI} even for higher input voltages. As predicted by (2), the slope of the shown curves is strongly temperature dependent.

Using a PTAT slope of 5000 ppm/K the output current of the temperature compensation block shown in Fig. 5 is generated. Note that even if no PTAT current source with such a high temperature coefficient is available on-chip, clever current mirroring and combining of PTAT currents as in [9] can yield a current with a suitable temperature characteristic. Comparing



(a) un-trimmed

(b) trimmed

Figure 7: Process corner simulation of the I_{out}-V_{in} slope

Table I: Comparison of temperature-compensated log amps

	[4]	[3]	[11]	[12]	This
Tech. (µm)	0.35 BiCMOS	0.13 CMOS	0.5 CMOS	0.13 CMOS	0.18 BiCMOS
sim/exp	sim	exp	exp	sim	sim
Temp. (°C)	25-100	0-90	27-57	0-100	−40-125
Dyn. rng. (dB)	40	45	120	8	50
Supply (V)	3.3	1.2	3.3	1.2	3.3
Power	1.5 mW	-	10 µW	-	3 mW
Area (mm^2)	0.0125	0.1	0.04	-	0.13

the input of the temperature compensation block in Fig. 4 with its output from Fig. 5, it is apparent that the proposed approach increases the spread of the output current at a fixed input voltage, but removes the temperature dependence of the I_o-V_{in} slope.

In Fig. 6 the derivative of I_o with respect to V_{in} is shown for the same three temperatures as before. It is easy to see that the compensation circuit has successfully removed any temperature variation of this slope.

An issue with the architecture of the V-I converter is that its performance depends on the value of the resistor R in Fig. 2a, and is therefore sensitive to process variations. Fig. 7a shows the variation of the I_o-V_{in} slope for slow, typical, and fast process corners at 27 °C. It varies by approximately 45 %. To remove this variation, digital trimming for the resistors R similar to [10] has been implemented. In the application of on-chip power measurement, digital calibration has to be performed for an accurate correlation of the DC output voltage with the high-frequency input power. During this calibration step, the resistor values can be adjusted to minimize both inter-die and intra-die variations. In Fig. 7b the corner simulation has been repeated with five bit trimming for both resistors. It is obvious that this procedure is able to remove the differences generated by process variations.

VI. Conclusion

For a fair comparison, the logarithmic amplifier from Fig. 1 is added to the temperature compensation circuit and both circuits together are compared to other log amp designs in Tab. I. Note that logarithmic amplifiers based on compression by a multi-stage limiting amplifier chain have not been included because these architectures tend to have applications at higher frequencies.

As a figure of merit for the temperature performance, authors usually give the temperature coefficient of the output signal at a fixed input voltage. A low TC then means that the curves in Fig. 4 move closer together at that input voltage. When the log amp is used together with a power detector, which is the target application for this work, a digital calibration has to performed to remove any DC offset, and the temperature-induced distance between the output curves in Fig. 5 is removed as a by-product. Therefore, this work does not aim to achieve a low TC in the traditional sense, and the measure is left out of the comparison table.

The presented circuit has the highest temperature range of all compared designs. Furthermore, the dynamic range is very good and more than sufficient for the target application. Area and power consumption are on the high side, but not by a large margin.

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