DCCDL LAB5

Verilog

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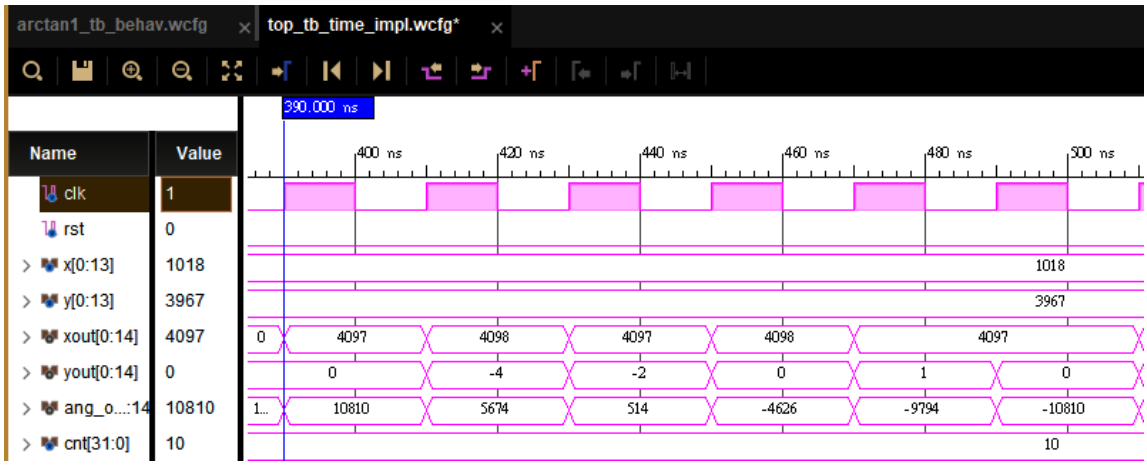
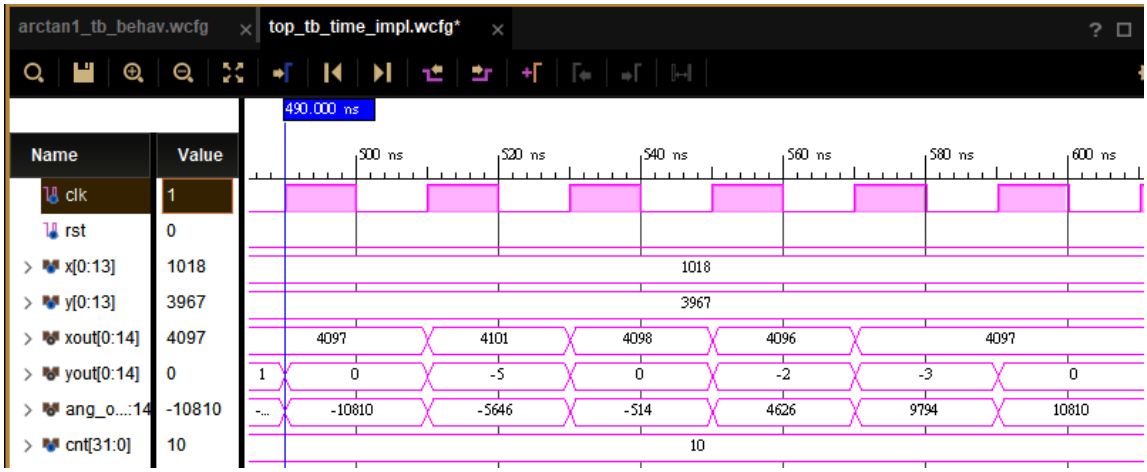
8. Print the timing diagram of the behavior simulation result and post-route simulation result of your arctangent function. Show the error between the Verilog output and Matlab output by figures.

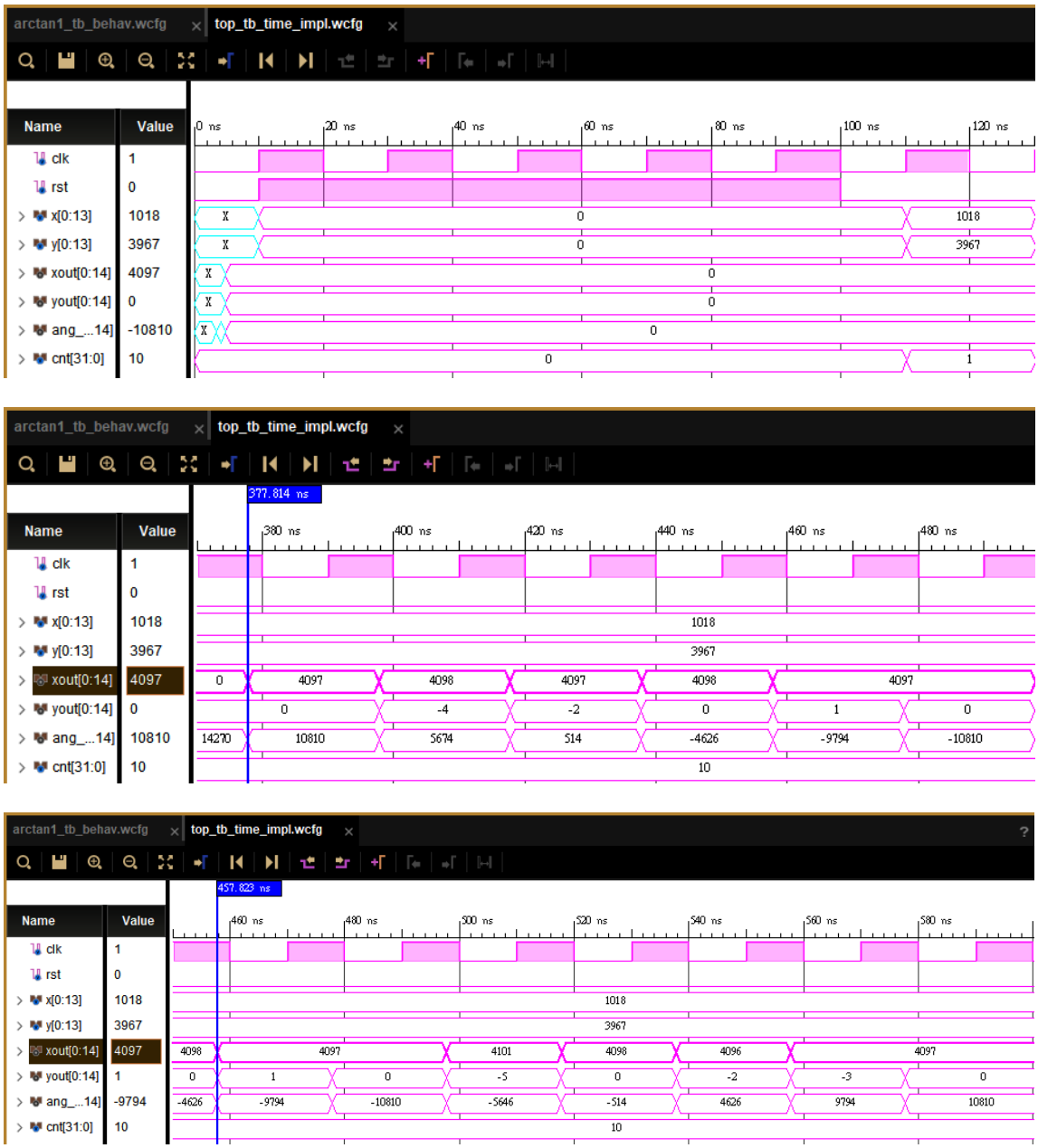
Xout: [4097, 4098, 4097, 4098, 4097, 4097, 4101, 4098, 4096, 4097, 4097]
Yout: [0, -4, -2, 0, 1, 0, -5, 0, -2, -3, 0]
Ang_out: [10810, 5674, 514, -4626, -9794, -10810, -5646, -514, 4626, 9794, 10810]

behavior simulation result timing diagram:

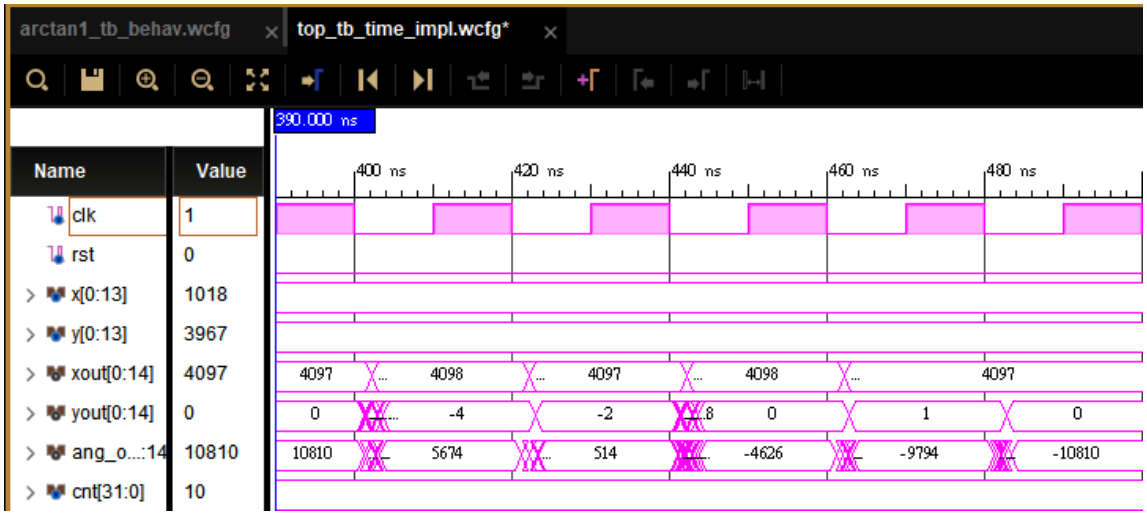


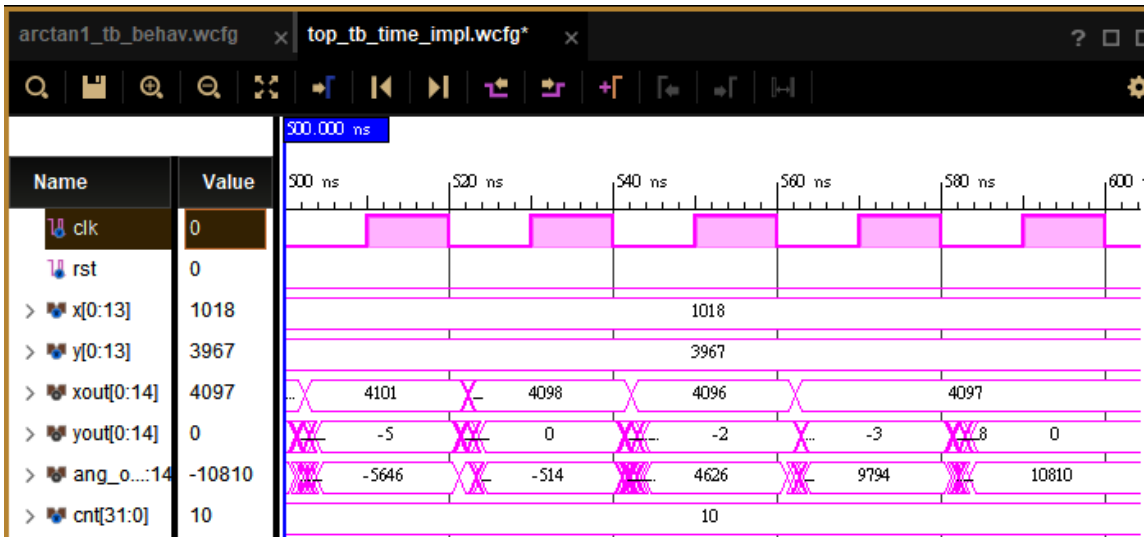


synthesis simulation result timing diagram:

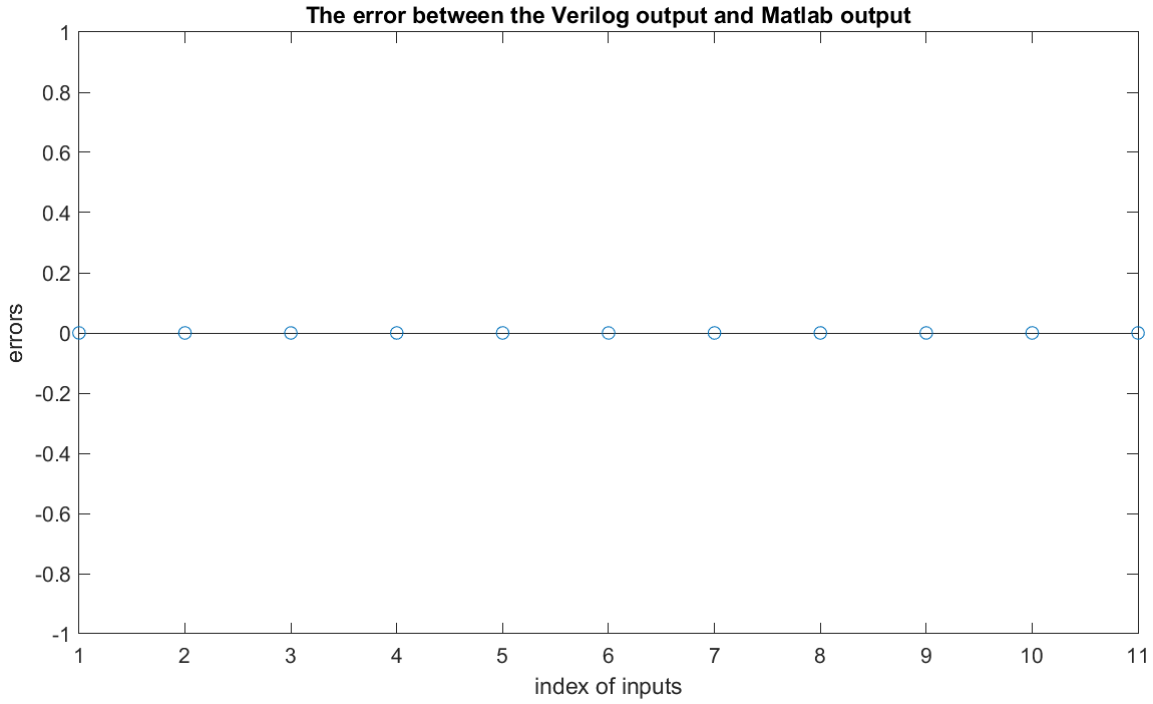


implementation simulation result timing diagram:

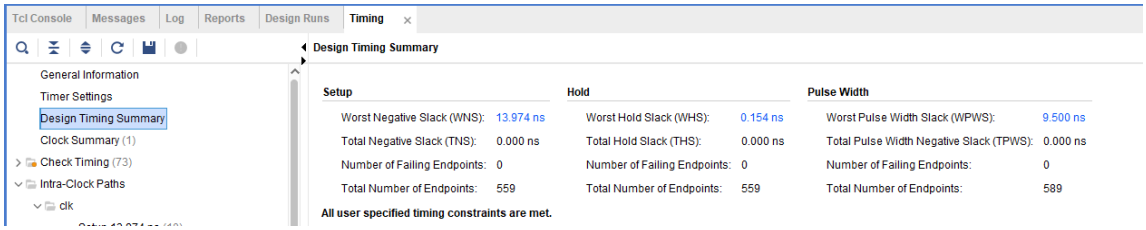




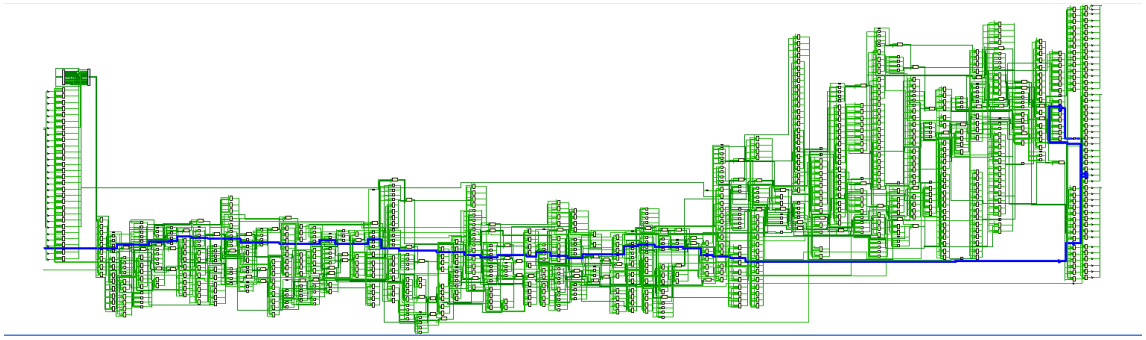
The error between the Verilog implementation simulation and Matlab output:

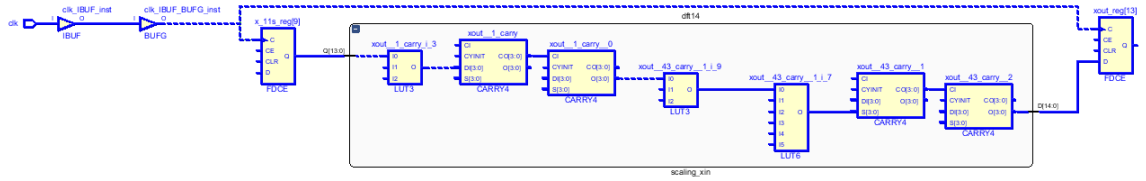


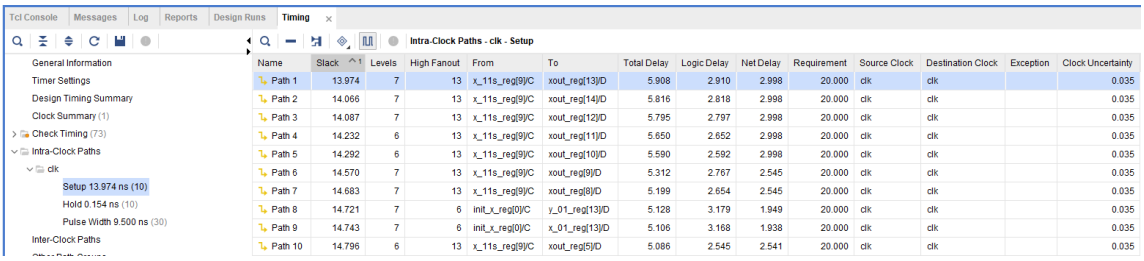
9. List the timing report of the arctangent function and show the critical path in your block diagram.



Setup:

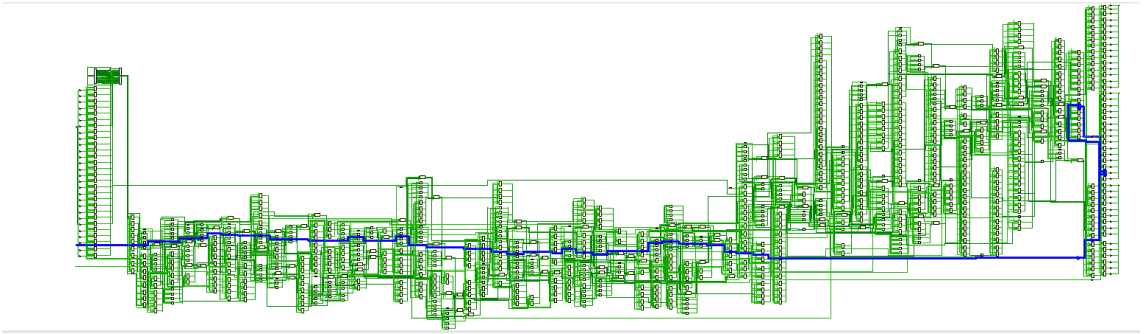


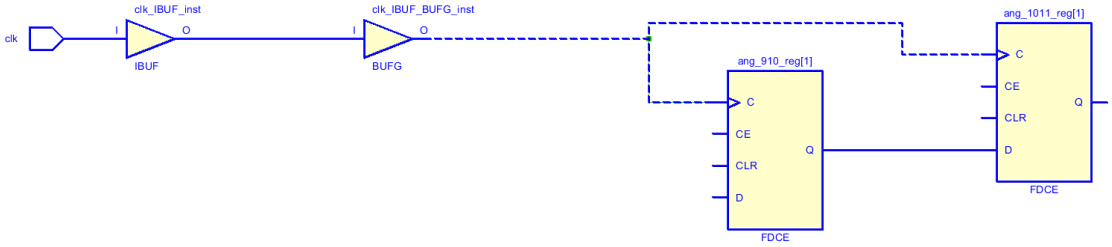




Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 1	13.974	7	13	x_11s_reg[9]/C	xout_reg[13]/D	5.908	2.910	2.998	20.000	clk	clk		0.035
Path 2	14.066	7	13	x_11s_reg[9]/C	xout_reg[14]/D	5.816	2.818	2.998	20.000	clk	clk		0.035
Path 3	14.087	7	13	x_11s_reg[9]/C	xout_reg[12]/D	5.795	2.797	2.998	20.000	clk	clk		0.035
Path 4	14.232	6	13	x_11s_reg[9]/C	xout_reg[11]/D	5.650	2.652	2.998	20.000	clk	clk		0.035
Path 5	14.292	6	13	x_11s_reg[9]/C	xout_reg[10]/D	5.590	2.592	2.998	20.000	clk	clk		0.035
Path 6	14.570	7	13	x_11s_reg[9]/C	xout_reg[9]/D	5.312	2.767	2.545	20.000	clk	clk		0.035
Path 7	14.683	7	13	x_11s_reg[9]/C	xout_reg[8]/D	5.199	2.654	2.545	20.000	clk	clk		0.035
Path 8	14.721	7	6	init_x_reg[0]/C	y_01_reg[13]/D	5.128	3.179	1.949	20.000	clk	clk		0.035
Path 9	14.743	7	6	init_x_reg[0]/C	x_01_reg[13]/D	5.106	3.168	1.938	20.000	clk	clk		0.035
Path 10	14.796	6	13	x_11s_reg[9]/C	xout_reg[5]/D	5.086	2.545	2.541	20.000	clk	clk		0.035

Hold time:





Tcl Console | Messages | Log | Reports | Design Runs | Timing

Intra-Clock Paths - clk - Hold

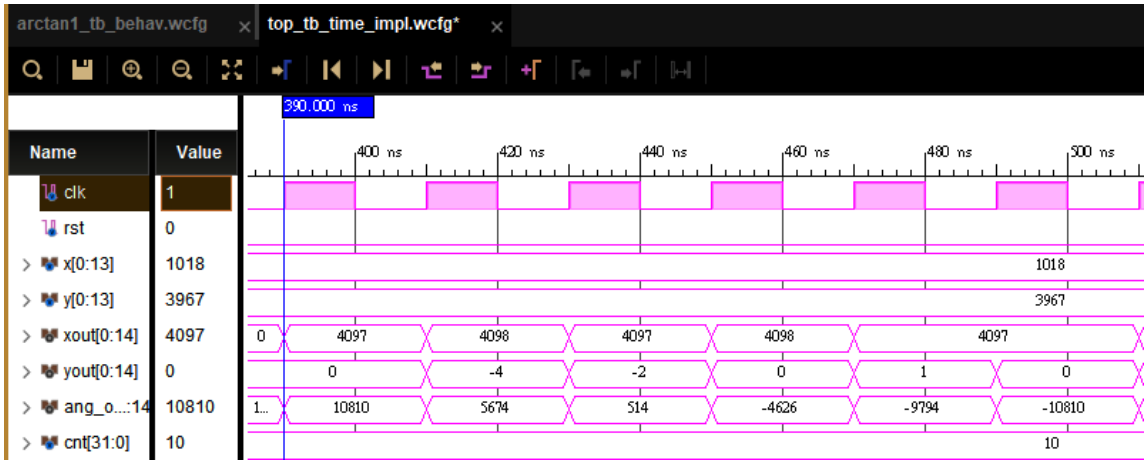
- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (73)
- Intra-Clock Paths
  - clk
    - Setup 13.974 ns (10)
    - Hold 0.154 ns (10)
    - Pulse Width 9.500 ns (30)
  - Inter-Clock Paths

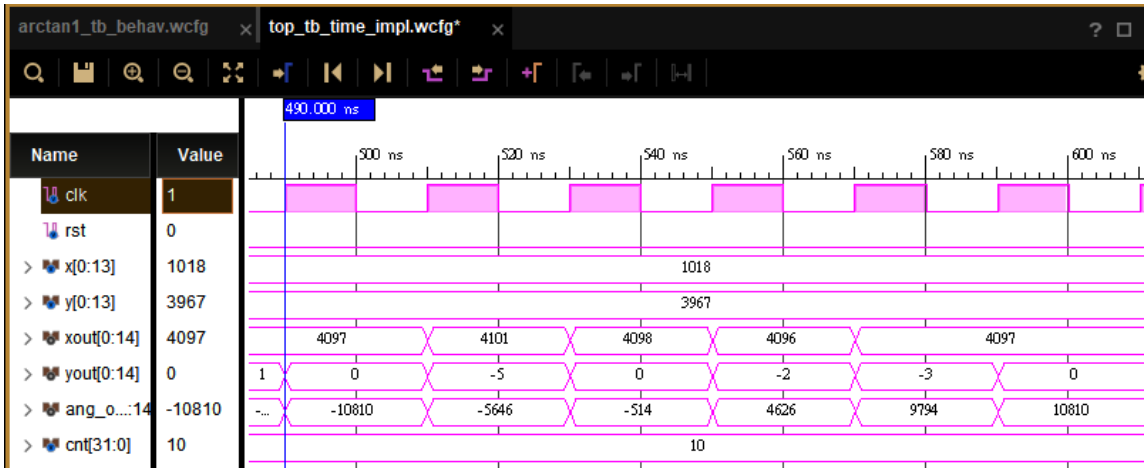
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 11	0.154	0	1	ang_910_reg[1]/C	ang_1011_reg[1]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 12	0.154	0	1	ang_01_reg[1]/C	ang_12_reg[1]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 13	0.154	0	1	ang_34_reg[1]/C	ang_45_reg[1]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 14	0.154	0	1	ang_34_reg[2]/C	ang_45_reg[2]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 15	0.154	0	1	ang_34_reg[3]/C	ang_45_reg[3]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 16	0.154	0	1	ang_34_reg[4]/C	ang_45_reg[4]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 17	0.154	0	1	ang_34_reg[5]/C	ang_45_reg[5]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 18	0.154	0	1	ang_34_reg[6]/C	ang_45_reg[6]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 19	0.154	0	1	ang_34_reg[7]/C	ang_45_reg[7]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 20	0.154	0	1	ang_45_reg[1]/C	ang_56_reg[1]/D	0.282	0.141	0.141	0.000	clk	clk		0.000

10. Print the timing diagram of the behavior simulation result and post-route simulation result of your magnitude function. Show the error between the Verilog output and Matlab output by figures.

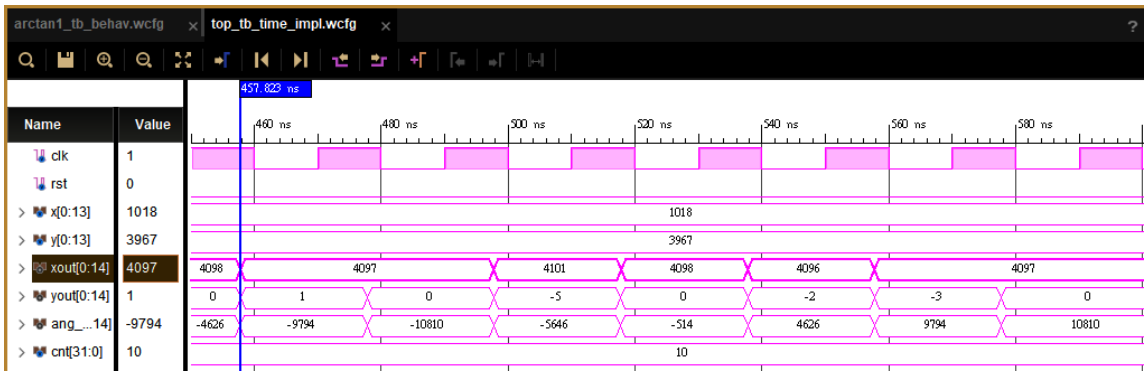
Xout: [4097, 4098, 4097, 4098, 4097, 4097, 4101, 4098, 4096, 4097, 4097]
Yout: [0, -4, -2, 0, 1, 0, -5, 0, -2, -3, 0]
Ang_out: [10810, 5674, 514, -4626, -9794, -10810, -5646, -514, 4626, 9794, 10810]

behavior simulation result timing diagram:

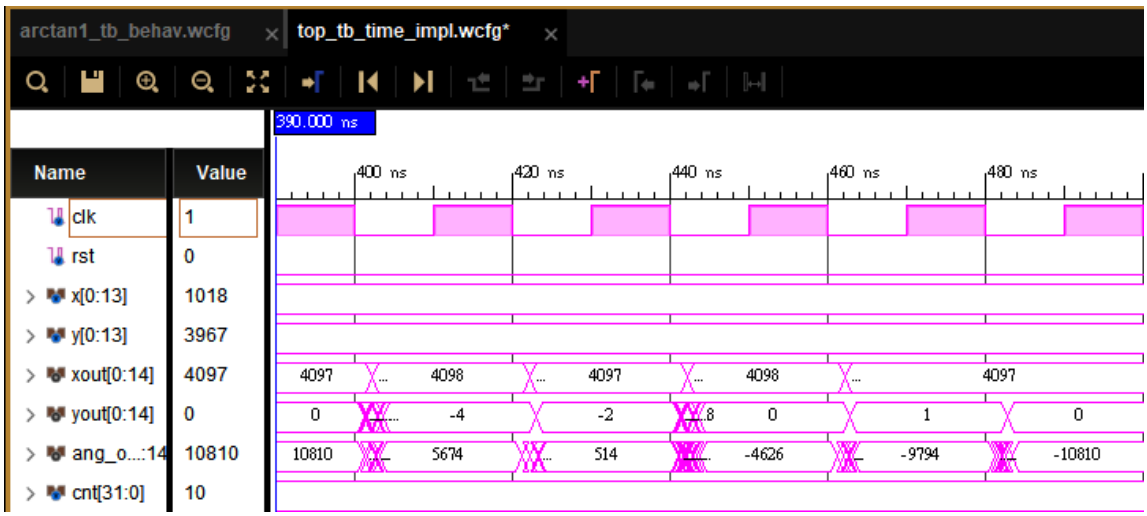


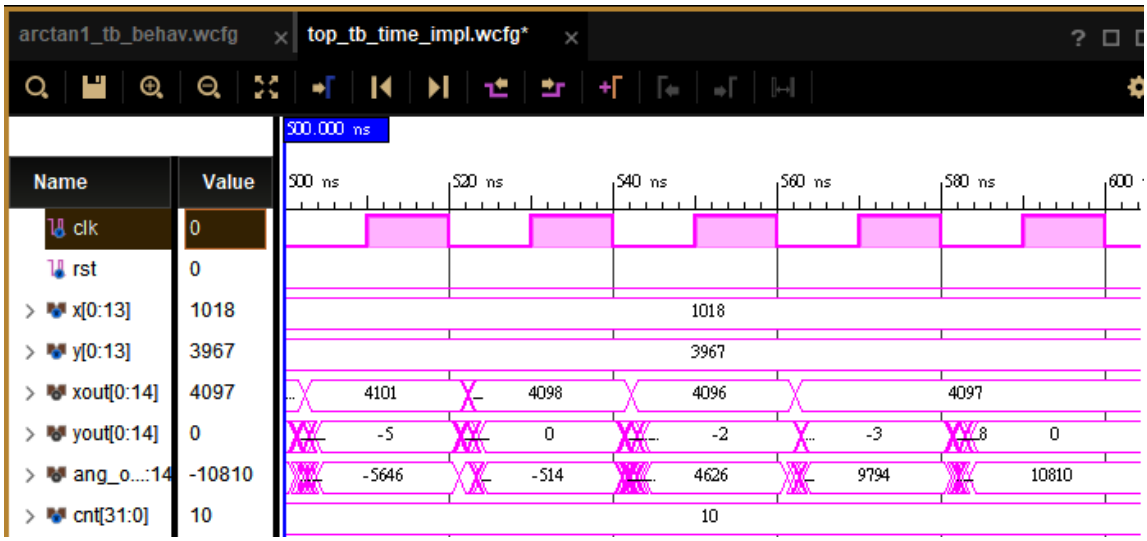


synthesis simulation result timing diagram:

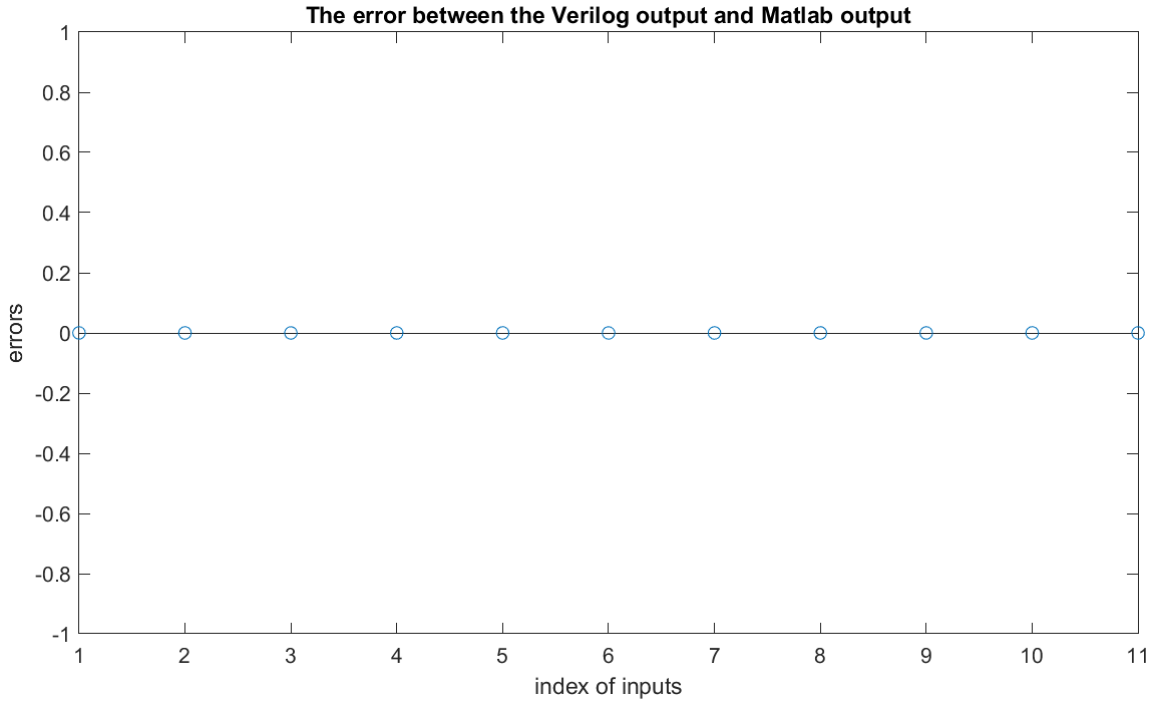


implementation simulation result timing diagram:



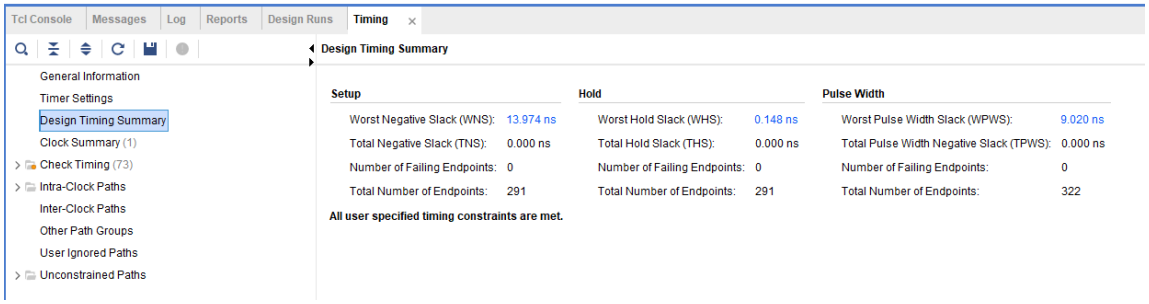


The error between the Verilog implementation simulation and Matlab output:

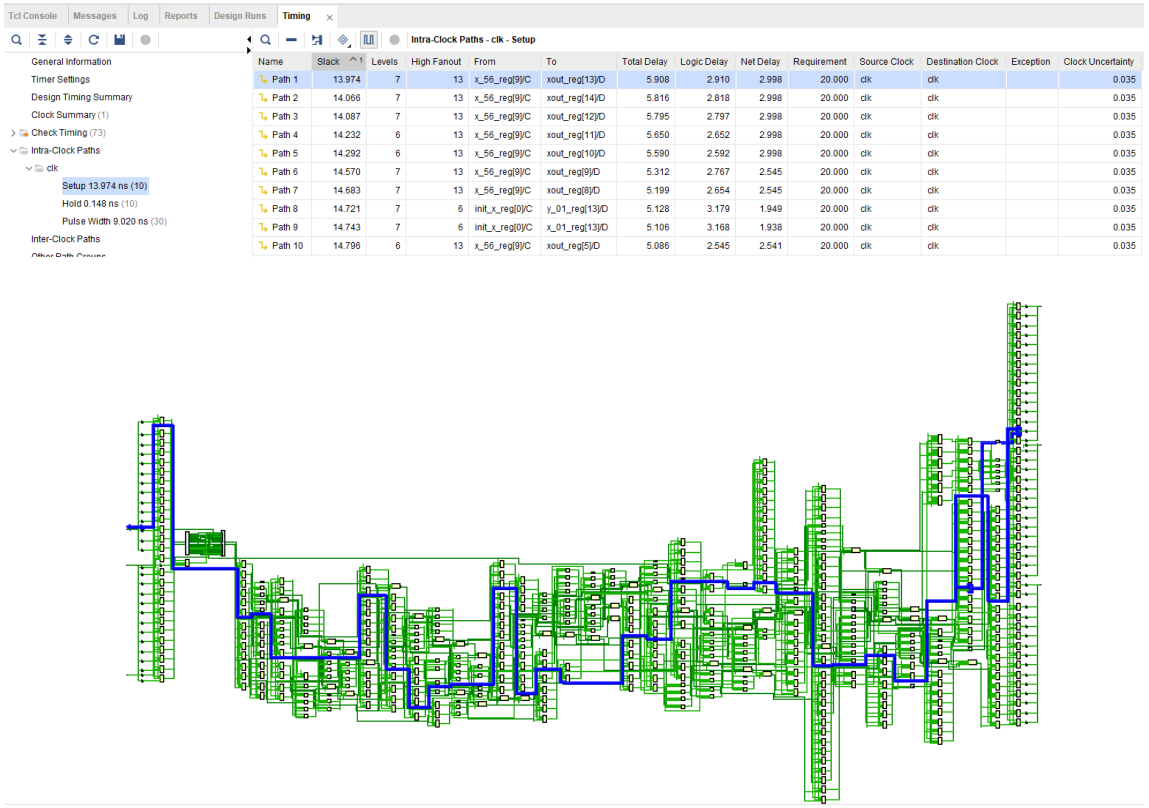


11. List the timing report of the magnitude function and show the critical path in your block diagram.

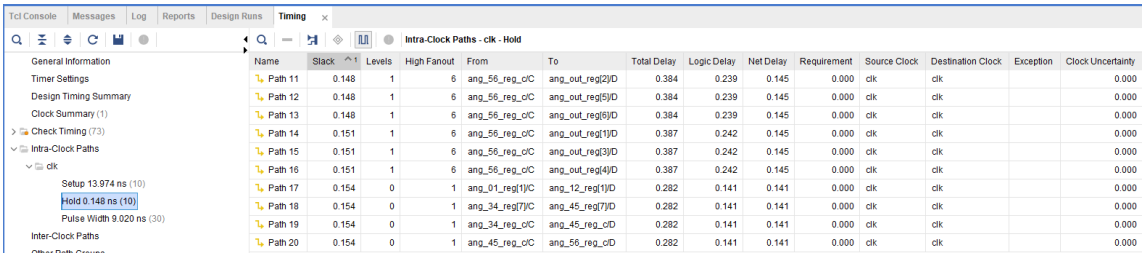
Timing diagram:



Setup timing report



Hold timing report:

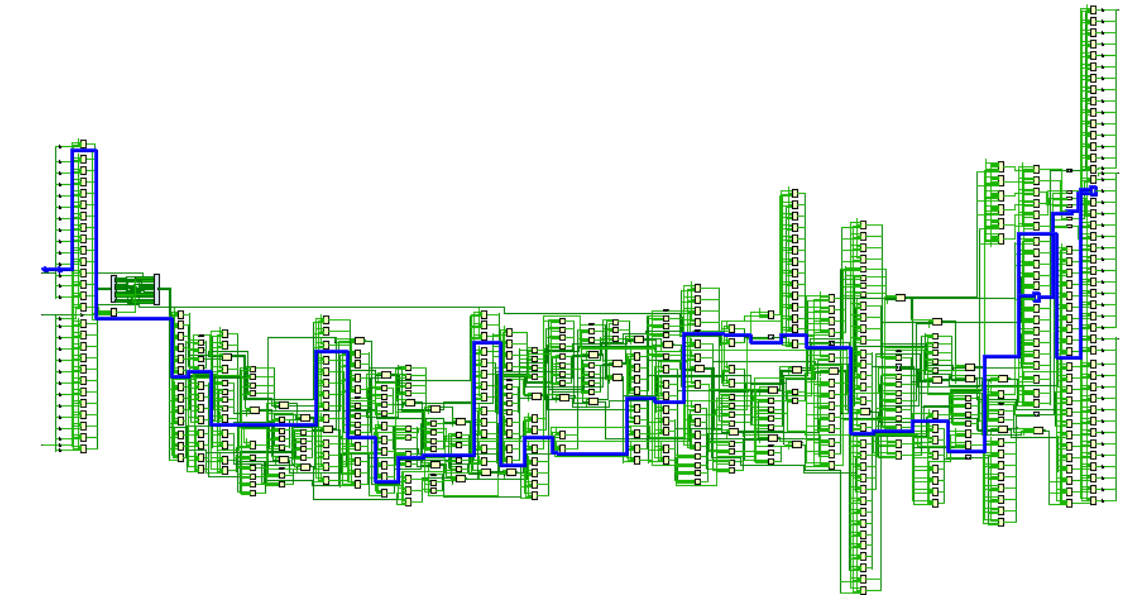


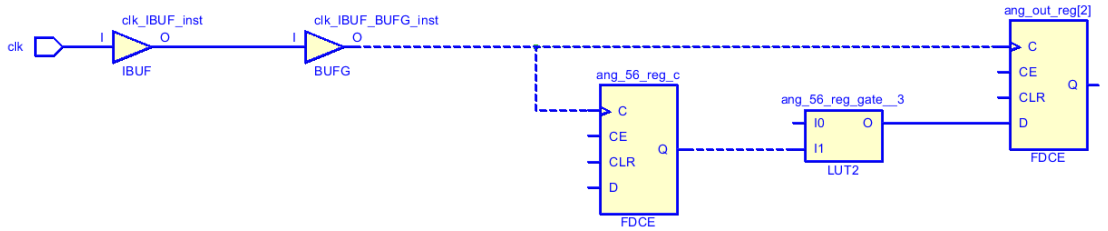
Tcl Console | Messages | Log | Reports | Design Runs | Timing

Intra-Clock Paths - clk - Hold

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (73)
- Intra-Clock Paths
  - clk
    - Setup 13.974 ns (10)
    - Hold 0.148 ns (10)
    - Pulse Width 9.020 ns (30)
- Inter-Clock Paths

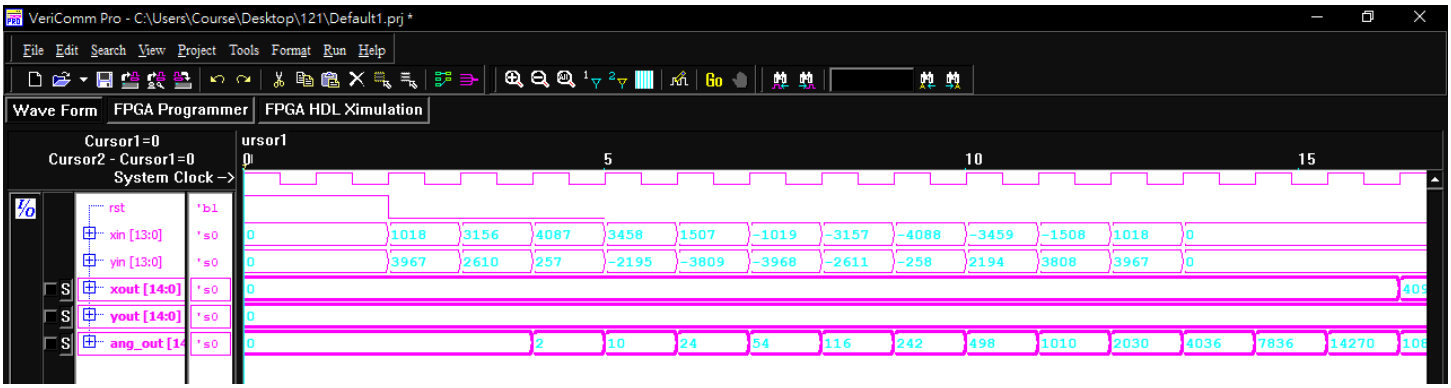
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 11	0.148	1	6	ang_56_reg_c/C	ang_out_reg[2]/D	0.384	0.239	0.145	0.000	clk	clk		0.000
Path 12	0.148	1	6	ang_56_reg_c/C	ang_out_reg[5]/D	0.384	0.239	0.145	0.000	clk	clk		0.000
Path 13	0.148	1	6	ang_56_reg_c/C	ang_out_reg[6]/D	0.384	0.239	0.145	0.000	clk	clk		0.000
Path 14	0.151	1	6	ang_56_reg_c/C	ang_out_reg[1]/D	0.387	0.242	0.145	0.000	clk	clk		0.000
Path 15	0.151	1	6	ang_56_reg_c/C	ang_out_reg[3]/D	0.387	0.242	0.145	0.000	clk	clk		0.000
Path 16	0.151	1	6	ang_56_reg_c/C	ang_out_reg[4]/D	0.387	0.242	0.145	0.000	clk	clk		0.000
Path 17	0.154	0	1	ang_01_reg[1]/C	ang_12_reg[1]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 18	0.154	0	1	ang_34_reg[7]/C	ang_45_reg[7]/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 19	0.154	0	1	ang_34_reg_c/C	ang_45_reg_c/D	0.282	0.141	0.141	0.000	clk	clk		0.000
Path 20	0.154	0	1	ang_45_reg_c/C	ang_56_reg_c/D	0.282	0.141	0.141	0.000	clk	clk		0.000



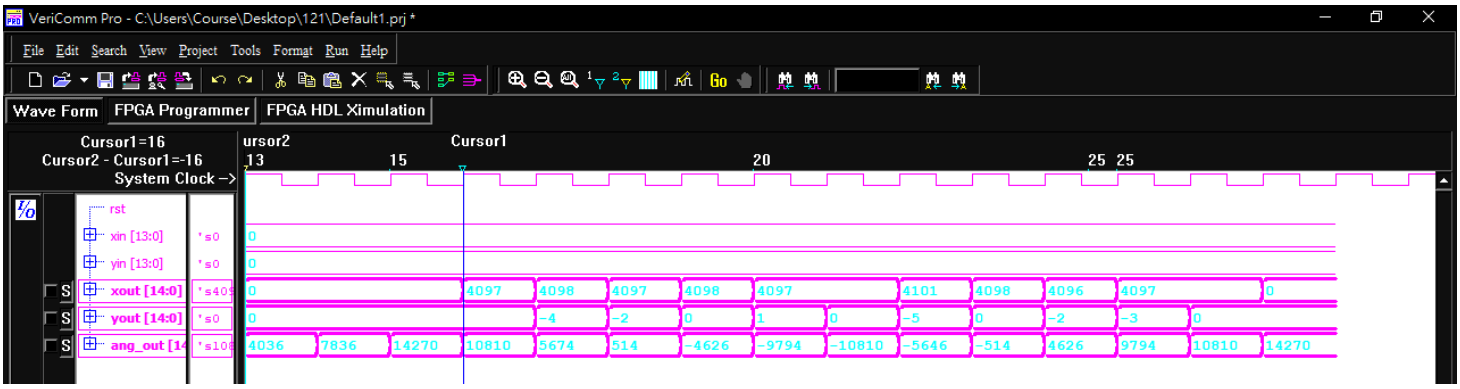


12. Show your measurement results of Q8 and Q10 (40%). Please paste your measurement results and show the error between measurement results and post-route simulation results by Matlab figure.

Input:



Output:



Xout:

[4097 4098 4097 4098 4097 4097 4101 4098 4096 4097 4097]

Yout:

[0 -4 -2 0 1 0 -5 0 -2 -3 0]

Ang_out:

[10810 5674 514 -4626 -9794 -10810 -5646 -514 4626 9794 10810]

The error between the measurement results and the post-route simulation results: