DCCDL LAB6

Part II

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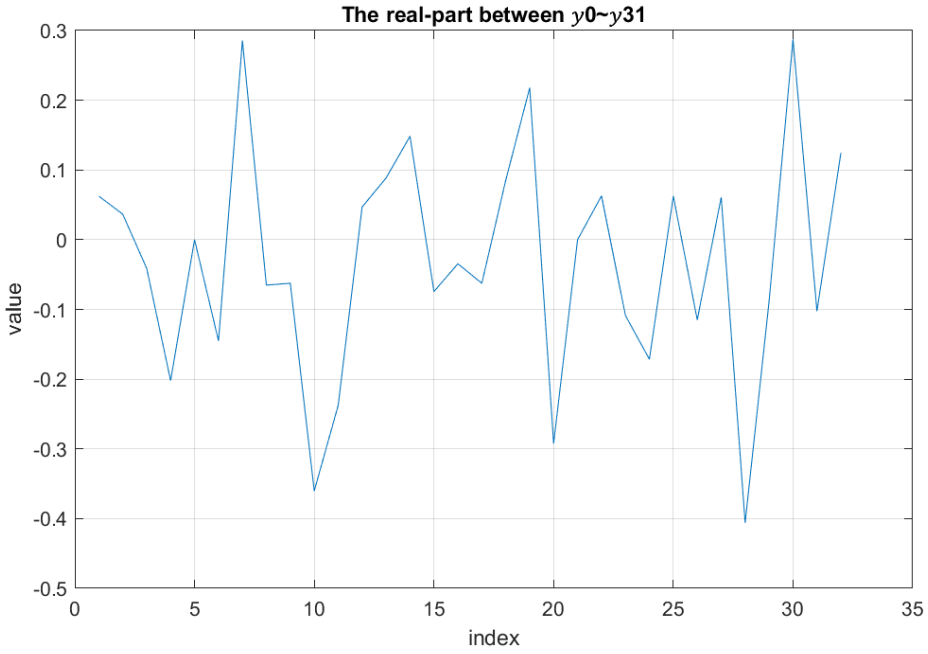
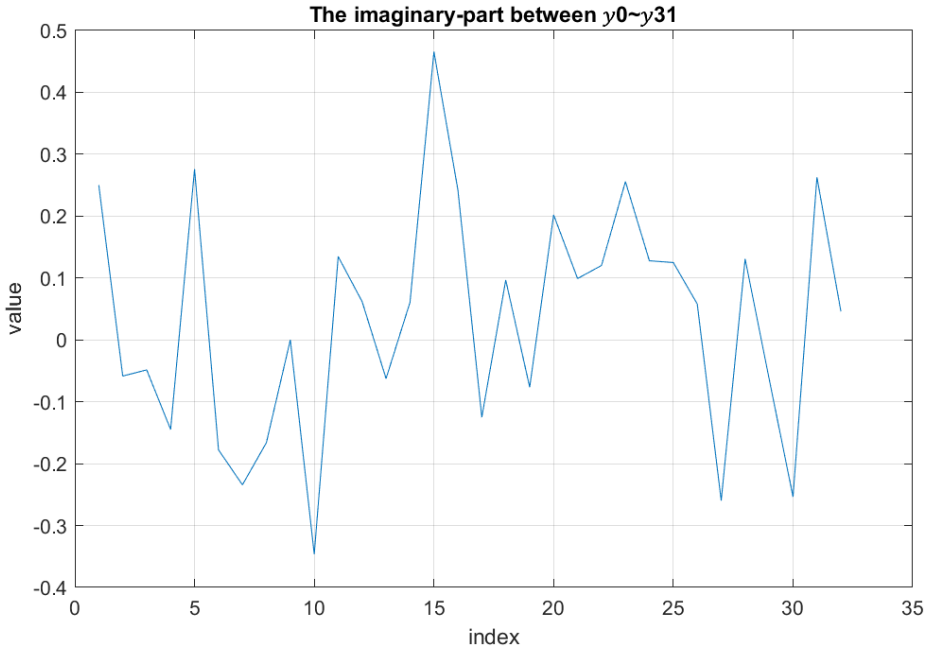
6. Use Matlab program to implement 32-point MDC IFFT architecture and the bit-reversal module. Draw the real-part and imaginary-part of $y_0 \sim y_{31}$ and $X_0 \sim X_{31}$. Compare them with the real-part and imaginary-part of $Y_0 \sim Y_{31}$. Depict the error.

(1) the real-part and imaginary-part of $y_0 \sim y_{31}$

real-part of $y_0 \sim y_{31}$

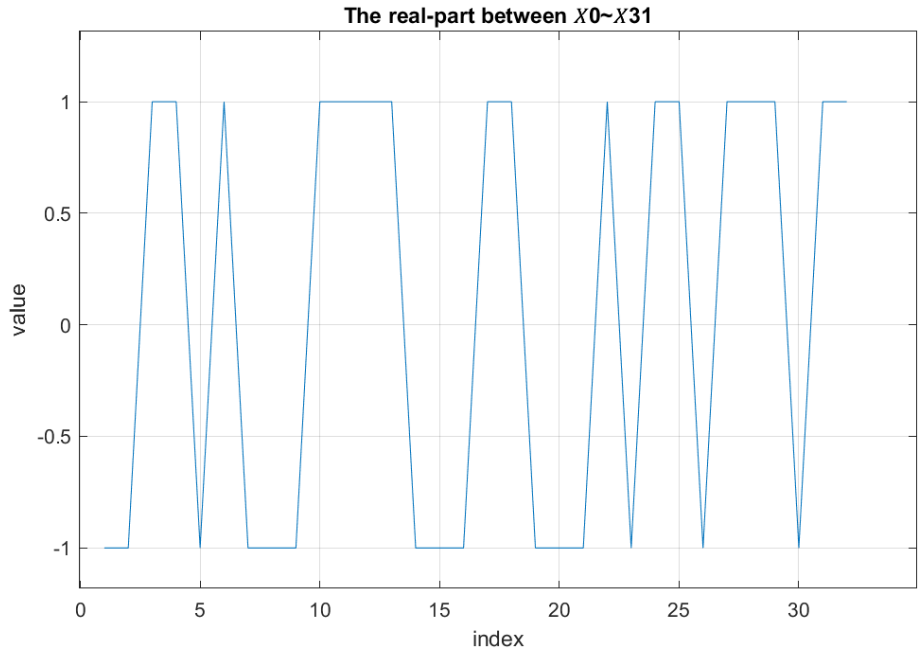


imaginary-part of $y_0 \sim y_{31}$

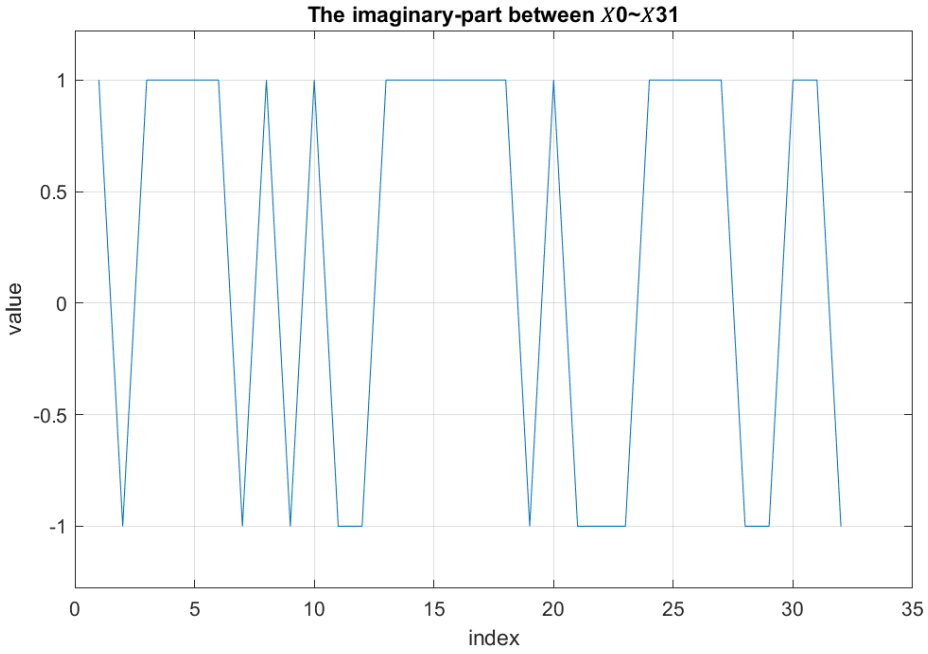


(2) the real-part and imaginary-part of $X_0 \sim X_{31}$

real-part of $X_0 \sim X_{31}$

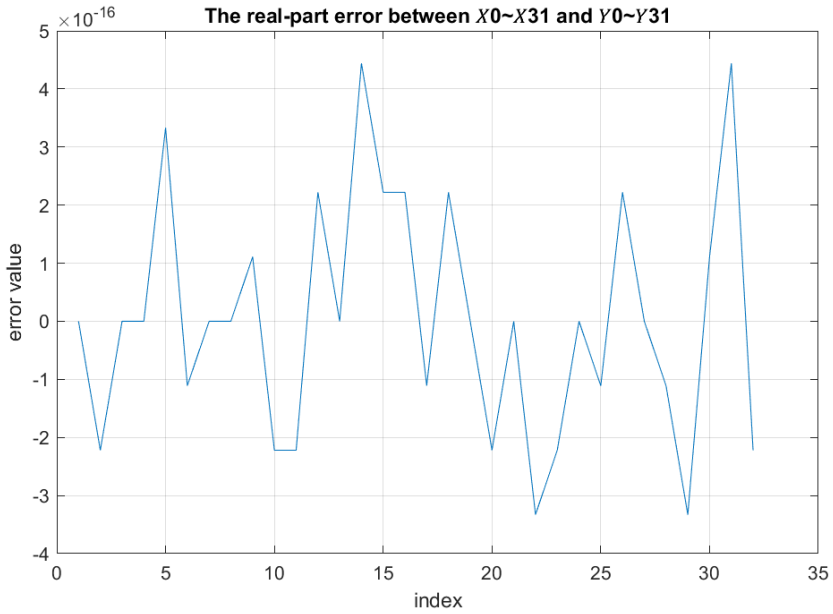


imaginary-part of $X_0 \sim X_{31}$

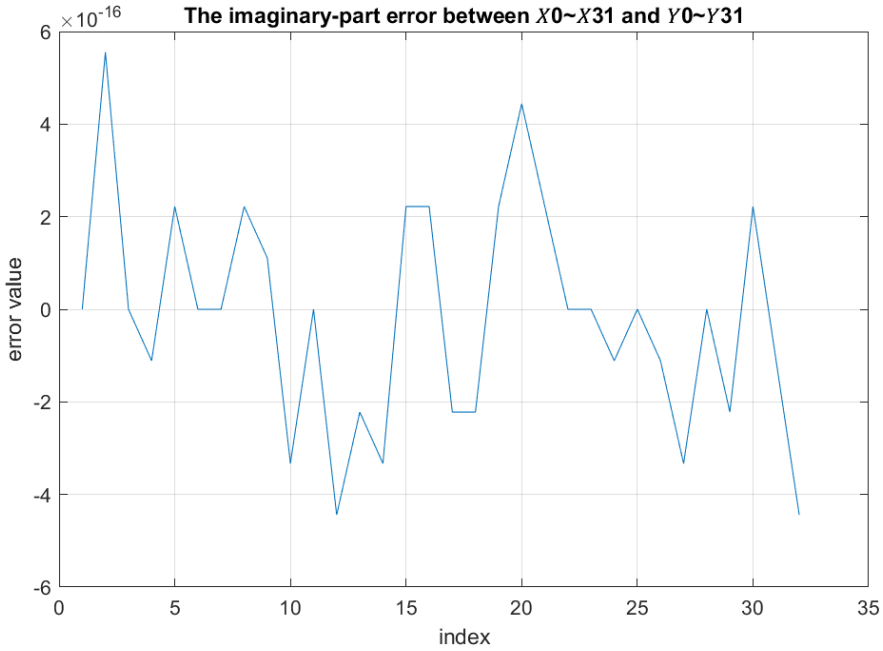


(3) the error between $X_0 \sim X_{31}$ and $Y_0 \sim Y_{31}$

The real-part error between $X_0 \sim X_{31}$ and $Y_0 \sim Y_{31}$



The imaginary-part error between $X_0 \sim X_{31}$ and $Y_0 \sim Y_{31}$



7. Show the timing diagram of your Verilog behavior and post-route simulation results of 32-point MDC IFFT.

Matlab input and output:

Real-part input:

```
[-512 -512 512 512 -512 512 -512 -512 -512 512 512 512 512 -512 -512 512
512 512 -512 -512 -512 512 -512 512 512 -512 512 512 512 -512 512 512]
```

Imaginary-part input:

```
[-512 512 -512 -512 -512 -512 512 -512 512 -512 512 512 -512 -512 -512 -
512 -512 -512 512 -512 512 512 512 -512 -512 -512 -512 512 512 -512 -512
512]
```

Real-part output:

```
[1024 602 -672 -3310 -1 -2375 4680 -1067 -1025 -5910 -3902 764 1451 2429
-1222 -565 -1024 1398 3570 -4786 1 1031 -1780 -2807 1025 -1890 1000 -6662
-1451 4713 -1682 2043]
```

Imaginary-part output:

```
[-4096 958 795 2363 -4521 2912 3838 2724 0 5682 -2204 -1010 1023 -994 -
7637 -3970 2048 -1584 1249 -3307 -1623 -1974 -4188 -2094 -2050 -952 4258
-2146 1027 4150  -4313 -762]
```

The timing diagram of behavior simulation results of 32-point MDC IFFT:

Rst: 重置

Clk: 時脈

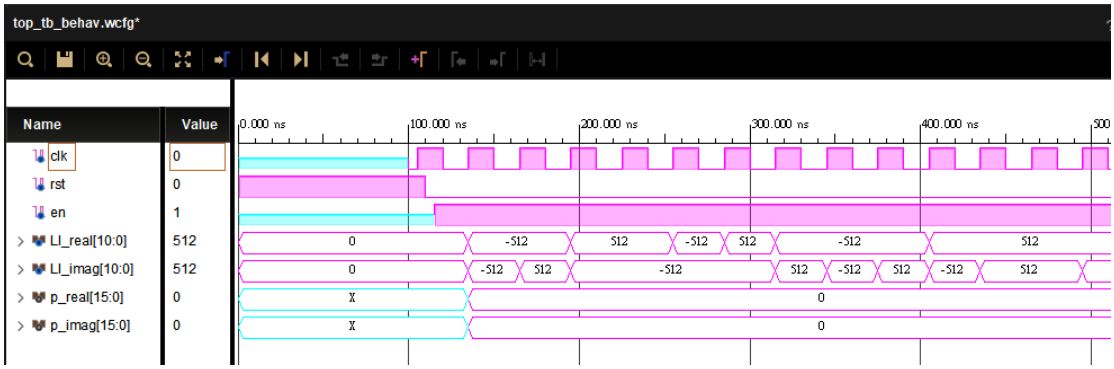
LI_real: MDC IFFT 輸入 real part

LI_imag: MDC IFFT 輸入 imaginary part

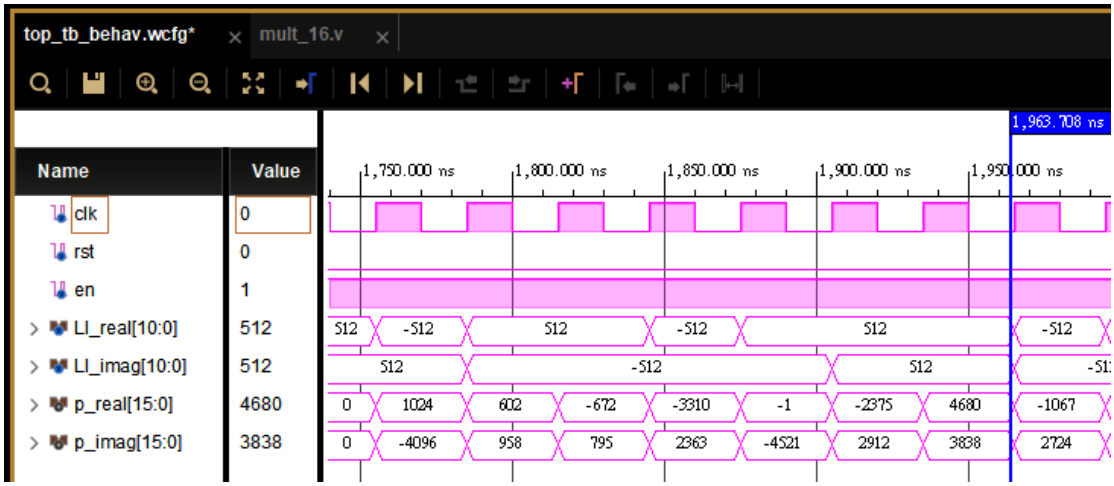
P_real: MDC IFFT 輸出 real part

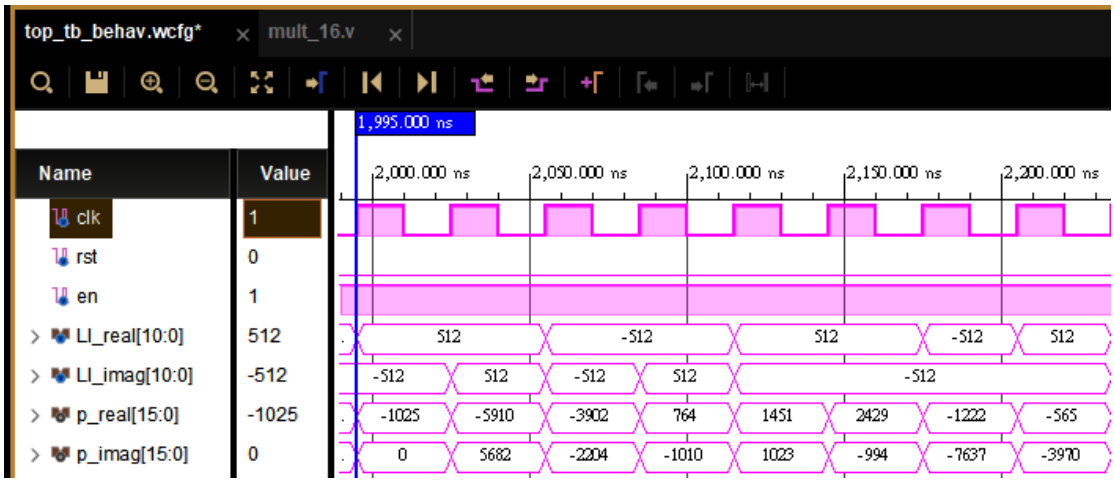
P_imag: MDC IFFT 輸出 imaginary part

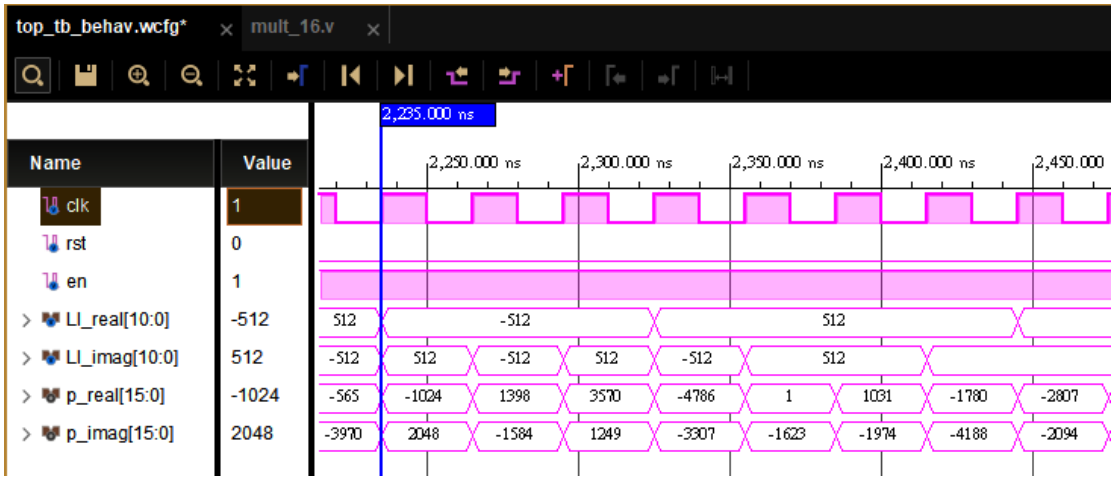
Input part:

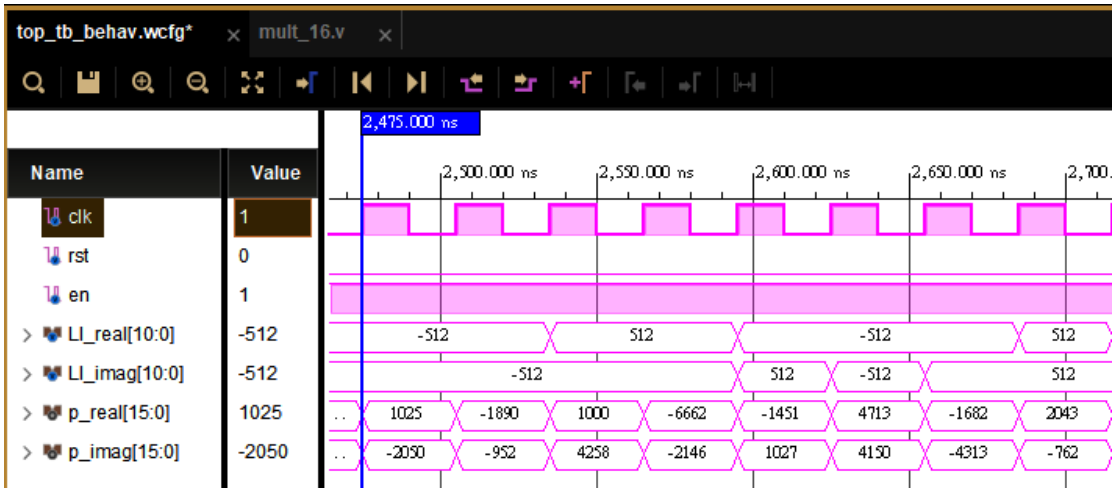


Output part:






top_tb_behav.wcfg*
mult_16.v
2,235.000 ns
Name
Value
clk
1
rst
0
en
1
LI_real[10:0]
-512
LI_imag[10:0]
512
p_real[15:0]
-1024
p_imag[15:0]
2048
2,250.000 ns
2,300.000 ns
2,350.000 ns
2,400.000 ns
2,450.000
512
-512
512
-512
512
-512
512
-512
512
-512
512
-565
-1024
1398
3570
-4786
1
1031
-1780
-2807
-3970
2048
-1584
1249
-3307
-1623
-1974
-4188
-2094


top_tb_behav.wcfg*
mult_16.v
2,475.000 ns
Name
Value
clk
1
rst
0
en
1
LI_real[10:0]
-512
LI_imag[10:0]
-512
p_real[15:0]
1025
p_imag[15:0]
-2050
2,500.000 ns
2,550.000 ns
2,600.000 ns
2,650.000 ns
2,700.
-512
512
-512
512
-512
512
-512
512
1025
-1890
1000
-6662
-1451
4713
-1682
2043
-2050
-952
4258
-2146
1027
4150
-4313
-762

The timing diagram of post-synthesis simulation results of 32-point MDC IFFT:

`Rst:` 重置

`Clk:` 時脈

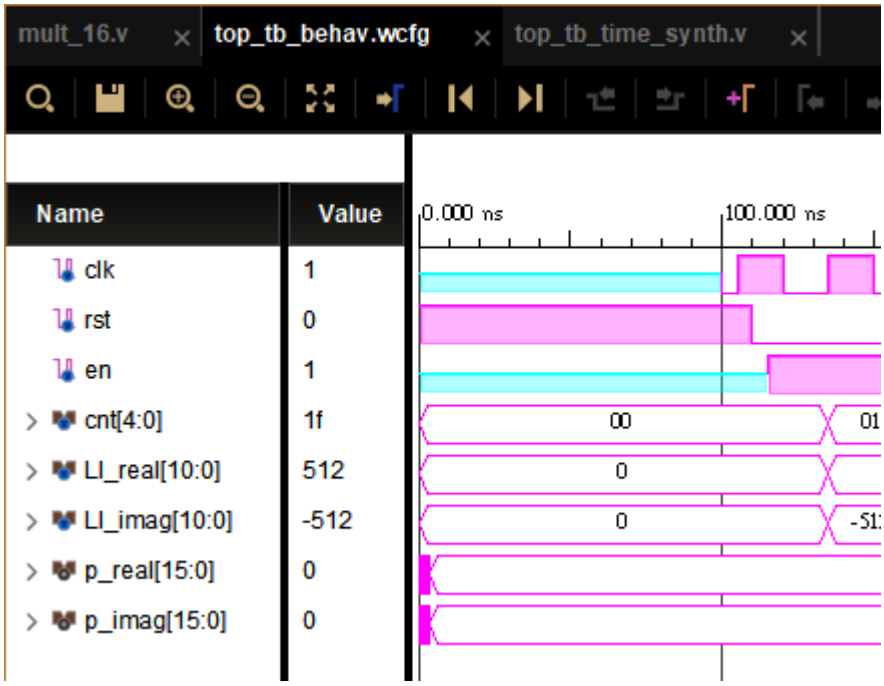
`LI_real: MDC IFFT` 輸入 `real part`

`LI_imag: MDC IFFT` 輸入 `imaginary part`

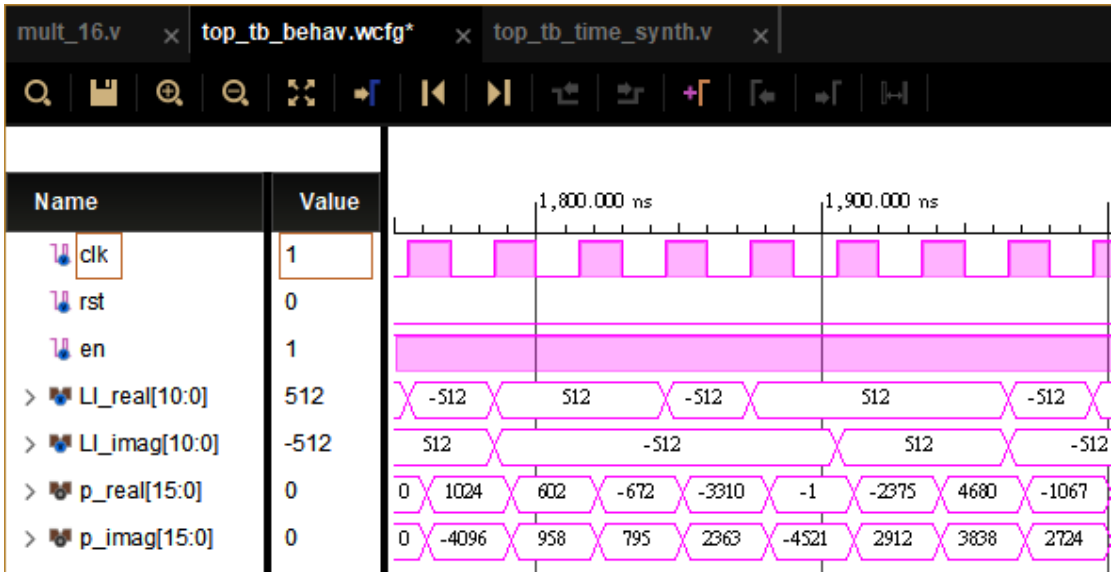
`P_real: MDC IFFT` 輸出 `real part`

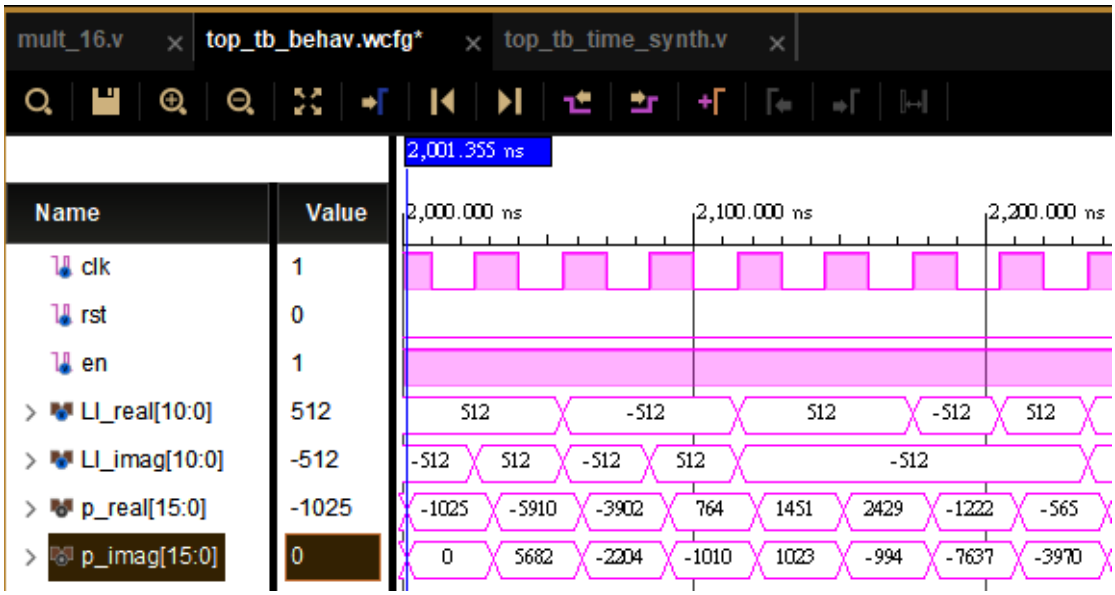
`P_imag: MDC IFFT` 輸出 `imaginary part`

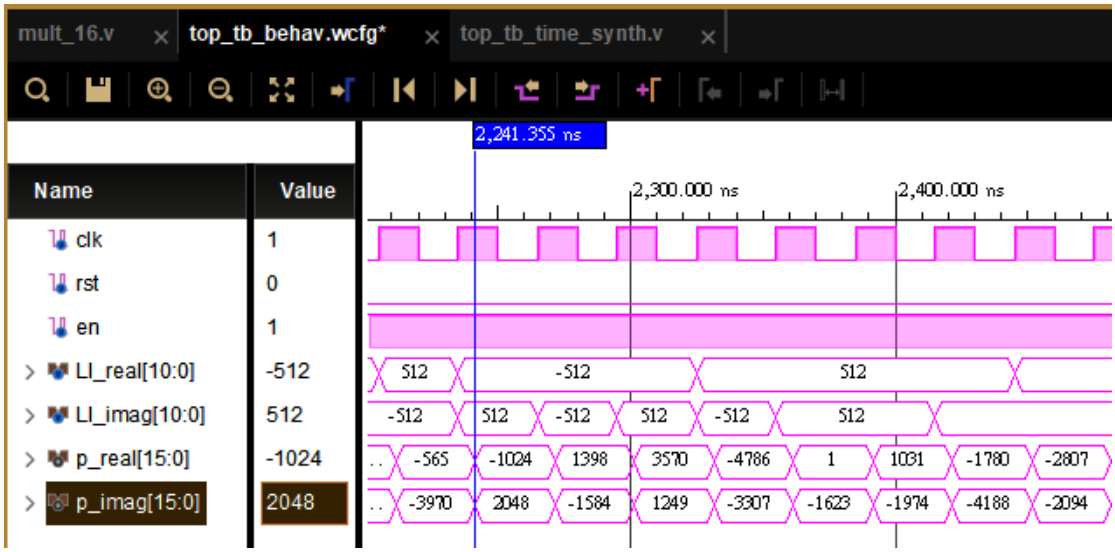
Global reset:

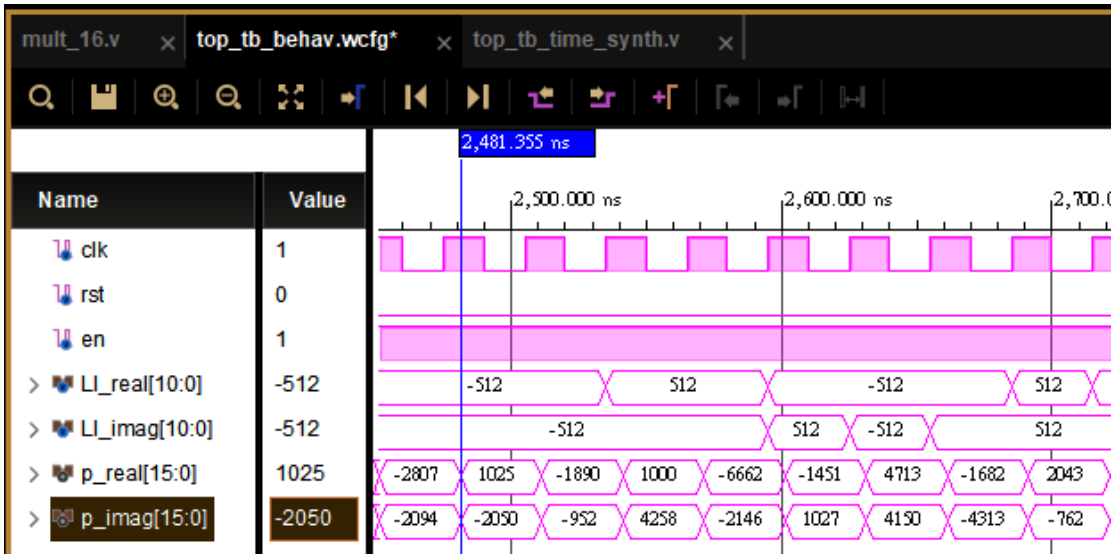


Output:




mult_16.v
top_tb_behav.wcfg*
top_tb_time_synth.v
2,001.355 ns
Name
Value
2,000.000 ns
2,100.000 ns
2,200.000 ns
clk 1
rst 0
en 1
LI_real[10:0] 512 512 -512 512 -512 512
LI_imag[10:0] -512 -512 512 -512 512 -512
p_real[15:0] -1025 -1025 -5910 -3902 764 1451 2429 -1222 -565
p_imag[15:0] 0 0 5682 -2204 -1010 1023 -994 -7637 -3970


mult_16.v
top_tb_behav.wcfg*
top_tb_time_synth.v
2,241.355 ns
Name
Value
2,300.000 ns
2,400.000 ns
clk 1
rst 0
en 1
LI_real[10:0] -512 512 -512 512
LI_imag[10:0] 512 -512 512 -512 512 -512
p_real[15:0] -1024 -565 -1024 1398 3570 -4786 1 1031 -1780 -2807
p_imag[15:0] 2048 -3970 2048 -1584 1249 -3307 -1623 -1974 -4188 -2094


mult_16.v
top_tb_behav.wcfg*
top_tb_time_synth.v
2,481.355 ns
Name
Value
2,500.000 ns
2,600.000 ns
clk 1
rst 0
en 1
LI_real[10:0] -512 -512 512 -512 512
LI_imag[10:0] -512 -512 512 -512 512
p_real[15:0] 1025 -2807 1025 -1890 1000 -6662 -1451 4713 -1682 2043
p_imag[15:0] -2050 -2094 -2050 -952 4258 -2146 1027 4150 -4313 -762

The timing diagram of post-implementation simulation results of 32-point MDC IFFT:

`Rst:` 重置

`Clk:` 時脈

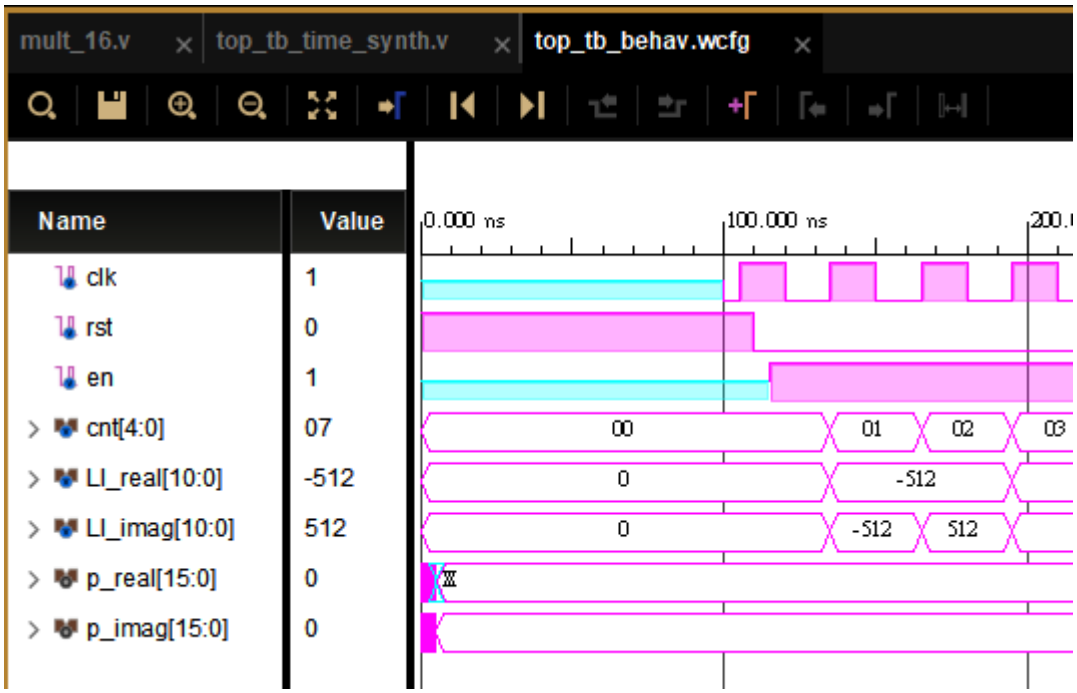
`LI_real: MDC IFFT` 輸入 `real part`

`LI_imag: MDC IFFT` 輸入 `imaginary part`

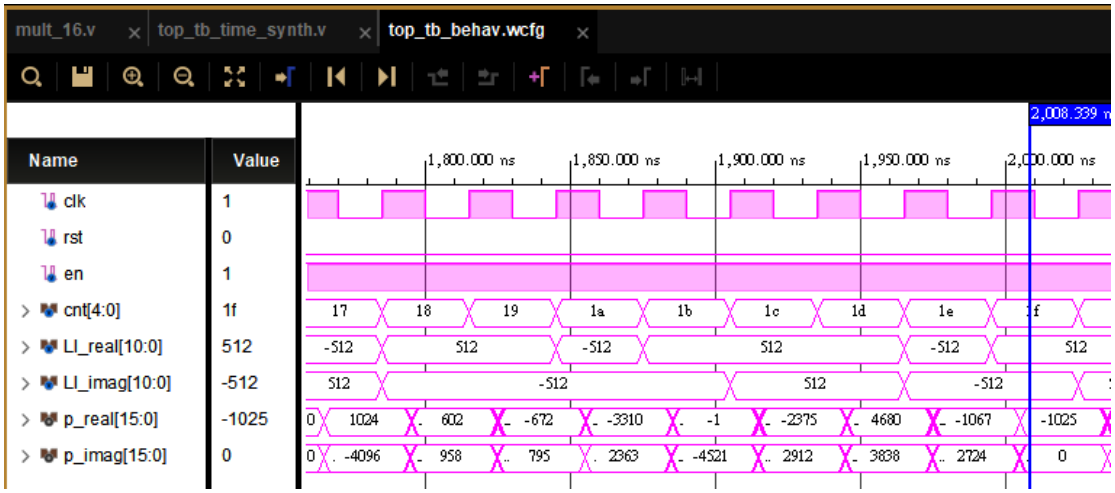
`P_real: MDC IFFT` 輸出 `real part`

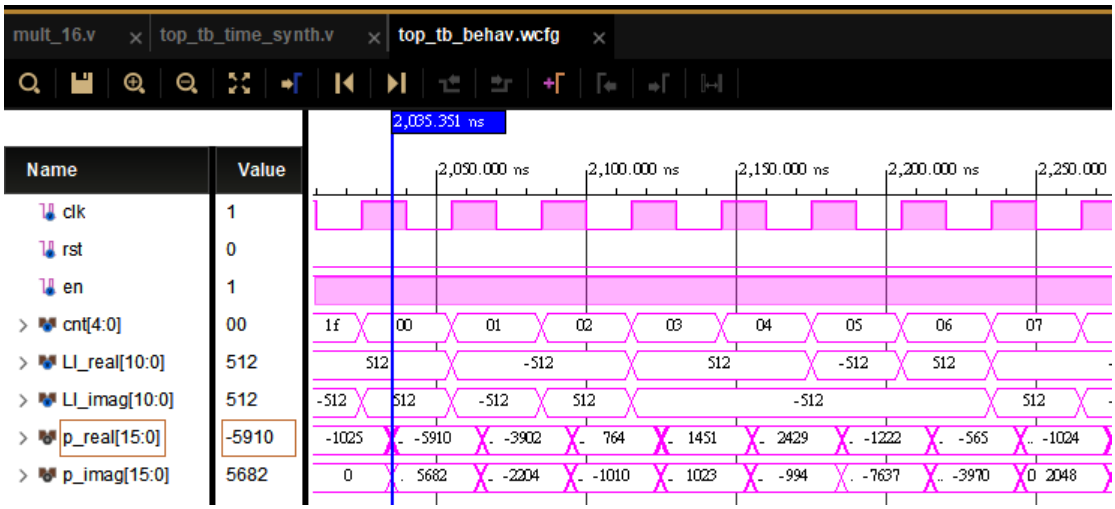
`P_imag: MDC IFFT` 輸出 `imaginary part`

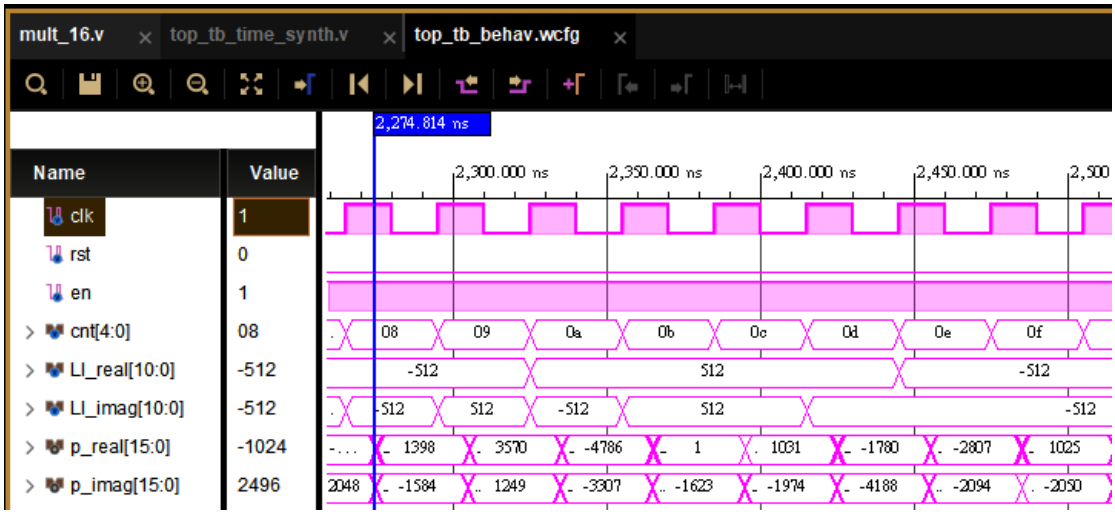
Global reset:

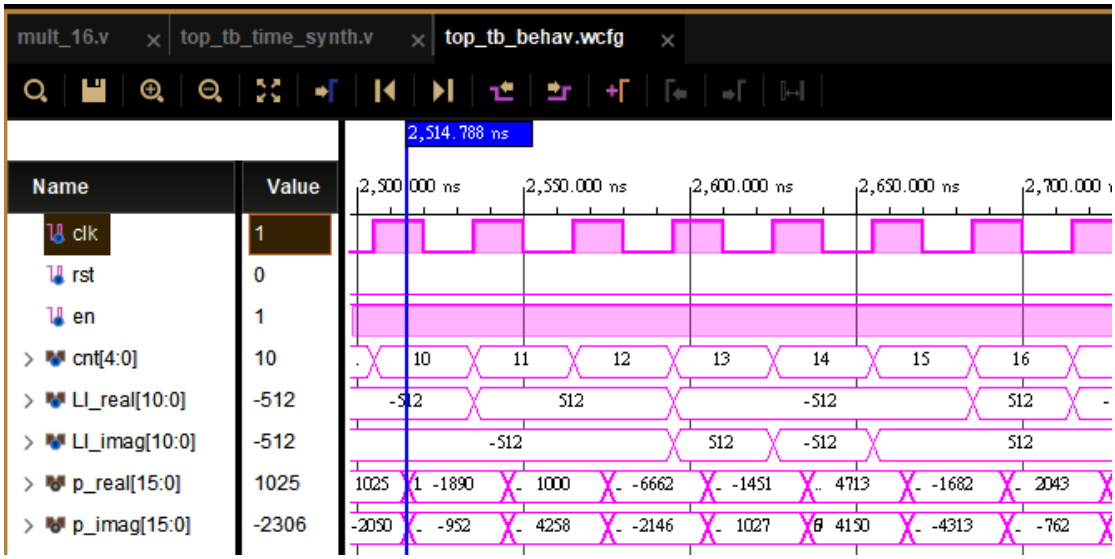


Output:



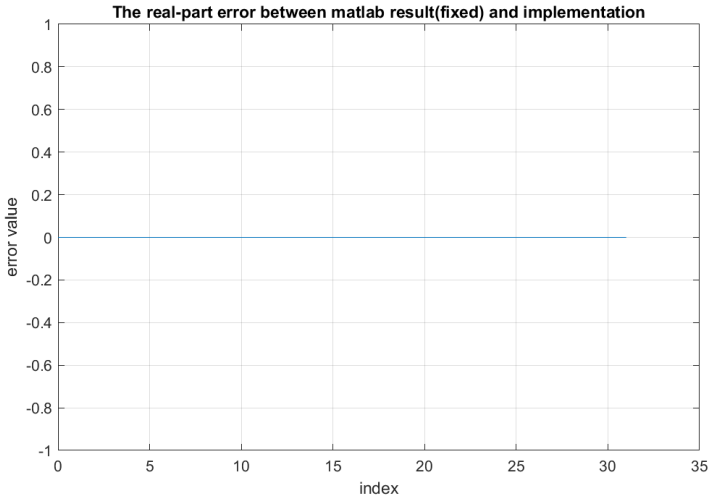

mult_16.v
top_tb_time_synth.v
top_tb_behav.wcfg
2,035.351 ns
Name
Value
clk 1
rst 0
en 1
cnt[4:0] 00
LI_real[10:0] 512
LI_imag[10:0] 512
p_real[15:0] -5910
p_imag[15:0] 5682
2,050.000 ns
2,100.000 ns
2,150.000 ns
2,200.000 ns
2,250.000


mult_16.v
top_tb_time_synth.v
top_tb_behav.wcfg
2,274.814 ns
Name
Value
clk 1
rst 0
en 1
cnt[4:0] 08
LI_real[10:0] -512
LI_imag[10:0] -512
p_real[15:0] -1024
p_imag[15:0] 2496
2,300.000 ns
2,350.000 ns
2,400.000 ns
2,450.000 ns

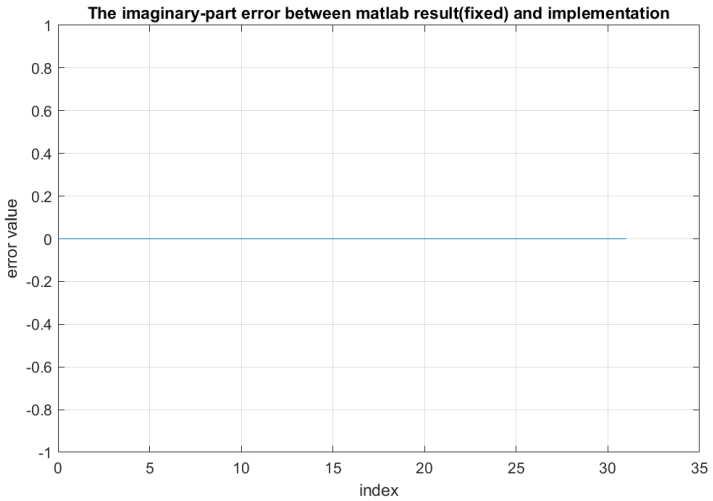

mult_16.v
top_tb_time_synth.v
top_tb_behav.wcfg
2,514.788 ns
Name
Value
clk 1
rst 0
en 1
cnt[4:0] 10
LI_real[10:0] -512
LI_imag[10:0] -512
p_real[15:0] 1025
p_imag[15:0] -2306
2,550.000 ns
2,600.000 ns
2,650.000 ns

Compare with the Matlab results to check your implementation error. Depict the error.

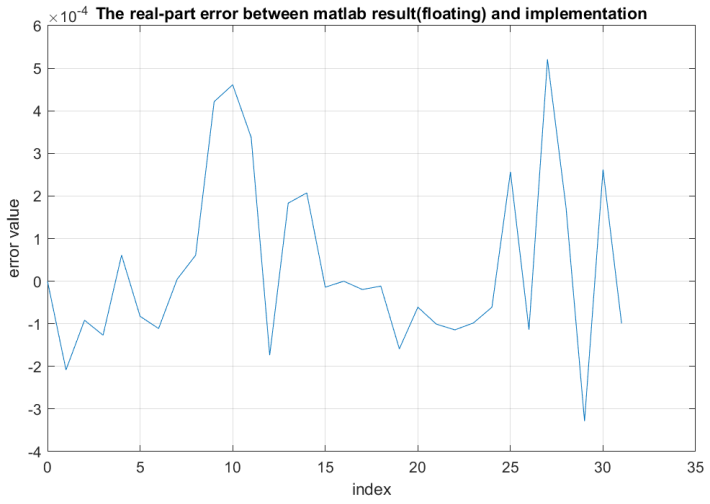
The real-part error between matlab result(fixed) and implementation:



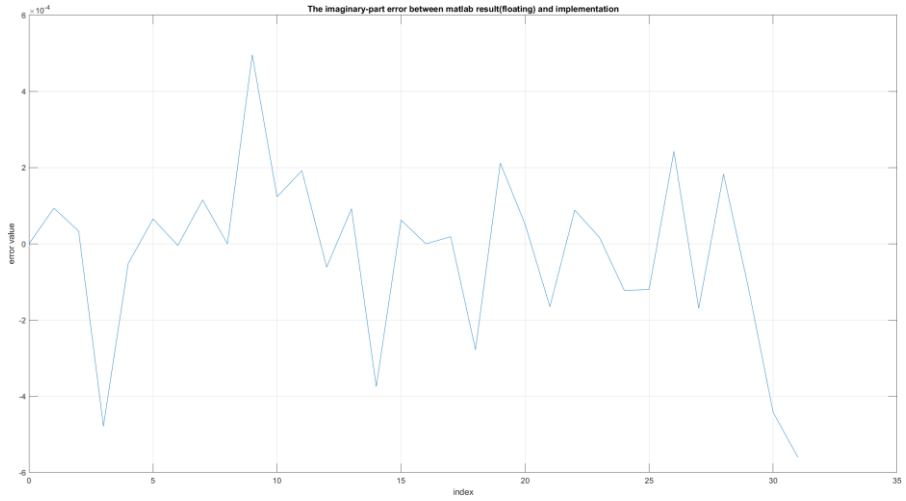
The imaginary-part error between matlab result(fixed) and implementation:



The real-part error between matlab result(floating) and implementation:



The imaginary-part error between matlab result(floating) and implementation:



8. Show your measurement results and paste the measurement results in your report. (demo until 12/19)

`Rst:` 重置

`Clk:` 時脈

`LI_real: MDC IFFT` 輸入 `real part`

`LI_imag: MDC IFFT` 輸入 `imaginary part`

`P_real: MDC IFFT` 輸出 `real part`

`P_imag: MDC IFFT` 輸出 `imaginary part`

Input part:

Output part