VIVADO Simulator

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TA : Po-Ta, Chen

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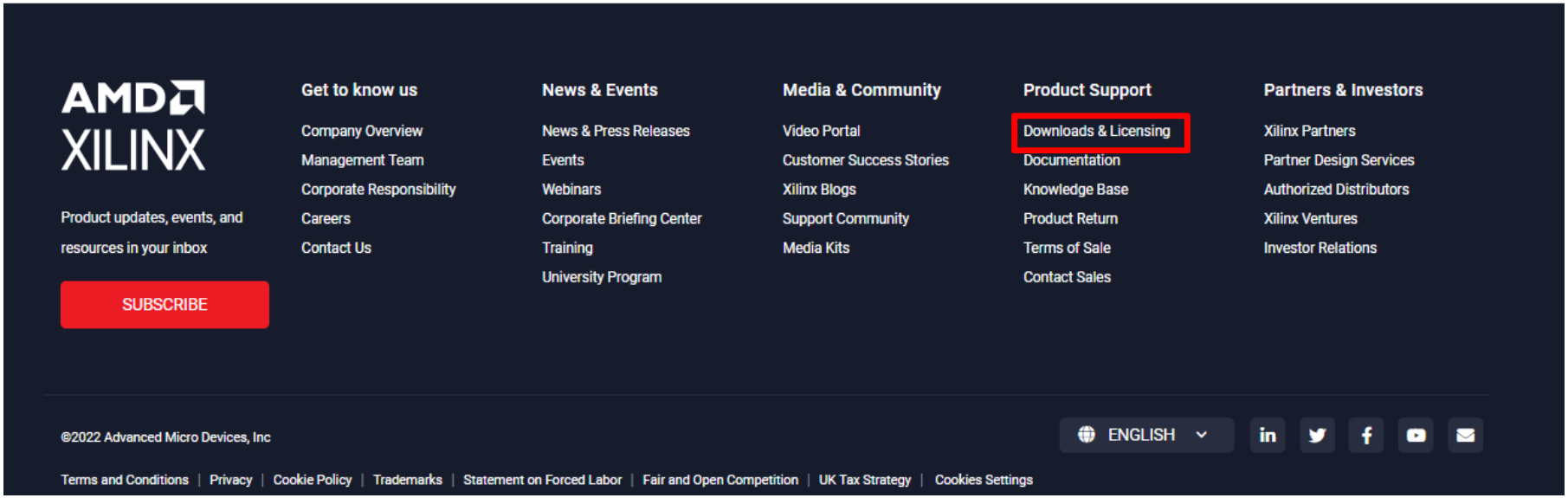

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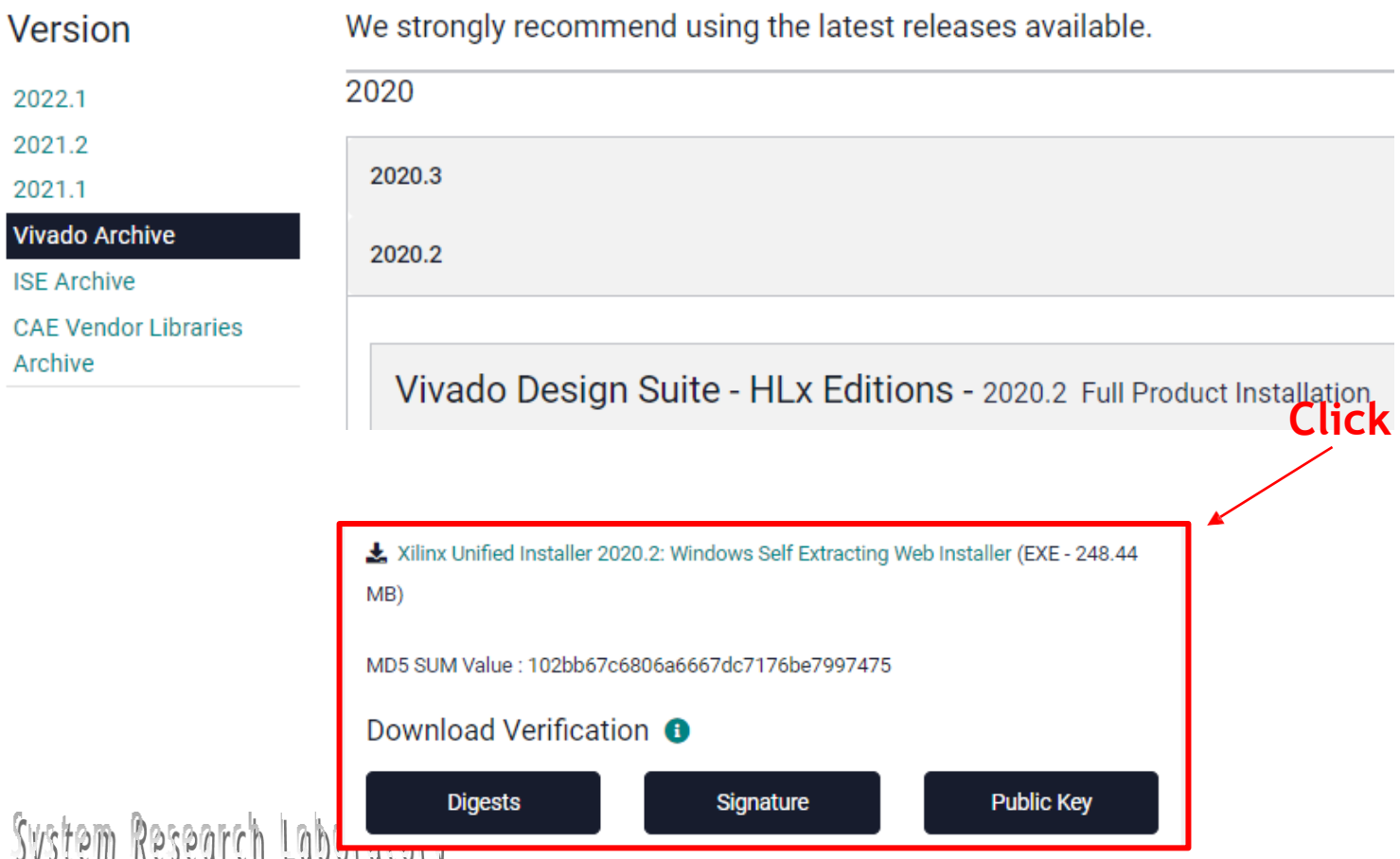

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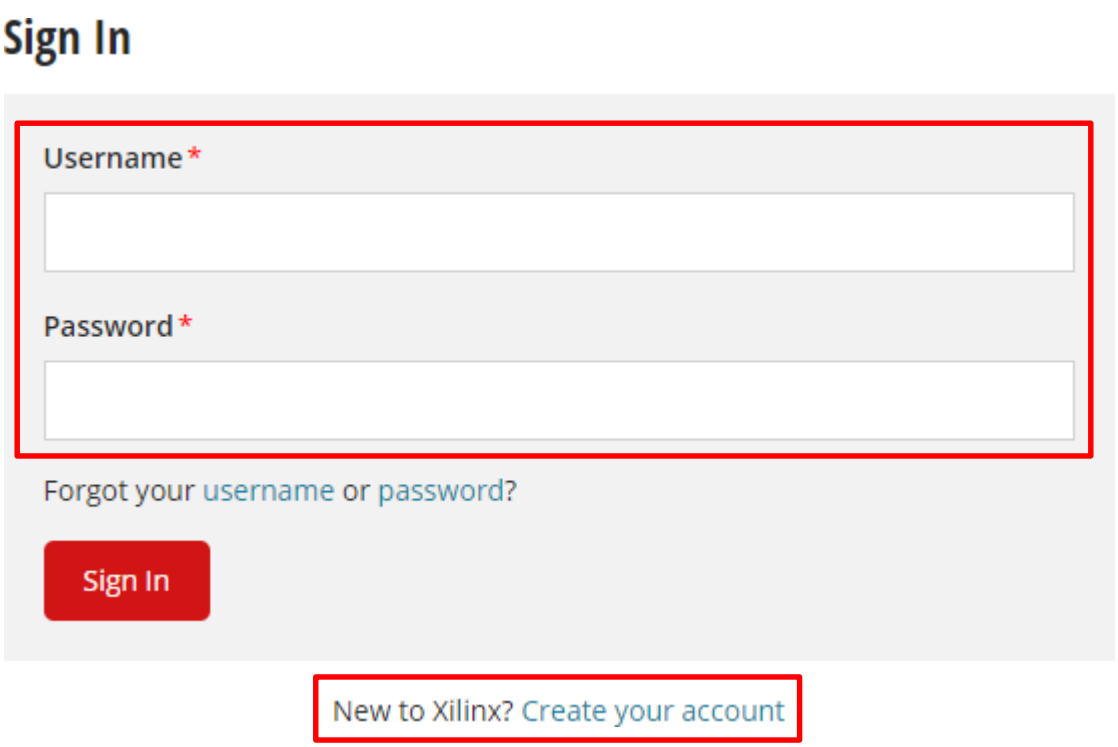

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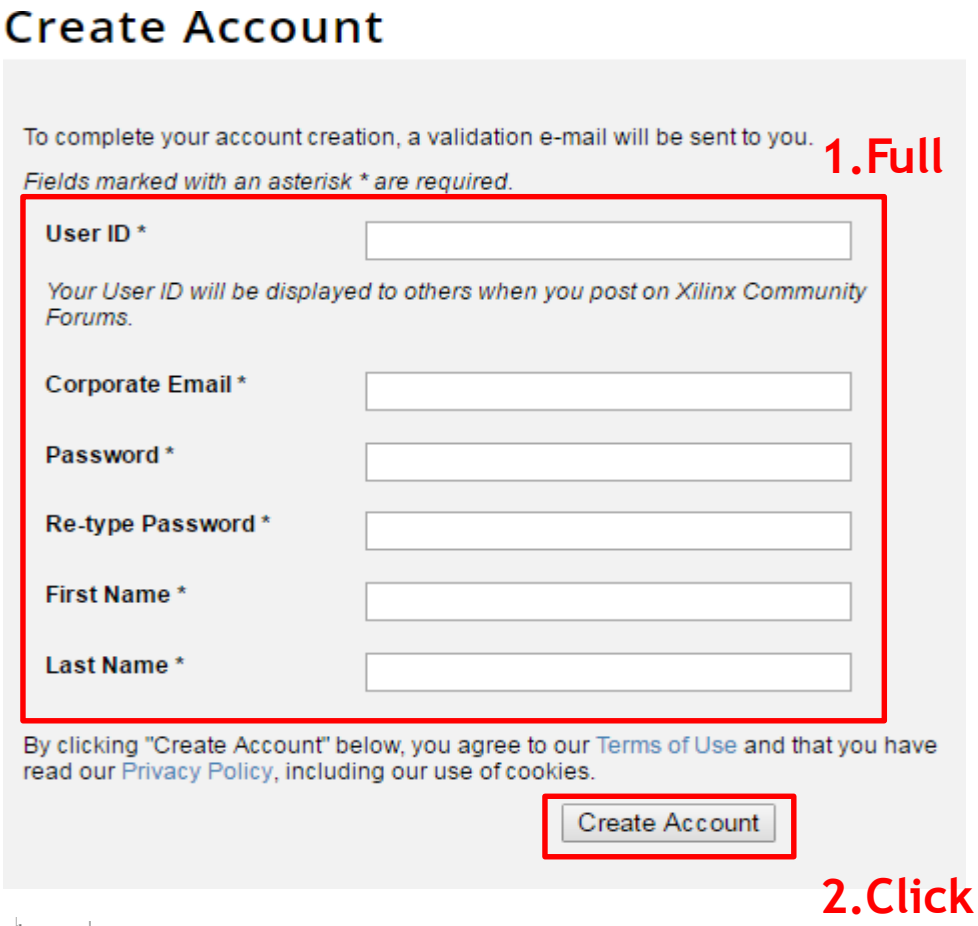

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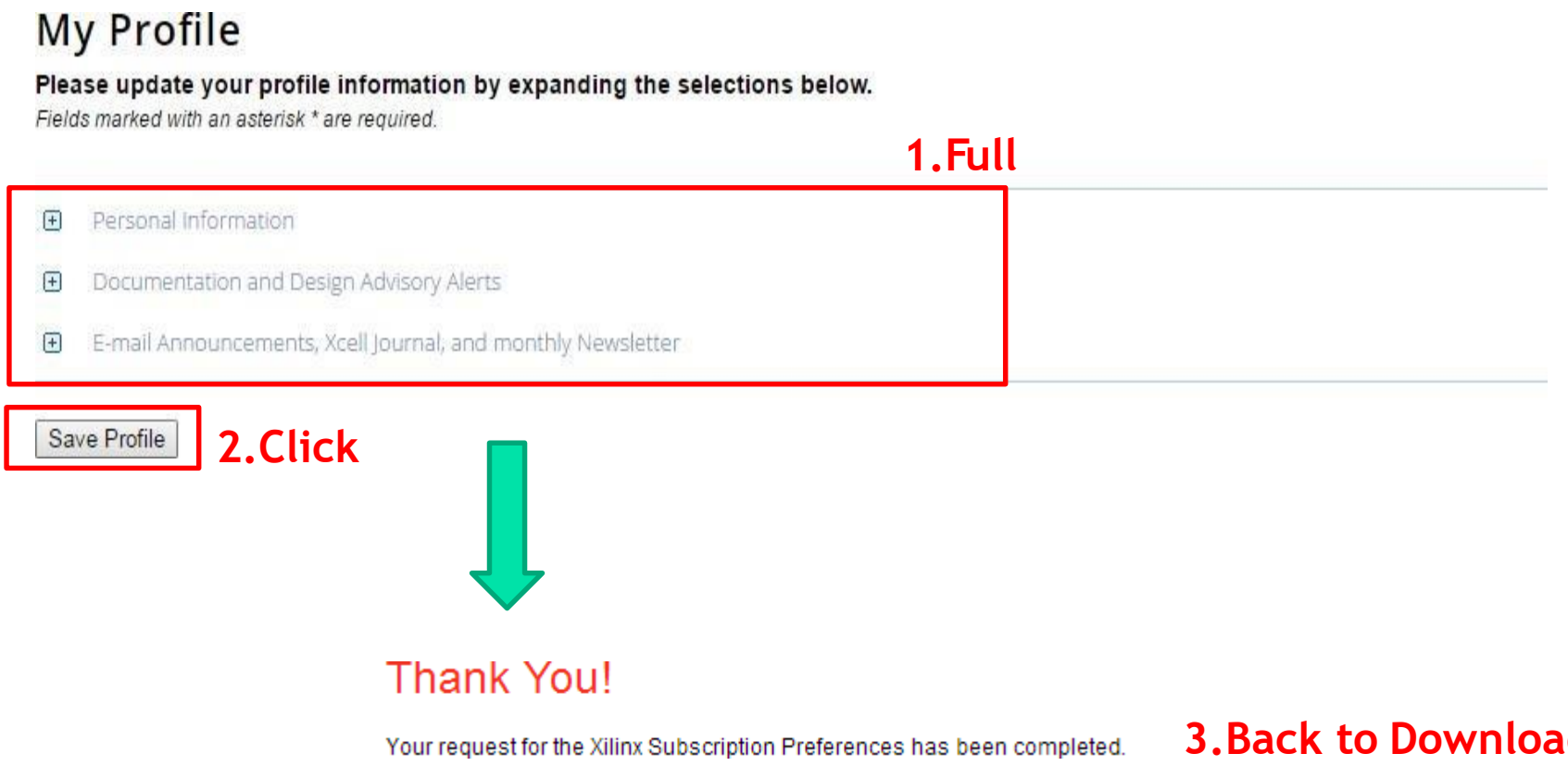

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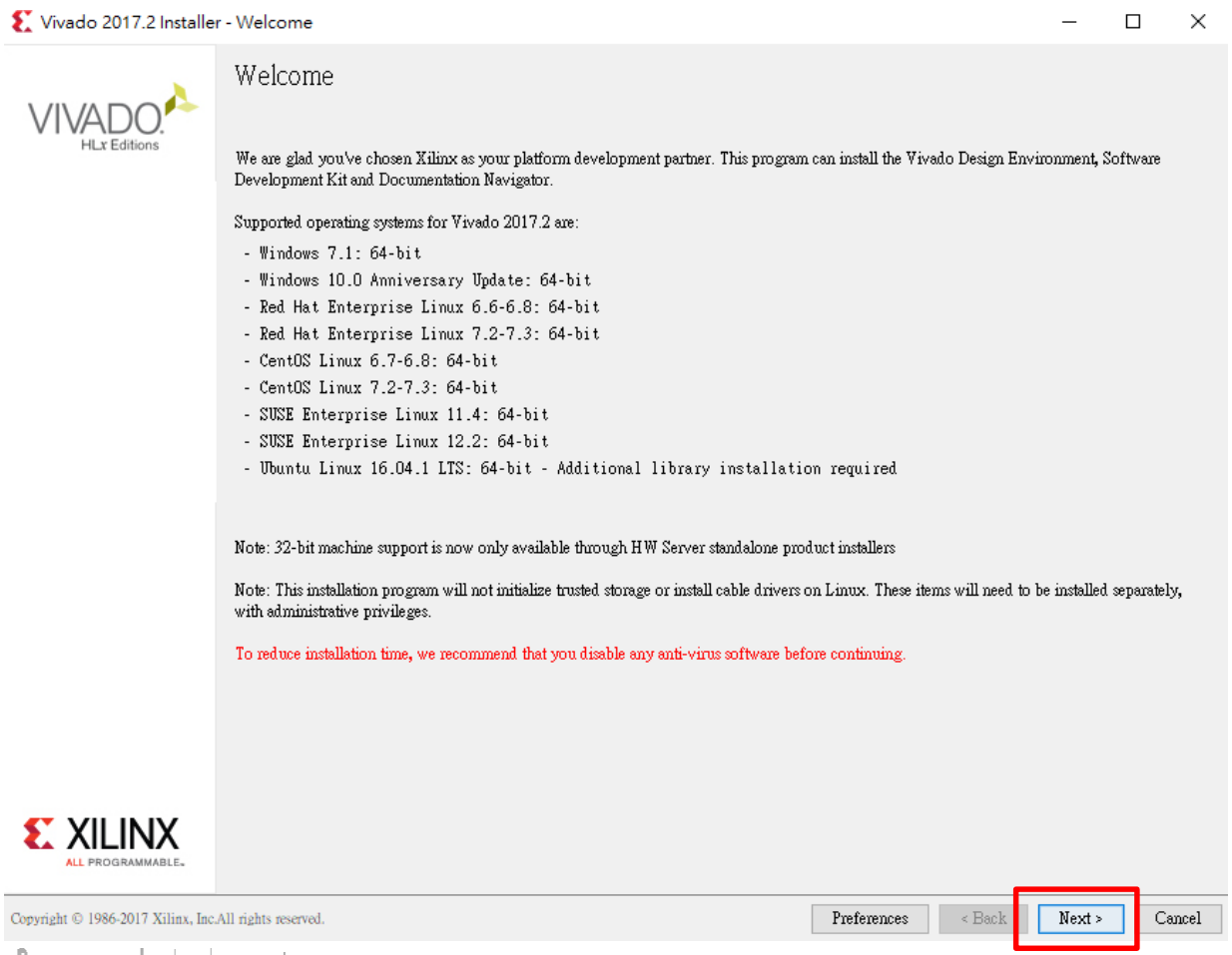

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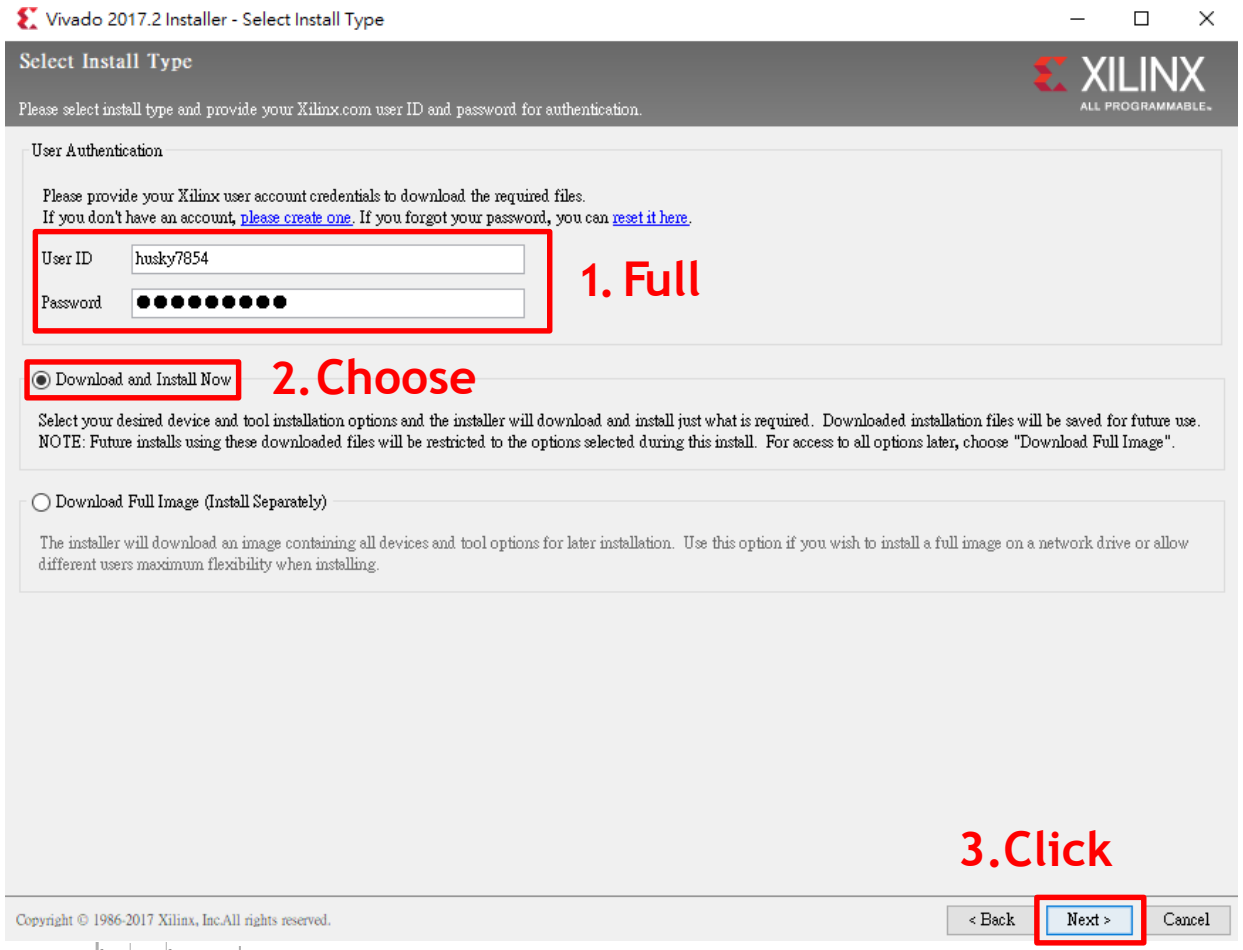

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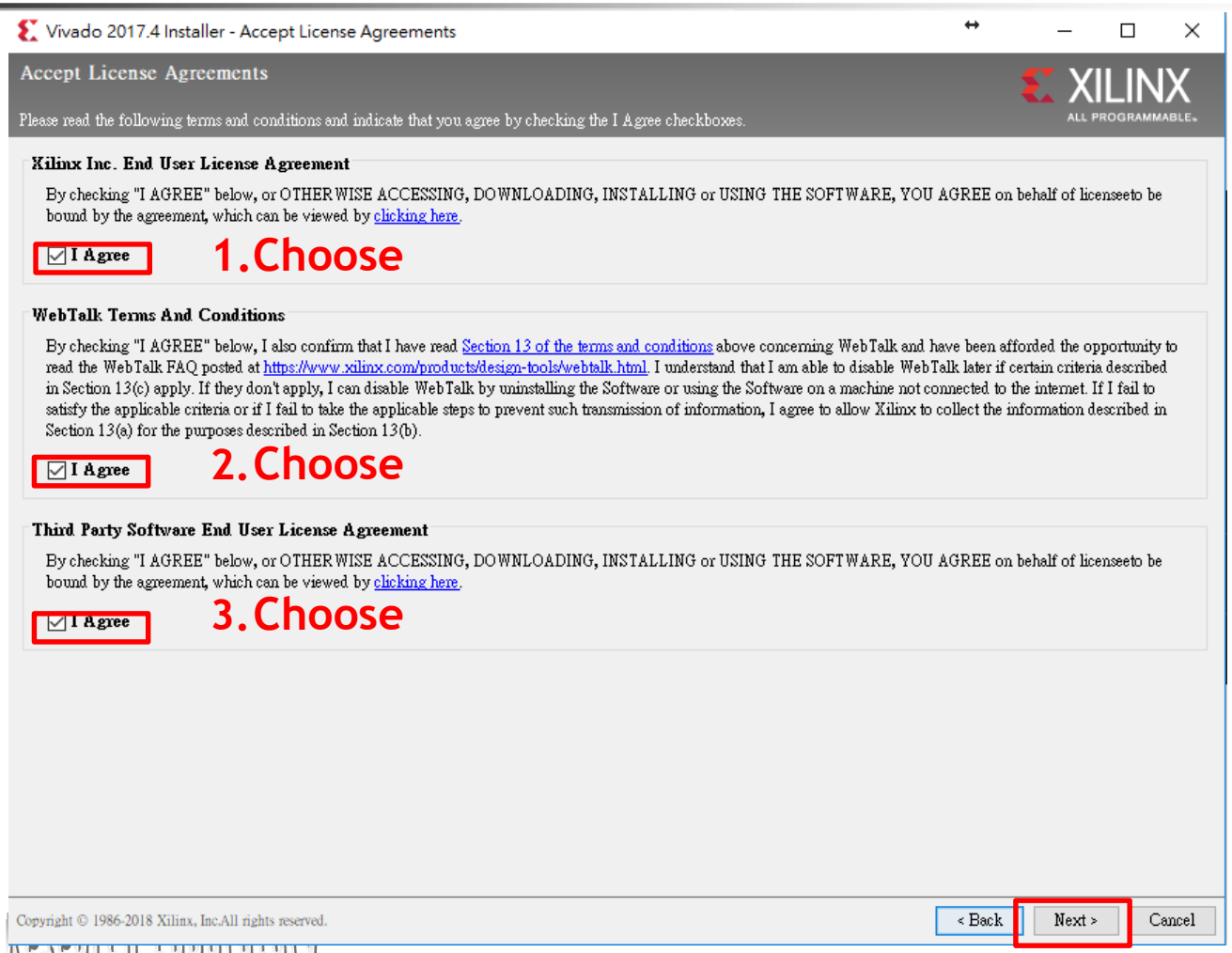

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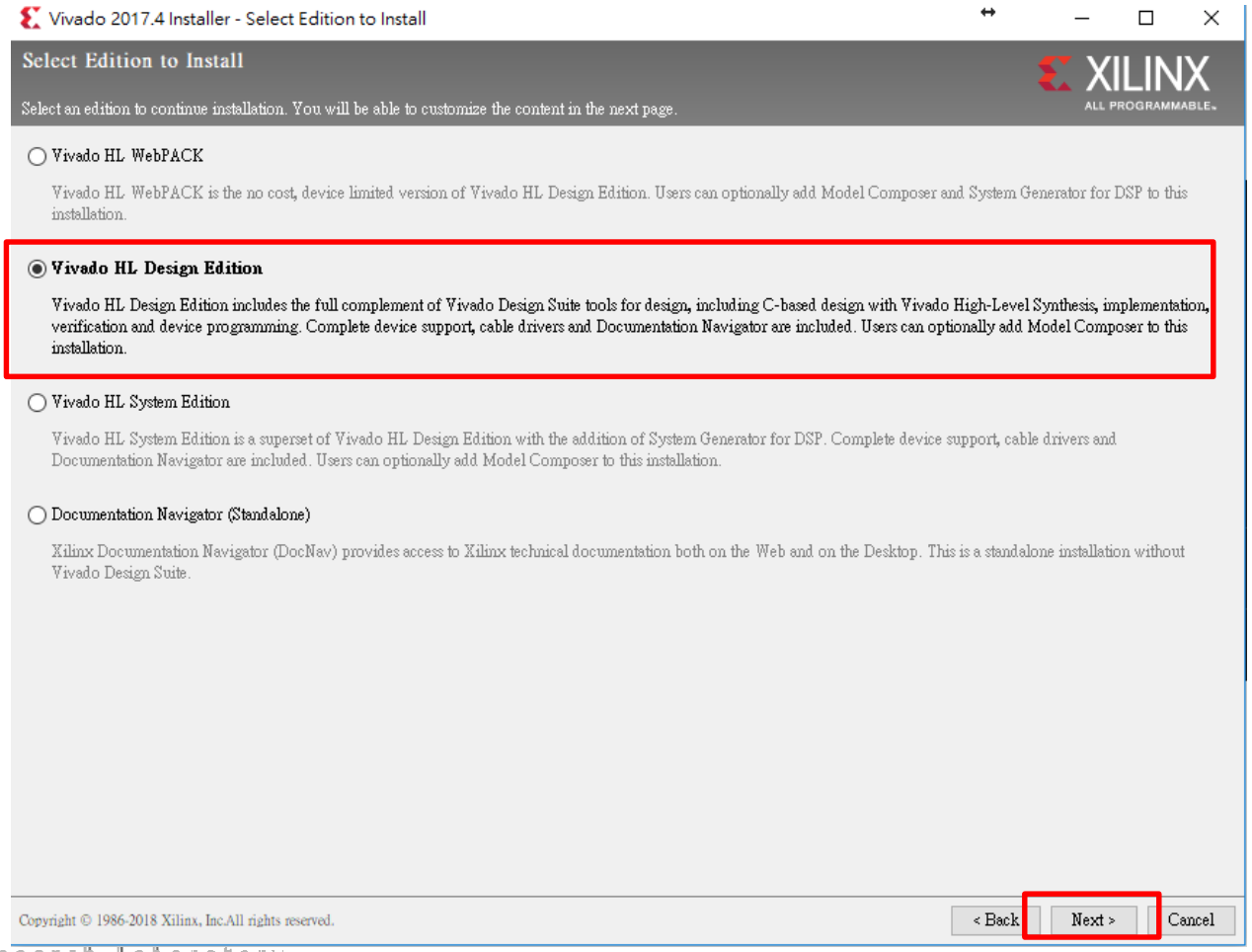

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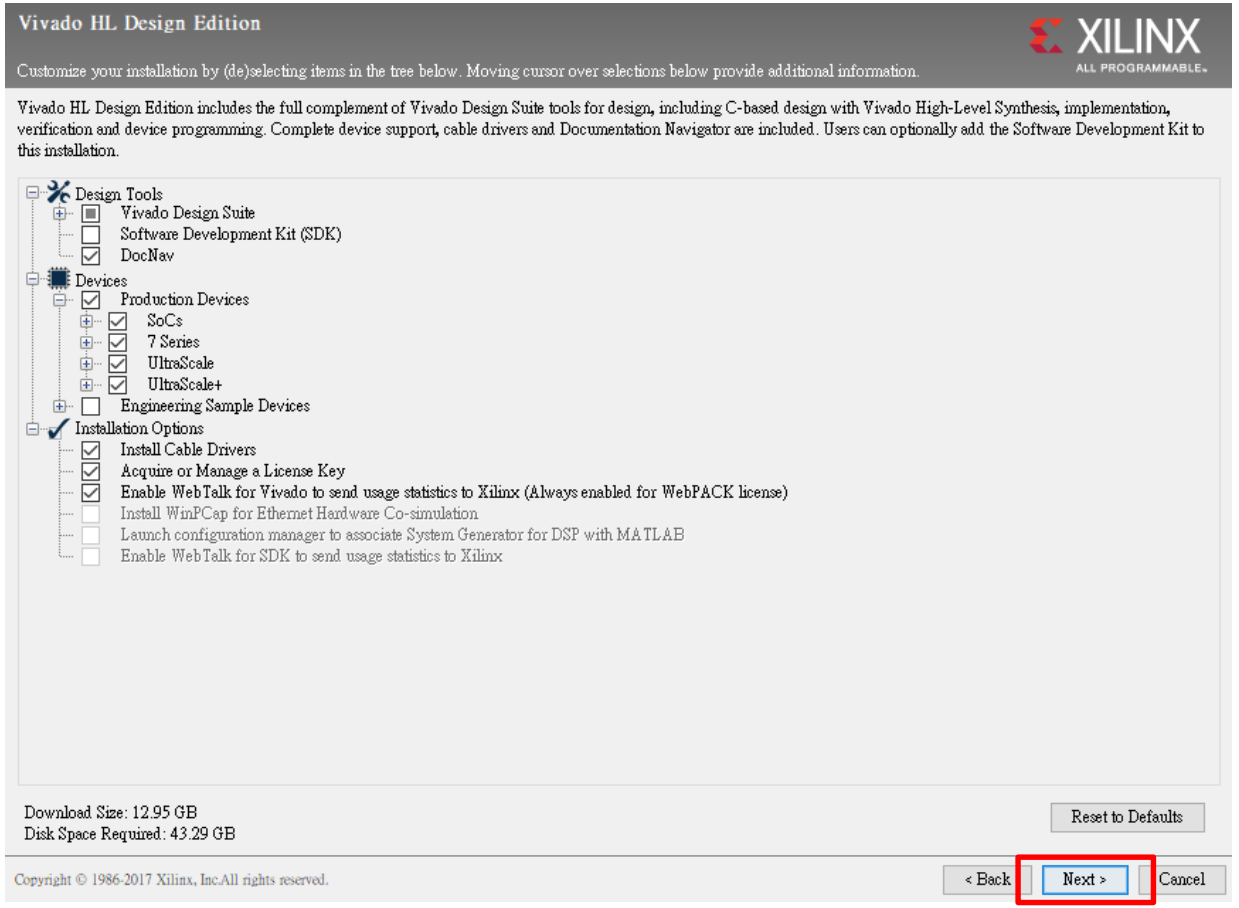

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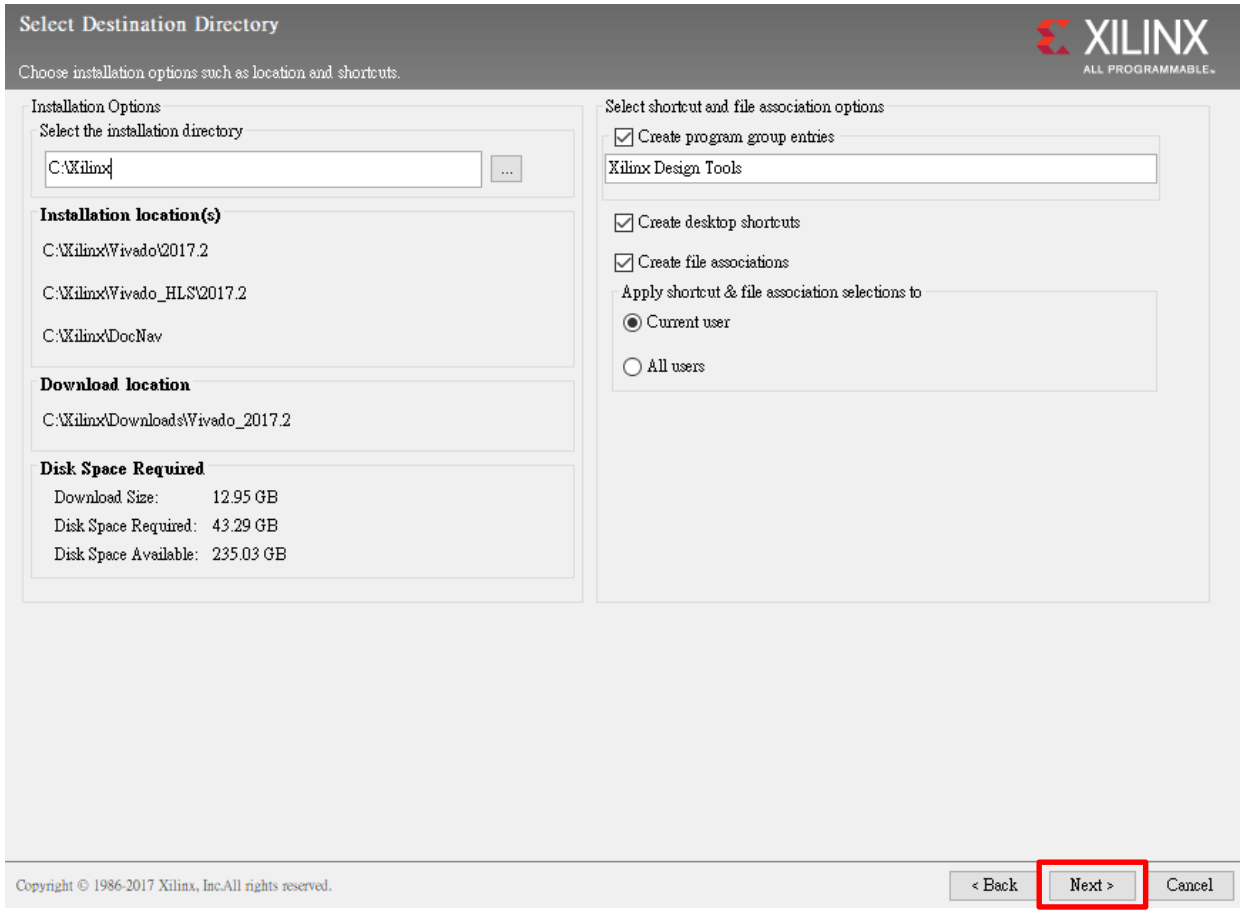

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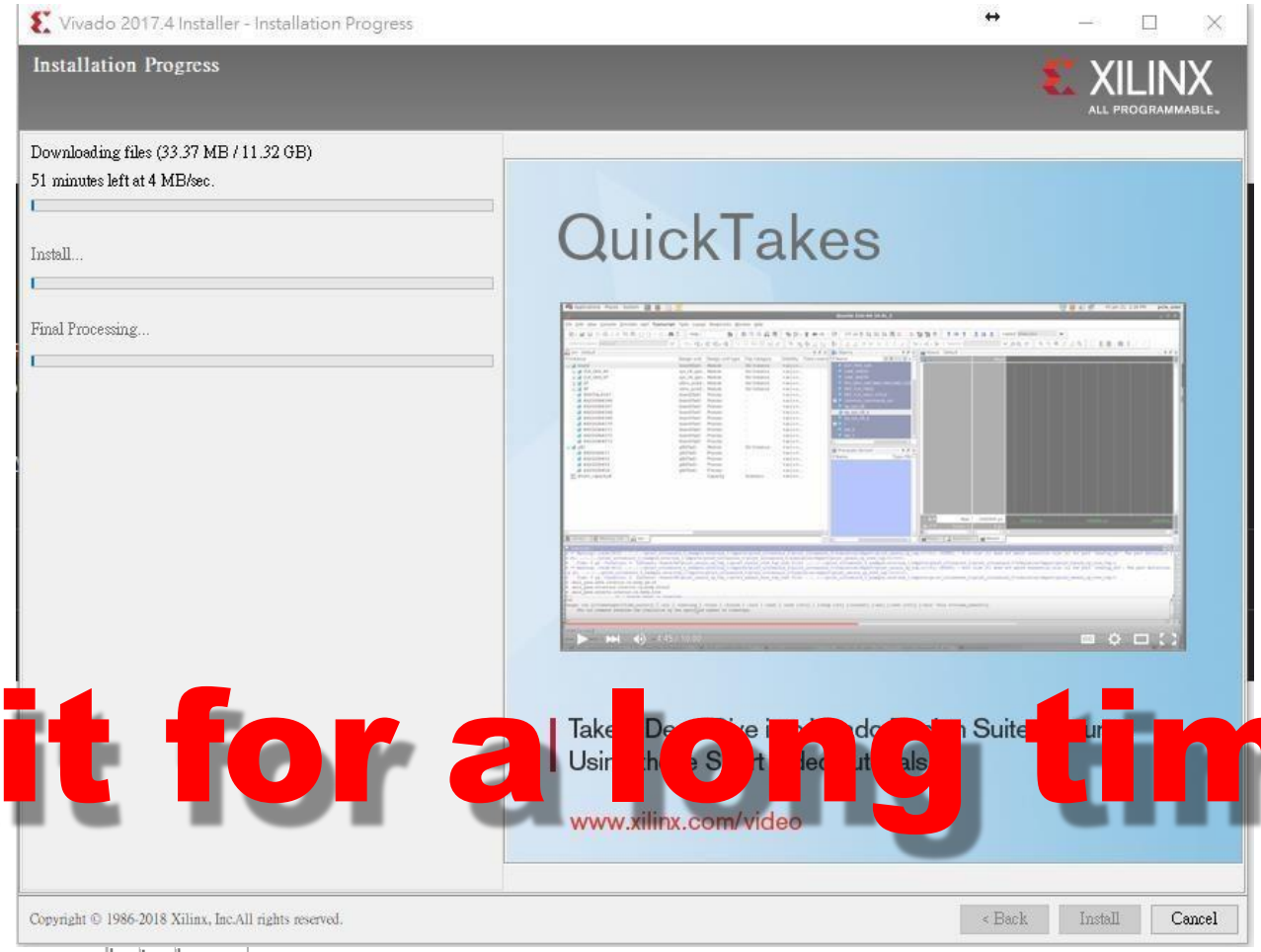

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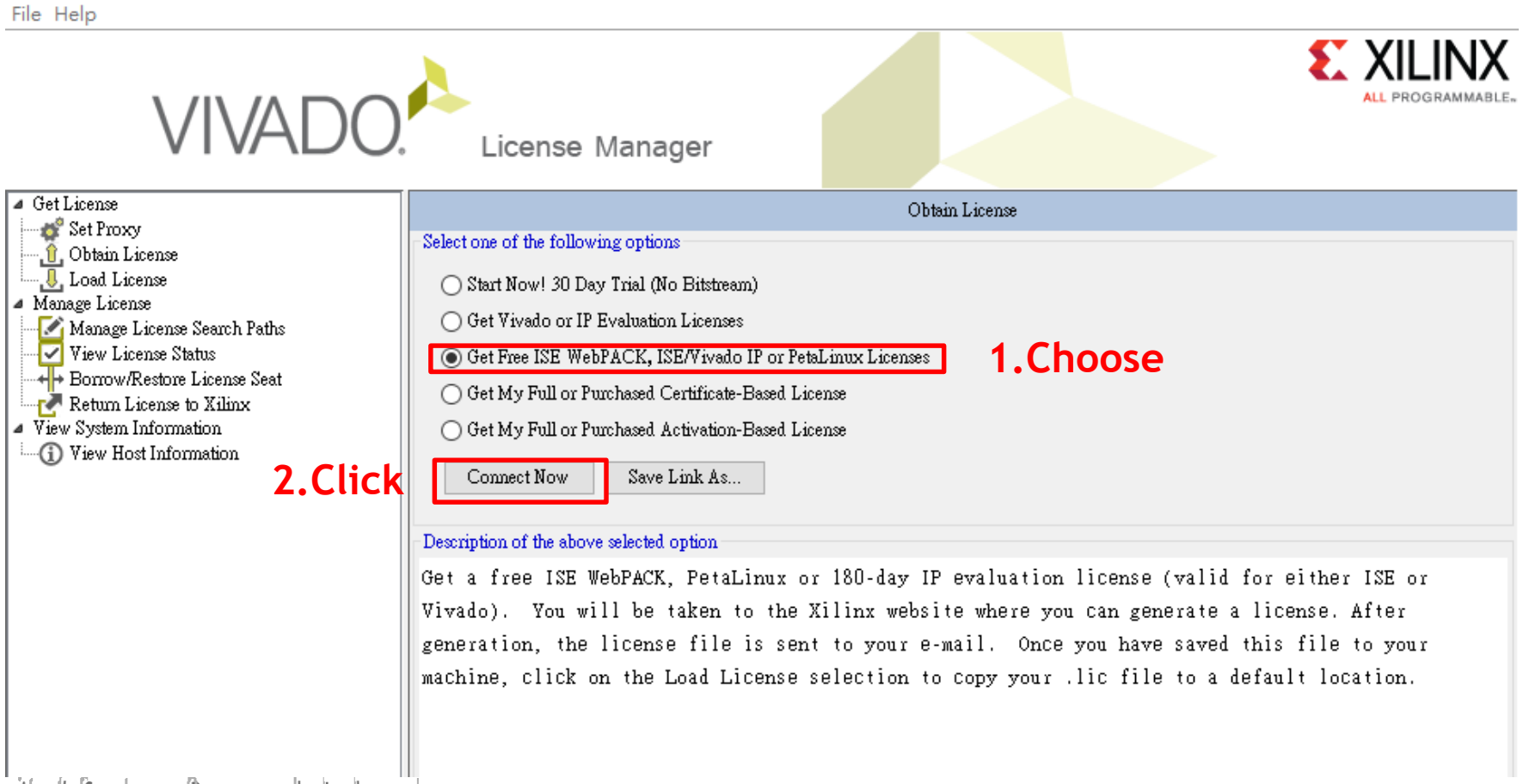

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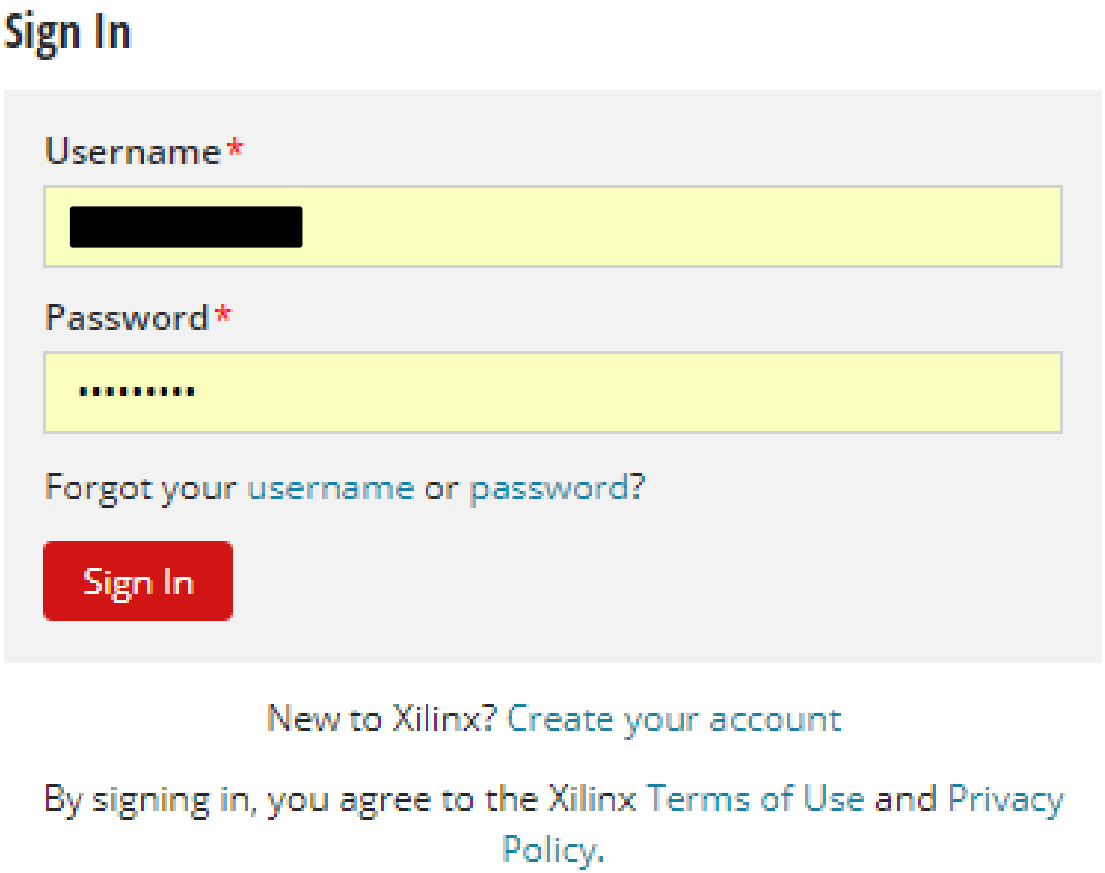

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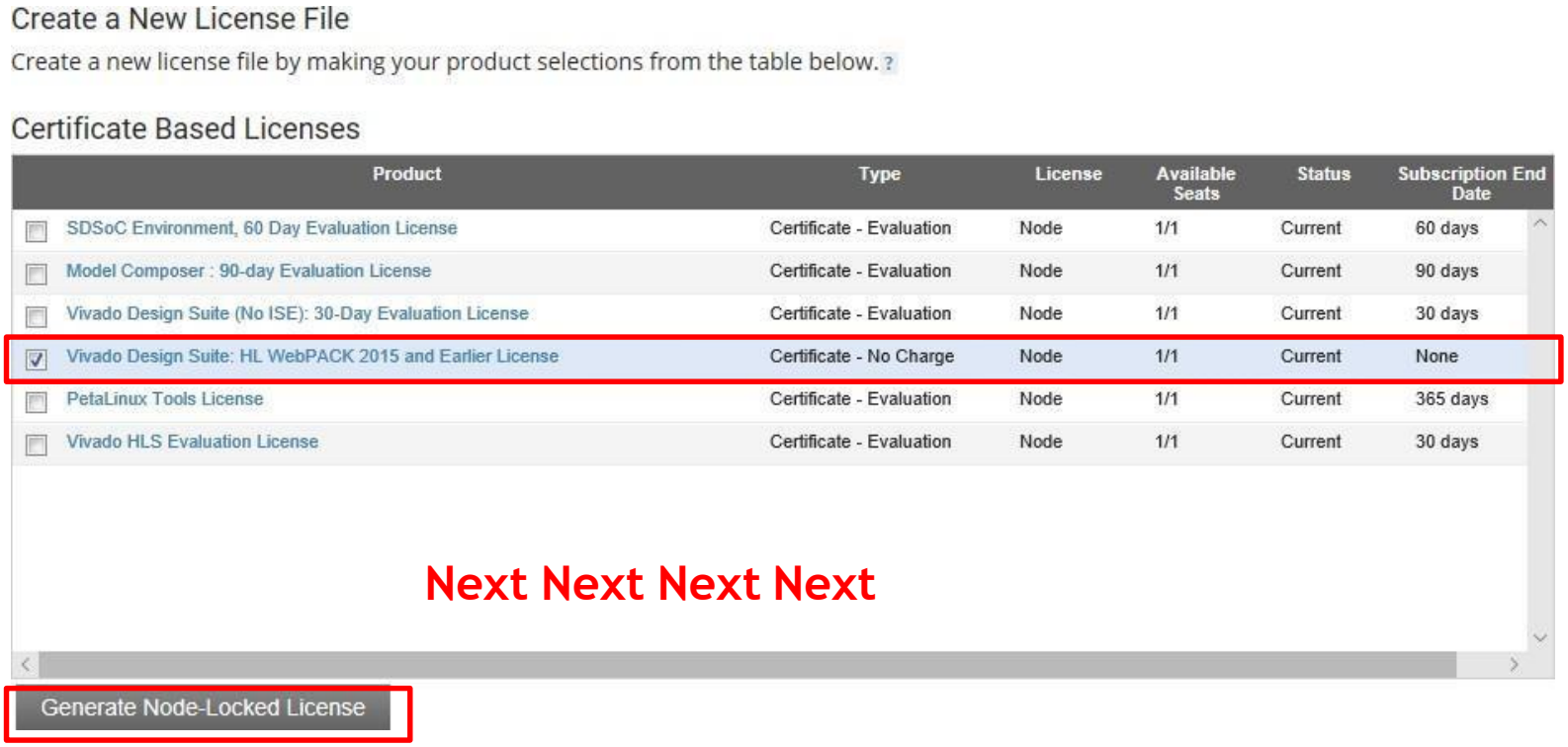

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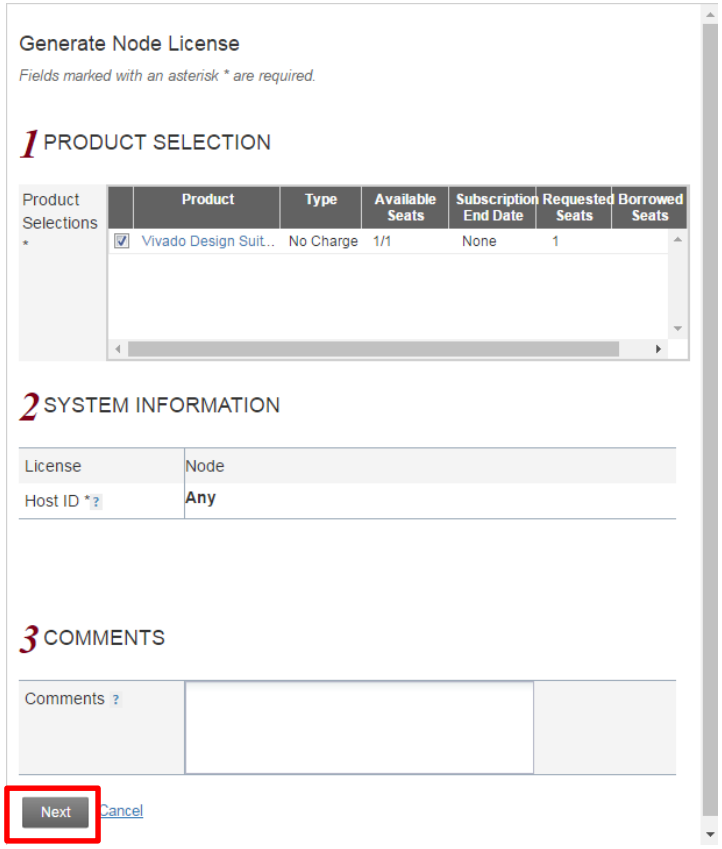

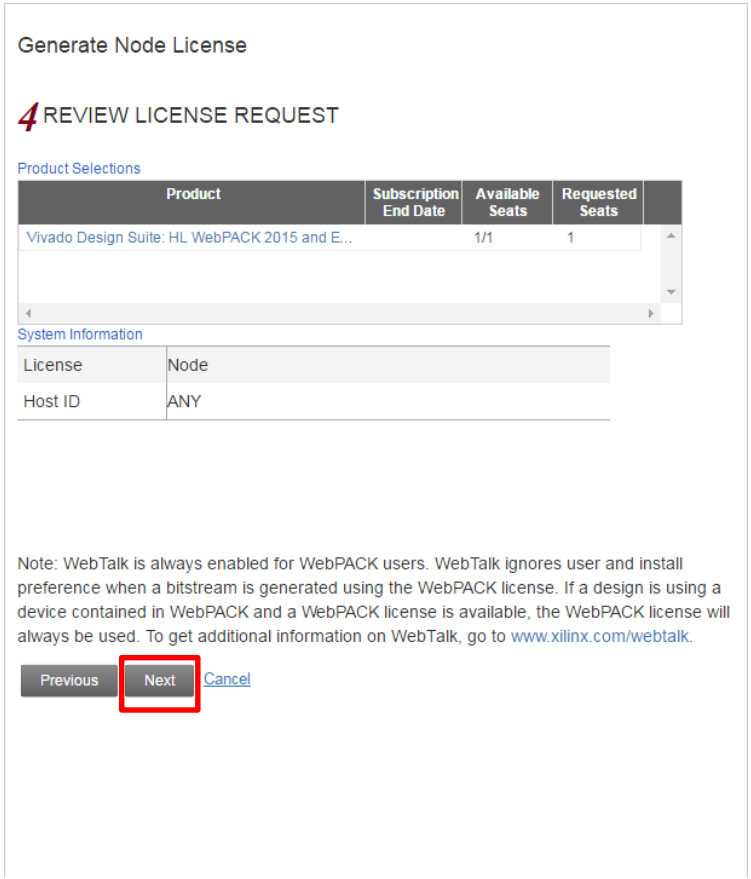

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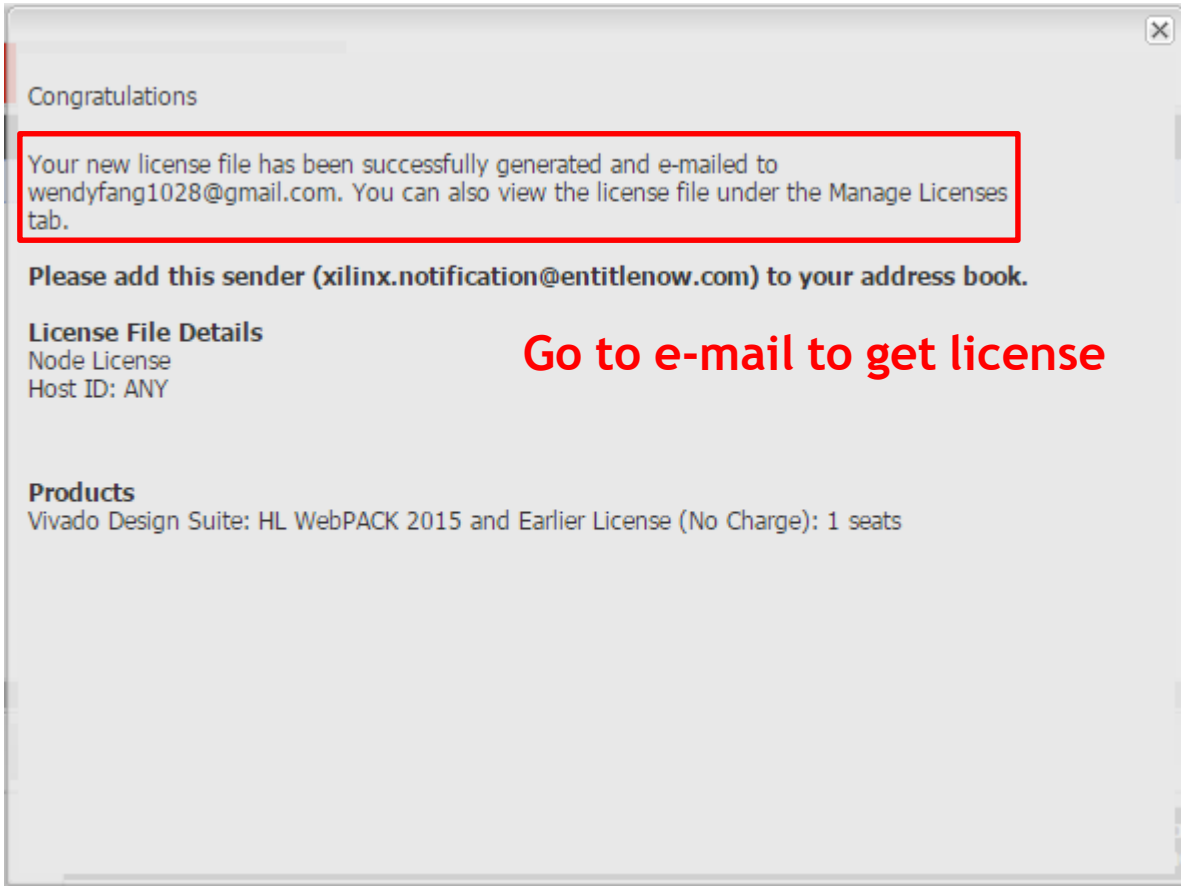

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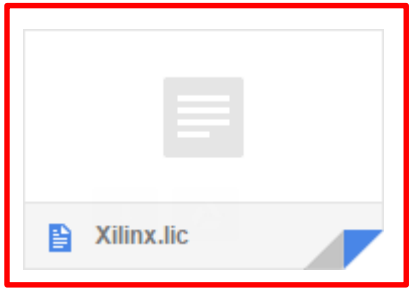

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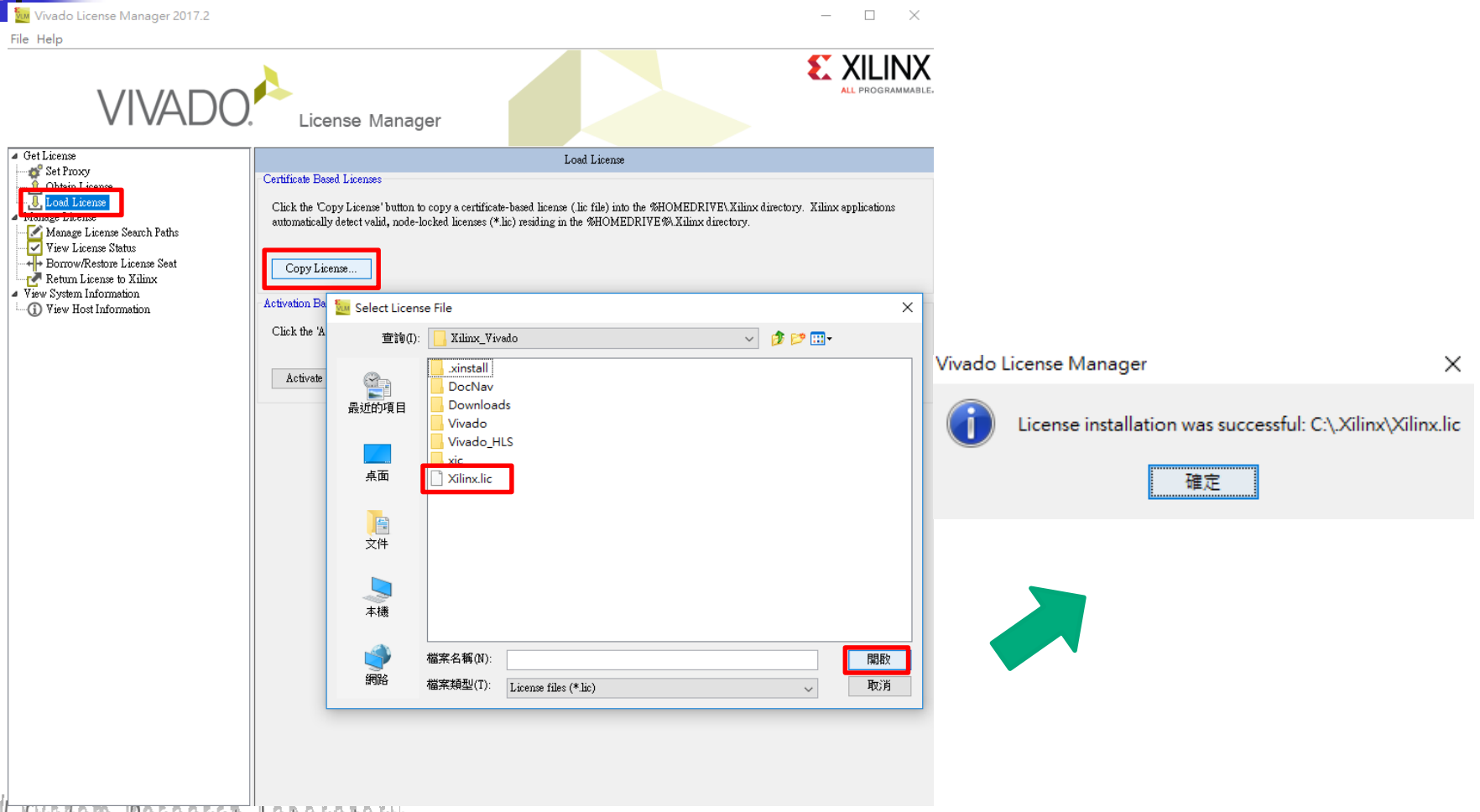

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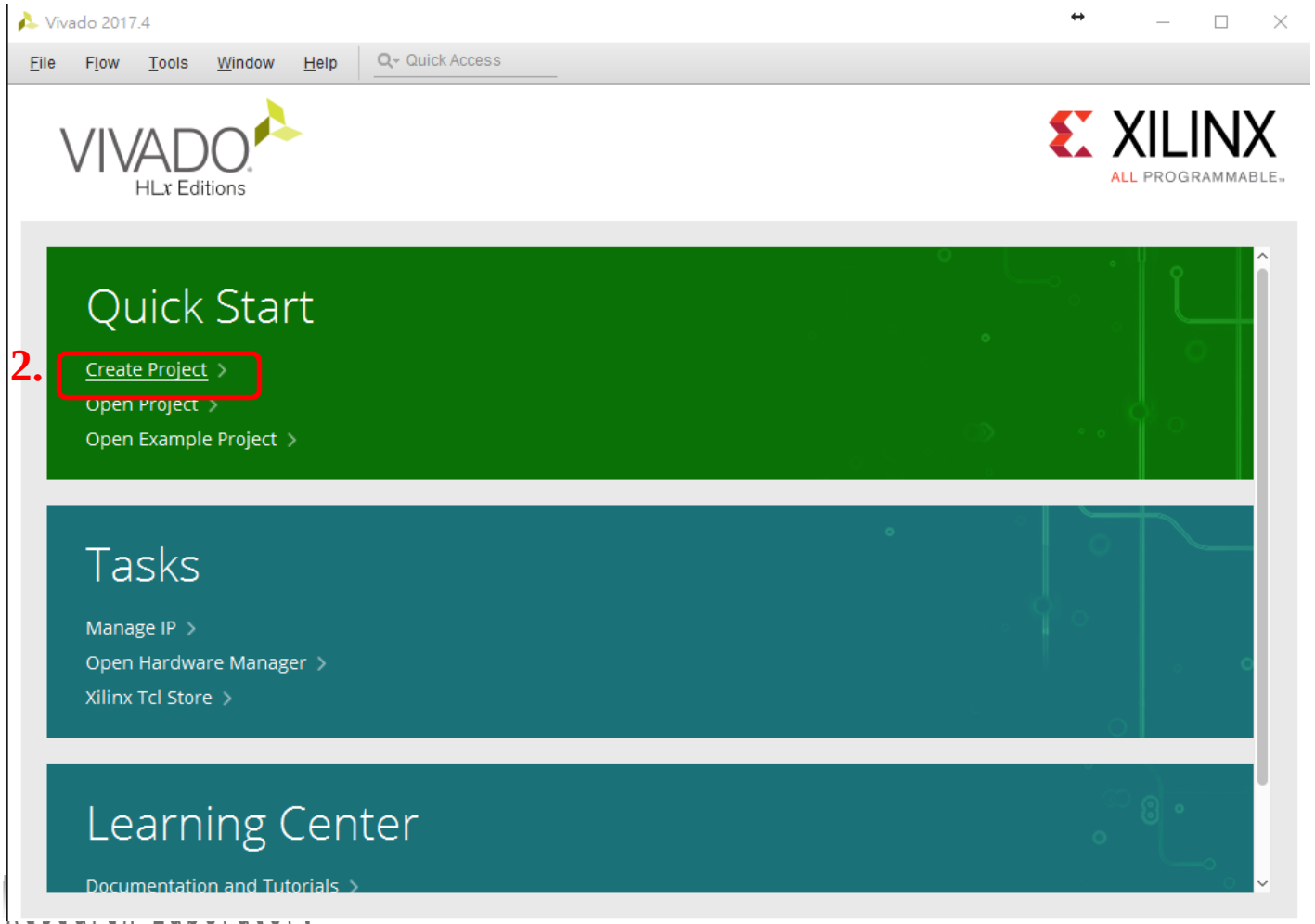

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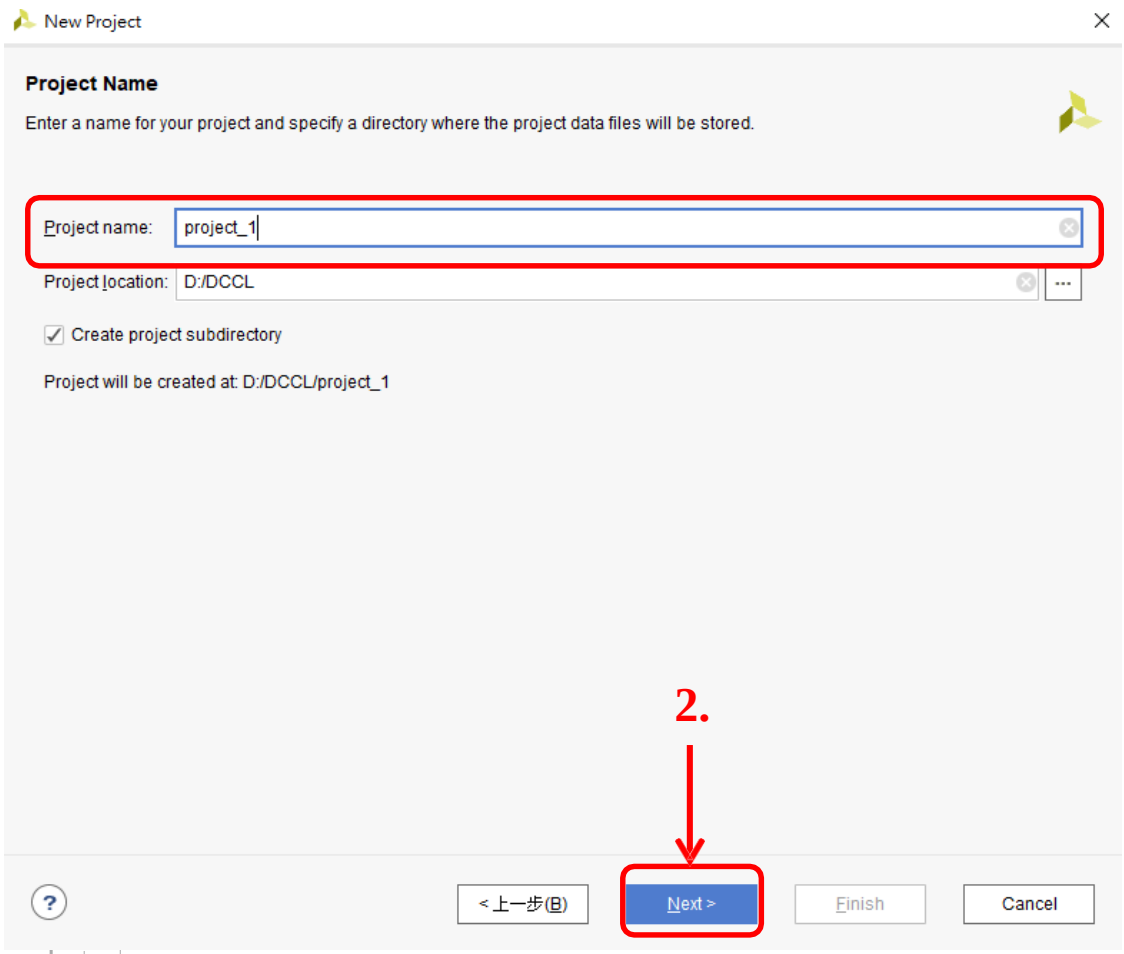
1. Project name



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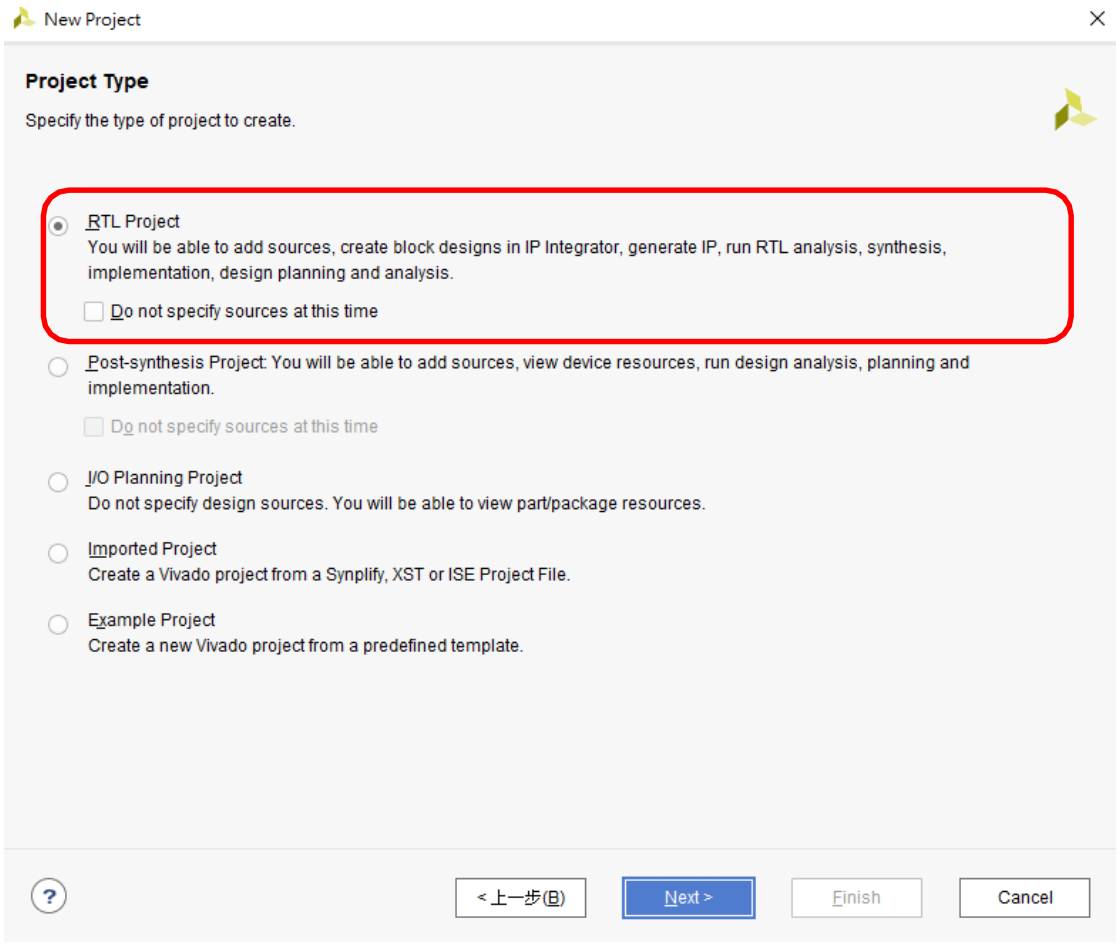

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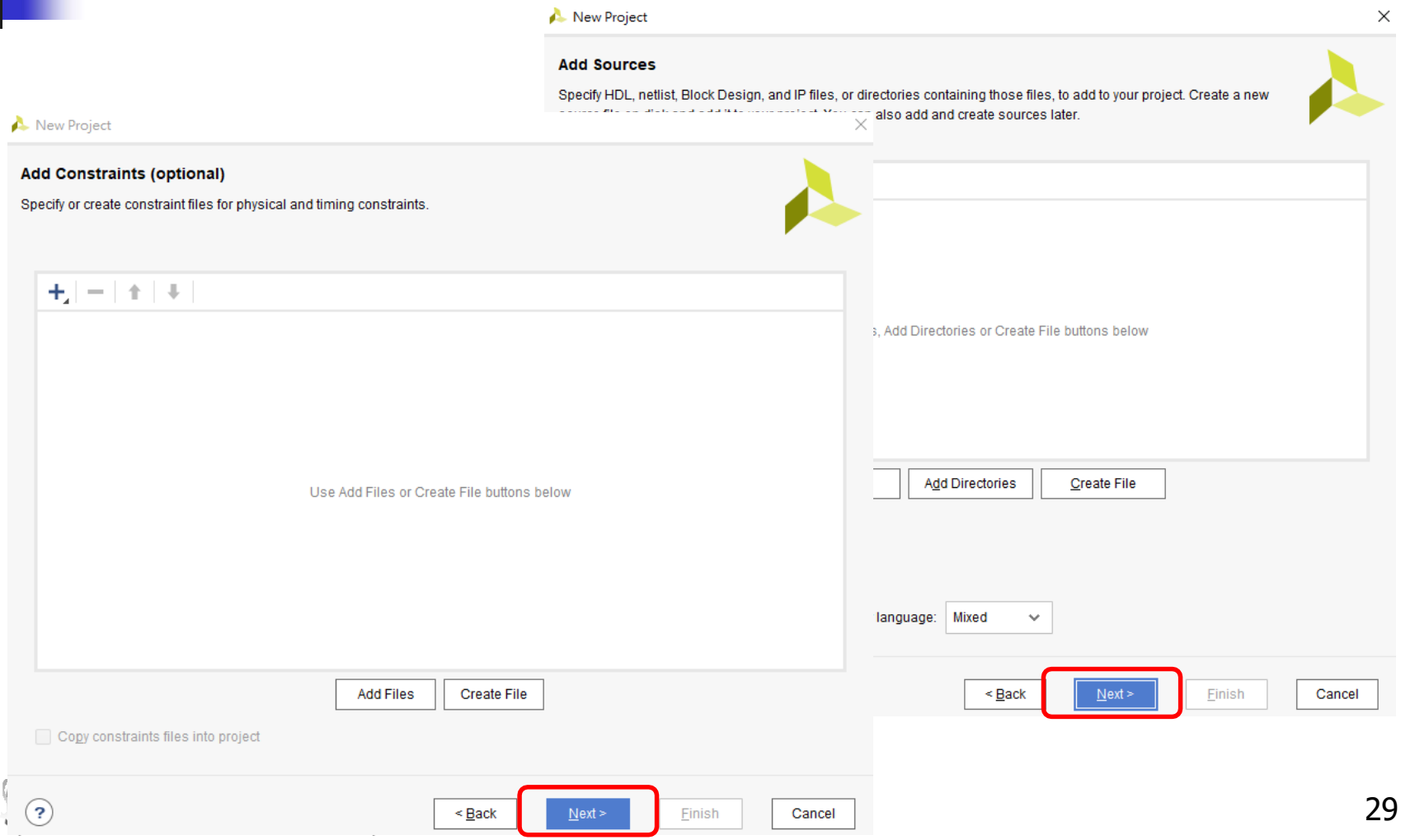

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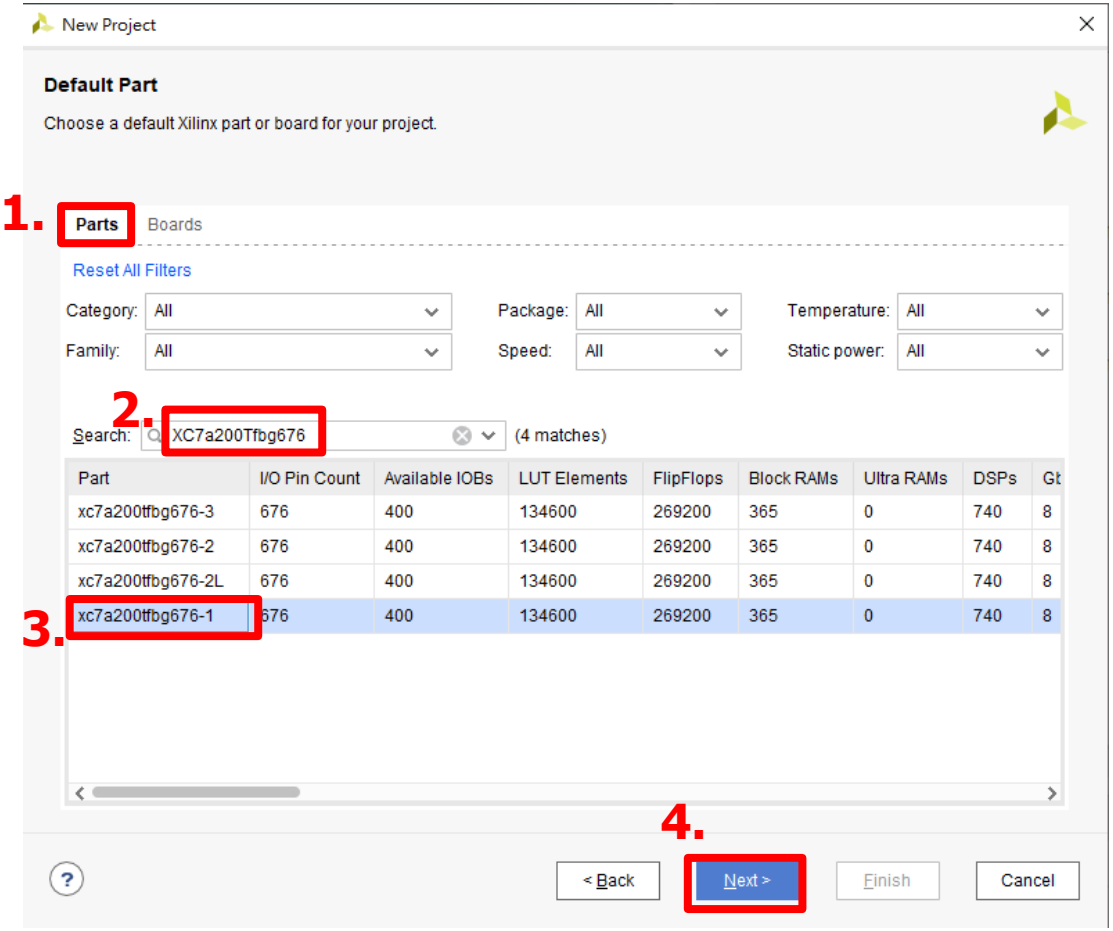

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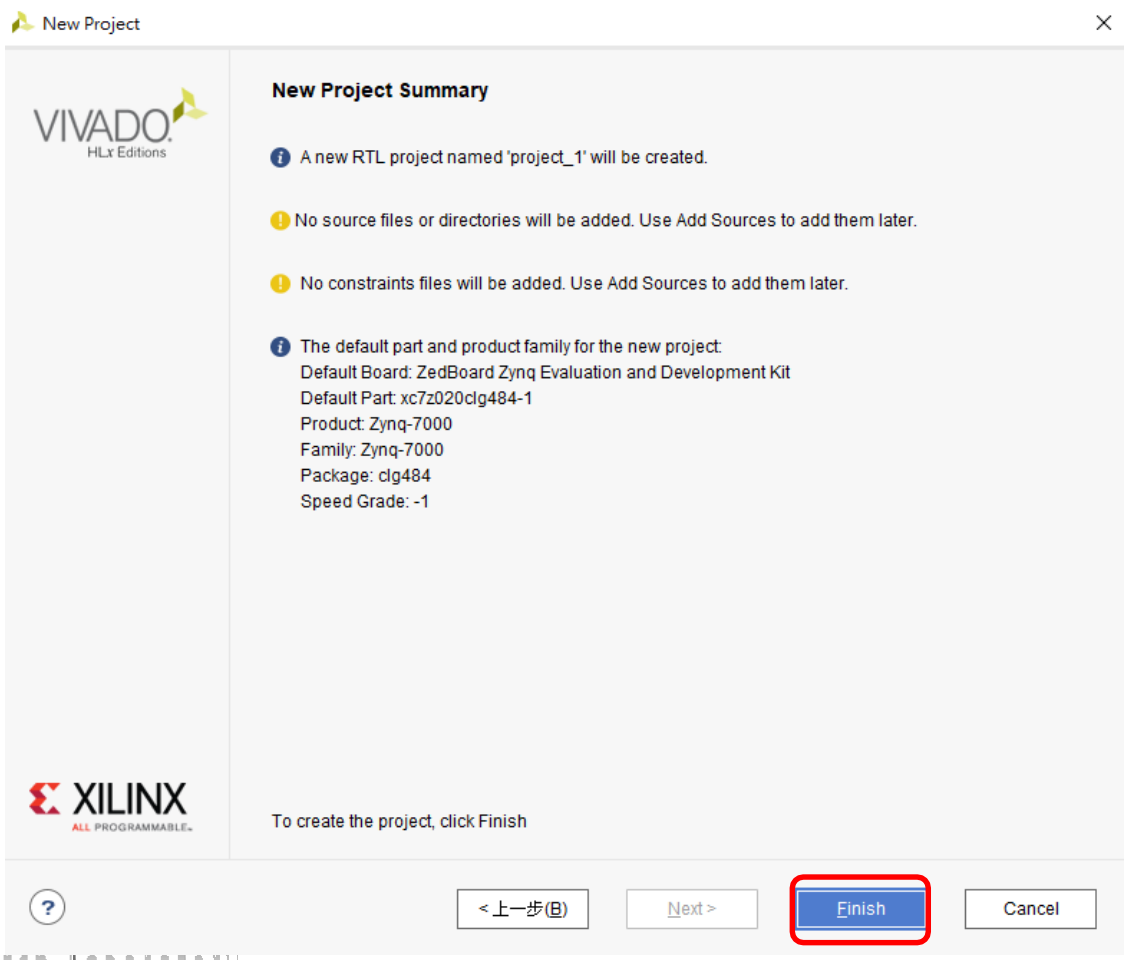

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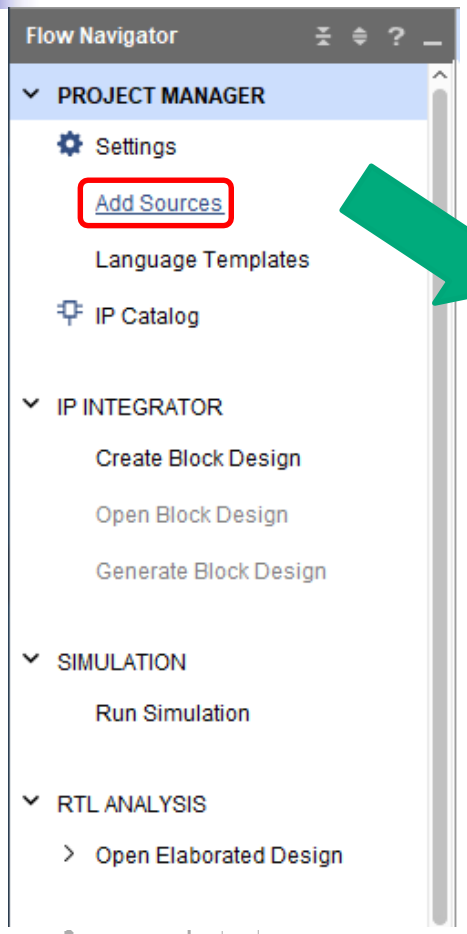

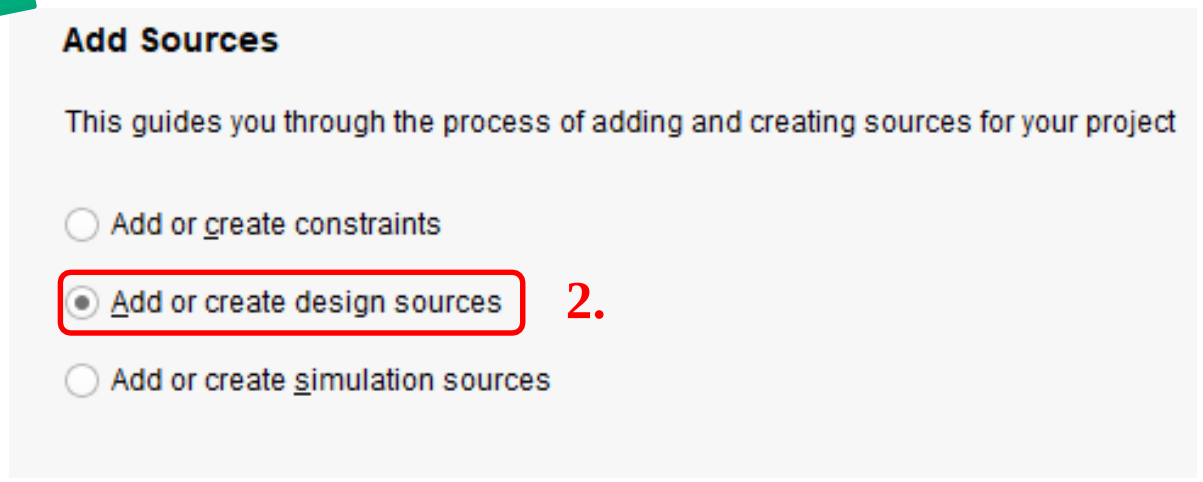

2.

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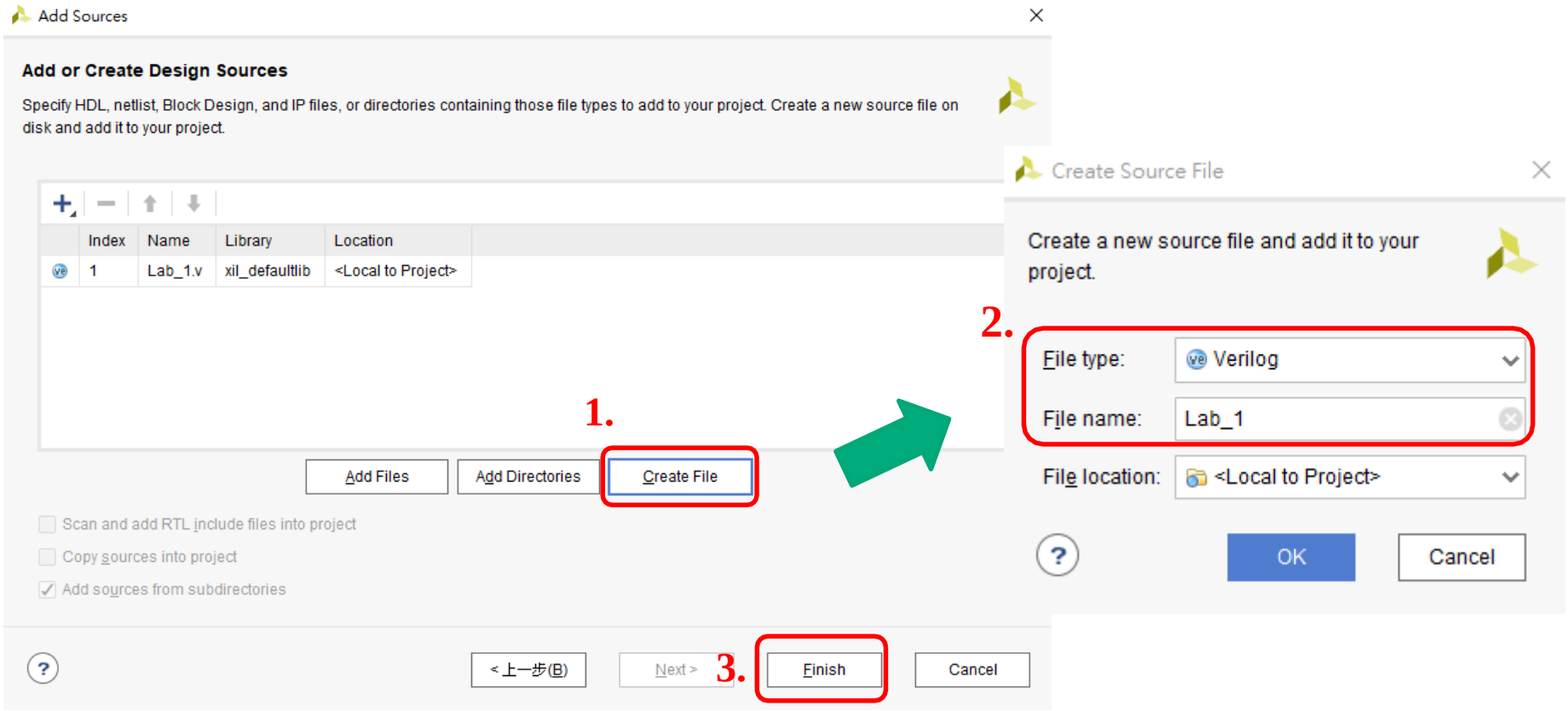

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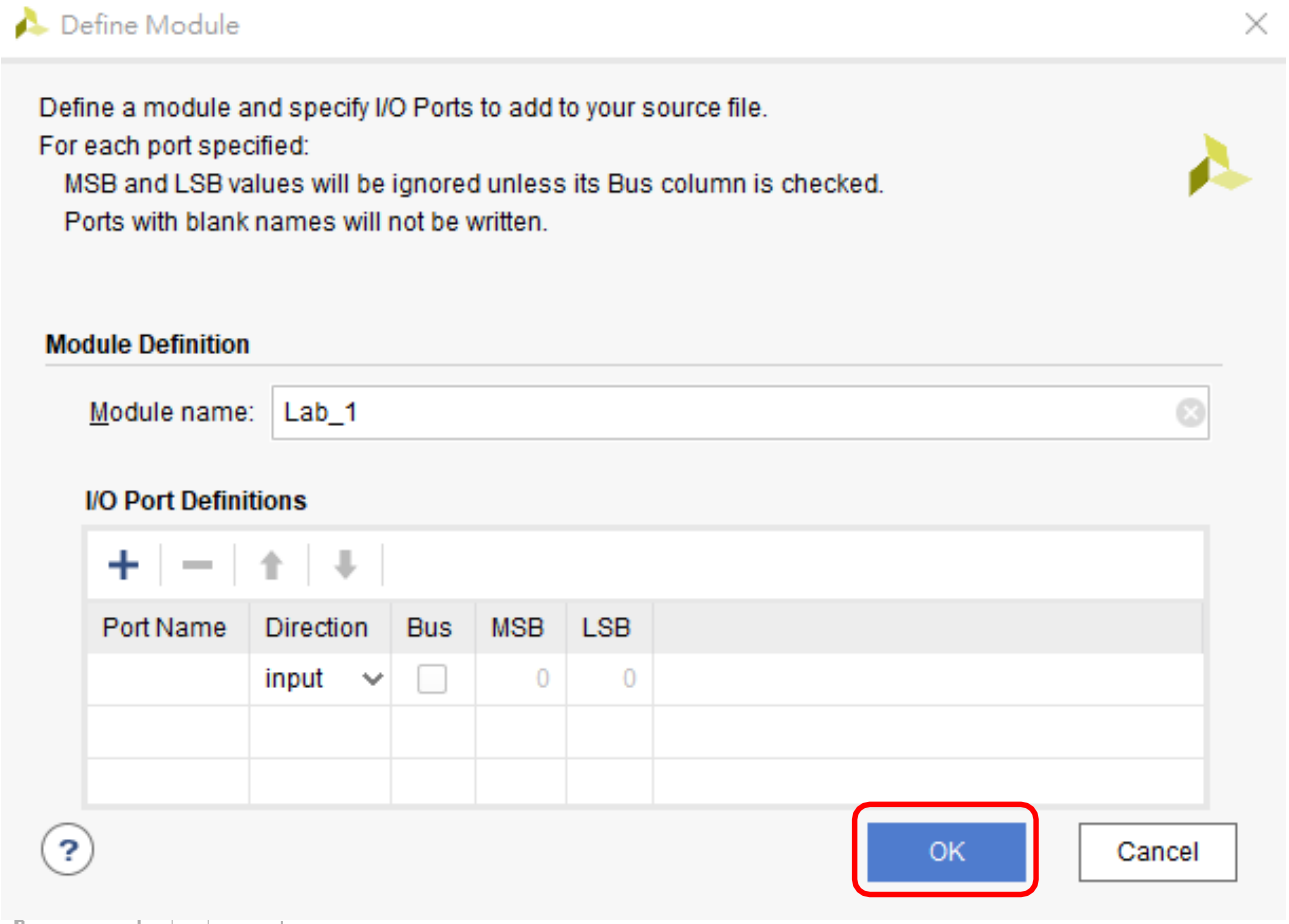
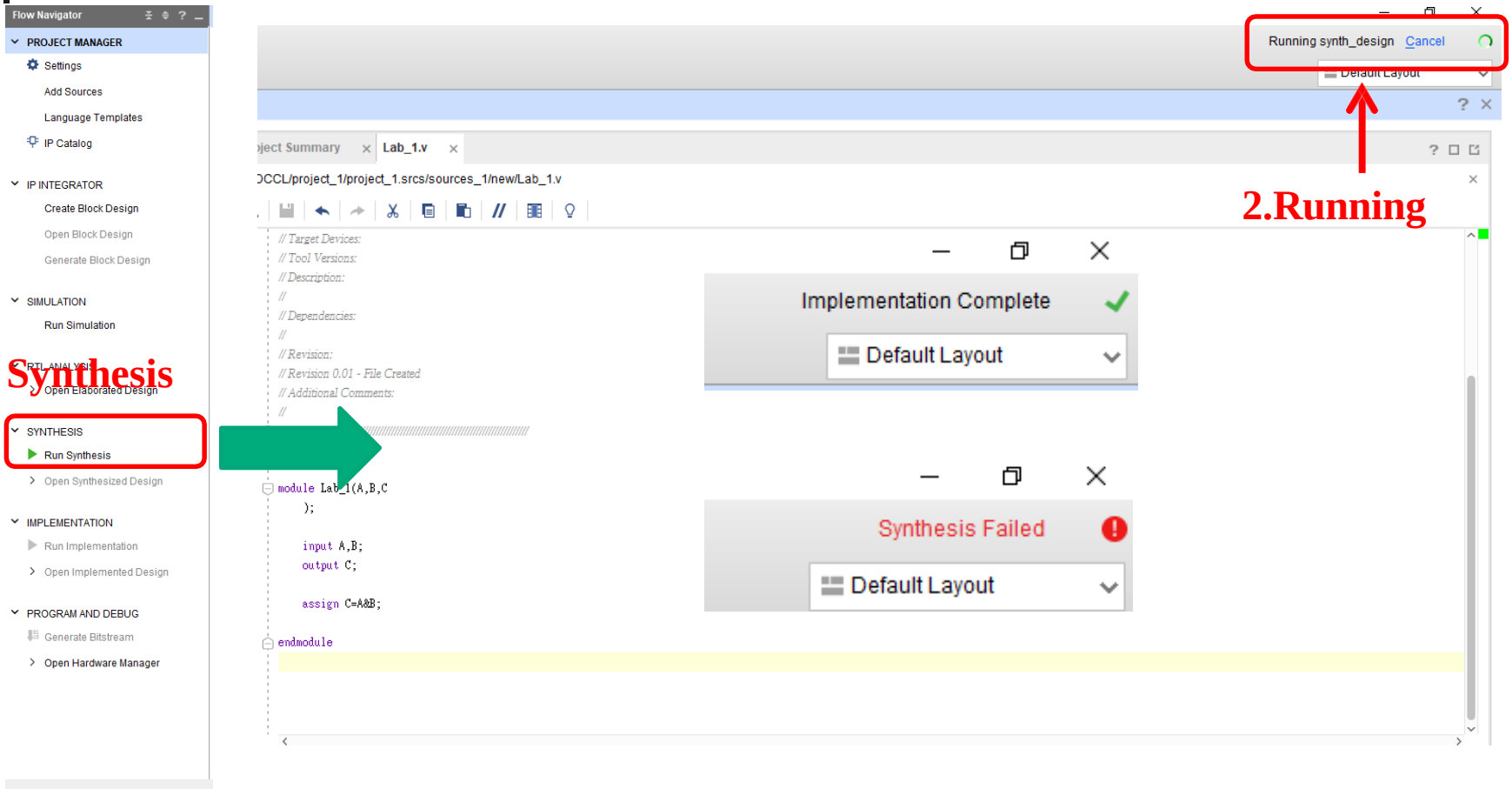


Example for TEST.V

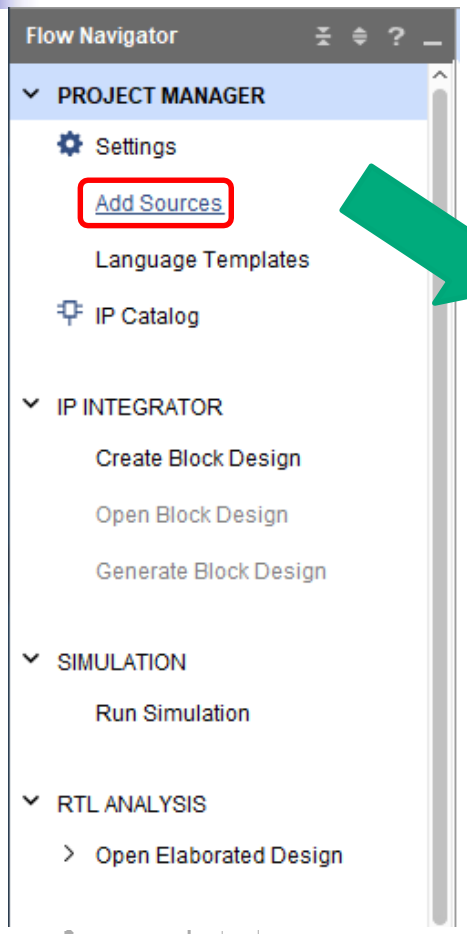
```
module TEST(A,B,C);
input A,B;
output C;
assign
C=A&B;
endmodule
```

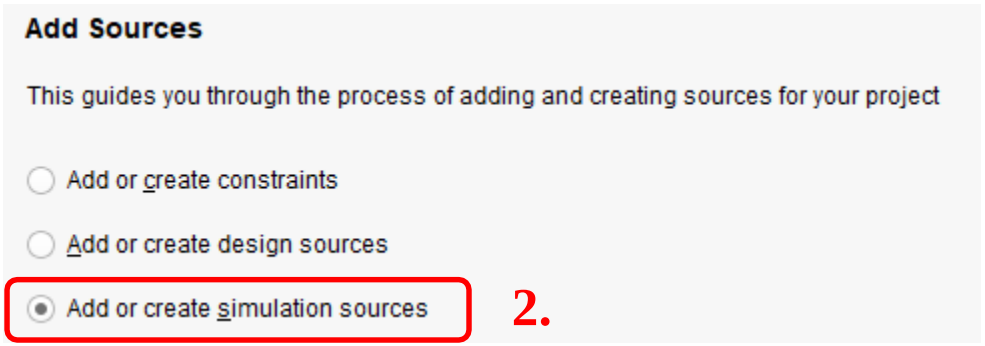
After complete TEST.V



Add TESTBENCH.V(1/2)

1. click





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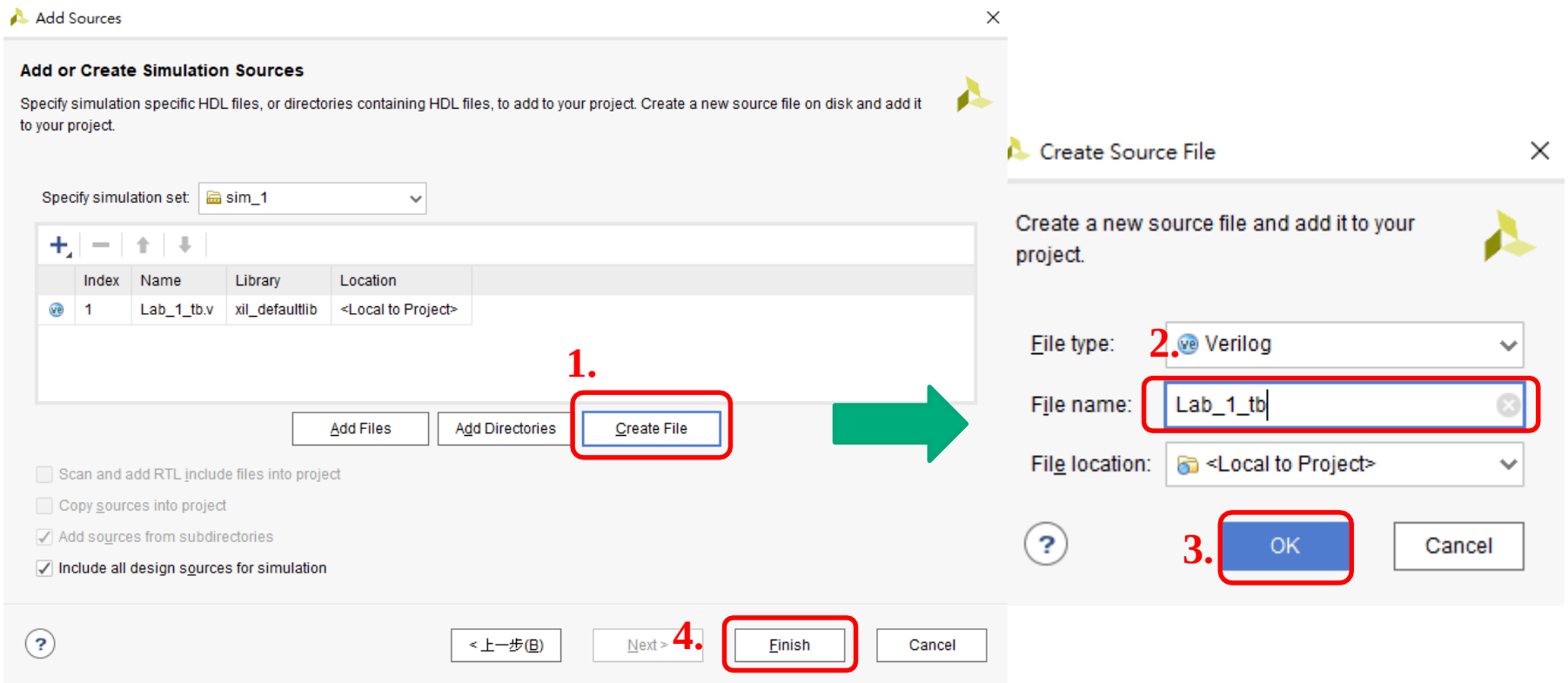
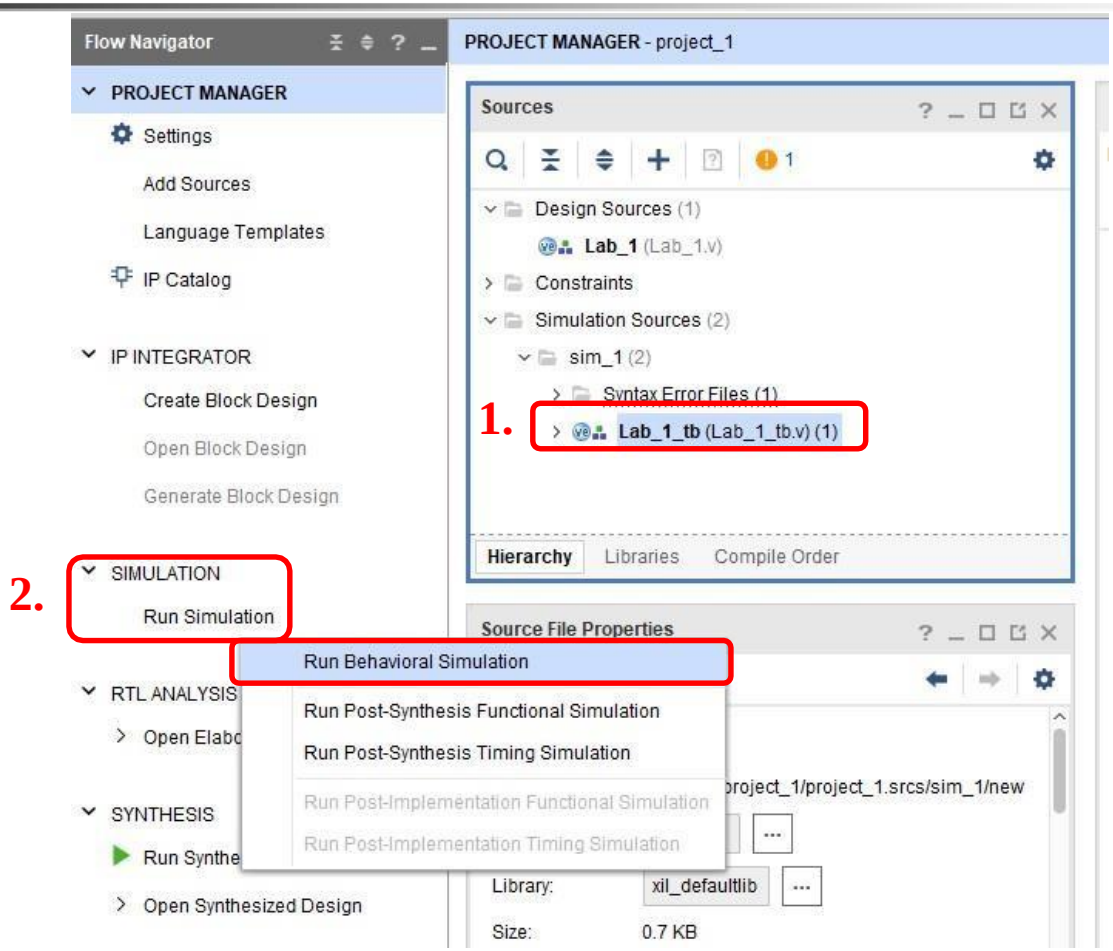


Run Behavioral Simulation



Example for TESTBENCH.V

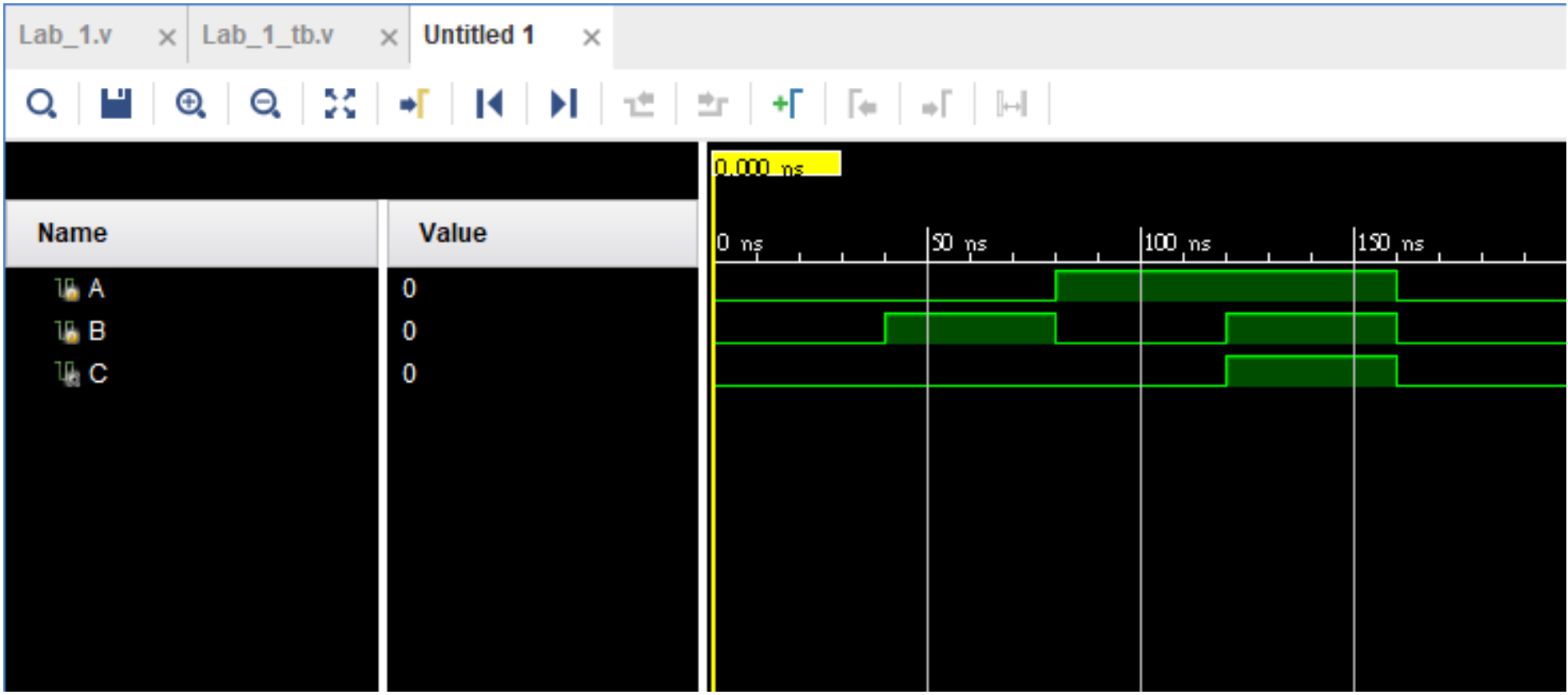
```
module testbench;
    // Inputs
    reg A;
    reg B;
    // Outputs
    wire C;
    // Instantiate the Unit Under Test (UUT)
    Lab_1 uut (
            .A(A),
            .B(B),
            .C(C)
            );
```

```
initial begin // Initialize Inputs
      A = 0; B = 0;
// Wait 100 ns for global reset to finish

// Add stimulus here
        A=0; B=0;
#40;    A=0; B=1;
#40;    A=1; B=0;
#40;    A=1; B=1;
#40;    A=0; B=0;
end

endmodule
```

Behavioral Simulation Result



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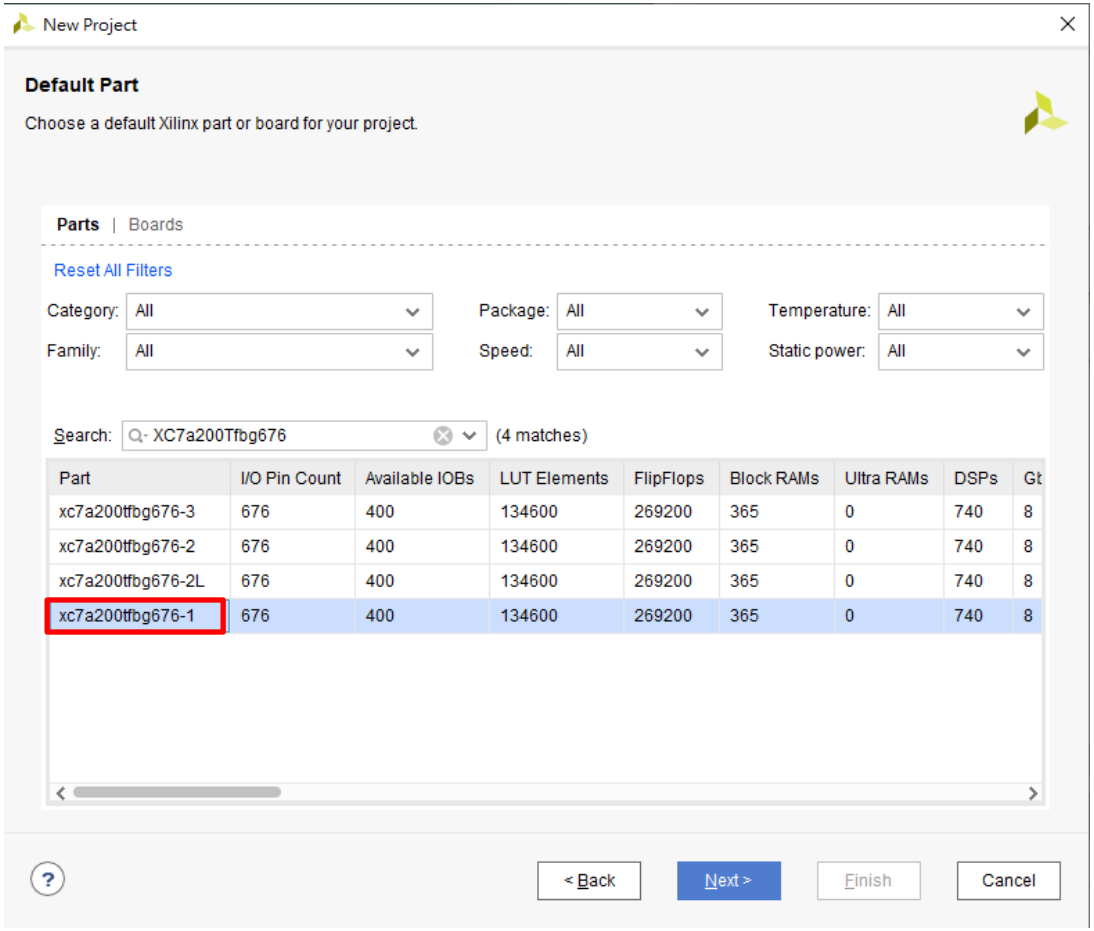
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