DCCDL LAB3

Verilog

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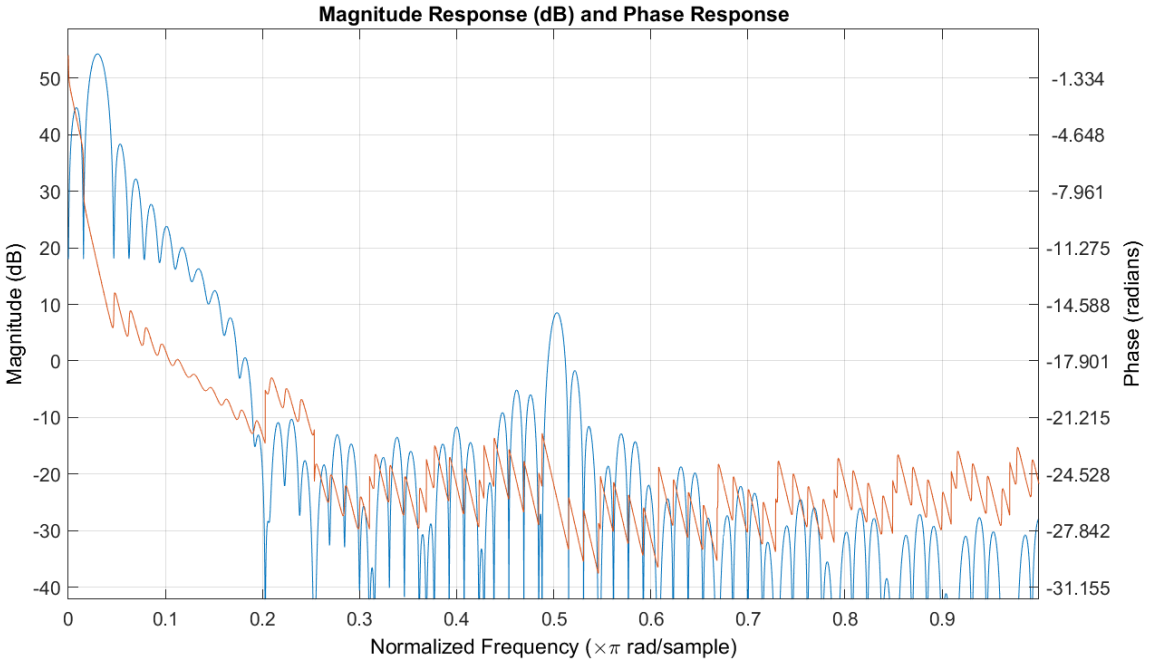
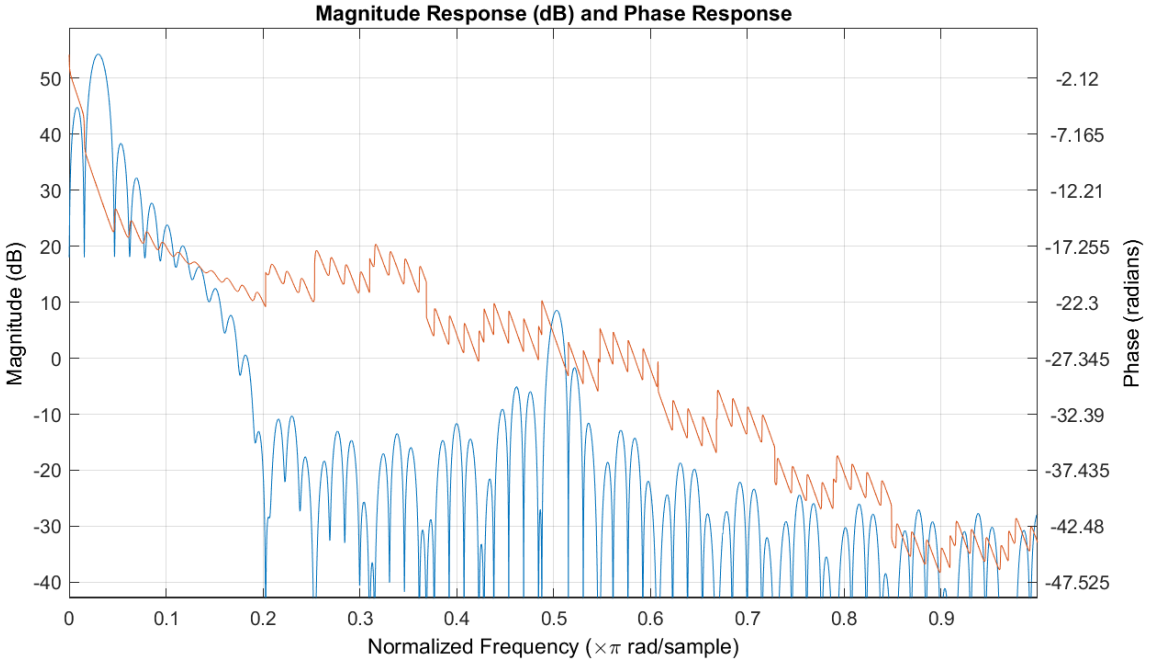
5. Compare the frequency-domain magnitude responses of ideal floating-point representation in 1 and fixed-point representation in 3 and 4. Please given some explanations about their performances. (20%)

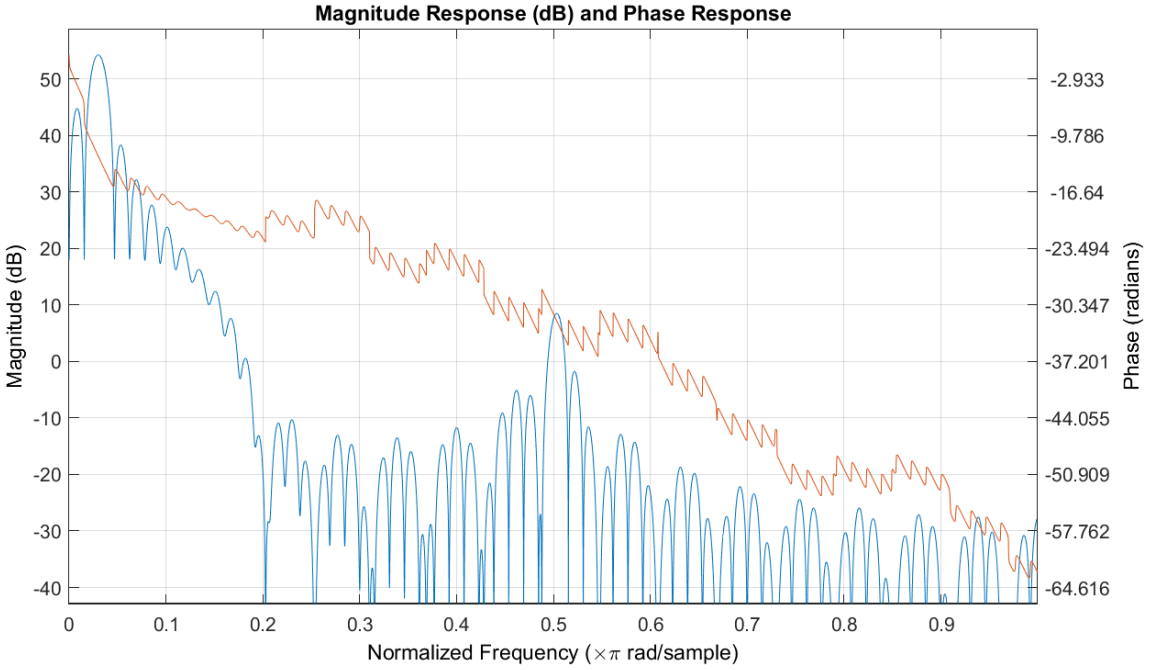
the frequency-domain magnitude response for floating-point:



The frequency-domain magnitude response for fixed-point direct-form FIR filter:



the frequency-domain magnitude response for fixed-point transposed-form FIR filter:

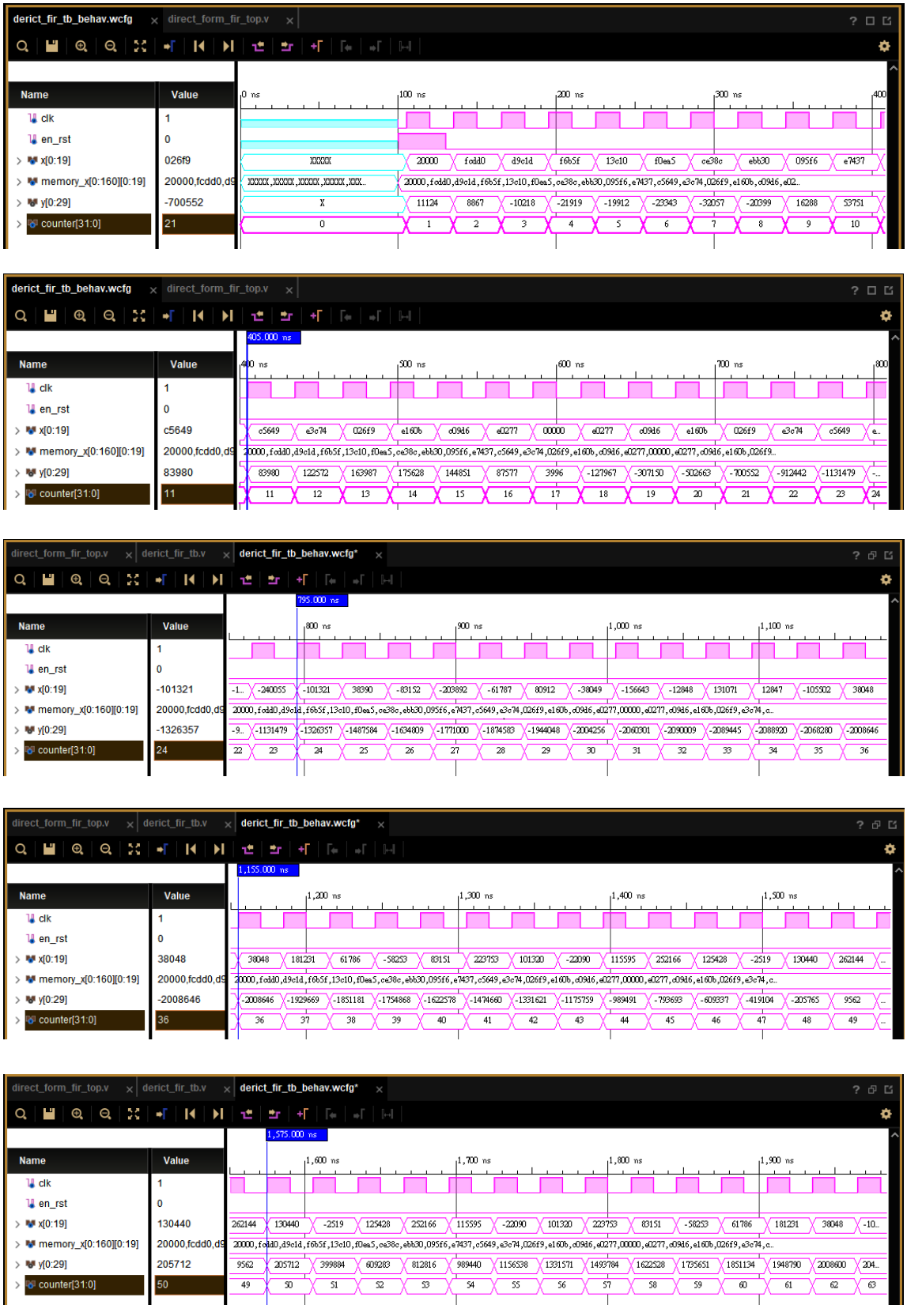


第一張圖為floating-point的frequency response。與direct form、transposed form的frequency response比較過後可以觀察到三者之間的magnitude並無太大的變化。

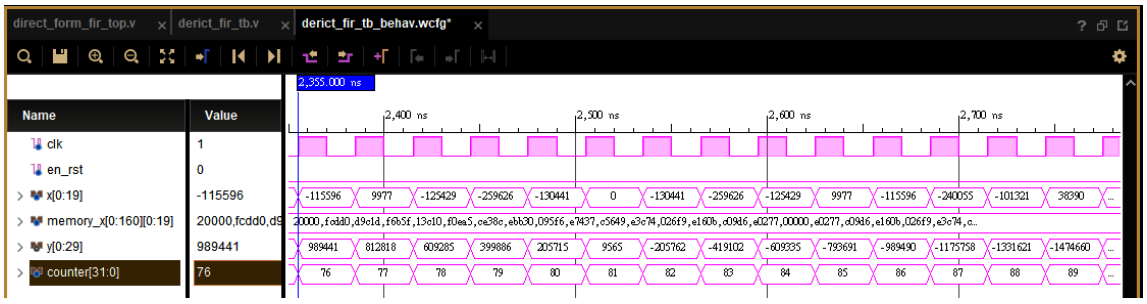
但是因為進行過truncation後其Phase出現了些微差距，隨著truncation之後的小數位越來越少，其與ideal的Phase差距越大。可以觀察到truncation之後的小數位越少其Phase變化的幅度越大。

6. Please implement the direct form FIR. Use $x[n]$ as the input. Check the behavior and post-route simulation results. Compare the results with the Matlab floating-point results. (30%)

Direct form behavior simulation:




direct_form_fir_top.v
derict_fir_tb.v
derict_fir_tb_behav.wcfg*
1,965.000 ns
Name
Value
clk
1
en_rst
0
x[0:19]
-105502
memory_x[0:160][0:19]
20000,fcdd0,d9c1d,f6b5f,13c10,f0ea5,ce38c,ebb30,095f6,e7437,c5649,e3c74,026f9,e160b,c0946,e0277,00000,e0277,c0946,e160b,026f9,e3c74,c...
y[0:29]
2049063
counter[31:0]
63
2,000 ns
2,100 ns
2,200 ns
2,300 ns
38... -105502 12847 131072 -12848 -156643 -38049 80912 -61787 -203892 -83152 38390 -101321 -240055 -115596
20... 2049063 2088872 2108569 2088873 2049064 2008600 1948790 1851134 1735651 1622528 1493784 1331571 1156539 989441
62 63 64 65 66 67 68 69 70 71 72 73 74 75 76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derict_fir_tb_behav.wcfg*
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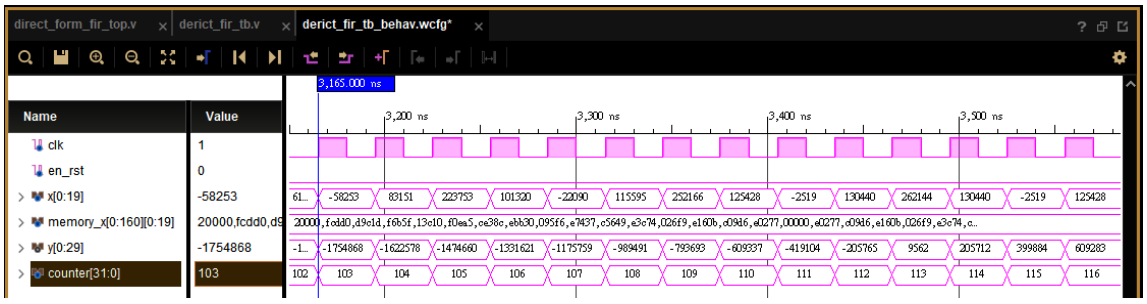
Name
Value
clk
1
en_rst
0
x[0:19]
-115596
memory_x[0:160][0:19]
20000,fcdd0,d9c1d,f6b5f,13c10,f0ea5,ce38c,ebb30,095f6,e7437,c5649,e3c74,026f9,e160b,c0946,e0277,00000,e0277,c0946,e160b,026f9,e3c74,c...
y[0:29]
989441
counter[31:0]
76
2,400 ns
2,500 ns
2,600 ns
2,700 ns
-115596 9977 -125429 -259626 -130441 0 -130441 -259626 -125429 9977 -115596 -240055 -101321 38390
989441 812818 609285 399886 205715 9565 -205762 -419102 -609335 -793691 -989490 -1175758 -1331621 -1474660
76 77 78 79 80 81 82 83 84 85 86 87 88 89


direct_form_fir_top.v
derict_fir_tb.v
derict_fir_tb_behav.wcfg*
2,775.000 ns
Name
Value
clk
1
en_rst
0
x[0:19]
-83152
memory_x[0:160][0:19]
20000,fcdd0,d9c1d,f6b5f,13c10,f0ea5,ce38c,ebb30,095f6,e7437,c5649,e3c74,026f9,e160b,c0946,e0277,00000,e0277,c0946,e160b,026f9,e3c74,c...
y[0:29]
-1622578
counter[31:0]
90
2,800 ns
2,900 ns
3,000 ns
3,100 ns
38390 -83152 -203892 -61787 80912 -38049 -156643 -12848 131071 12847 -105502 38048 181231 61786
-1474... -1622578 -1754868 -1851181 -1929669 -2008646 -2068279 -2088919 -2089445 -2088920 -2068280 -2008646 -1929669 -1851181
89 90 91 92 93 94 95 96 97 98 99 100 101 102 103


direct_form_fir_top.v
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derict_fir_tb_behav.wcfg*
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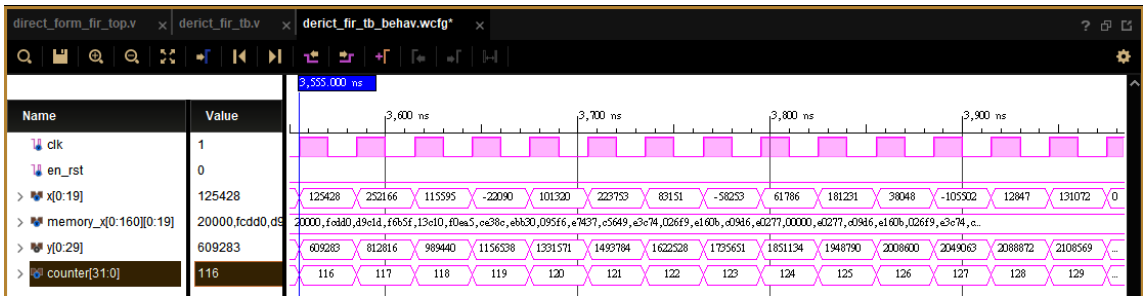
Name
Value
clk
1
en_rst
0
x[0:19]
-58253
memory_x[0:160][0:19]
20000,fcdd0,d9c1d,f6b5f,13c10,f0ea5,ce38c,ebb30,095f6,e7437,c5649,e3c74,026f9,e160b,c0946,e0277,00000,e0277,c0946,e160b,026f9,e3c74,c...
y[0:29]
-1754868
counter[31:0]
103
3,200 ns
3,300 ns
3,400 ns
3,500 ns
61... -58253 83151 223753 101320 -22090 115595 252166 125428 -2519 130440 262144 130440 -2519 125428
-1... -1754868 -1622578 -1474660 -1331621 -1175759 -989491 -793693 -609337 -419104 -205765 9562 205712 399884 609283
102 103 104 105 106 107 108 109 110 111 112 113 114 115 116


direct_form_fir_top.v
derict_fir_tb.v
derict_fir_tb_behav.wcfg*
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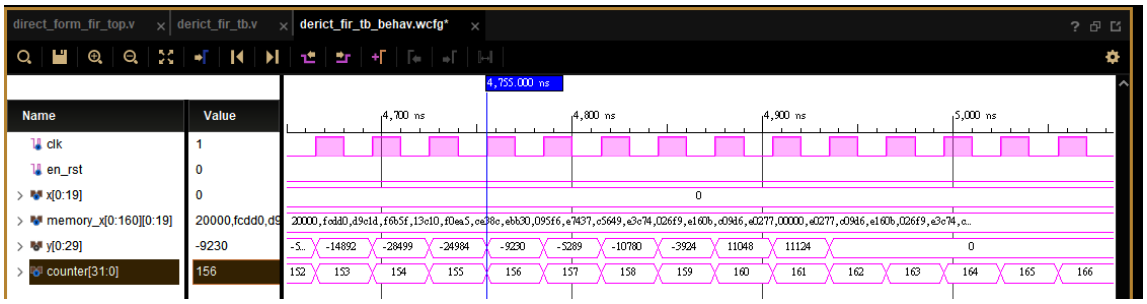
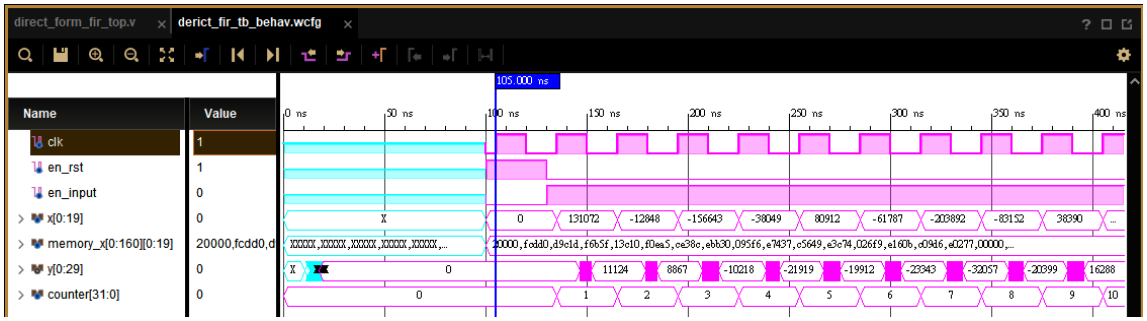
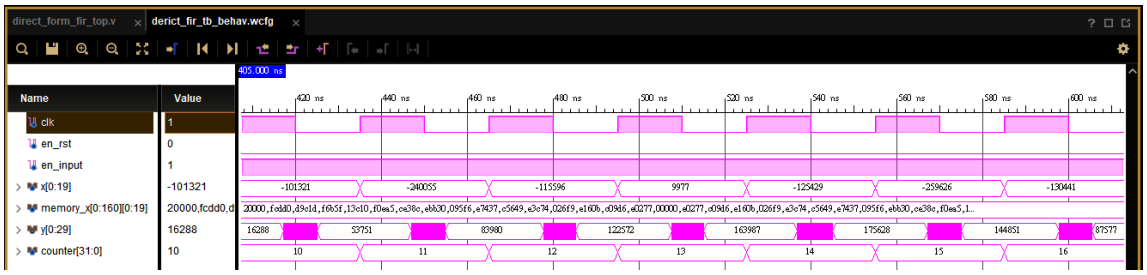
Name
Value
clk
1
en_rst
0
x[0:19]
125428
memory_x[0:160][0:19]
20000,fcdd0,d9c1d,f6b5f,13c10,f0ea5,ce38c,ebb30,095f6,e7437,c5649,e3c74,026f9,e160b,c0946,e0277,00000,e0277,c0946,e160b,026f9,e3c74,c...
y[0:29]
609283
counter[31:0]
116
3,600 ns
3,700 ns
3,800 ns
3,900 ns
125428 252166 115595 -22090 101320 223753 83151 -58253 61786 181231 38048 -105502 12847 131072 0
609283 812816 989440 1156538 1331571 1493784 1622528 1735651 1851134 1948790 2008600 2049063 2088872 2108569
116 117 118 119 120 121 122 123 124 125 126 127 128 129

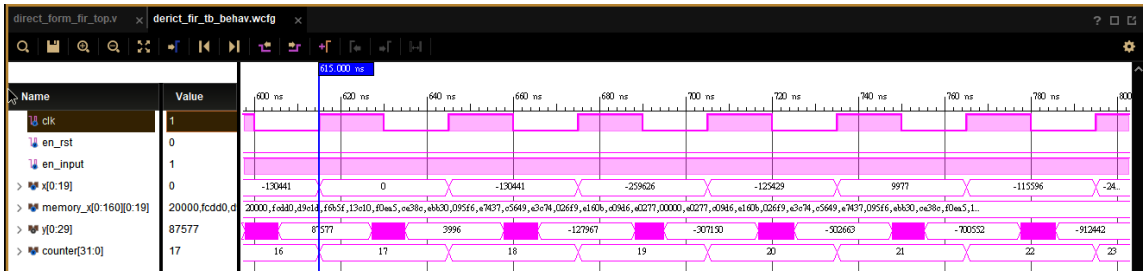


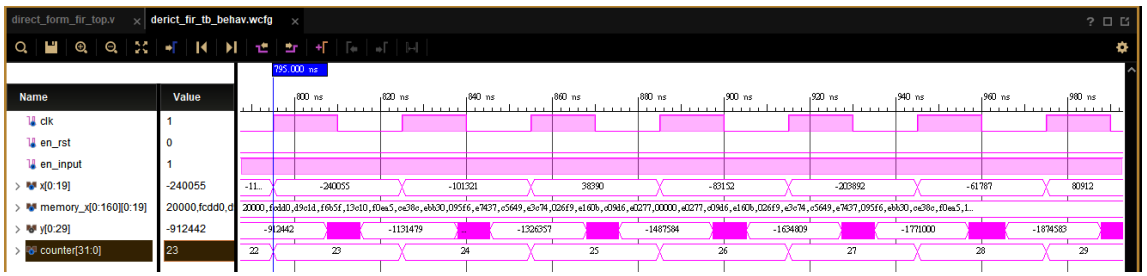

```
vivado3_y = [11124  8867    -10218  -21919  -19912  -23343  -32057  -20399
             16288   53751   83980   122572  163987  175628  144851  87577
             3996    -127967 -307150 -502663 -700552 -912442 -1131479
             -1326357    -1487584    -1634809    -1771000    -1874583
             -1944048    -2004256    -206301 -2090009    -2089445
             -2088920    -2068280    -2008646    -1929669    -1851181
             -1754868    -1622578    -1474660    -1331621    -1175759
             -989491 -793693 -609337 -419104 -205765 9562    205712
             399884  609283  812816  989440  1156538 1331571 1493784
             1622528 1735651 1851134 1948790 2008600 2049063 2088872
             2108569 2088873 2049064 2008600 1948790 1851134 1735651
             1622528 1493784 1331571 1156539 989441  812818  609285
             399886  205715  9565    -205762 -419102 -609335 -793691
             -989490 -1175758    -1331621    -1474660    -1622578
             -1754868    -1851181    -1929669    -2008646    -2068279
             -2088919    -2089445    -2088920    -2068280    -2008646
             -1929669    -1851181    -1754868    -1622578    -1474660
             -1331621    -1175759    -989491 -793693 -609337 -419104
             -205765 9562    205712  399884  609283  812816  989440
             1156538 1331571 1493784 1622528 1735651 1851134 1948790
             2008600 2049063 2088872 2108569 2089964 2063336 2024129
             1949034 1841845 1726592 1602197 1449680 1277424 1113673
             960505  800515  641803  510493  405062  303527  209129
             143506  101474  58545   16588   -3165   -5660   -14892
             -28499  -24984  -9230   -5289   -10780  -3924   11048   11124];
```

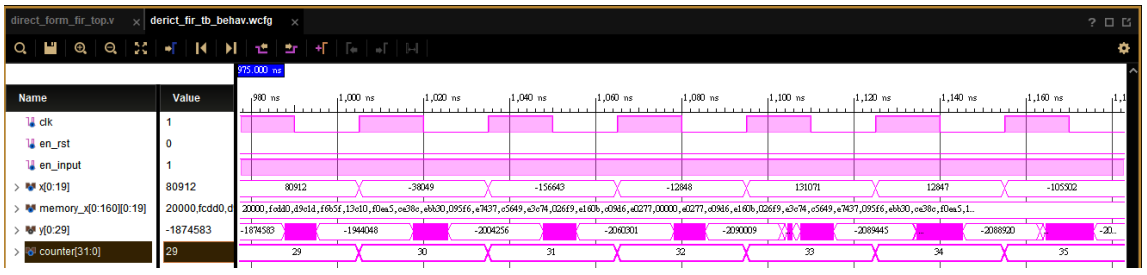
Post-Synthesis timing simulation:

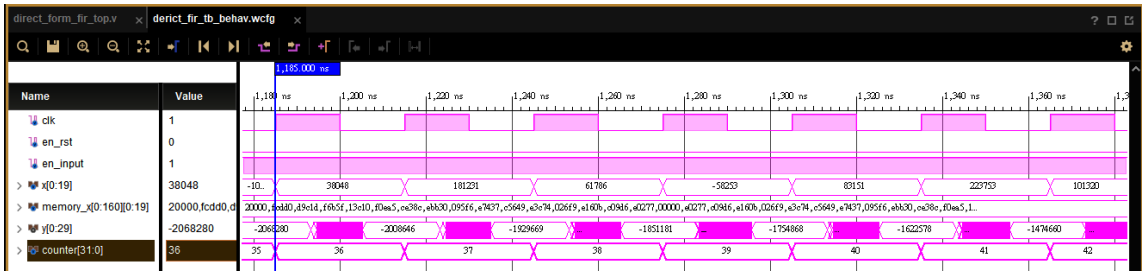


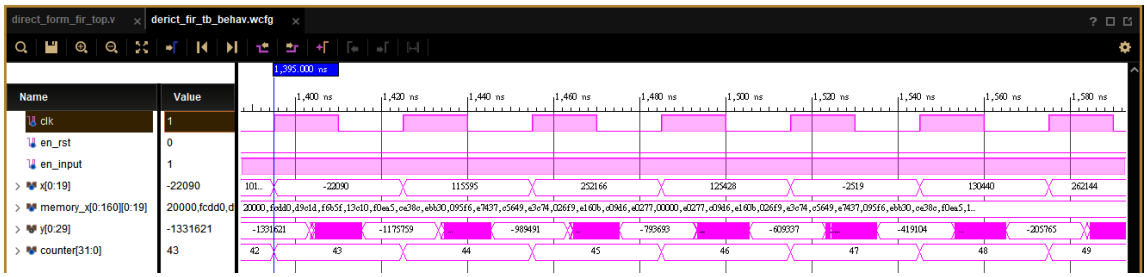


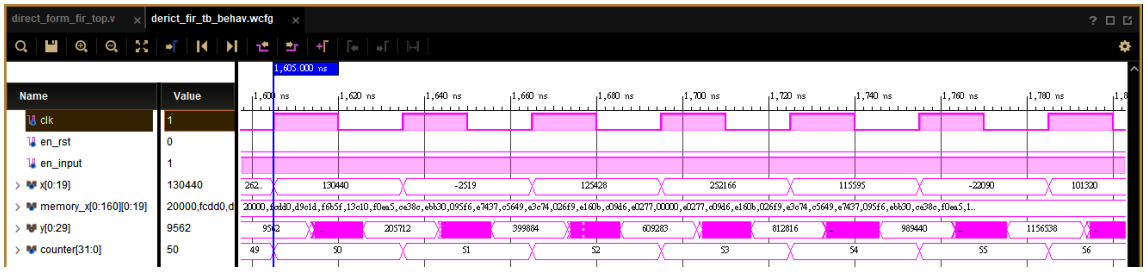









direct_form_fir_top.v
derict_fir_tb_behav.wcfg
1,395.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
-22090
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
-1331621
counter[31:0]
43


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
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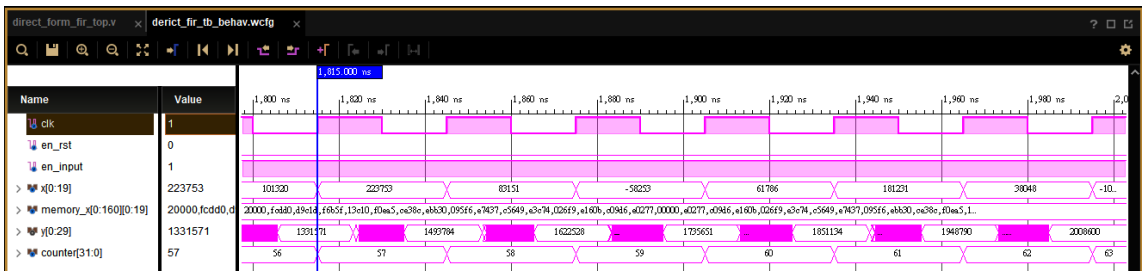
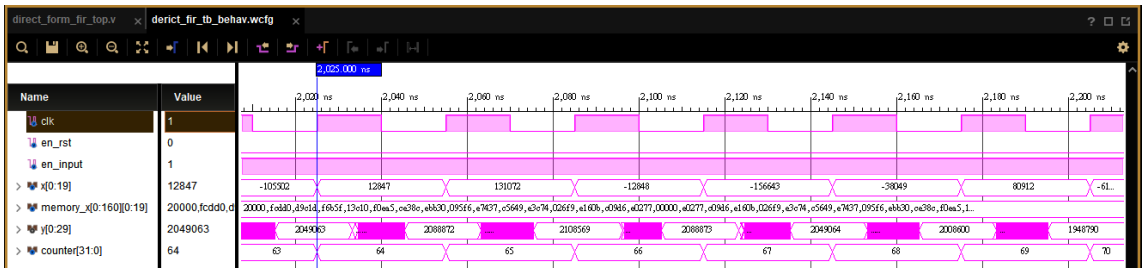
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
130440
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
9562
counter[31:0]
50


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
1,815.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
223753
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
1331571
counter[31:0]
57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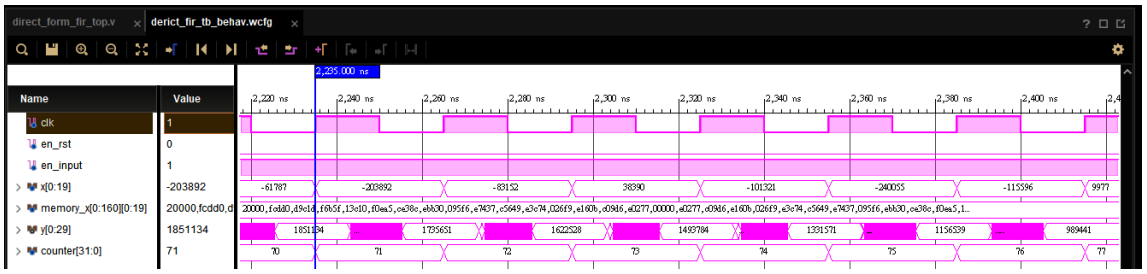
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
12847
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
2049063
counter[31:0]
64


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
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Value
clk
1
en_rst
0
en_input
1
x[0:19]
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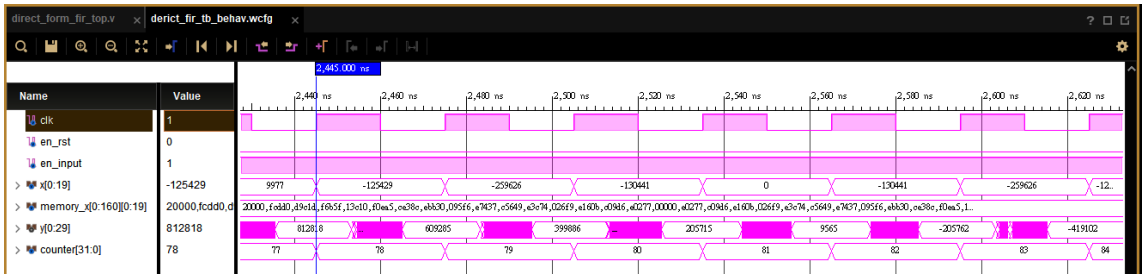
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
1851134
counter[31:0]
71


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,445.000 ns
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Value
clk
1
en_rst
0
en_input
1
x[0:19]
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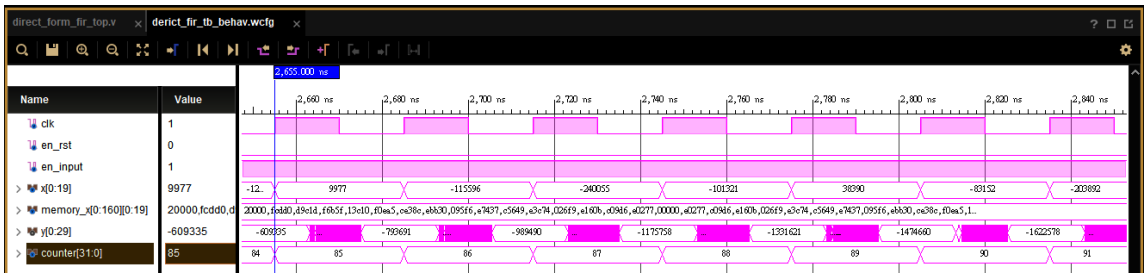
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
812818
counter[31:0]
78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Value
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en_rst 0
en_input 1
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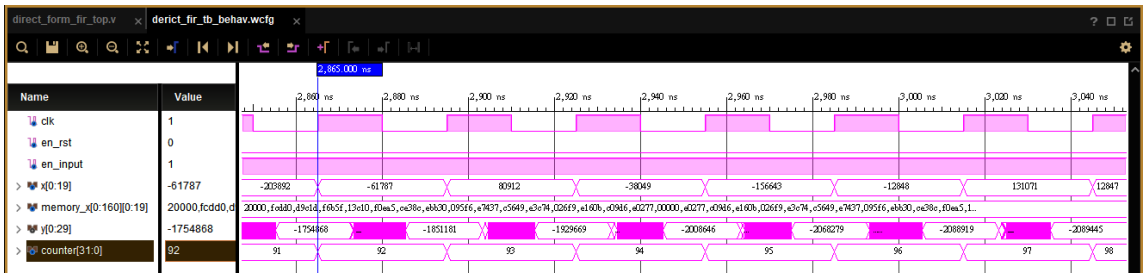
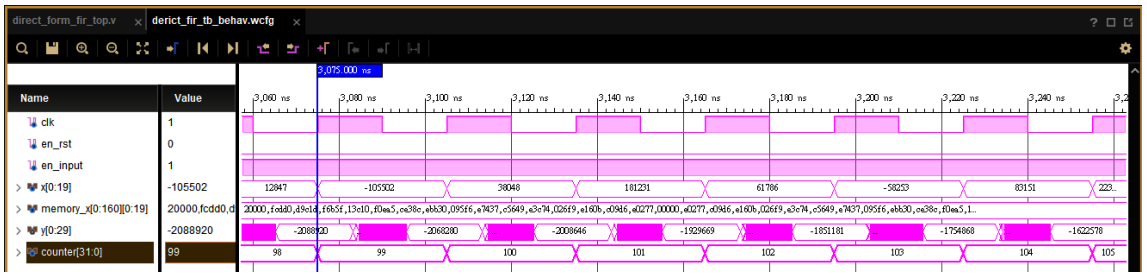
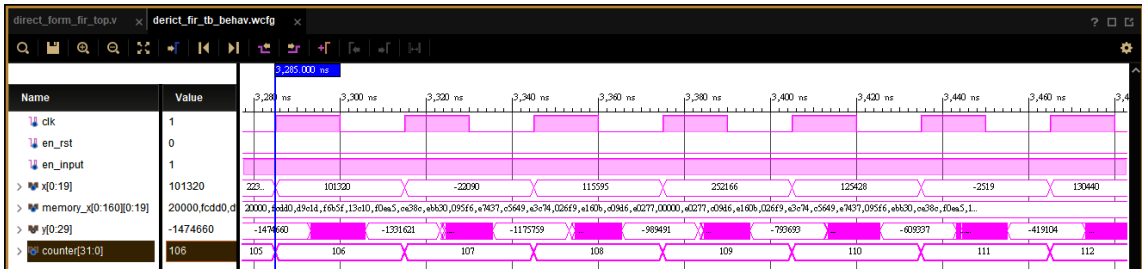
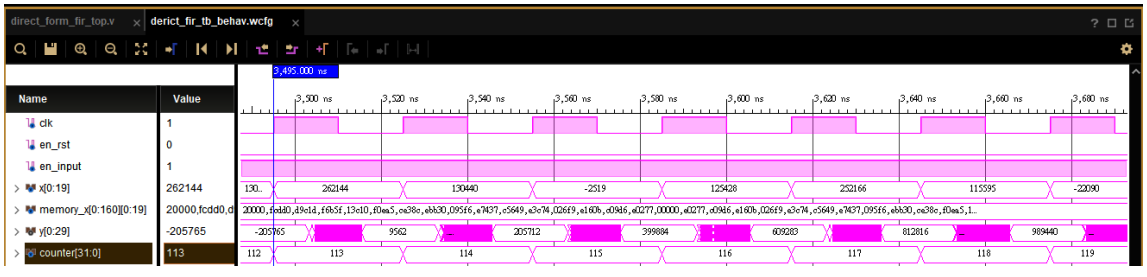
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -609335
counter[31:0] 85


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,865.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] -61787
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -1754868
counter[31:0] 92


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,075.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] -105502
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -2088920
counter[31:0] 99


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,285.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 101320
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -1474660
counter[31:0] 106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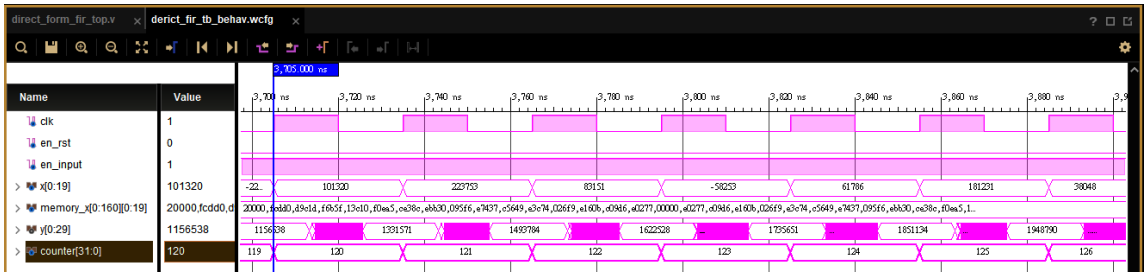
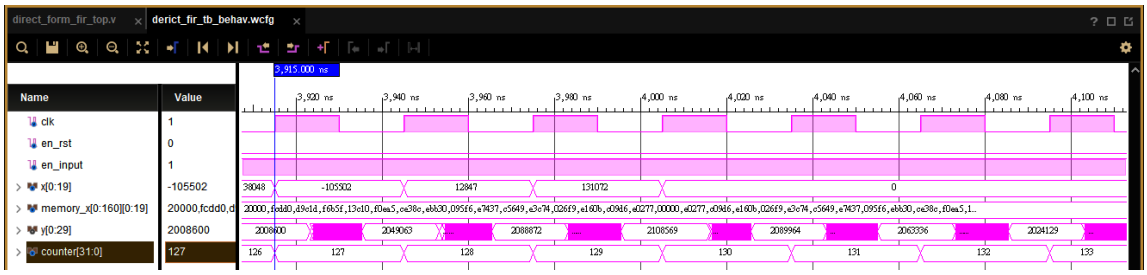
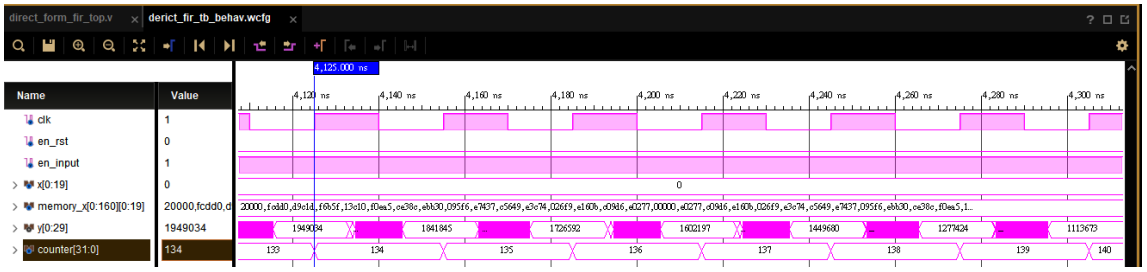
derict_fir_tb_behav.wcfg
3,495.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 262144
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -205765
counter[31:0] 113


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,705.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 101320
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] 1156538
counter[31:0] 120


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
-105502
20000,fcdd0,d
2008600
127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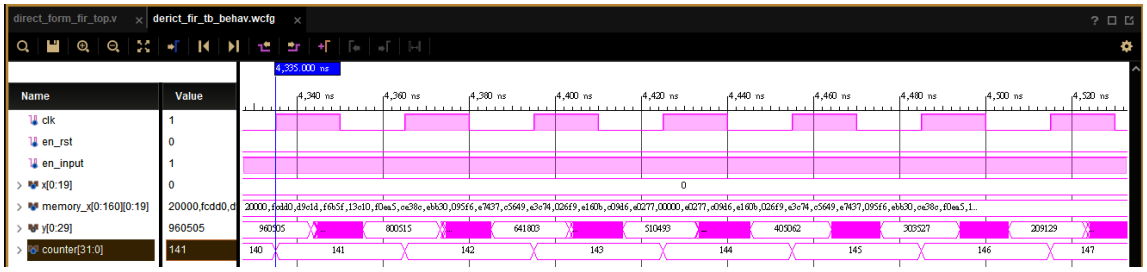
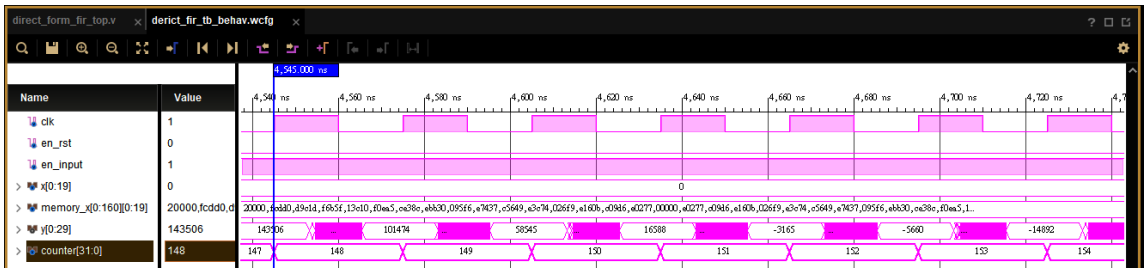
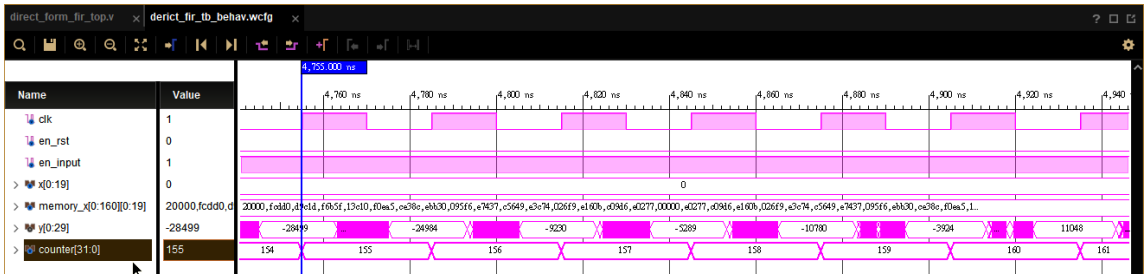
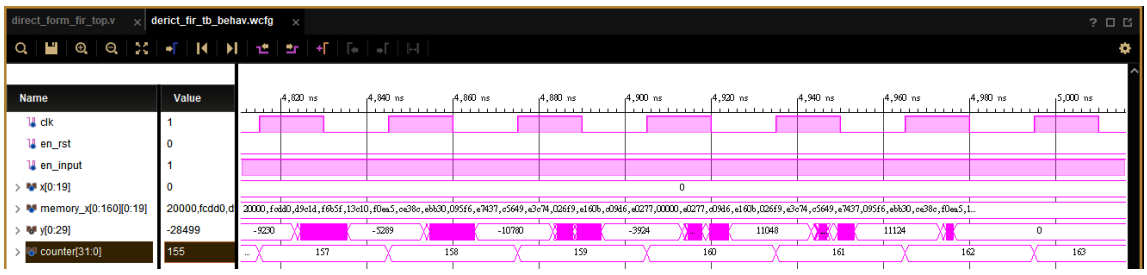
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
1949034
134

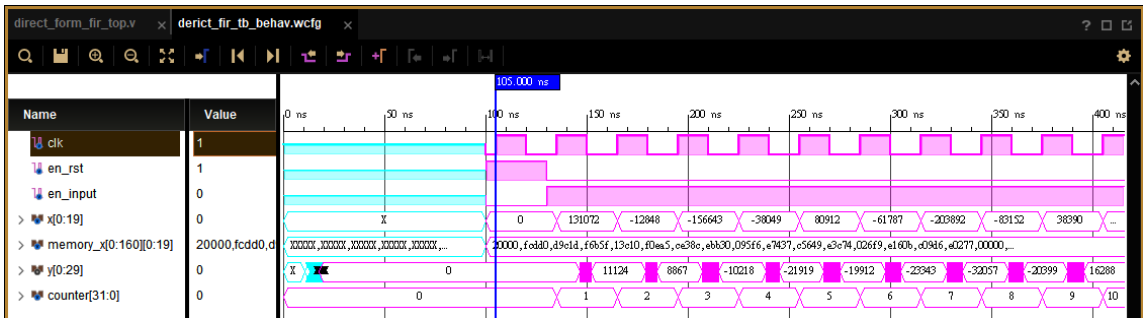

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
960505
141

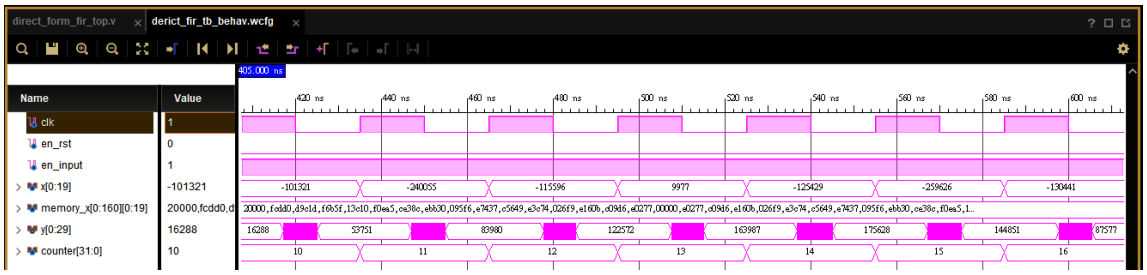

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
143506
148

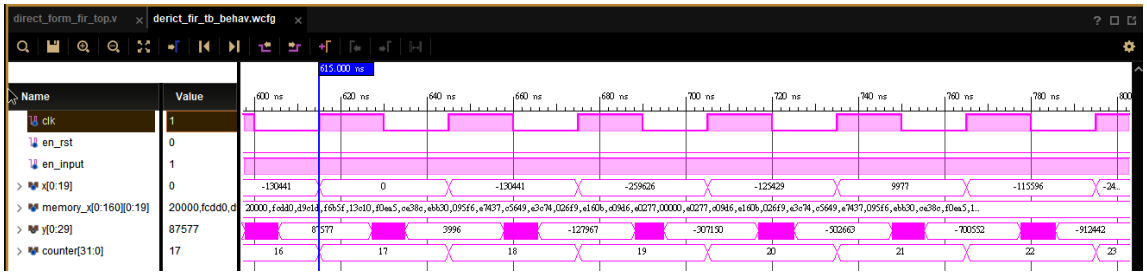

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
-28499
155

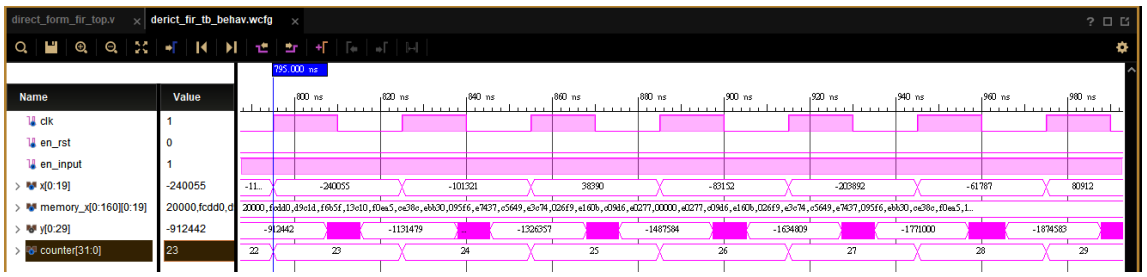

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
-28499
155

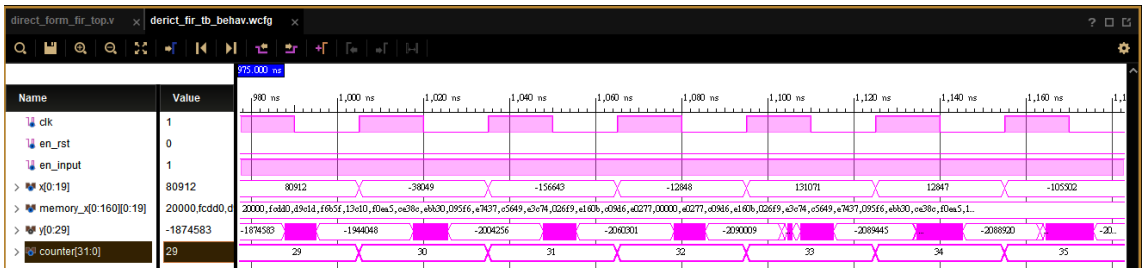
Post-implementation timing simulation:

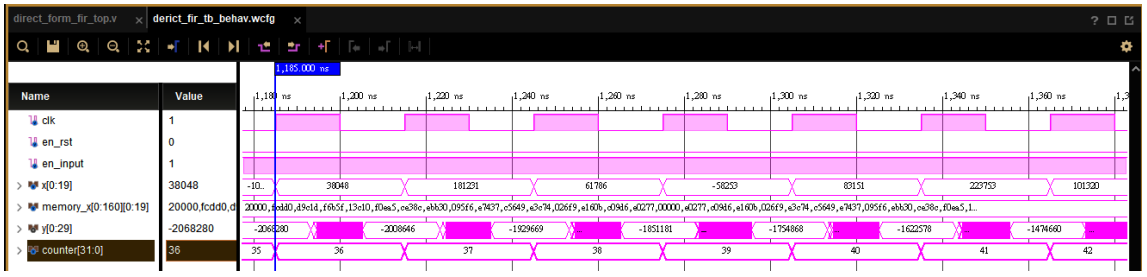


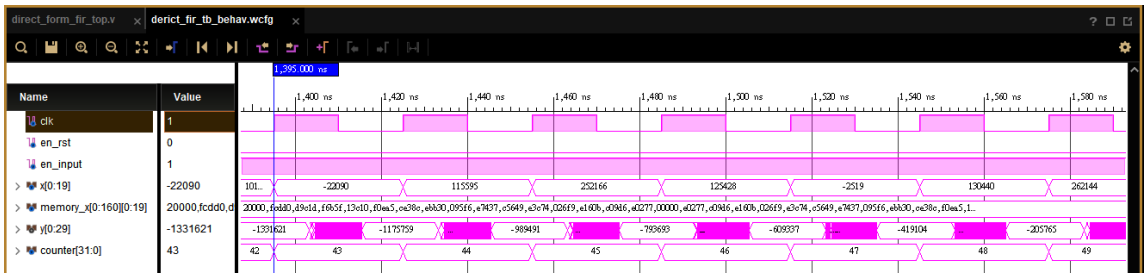


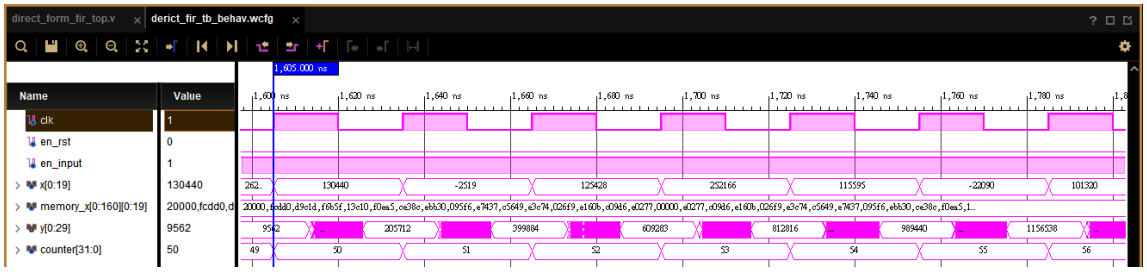


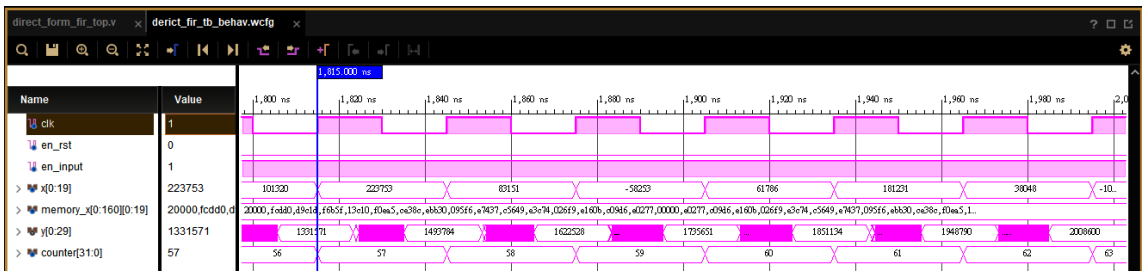


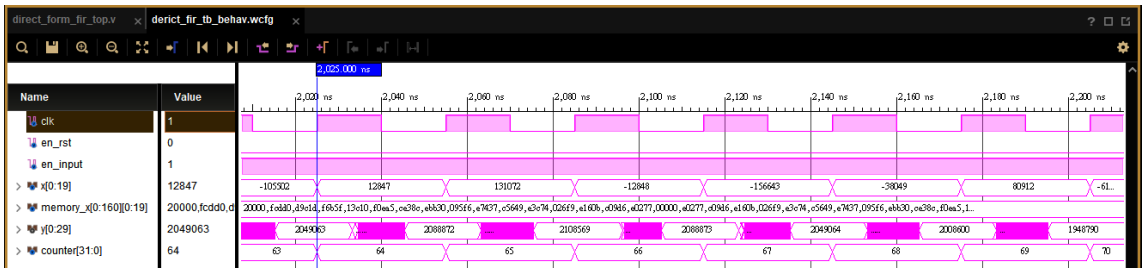


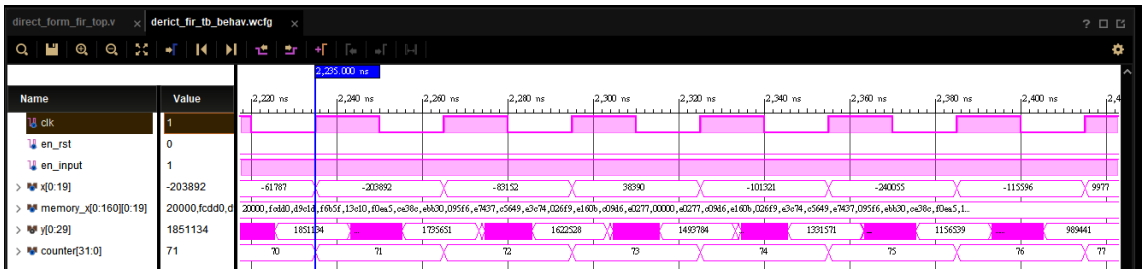


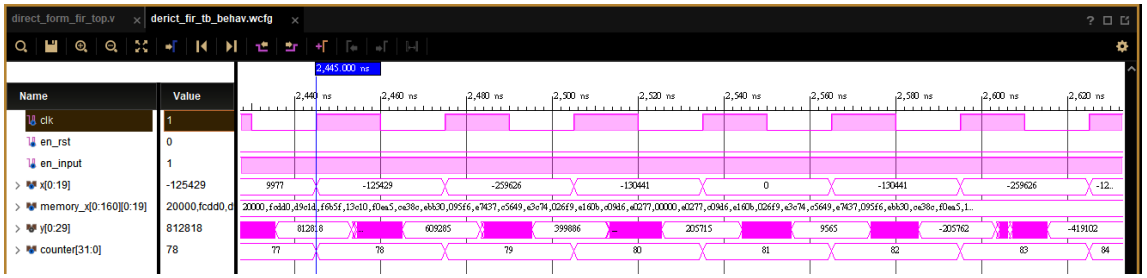

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
1,395.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
-22090
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
-1331621
counter[31:0]
43

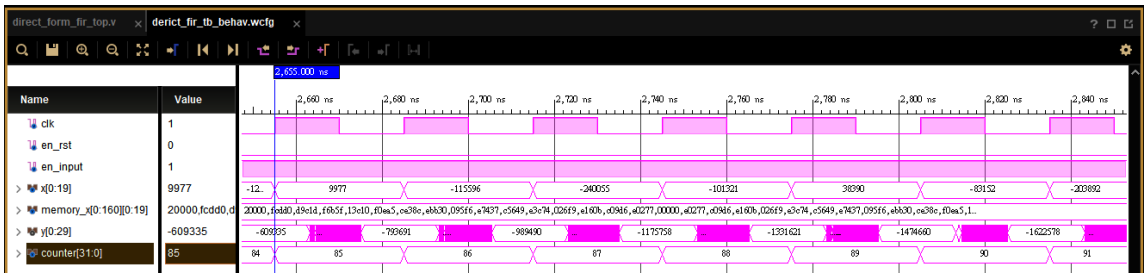

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
1,605.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
130440
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
9562
counter[31:0]
50

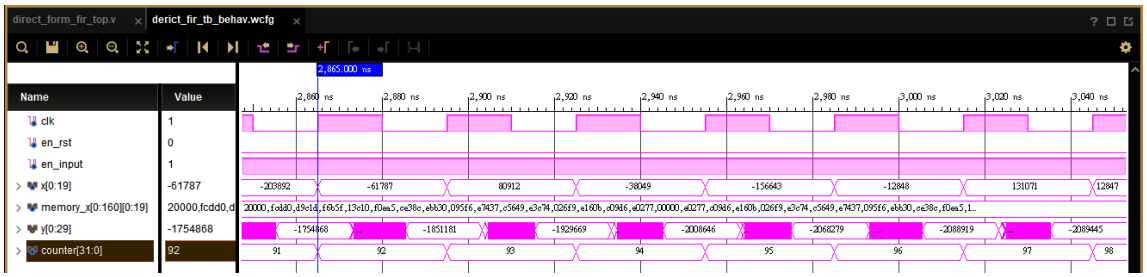

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
1,815.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
223753
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
1331571
counter[31:0]
57

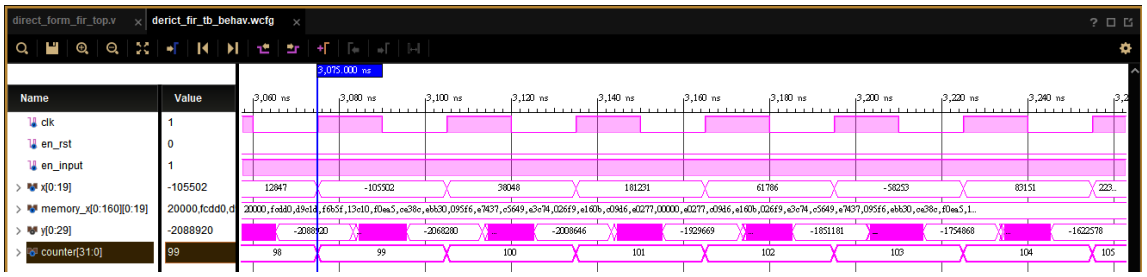

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,025.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
12847
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
2049063
counter[31:0]
64

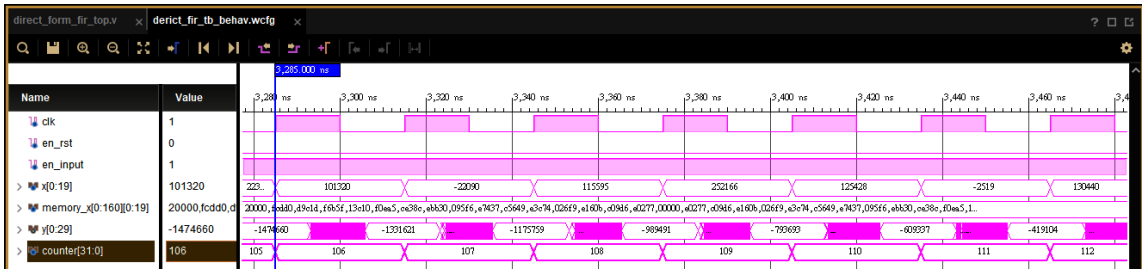

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,295.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
-203892
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
1851134
counter[31:0]
71

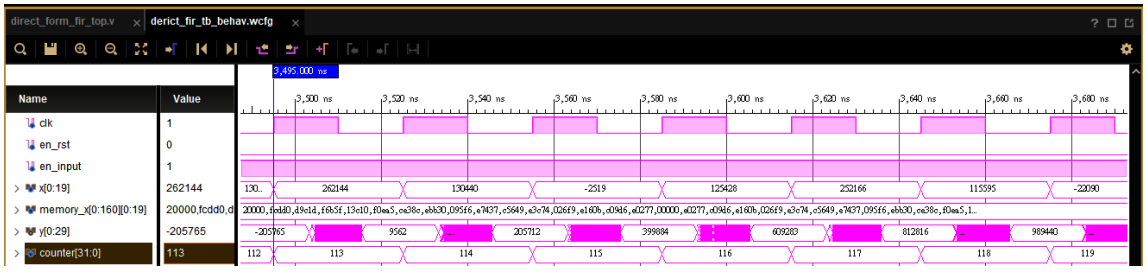

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,445.000 ns
Name
Value
clk
1
en_rst
0
en_input
1
x[0:19]
-125429
memory_x[0:160][0:19]
20000,fcdd0,d
y[0:29]
812818
counter[31:0]
78

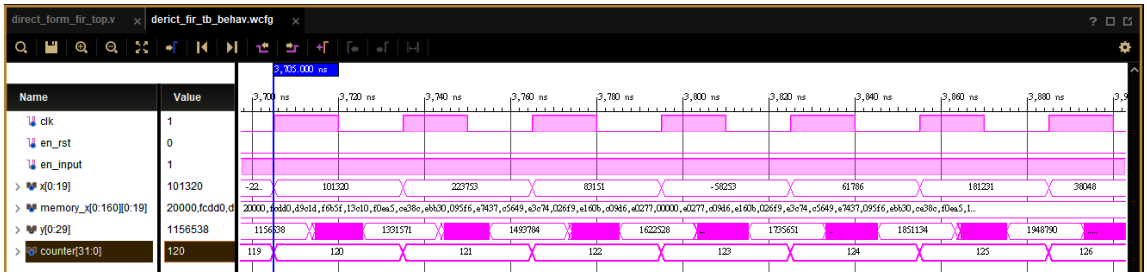

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,655.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 9977
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -609335
counter[31:0] 85

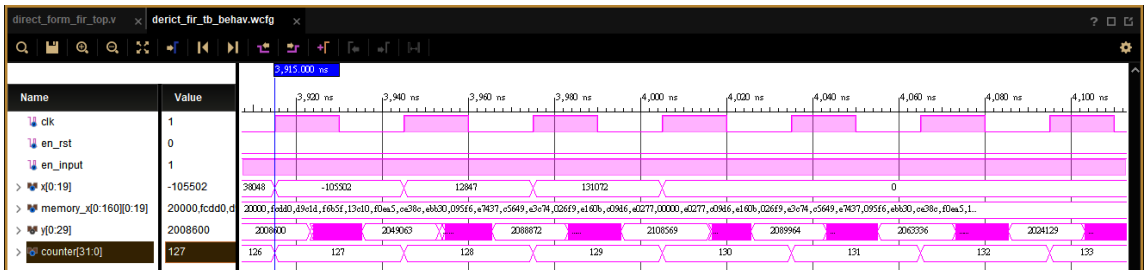

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
2,865.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] -61787
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -1754868
counter[31:0] 92

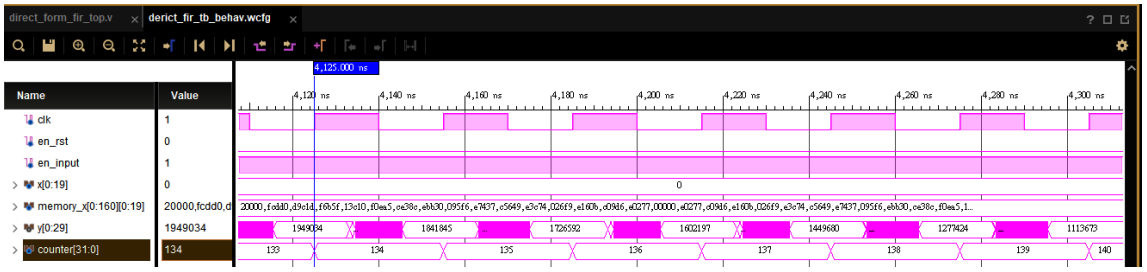

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,075.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] -105502
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -2088920
counter[31:0] 99

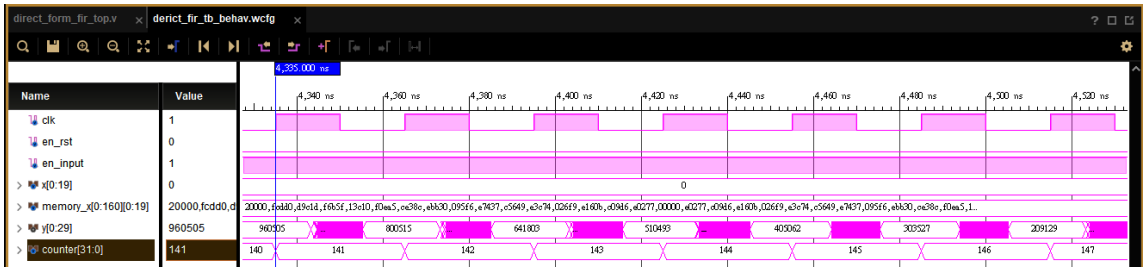

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,285.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 101320
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -1474660
counter[31:0] 106

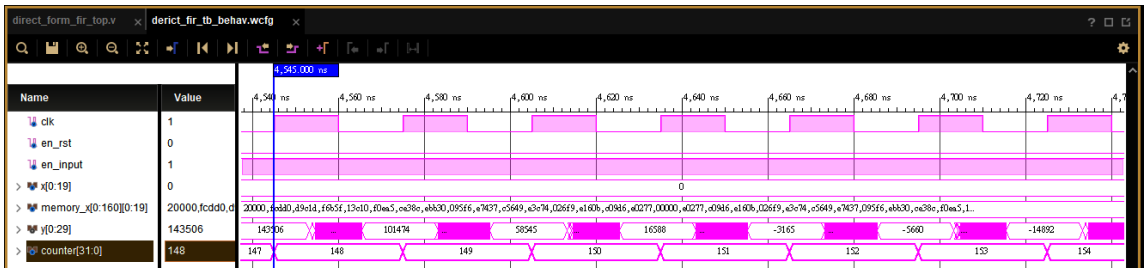

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,495.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 262144
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] -205765
counter[31:0] 113

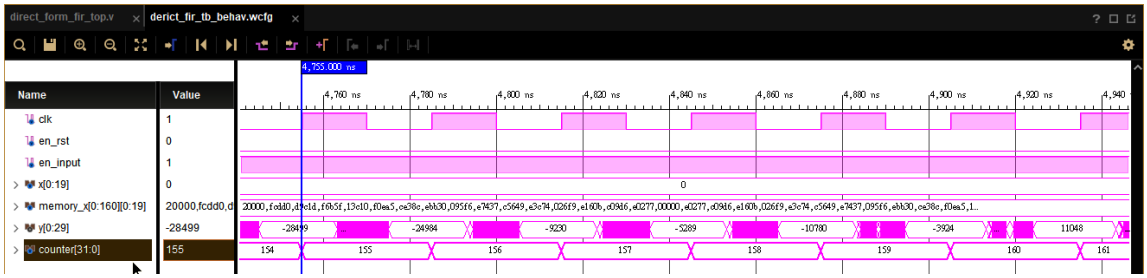

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
3,705.000 ns
Name
Value
clk 1
en_rst 0
en_input 1
x[0:19] 101320
memory_x[0:160][0:19] 20000,fcdd0,d
y[0:29] 1156538
counter[31:0] 120

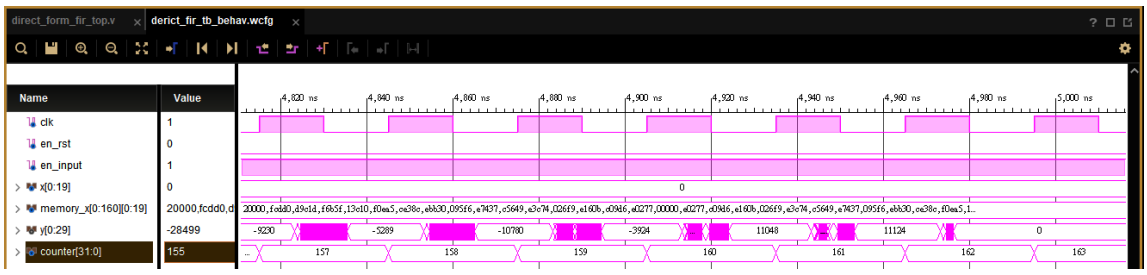

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
-105502
20000,fcdd0,d
2008600
127


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
1949034
134

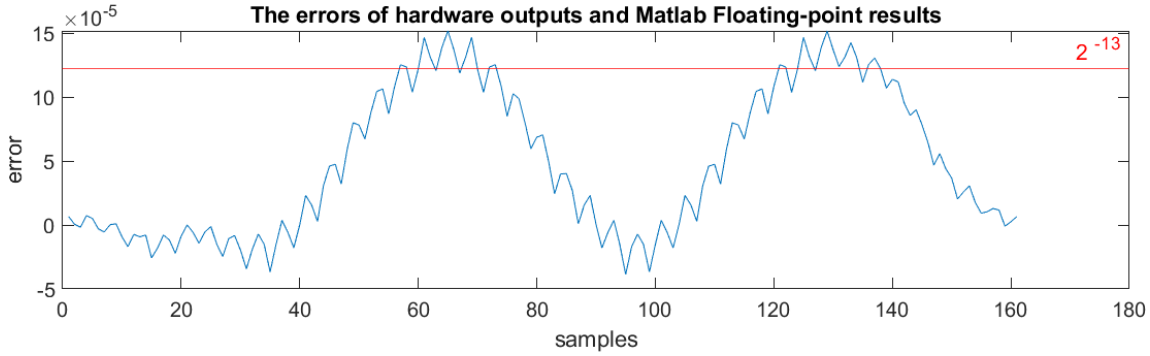

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
960505
141


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
143506
148


direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
-28499
155

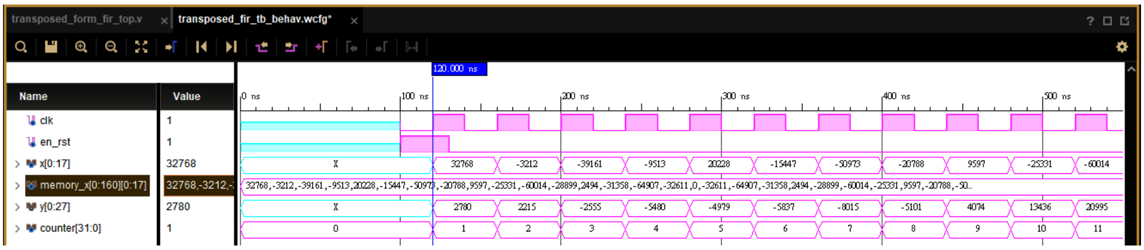

direct_form_fir_top.v
derict_fir_tb_behav.wcfg
Name
Value
clk
en_rst
en_input
x[0:19]
memory_x[0:160][0:19]
y[0:29]
counter[31:0]
1
0
1
0
20000,fcdd0,d
-28499
155

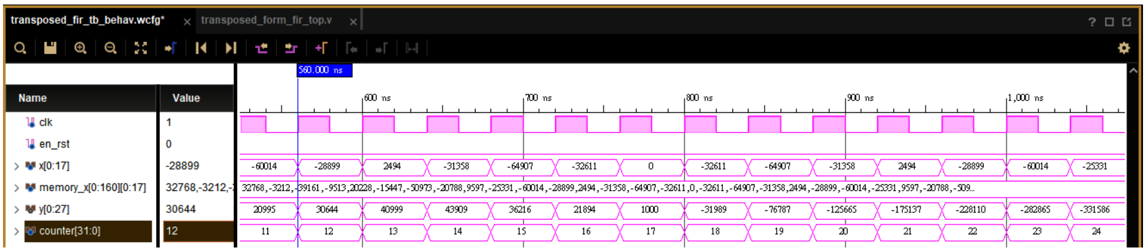
Show the errors of hardware outputs and Matlab floating-point results of direct from FIR by Matlab figures.

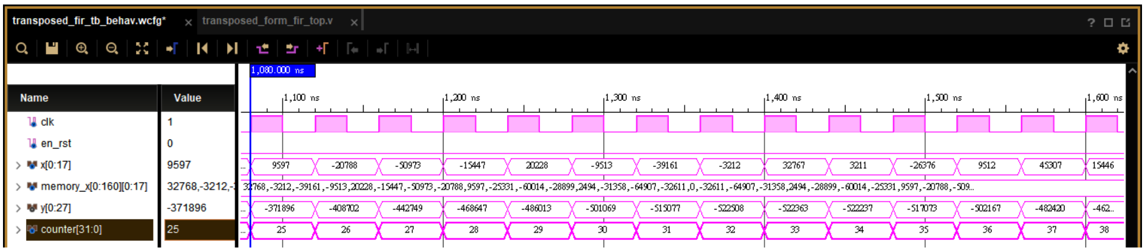


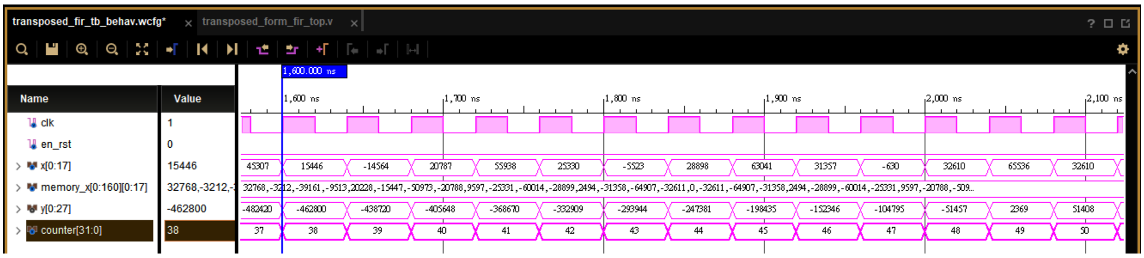
7. Please implement the transposed form. Note that modularity and parametric design can ease your loading. Use $x[n]$ as the input. Check the behavior and post-route simulation results. Compare the results with the Matlab floating-point results. (30%)

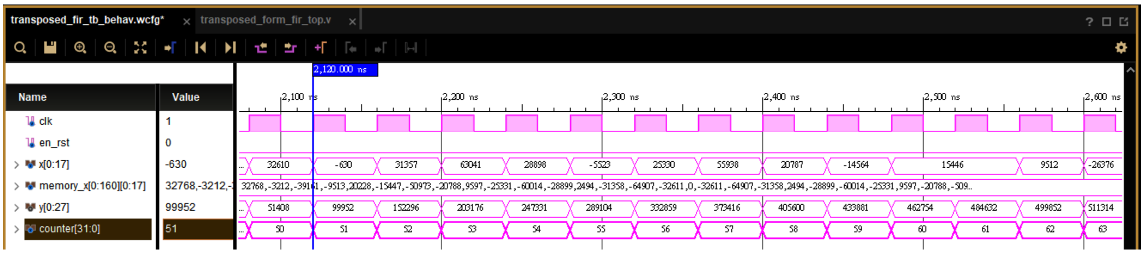
Behavior simulation:

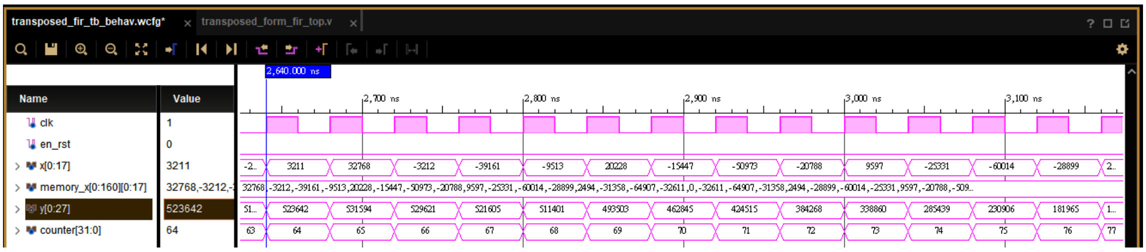


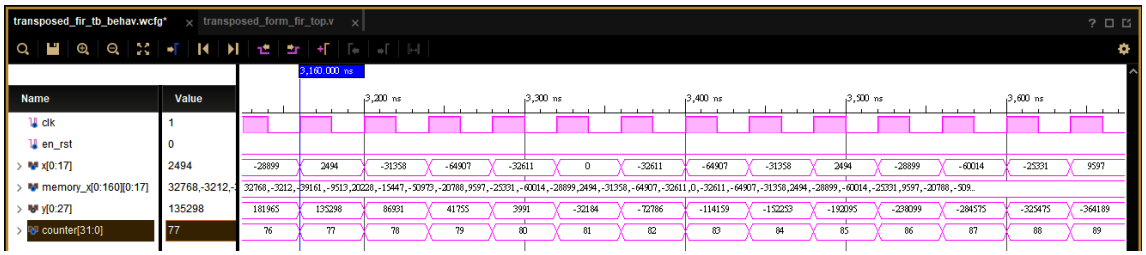


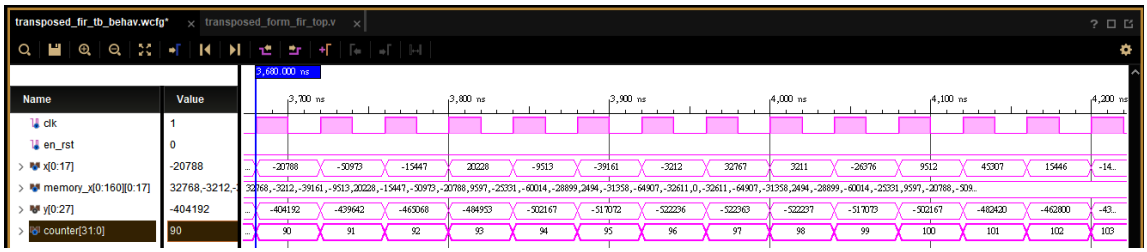


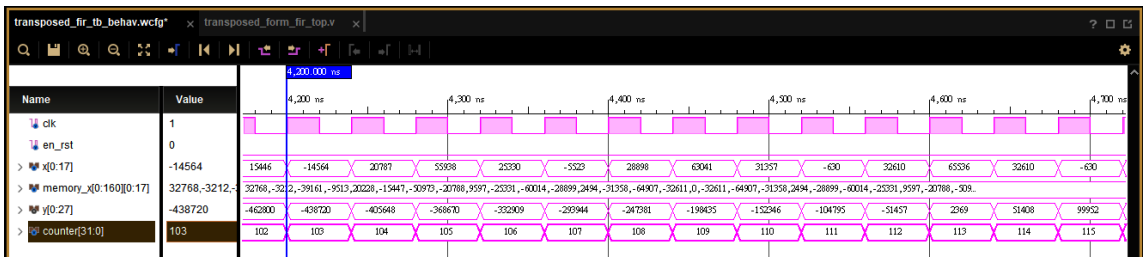


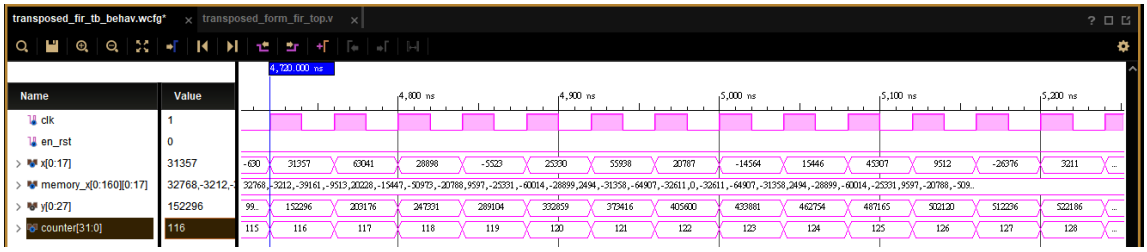


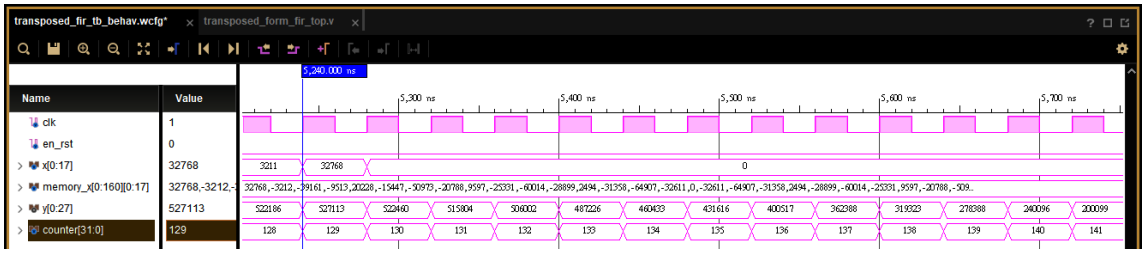


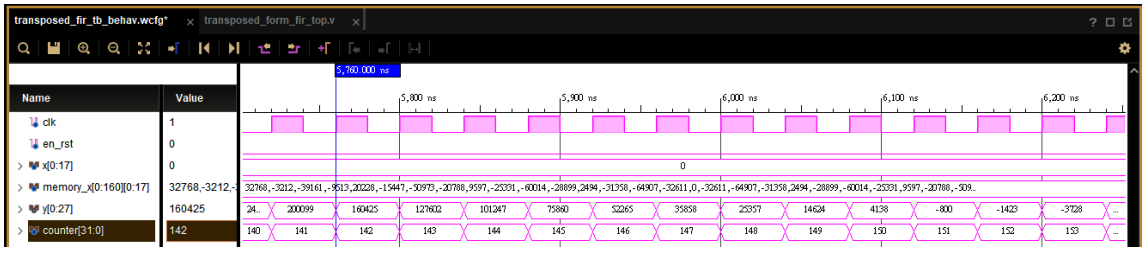

transposed_fir_tb_behav.wcfg*
transposed_form_fir_top.v
Name
Value
clk
1
en_rst
0
x[0:17]
2494
memory_x[0:160][0:17]
32768,-3212,-
y[0:27]
135298
counter[31:0]
77

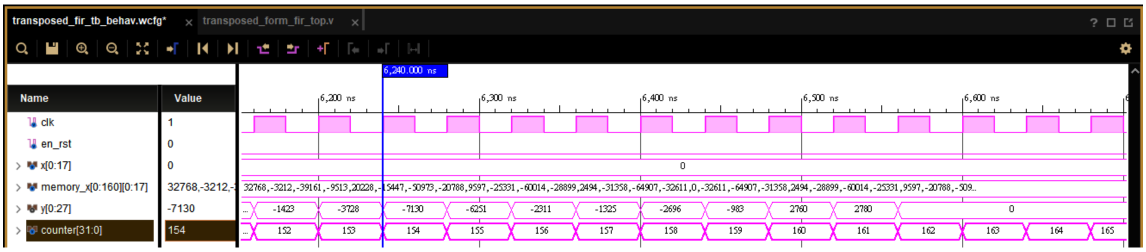

transposed_fir_tb_behav.wcfg*
transposed_form_fir_top.v
Name
Value
clk
1
en_rst
0
x[0:17]
-20788
memory_x[0:160][0:17]
32768,-3212,-
y[0:27]
-404192
counter[31:0]
90


transposed_fir_tb_behav.wcfg*
transposed_form_fir_top.v
Name
Value
clk
1
en_rst
0
x[0:17]
-14564
memory_x[0:160][0:17]
32768,-3212,-
y[0:27]
-438720
counter[31:0]
103


transposed_fir_tb_behav.wcfg*
transposed_form_fir_top.v
Name
Value
clk
1
en_rst
0
x[0:17]
31357
memory_x[0:160][0:17]
32768,-3212,-
y[0:27]
152296
counter[31:0]
116

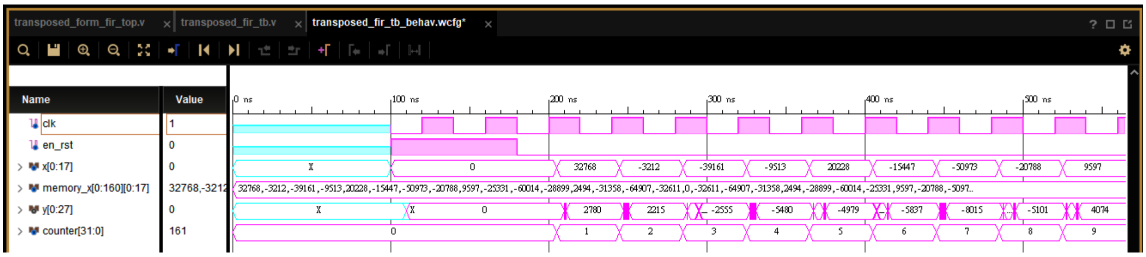

transposed_fir_tb_behav.wcfg*
transposed_form_fir_top.v
Name
Value
clk
1
en_rst
0
x[0:17]
32768
memory_x[0:160][0:17]
32768,-3212,-
y[0:27]
527113
counter[31:0]
129

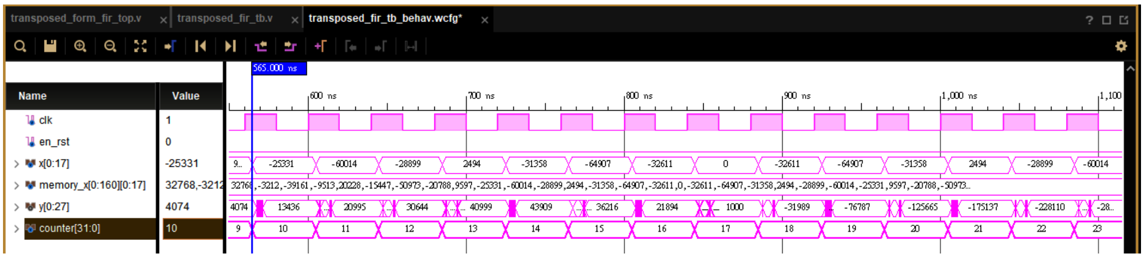

transposed_fir_tb_behav.wcfg*
transposed_form_fir_top.v
Name
Value
clk
1
en_rst
0
x[0:17]
0
memory_x[0:160][0:17]
32768,-3212,-
y[0:27]
160425
counter[31:0]
142

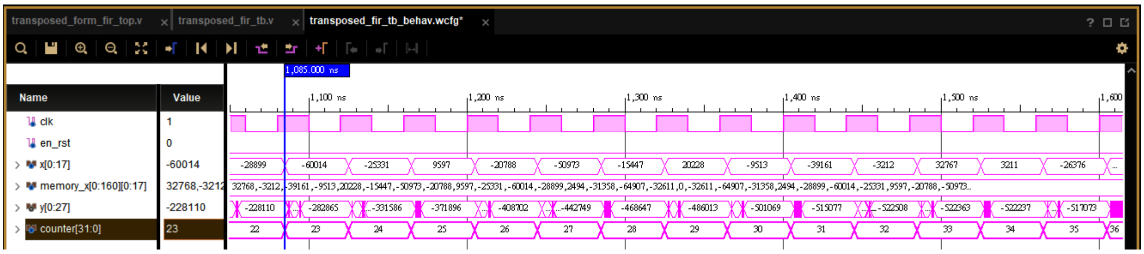


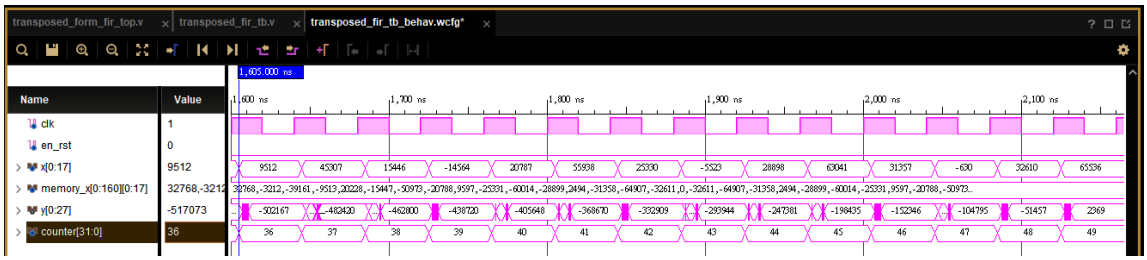

```
vivado4_y = [ 2780 2215 -2555 -5480 -4979 -5837 -8015 -5101 4074 13436 20995 ...
             30644 40999 43909 36216 21894 1000 -31989 -76787 -125665 -175137 ..
             -228110 -282865 -331586 -371896 -408702 -442749 -468647 -486013 ...
             -501069 -515077 -522508 -522363 -522237 -517073 -502167 -482420 ...
             -462800 -438720 -405648 -368670 -332909 -293944 -247381 -198435 ...
             -152346 -104795 -51457 2369 51408 99952 152296 203176 247331 ...
             289104 332859 373416 405600 433881 462754 487165 502120 512236 ...
             522186 527113 522187 512237 502120 487165 462754 433881 405600 ...
             373416 332859 289105 247332 203178 152298 99954 51411 2372 ...
             -51454 -104793 -152344 -198433 -247380 -293943 -332909 -368670 ...
             -405648 -438720 -462800 -482420 -502167 -517072 -522236 -522363 ...
             -522237 -517073 -502167 -482420 -462800 -438720 -405648 -368670 ...
             -332909 -293944 -247381 -198435 -152346 -104795 -51457 2369 ...
             51408 99952 152296 203176 247331 289104 332859 373416 405600 ...
             433881 462754 487165 502120 512236 522186 527113 522460 515804 ...
             506002 487226 460433 431616 400517 362388 319323 278388 240096 ...
             200099 160425 127602 101247 75860 52265 35858 25357 14624 ...
             4138 -800 -1423 -3728 -7130 -6251 -2311 -1325 -2696 -983 2760 ...
             2780];
```

Post-synthesis timing simulation:








transposed_form_fir_top.v
transposed_fir_tb.v
transposed_fir_tb_behav.wcfg*
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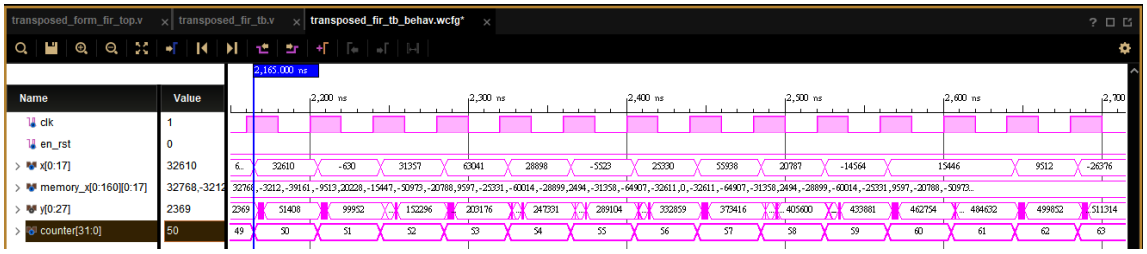
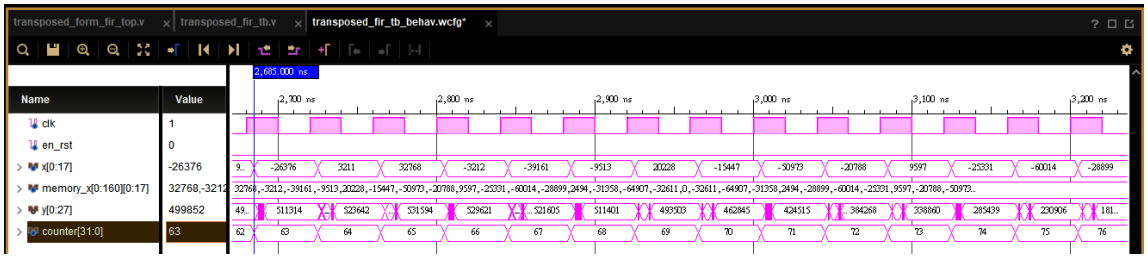
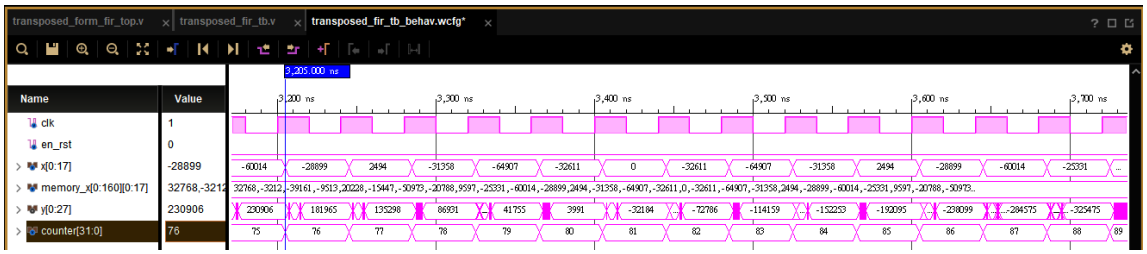
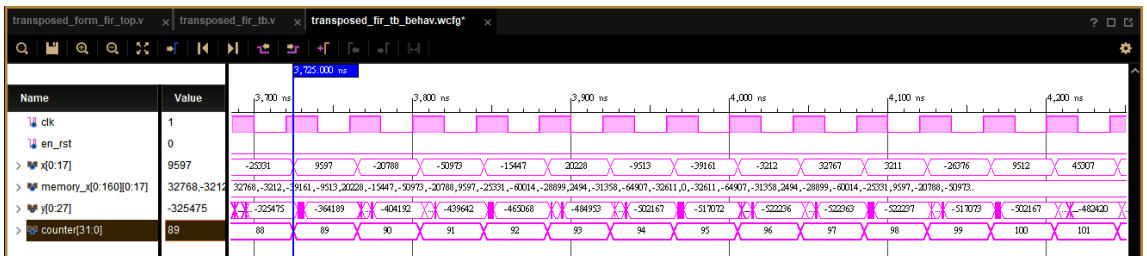
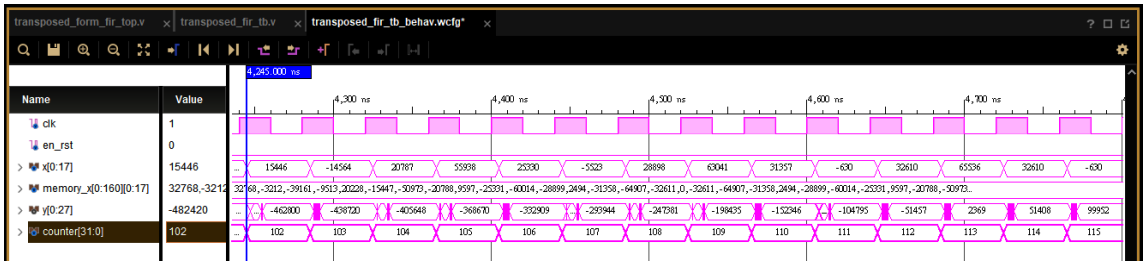
Name
Value
clk
1
en_rst
0
x[0:17]
9512
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-517073
counter[31:0]
36

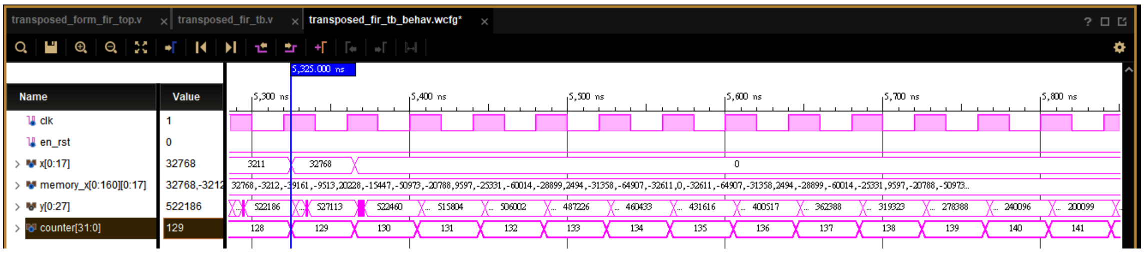

transposed_form_fir_top.v
transposed_fir_tb.v
transposed_fir_tb_behav.wcfg*
2,165.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
32610
memory_x[0:160][0:17]
32768,-3212
y[0:27]
2369
counter[31:0]
50


transposed_form_fir_top.v
transposed_fir_tb.v
transposed_fir_tb_behav.wcfg*
2,685.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-26376
memory_x[0:160][0:17]
32768,-3212
y[0:27]
499852
counter[31:0]
63

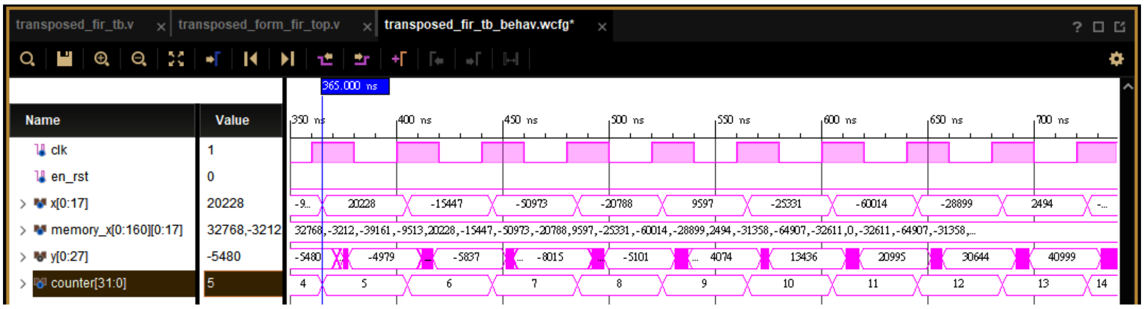

transposed_form_fir_top.v
transposed_fir_tb.v
transposed_fir_tb_behav.wcfg*
3,205.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-28899
memory_x[0:160][0:17]
32768,-3212
y[0:27]
230906
counter[31:0]
76

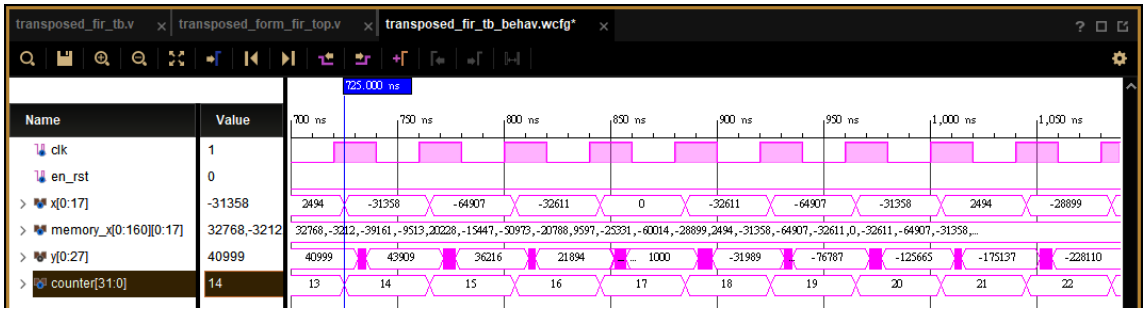

transposed_form_fir_top.v
transposed_fir_tb.v
transposed_fir_tb_behav.wcfg*
3,725.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
9597
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-325475
counter[31:0]
89


transposed_form_fir_top.v
transposed_fir_tb.v
transposed_fir_tb_behav.wcfg*
4,245.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
15446
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-482420
counter[31:0]
102



Post-implementation timing simulation:

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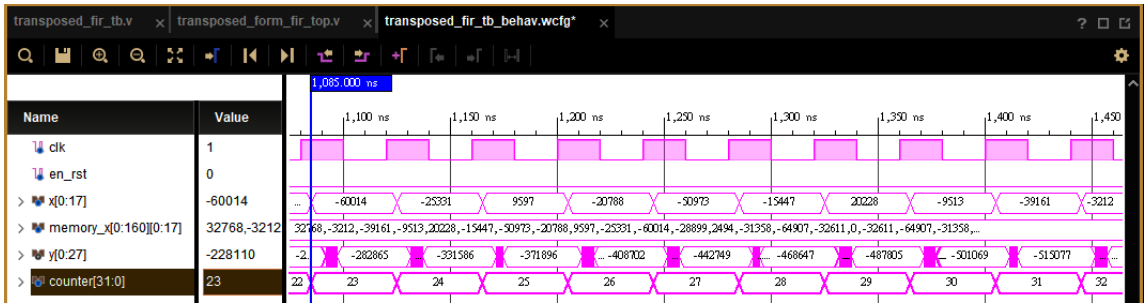
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
725.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-31358
memory_x[0:160][0:17]
32768,-3212
y[0:27]
40999
counter[31:0]
14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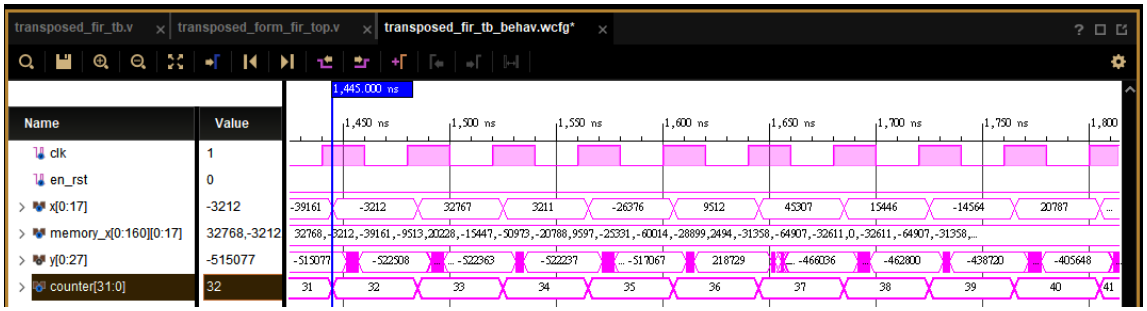
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
1,085.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-60014
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-228110
counter[31:0]
23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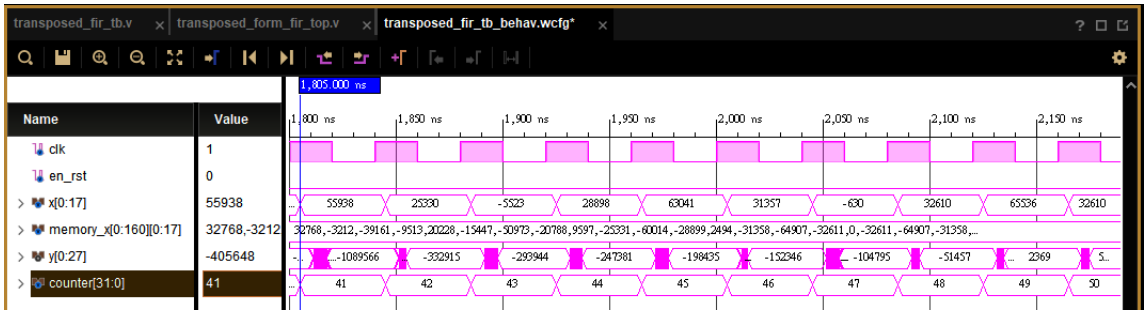
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
1,445.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-3212
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-515077
counter[31:0]
32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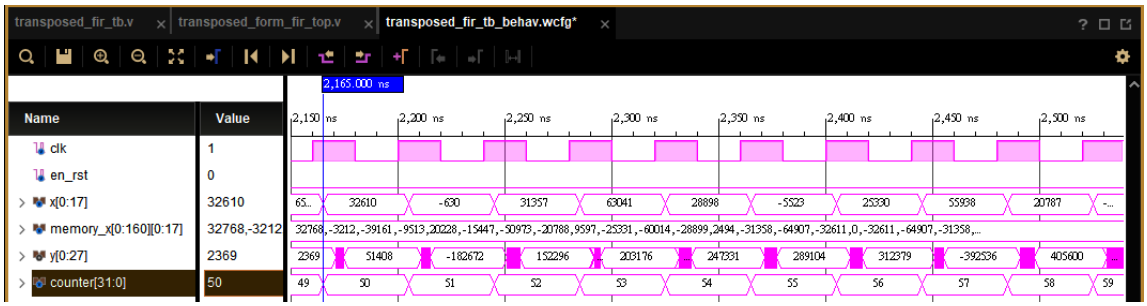
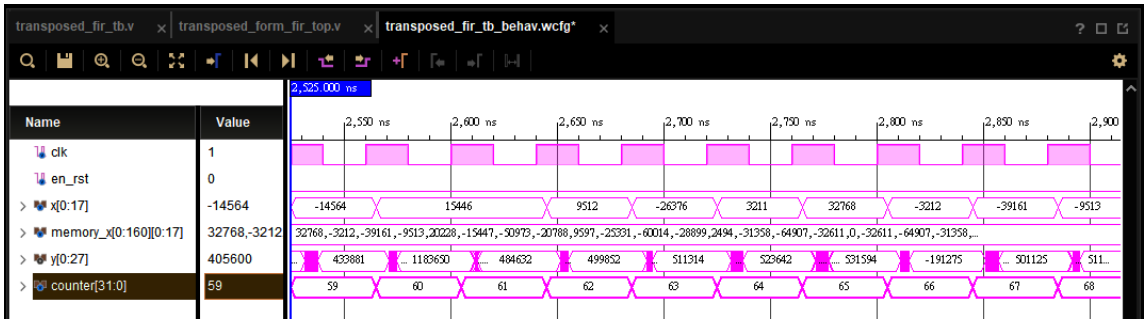
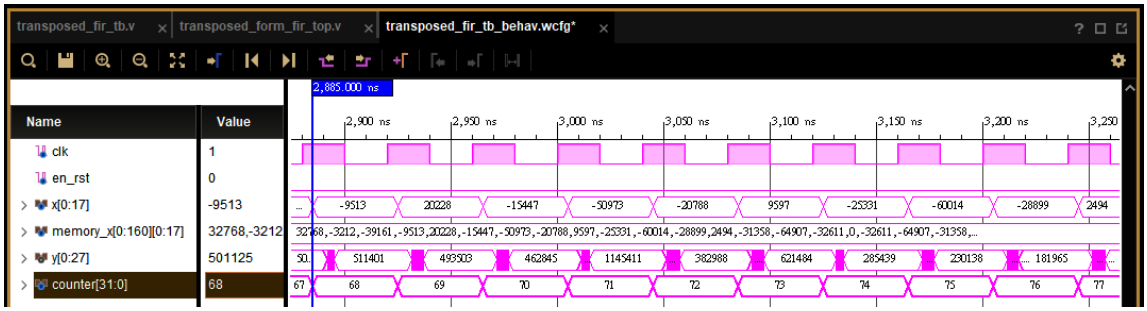
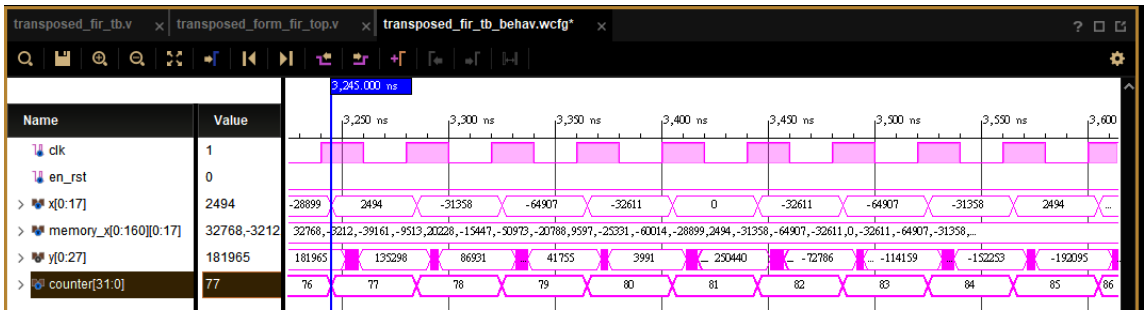
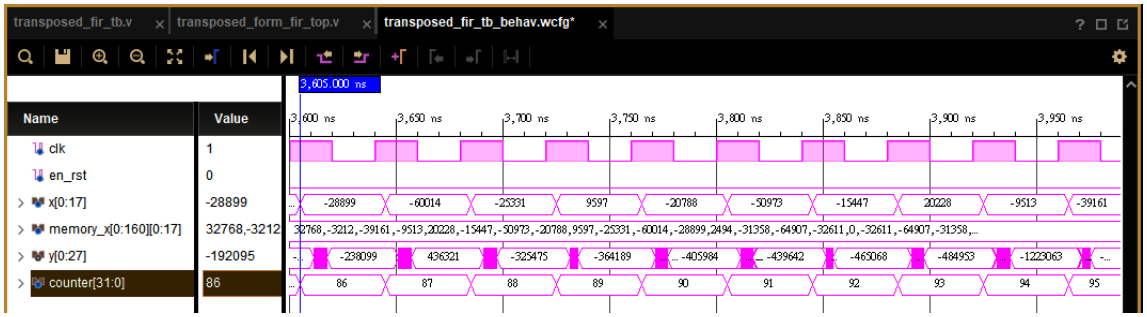
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
1,805.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
55938
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-405648
counter[31:0]
41

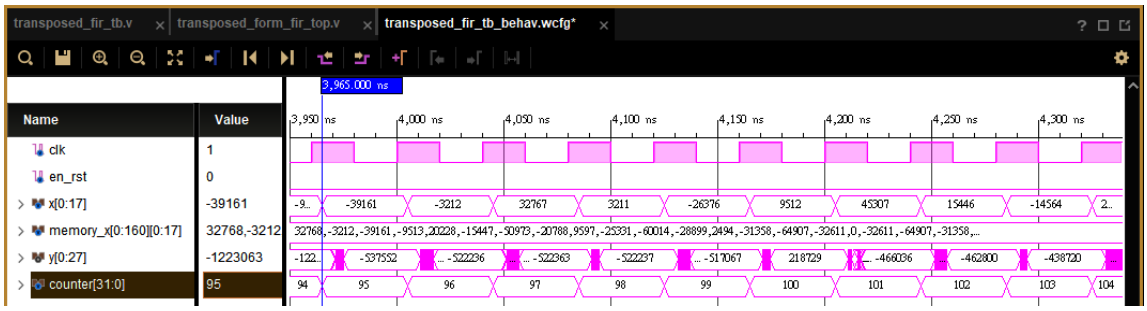

transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
2,165.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
32610
memory_x[0:160][0:17]
32768,-3212
y[0:27]
2369
counter[31:0]
50


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
2,525.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-14564
memory_x[0:160][0:17]
32768,-3212
y[0:27]
405600
counter[31:0]
59


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
2,885.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-9513
memory_x[0:160][0:17]
32768,-3212
y[0:27]
501125
counter[31:0]
68


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
3,245.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
2494
memory_x[0:160][0:17]
32768,-3212
y[0:27]
181965
counter[31:0]
77


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
3,605.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-28899
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-192095
counter[31:0]
86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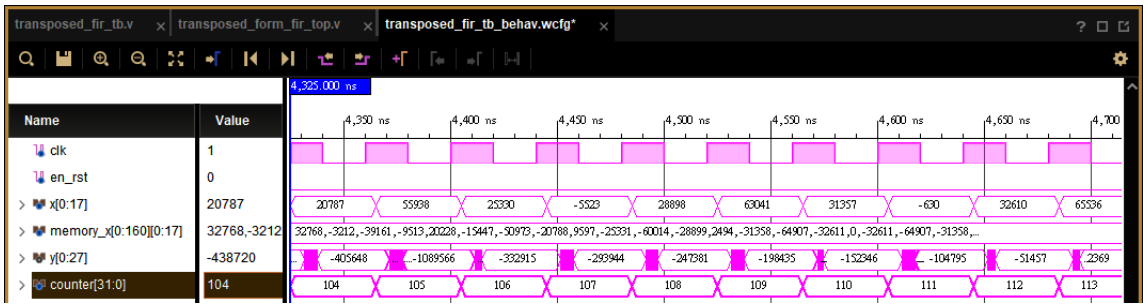
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
3,965.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
-39161
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-1223063
counter[31:0]
95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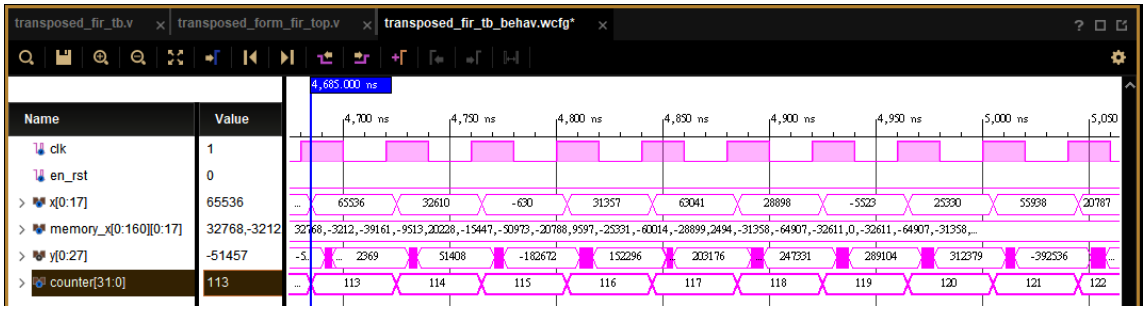
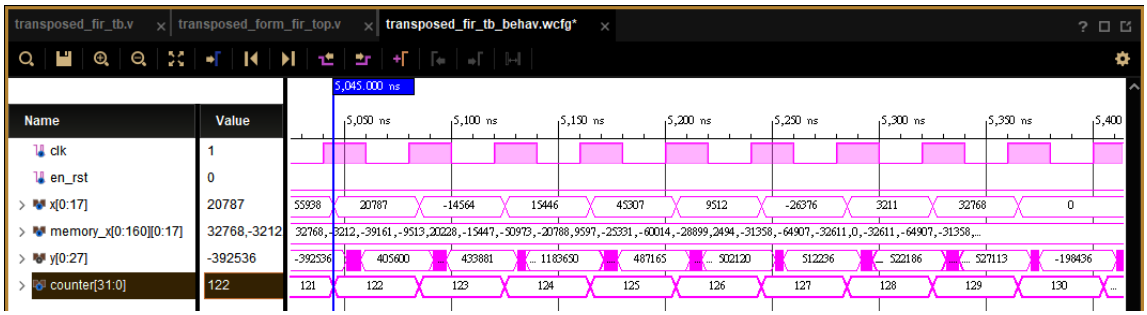
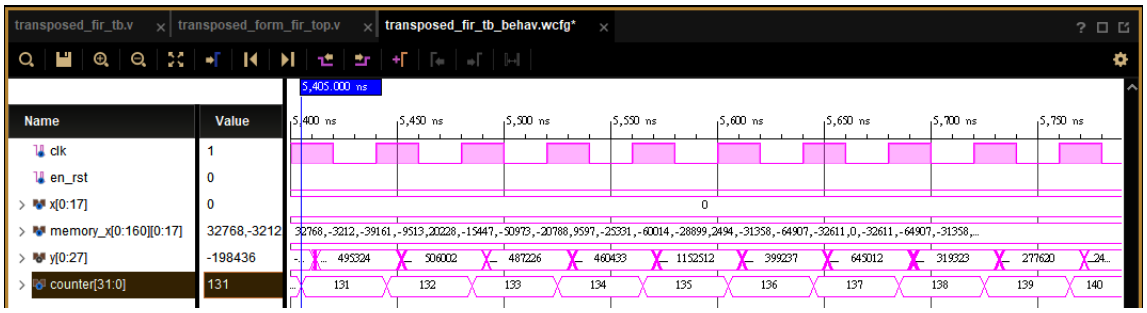
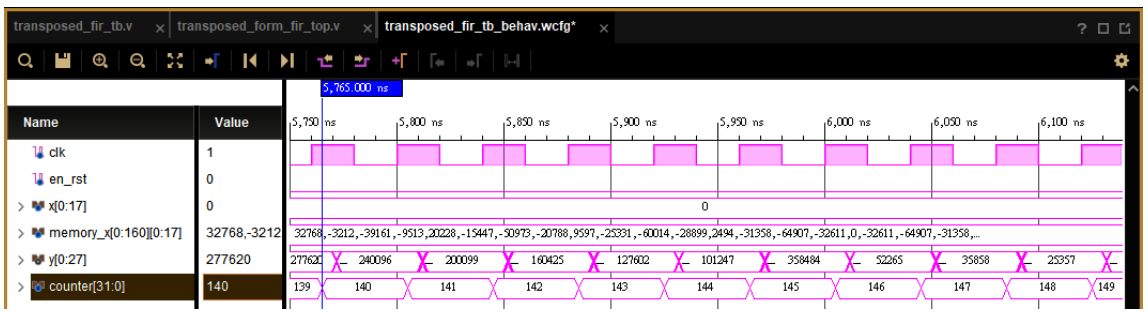
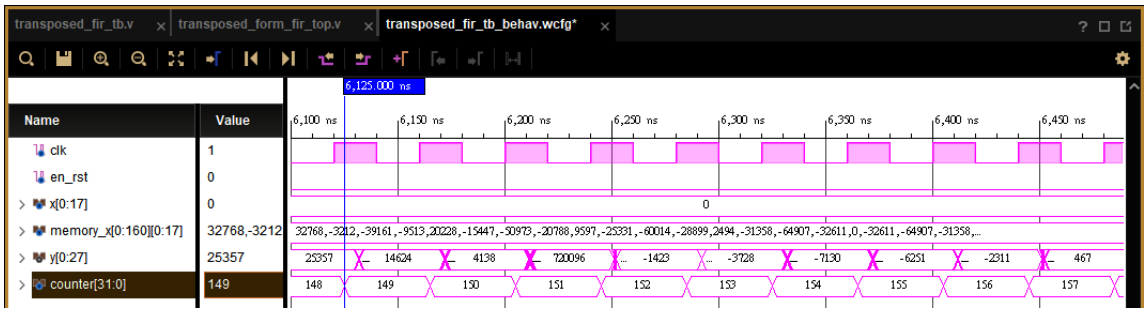
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
4,325.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
20787
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-438720
counter[31:0]
104
4,350 ns
4,400 ns
4,450 ns
4,500 ns
4,550 ns
4,600 ns
4,650 ns
4,700
20787
55938
25330
-5523
28898
63041
31357
-630
32610
65536
32768,-3212,-39161,-9513,20228,-15447,-30973,-20788,9597,-25331,-60014,-28899,2494,-31358,-64907,-32611,0,-32611,-64907,-31358,...
-405648
-1089566
-332915
-293944
-247381
-198435
-152346
-104795
-51457
2369
104
105
106
107
108
109
110
111
112
113


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
4,685.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
65536
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-51457
counter[31:0]
113
4,700 ns
4,750 ns
4,800 ns
4,850 ns
4,900 ns
4,950 ns
5,000 ns
5,050
65536
32610
-630
31357
63041
28898
-5523
25330
55938
20787
32768,-3212,-39161,-9513,20228,-15447,-30973,-20788,9597,-25331,-60014,-28899,2494,-31358,-64907,-32611,0,-32611,-64907,-31358,...
2369
51408
-182672
152296
203176
247331
289104
312379
-392536
113
114
115
116
117
118
119
120
121
122

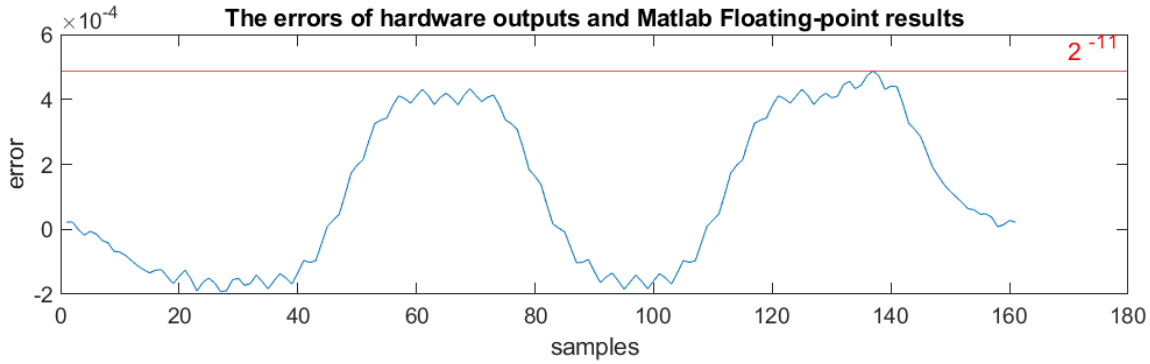

transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
5,045.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
20787
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-392536
counter[31:0]
122
5,050 ns
5,100 ns
5,150 ns
5,200 ns
5,250 ns
5,300 ns
5,350 ns
5,400
55938
20787
-14564
15446
45307
9512
-26376
3211
32768
0
32768,-3212,-39161,-9513,20228,-15447,-30973,-20788,9597,-25331,-60014,-28899,2494,-31358,-64907,-32611,0,-32611,-64907,-31358,...
405600
433881
1183650
487165
902120
522236
522186
527113
-198436
121
122
123
124
125
126
127
128
129
130


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
5,405.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
0
memory_x[0:160][0:17]
32768,-3212
y[0:27]
-198436
counter[31:0]
131
5,400 ns
5,450 ns
5,500 ns
5,550 ns
5,600 ns
5,650 ns
5,700 ns
5,750 ns
0
32768,-3212,-39161,-9513,20228,-15447,-30973,-20788,9597,-25331,-60014,-28899,2494,-31358,-64907,-32611,0,-32611,-64907,-31358,...
495324
506002
487226
460433
1152512
399237
645012
319323
277620
131
132
133
134
135
136
137
138
139
140


transposed_fir_tb.v
transposed_form_fir_top.v
transposed_fir_tb_behav.wcfg*
5,765.000 ns
Name
Value
clk
1
en_rst
0
x[0:17]
0
memory_x[0:160][0:17]
32768,-3212
y[0:27]
277620
counter[31:0]
140
5,750 ns
5,800 ns
5,850 ns
5,900 ns
5,950 ns
6,000 ns
6,050 ns
6,100 ns
0
32768,-3212,-39161,-9513,20228,-15447,-30973,-20788,9597,-25331,-60014,-28899,2494,-31358,-64907,-32611,0,-32611,-64907,-31358,...
240096
200099
160425
127602
101247
358484
52265
35858
25357
139
140
141
142
143
144
145
146
147
148
149

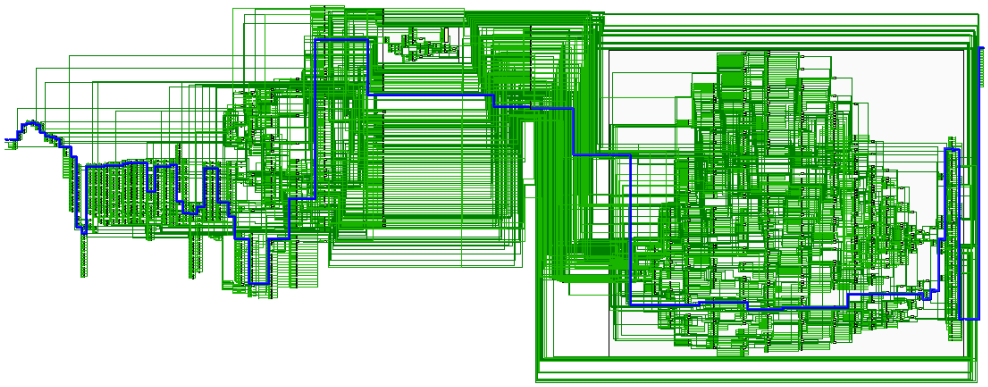


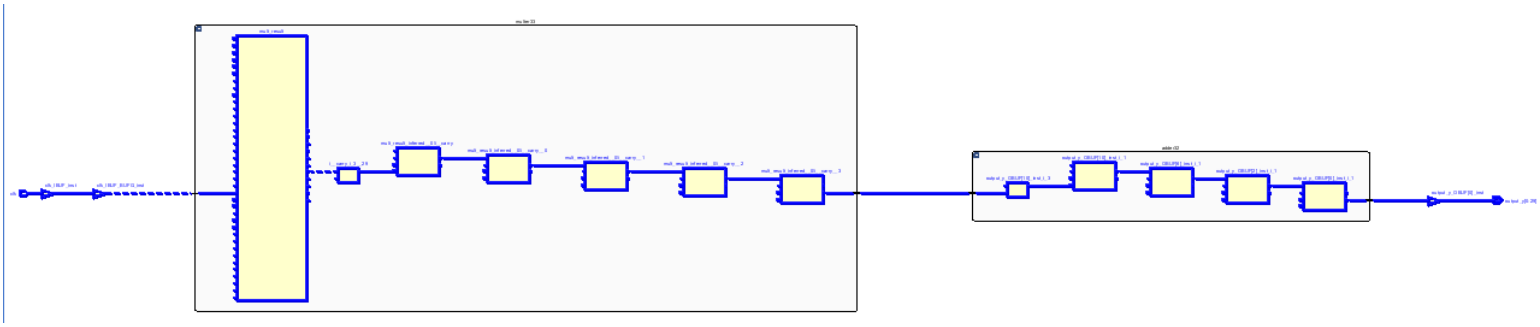
Show the errors of hardware outputs and Matlab floating-point results of transposed from FIR by Matlab figures.



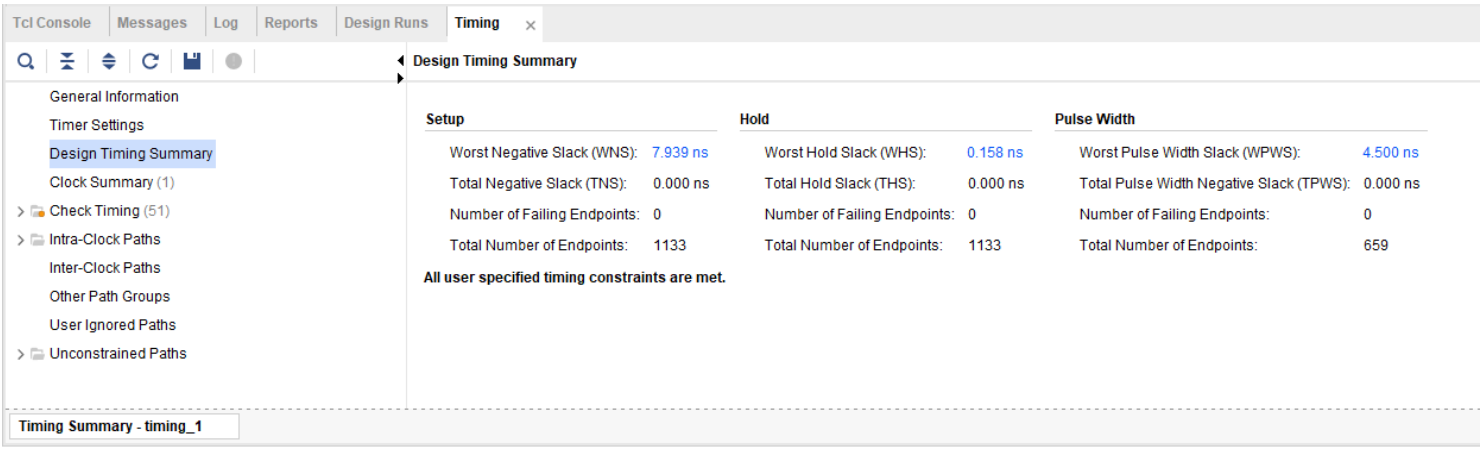
8. Find out the critical path of your design in Q5. Show the numbers of adders and multipliers in the critical path and list the timing information. (10%)

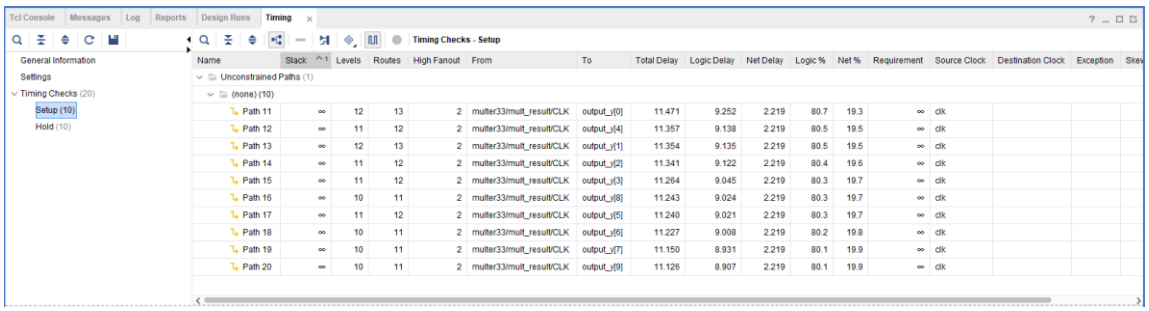
Setup time & critical path:



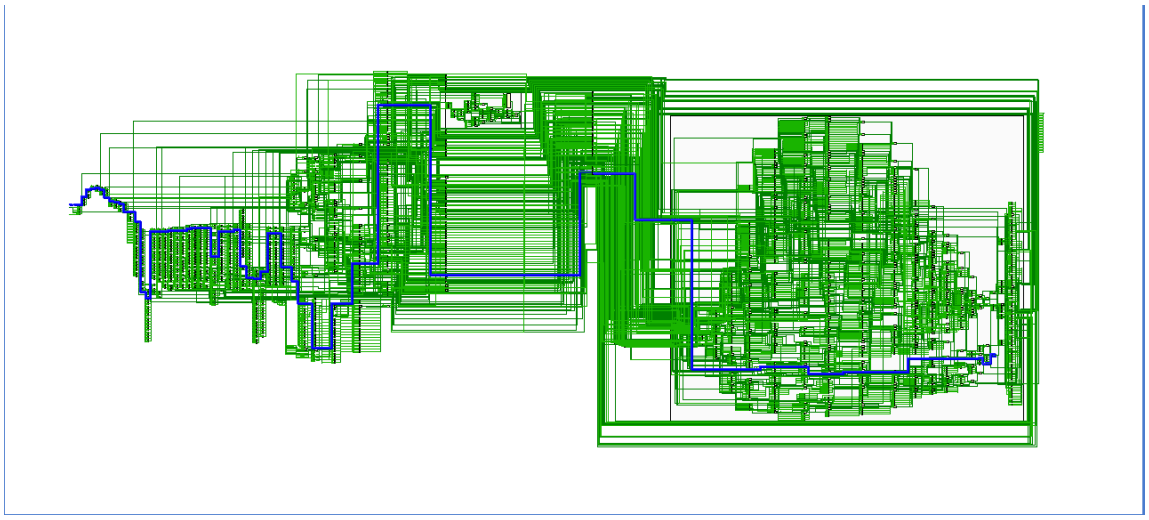


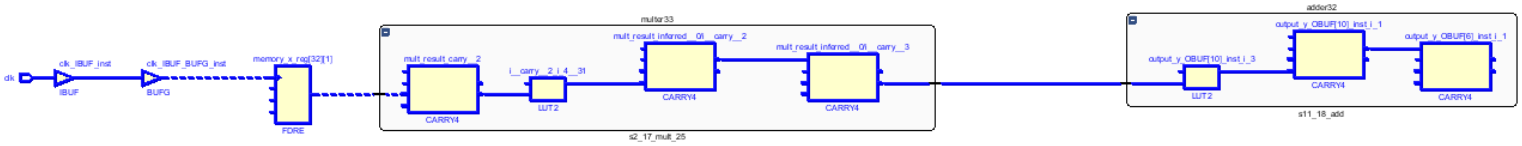
Print out the timing report.



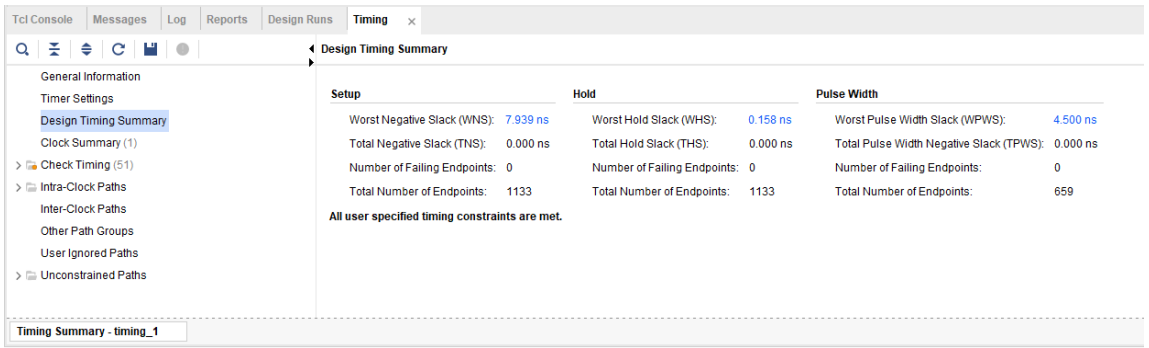


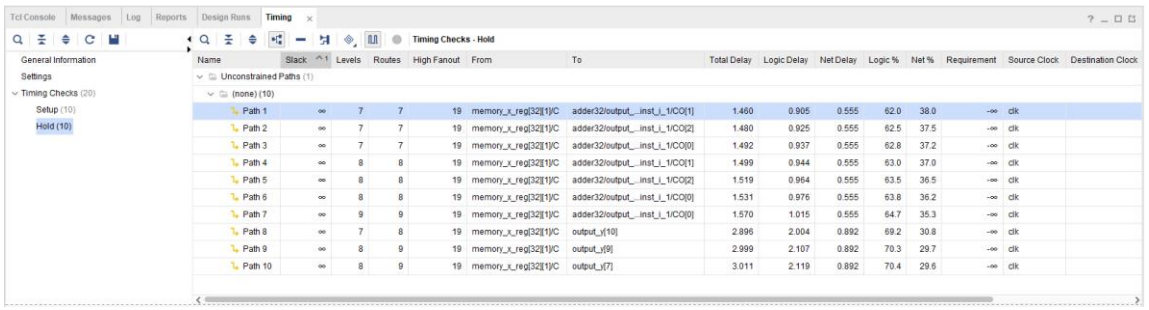
Hold time & critical path:





Print out the timing report.



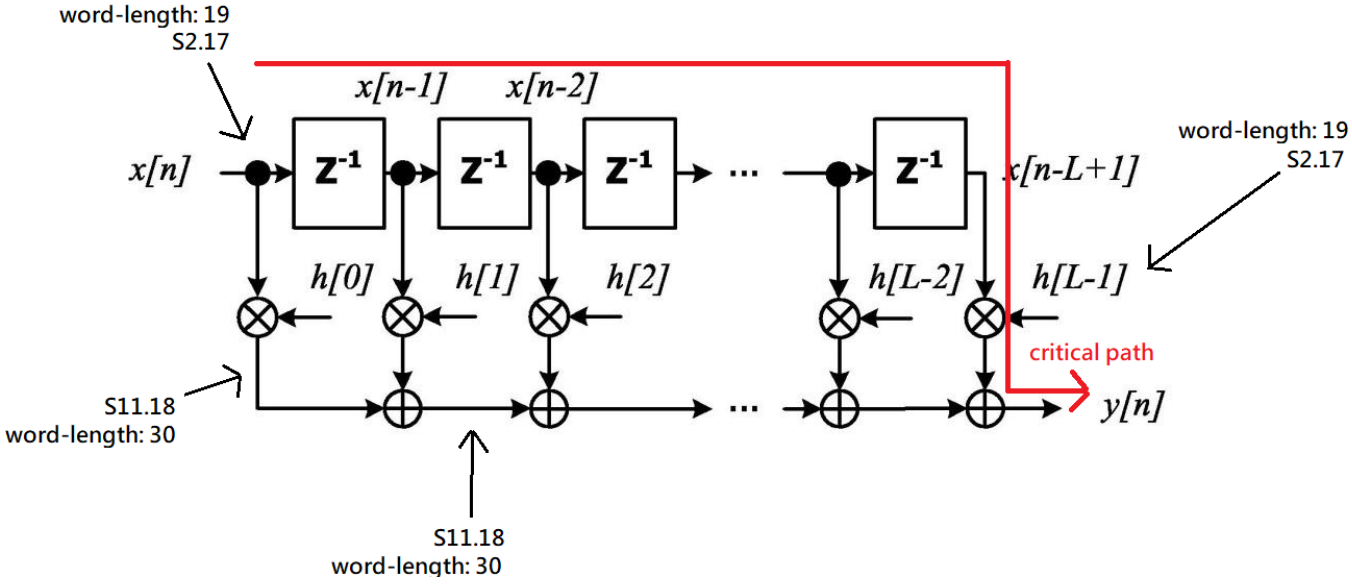


Show the numbers of adders and multipliers in the critical path

One adder + one multiplier in setup time critical path.

One adder + one multiplier in hold time critical path.

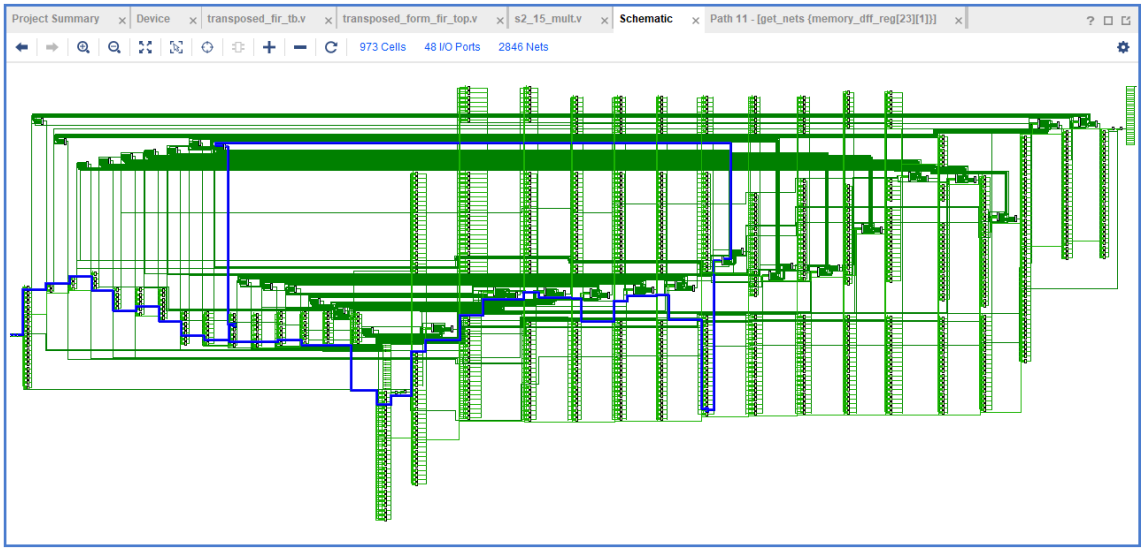
Mark the critical path of your direct-form FIR design in the block diagram. Also mark the input/output variable names and the word-lengths in the block diagram, which must be consistent with your Verilog codes.

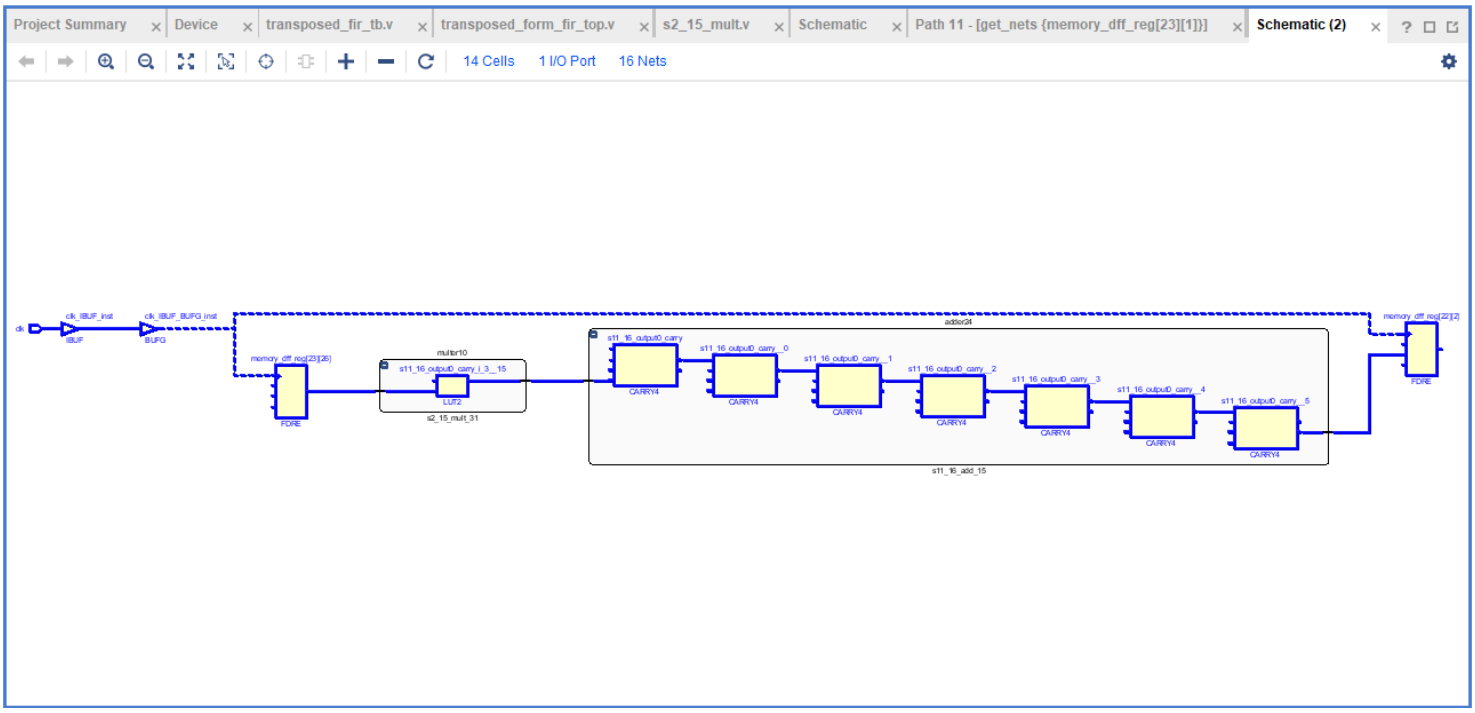



```
input signed [0:19] input_x; //s2.17
output signed [0:29] output_y; //s11.18
```

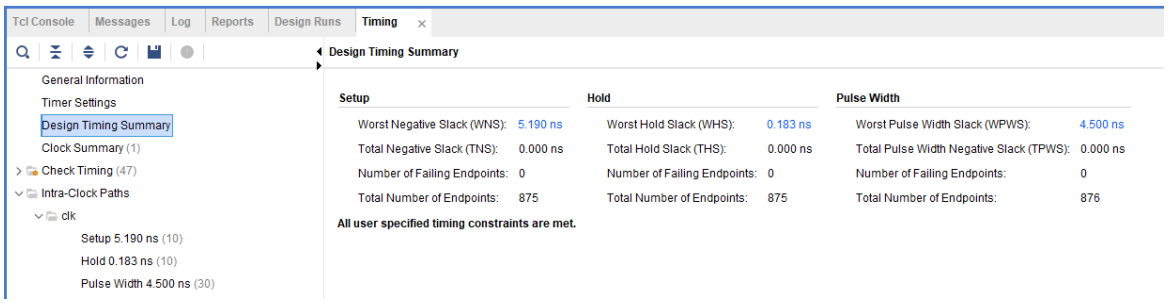
9. Find out the critical path of your design in Q6. Show the numbers of adders and multipliers in the critical path and list the timing information. (10%)

Setup time & critical path:





Print out the timing report.



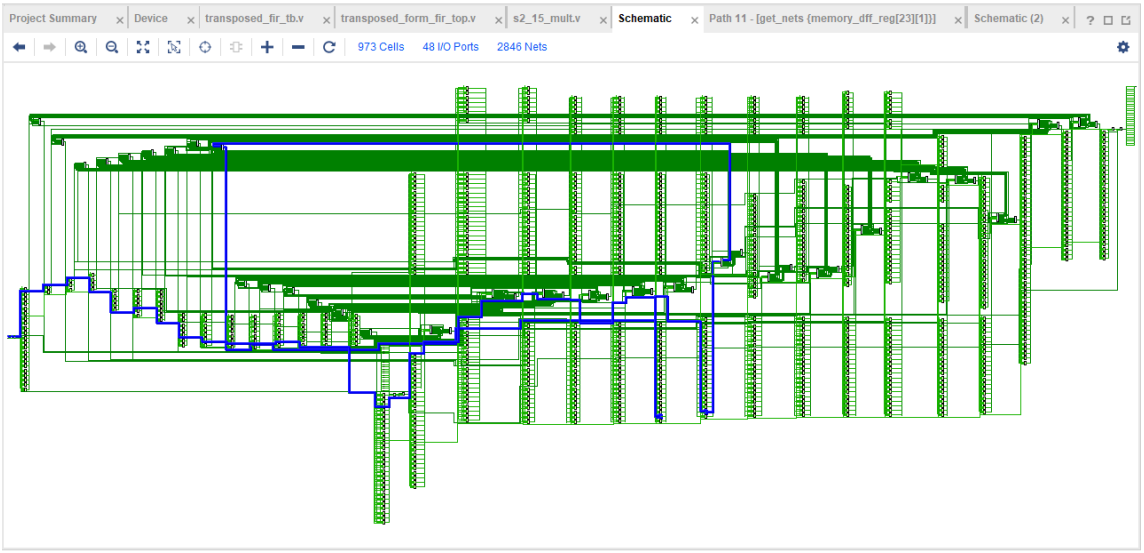
Tcl Console | Messages | Log | Reports | Design Runs | Timing

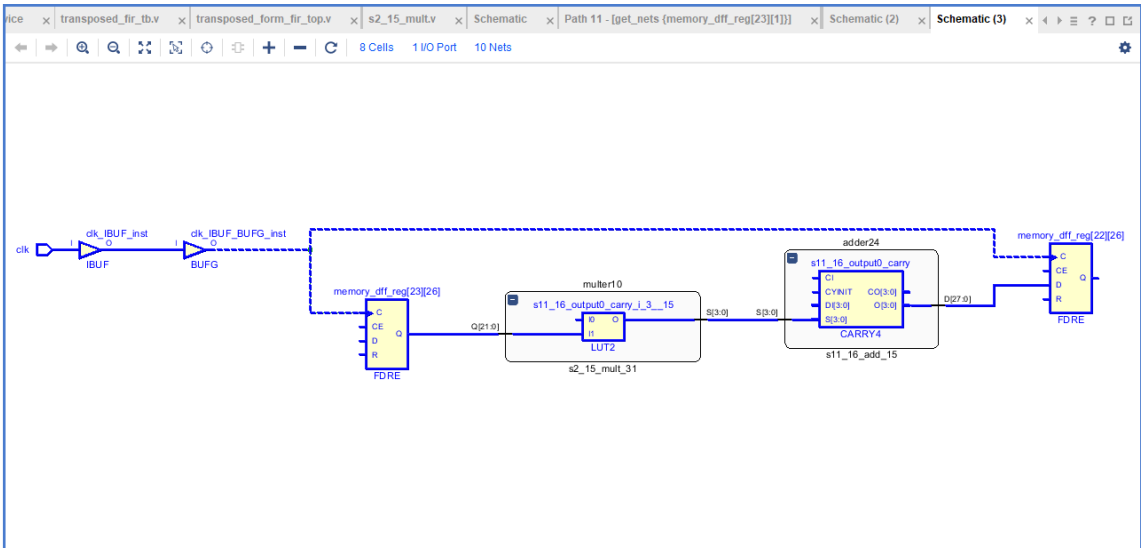
- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (47)
- Intra-Clock Paths
  - clk
    - Setup 5.190 ns (10)
    - Hold 0.183 ns (10)
    - Pulse Width 4.500 ns (30)
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths

Intra-Clock Paths - clk - Setup

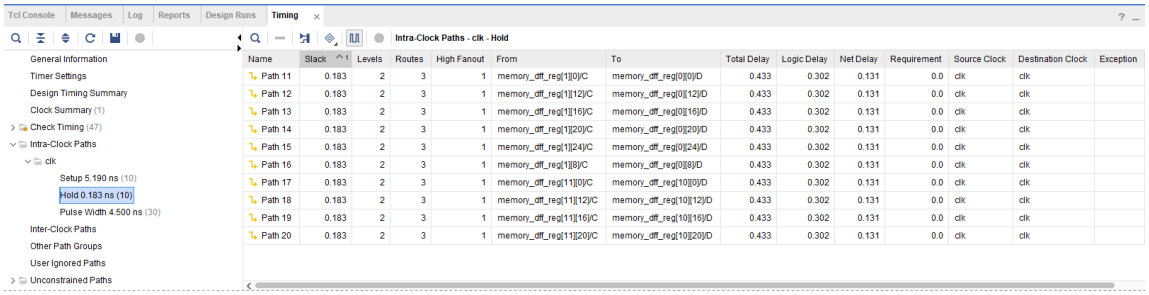
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.190	8	9	4	multer2/mult_result/CLK	memory_dff_reg[0][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 2	5.190	8	9	4	multer12/mult_result/CLK	memory_dff_reg[10][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 3	5.190	8	9	4	multer13/mult_result/CLK	memory_dff_reg[11][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 4	5.190	8	9	4	multer14/mult_result/CLK	memory_dff_reg[12][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 5	5.190	8	9	4	multer15/mult_result/CLK	memory_dff_reg[13][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 6	5.190	8	9	4	multer16/mult_result/CLK	memory_dff_reg[14][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 7	5.190	8	9	2	multer17/mult_result/CLK	memory_dff_reg[15][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 8	5.190	8	9	4	multer16/mult_result/CLK	memory_dff_reg[16][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 9	5.190	8	9	4	multer15/mult_result/CLK	memory_dff_reg[17][2]/D	4.692	3.883	0.809	10.0	clk	clk
Path 10	5.190	8	9	4	multer14/mult_result/CLK	memory_dff_reg[18][2]/D	4.692	3.883	0.809	10.0	clk	clk

Hold time & critical path:





Print out the timing report.

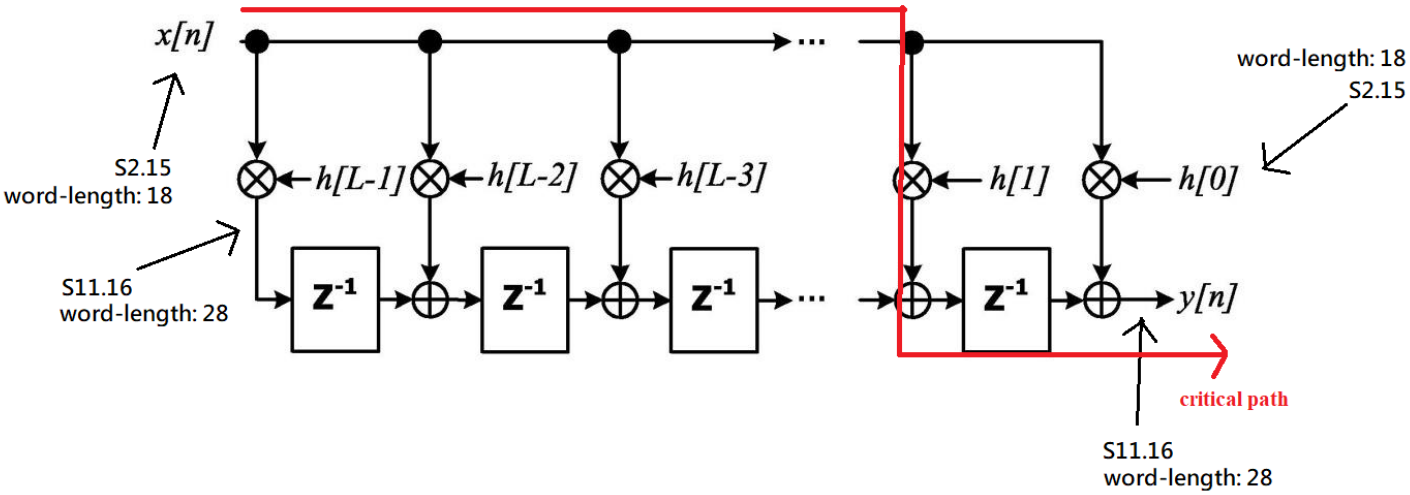


Show the numbers of adders and multipliers in the critical path

One adder + one multiplier in setup time critical path.

One adder + one multiplier in hold time critical path.

Mark the critical path of your transposed form FIR in the block diagram. Also mark the input/output variable names and the word-lengths in the block diagram, which must be consistent with your Verilog codes.




```
input signed [0:17] input_x; //s2.15
output signed [0:27] output_y; //s11.16
```