DCCDL LAB2

Verilog

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6. Show the Verilog behavior simulation results and post-route simulations results. (20%)

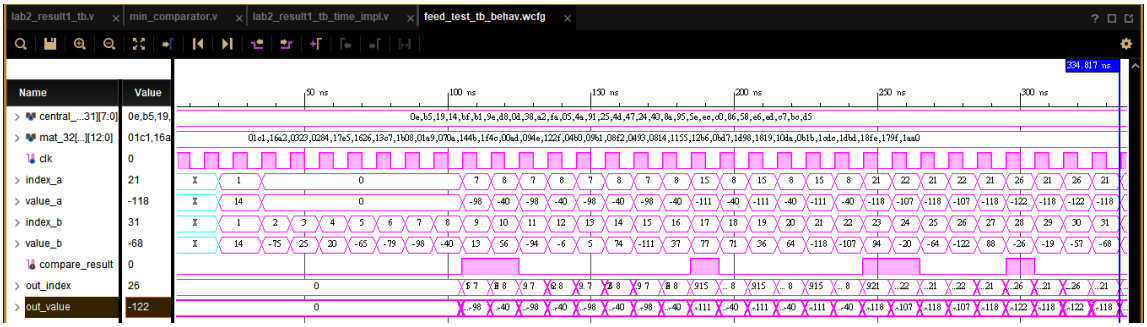
Behavior simulation results:

Serial compare results from matlab:

Command Window

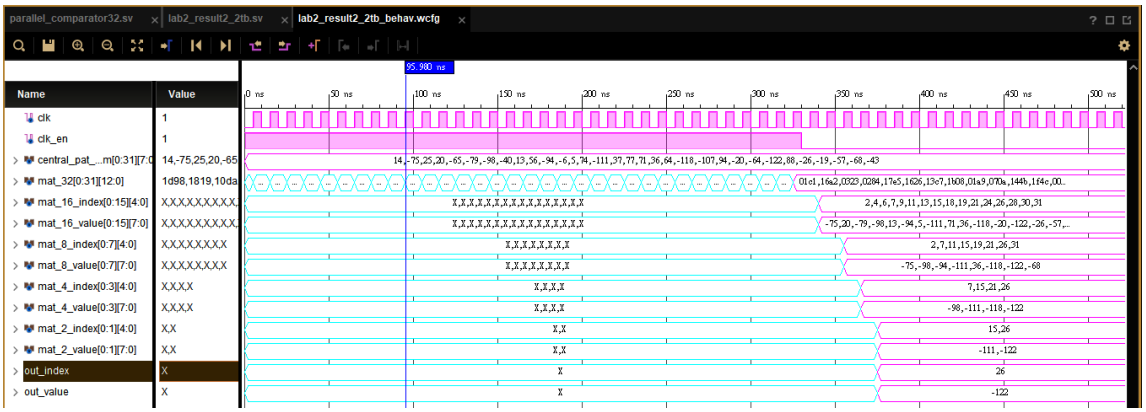
```
Clock  1 : Compare   14 and   14     Value of comparator is 0    Min/Index = 14/1
Clock  2 : Compare   14 and  -75     Value of comparator is 1    Min/Index = -75/2
Clock  3 : Compare  -75 and   25     Value of comparator is 0    Min/Index = -75/2
Clock  4 : Compare  -75 and   20     Value of comparator is 0    Min/Index = -75/2
Clock  5 : Compare  -75 and  -65     Value of comparator is 0    Min/Index = -75/2
Clock  6 : Compare  -75 and  -79     Value of comparator is 1    Min/Index = -79/6
Clock  7 : Compare  -79 and  -98     Value of comparator is 1    Min/Index = -98/7
Clock  8 : Compare  -98 and  -40     Value of comparator is 0    Min/Index = -98/7
Clock  9 : Compare  -98 and   13     Value of comparator is 0    Min/Index = -98/7
Clock 10 : Compare  -98 and   56     Value of comparator is 0    Min/Index = -98/7
Clock 11 : Compare  -98 and  -94     Value of comparator is 0    Min/Index = -98/7
Clock 12 : Compare  -98 and   -6     Value of comparator is 0    Min/Index = -98/7
Clock 13 : Compare  -98 and    5     Value of comparator is 0    Min/Index = -98/7
Clock 14 : Compare  -98 and   74     Value of comparator is 0    Min/Index = -98/7
Clock 15 : Compare  -98 and -111     Value of comparator is 1    Min/Index = -111/15
Clock 16 : Compare -111 and   37     Value of comparator is 0    Min/Index = -111/15
Clock 17 : Compare -111 and   77     Value of comparator is 0    Min/Index = -111/15
Clock 18 : Compare -111 and   71     Value of comparator is 0    Min/Index = -111/15
Clock 19 : Compare -111 and   36     Value of comparator is 0    Min/Index = -111/15
Clock 20 : Compare -111 and   64     Value of comparator is 0    Min/Index = -111/15
Clock 21 : Compare -111 and -118     Value of comparator is 1    Min/Index = -118/21
Clock 22 : Compare -118 and -107     Value of comparator is 0    Min/Index = -118/21
Clock 23 : Compare -118 and   94     Value of comparator is 0    Min/Index = -118/21
Clock 24 : Compare -118 and  -20     Value of comparator is 0    Min/Index = -118/21
Clock 25 : Compare -118 and  -64     Value of comparator is 0    Min/Index = -118/21
Clock 26 : Compare -118 and -122     Value of comparator is 1    Min/Index = -122/26
Clock 27 : Compare -122 and   88     Value of comparator is 0    Min/Index = -122/26
Clock 28 : Compare -122 and  -26     Value of comparator is 0    Min/Index = -122/26
Clock 29 : Compare -122 and  -19     Value of comparator is 0    Min/Index = -122/26
Clock 30 : Compare -122 and  -57     Value of comparator is 0    Min/Index = -122/26
Clock 31 : Compare -122 and  -68     Value of comparator is 0    Min/Index = -122/26
Clock 32 : Compare -122 and  -43     Value of comparator is 0    Min/Index = -122/26
```

post-route simulation results :



7. Show the Verilog behavior simulation results and post-route simulation results of every layer. (20%)

Behavior simulation results:

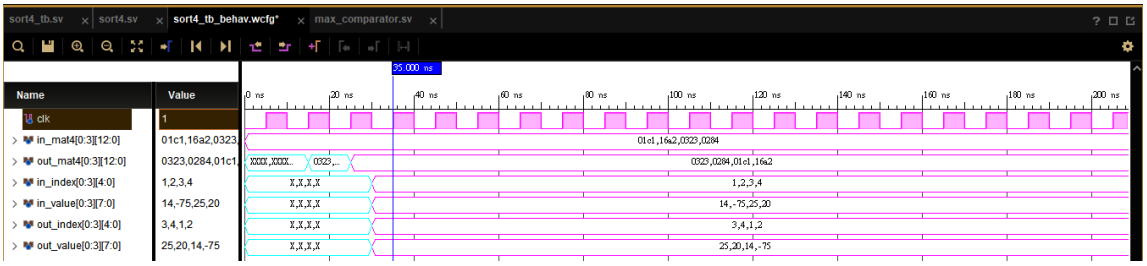



```
First layer [-75/02 20/04 -79/06 -98/07 13/09 -94/11 5/13 -111/15
             71/18 36/19 -118/21 -20/24 -122/26 -26/28 -57/30 -68/31]
Second layer [-75/02 -98/07 -94/11 -111/15 36/19 -118/21 -122/26 -68/31]
Third layer [-98/07 -111/15 -118/21 -122/26]
Fourth layer [-111/15 -122/26]
Final result [-122/26]
```

post-route simulation results :

8. Show the Verilog behavior simulation results and post-route simulation results. (20%)

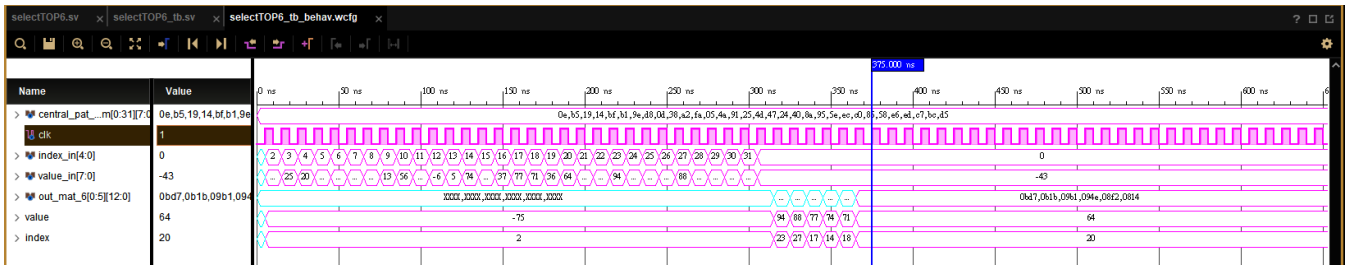
Behavior simulation results:



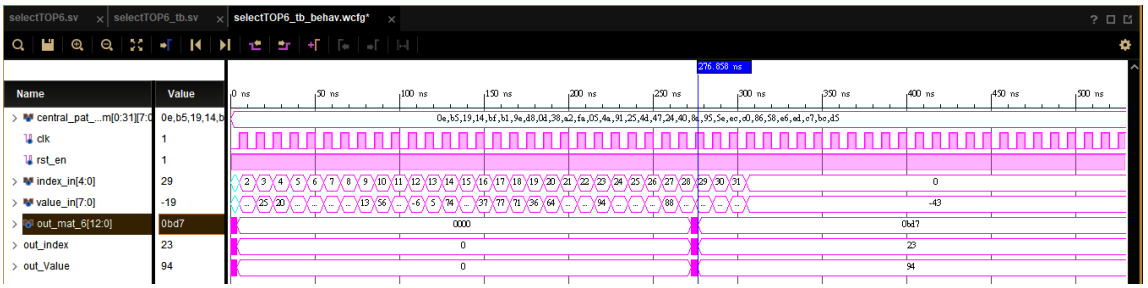
post-route simulation results :

9. Show the Verilog behavior simulation results and post-route simulation results. (20%)

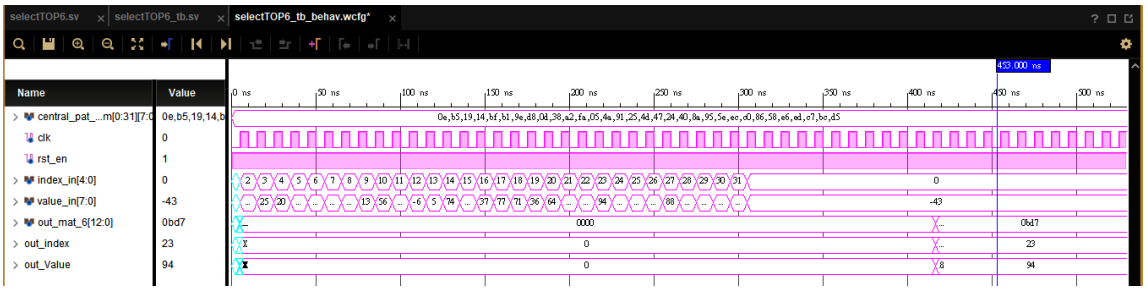
Behavior simulation results:



Post- synthesis timing simulation:



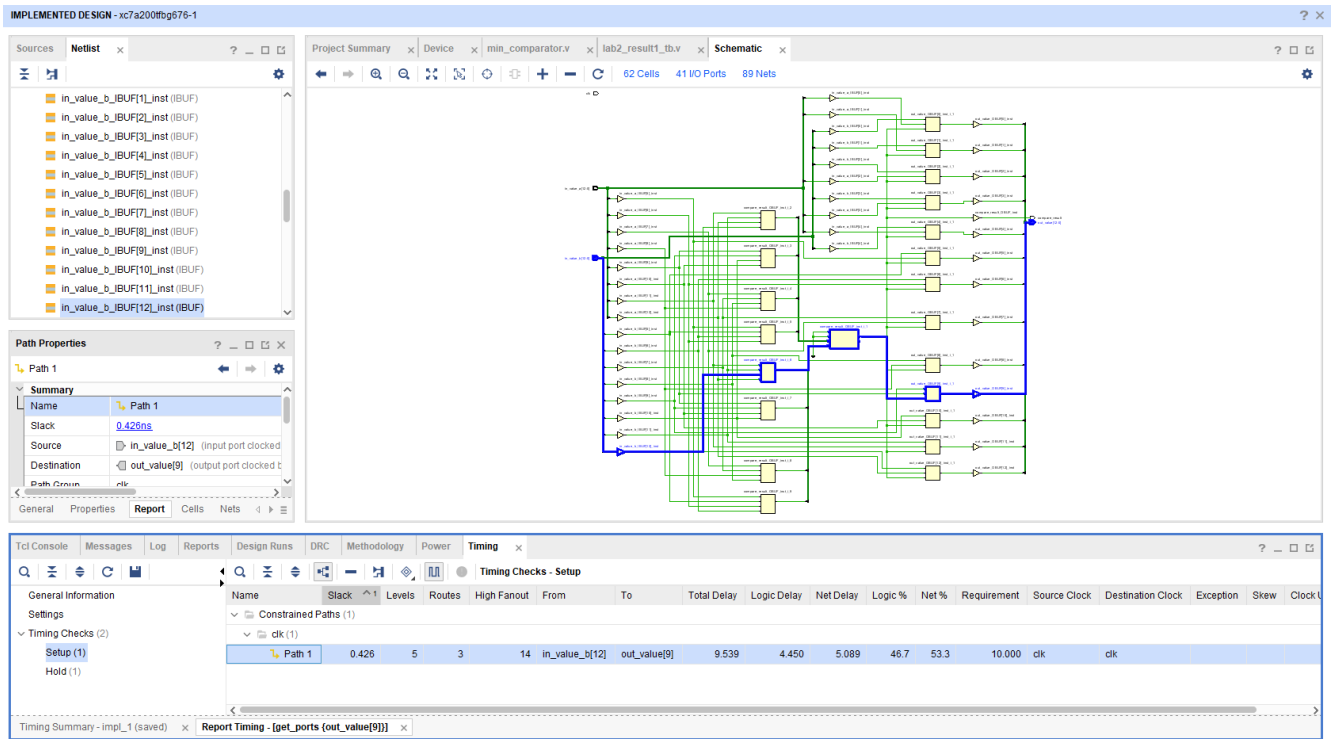
Post-implementation simulation:



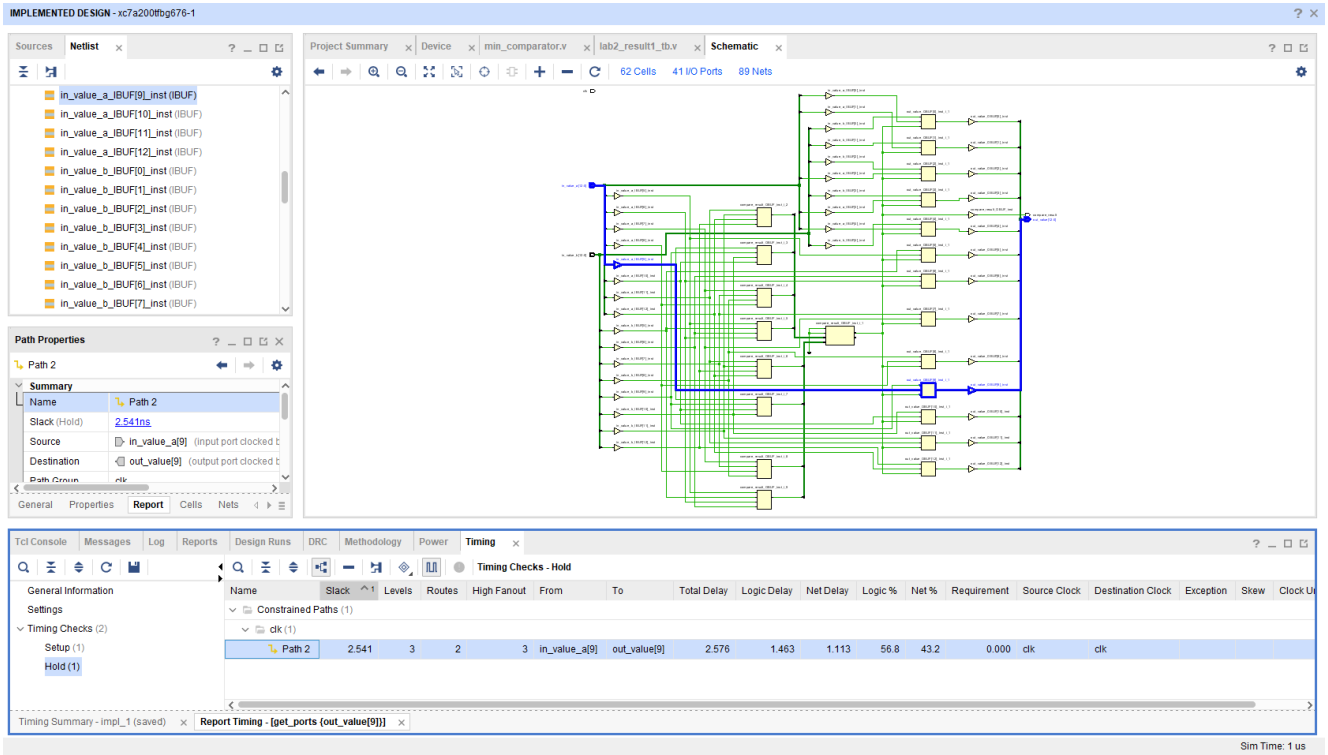
10. Show your timing report and draw the critical path from the max delay timing report of the block designed in Q6 and Q8 of Procedure. (20%)

Q6

Setup time:

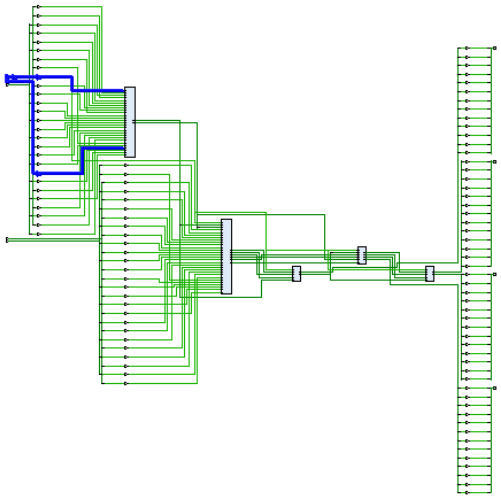


Setup time:

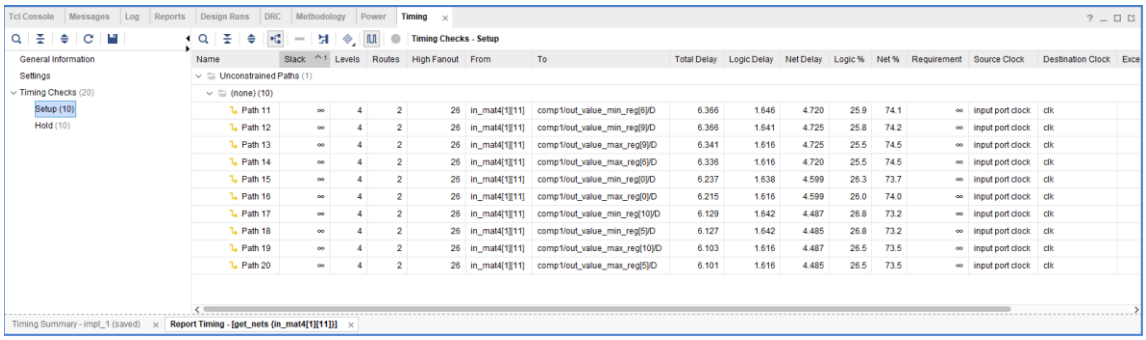


Q8

Setup time:



Timing report



Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | Power | Timing

Timing Checks - Setup

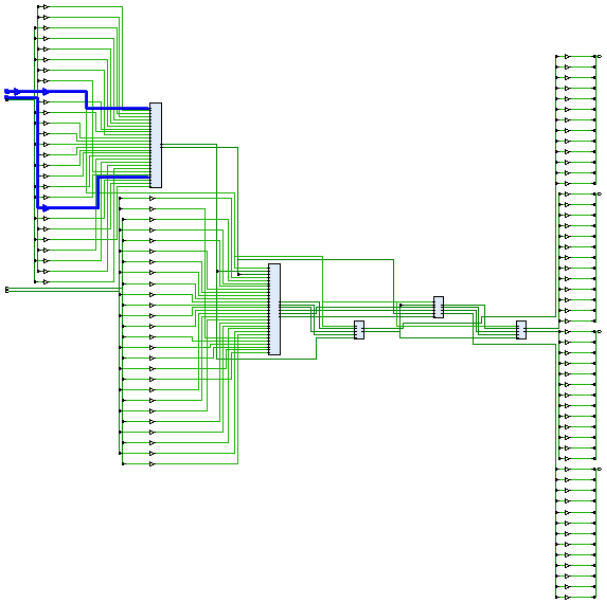
General Information
Settings
Timing Checks (20)
Setup (10)
Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exce
Unconstrained Paths (1)															
(none) (10)															
Path 11	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[6]/D	6.366	1.646	4.720	25.9	74.1	∞	input port clock	clk	
Path 12	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[9]/D	6.366	1.641	4.725	25.8	74.2	∞	input port clock	clk	
Path 13	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[9]/D	6.341	1.616	4.725	25.5	74.5	∞	input port clock	clk	
Path 14	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[6]/D	6.336	1.616	4.720	25.5	74.5	∞	input port clock	clk	
Path 15	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[0]/D	6.237	1.638	4.599	26.3	73.7	∞	input port clock	clk	
Path 16	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[0]/D	6.215	1.616	4.599	26.0	74.0	∞	input port clock	clk	
Path 17	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[10]/D	6.129	1.642	4.487	26.8	73.2	∞	input port clock	clk	
Path 18	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[5]/D	6.127	1.642	4.485	26.8	73.2	∞	input port clock	clk	
Path 19	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[10]/D	6.103	1.616	4.487	26.5	73.5	∞	input port clock	clk	
Path 20	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[5]/D	6.101	1.616	4.485	26.5	73.5	∞	input port clock	clk	

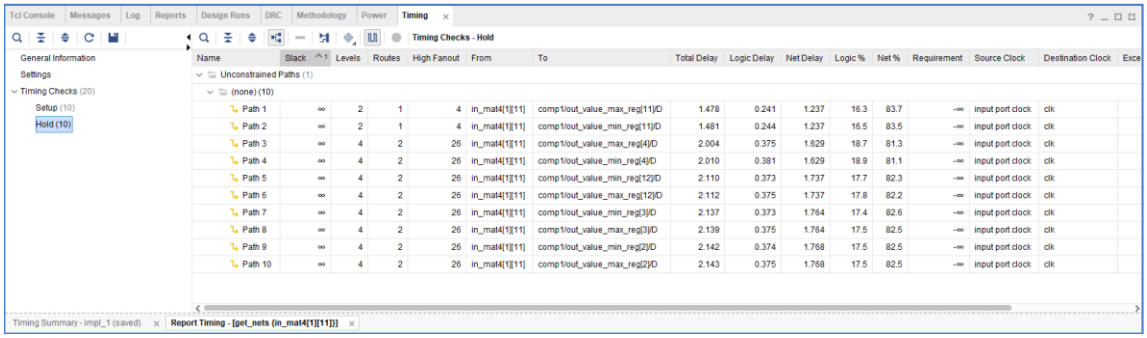
Timing Summary - impl_1 (saved) | Report Timing - [get_nets {in_mat4[1][11]}]

Hold time:

critical path



Timing report:



Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | Power | Timing

Timing Checks - Hold

General Information
Settings
Timing Checks (20)
Setup (10)
Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock	Exce
Unconstrained Paths (1)															
(none) (10)															
Path 1	∞	2	1	4	in_mat4[1][11]	comp1/out_value_max_reg[11]/D	1.478	0.241	1.237	16.3	83.7	-∞	input port clock	clk	
Path 2	∞	2	1	4	in_mat4[1][11]	comp1/out_value_min_reg[11]/D	1.481	0.244	1.237	16.5	83.5	-∞	input port clock	clk	
Path 3	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[4]/D	2.004	0.375	1.629	18.7	81.3	-∞	input port clock	clk	
Path 4	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[4]/D	2.010	0.381	1.629	18.9	81.1	-∞	input port clock	clk	
Path 5	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[12]/D	2.110	0.373	1.737	17.7	82.3	-∞	input port clock	clk	
Path 6	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[12]/D	2.112	0.375	1.737	17.8	82.2	-∞	input port clock	clk	
Path 7	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[3]/D	2.137	0.373	1.764	17.4	82.6	-∞	input port clock	clk	
Path 8	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[3]/D	2.139	0.375	1.764	17.5	82.5	-∞	input port clock	clk	
Path 9	∞	4	2	26	in_mat4[1][11]	comp1/out_value_min_reg[2]/D	2.142	0.374	1.768	17.5	82.5	-∞	input port clock	clk	
Path 10	∞	4	2	26	in_mat4[1][11]	comp1/out_value_max_reg[2]/D	2.143	0.375	1.768	17.5	82.5	-∞	input port clock	clk	

Timing Summary - impl_1 (saved) | Report Timing - [get_nets {in_mat4[1][11]}]