DCCDL LAB4

Verilog

電機碩一　111521035　林豪澤

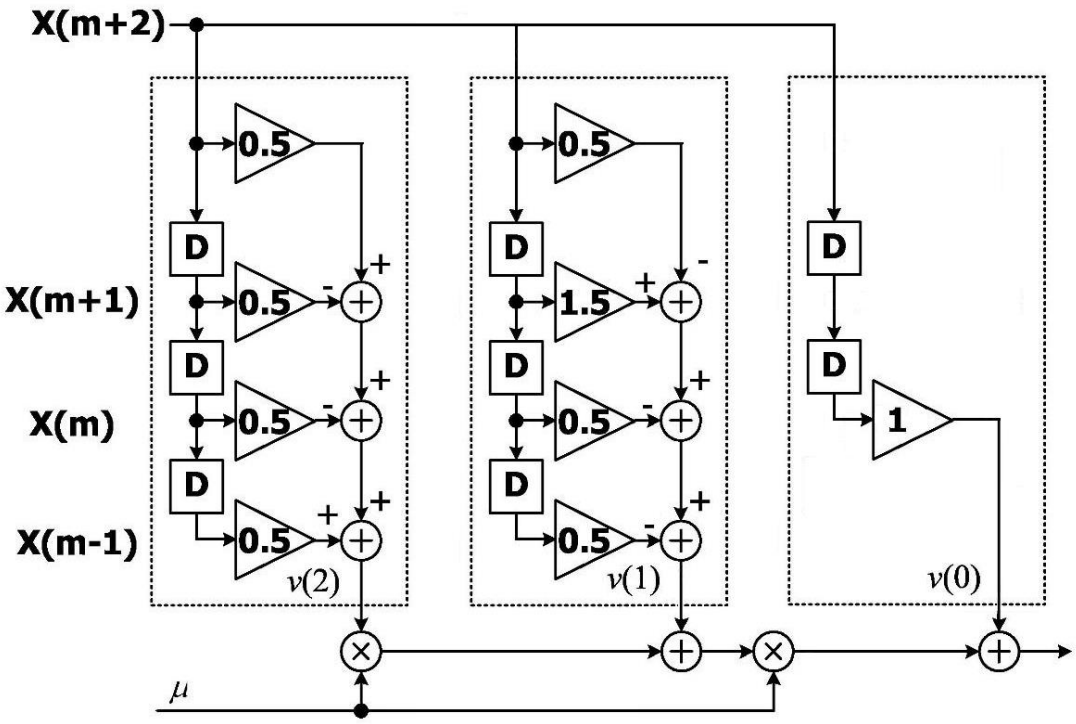
6. Please depict the final architecture of the piece-wise parabolic interpolator (10%) and show the results of different word-length settings versus the root mean squared error for

a. Wordlength of input (5%)

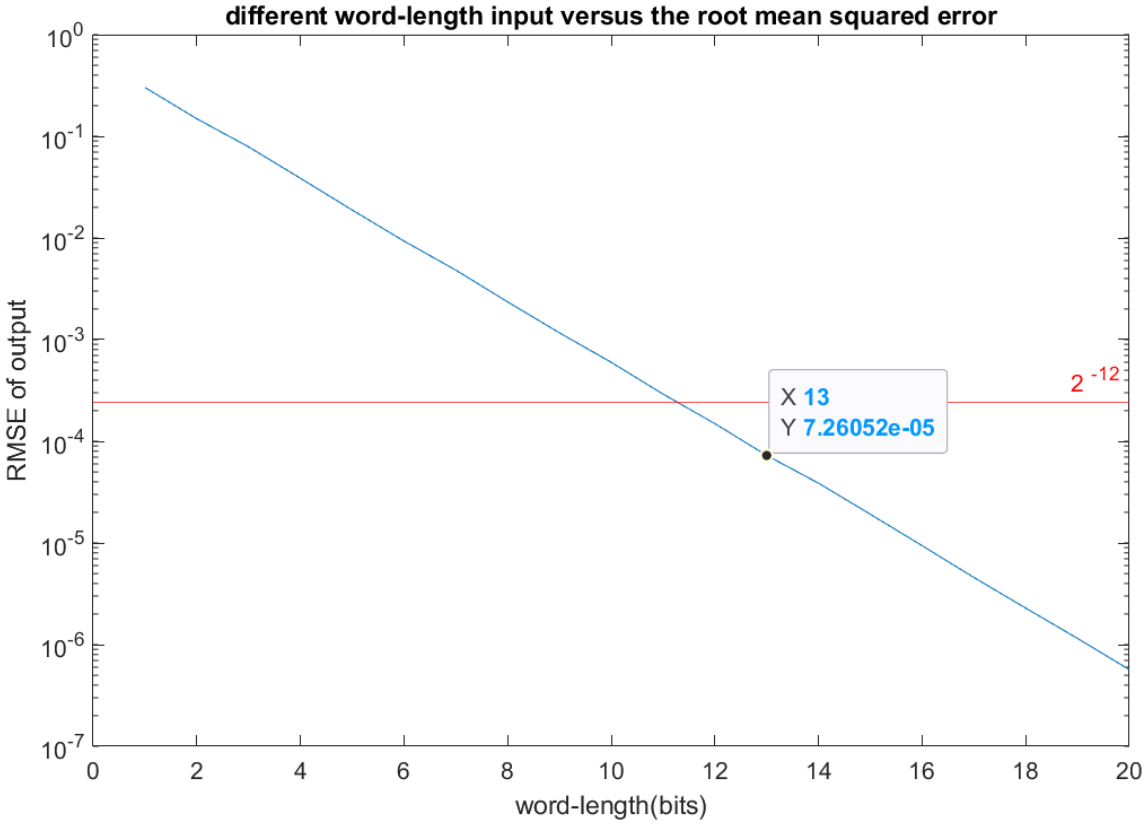
b. Wordlength of μ (5%)

c. Wordlength of multiplier (by μ) (5%)

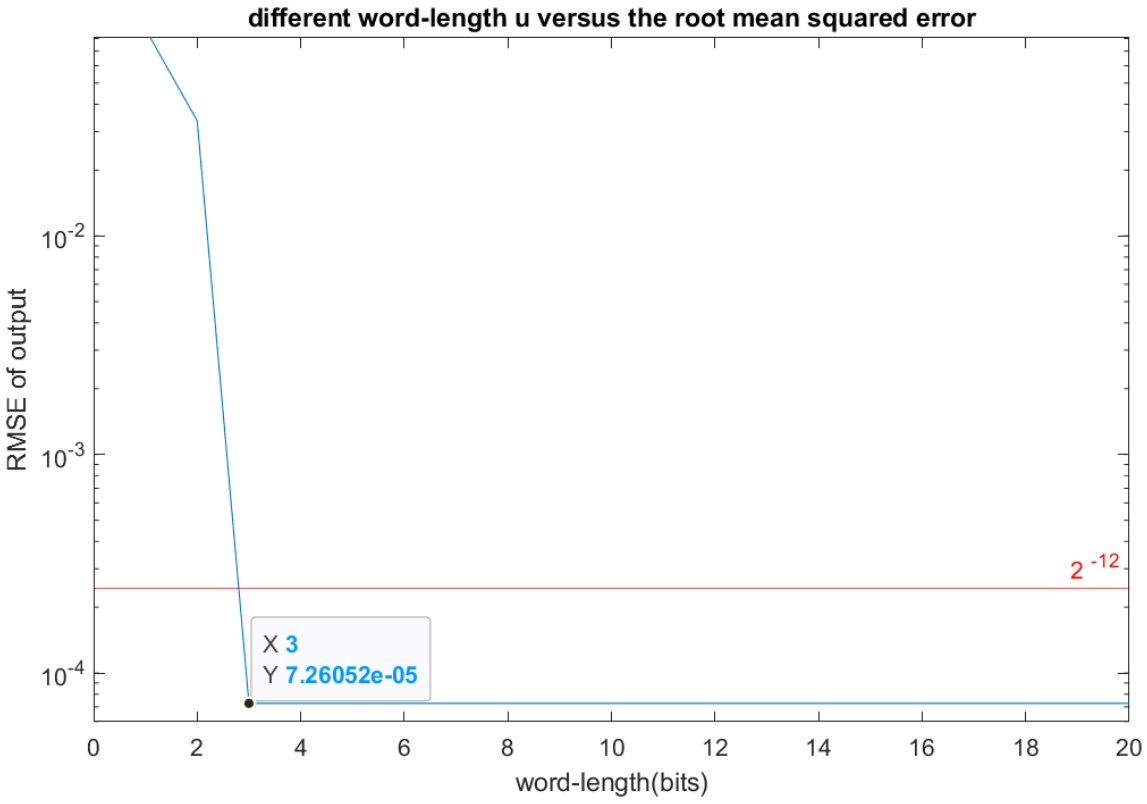
d. Wordlength of adder (5%)



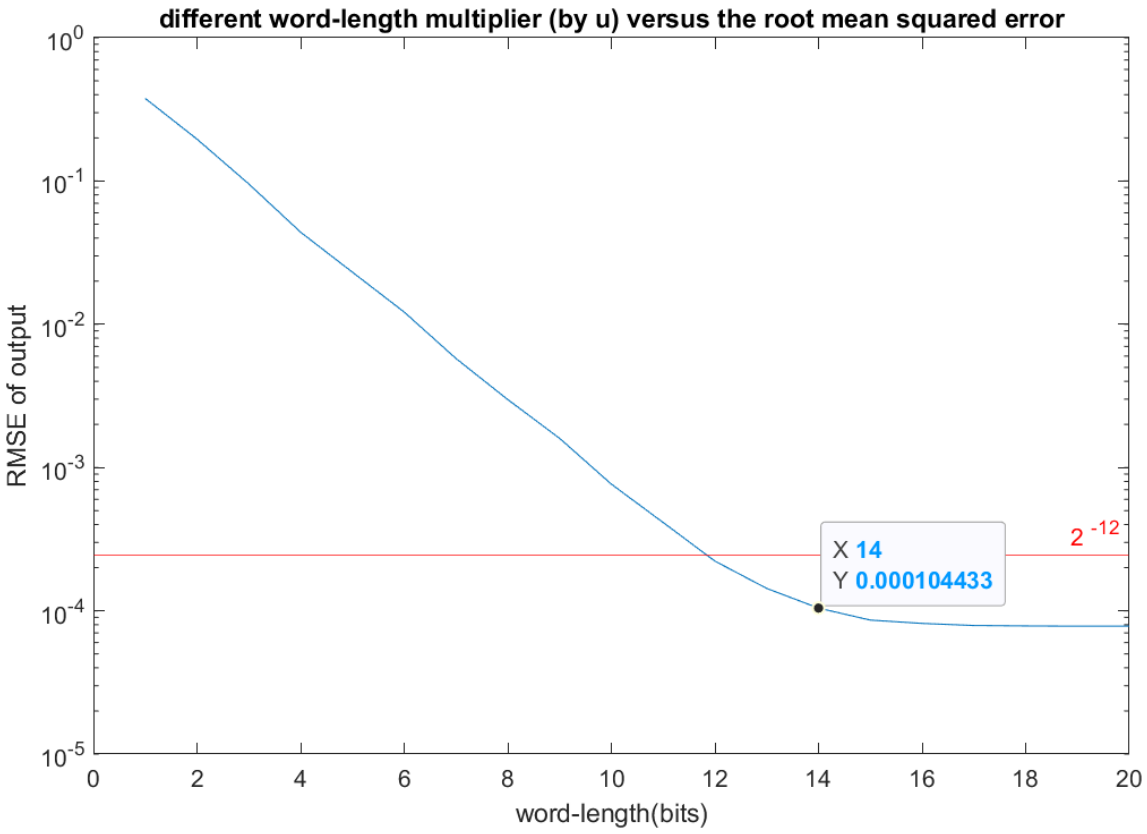
a. Wordlength of input (5%)



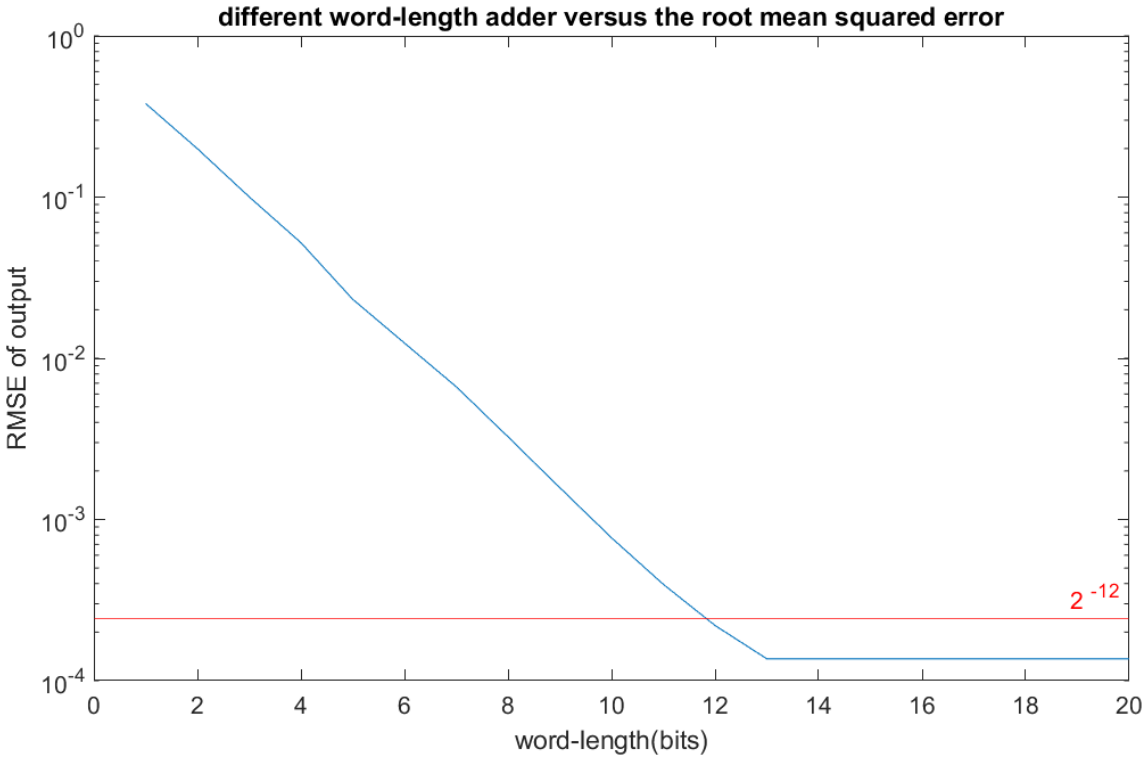
b. Wordlength of μ (5%)



c. Wordlength of multiplier (by μ) (5%)



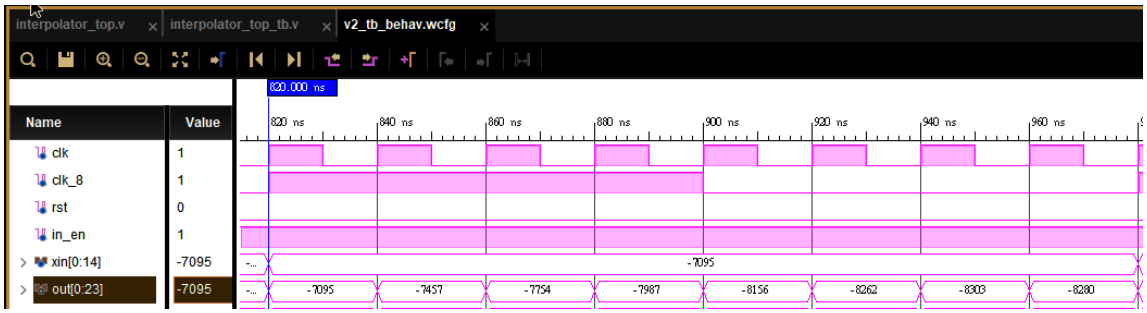
d. Wordlength of adder (5%)



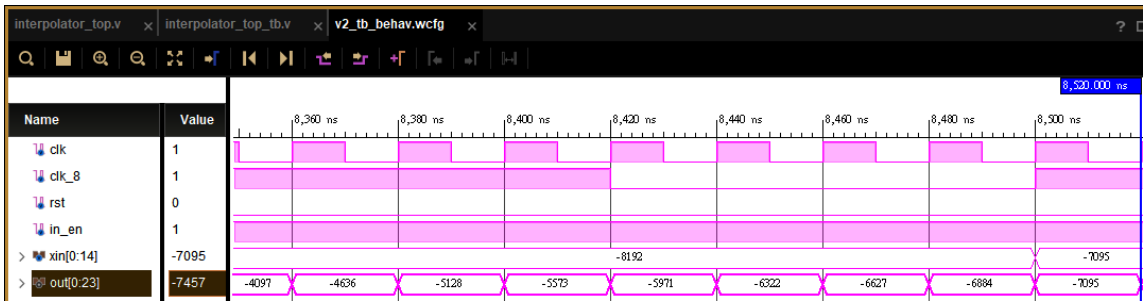
7. Design your piece-wise parabolic interpolator of Farrow structure. Please note that your input will change every 8 clock cycles and your μ value will change every clock cycle. Show the timing diagram of behavior simulation and post-route simulation results. Also depict the error between the Verilog outputs and Matlab floating-point outputs (30%)

(1) behavior simulation:

First 10 results:



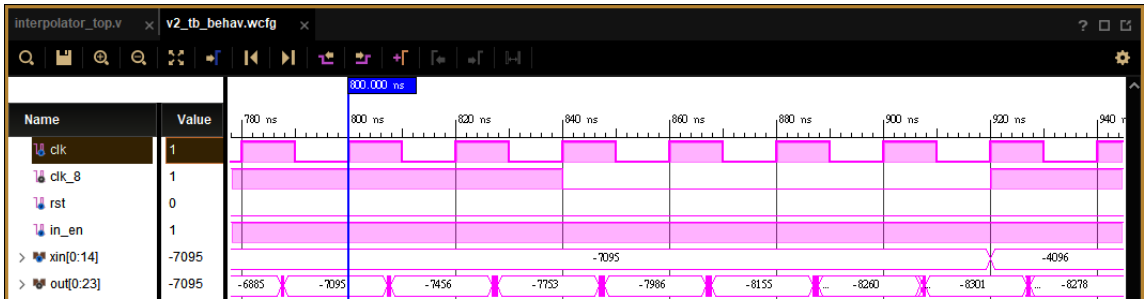
Last 10 results:

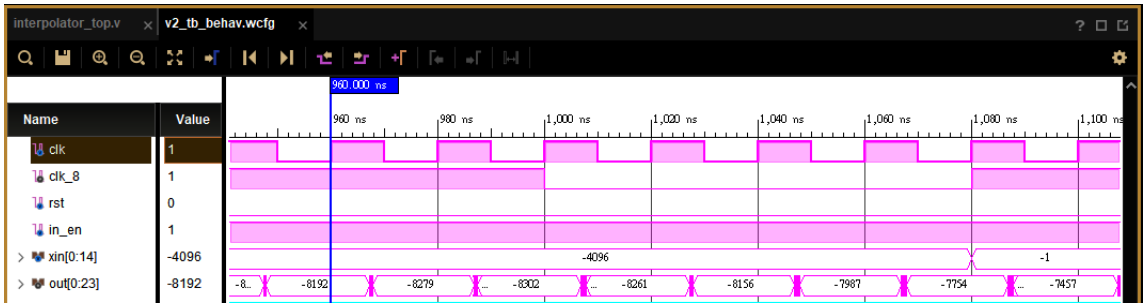


(2) post-Synthesis simulation:

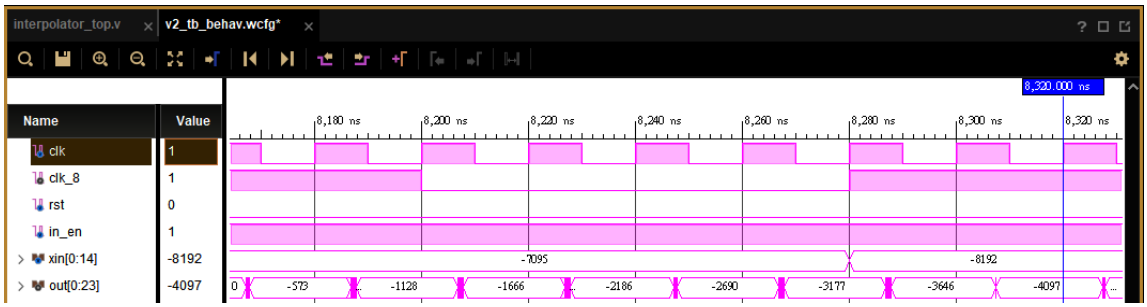
100 ns global reset:

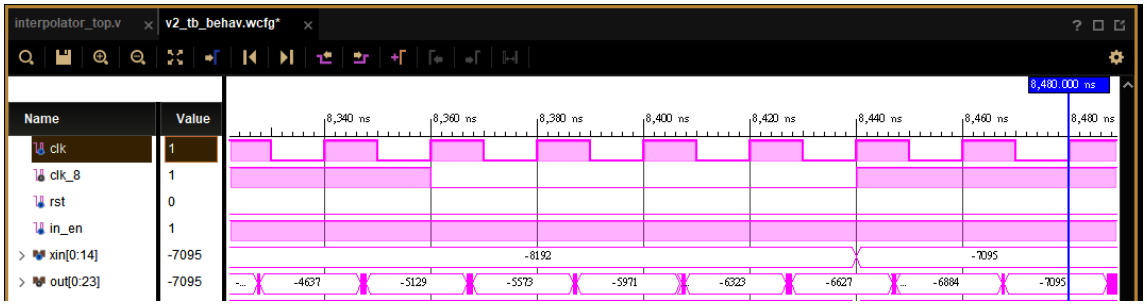
First 10 results:





Last 10 results:

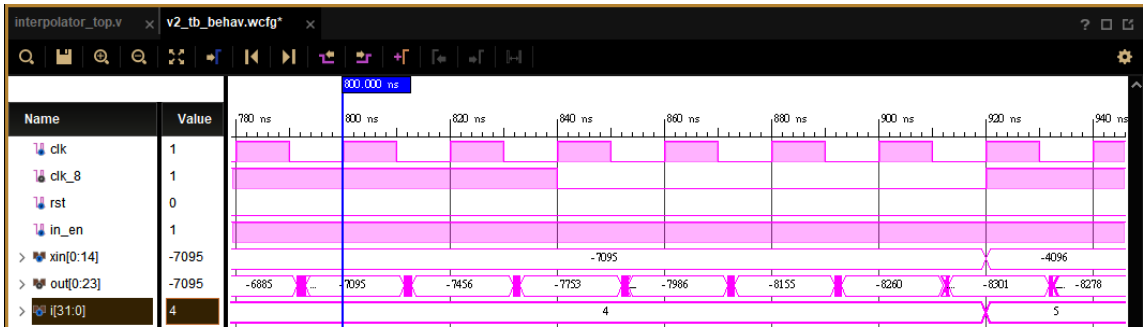




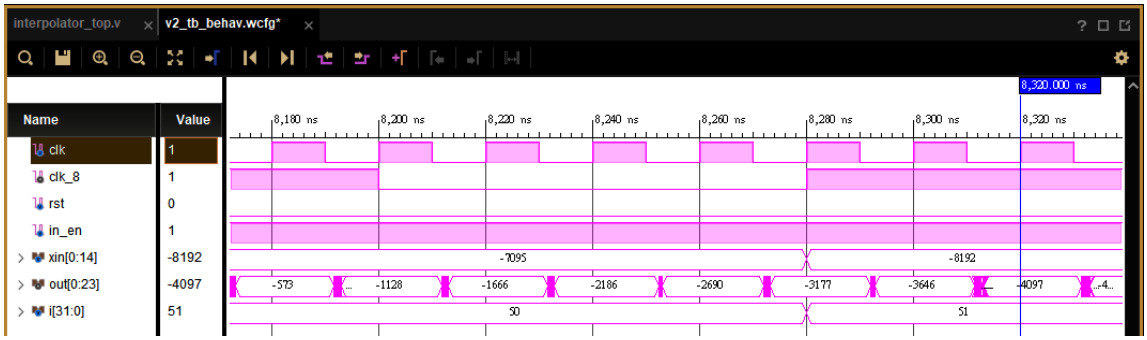
(3) post-Implementation simulation:

100 ns global reset:

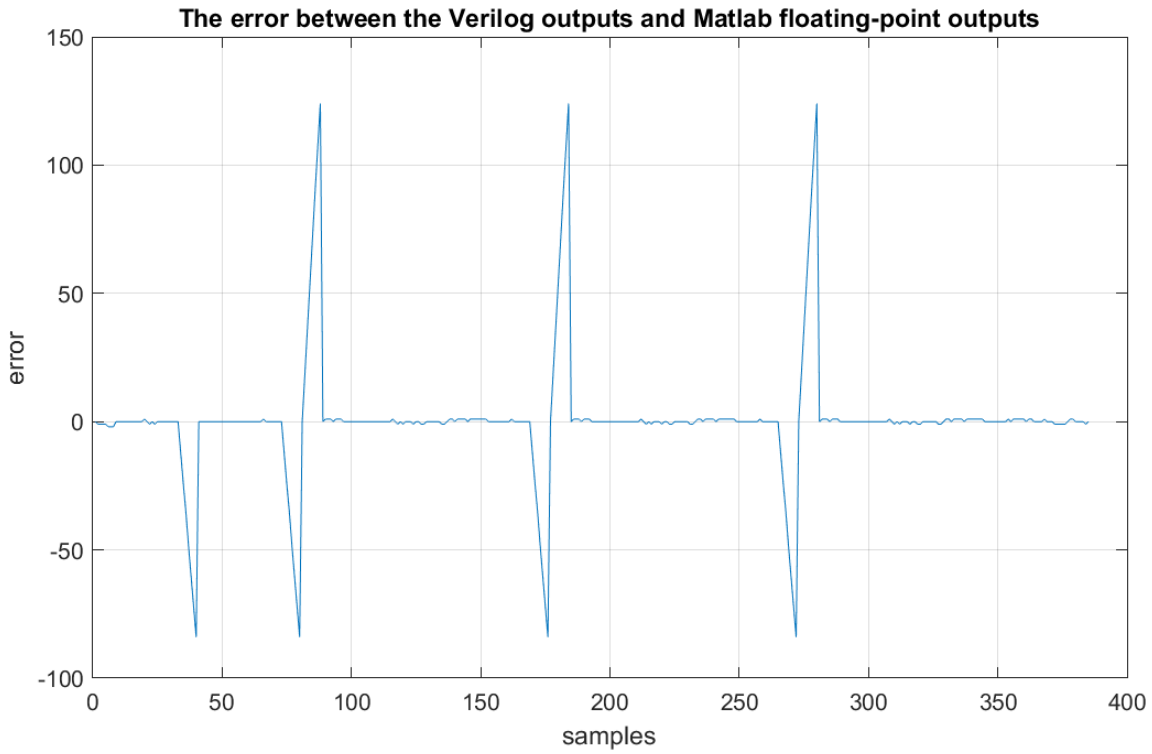
First 10 results:



Last 10 results:



(4) the error between the Verilog outputs and Matlab floating-point outputs



Matlab first 10 results:

[-7095 -7457 -7754 -7987 -8156 -8262 -8303 -8280 -8192 -8279]

Matlab last 10 results:

[-3178 -3647 -4097 -4636 -5128 -5573 -5971 -6323 -6627 -6885]

8. Show your timing report and critical path. Check if the critical path is reasonable. (10%)

Timing report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	10.376 ns	Worst Hold Slack (WHS):	0.279 ns	Worst Pulse Width Slack (WPWS):	9.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	27	Total Number of Endpoints:	27	Total Number of Endpoints:	43

All user specified timing constraints are met.

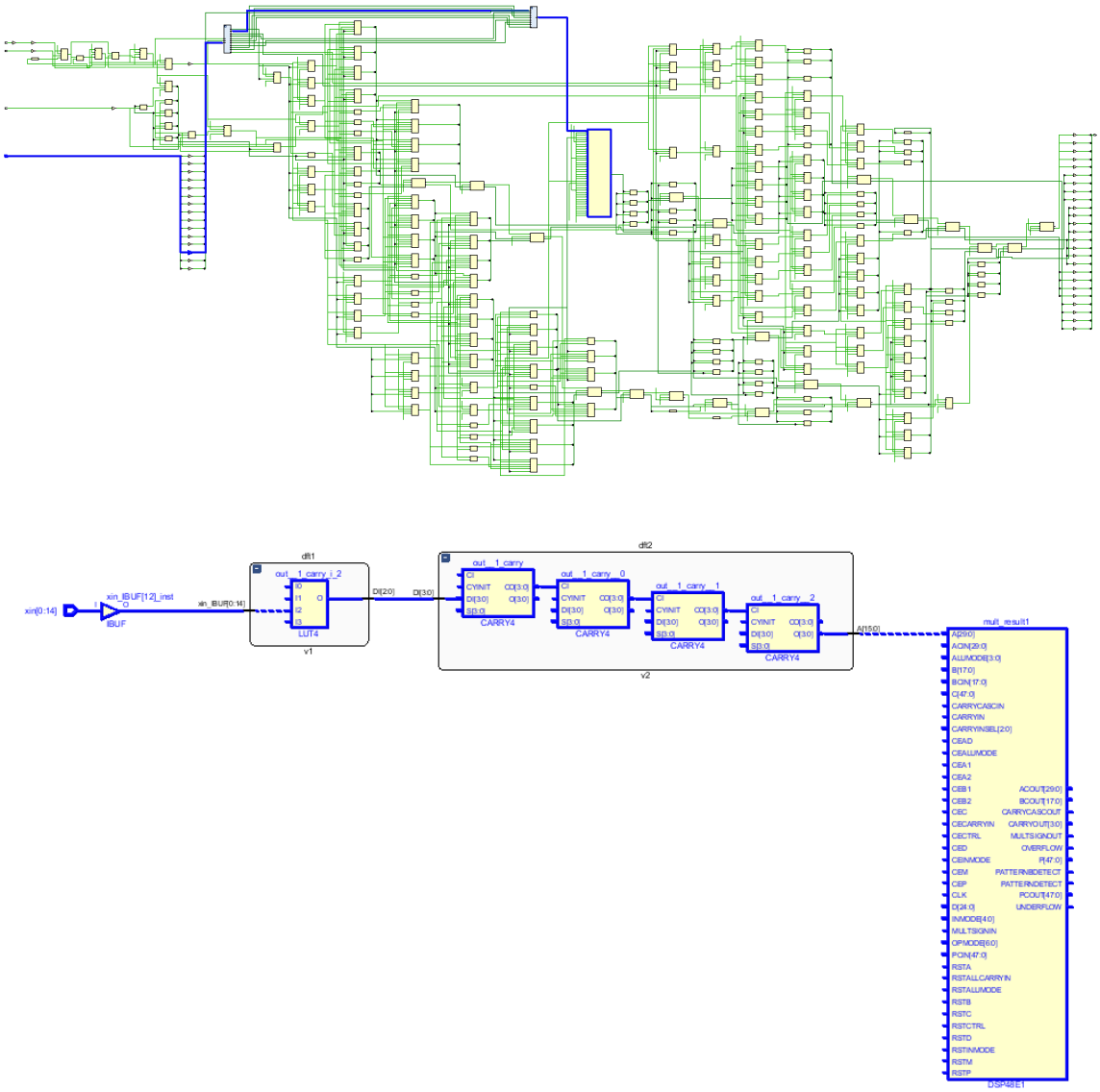
Setup time:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock	Destination Clock
Unconstrained Paths (1)														
(none) (10)														
Path 11	∞	6	6	15	xin[12]	mult_result1/A[20]	5.913	2.058	3.855	34.8	65.2	∞	input port clock	
Path 12	∞	6	6	15	xin[12]	mult_result1/A[21]	5.913	2.058	3.855	34.8	65.2	∞	input port clock	
Path 13	∞	6	6	15	xin[12]	mult_result1/A[22]	5.913	2.058	3.855	34.8	65.2	∞	input port clock	
Path 14	∞	6	6	15	xin[12]	mult_result1/A[23]	5.913	2.058	3.855	34.8	65.2	∞	input port clock	
Path 15	∞	6	6	15	xin[12]	mult_result1/A[16]	5.877	2.058	3.819	35.0	65.0	∞	input port clock	
Path 16	∞	6	6	15	xin[12]	mult_result1/A[17]	5.877	2.058	3.819	35.0	65.0	∞	input port clock	
Path 17	∞	6	6	15	xin[12]	mult_result1/A[18]	5.877	2.058	3.819	35.0	65.0	∞	input port clock	
Path 18	∞	6	6	15	xin[12]	mult_result1/A[19]	5.877	2.058	3.819	35.0	65.0	∞	input port clock	
Path 19	∞	6	6	15	xin[12]	mult_result1/A[24]	5.746	2.058	3.688	35.8	64.2	∞	input port clock	
Path 20	∞	6	6	15	xin[12]	mult_result1/A[25]	5.746	2.058	3.688	35.8	64.2	∞	input port clock	

Hold time:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock
Unconstrained Paths (1)													
(none) (10)													
Path 1	∞	3	3	13	dft1/dff_reg[1][12]/C	mult_result1/A[3]	0.915	0.315	0.600	34.4	65.6	-∞	
Path 2	∞	4	4	13	dft1/dff_reg[1][12]/C	mult_result1/A[4]	0.959	0.358	0.601	37.3	62.7	-∞	
Path 3	∞	4	4	13	dft1/dff_reg[1][12]/C	mult_result1/A[7]	0.997	0.397	0.600	39.8	60.2	-∞	
Path 4	∞	5	5	13	dft1/dff_reg[1][12]/C	mult_result1/A[8]	0.999	0.398	0.601	39.8	60.2	-∞	
Path 5	∞	4	4	13	dft1/dff_reg[1][12]/C	mult_result1/A[6]	1.025	0.371	0.654	36.2	63.8	-∞	
Path 6	∞	5	5	13	dft1/dff_reg[1][12]/C	mult_result1/A[11]	1.037	0.437	0.600	42.1	57.9	-∞	
Path 7	∞	4	4	13	dft1/dff_reg[1][12]/C	mult_result1/A[5]	1.056	0.395	0.661	37.4	62.6	-∞	
Path 8	∞	5	5	13	dft1/dff_reg[1][12]/C	mult_result1/A[10]	1.065	0.411	0.654	38.6	61.4	-∞	
Path 9	∞	5	5	13	dft1/dff_reg[1][12]/C	mult_result1/A[9]	1.096	0.435	0.661	39.7	60.3	-∞	
Path 10	∞	6	6	13	dft1/dff_reg[1][12]/C	mult_result1/A[12]	1.099	0.438	0.661	39.9	60.1	-∞	

critical path:

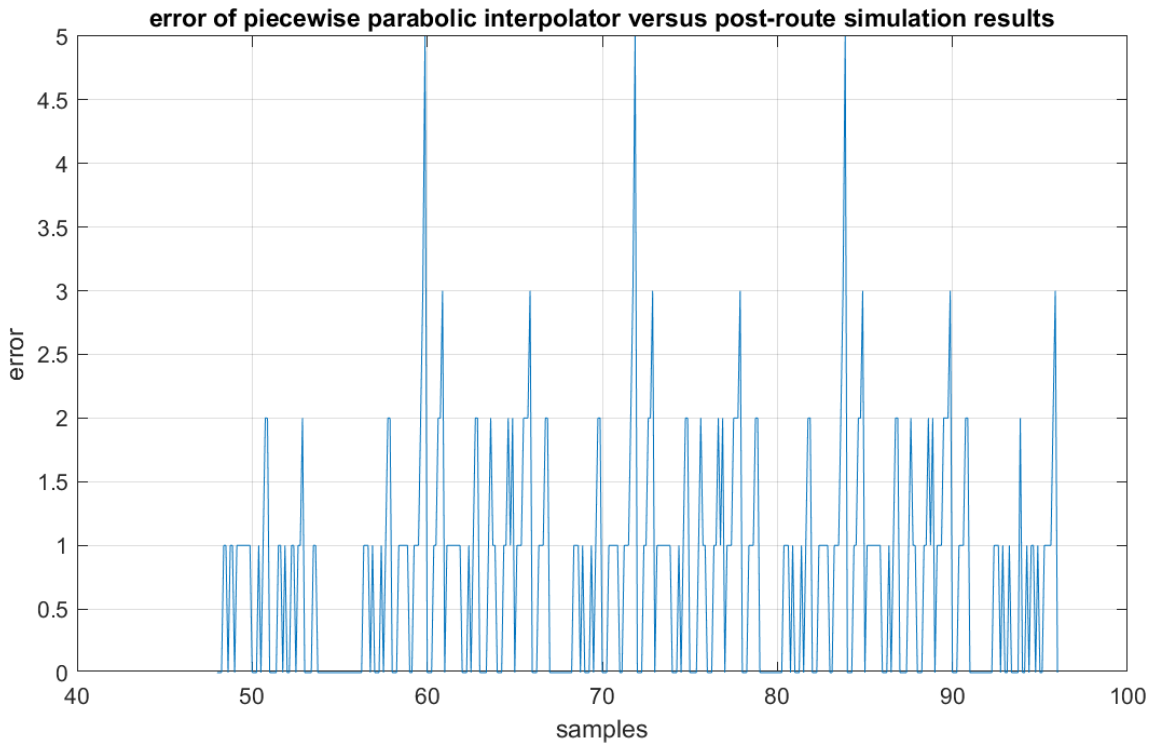


此次設計為了提高其運算速度採用了 pipeline 的設計，在 v0, v1, v2 之輸出擺上一個 latch 來減少 setup time，防止訊號走太長的路徑與經過太多運算，從而導致運算出錯。

這一路徑經過 1 次位移後分別經過了三顆加法器，最後到達與 mu 相乘的乘法器前的 latch。此一路徑作為本設計架構的 critical path 學生認為很合理。

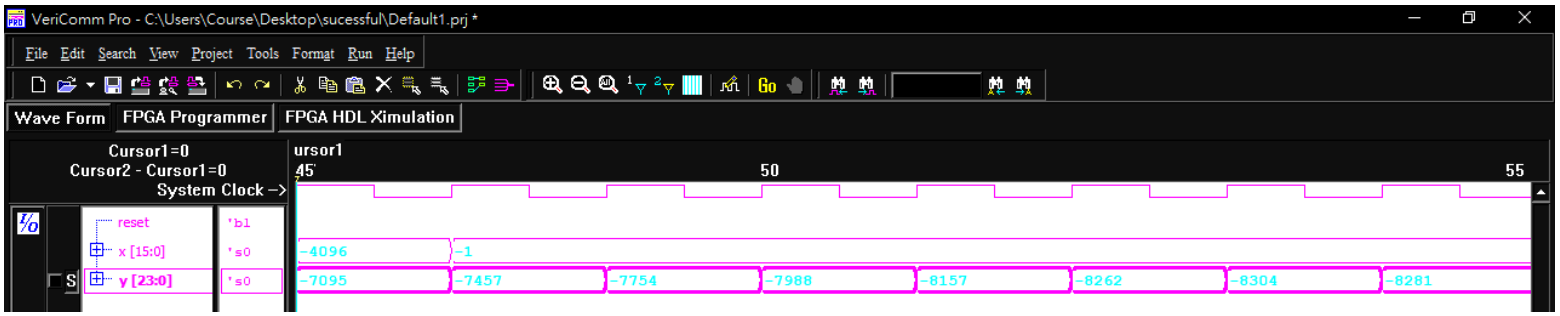
9. **Compare to the post-route simulation results (by Matlab figure.) (10%) and** show your measurement results on your hardcopy before the deadline. (10%) **(Demo to TA until 11/14. (10%))**

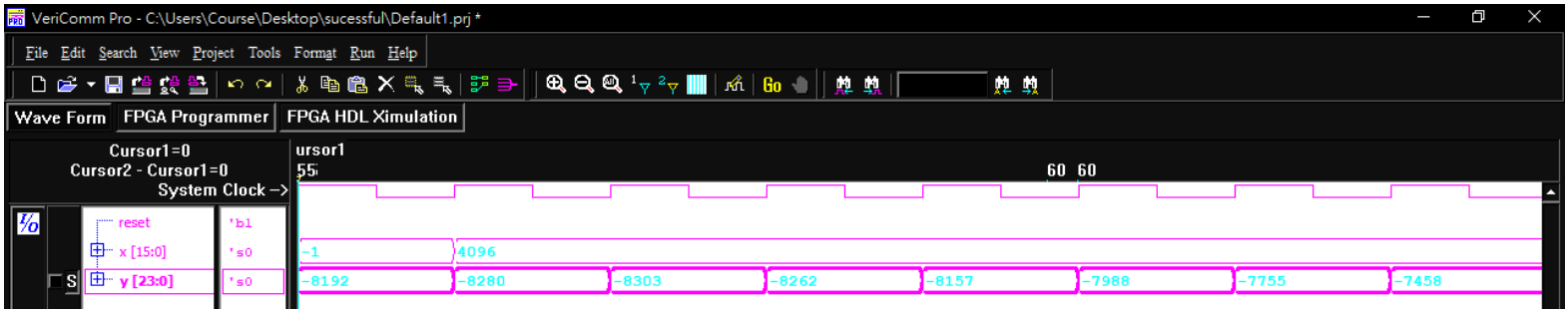
(1) Compare to the post-route simulation results (by Matlab figure.)



(2) FPGA result

First 10 result:





Last 10 result: