DCCDL LAB6

Part I

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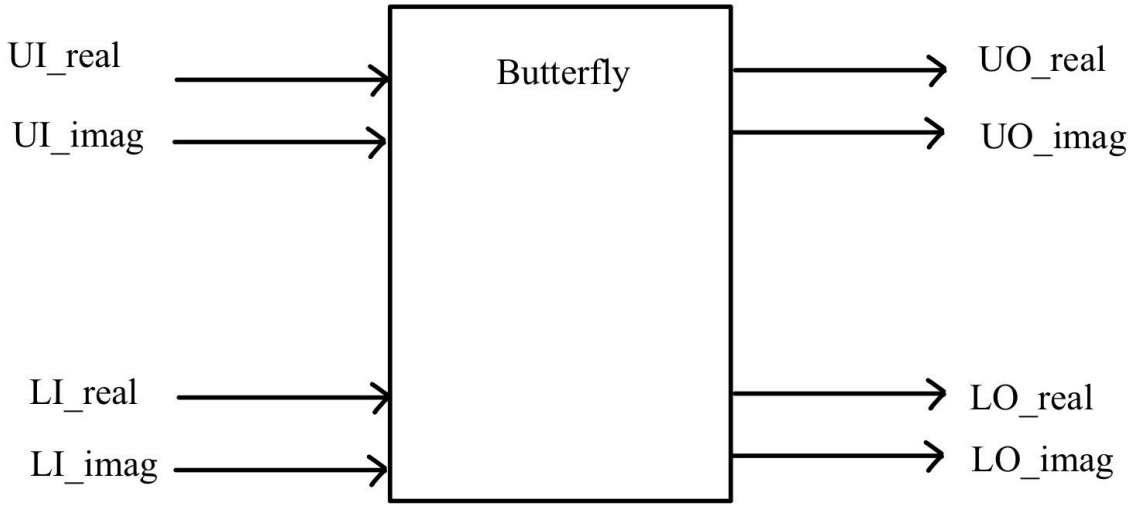
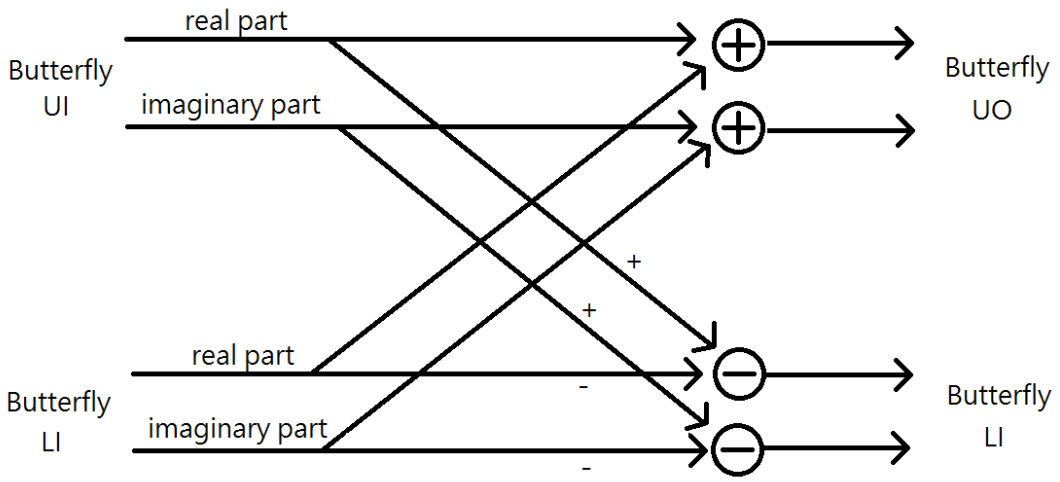
1. Draw your block diagram for the butterfly and commutator modules and explain the timing diagram of the control signals to the commutator modules at all the stages.

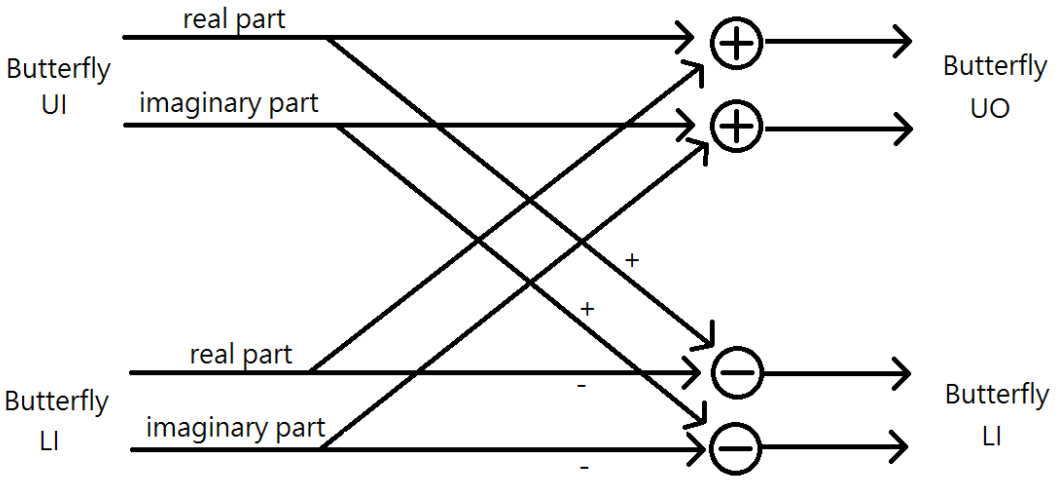
Butterfly block diagram:



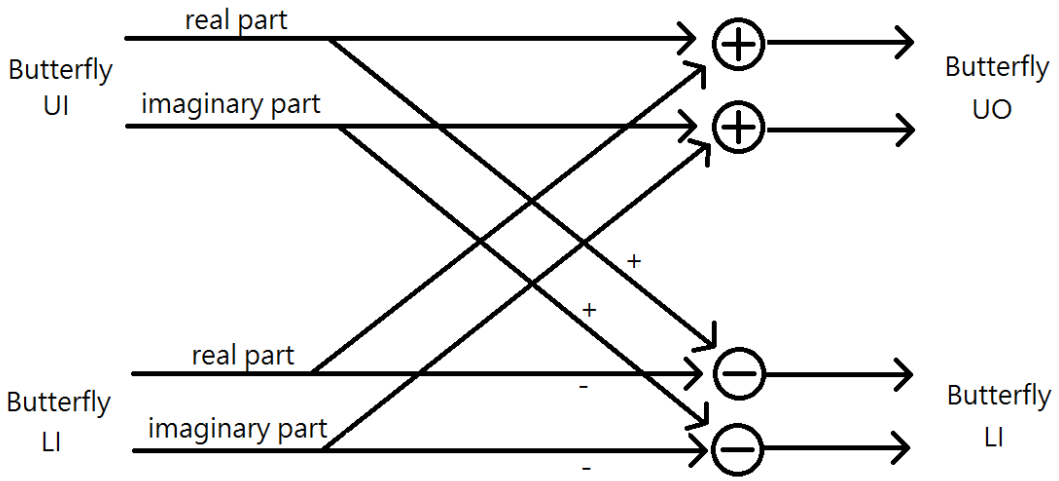
Stage1:



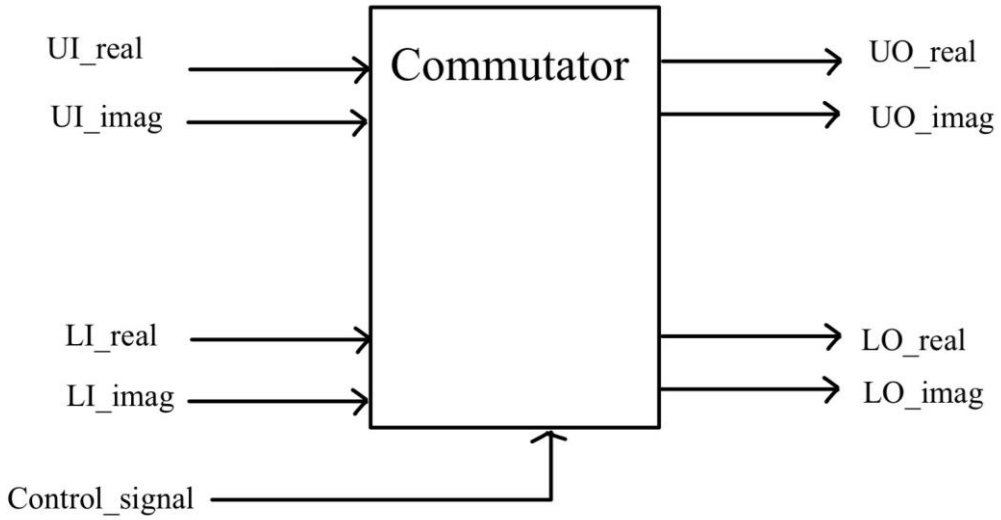
Stage2:


real part
Butterfly
UI
imaginary part
Butterfly
UO
+
+
real part
-
Butterfly
LI
imaginary part
Butterfly
LI
-

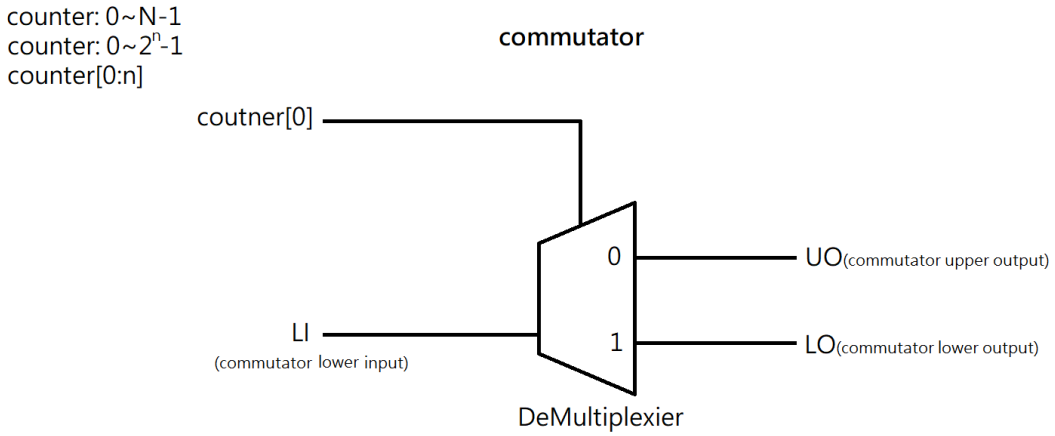
Stage3:


real part
Butterfly
UI
imaginary part
Butterfly
UO
+
+
real part
-
Butterfly
LI
imaginary part
Butterfly
LI
-

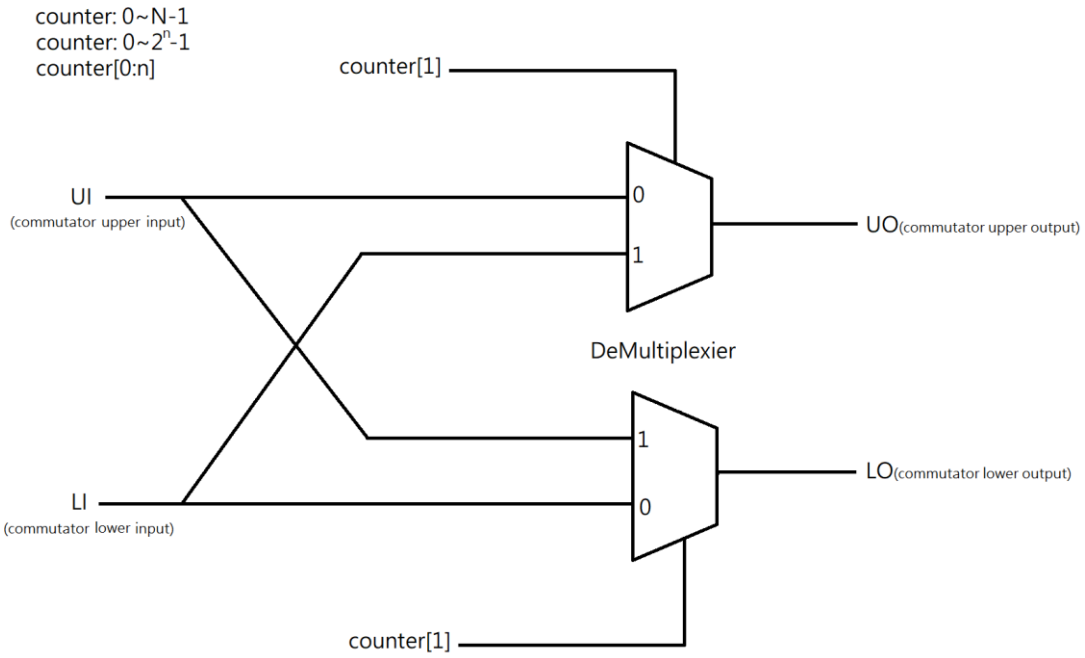
Commutator block diagram:



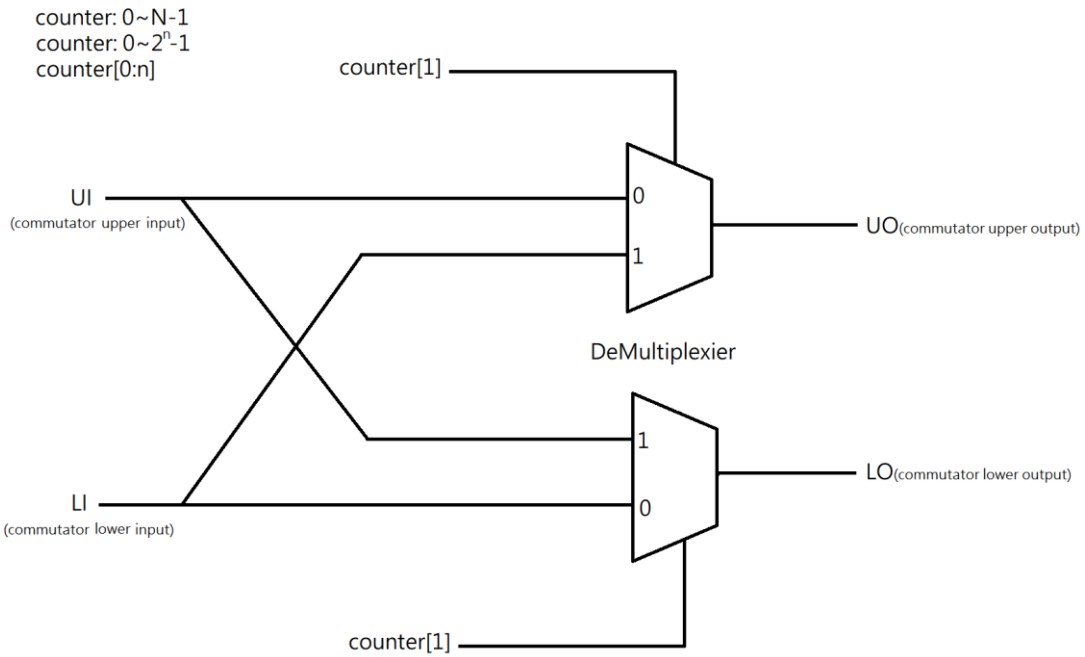
Stage1:



Stage2:

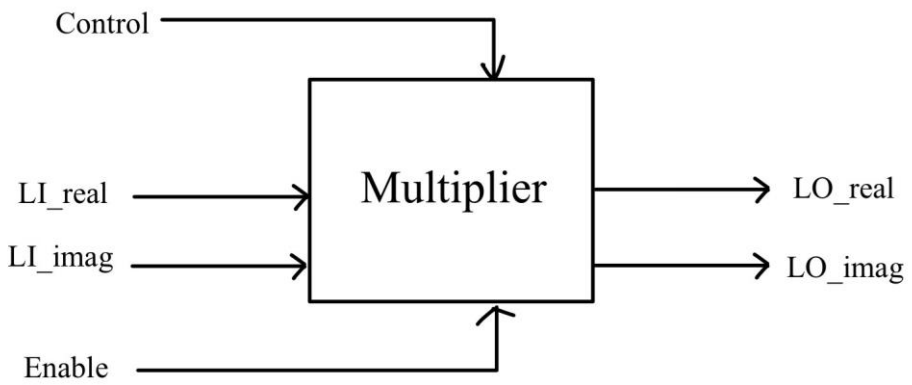


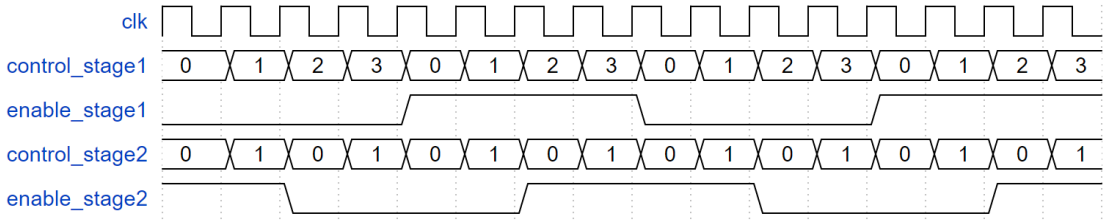
Stage3:


counter: 0~N-1
counter: 0~2^n-1
counter[0:n]
counter[1]
UI
(commutator upper input)
0
1
UO(commutator upper output)
DeMultiplexier
1
0
LO(commutator lower output)
LI
(commutator lower input)
counter[1]

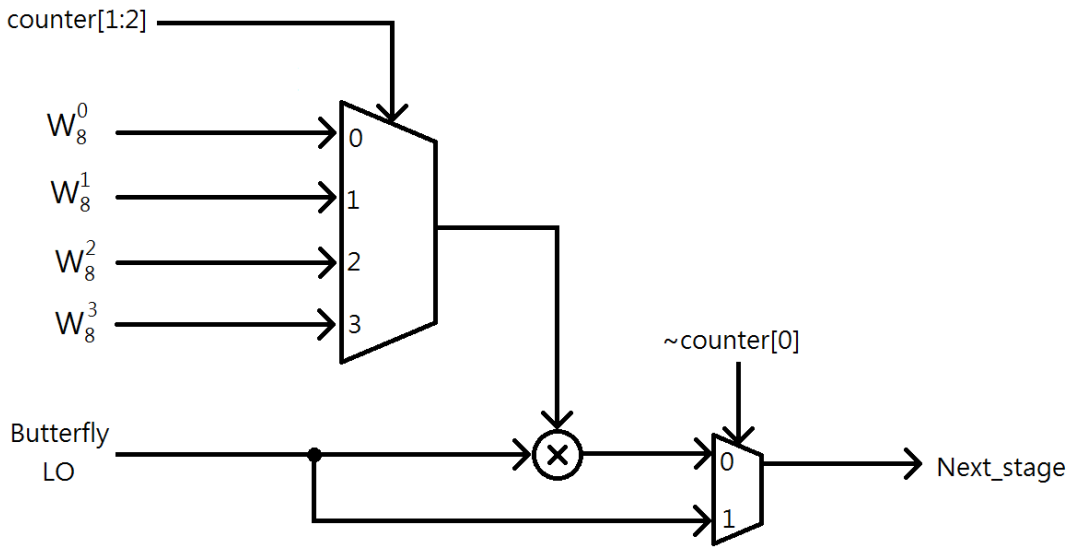
2. Draw the timing diagram of the control signals to the complex multiplier blocks at all the stages.

Multiplier block diagram:

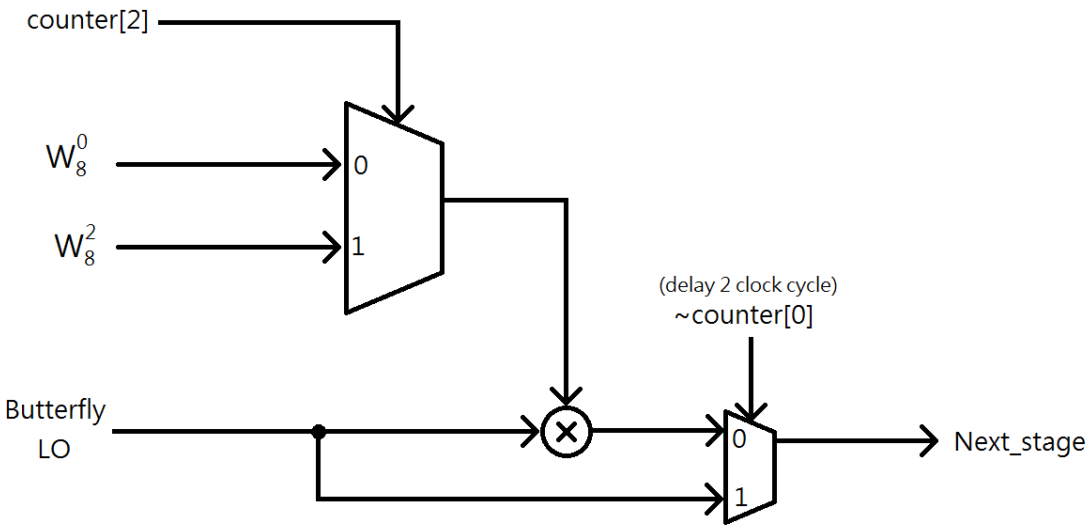




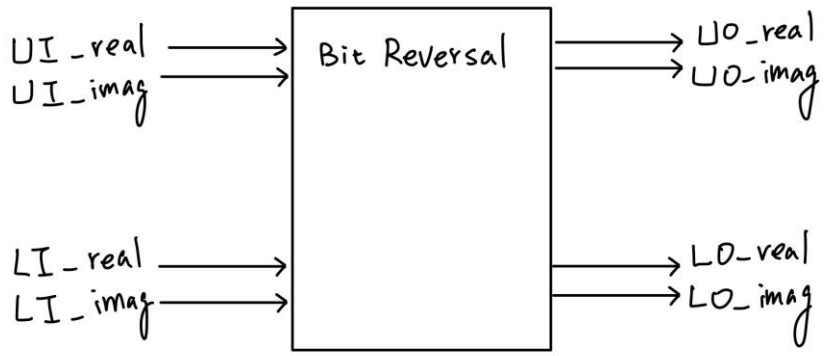
Stage1:

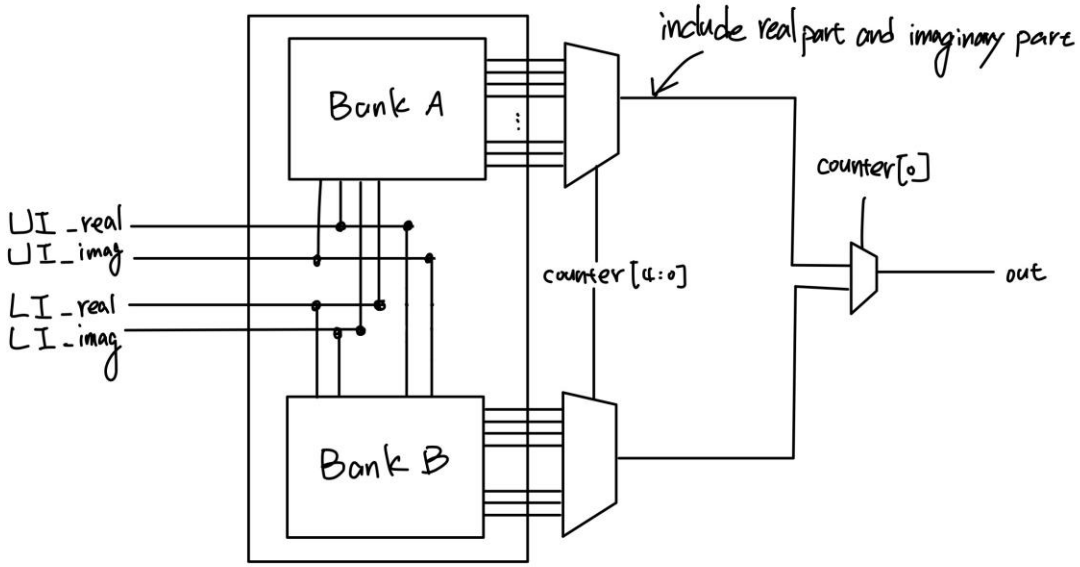


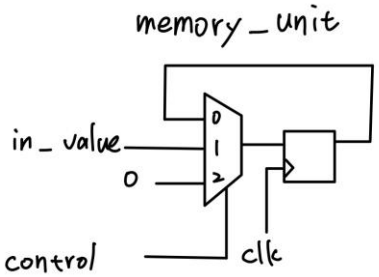
Stage2:


counter[2]
W_8^0
W_8^2
0
1
(delay 2 clock cycle)
~counter[0]
Butterfly
LO
0
1
Next_stage

3. Show your design for bit-reversal module to allow the frequency-domain samples appearing in order.

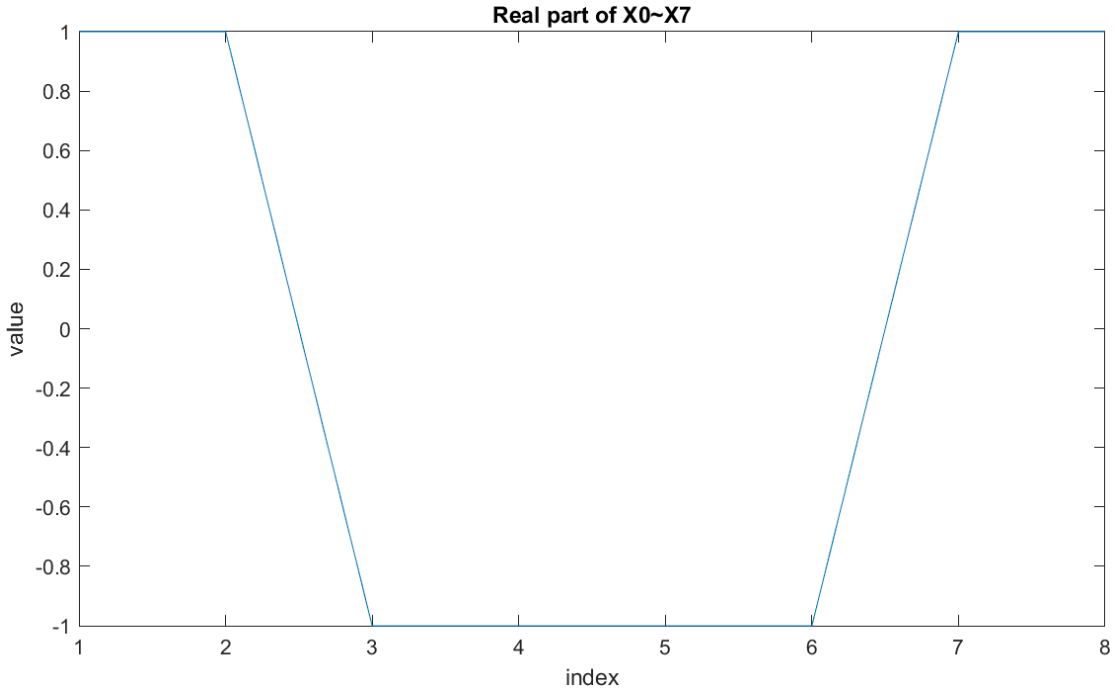


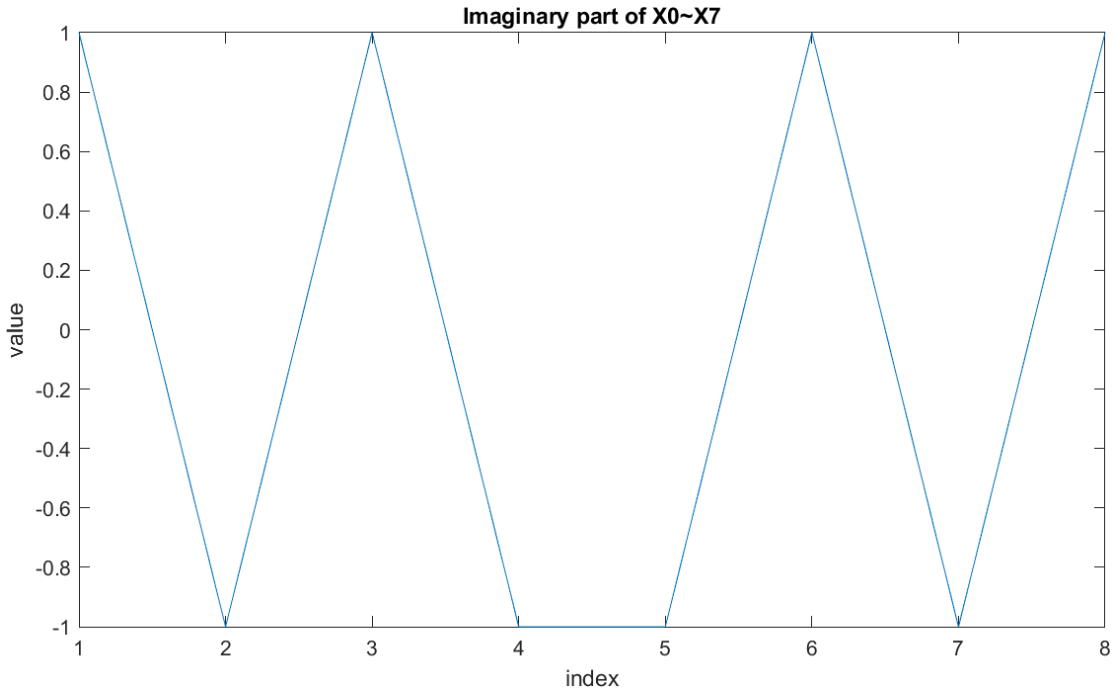


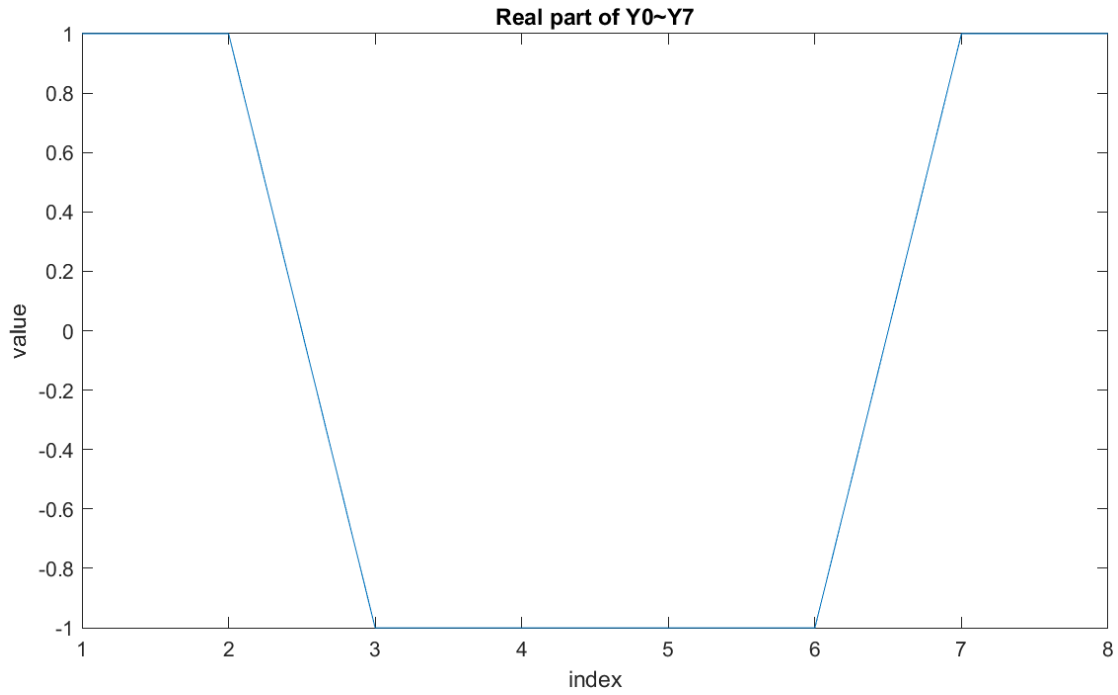


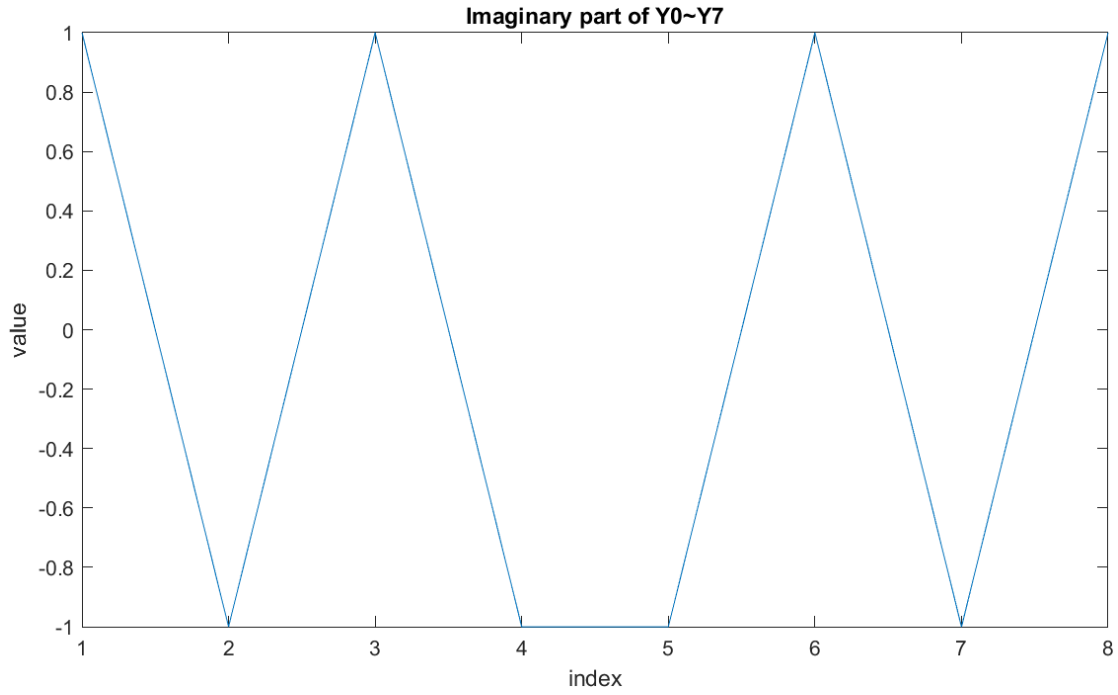
rst	write_en	control
1	X	0
0	1	1
0	0	0

4. Use Matlab program to implement 8-point MDC FFT architecture and the bit-reversal module. Draw the real-part and imaginary-part of $X_0 \sim X_7$. Compare them with the real-part and imaginary-part of $Y_0 \sim Y_7$. Depict the error.



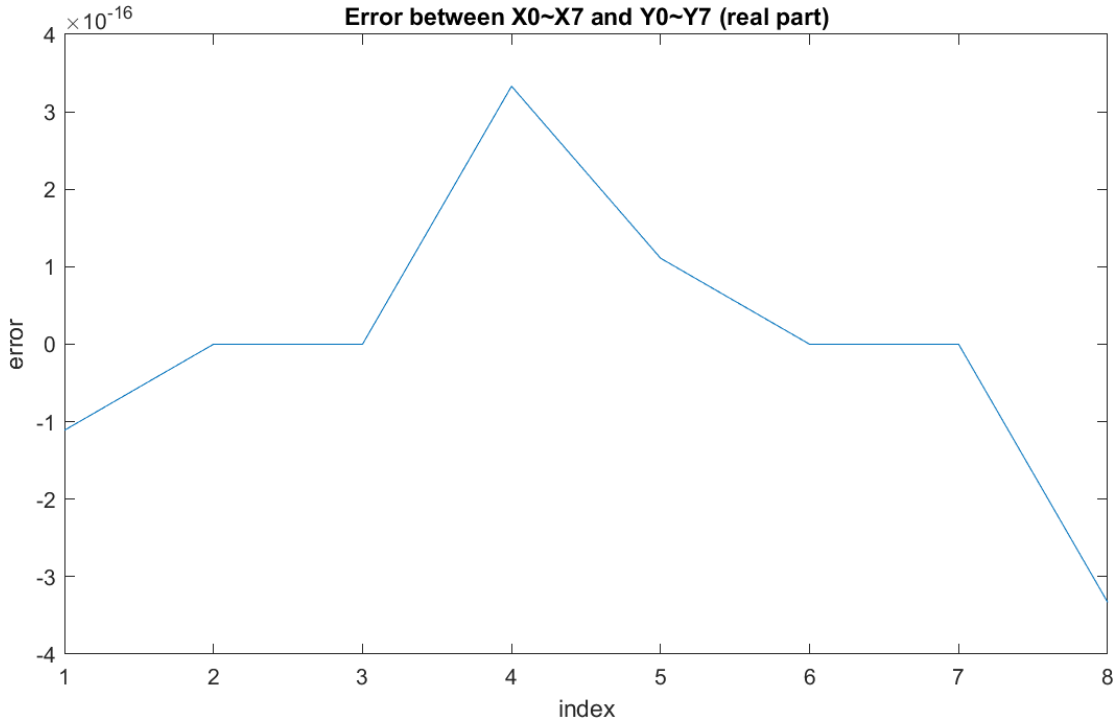



Real part of Y0~Y7
value
index
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
1
2
3
4
5
6
7
8

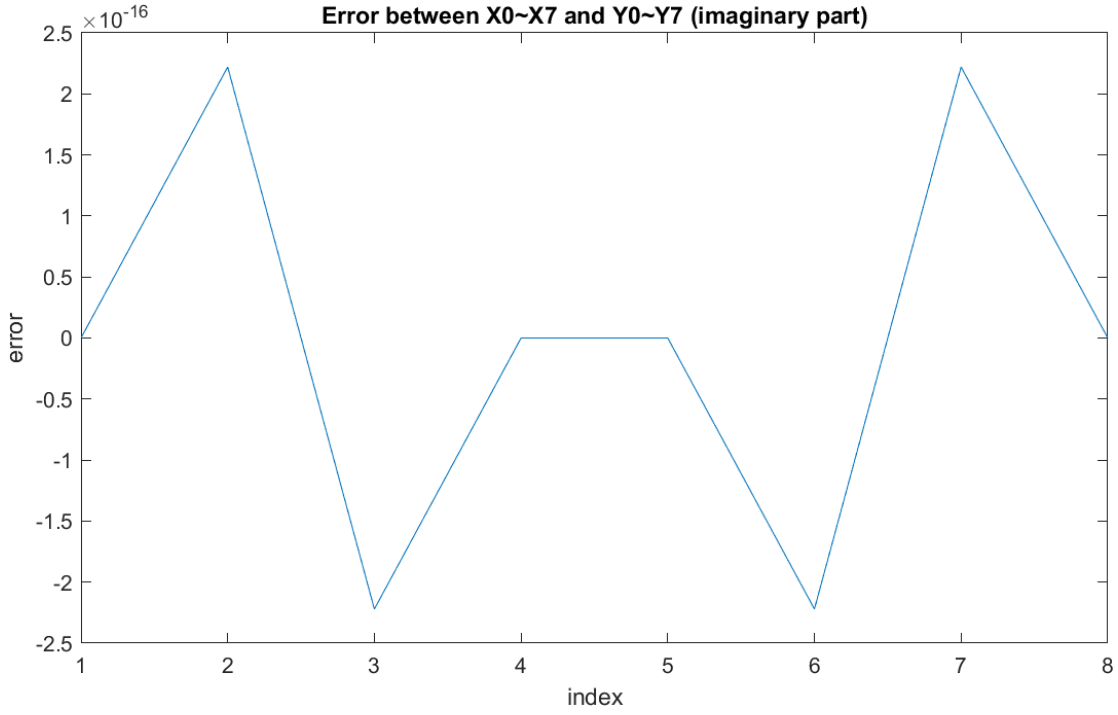

Imaginary part of Y0~Y7
value
index
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
1
2
3
4
5
6
7
8

Error between X0~X7 and Y0~Y7

Real part:

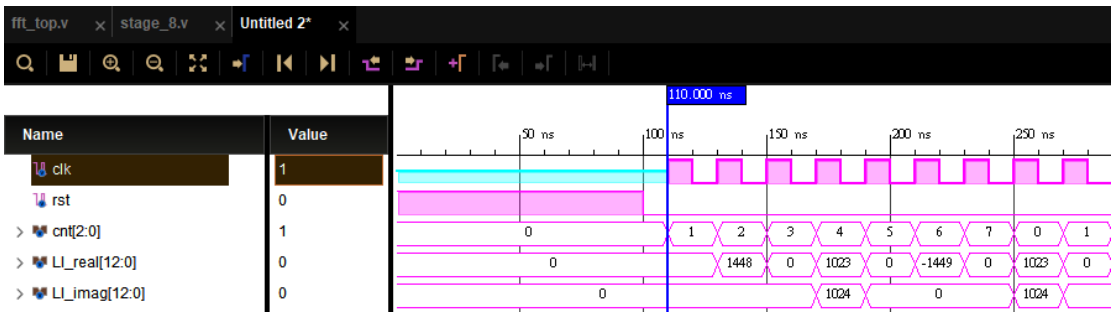


Imaginary part



5. Show the timing diagram of your Verilog behavior and post-route simulation results of 8-point MDC FFT. Compare with the Matlab results to check your implementation error. Depict the error of the real part and imaginary part of each point using figures.

Behavior timing diagram:



Matlab Input:

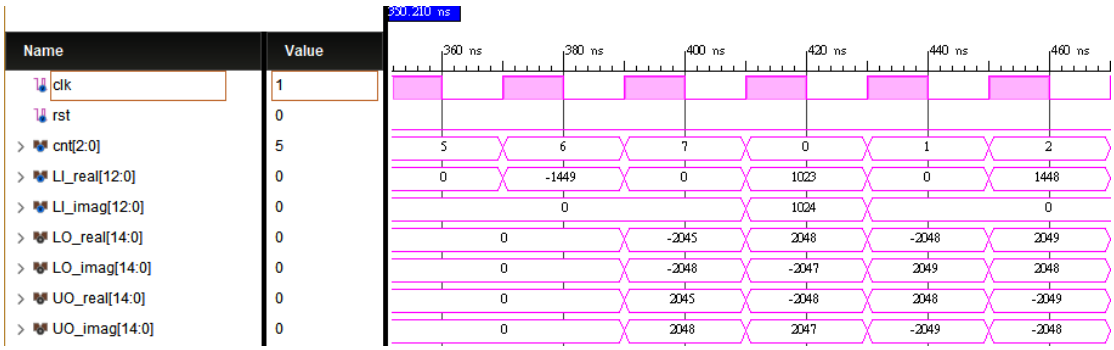
Real part:

[0 1448 0 1023 0 -1449 0 1023 0]

Imaginary part:

[0 0 0 1024 0 0 0 1024 0]

Output before ping-pong access:



Matlab Output:

UO_real :

[2045 -2048 2048 -2049]

UO_imag:

[2048 2047 -2049 -2048]

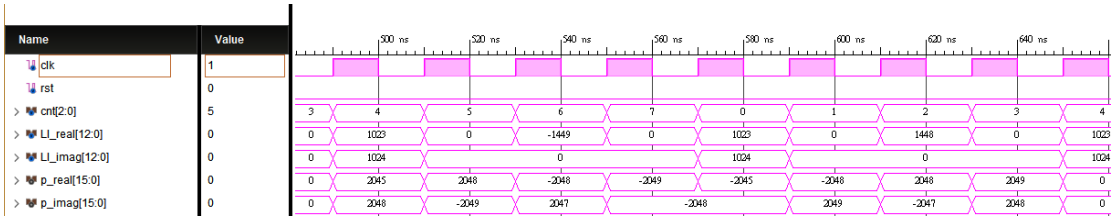
LO_real:

[-2045 2048 -2048 2049]

LO_imag:

[-2048 -2047 2049 2048]

Output after ping-pong access:



Matlab Output:

Real part

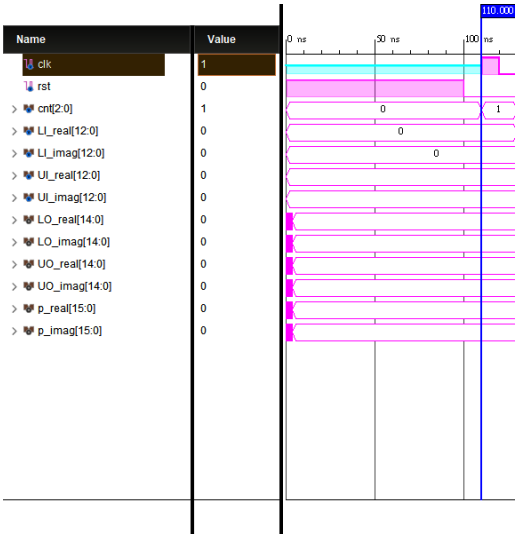
[2045 2048 -2048 -2049 -2045 -2048 2048 2049]

Imaginary part

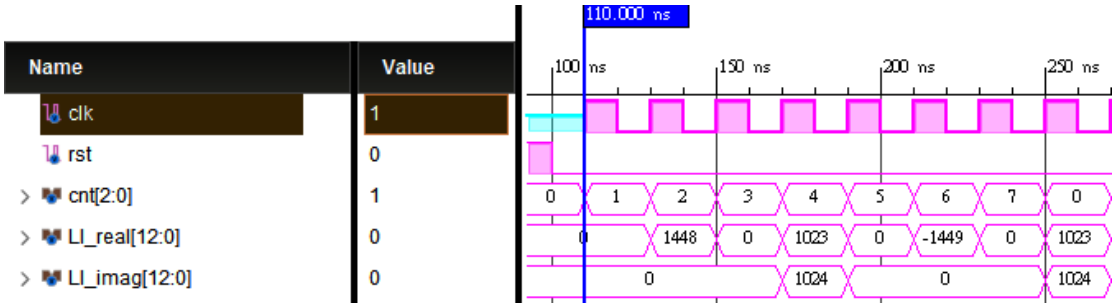
[2048 -2049 2047 -2049 -2048 2049 -2047 2048]

Synthesis timing diagram:

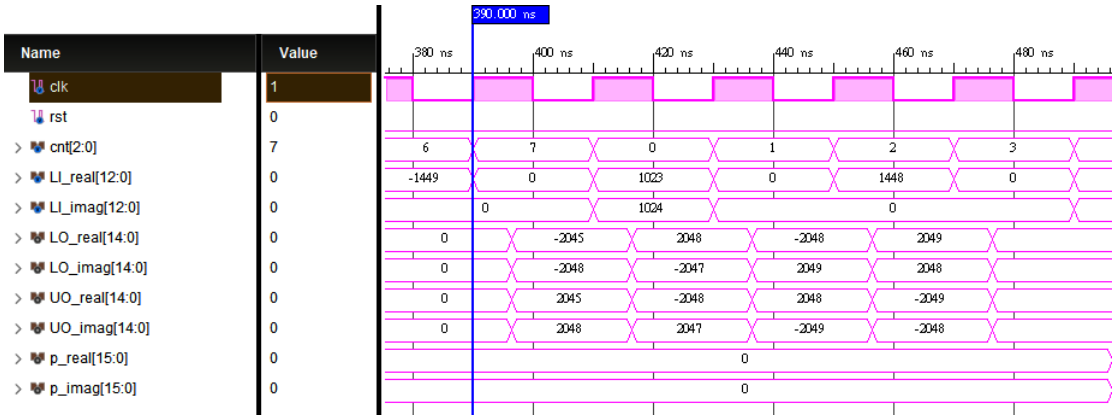
Global reset:



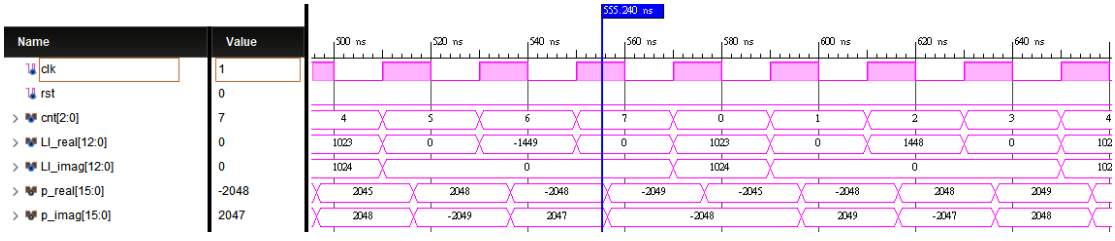
Input:



Output before ping-pong access:

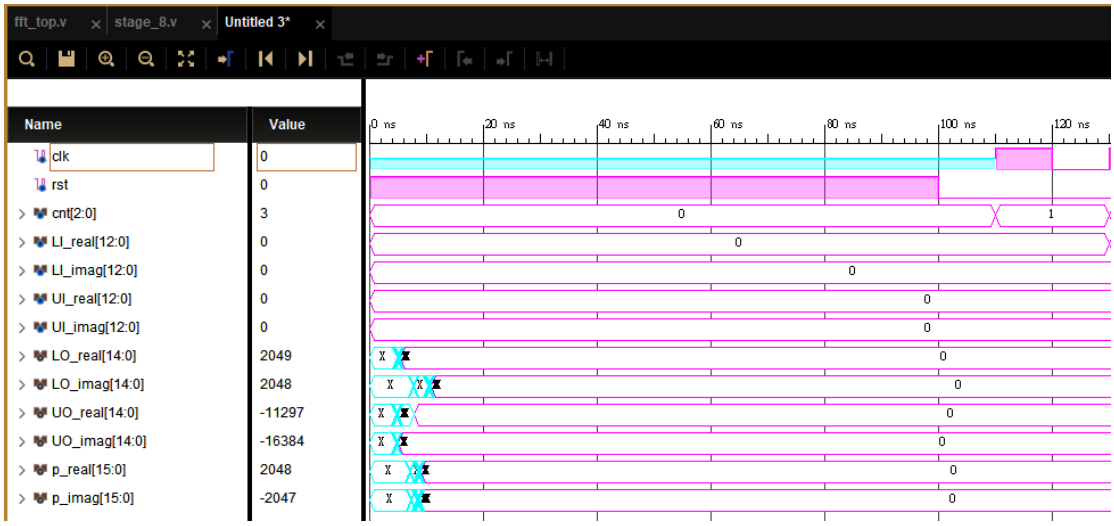


Output after ping-pong access:

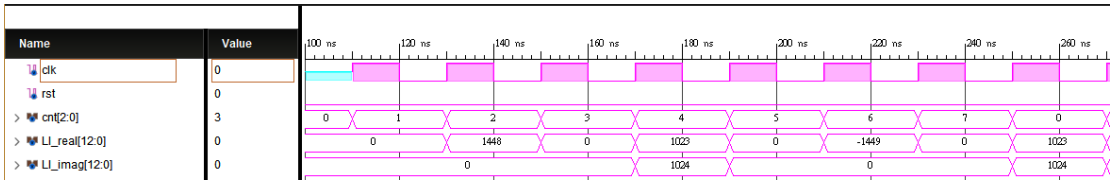


Implementation timing diagram:

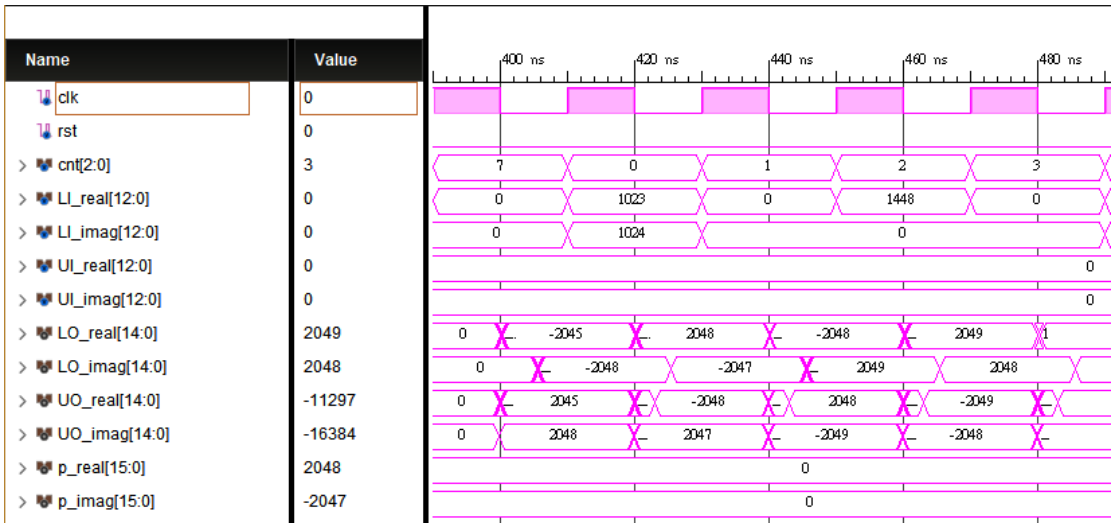
Global reset:



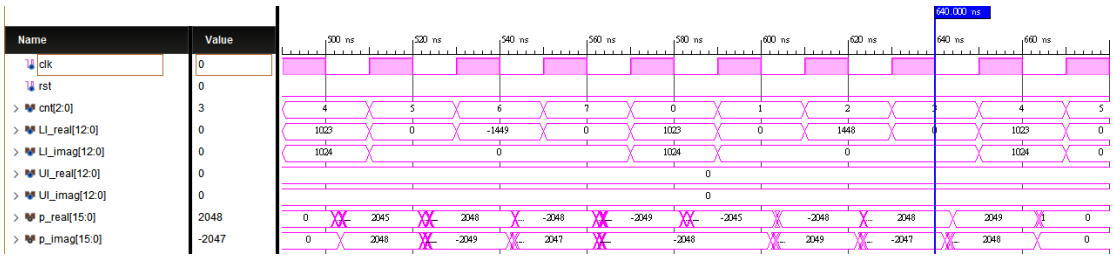
Input:

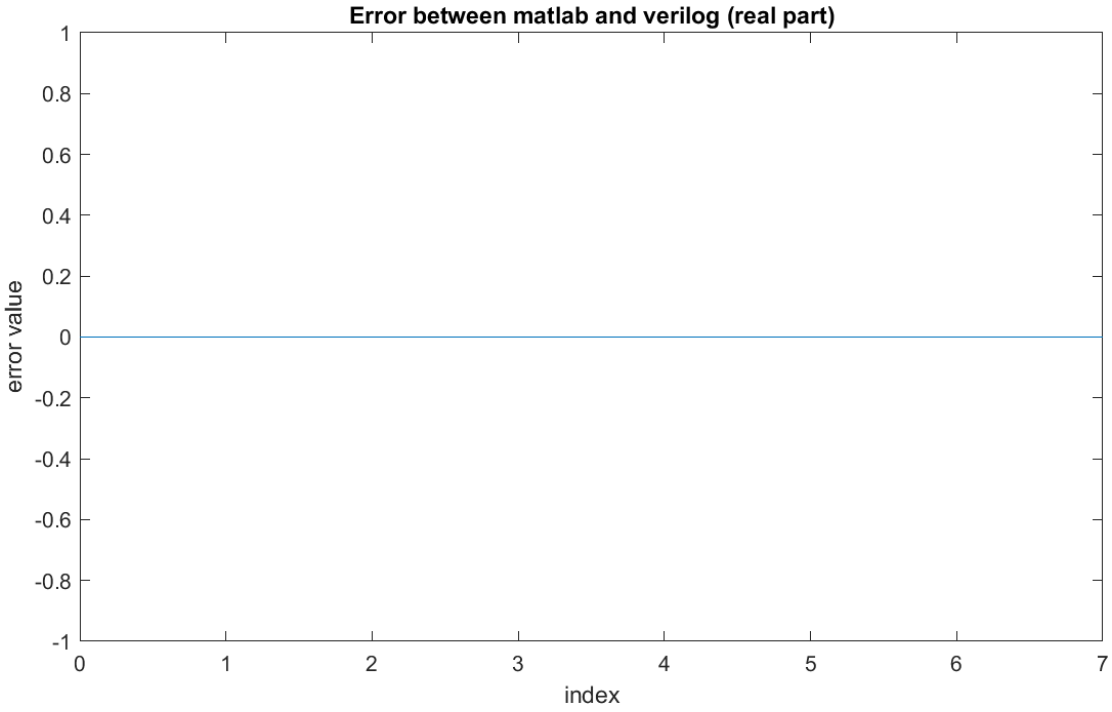


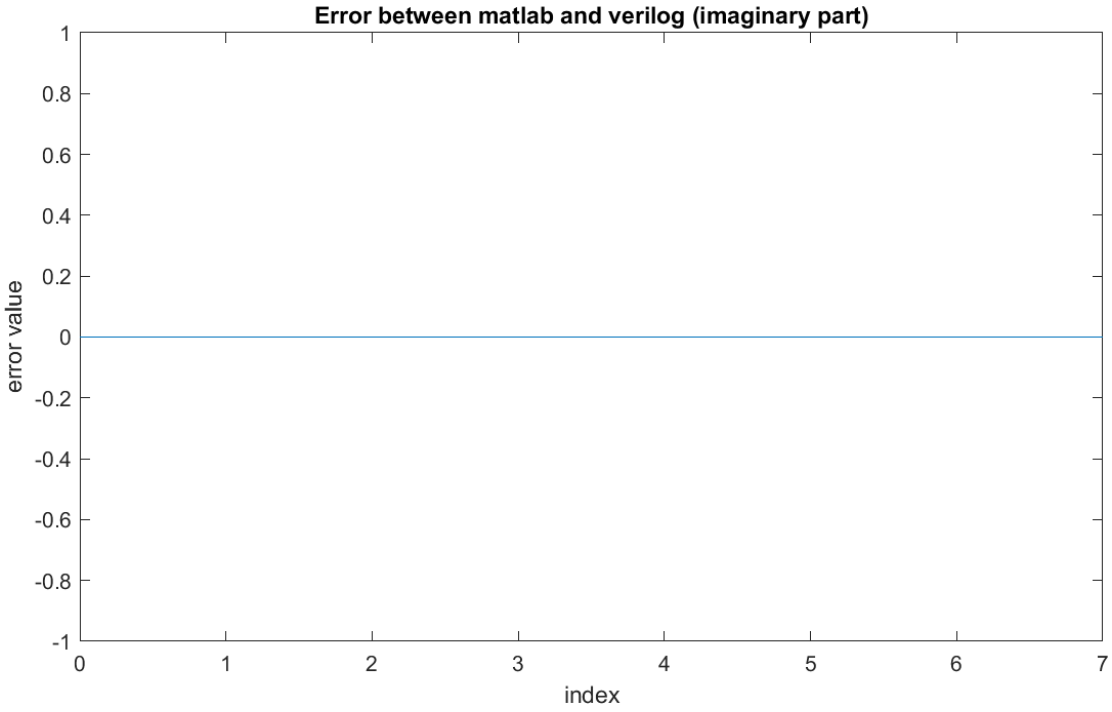
Output before ping-pong access:



Output after ping-pong access:




Error between matlab and verilog (real part)
error value
index
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
1
2
3
4
5
6
7


Error between matlab and verilog (imaginary part)
error value
index
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
1
2
3
4
5
6
7