**DCCDL LAB2**

**Verilog**

電機碩一 111521035 林豪澤

6. Show the Verilog behavior simulation results and post-route simulations results. (20%)

7. Show the Verilog behavior simulation results and post-route simulation results of every layer. (20%)

8. Show the Verilog behavior simulation results and post-route simulation results. (20%)

9. Show the Verilog behavior simulation results and post-route simulation results. (20%)

10. Show your timing report and draw the critical path from the max delay timing report of the block designed in Q6 and Q8 of Procedure. (20%)