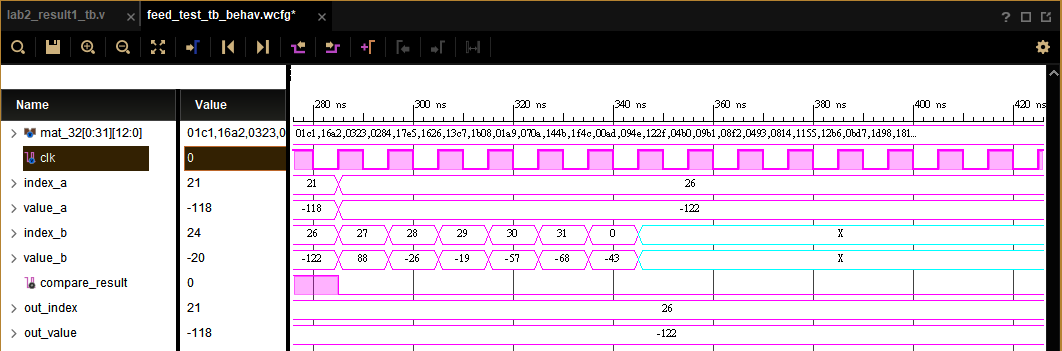
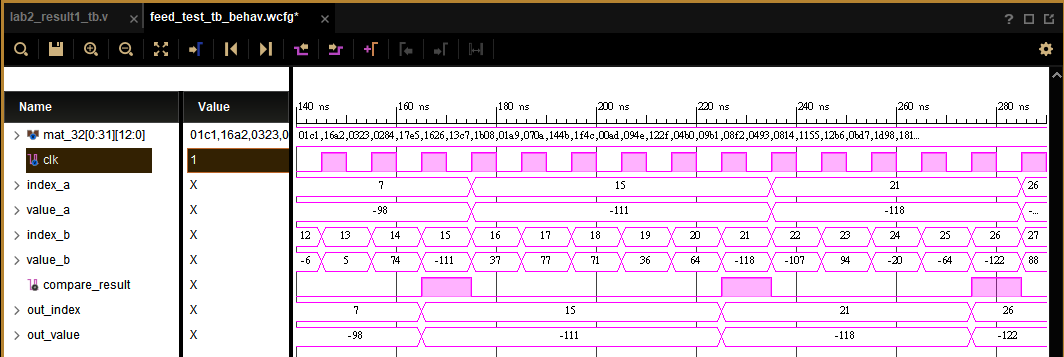
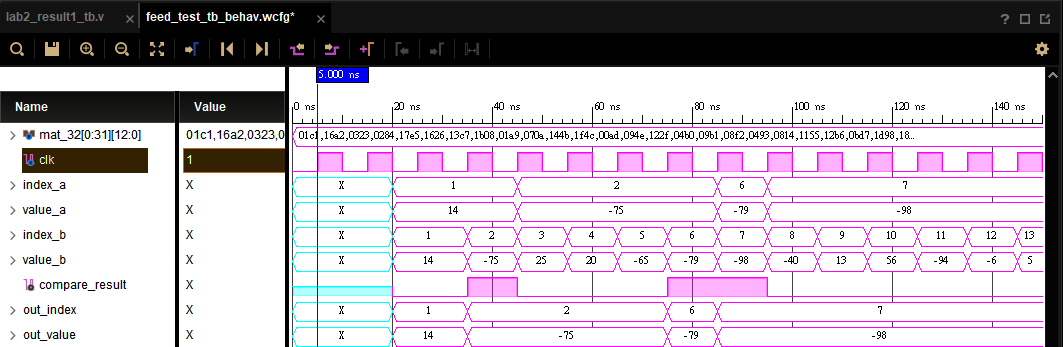
**DCCDL LAB2**

**Verilog**

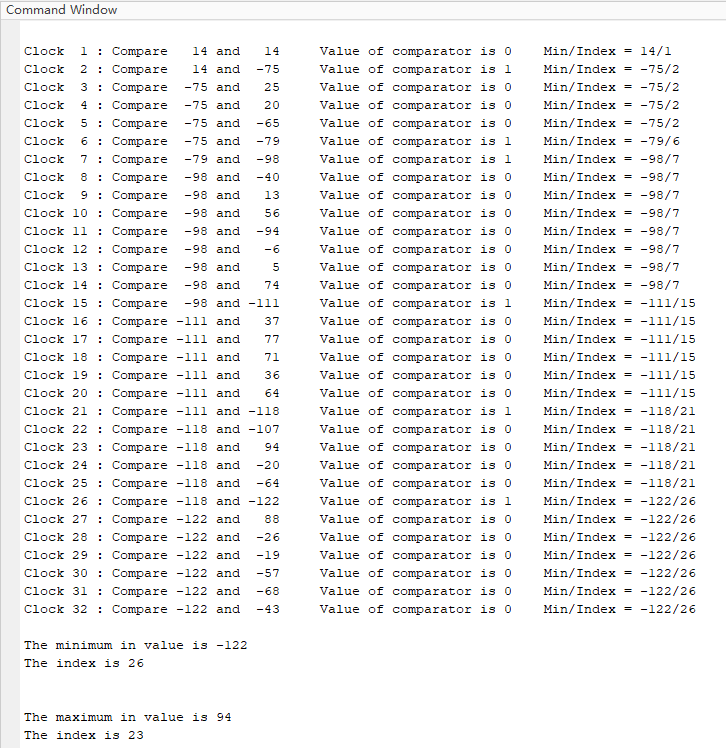
電機碩一 111521035 林豪澤

6. Show the Verilog behavior simulation results and post-route simulations results. (20%)

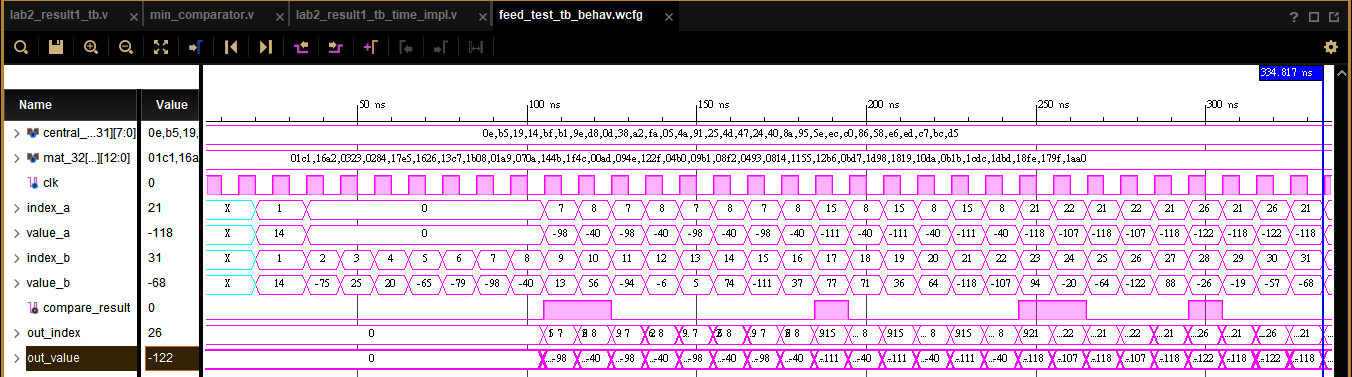
Behavior simulation results:



Serial compare results from matlab:

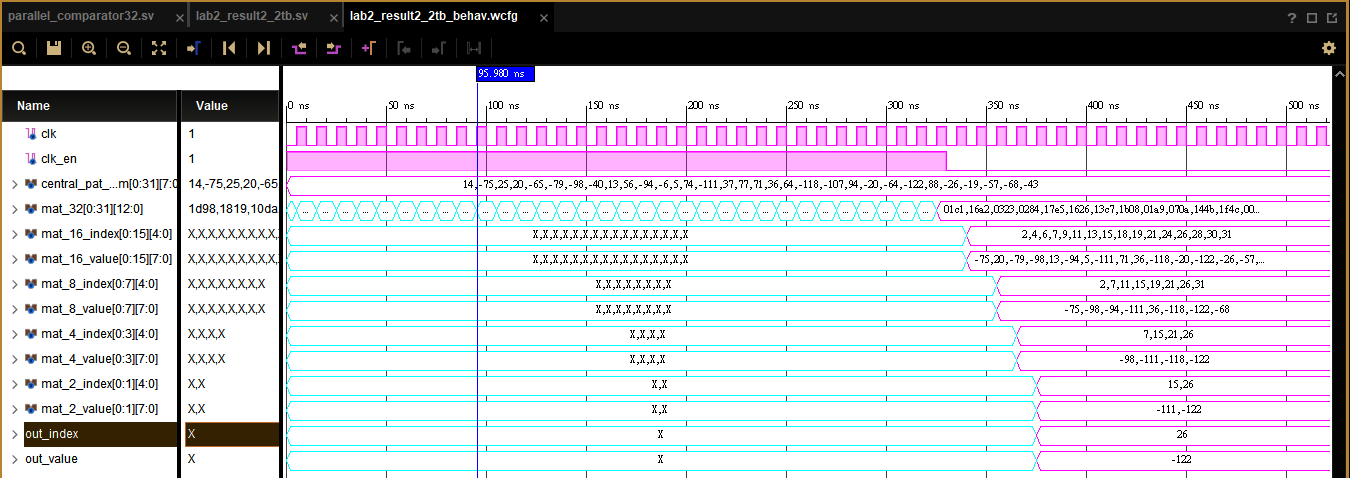


post-route simulation results :



7. Show the Verilog behavior simulation results and post-route simulation results of every layer. (20%)

Behavior simulation results:



First layer [-75/02 20/04 -79/06 -98/07 13/09 -94/11 5/13 -111/15

71/18 36/19 -118/21 -20/24 -122/26 -26/28 -57/30 -68/31]

Second layer [-75/02 -98/07 -94/11 -111/15 36/19 -118/21 -122/26 -68/31]

Third layer [-98/07 -111/15 -118/21 -122/26]

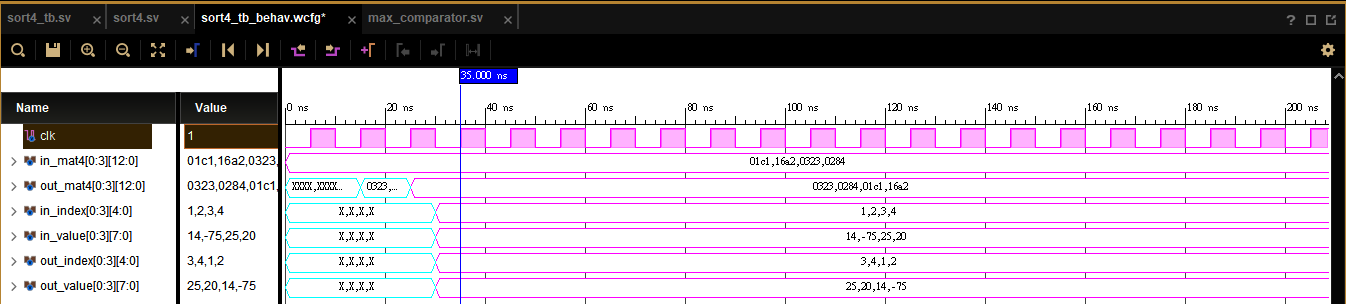
Fourth layer [-111/15 -122/26]

Final result [-122/26]

post-route simulation results :

8. Show the Verilog behavior simulation results and post-route simulation results. (20%)

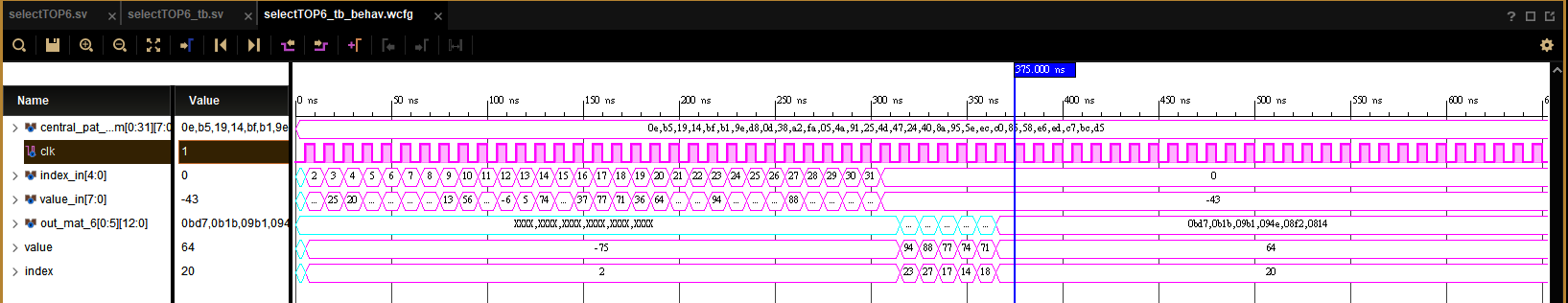
Behavior simulation results:



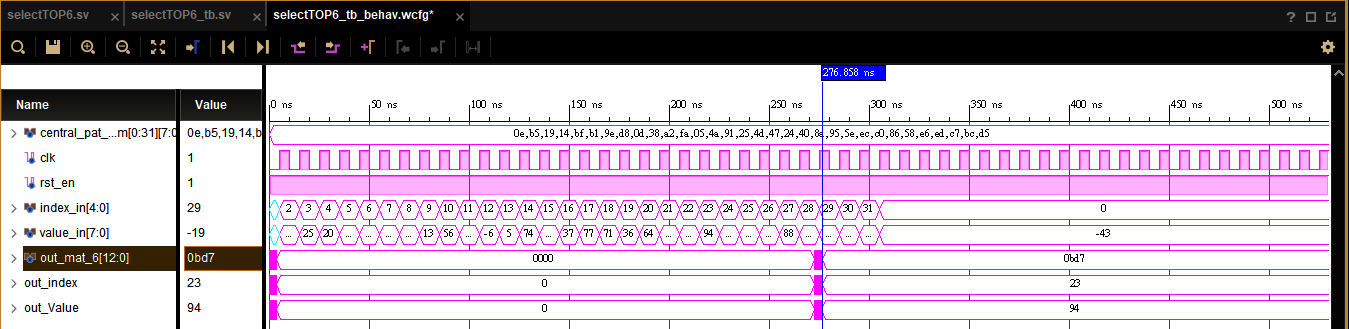
post-route simulation results :

9. Show the Verilog behavior simulation results and post-route simulation results. (20%)

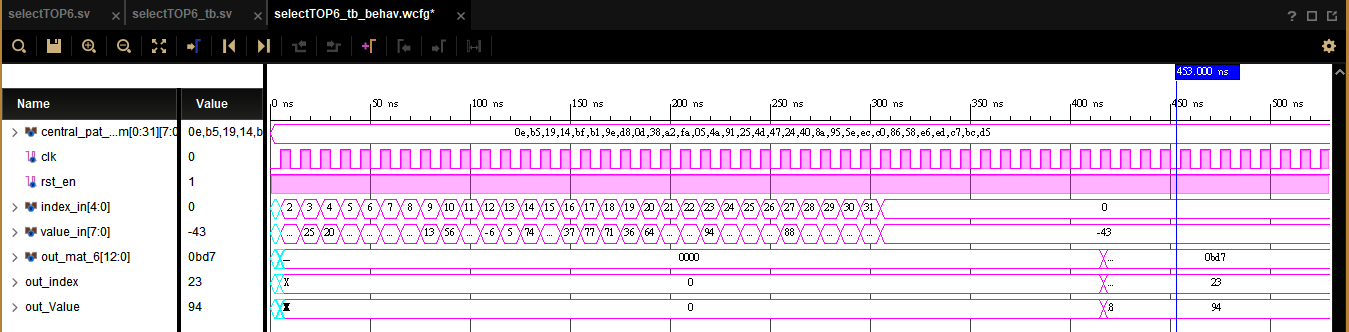
Behavior simulation results:



Post- synthesis timing simulation:



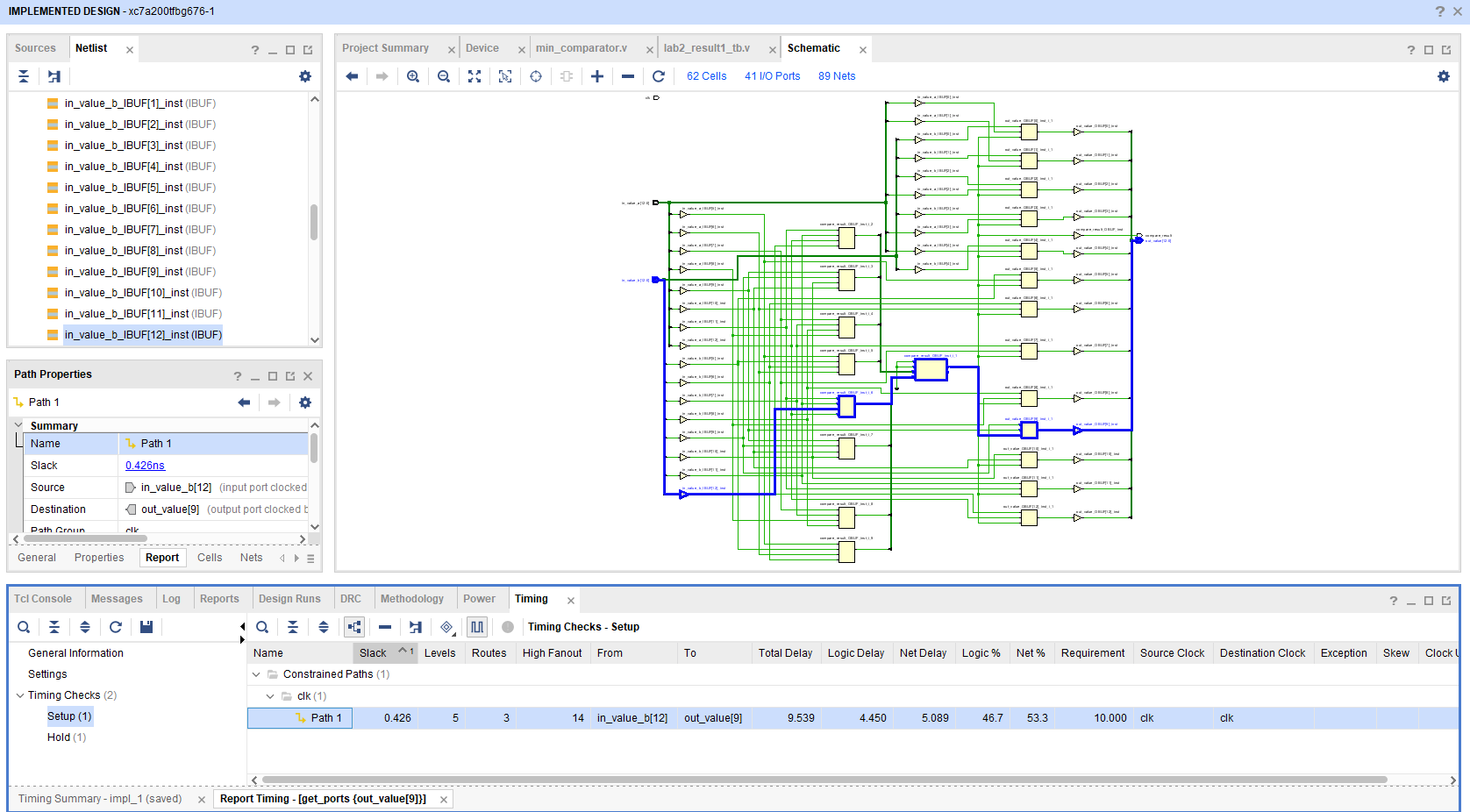
Post-implementation simulation:



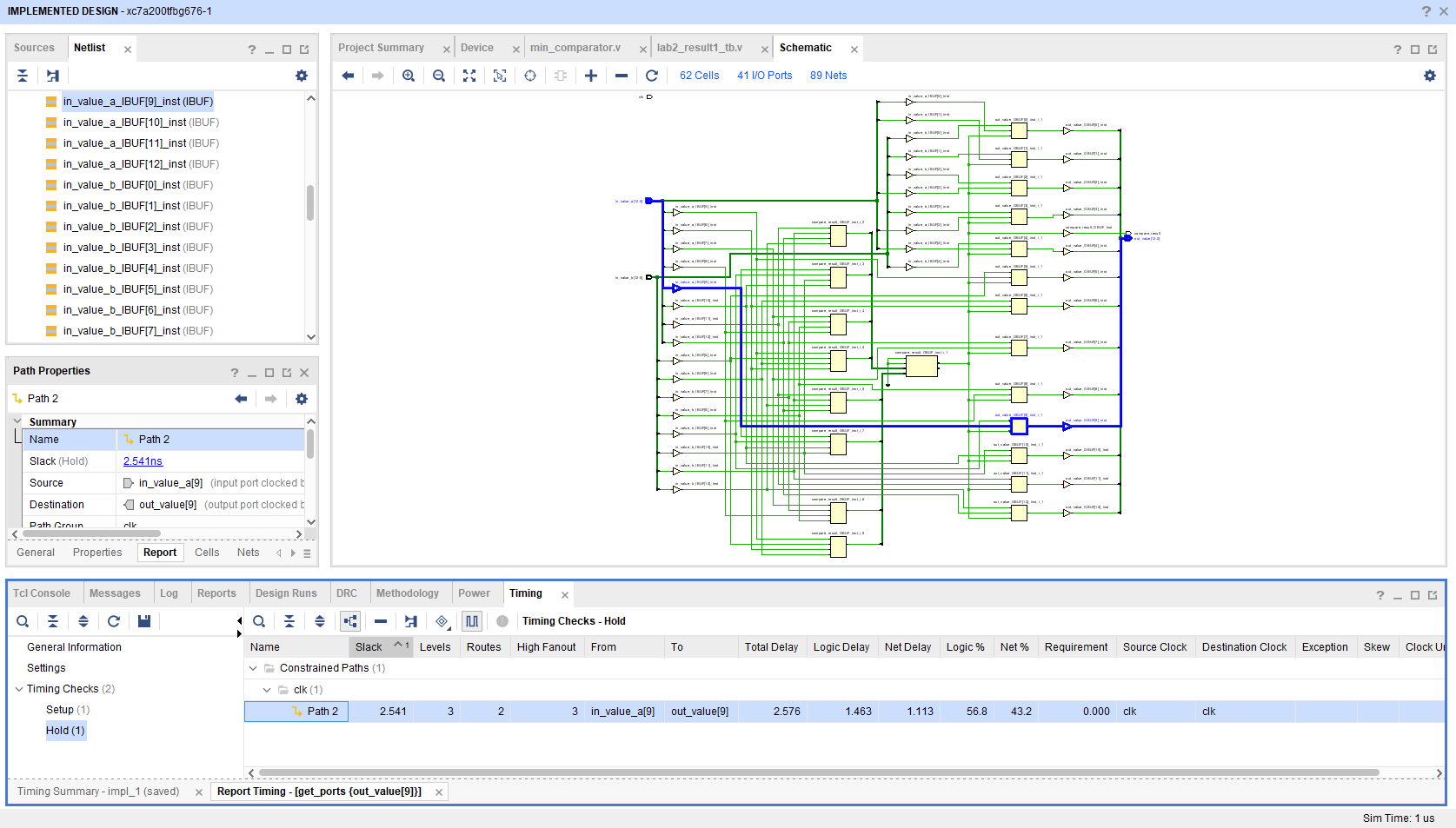
10. Show your timing report and draw the critical path from the max delay timing report of the block designed in Q6 and Q8 of Procedure. (20%)

Q6

Setup time:

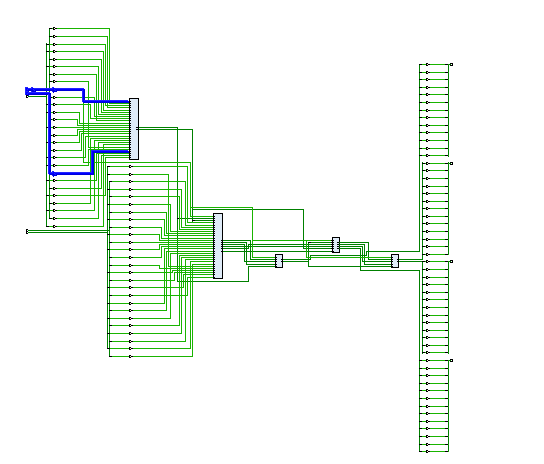


Setup time:

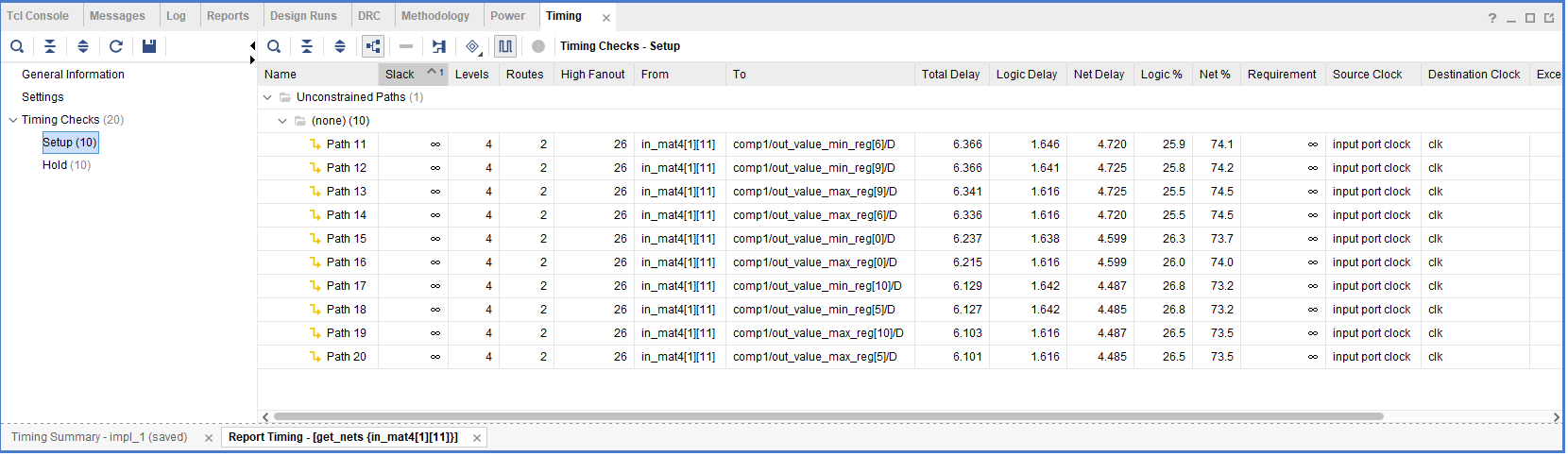


Q8

Setup time:

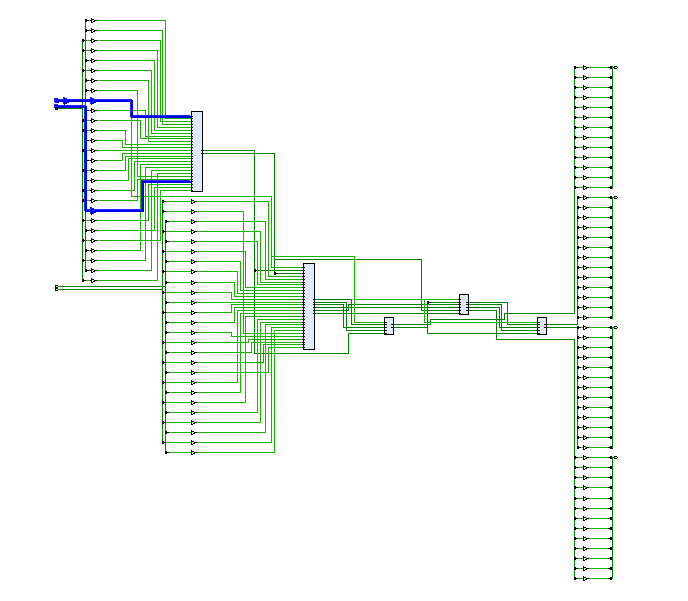


Timing report



Hold time:

critical path



Timing report:

