**DCCDL LAB4**

**Verilog**

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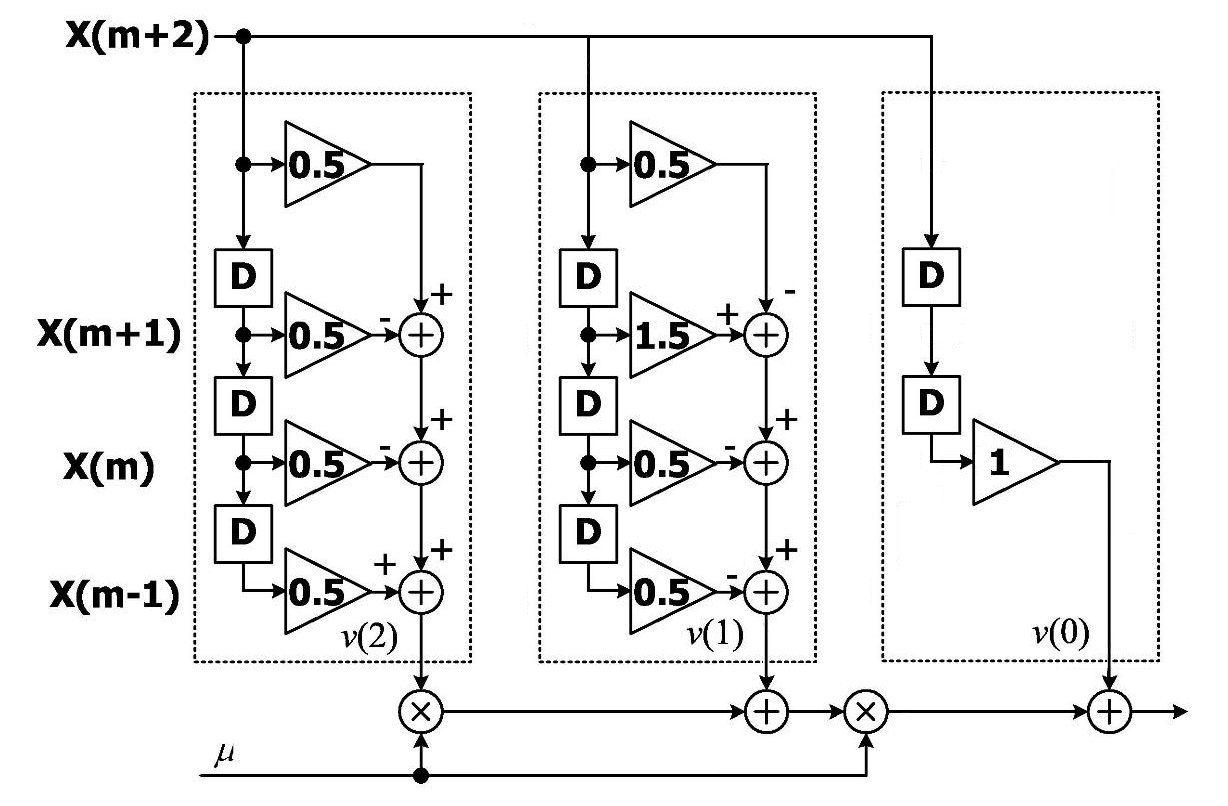
6. Please depict the final architecture of the piece-wise parabolic interpolator (10%) and show the results of different word-length settings versus the root mean squared error for

a. Wordlength of input (5%)

b. Wordlength of 𝜇 (5%)

c. Wordlength of multiplier (by 𝜇) (5%)

d. Wordlength of adder (5%)



7. Design your piece-wise parabolic interpolator of Farrow structure. Please note that your input will change every 8 clock cycles and your 𝜇 value will change every clock cycle. Show the timing diagram of behavior simulation and post-route simulation results. Also depict the error between the Verilog outputs and Matlab floating-point outputs (30%)

8. Show your timing report and critical path. Check if the critical path is reasonable. (10%)

9. **Compare to the post-route simulation results (by Matlab figure.) (10%) and** show your measurement results on your hardcopy before the deadline. (10%) **(Demo to TA until 11/14. (10%))**