**DCCDL LAB4**

**Verilog**

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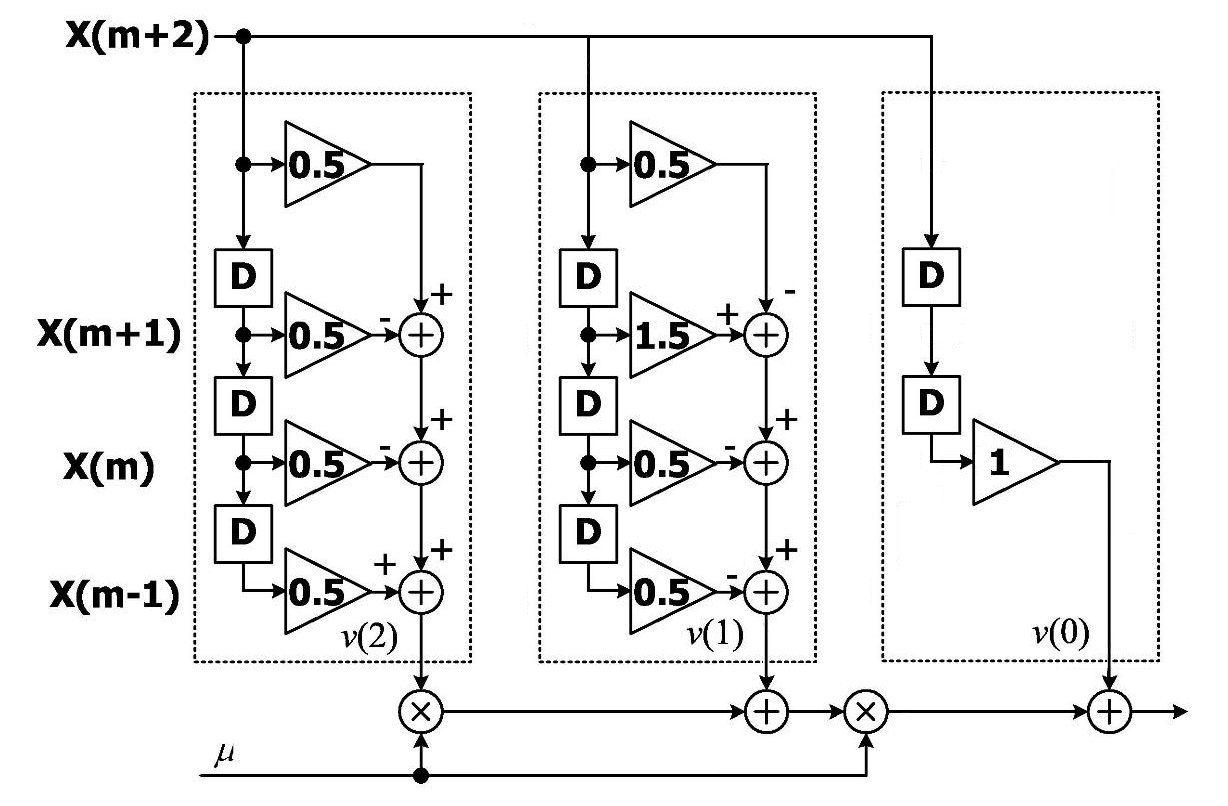
6. Please depict the final architecture of the piece-wise parabolic interpolator (10%) and show the results of different word-length settings versus the root mean squared error for

a. Wordlength of input (5%)

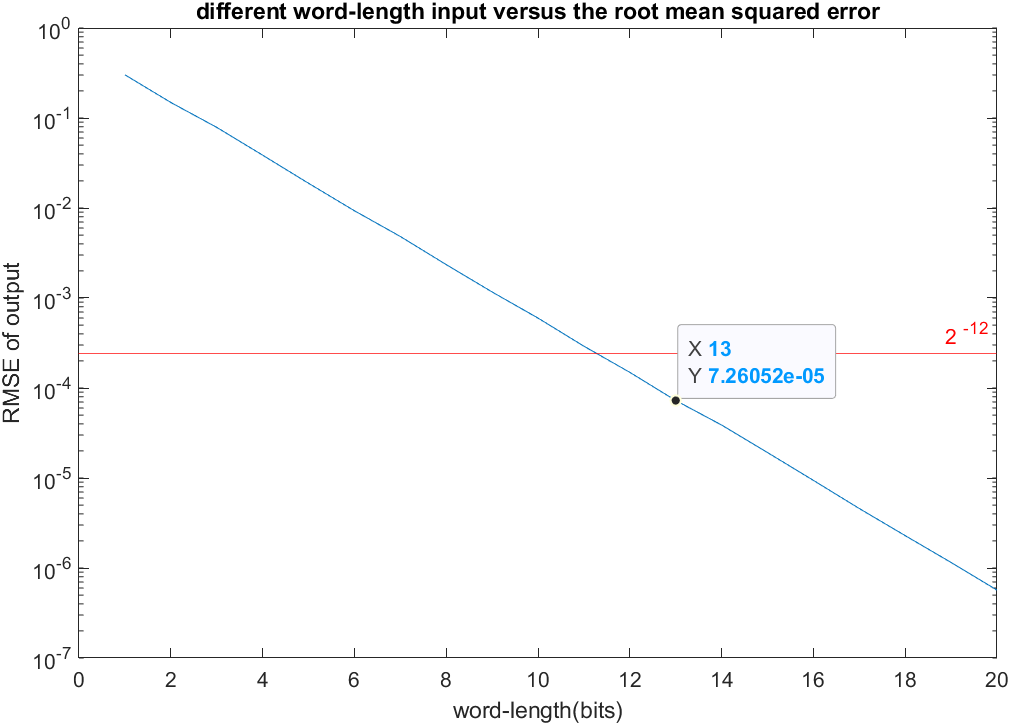
b. Wordlength of 𝜇 (5%)

c. Wordlength of multiplier (by 𝜇) (5%)

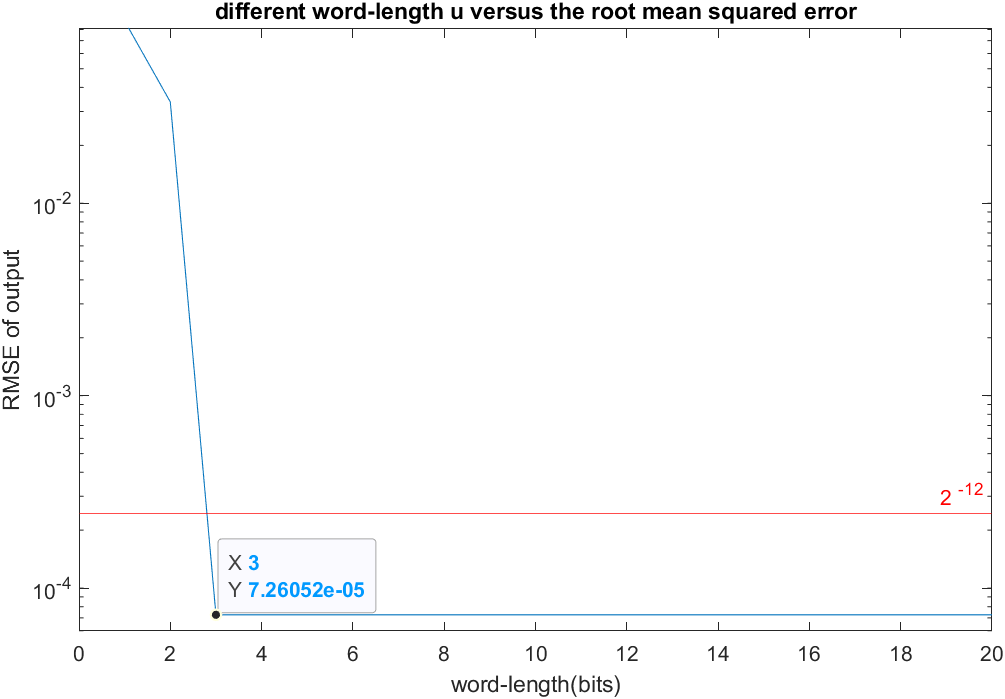
d. Wordlength of adder (5%)



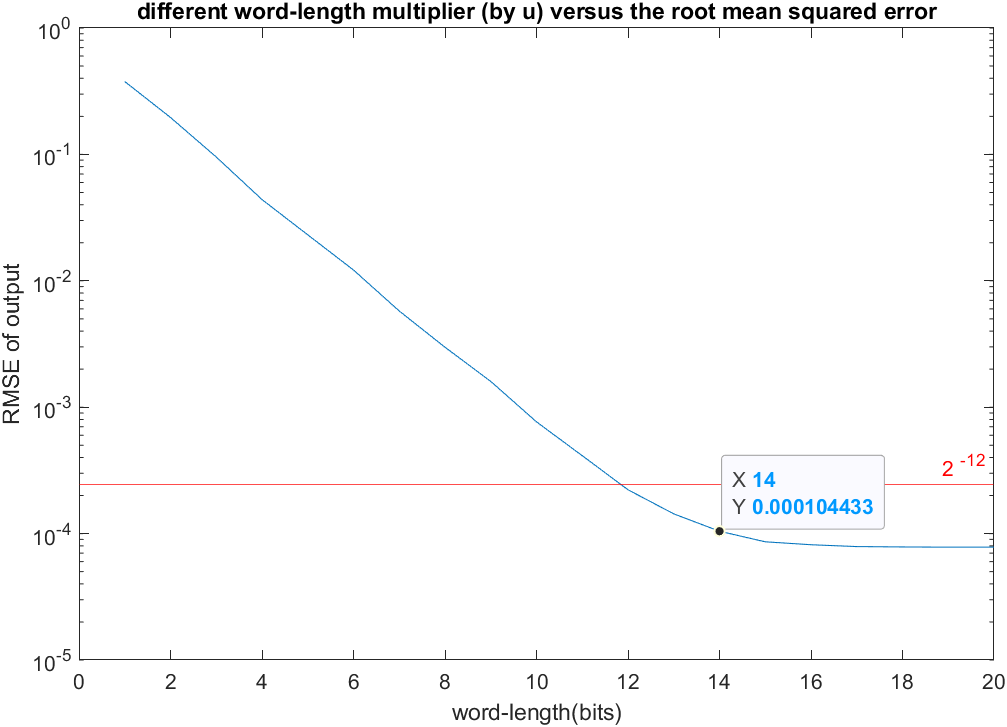
a. Wordlength of input (5%)



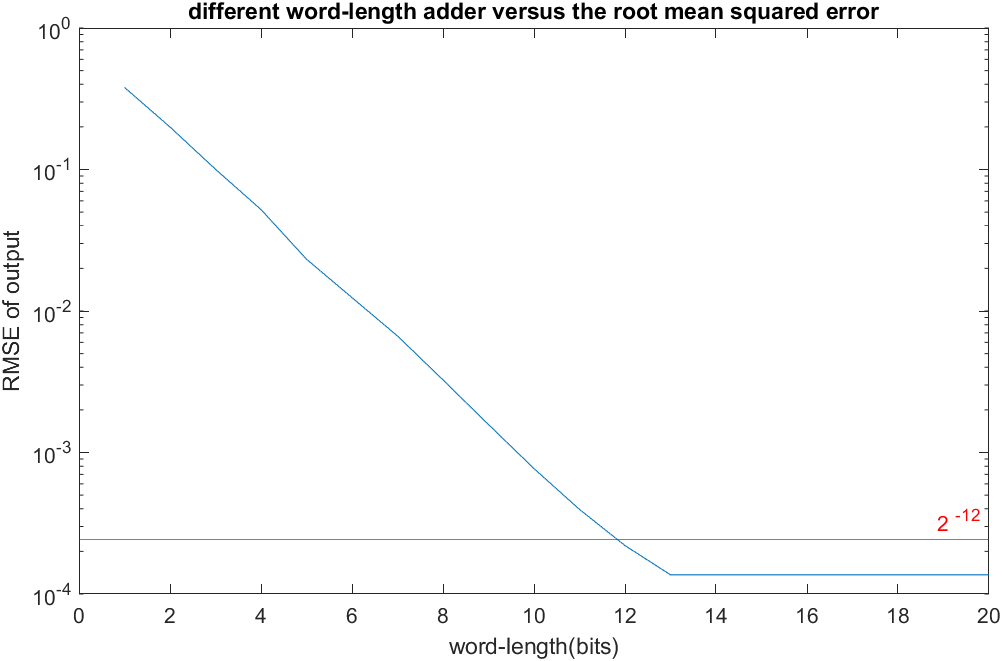
b. Wordlength of 𝜇 (5%)



c. Wordlength of multiplier (by 𝜇) (5%)



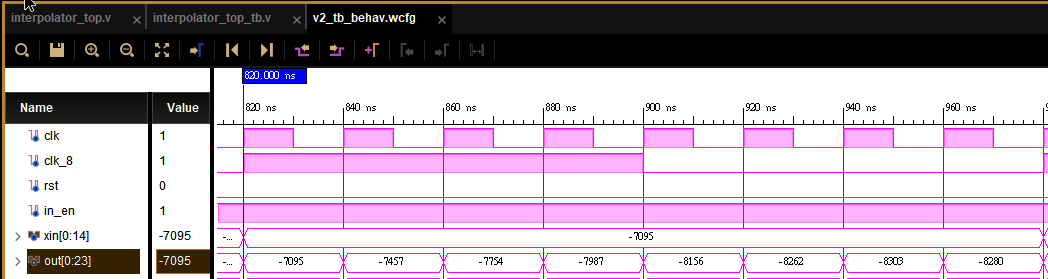
d. Wordlength of adder (5%)

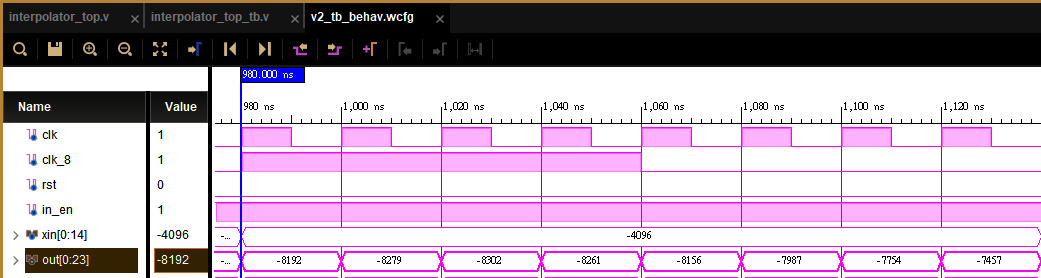


7. Design your piece-wise parabolic interpolator of Farrow structure. Please note that your input will change every 8 clock cycles and your 𝜇 value will change every clock cycle. Show the timing diagram of behavior simulation and post-route simulation results. Also depict the error between the Verilog outputs and Matlab floating-point outputs (30%)

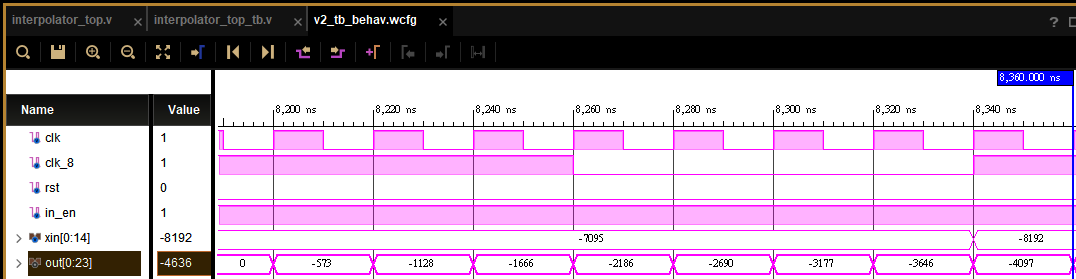
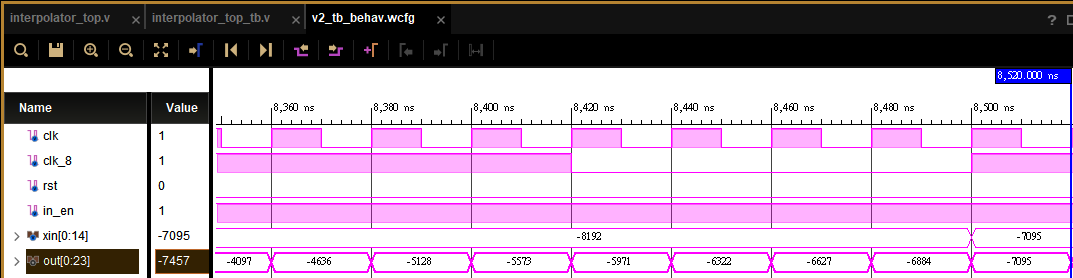
(1) behavior simulation:

First 10 results:





Last 10 results:

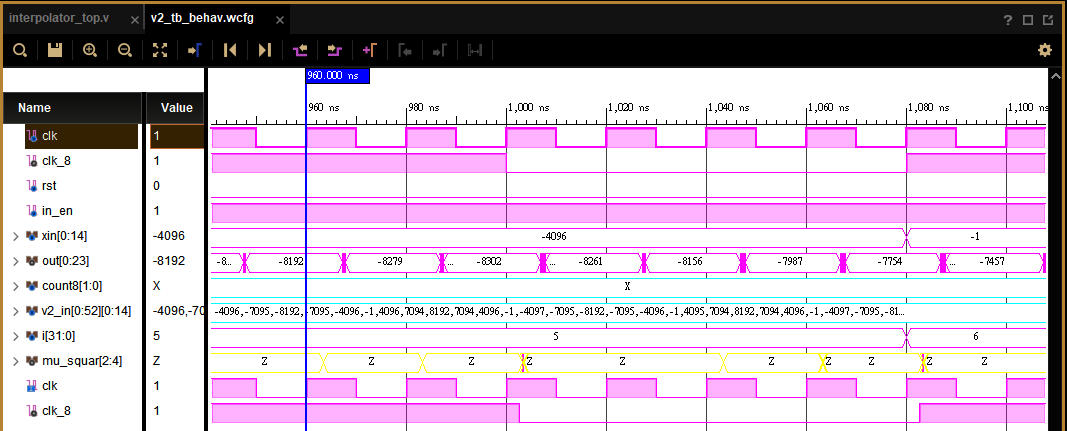
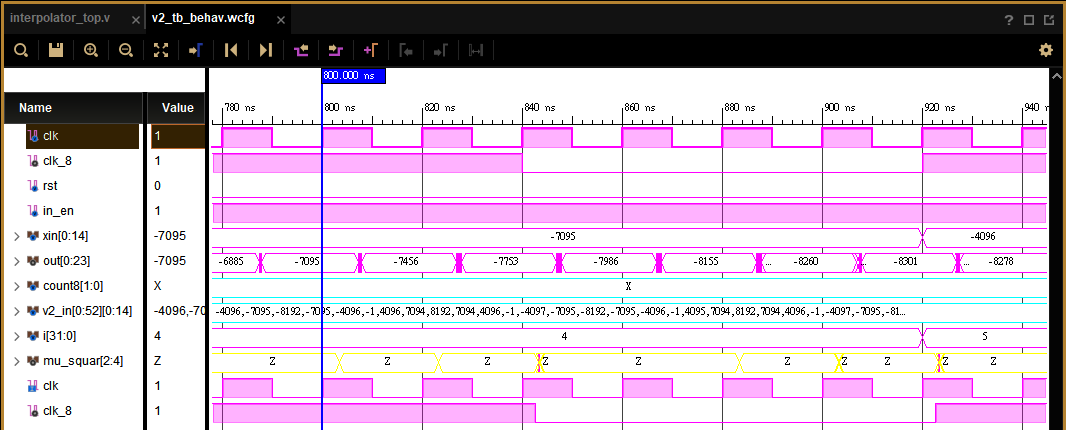


(2) post-Synthesis simulation:

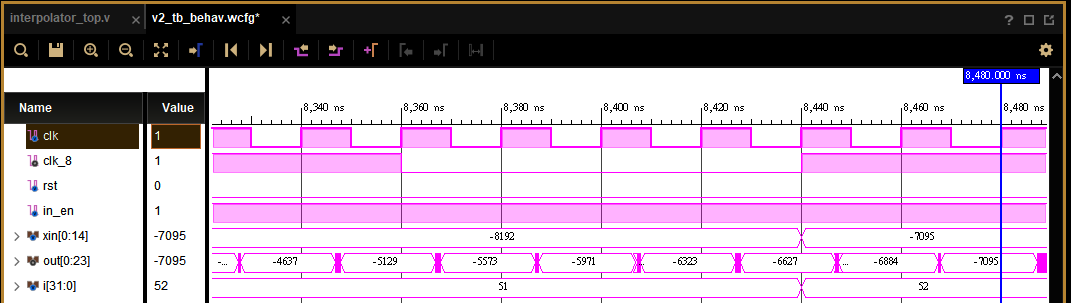
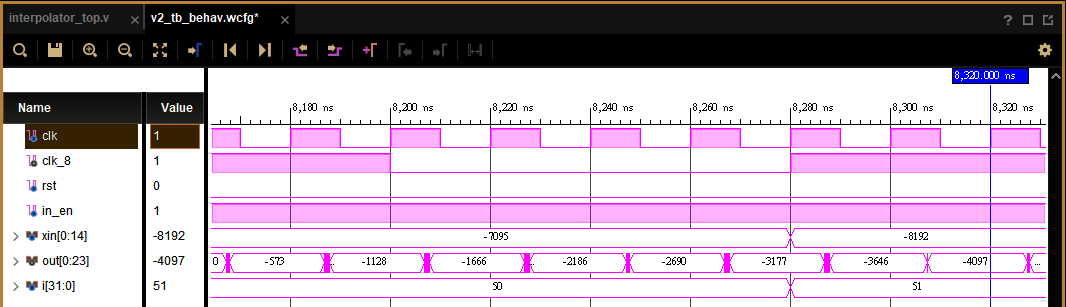
100 ns global reset:



First 10 results:

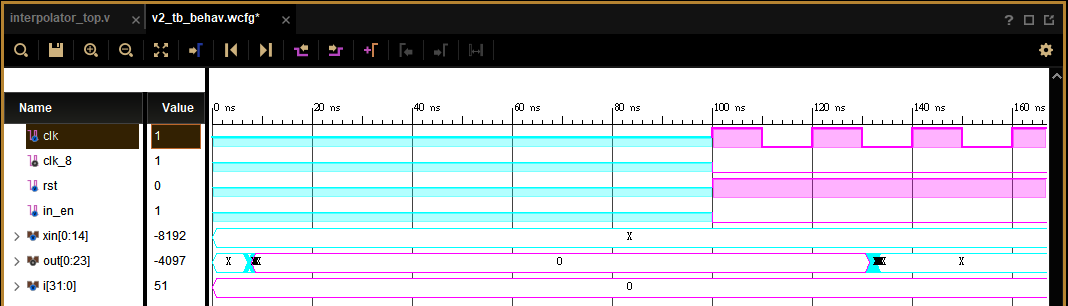


Last 10 results:

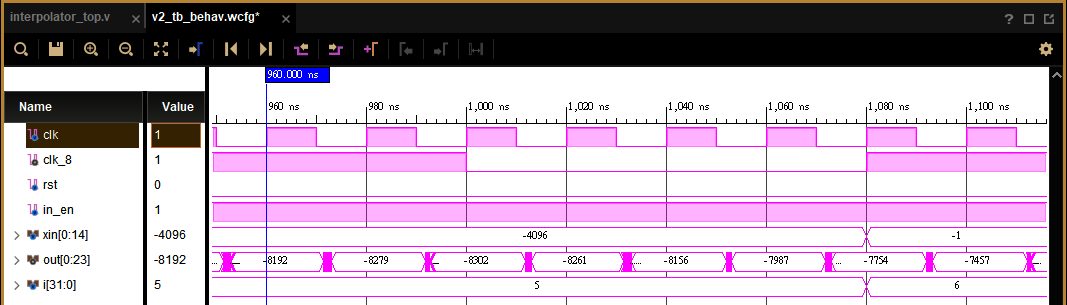
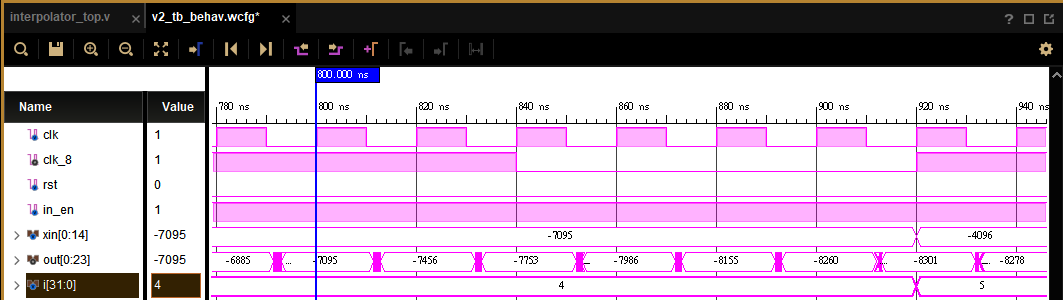


(3) post-Implementation simulation:

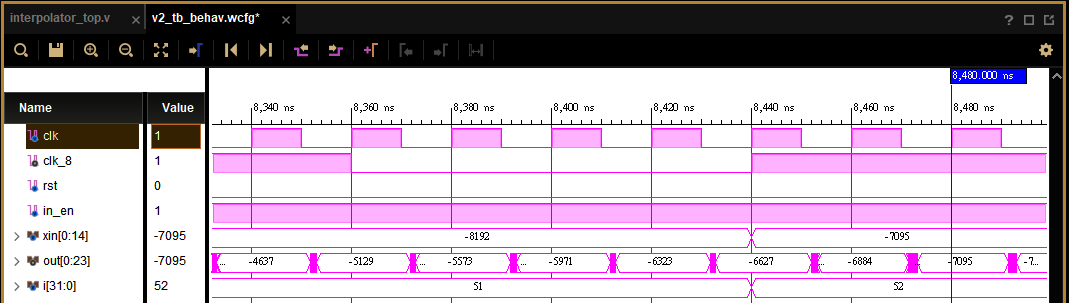
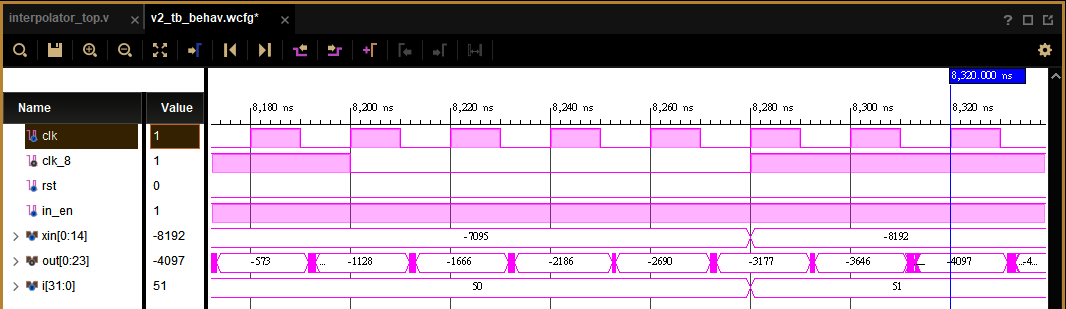
100 ns global reset:



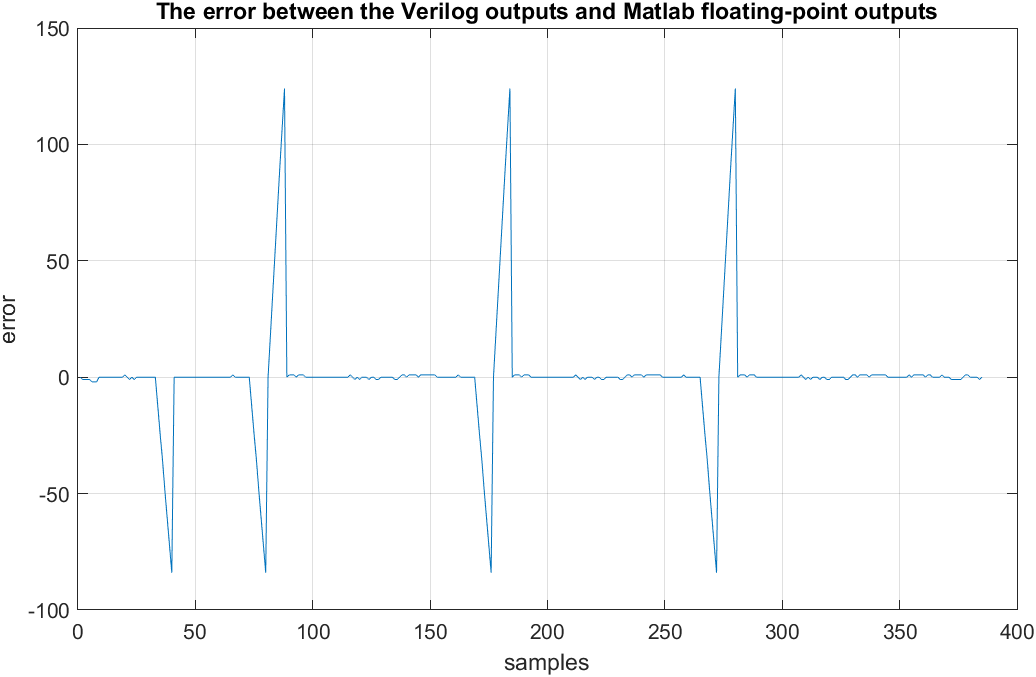
First 10 results:



Last 10 results:



(4) the error between the Verilog outputs and Matlab floating-point outputs



Matlab first 10 results:

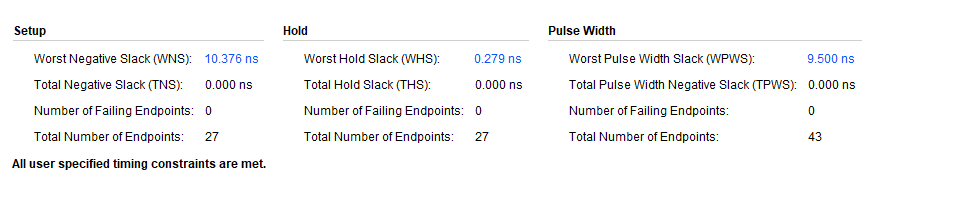
[ -7095 -7457 -7754 -7987 -8156 -8262 -8303 -8280 -8192 -8279 ]

Matlab last 10 results:

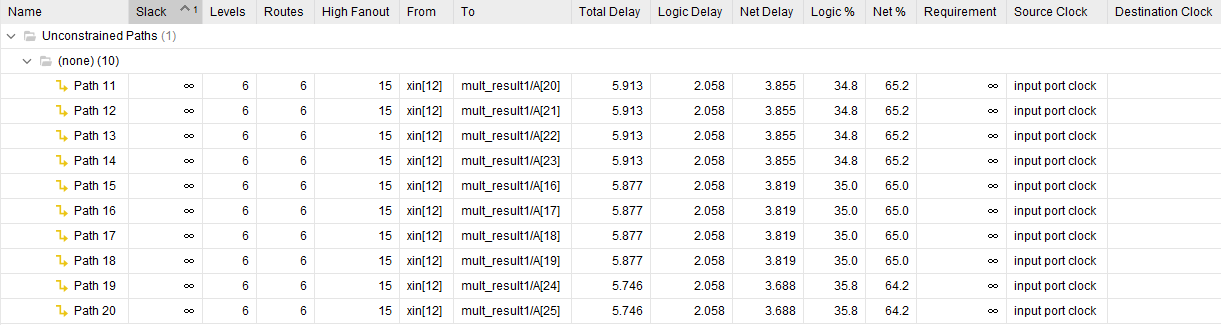
[ -3178 -3647 -4097 -4636 -5128 -5573 -5971 -6323 -6627 -6885 ]

8. Show your timing report and critical path. Check if the critical path is reasonable. (10%)

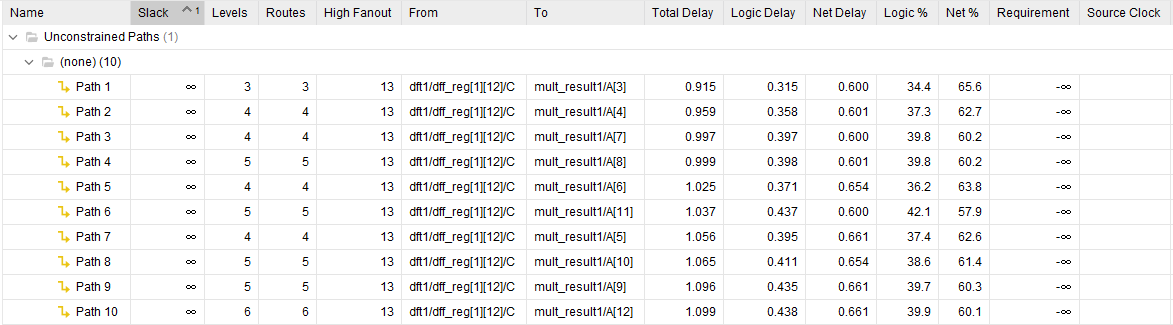
Timing report:



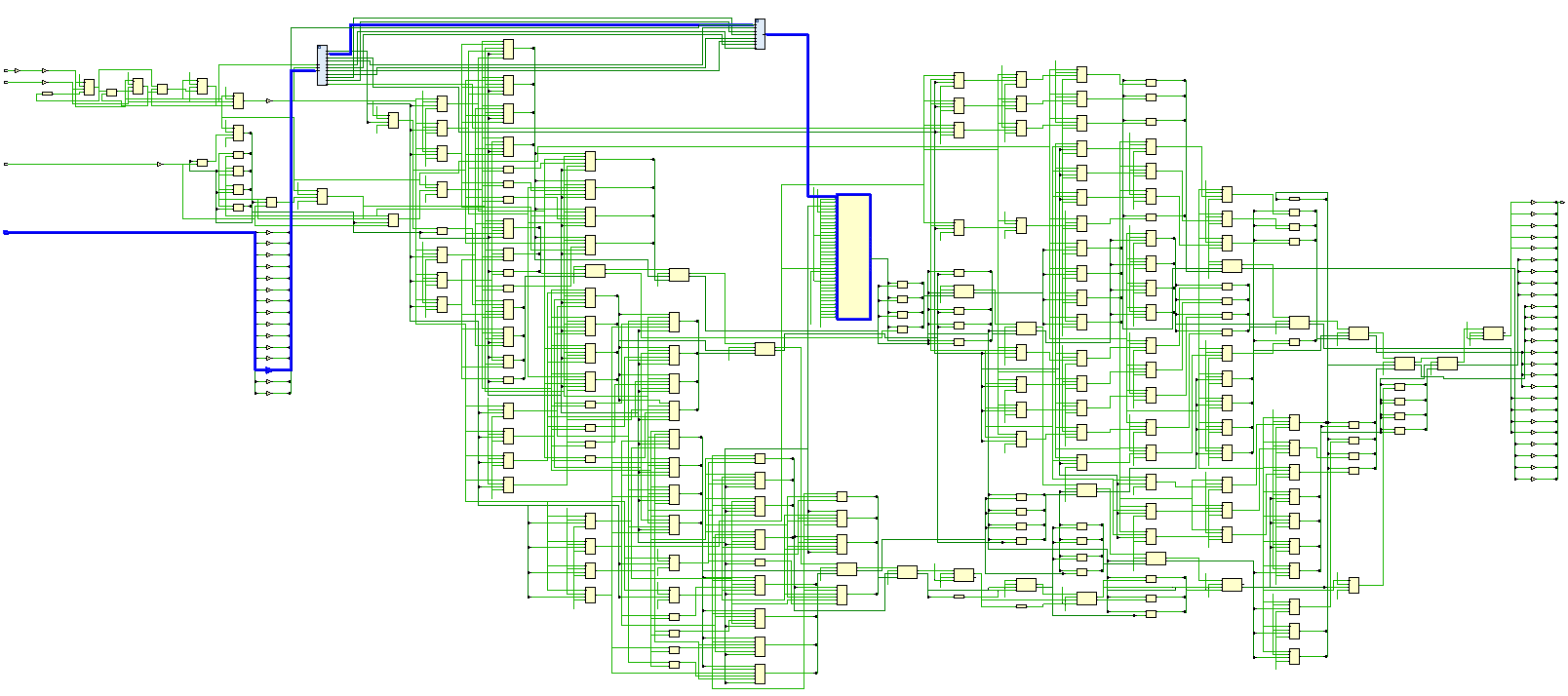
Setup time:

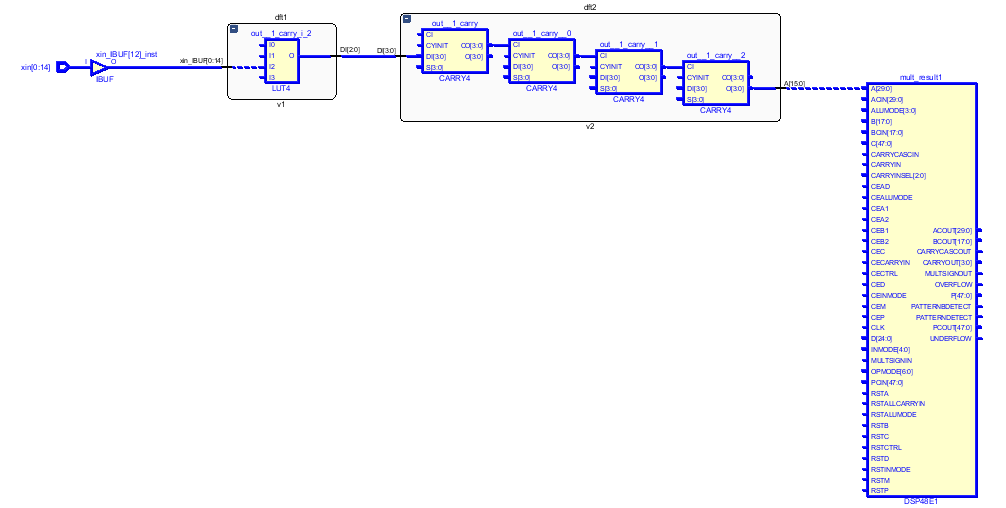


Hold time:



critical path:



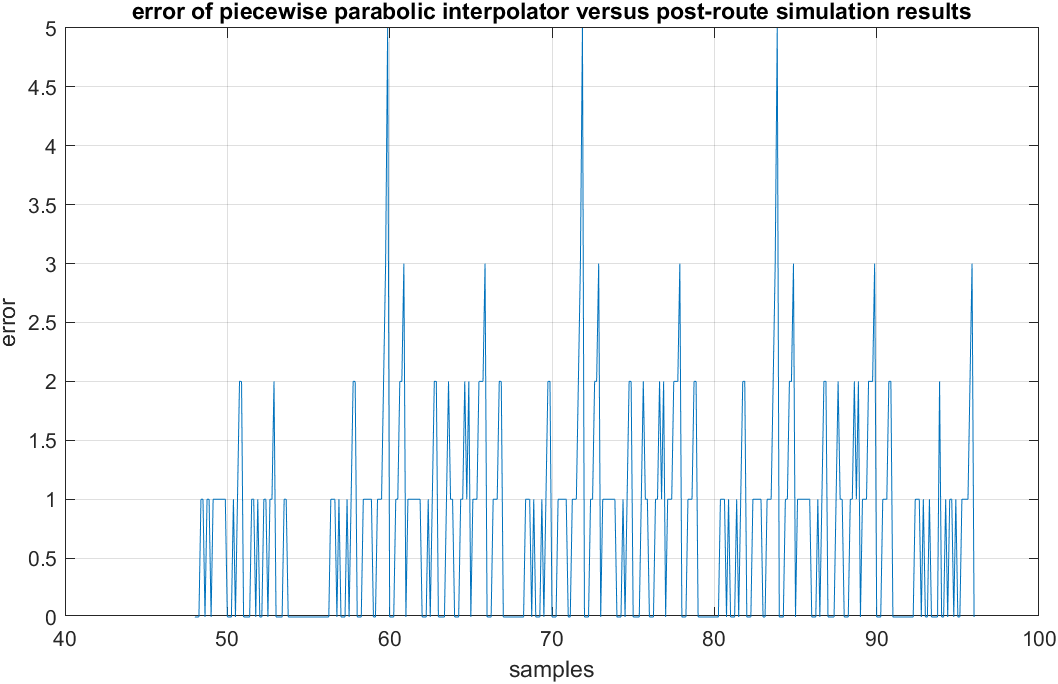


此次設計為了提高其運算速度採用了pipeline的設計，在v0, v1, v2之輸出擺上一個latch來減少setup time，防止訊號走太長的路徑與經過太多運算，從而導致運算出錯。

這一路徑經過1次位移後分別經過了三顆加法器，最後到達與mu相乘的乘法器前的latch。此一路徑作為本設計架構的critical path學生認為很合理。

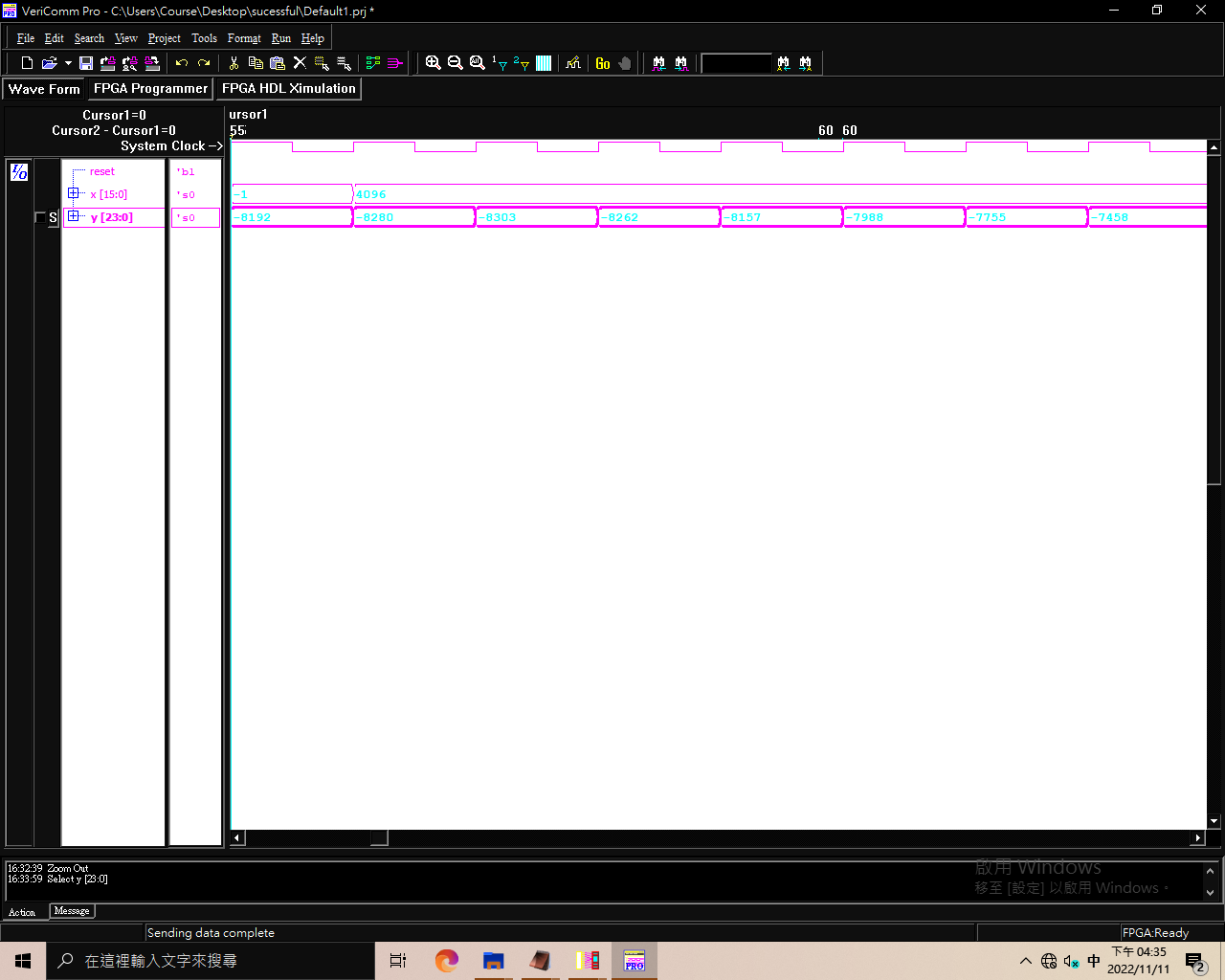
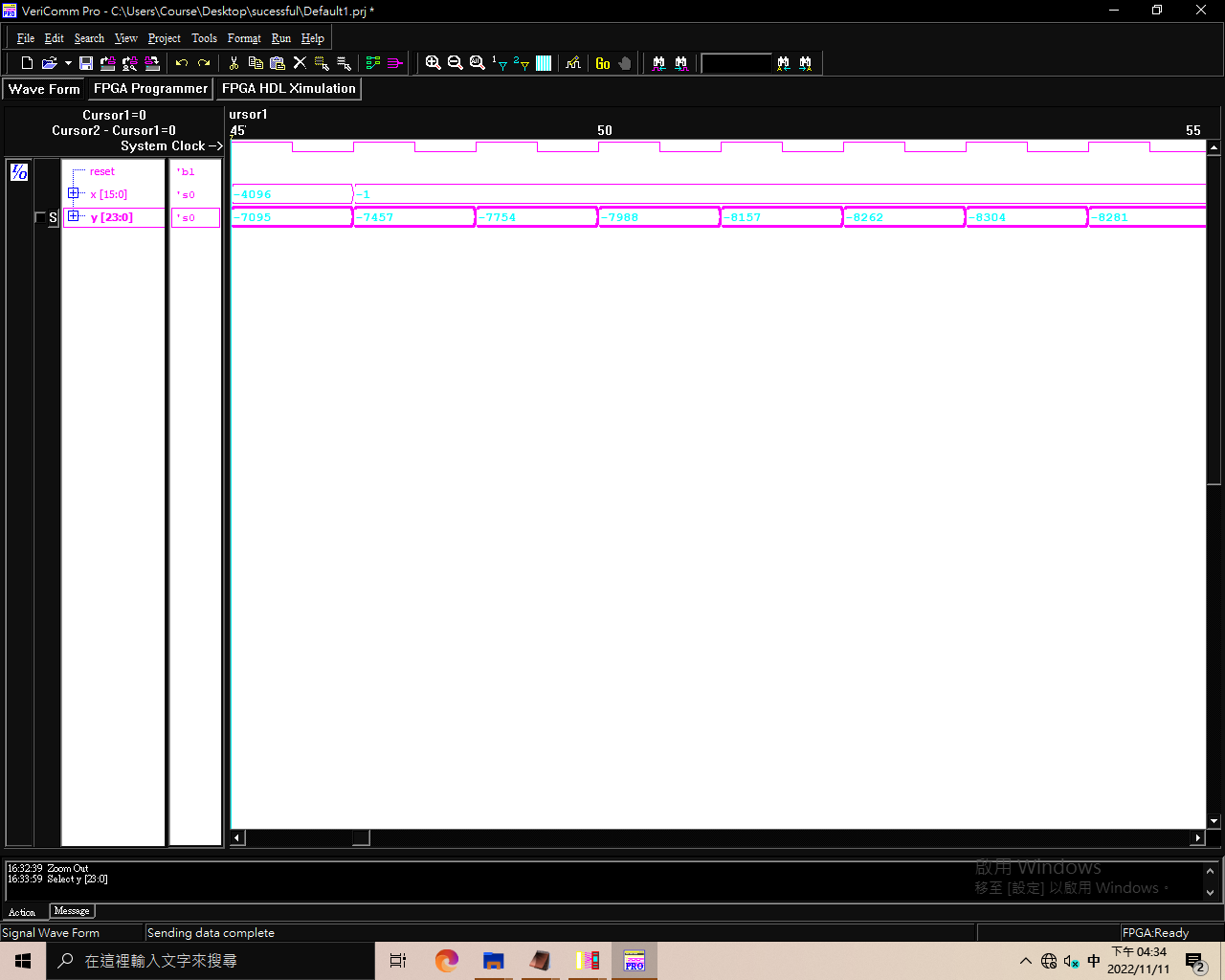
9. **Compare to the post-route simulation results (by Matlab figure.) (10%) and** show your measurement results on your hardcopy before the deadline. (10%) **(Demo to TA until 11/14. (10%))**

(1) Compare to the post-route simulation results (by Matlab figure.)



(2) FPGA result

First 10 result:



Last 10 result:

