**DCCDL LAB6**

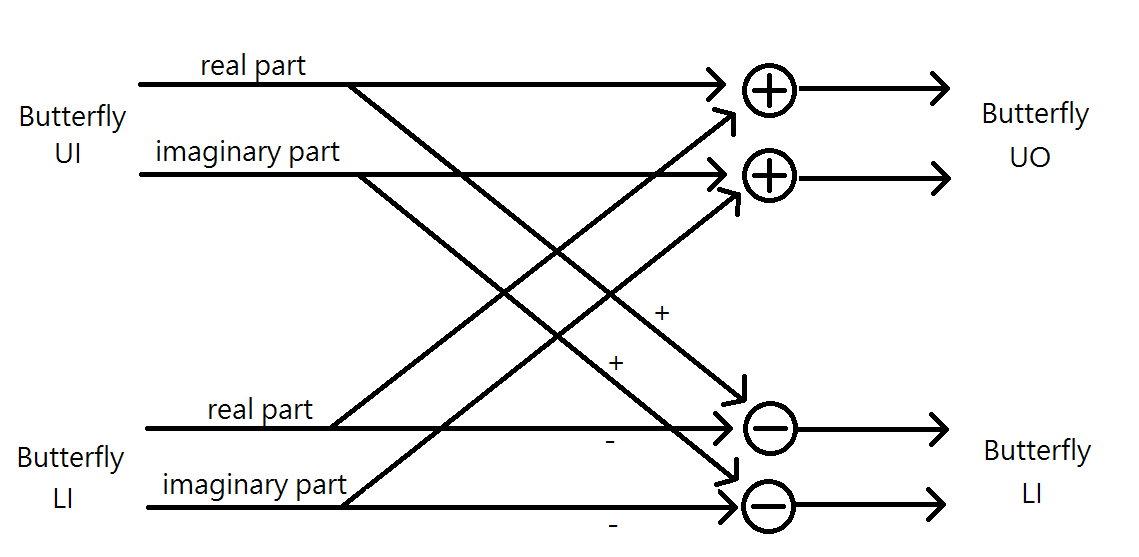
**Part I**

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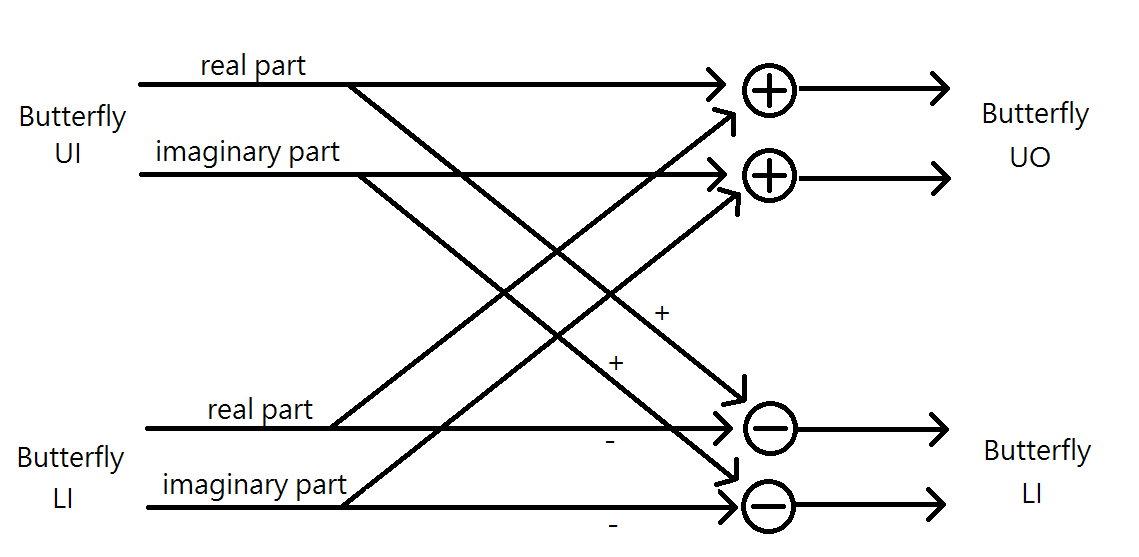
1. Draw your block diagram for the butterfly and commutator modules and explain the timing diagram of the control signals to the commutator modules at all the stages.

Butterfly block diagram:

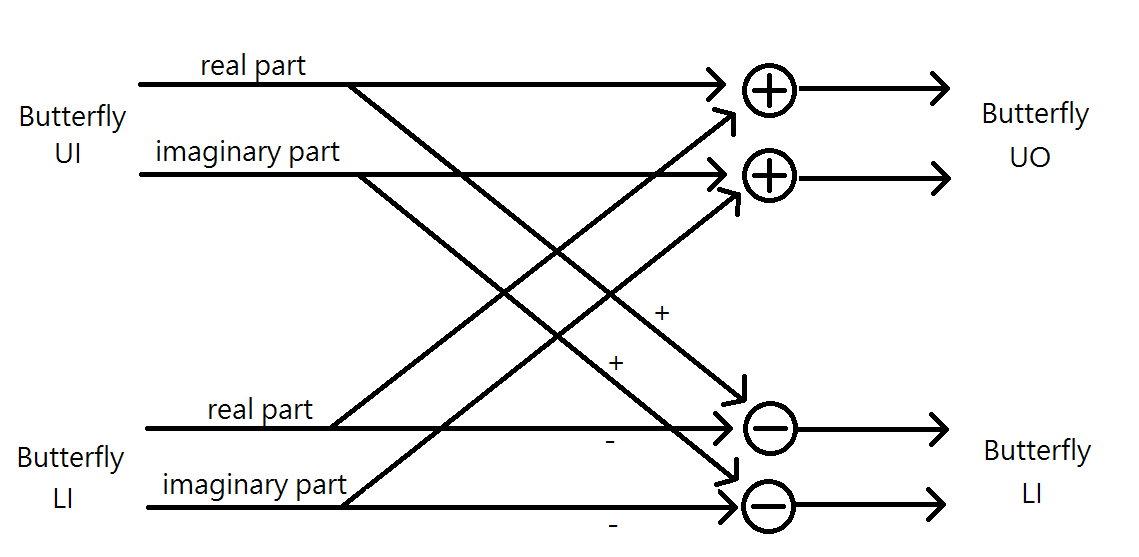
Stage1:



Stage2:

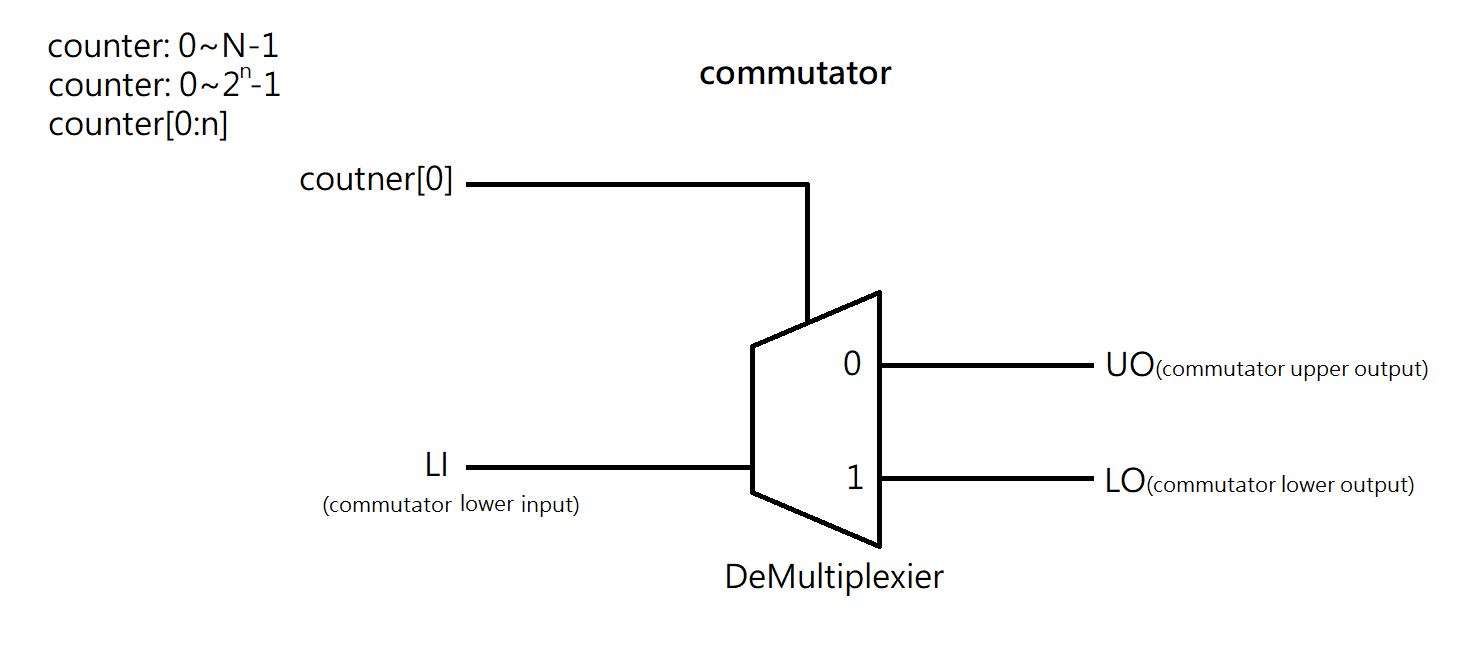


Stage3:

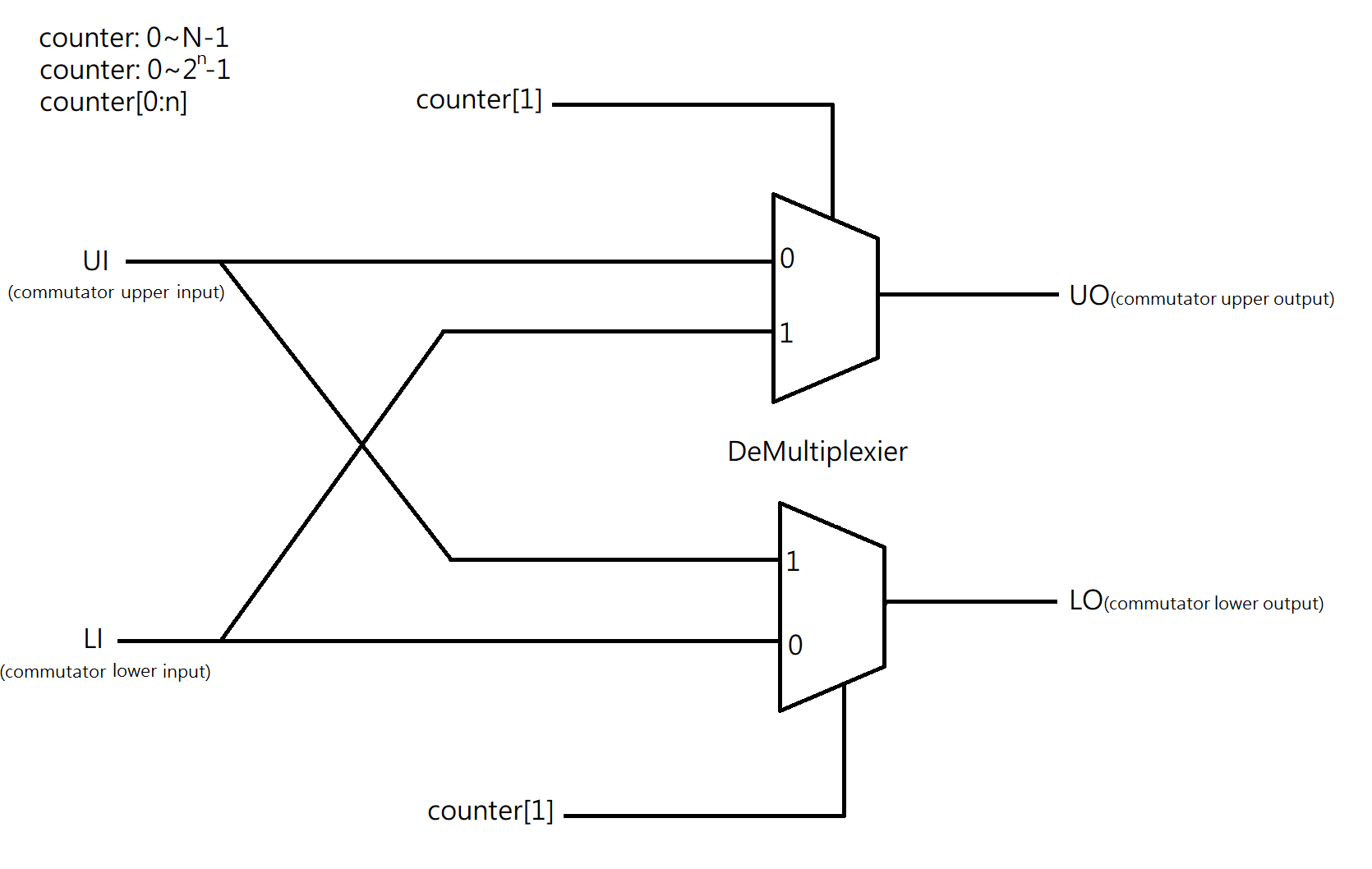


Commutator block diagram:

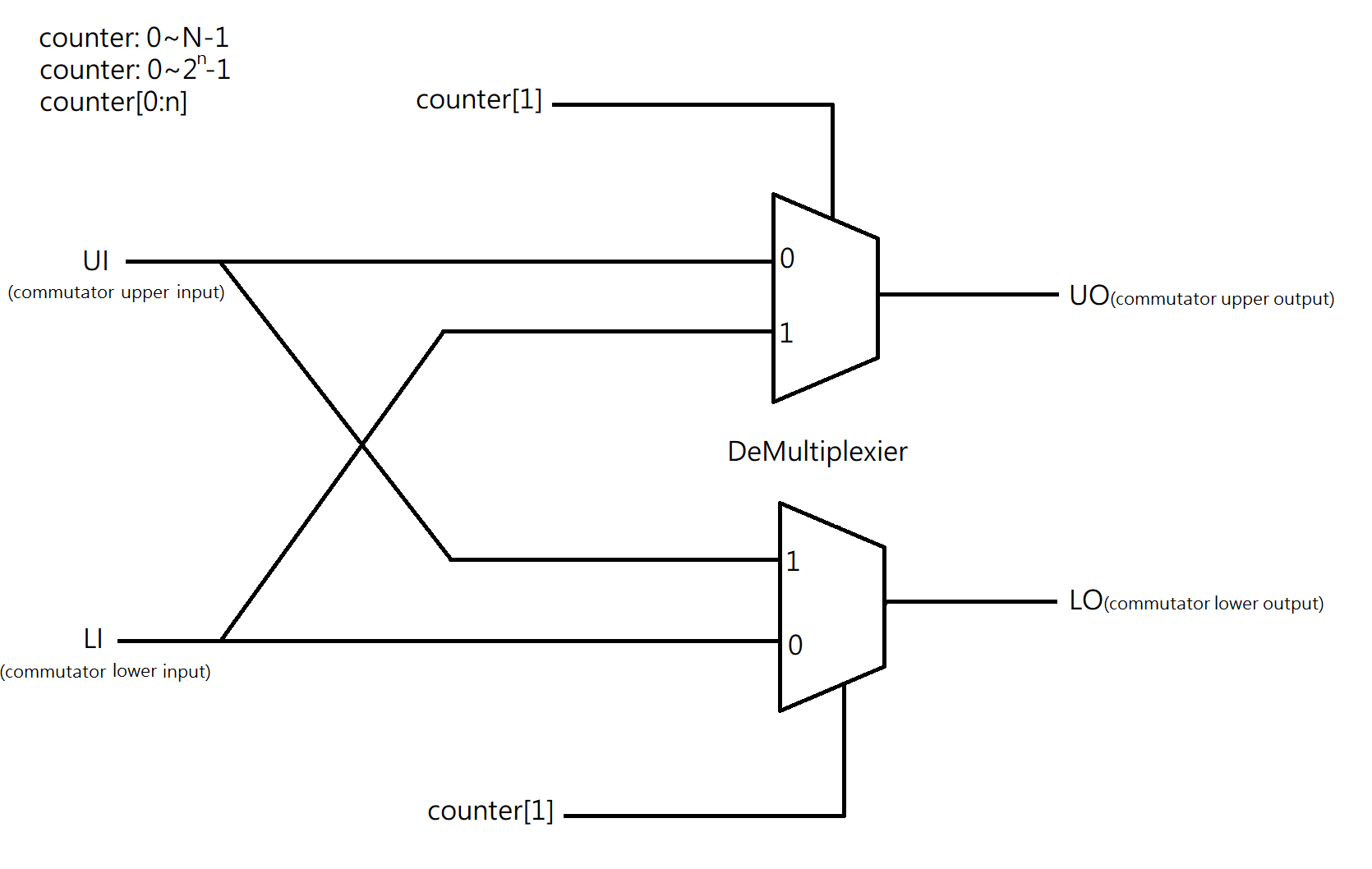
Stage1:



Stage2:



Stage3:



1. Draw the timing diagram of the control signals to the complex multiplier blocks at all the stages.
2. Show your design for bit-reversal module to allow the frequency-domain samples appearing in order.
3. Use Matlab program to implement 8-point MDC FFT architecture and the bit-reversal module. Draw the real-part and imaginary-part of 𝑋0~𝑋7. Compare them with the real-part and imaginary-part of 𝑌0~𝑌7. Depict the error.

5. Show the timing diagram of your Verilog behavior and post-route simulation results of 8-point MDC FFT. Compare with the Matlab results to check your implementation error. Depict the error of the real part and imaginary part of each point using figures.