**DCCDL LAB6**

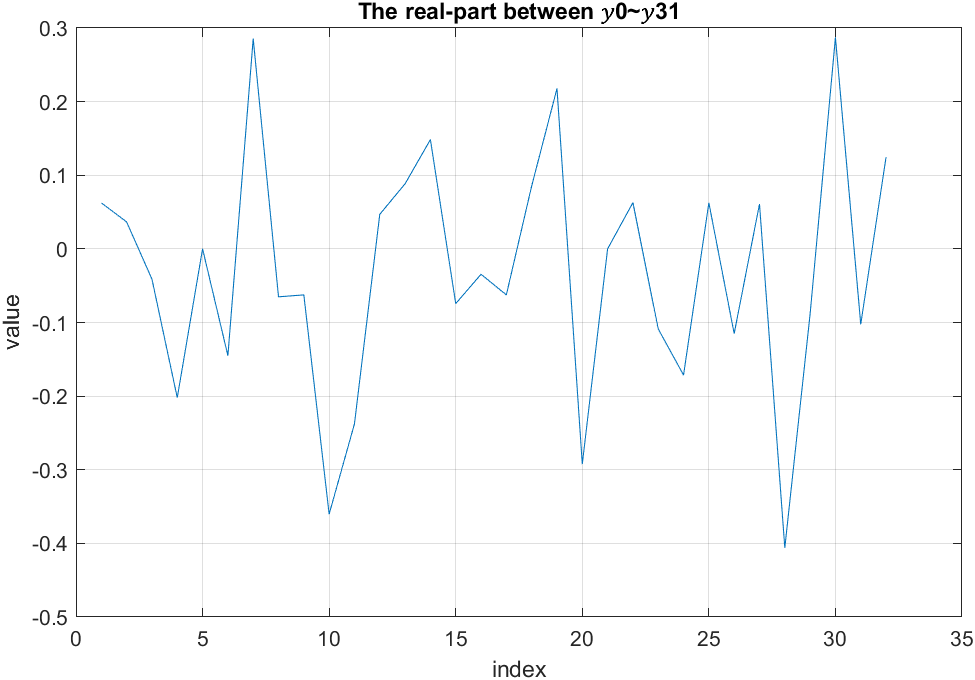
**Part II**

電機碩一 111521035 林豪澤

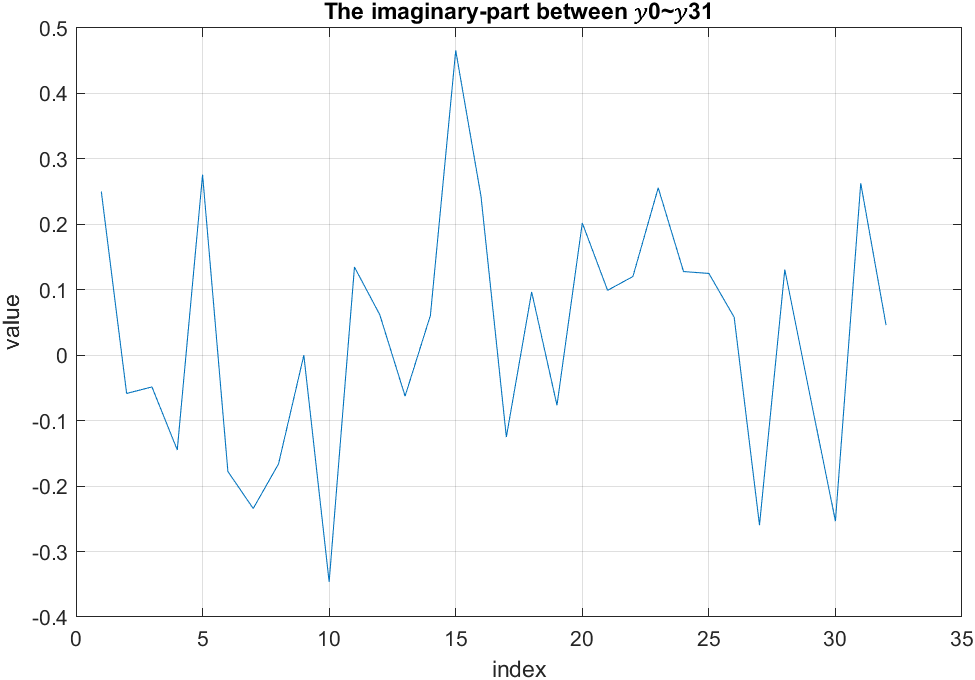
6. Use Matlab program to implement 32-point MDC IFFT architecture and the bit-reversal module. Draw the real-part and imaginary-part of 𝑦0~𝑦31 and 𝑋0~𝑋31. Compare them with the real-part and imaginary-part of 𝑌0~𝑌31. Depict the error.

(1) the real-part and imaginary-part of 𝑦0~𝑦31

real-part of 𝑦0~𝑦31

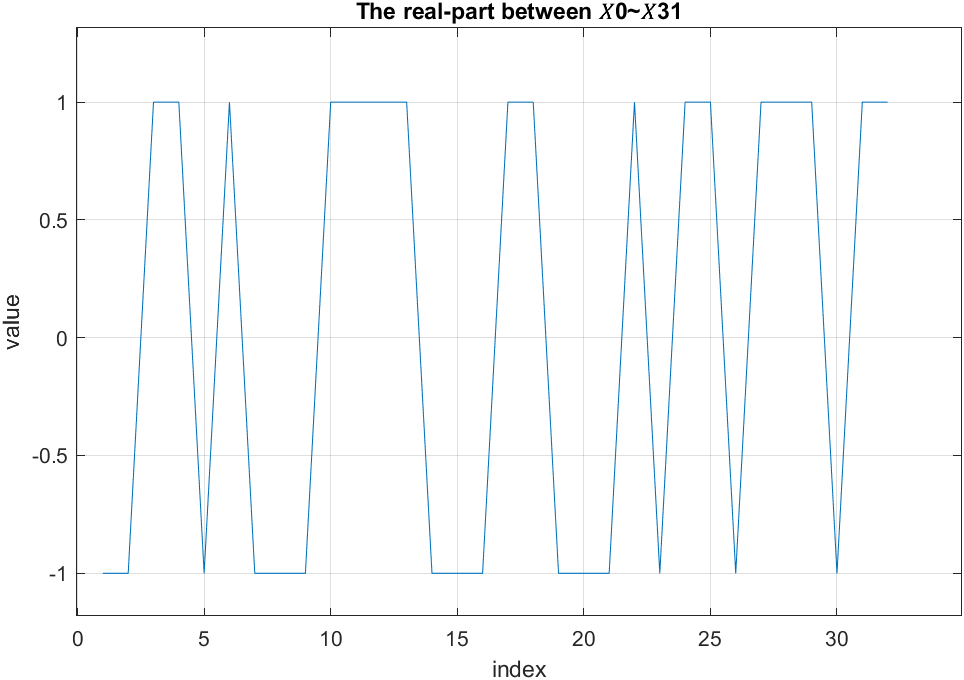


imaginary-part of 𝑦0~𝑦31

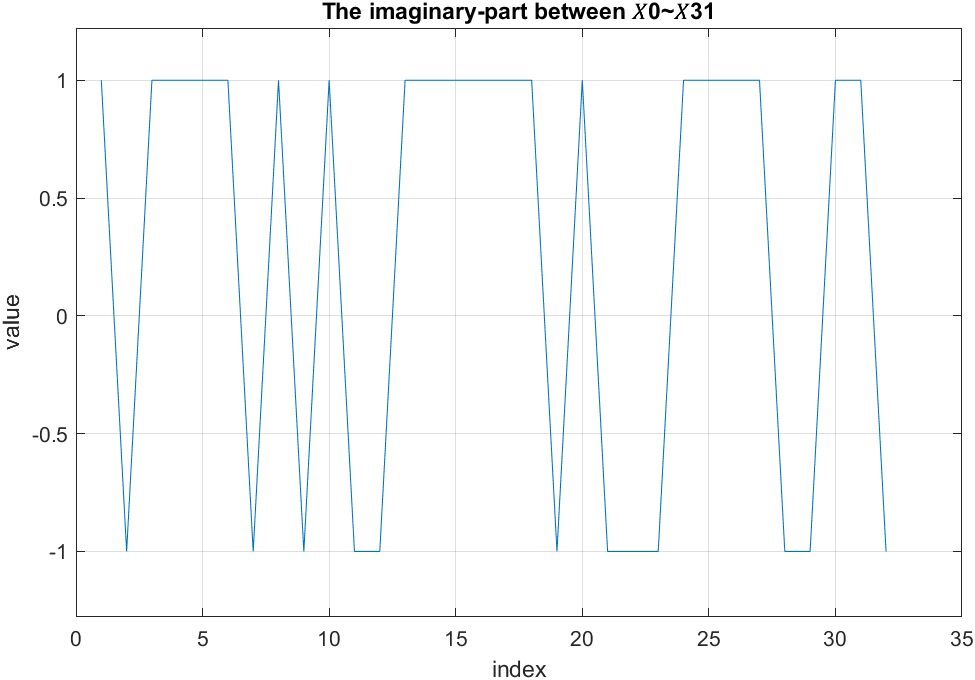


(2) the real-part and imaginary-part of 𝑋0~𝑋31

real-part of 𝑋0~𝑋31

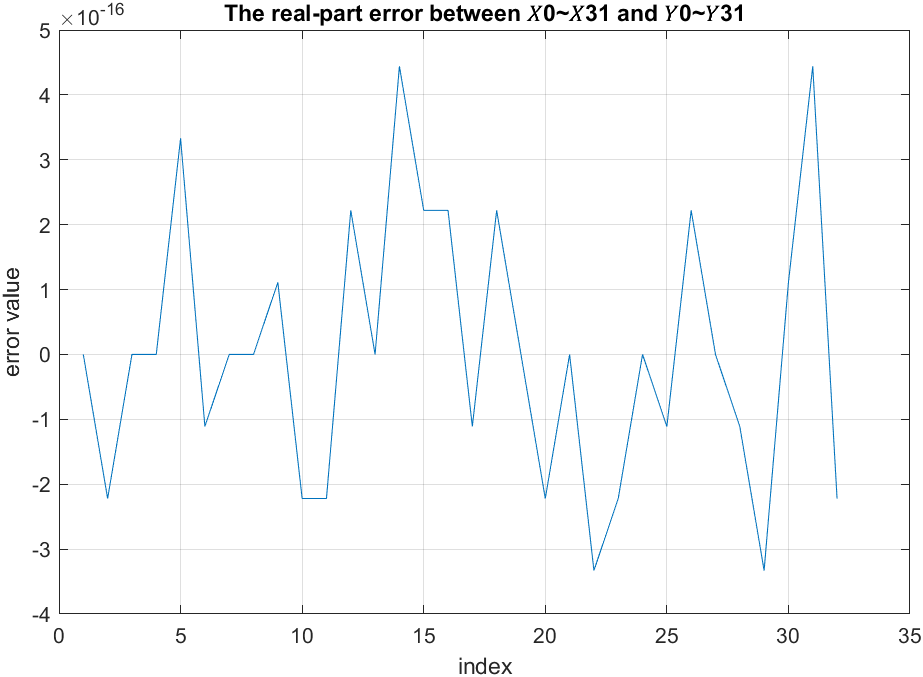


imaginary-part of 𝑋0~𝑋31

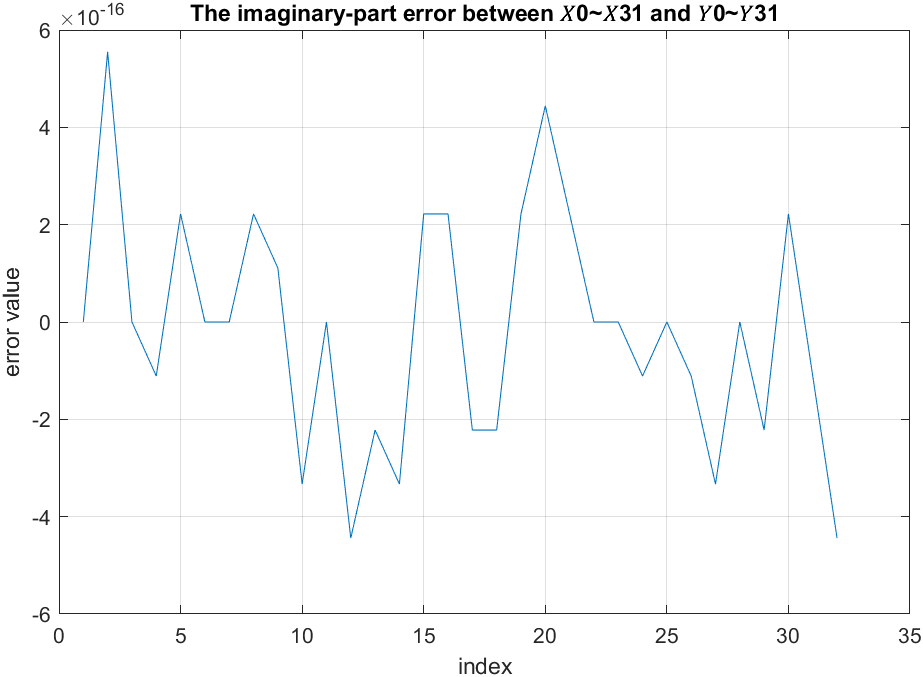


(3) the error between 𝑋0~𝑋31 and 𝑌0~𝑌31

The real-part error between 𝑋0~𝑋31 and 𝑌0~𝑌31



The imaginary-part error between 𝑋0~𝑋31 and 𝑌0~𝑌31



7. Show the timing diagram of your Verilog behavior and post-route simulation results of 32-point MDC IFFT.

Matlab input and output:

Real-part input:

[-512 -512 512 512 -512 512 -512 -512 -512 512 512 512 512 -512 -512 512 512 512 -512 -512 -512 512 -512 512 512 -512 512 512 512 -512 512 512]

Imaginary-part input:

[-512 512 -512 -512 -512 -512 512 -512 512 -512 512 512 -512 -512 -512 -512 -512 -512 512 -512 512 512 512 -512 -512 -512 -512 512 512 -512 -512 512]

Real-part output:

[1024 602 -672 -3310 -1 -2375 4680 -1067 -1025 -5910 -3902 764 1451 2429 -1222 -565 -1024 1398 3570 -4786 1 1031 -1780 -2807 1025 -1890 1000 -6662 -1451 4713 -1682 2043]

Imaginary-part output:

[-4096 958 795 2363 -4521 2912 3838 2724 0 5682 -2204 -1010 1023 -994 -7637 -3970 2048 -1584 1249 -3307 -1623 -1974 -4188 -2094 -2050 -952 4258 -2146 1027 4150 -4313 -762]

The timing diagram of behavior simulation results of 32-point MDC IFFT:

Rst: 重置

Clk: 時脈

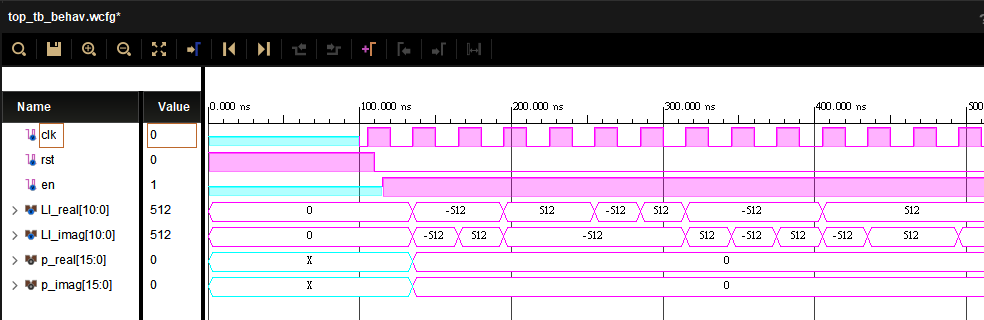
LI\_real: MDC IFFT 輸入 real part

LI\_imag: MDC IFFT 輸入 imaginary part

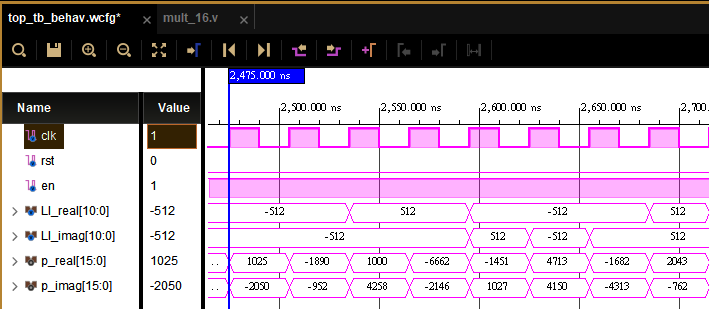
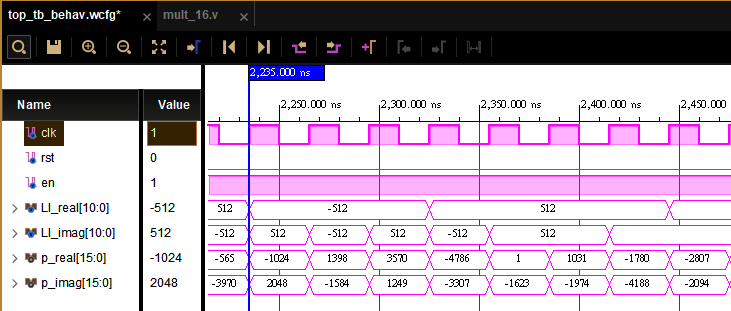
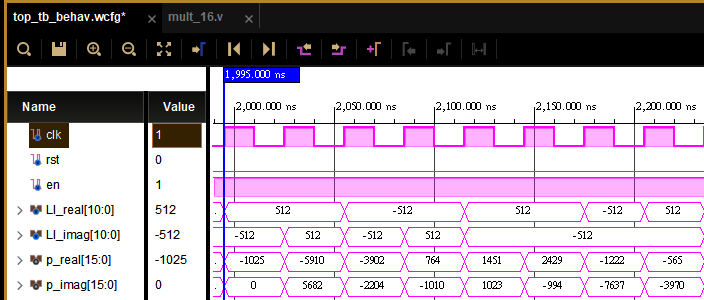
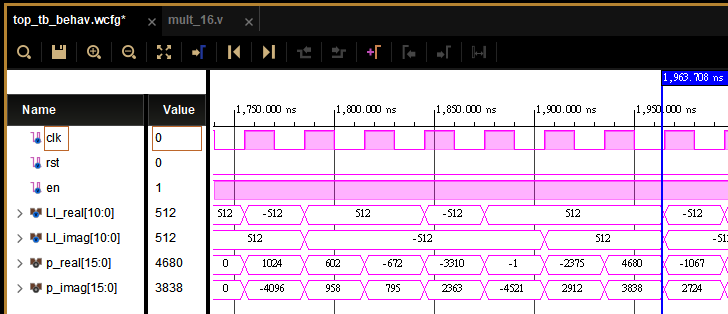
P\_real: MDC IFFT 輸出 real part

P\_imag: MDC IFFT 輸出 imaginary part

Input part:



Output part:



The timing diagram of post-synthesis simulation results of 32-point MDC IFFT:

Rst: 重置

Clk: 時脈

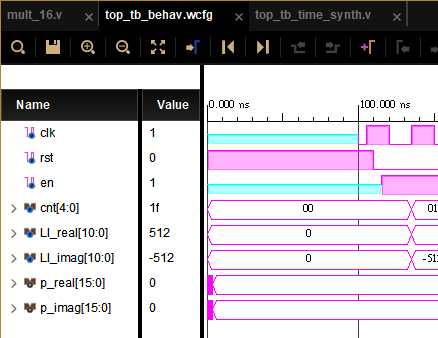
LI\_real: MDC IFFT 輸入 real part

LI\_imag: MDC IFFT 輸入 imaginary part

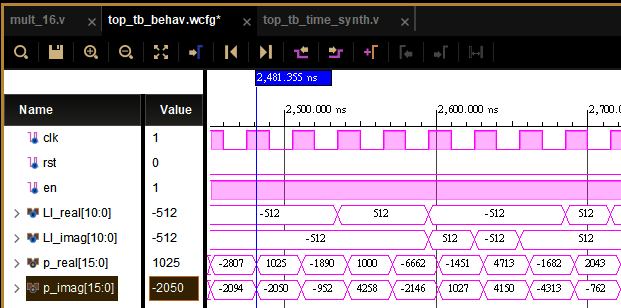
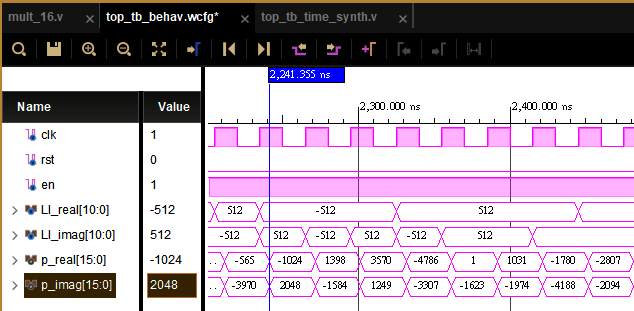
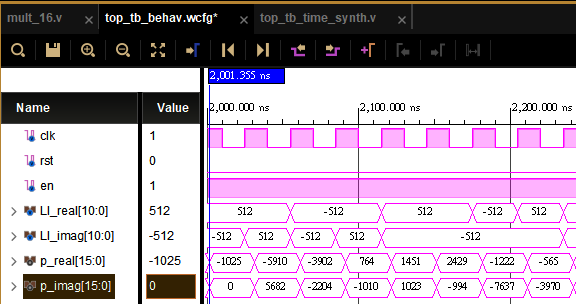
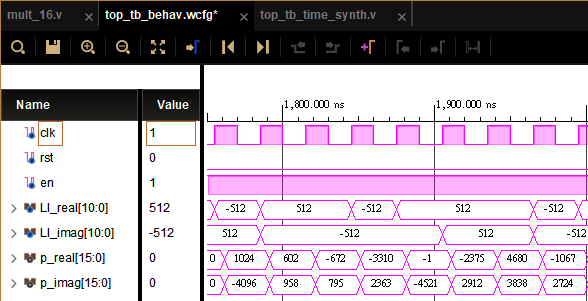
P\_real: MDC IFFT 輸出 real part

P\_imag: MDC IFFT 輸出 imaginary part

Global reset:



Output:



The timing diagram of post-implementation simulation results of 32-point MDC IFFT:

Rst: 重置

Clk: 時脈

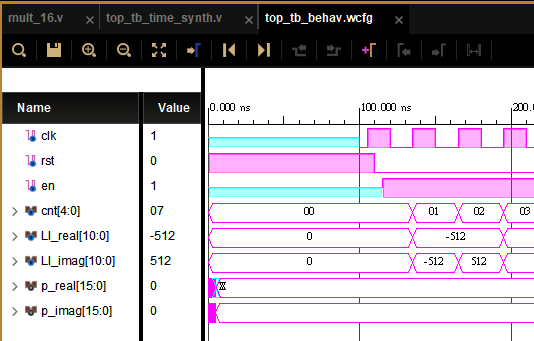
LI\_real: MDC IFFT 輸入 real part

LI\_imag: MDC IFFT 輸入 imaginary part

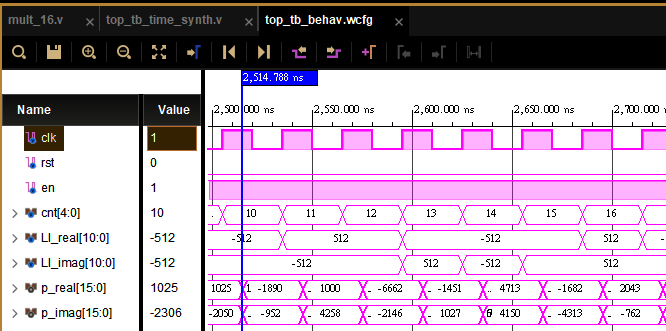
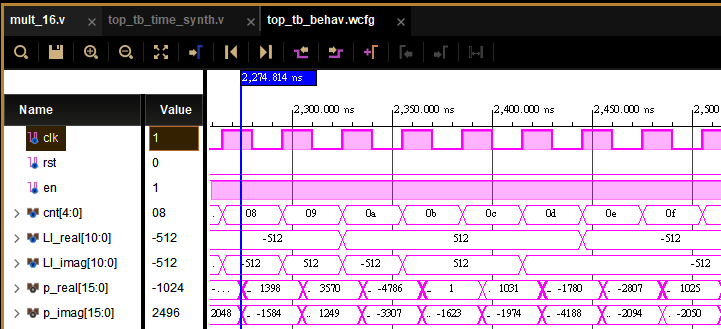
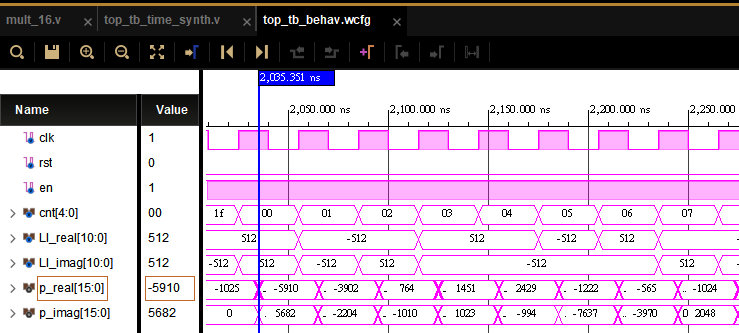
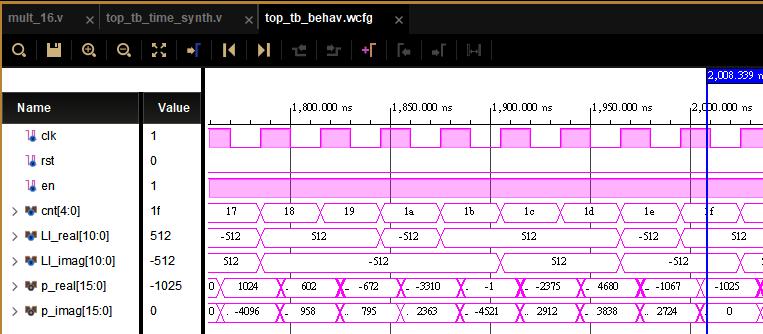
P\_real: MDC IFFT 輸出 real part

P\_imag: MDC IFFT 輸出 imaginary part

Global reset:

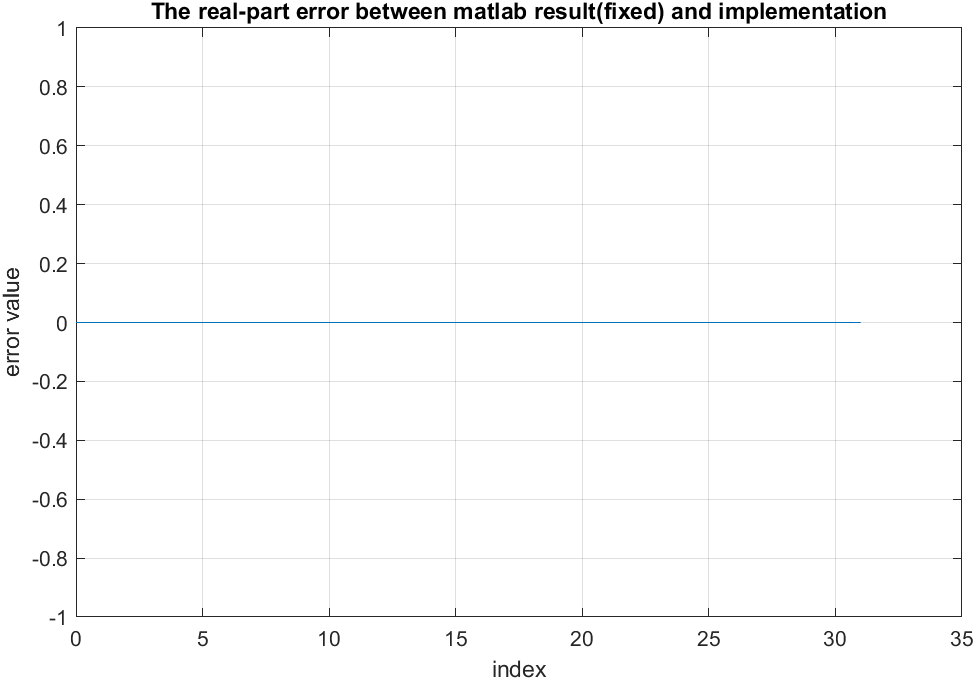


Output:

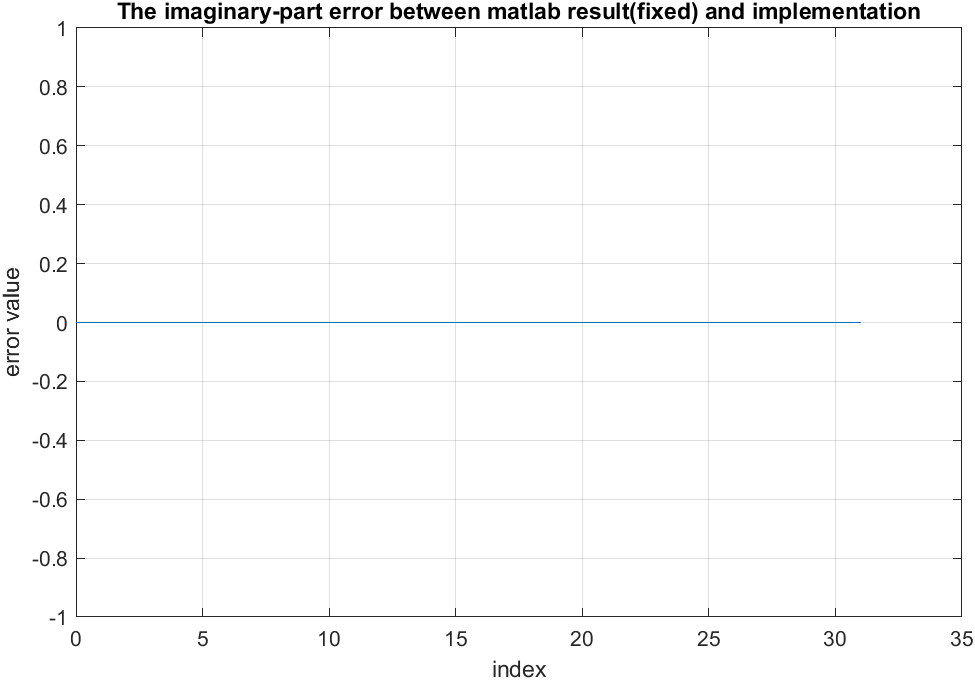


Compare with the Matlab results to check your implementation error. Depict the error.

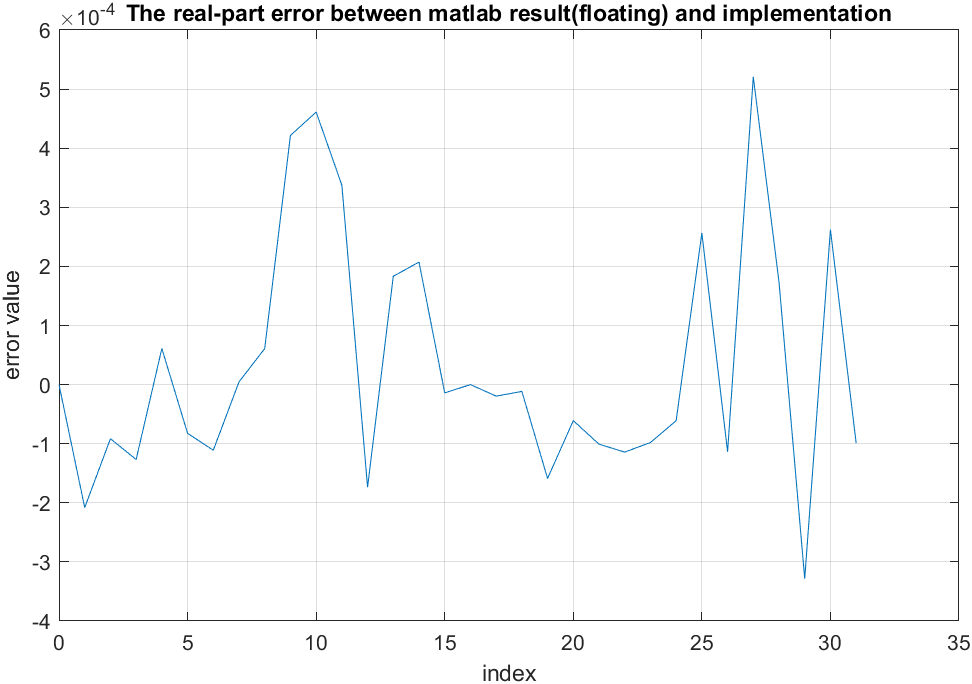
The real-part error between matlab result(fixed) and implementation:



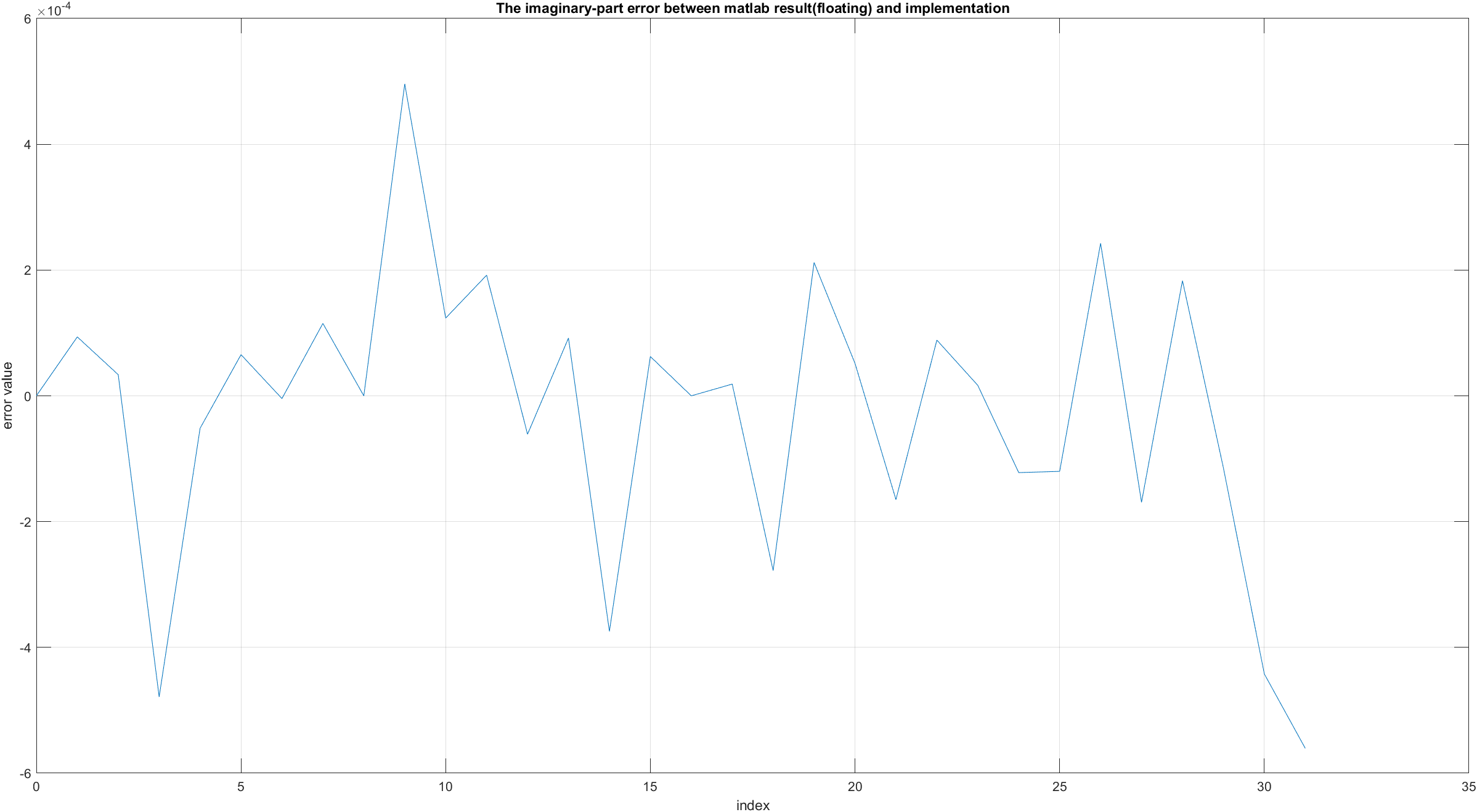
The imaginary-part error between matlab result(fixed) and implementation:



The real-part error between matlab result(floating) and implementation:



The imaginary-part error between matlab result(floating) and implementation:



8. Show your measurement results and paste the measurement results in your report. (demo until 12/19)

Rst: 重置

Clk: 時脈

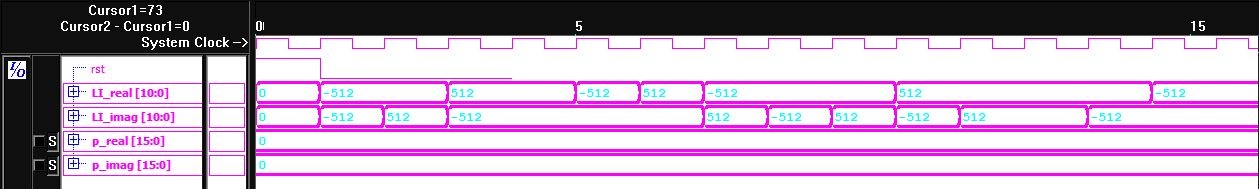
LI\_real: MDC IFFT 輸入 real part

LI\_imag: MDC IFFT 輸入 imaginary part

P\_real: MDC IFFT 輸出 real part

P\_imag: MDC IFFT 輸出 imaginary part

Input part:



Output part

