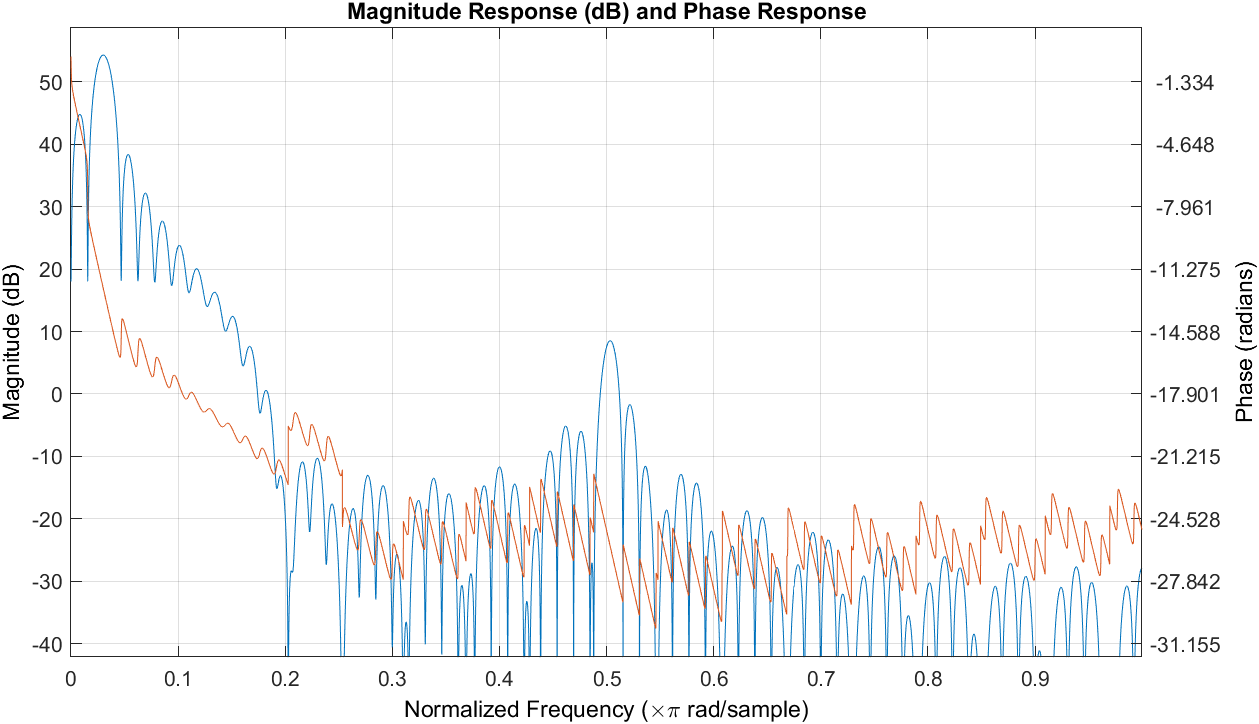
**DCCDL LAB3**

**Verilog**

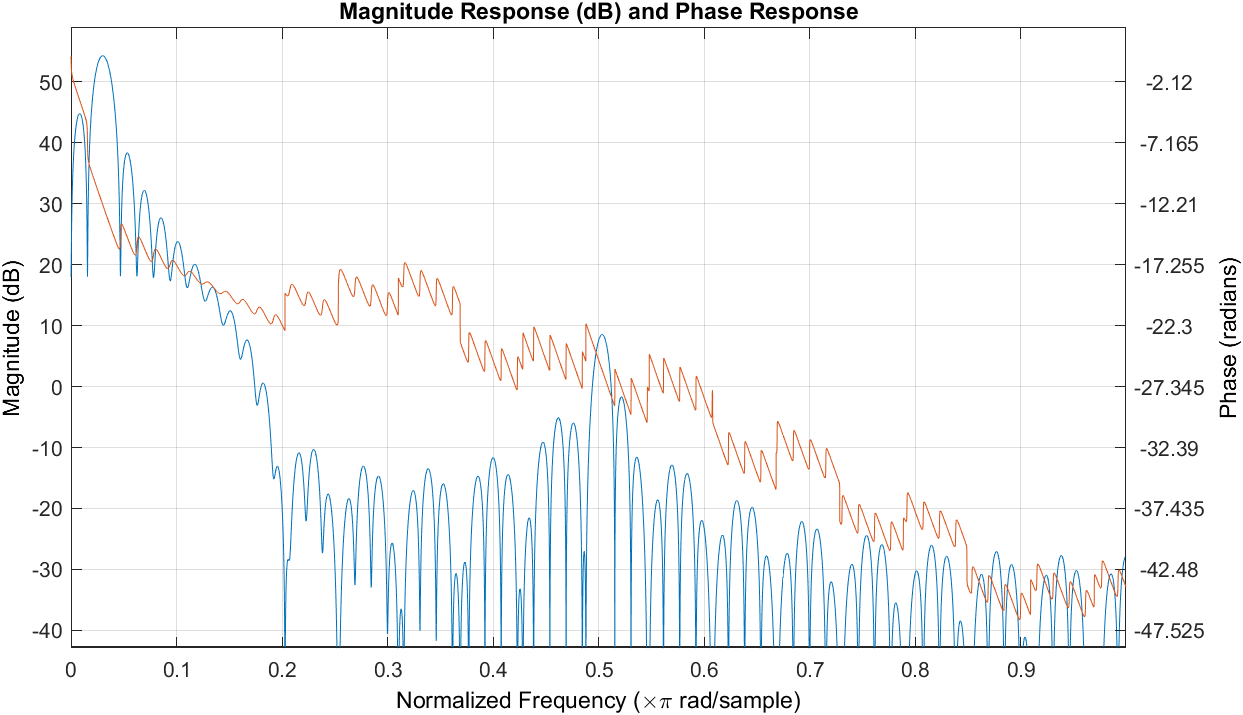
電機碩一 111521035 林豪澤

1. Compare the frequency-domain magnitude responses of ideal floating-point representation in 1 and fixed-point representation in 3 and 4. Please given some explanations about their performances. (20%)

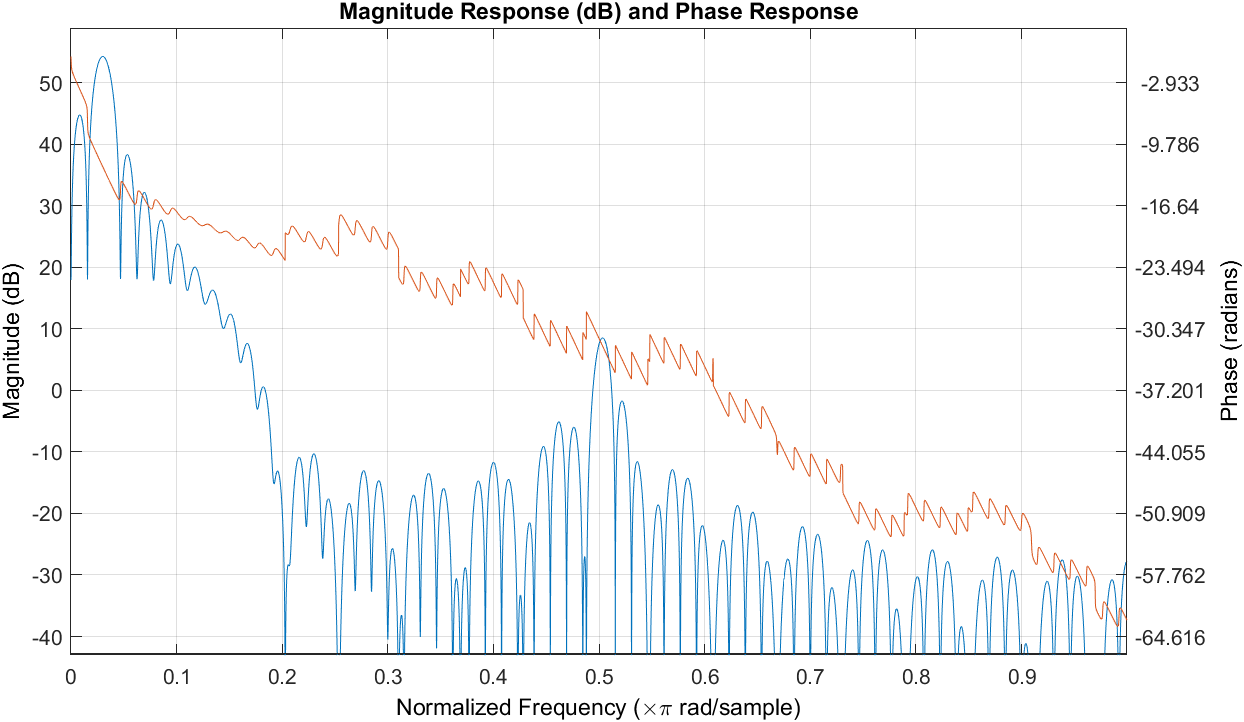
the frequency-domain magnitude response for floating-point:



The frequency-domain magnitude response for fixed-point direct-form FIR filter:



the frequency-domain magnitude response for fixed-point transposed-form FIR filter:

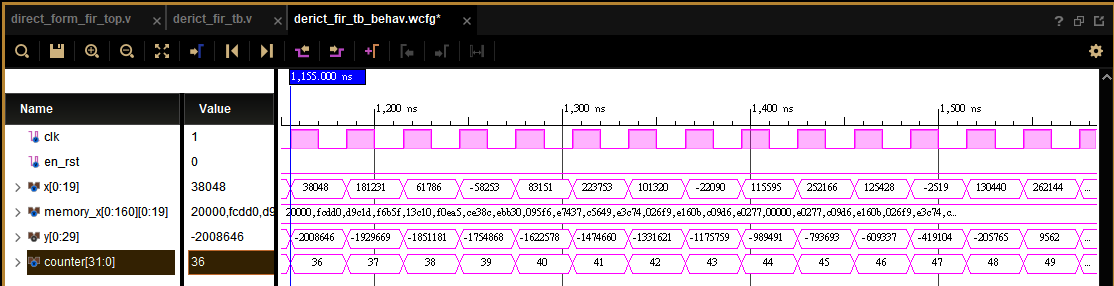
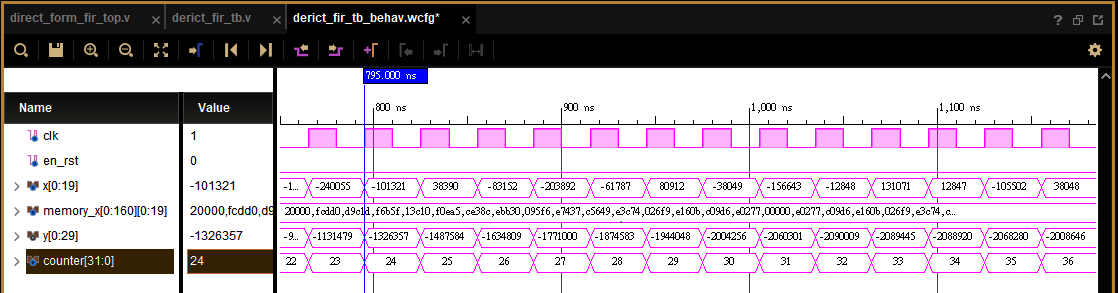
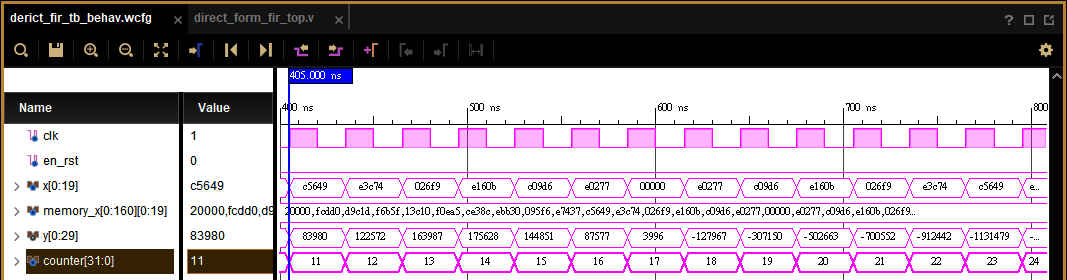
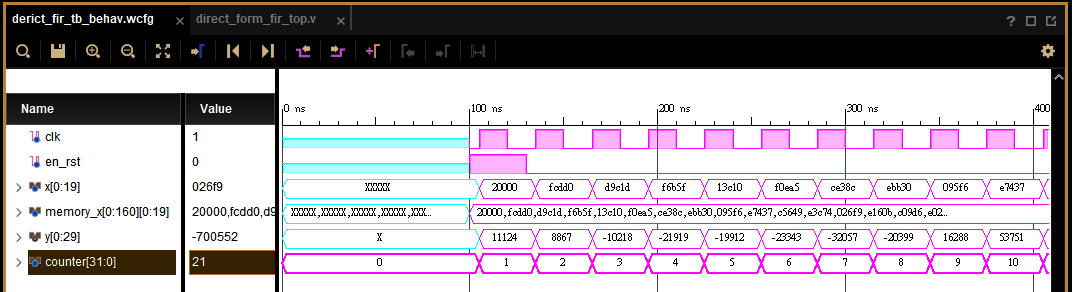


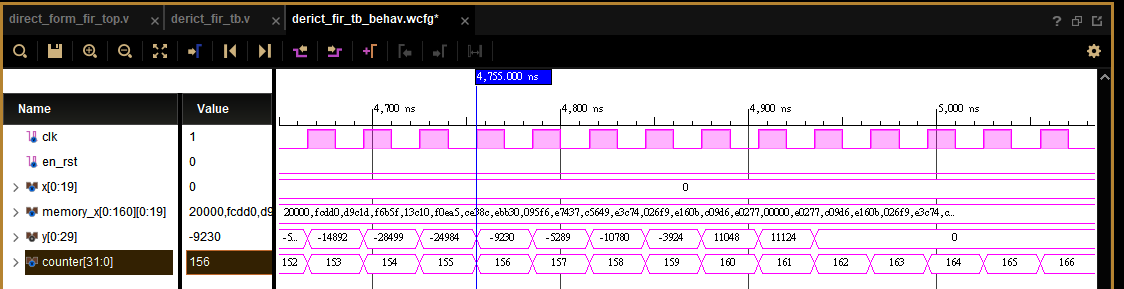
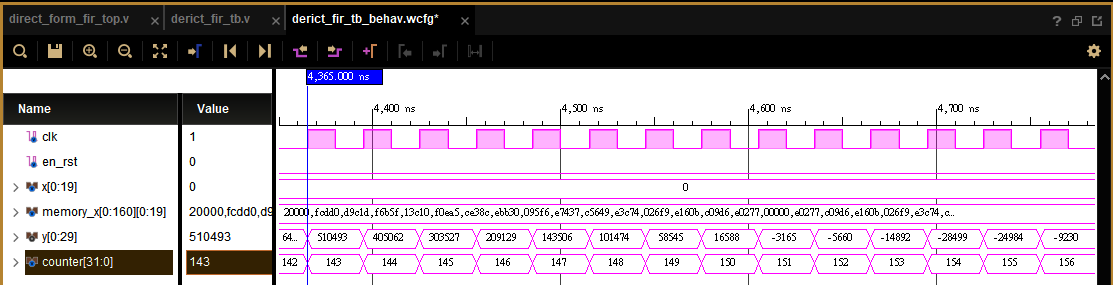
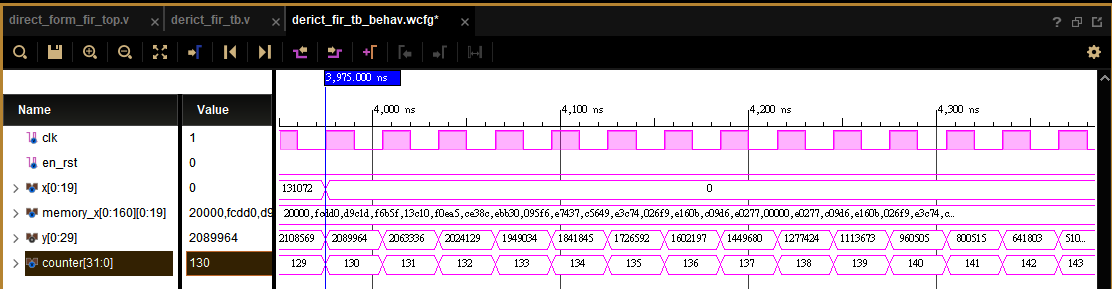
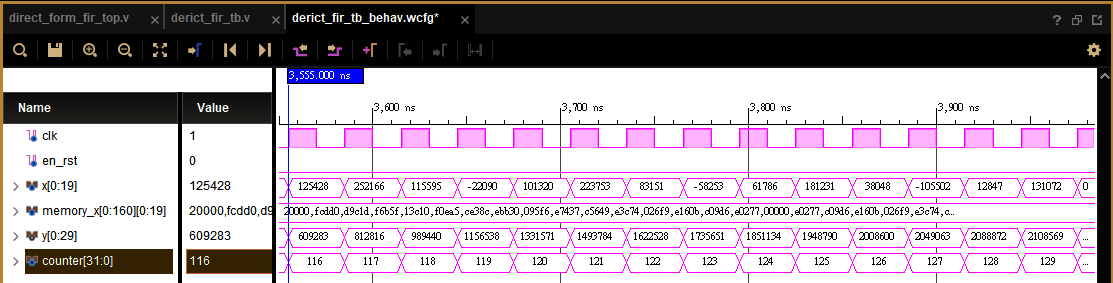
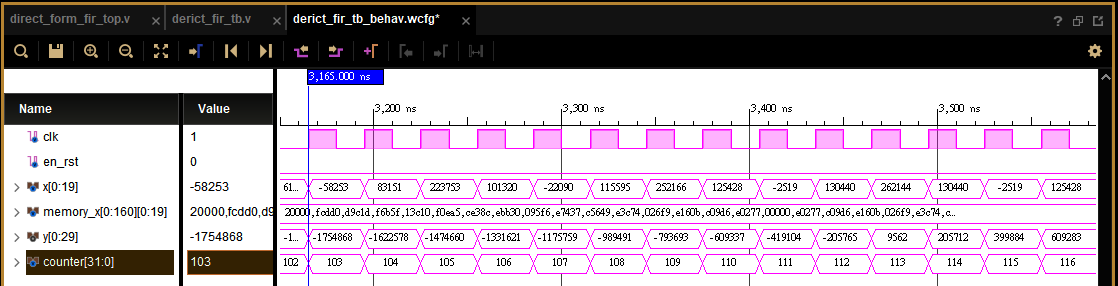
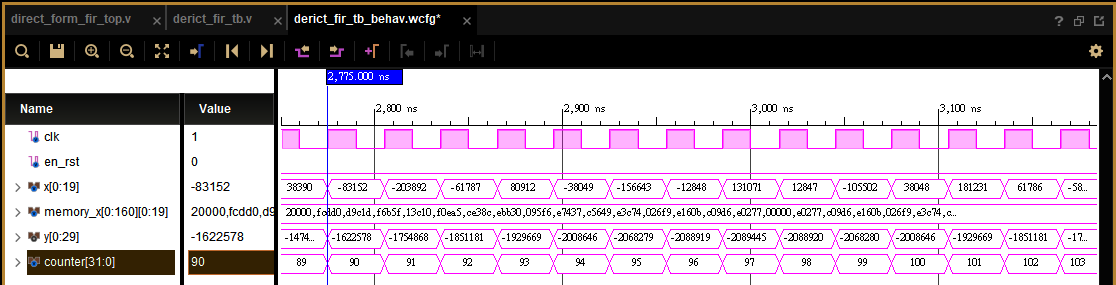
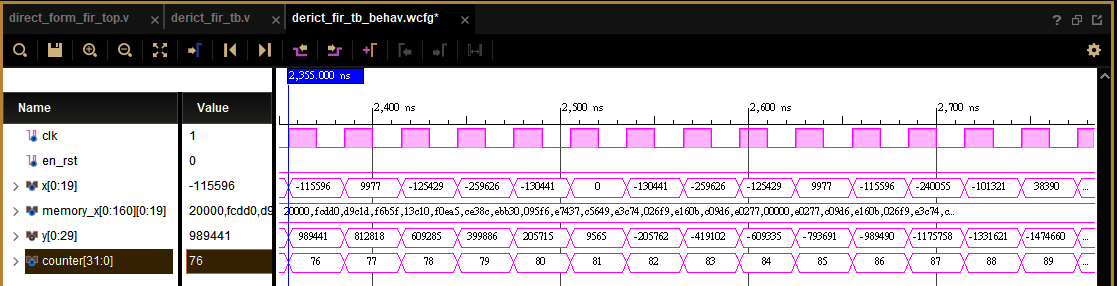
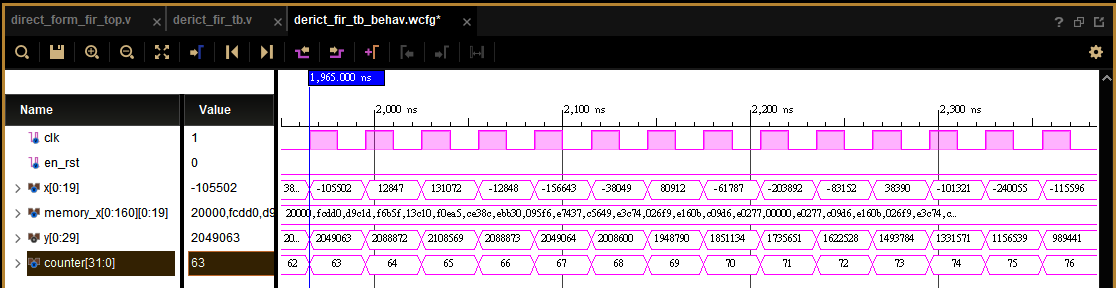
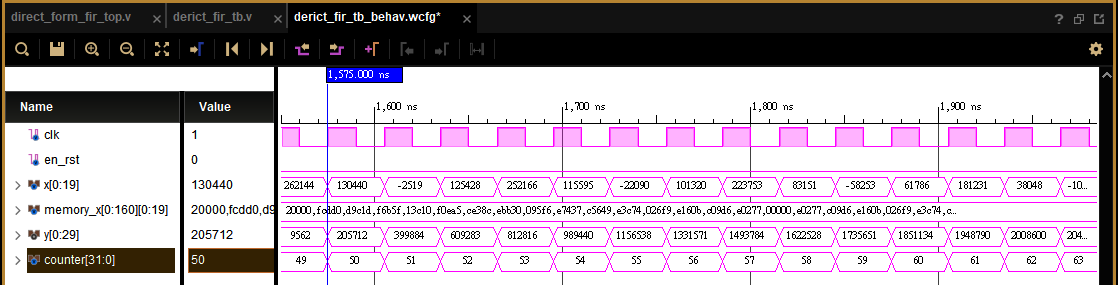
第一張圖為floating-point的frequency response。與direct form、transposed form的frequency response比較過後可以觀察到三者之間的magnitude並無太大的變化。

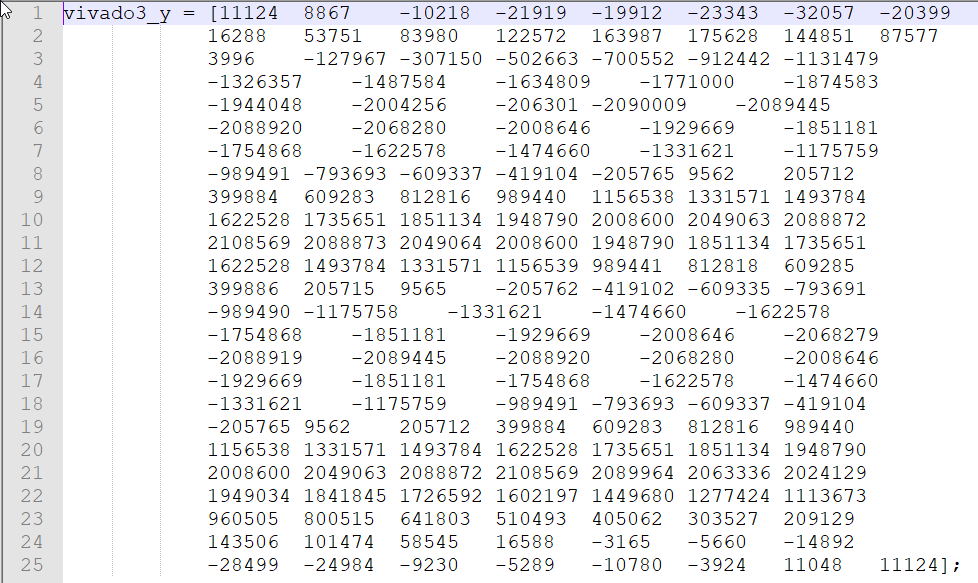
但是因為進行過truncation後其Phase出現了些微差距，隨著truncation之後的小數位越來越少，其與ideal的Phase差距越大。可以觀察到truncation之後的小數位越少其Phase變化的幅度越大。

1. Please implement the direct form FIR. Use 𝑥[𝑛] as the input. Check the behavior and post-route simulation results. Compare the results with the Matlab floating-point results. (30%)

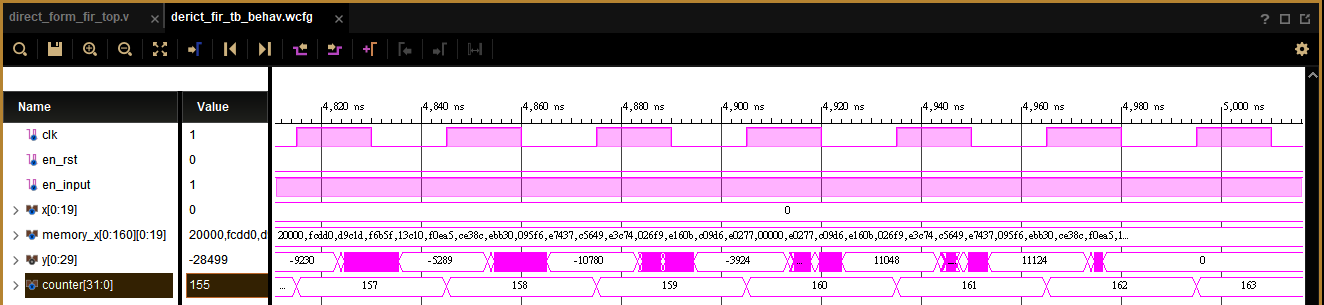
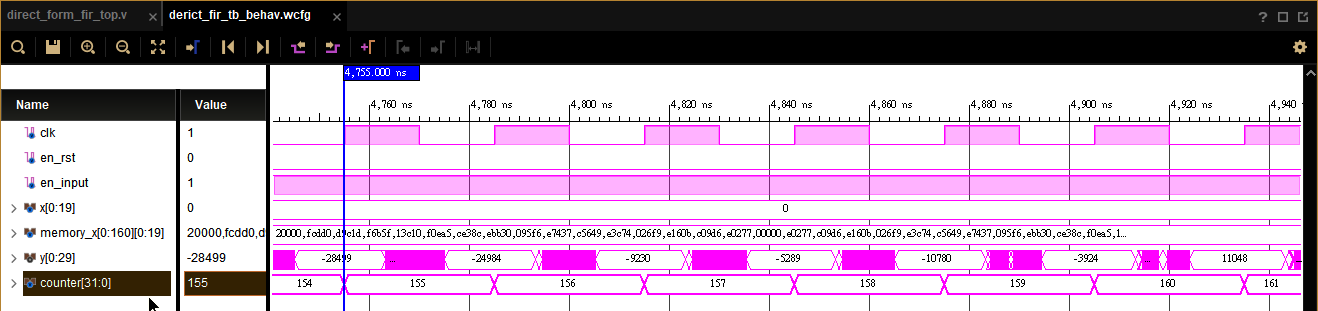
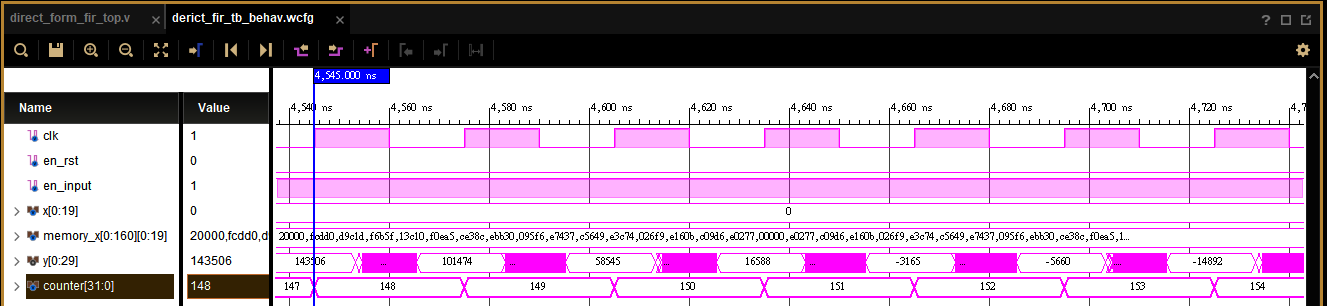
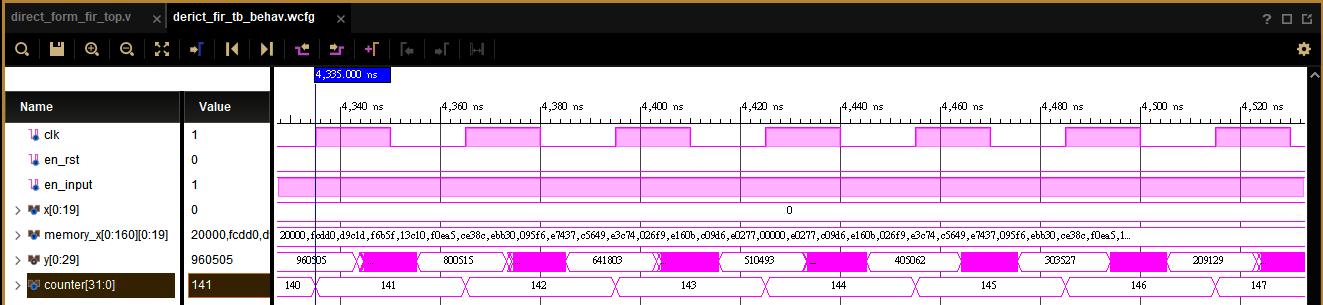
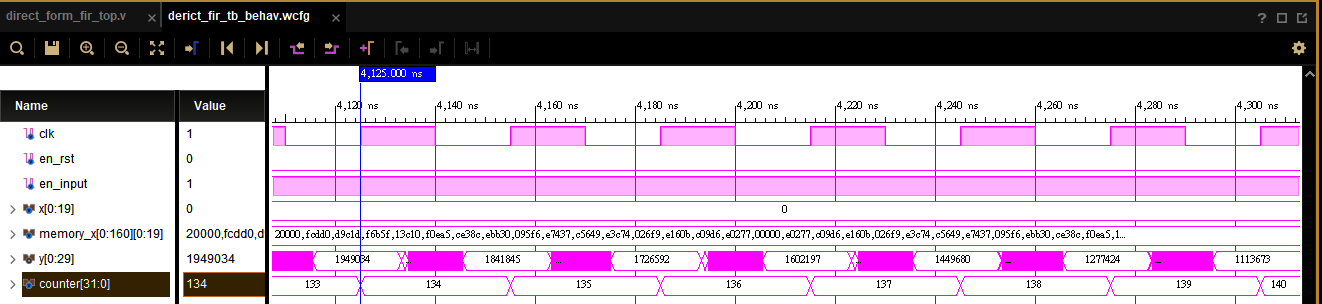
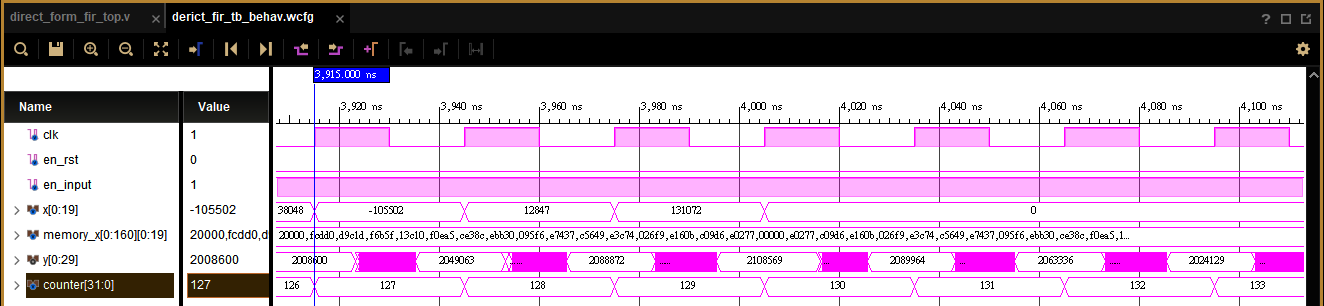
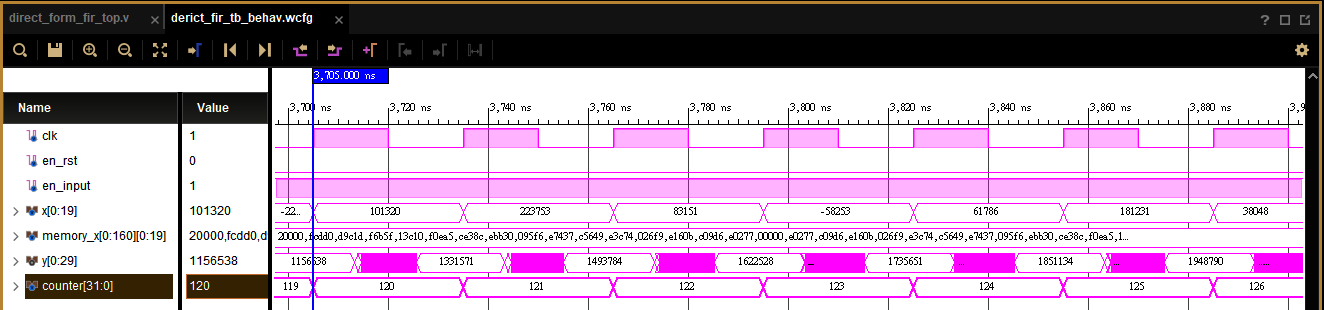
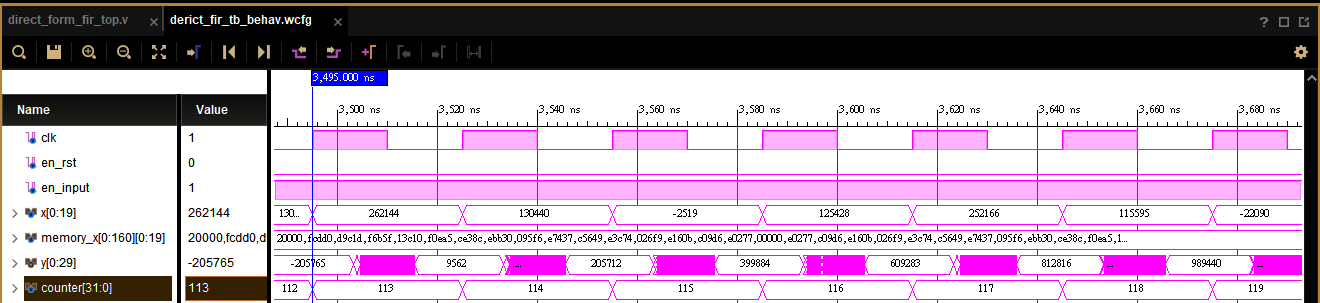
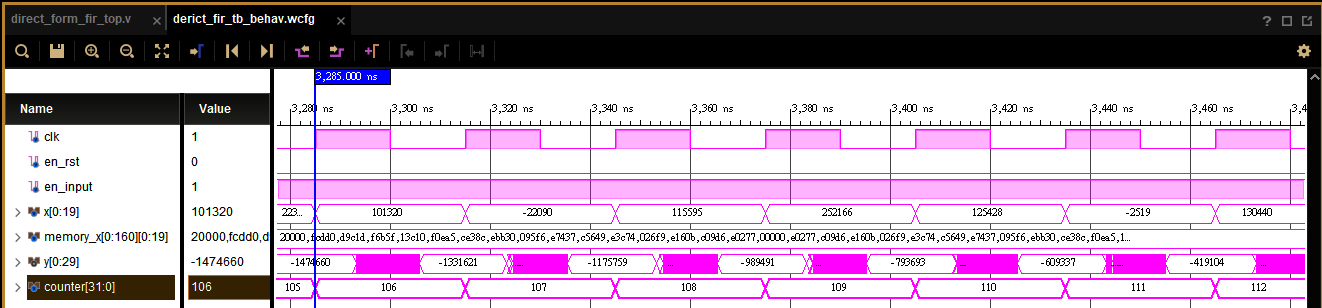
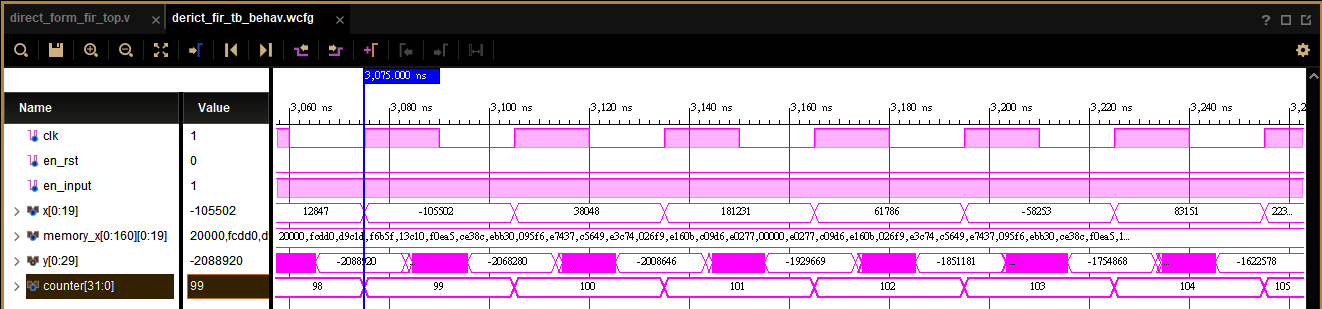
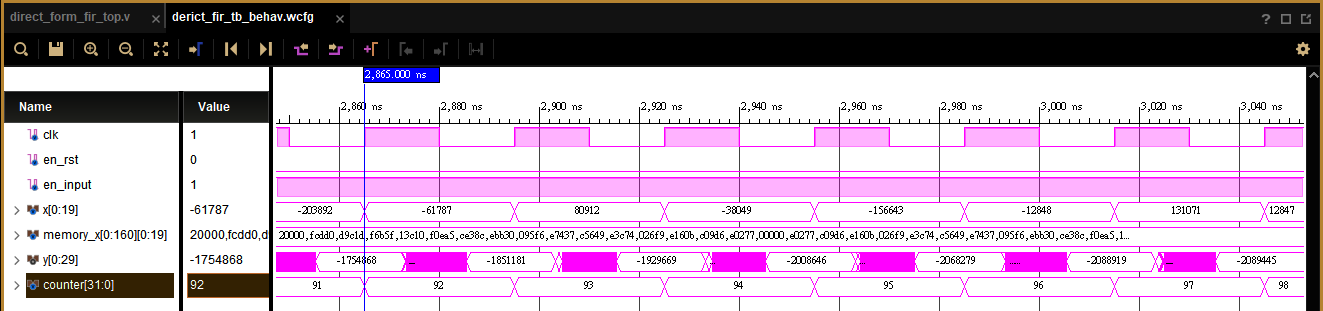
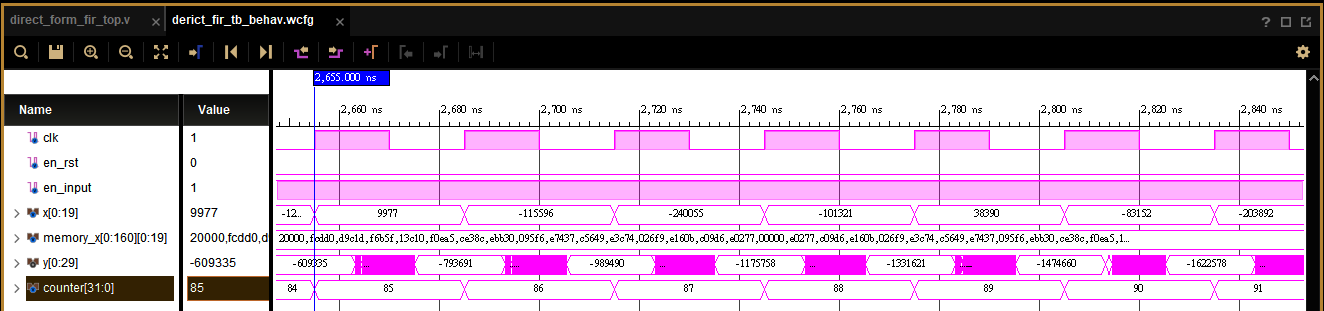
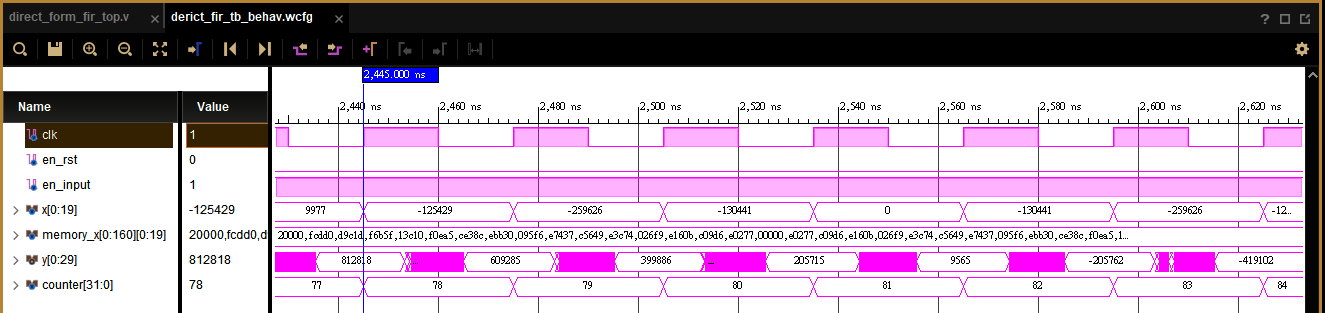
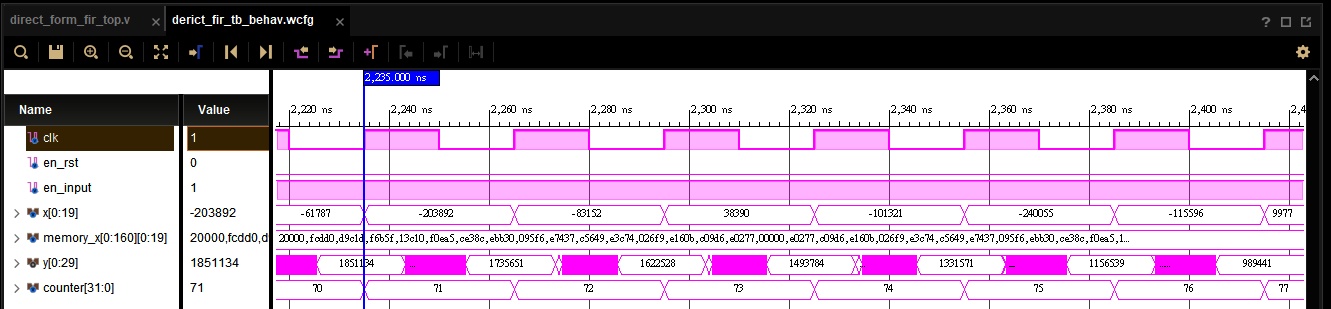
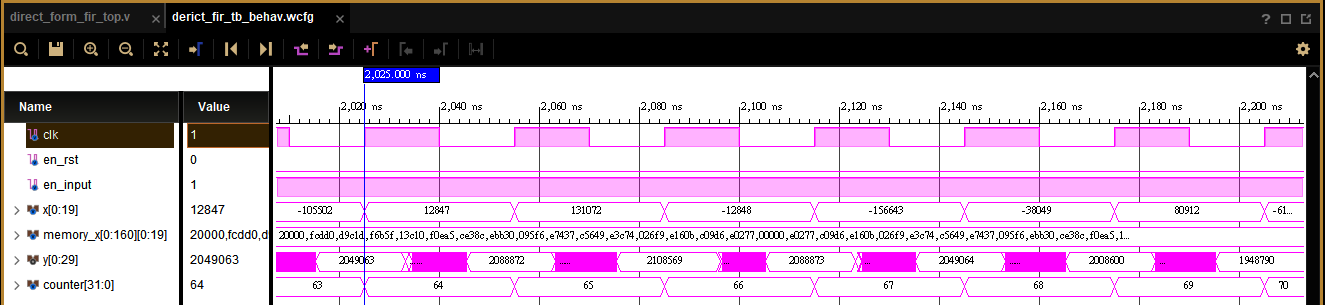
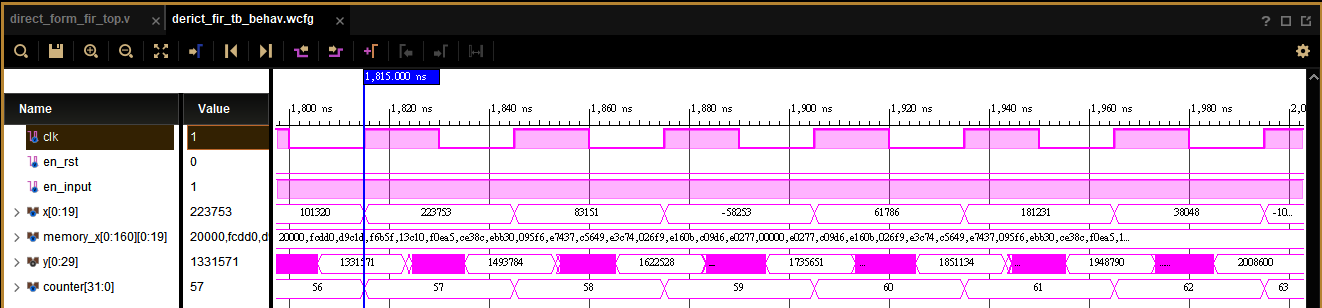
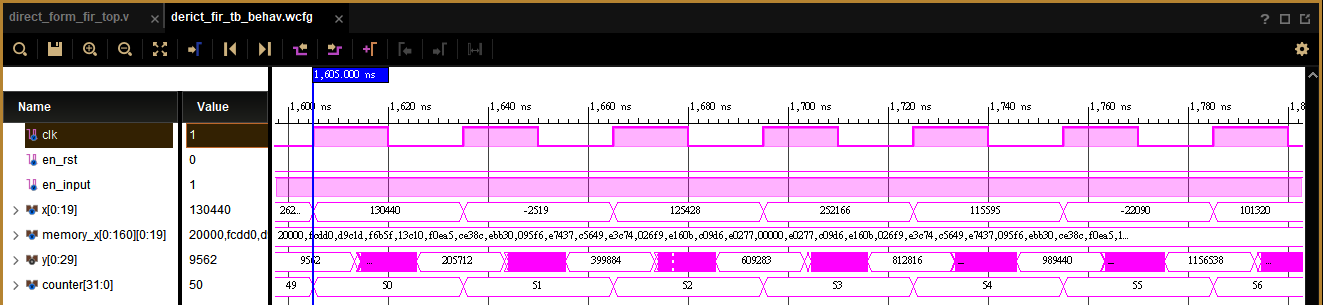
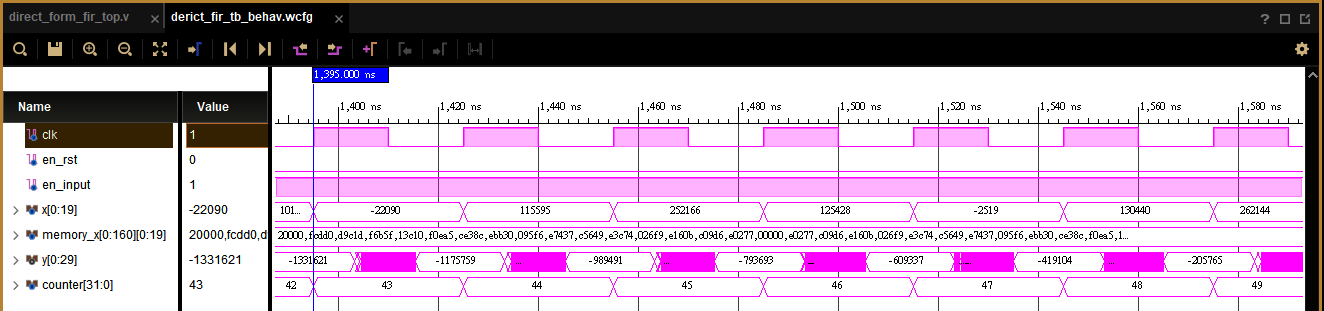
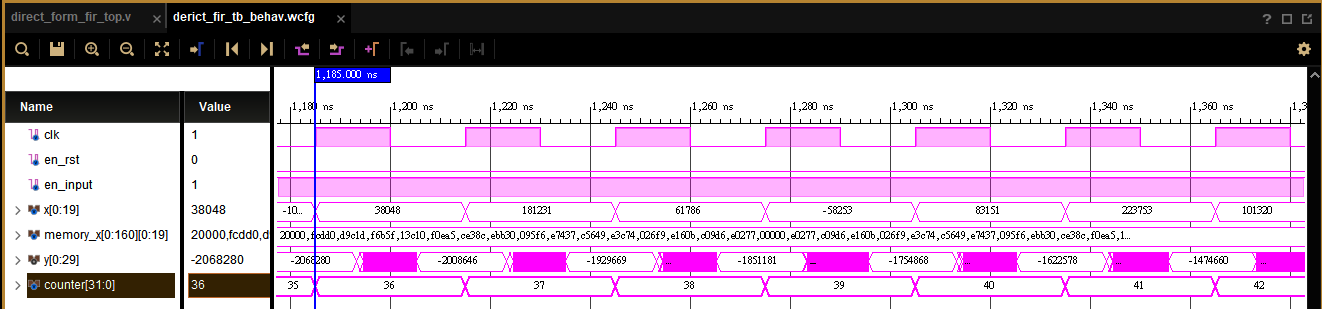
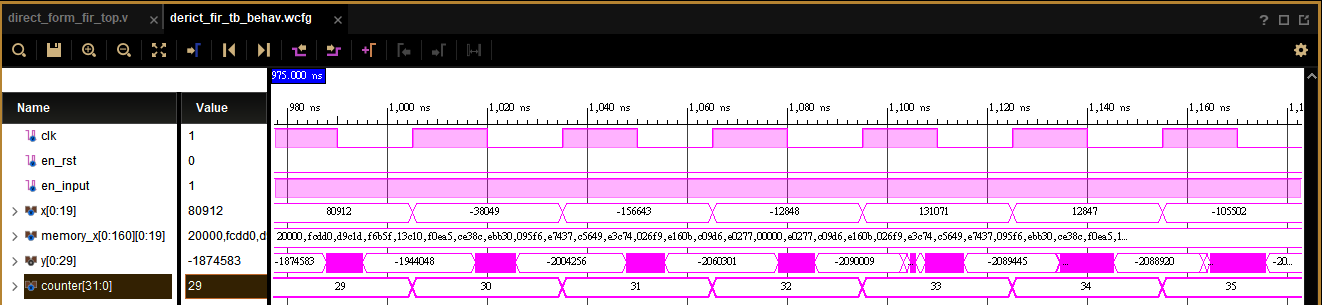
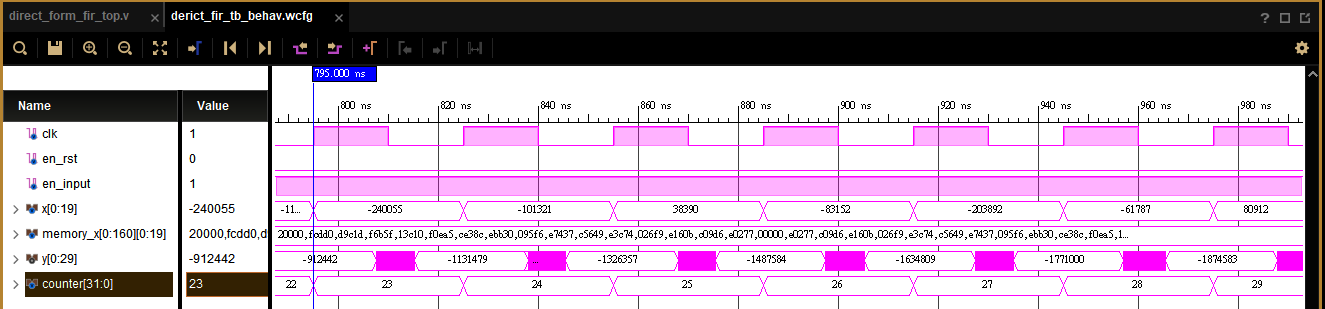
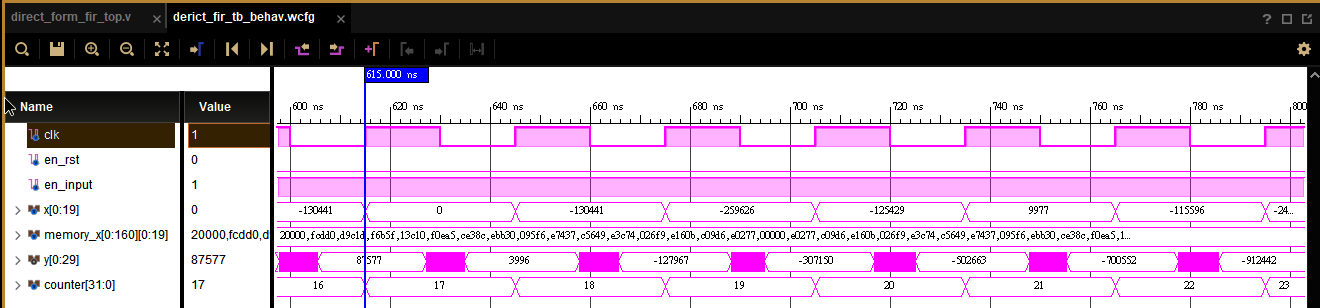
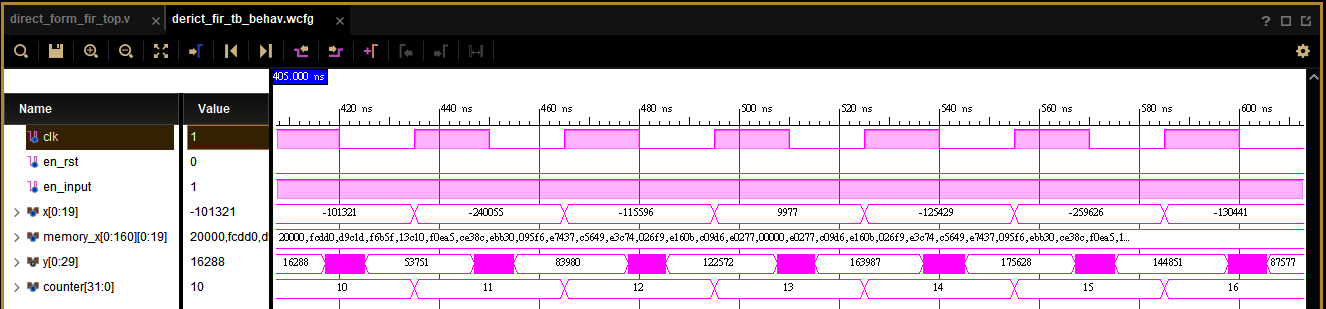
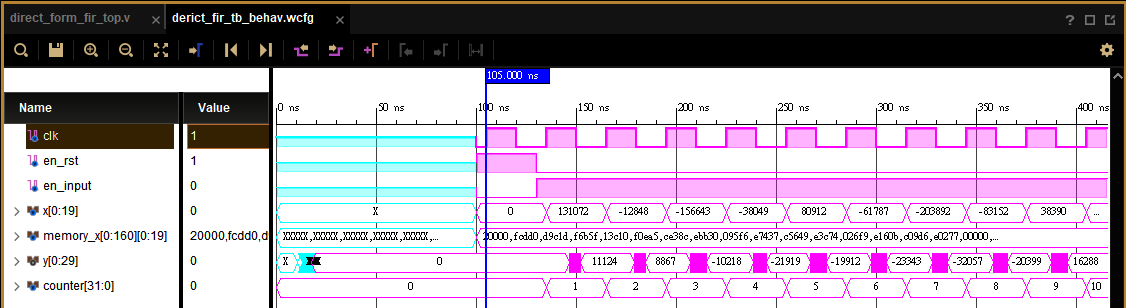
Direct form behavior simulation:



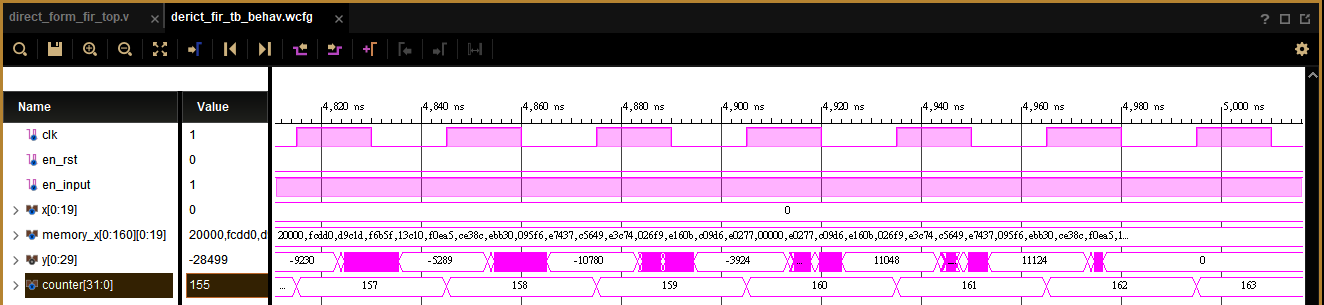
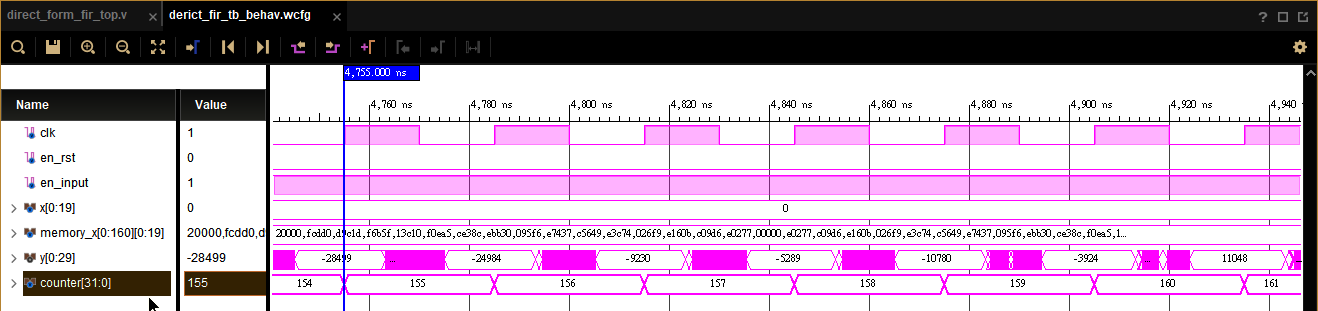
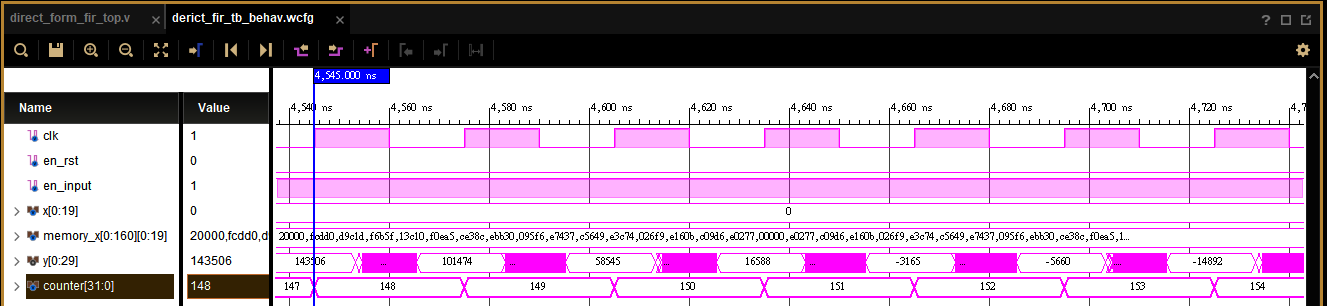
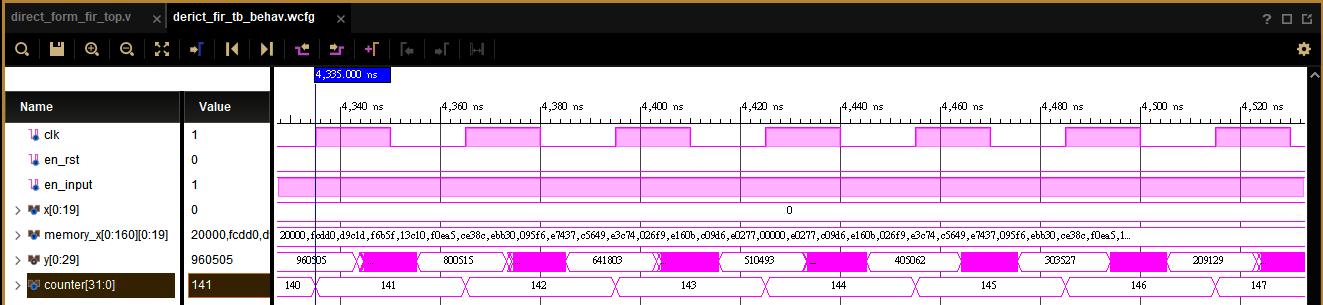
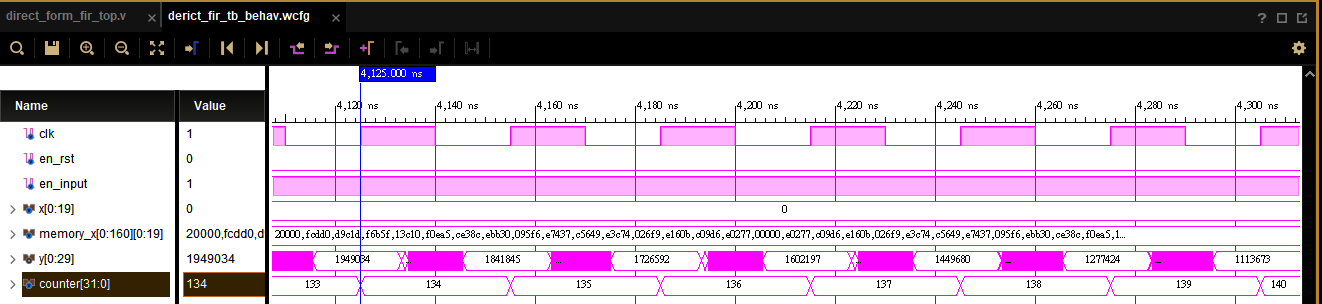
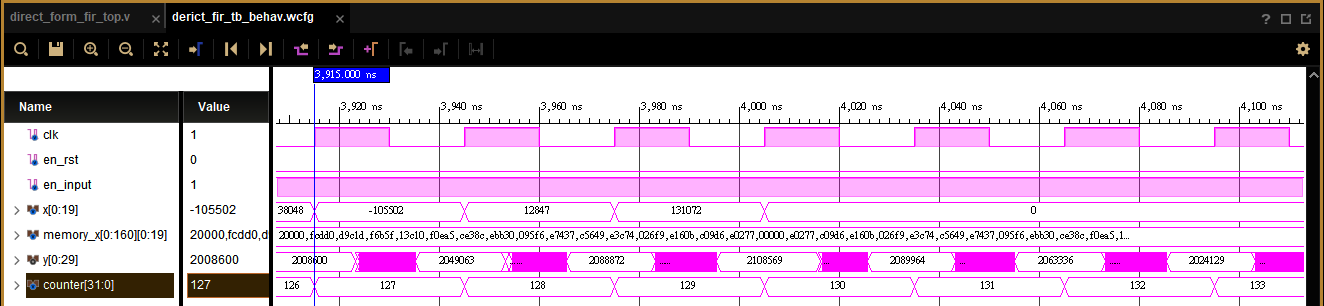
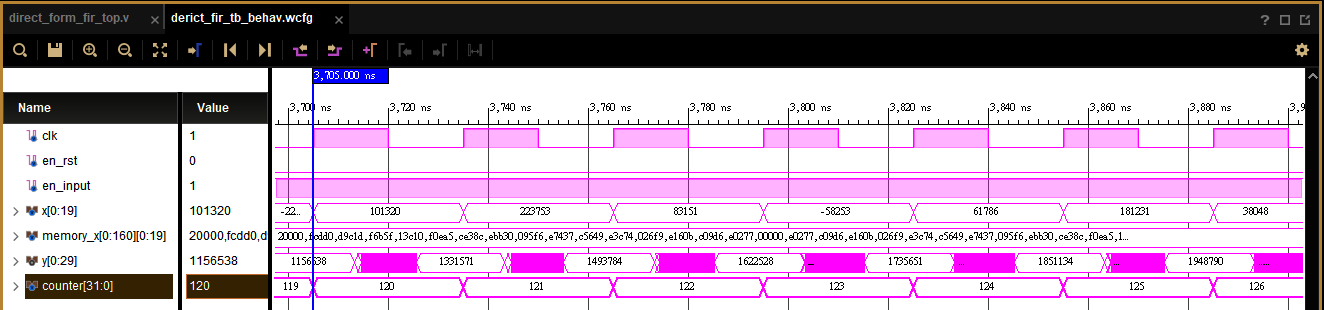
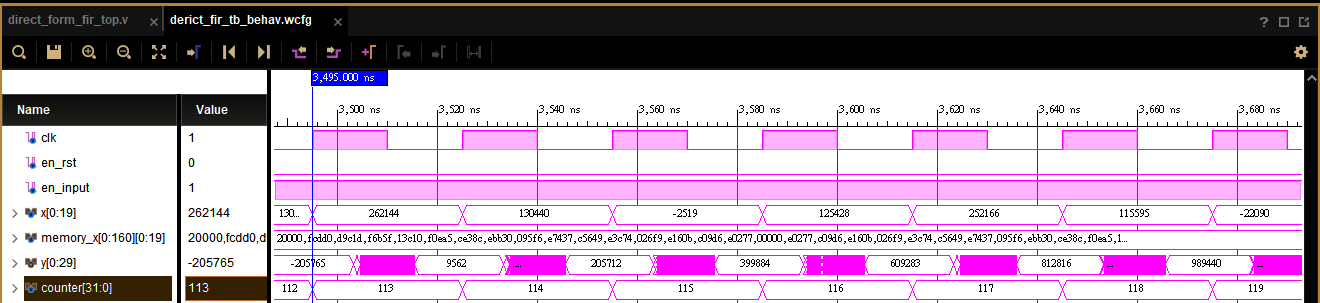
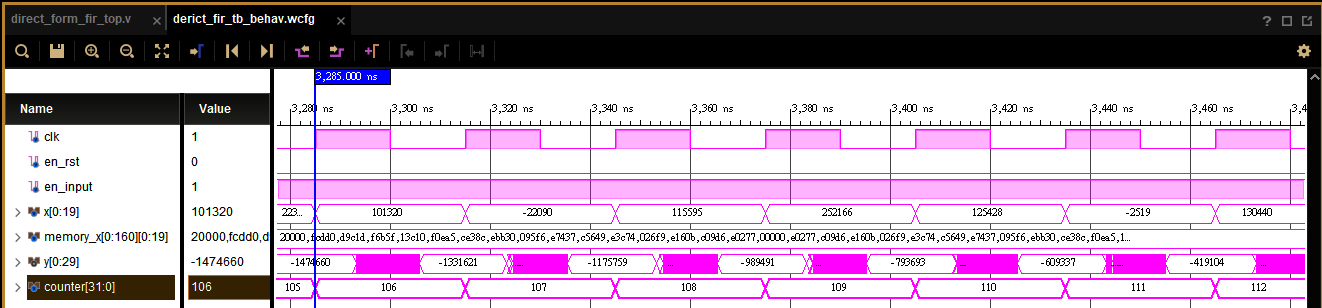
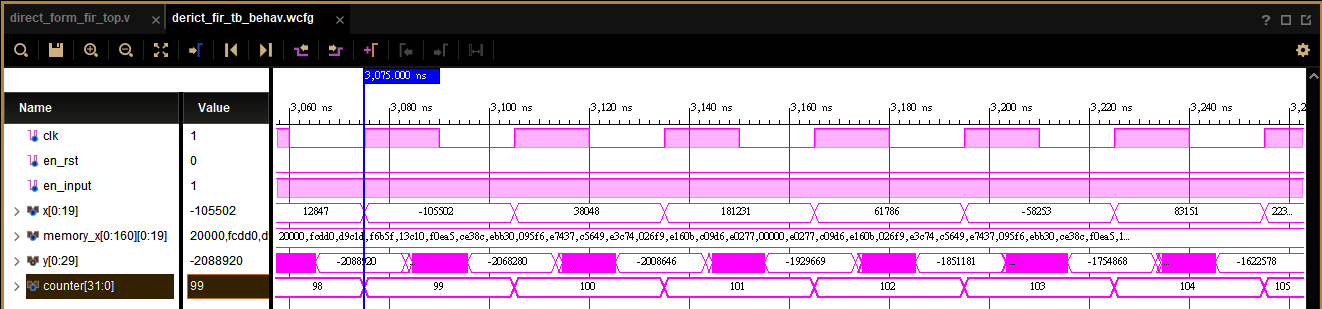
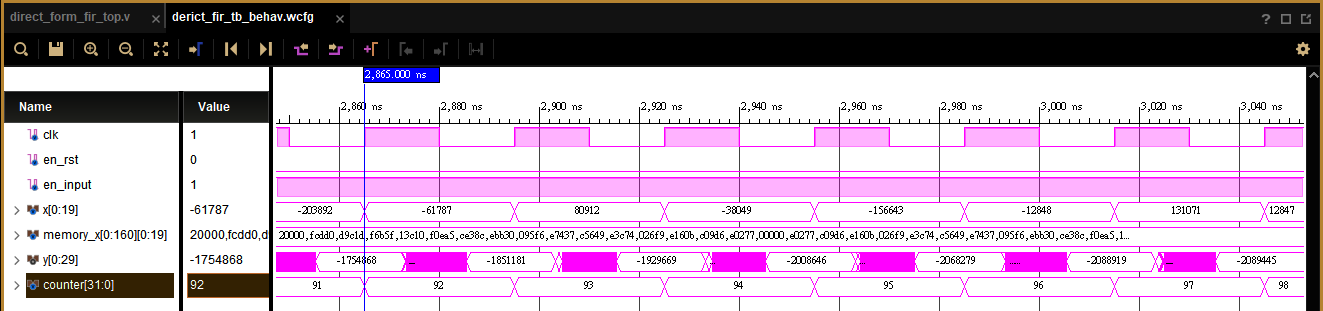
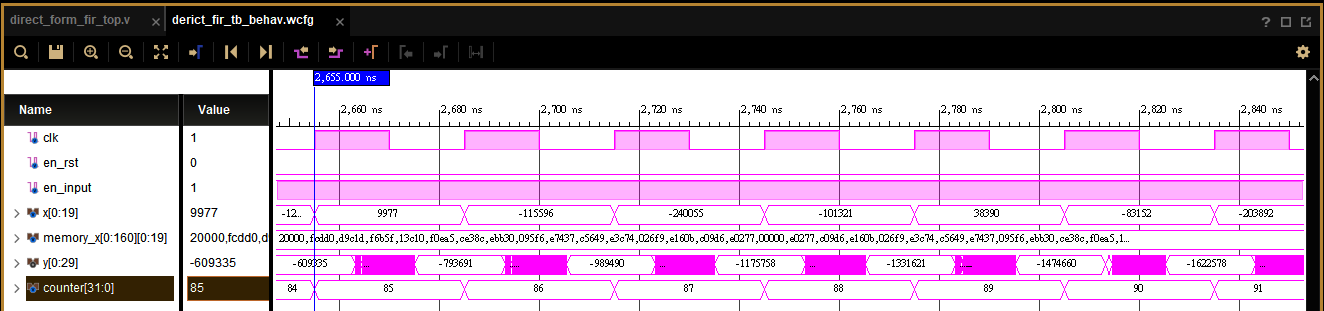
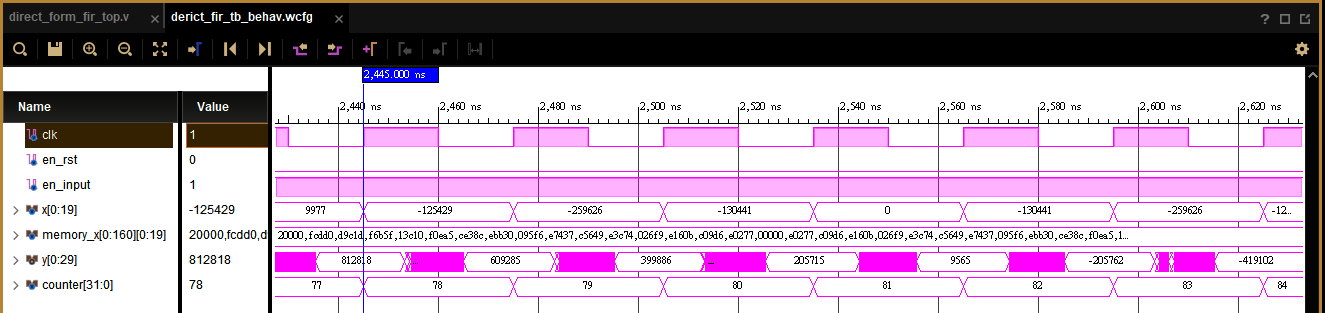
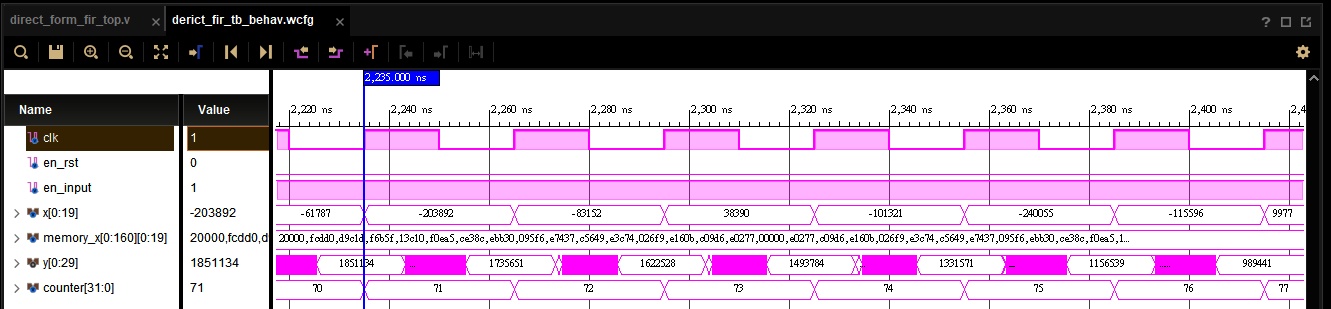
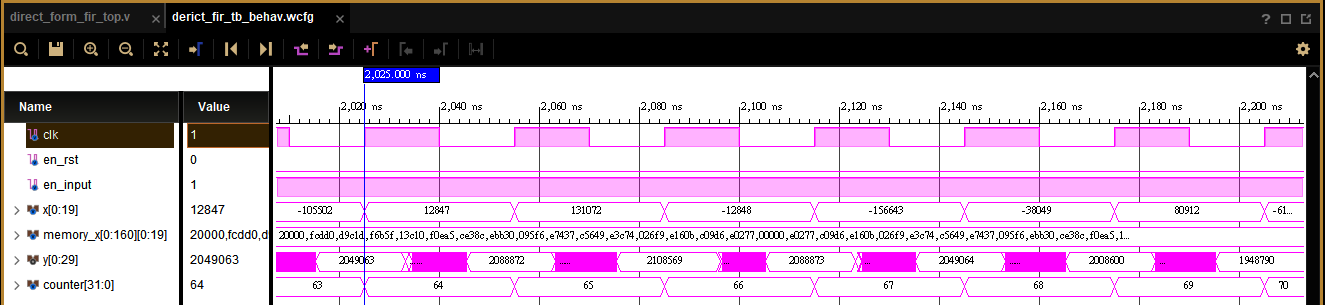
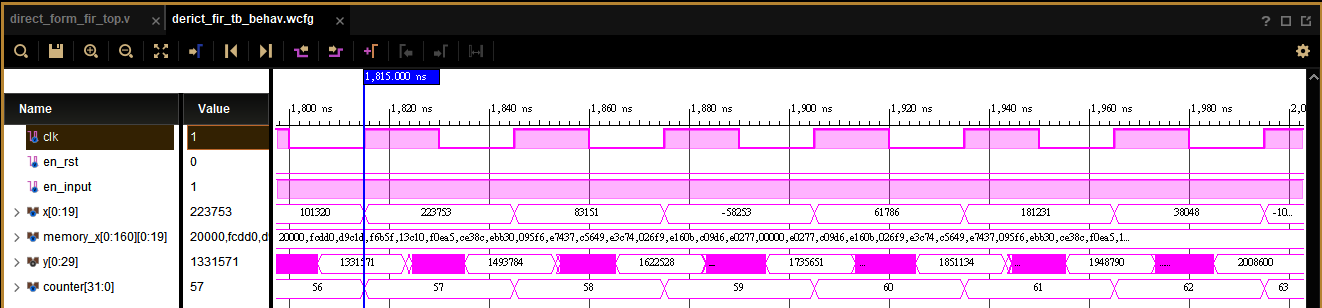
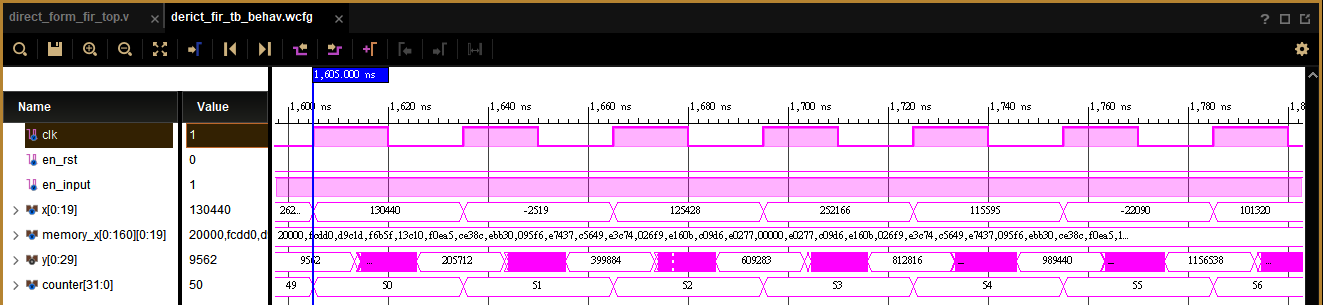
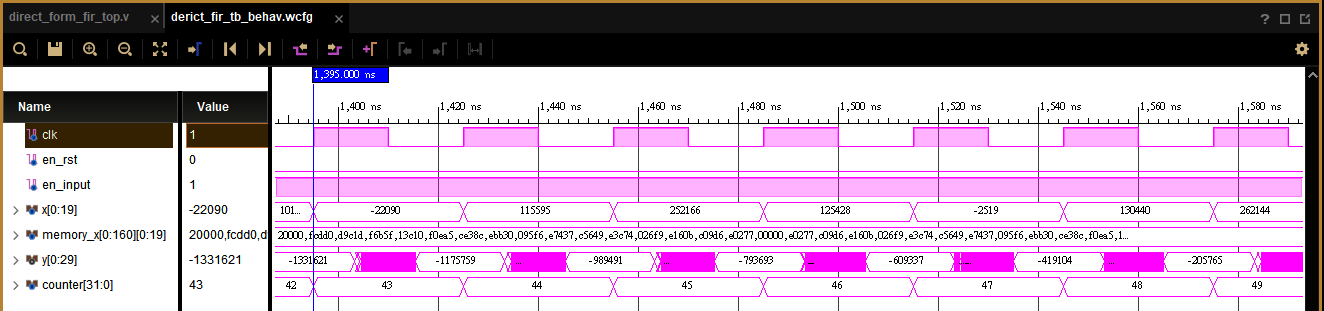
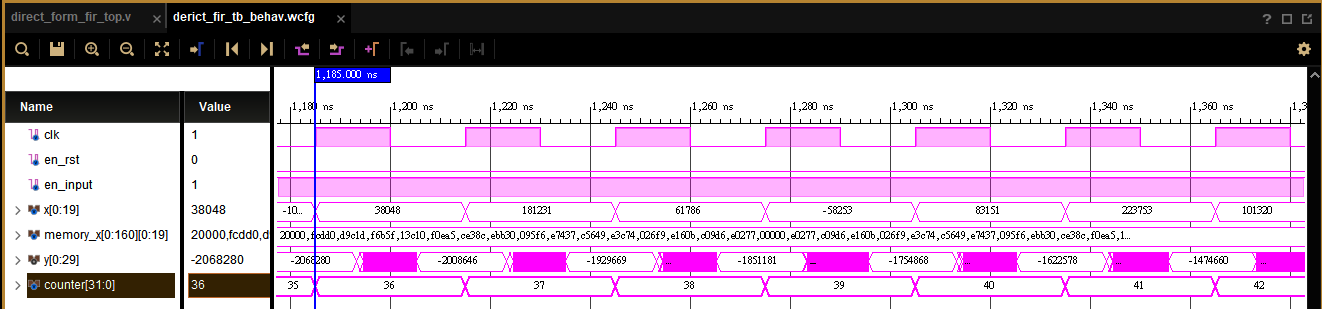
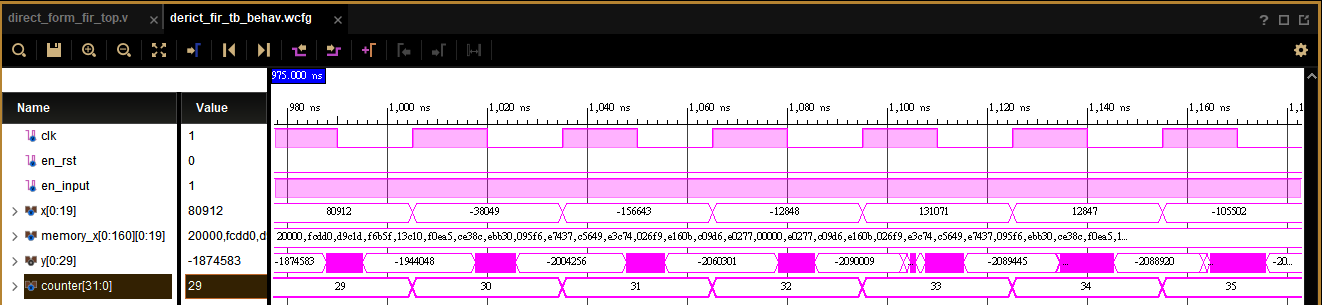
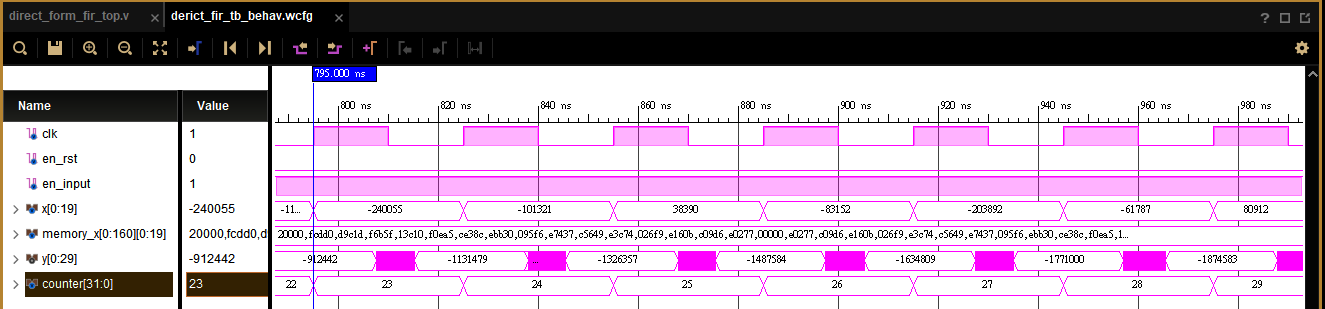
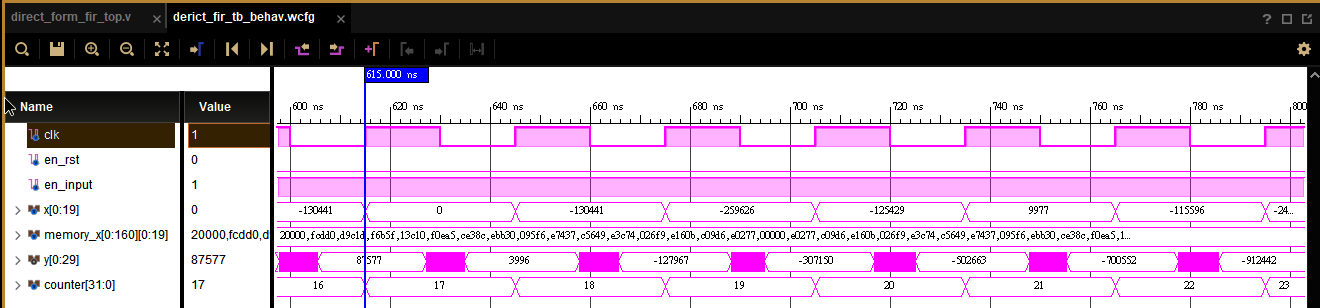
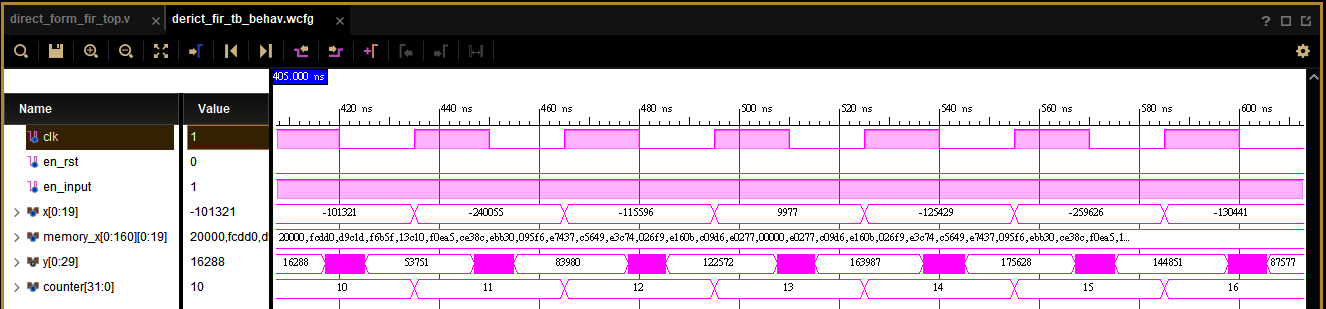
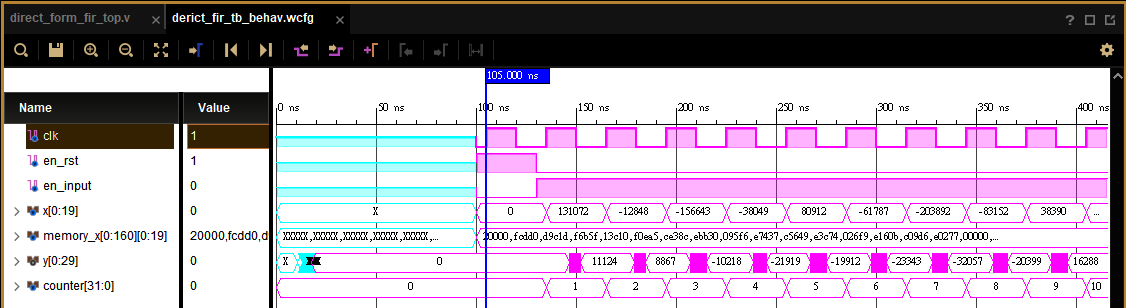




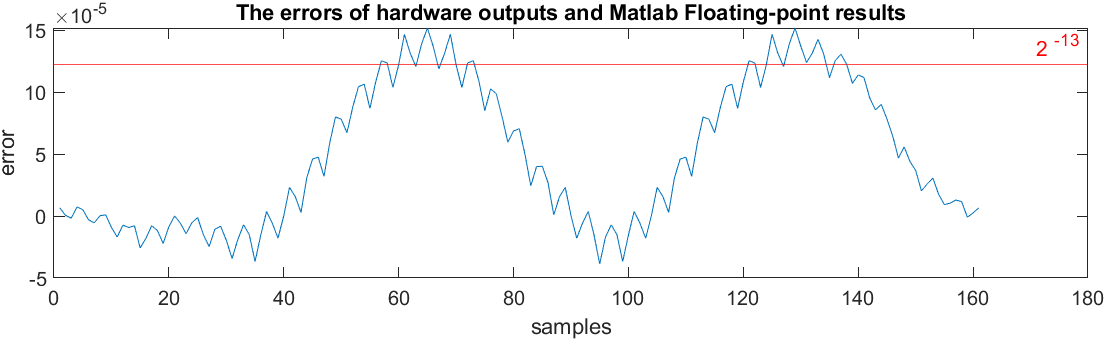
Post-Synthesis timing simulation:



Post-implementation timing simulation:

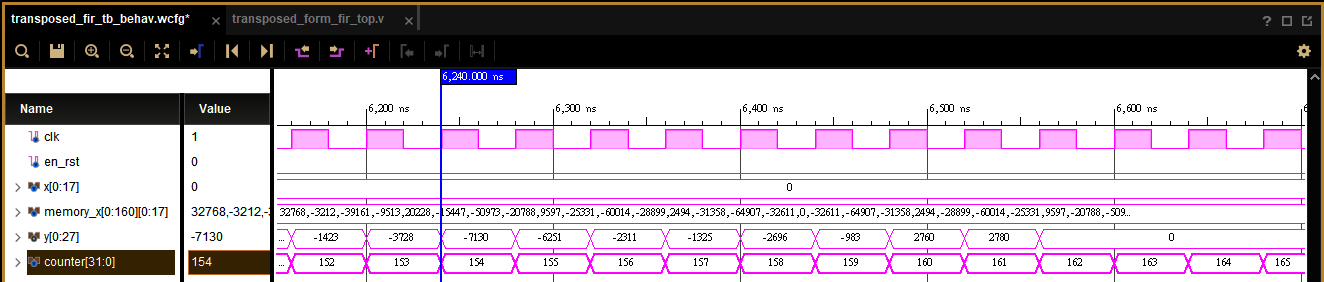
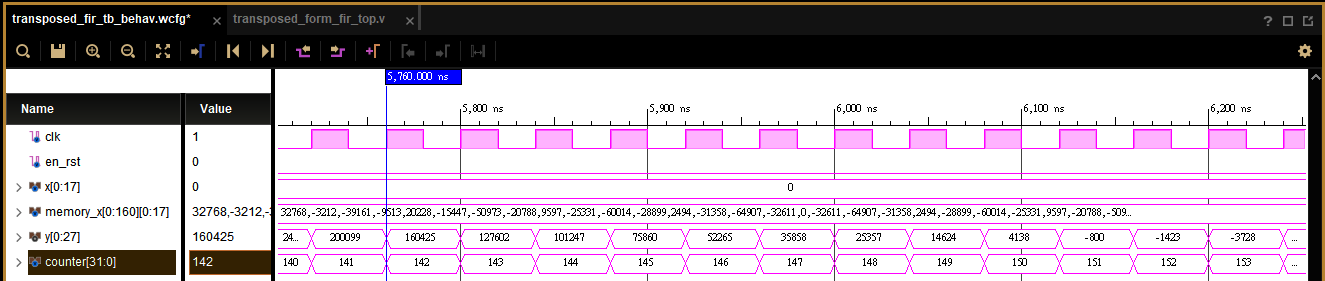
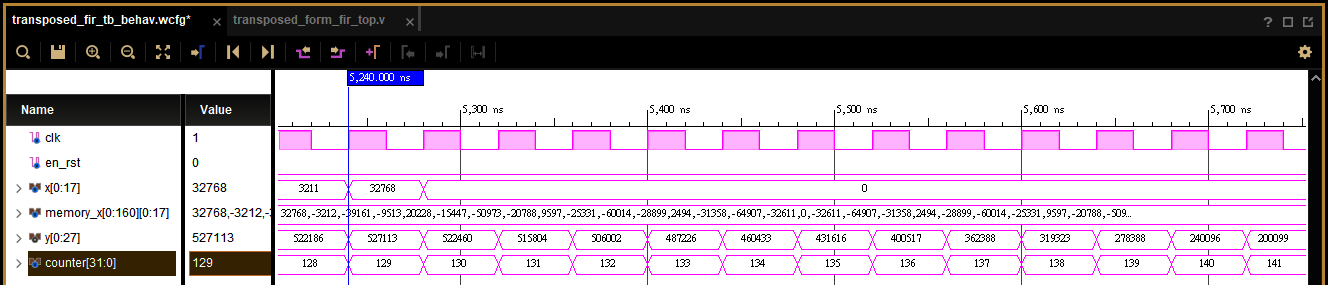
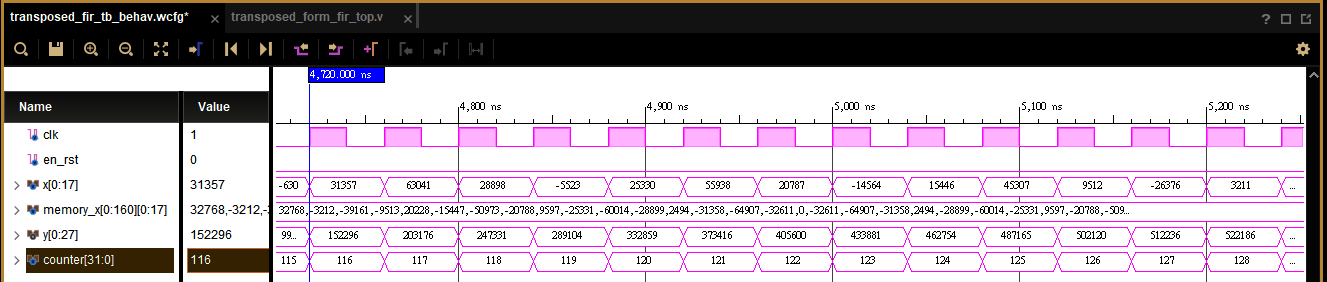
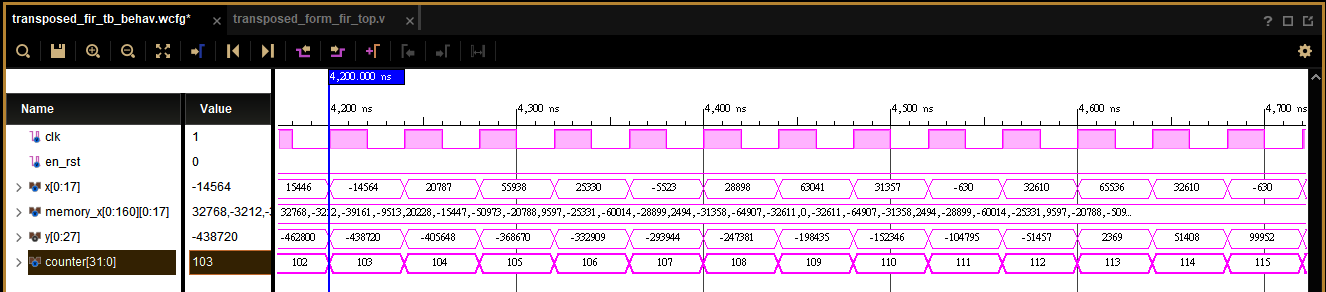
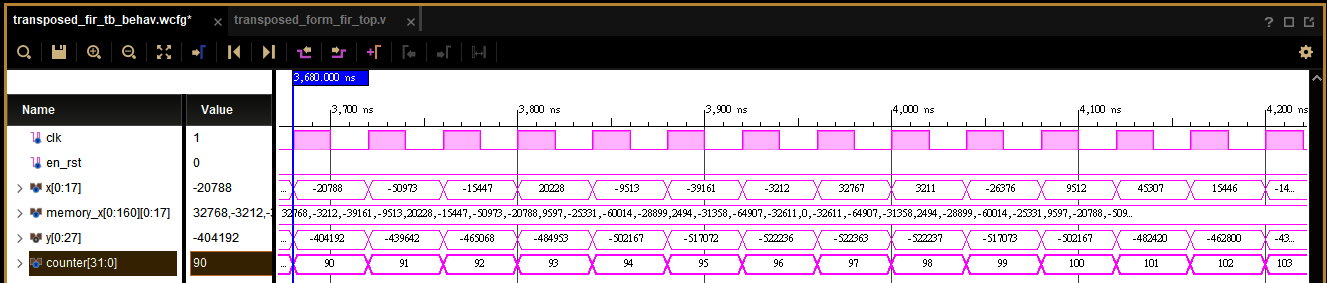
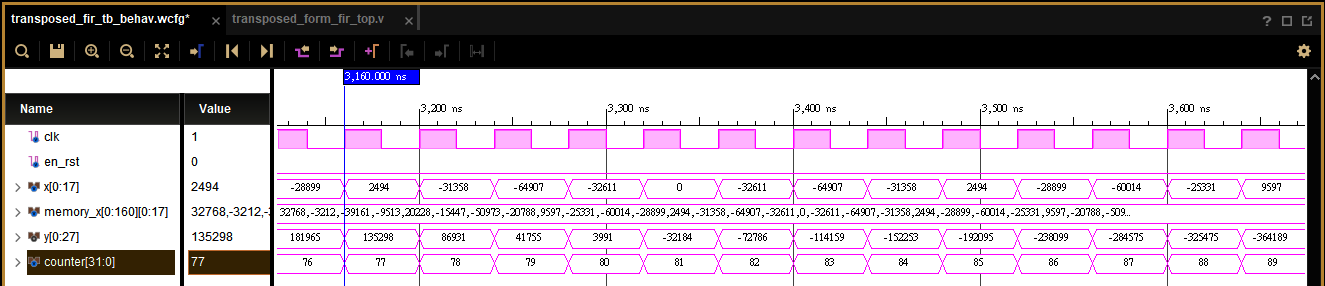
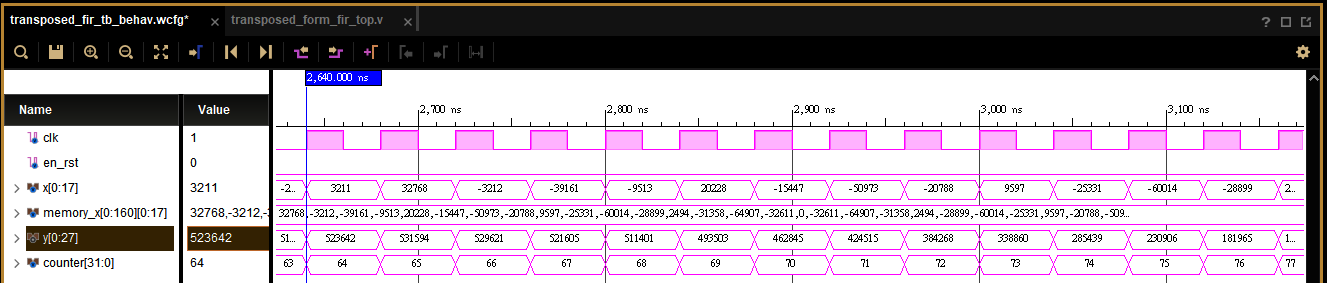
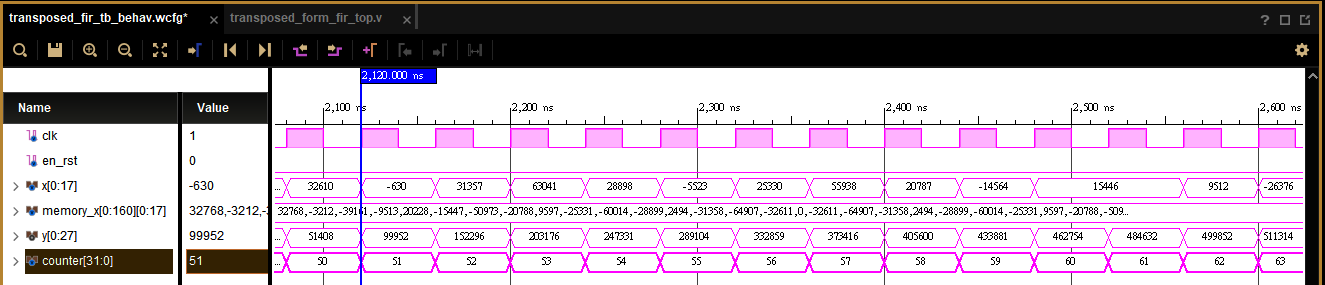
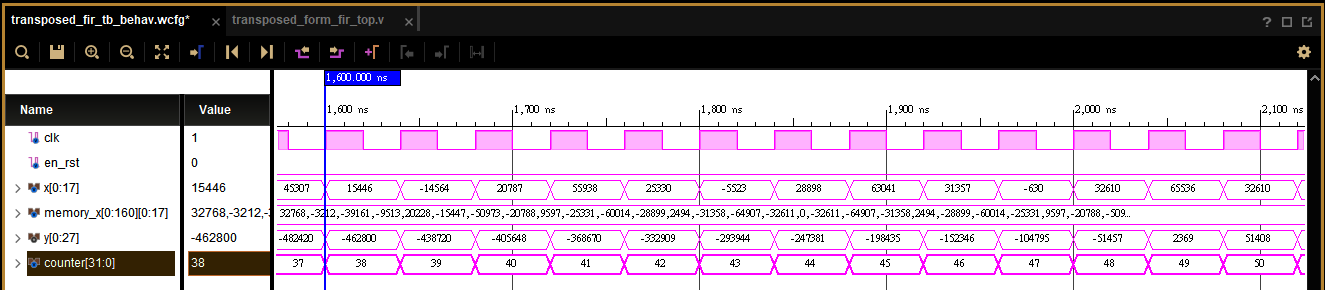
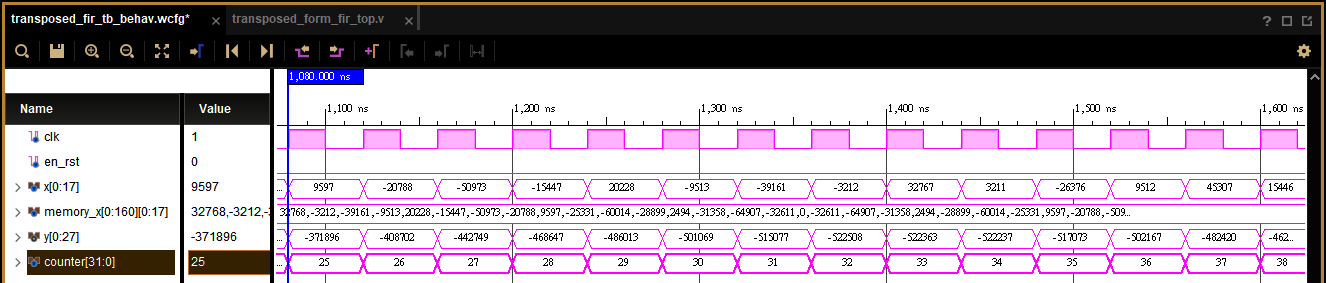
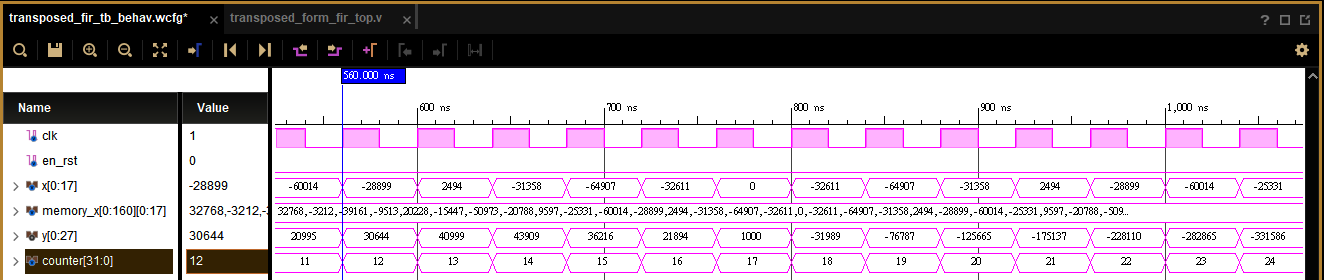
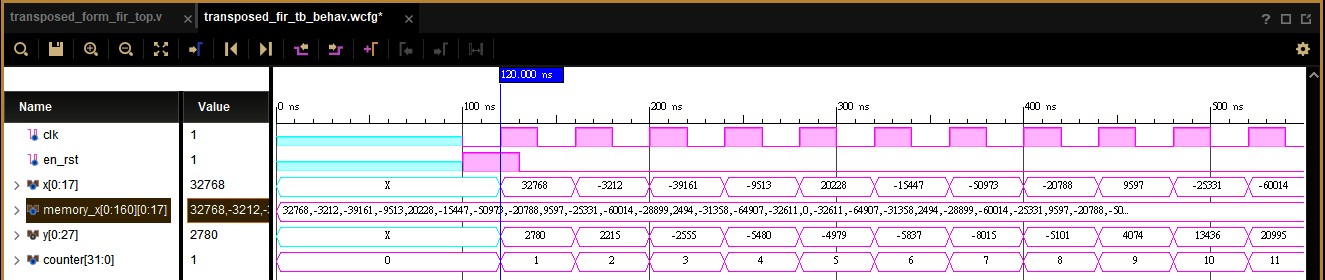


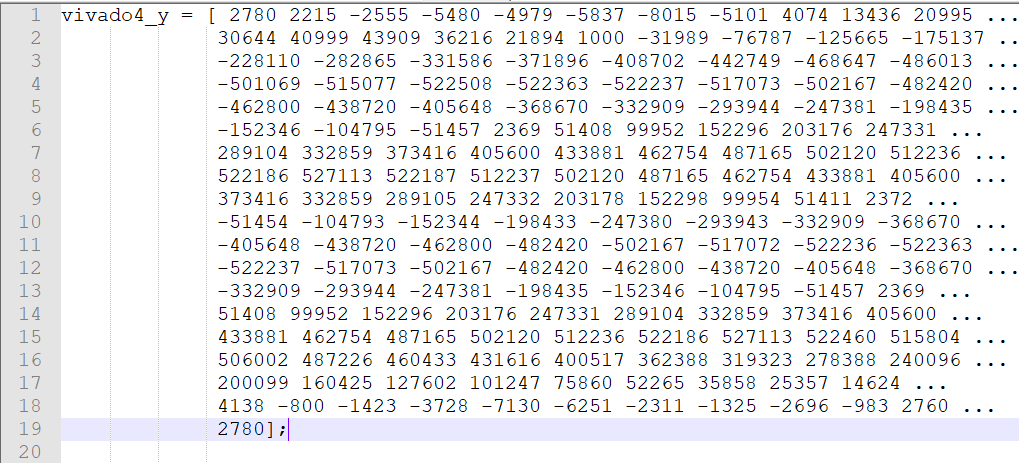
Show the errors of hardware outputs and Matlab floating-point results of direct from FIR by Matlab figures.



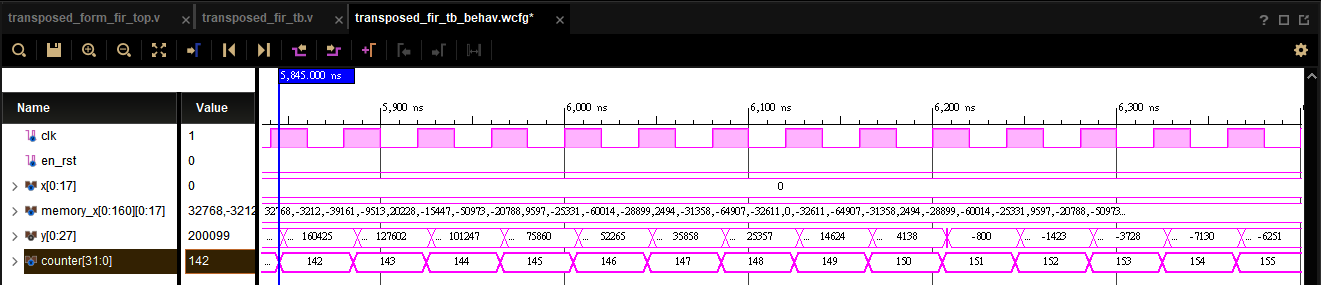
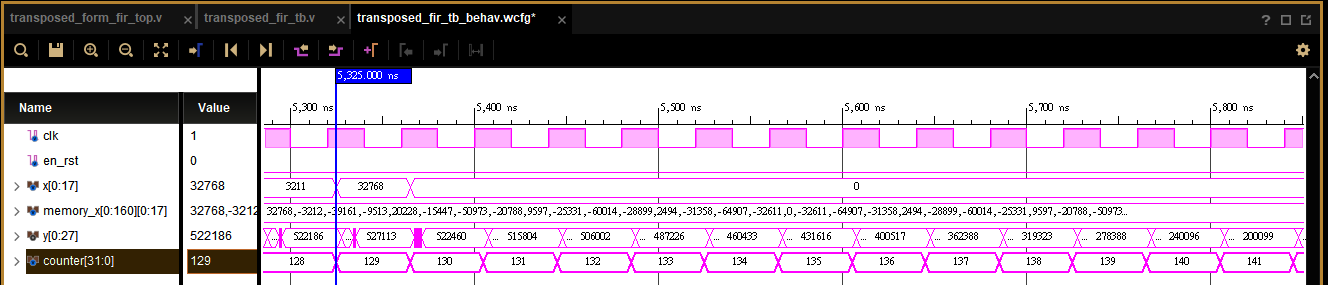
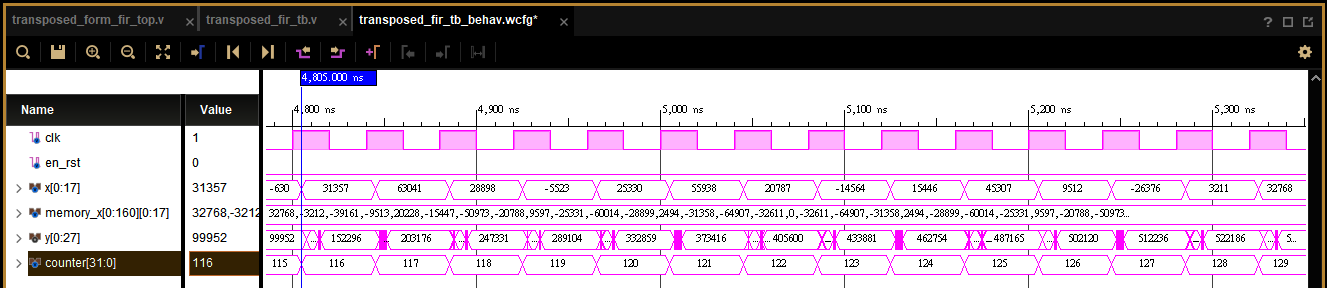
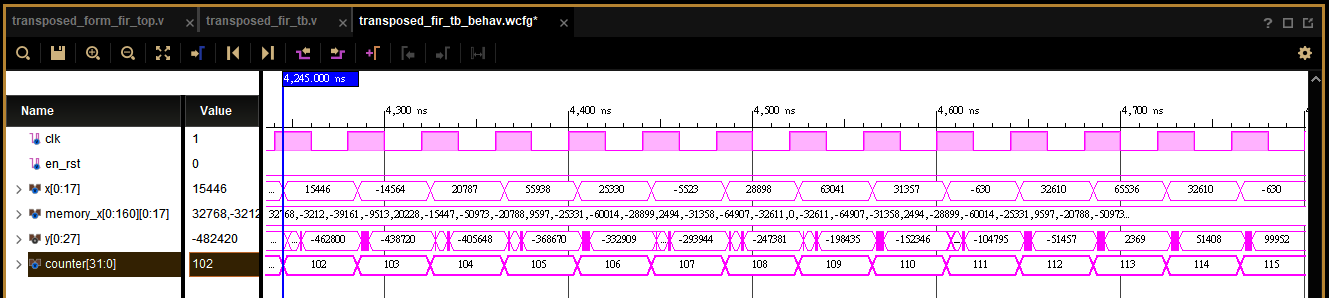
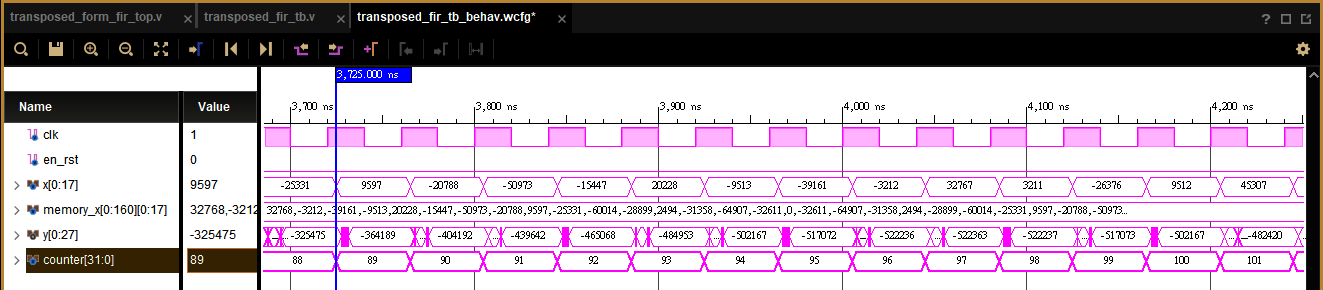
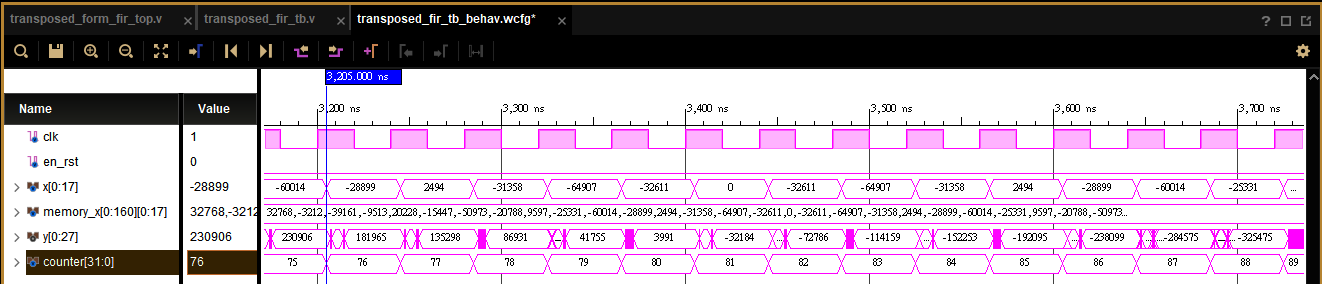
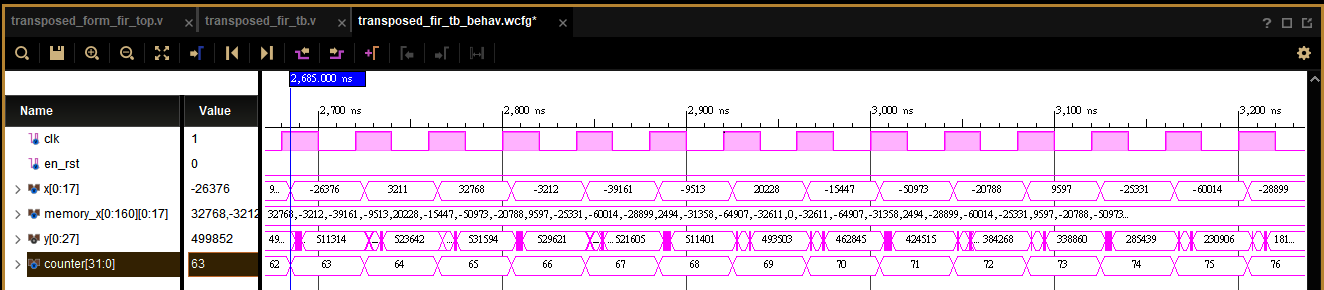
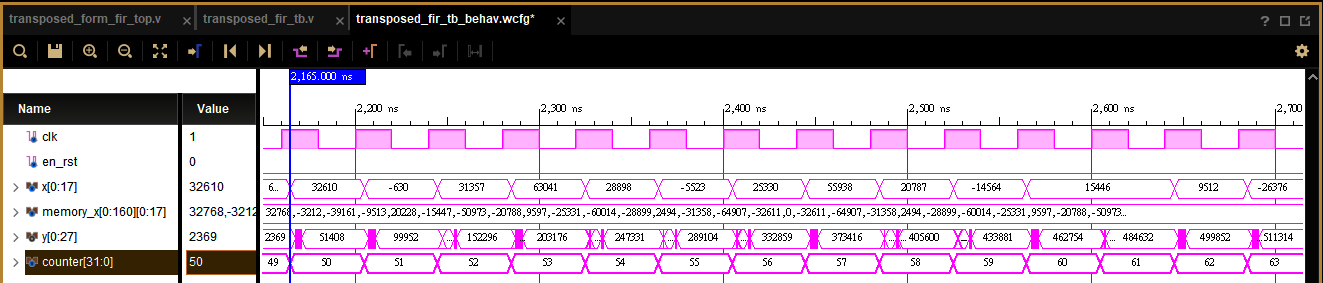
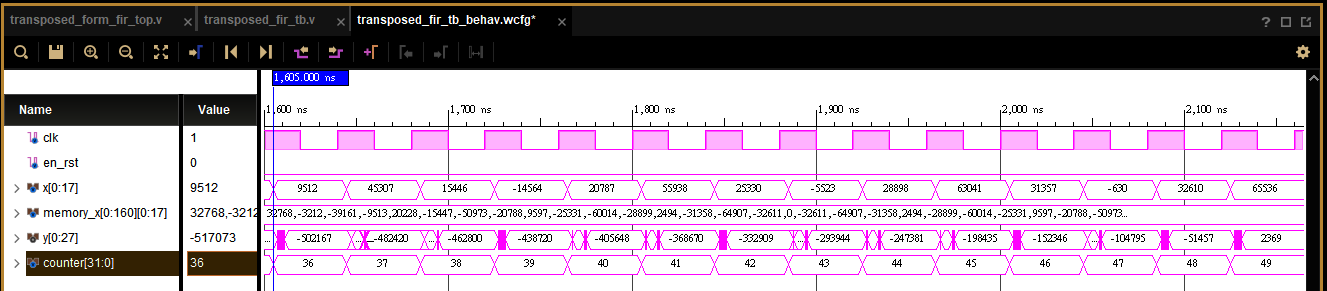
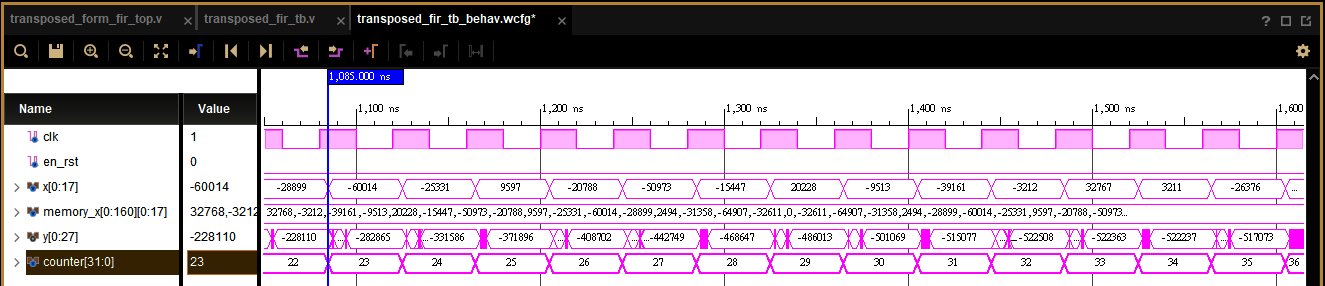
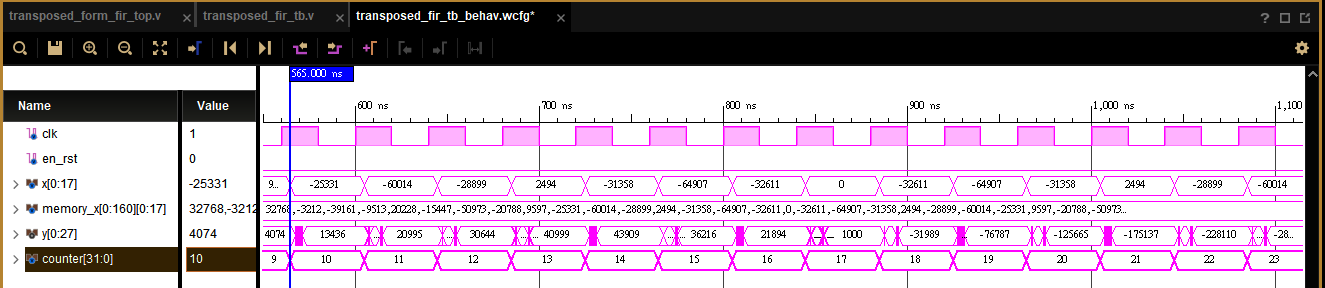
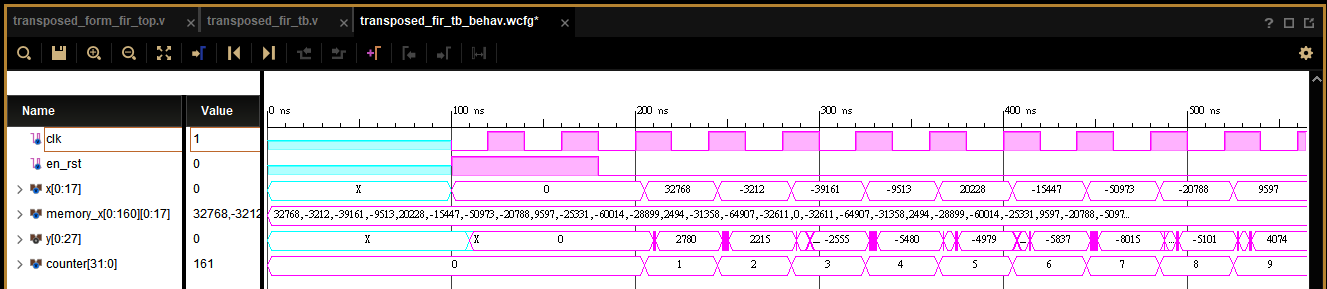
1. Please implement the transposed form. Note that modularity and parametric design can ease your loading. Use 𝑥[𝑛] as the input. Check the behavior and post-route simulation results. Compare the results with the Matlab floating-point results. (30%)

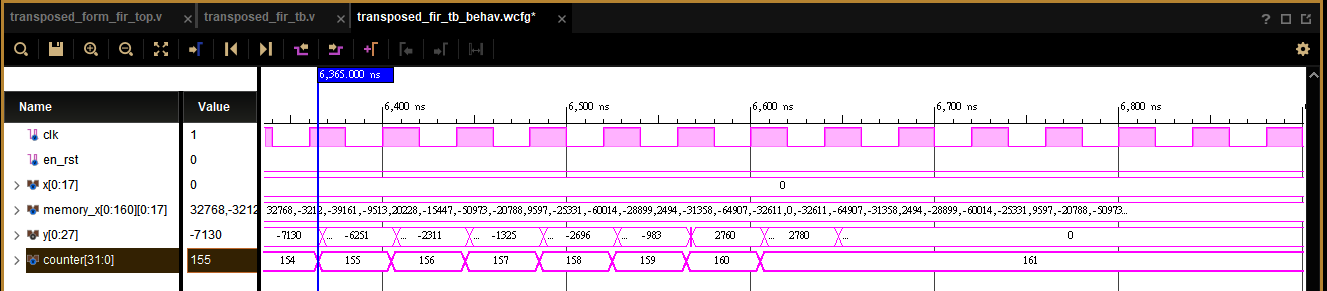
Behavior simulation:



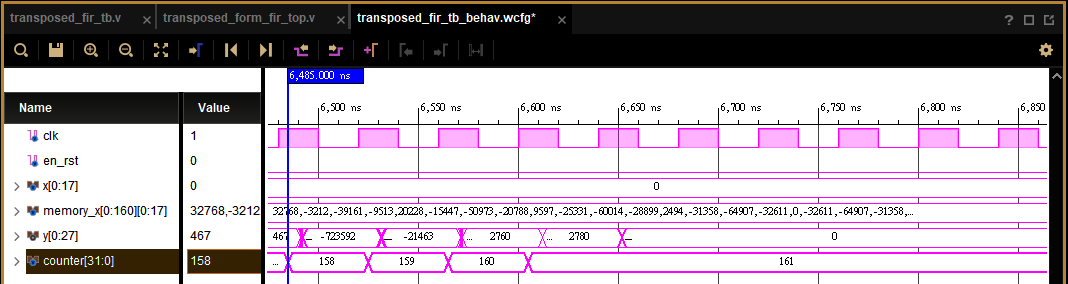


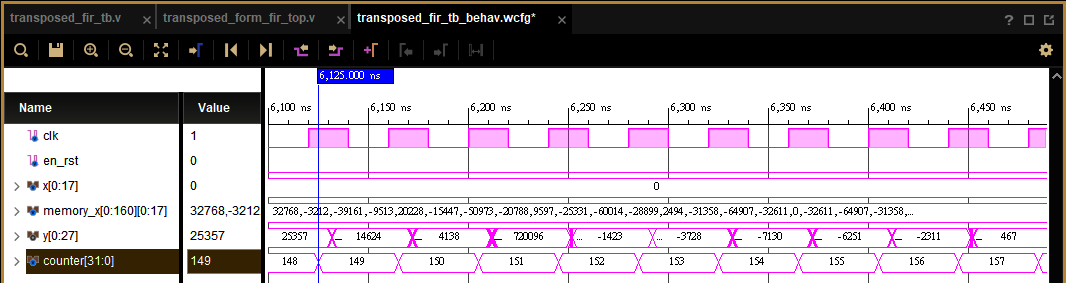
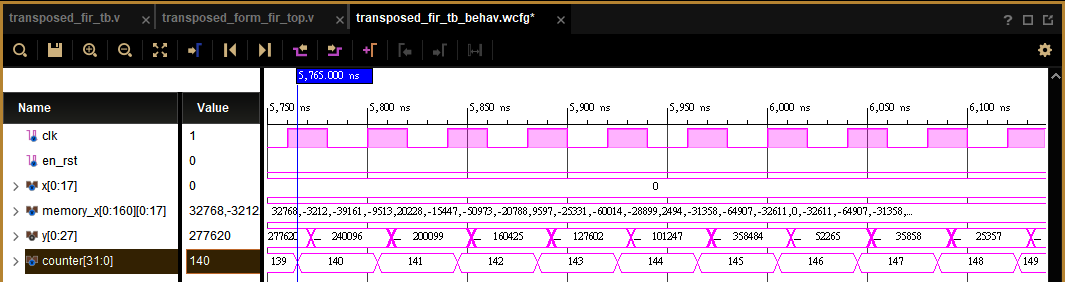
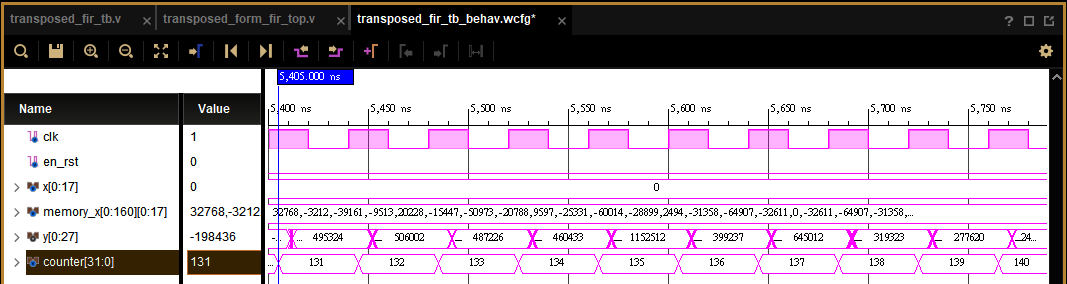
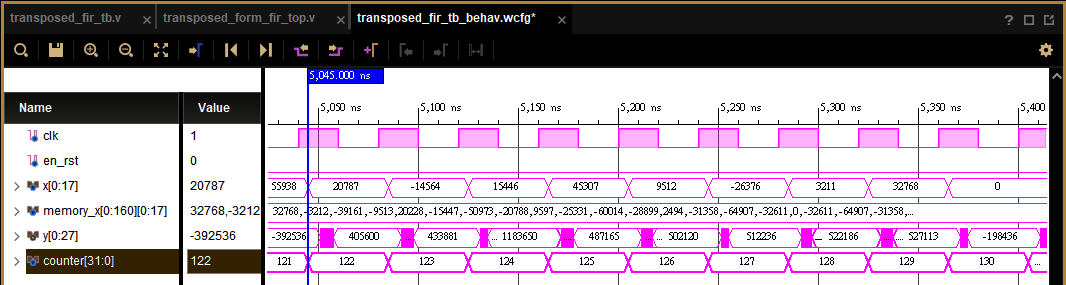
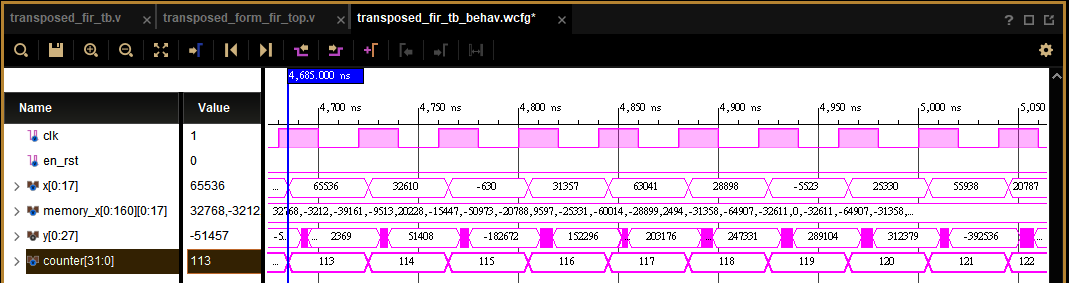
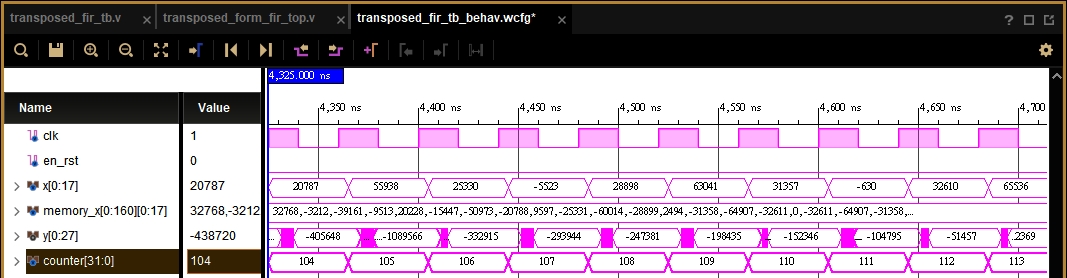
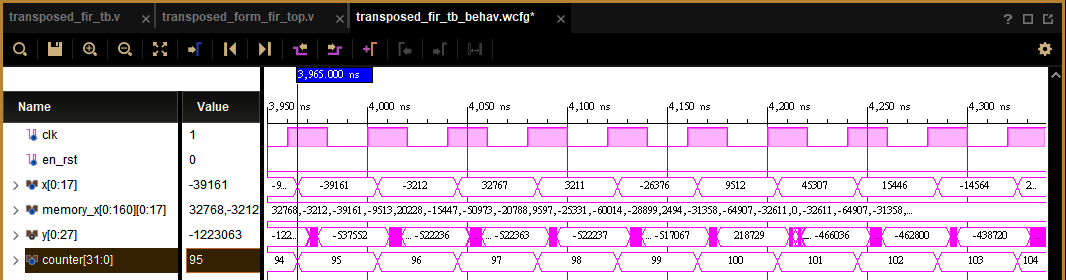
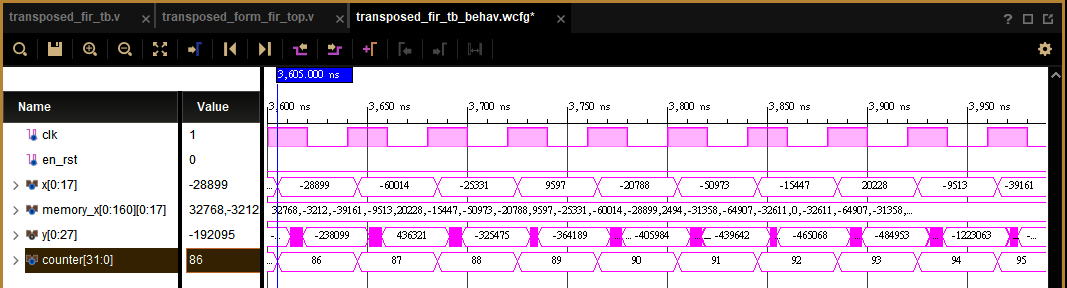
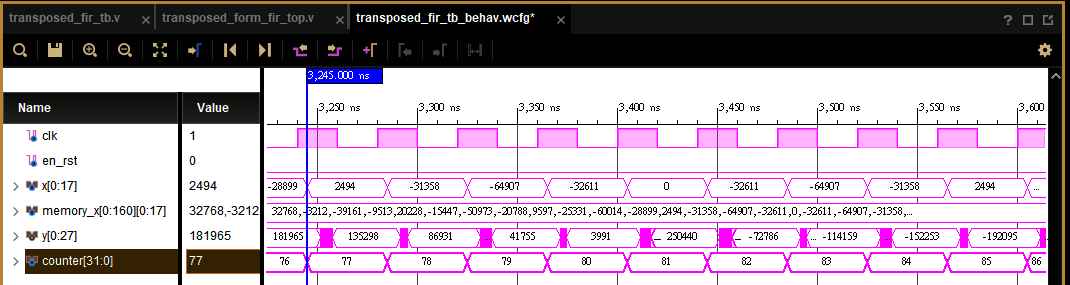
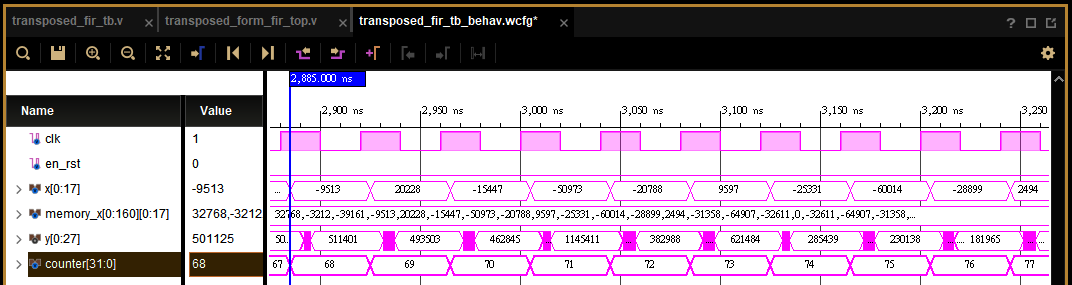
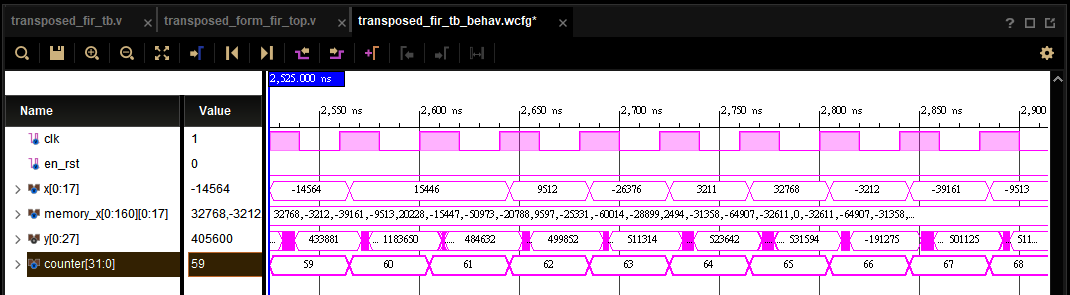
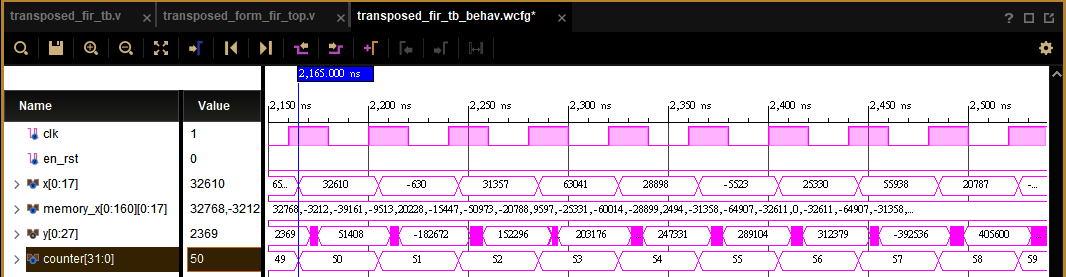
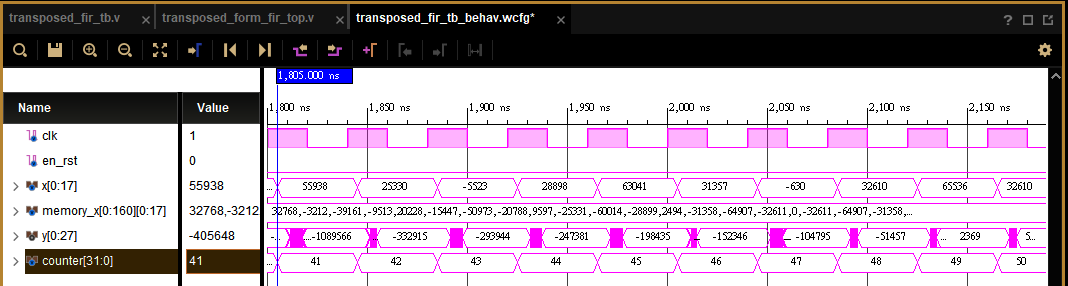
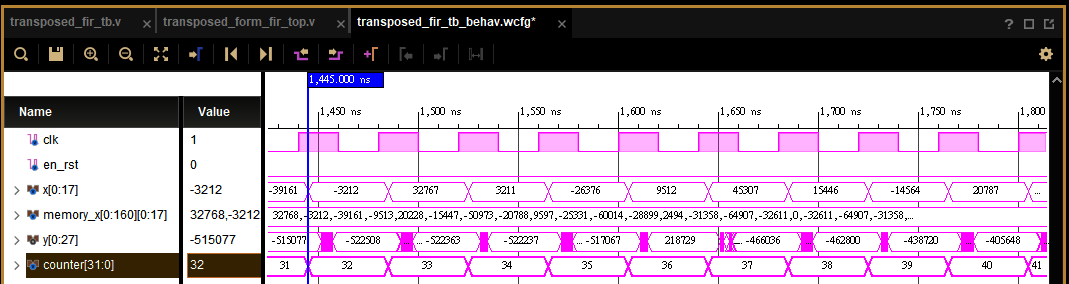
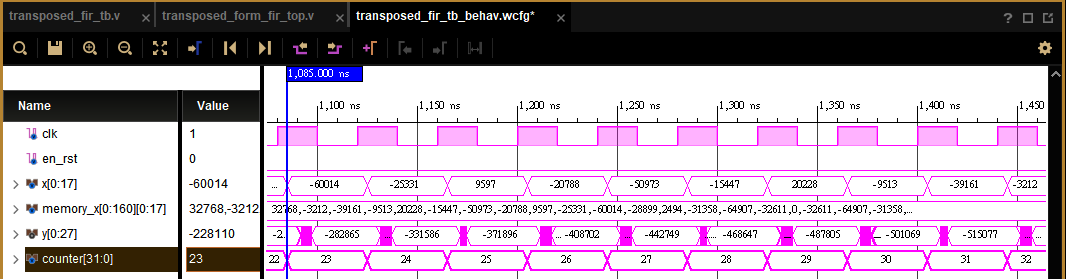
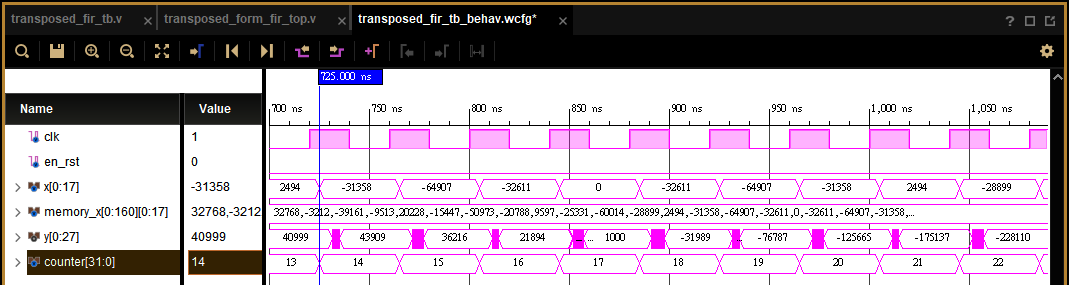
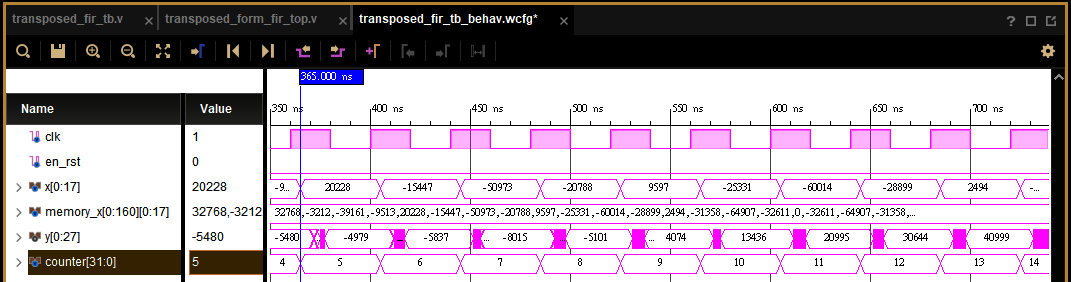
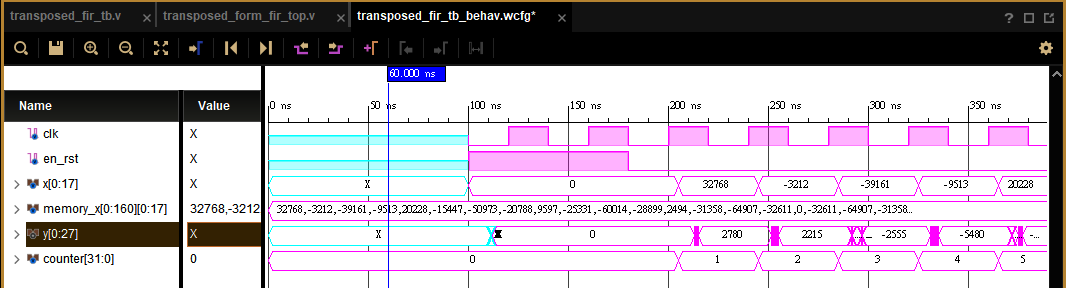
Post-synthesis timing simulation:



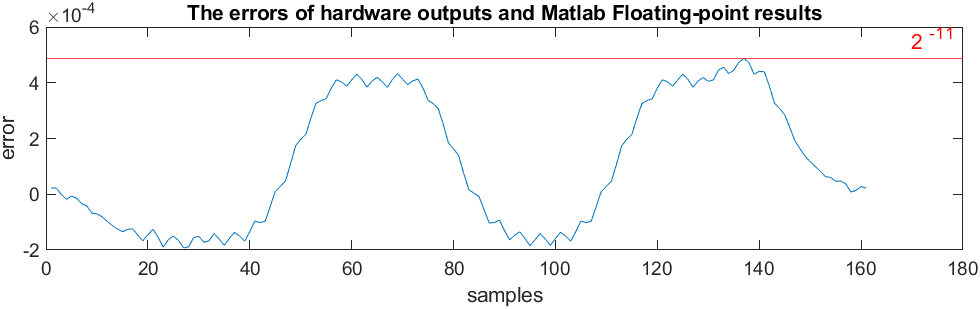


Post-implementation timing simulation:

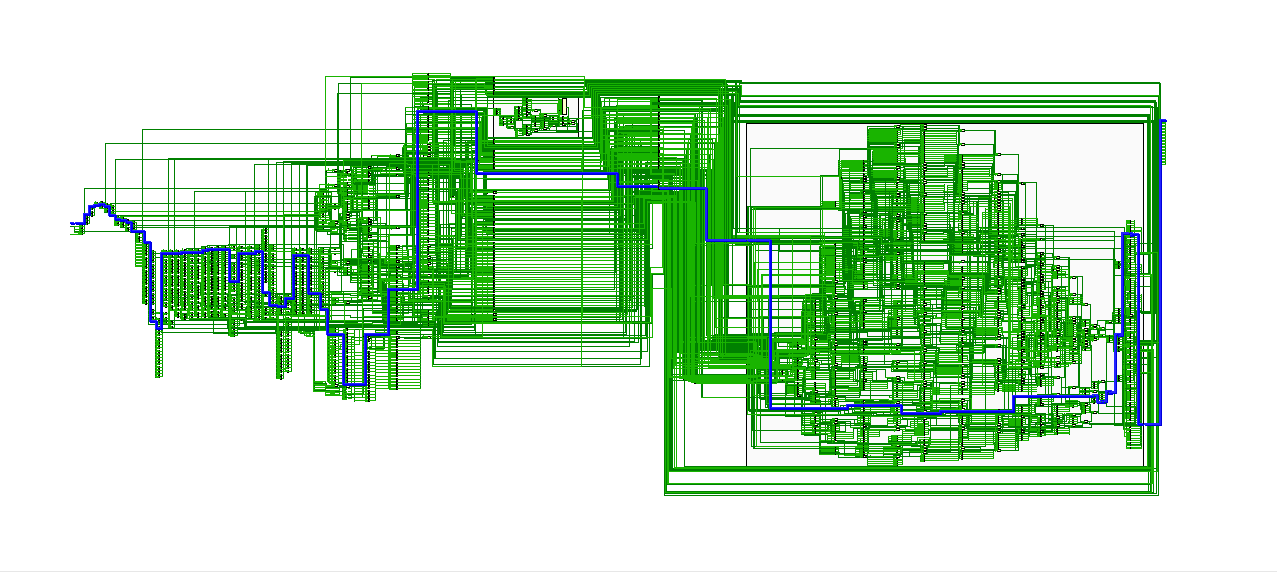


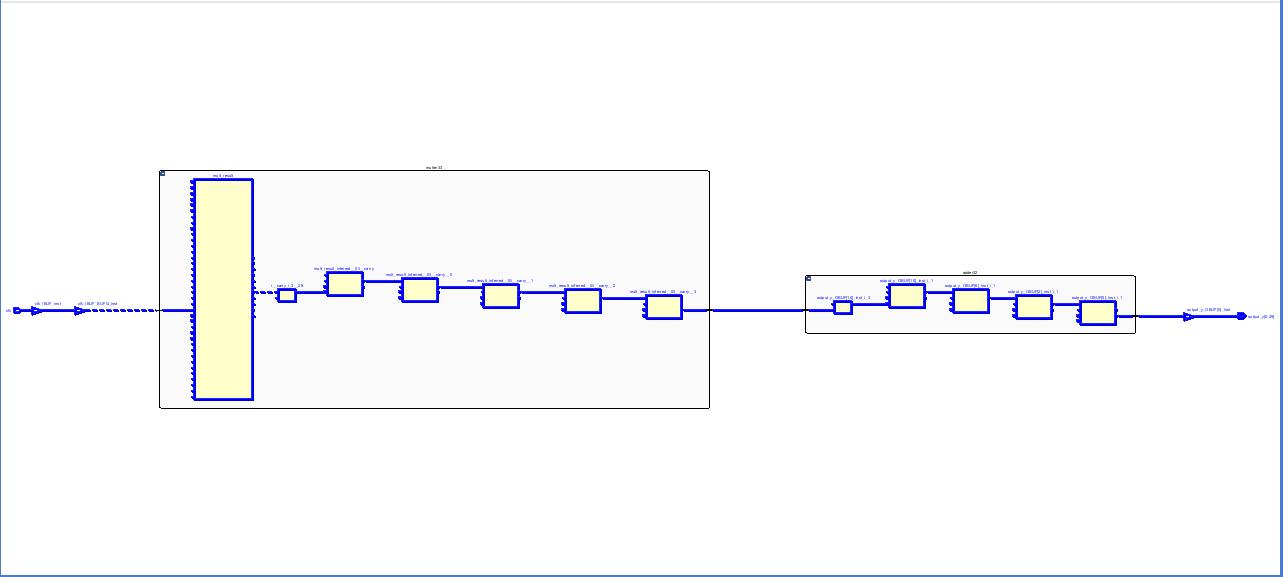


Show the errors of hardware outputs and Matlab floating-point results of transposed from FIR by Matlab figures.

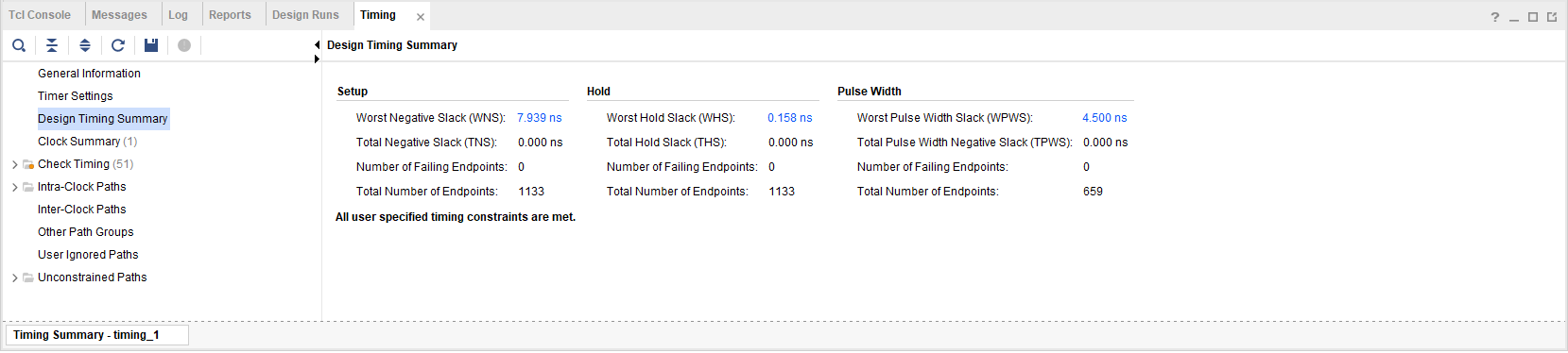


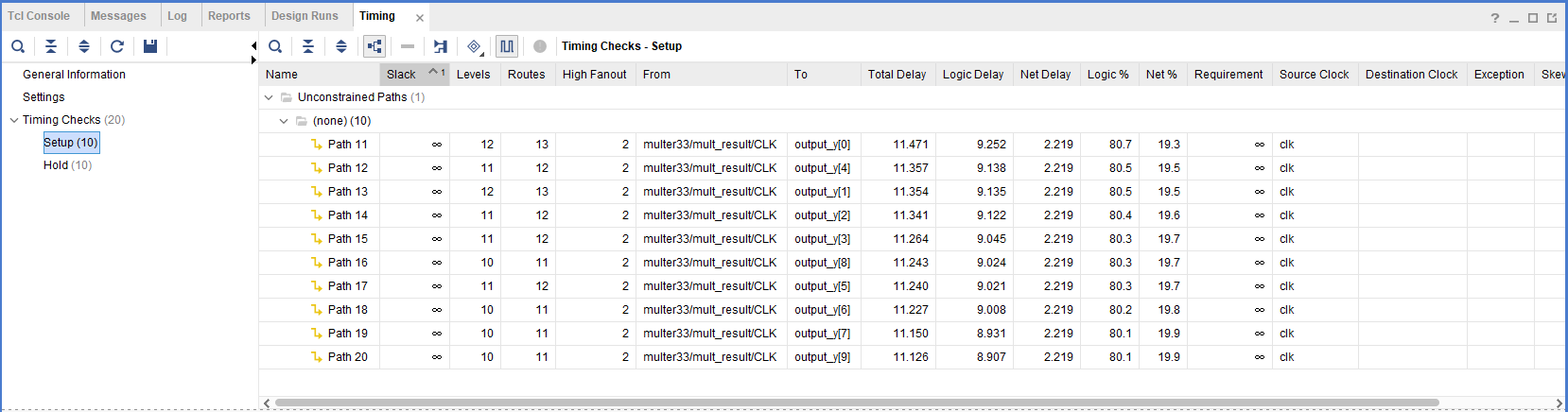
1. Find out the critical path of your design in Q5. Show the numbers of adders and multipliers in the critical path and list the timing information. (10%)

Setup time & critical path: 

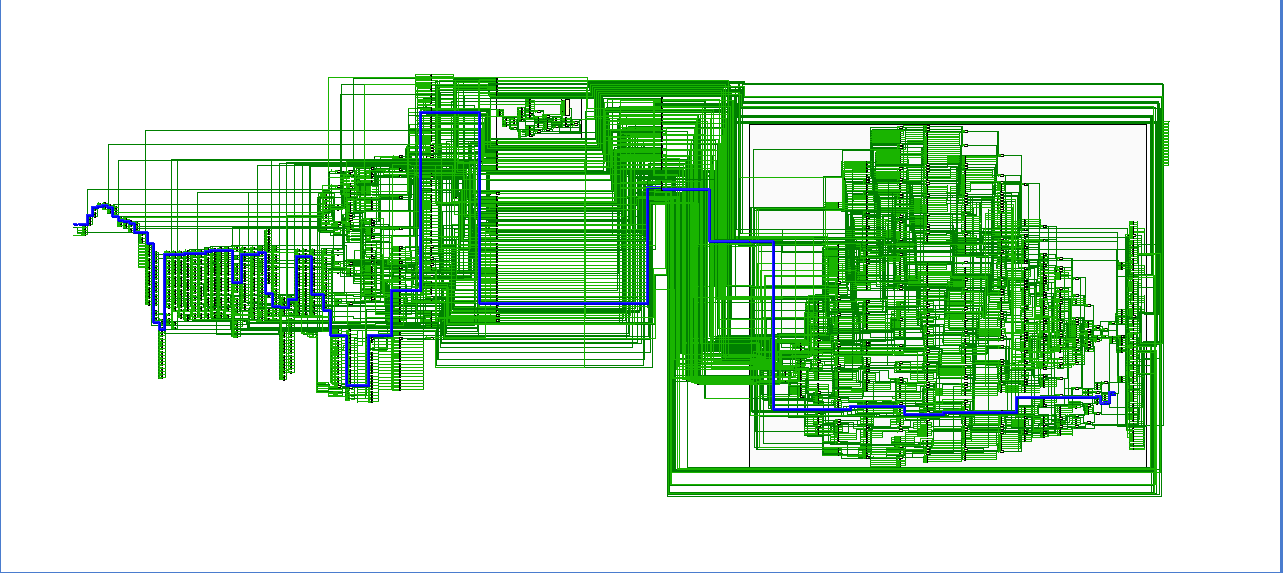


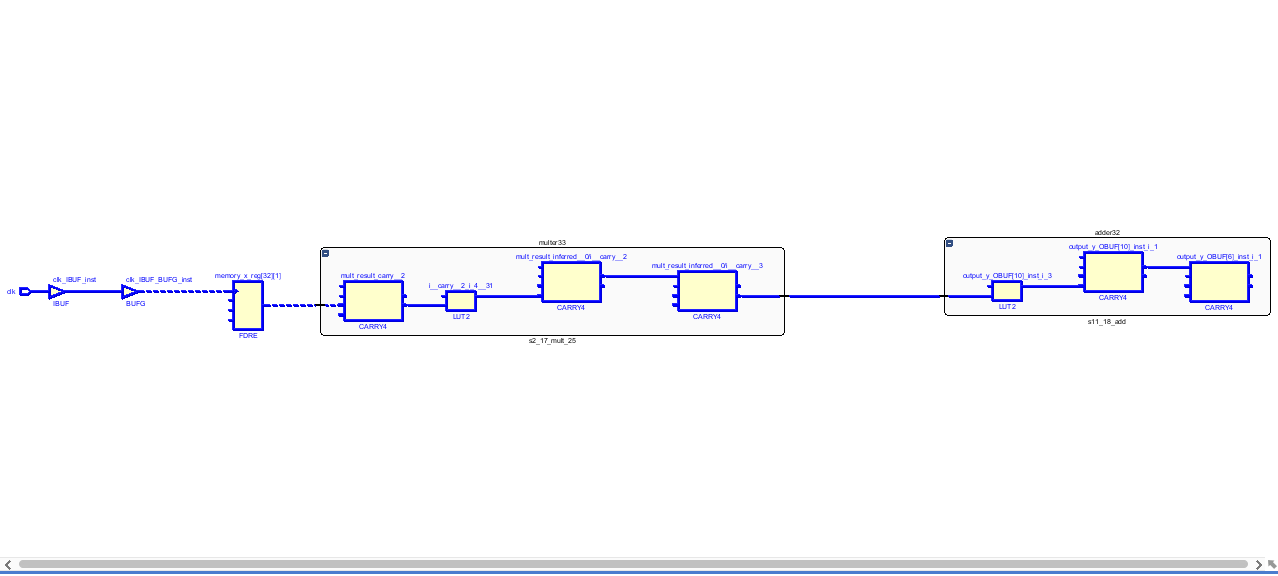
Print out the timing report.



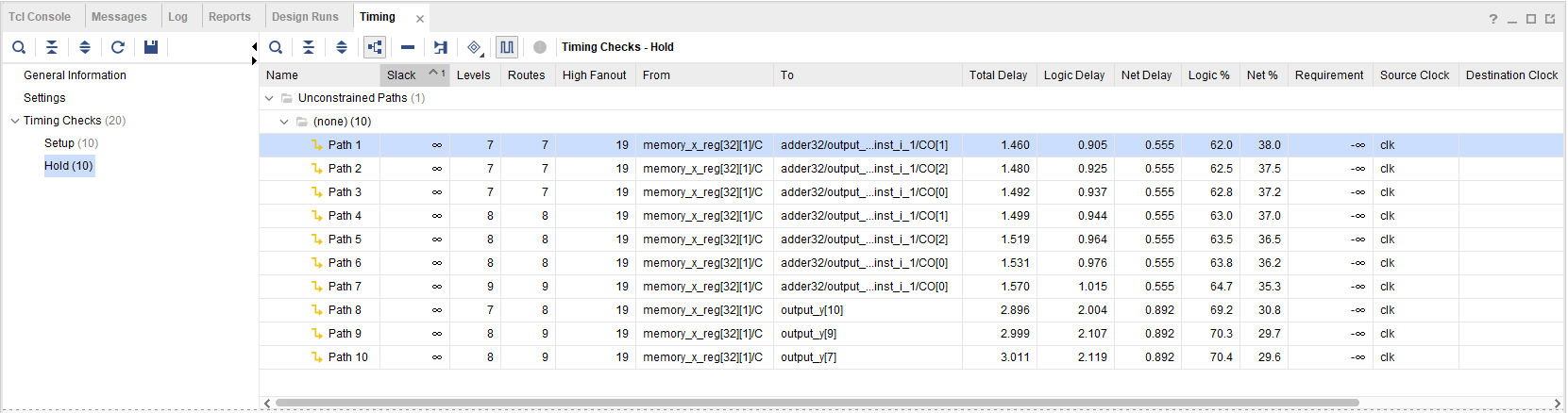
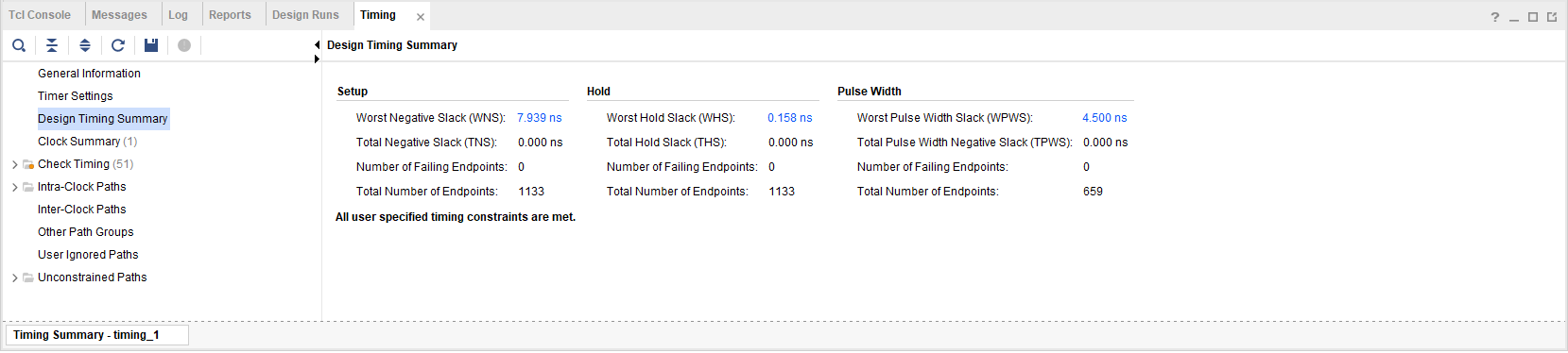


Hold time & critical path:





Print out the timing report.

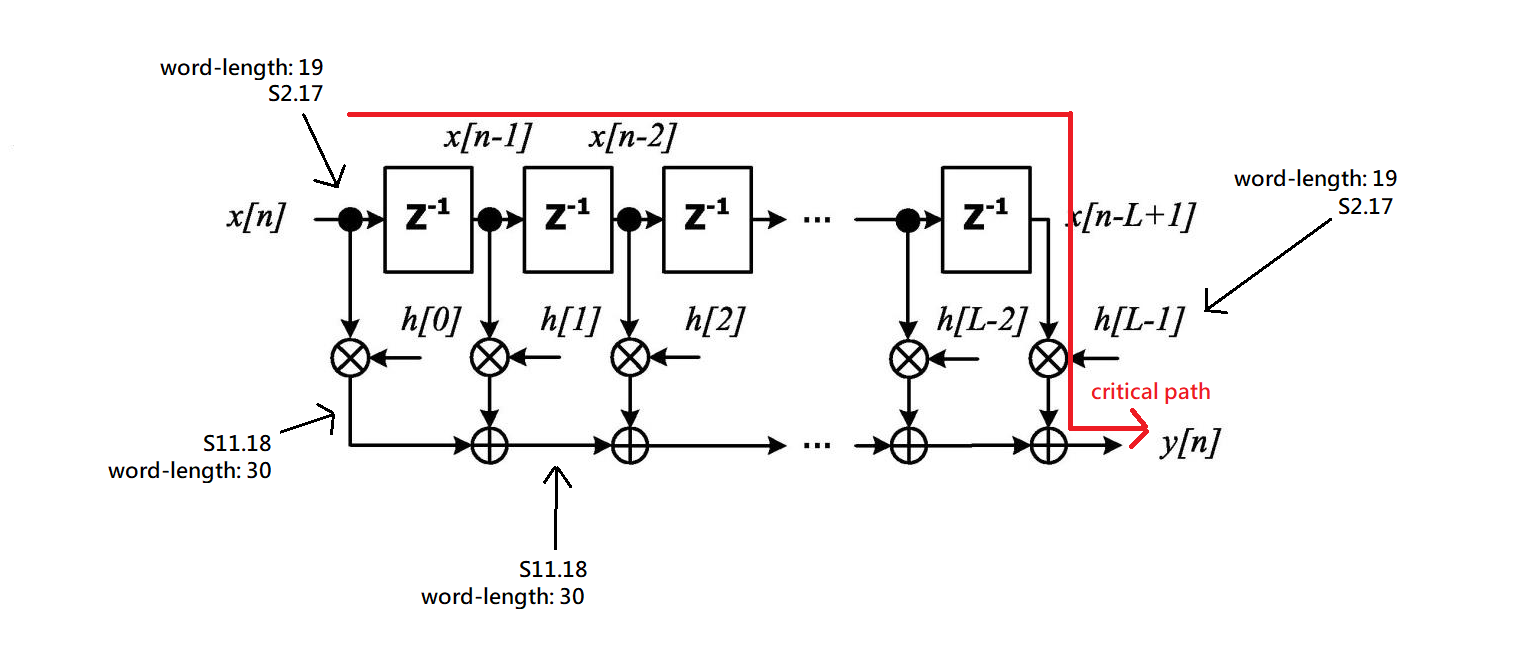


Show the numbers of adders and multipliers in the critical path

One adder + one multiplier in setup time critical path.

One adder + one multiplier in hold time critical path.

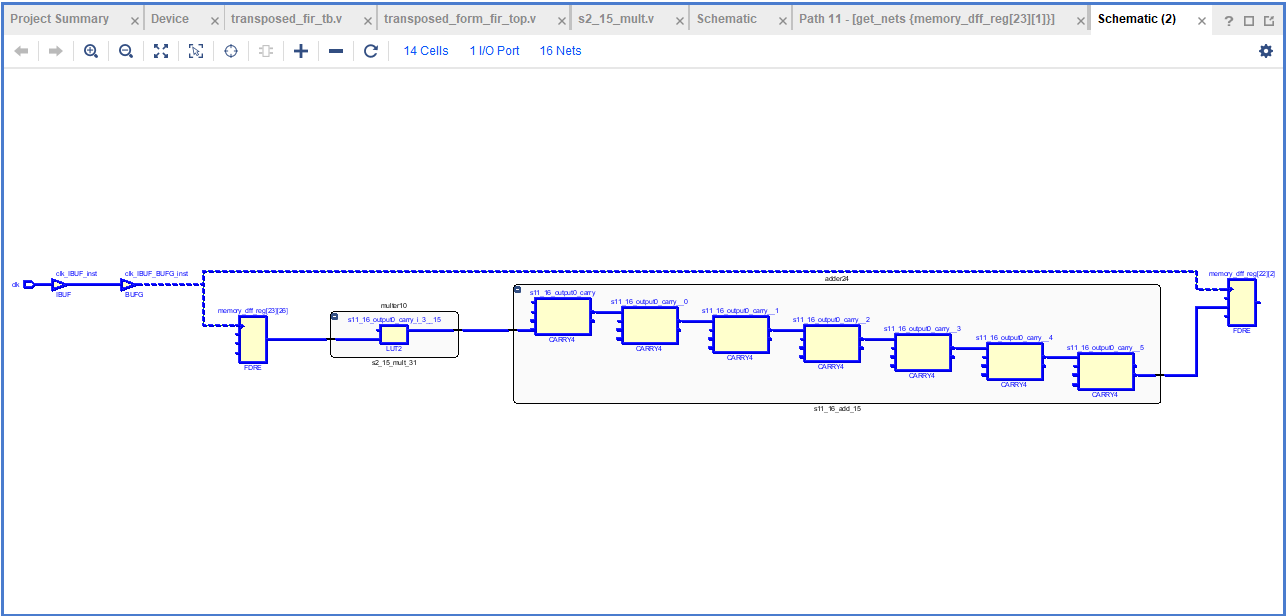
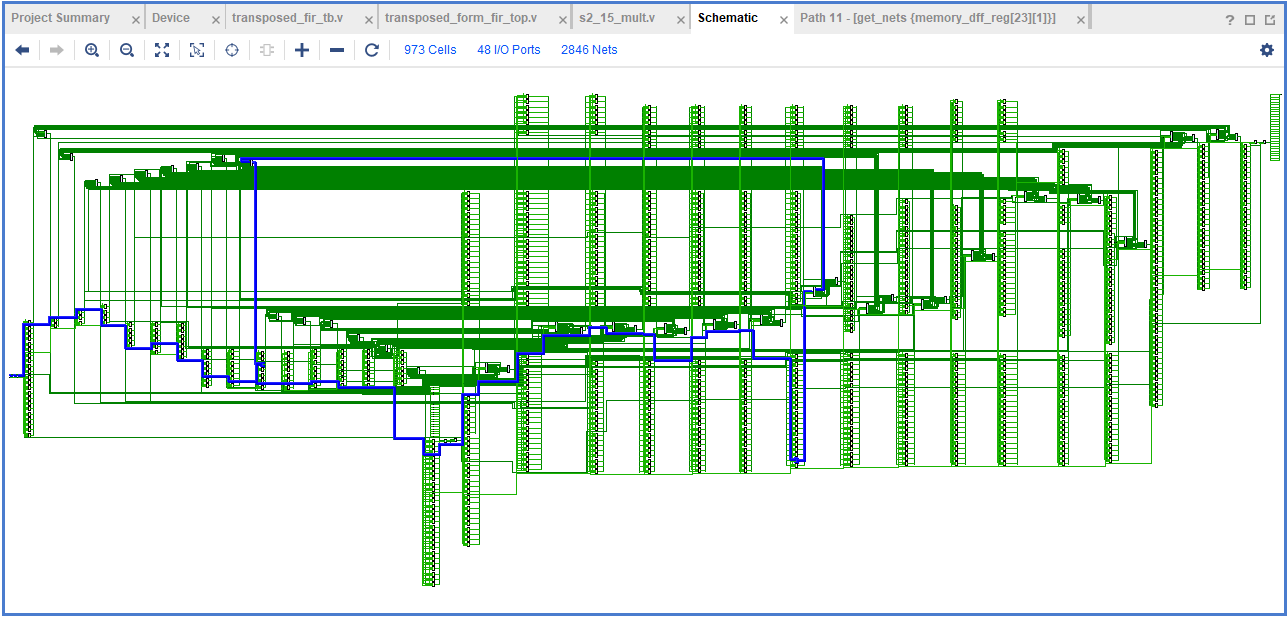
Mark the critical path of your direct-form FIR design in the block diagram. Also mark the input/output variable names and the word-lengths in the block diagram, which must be consistent with your Verilog codes.



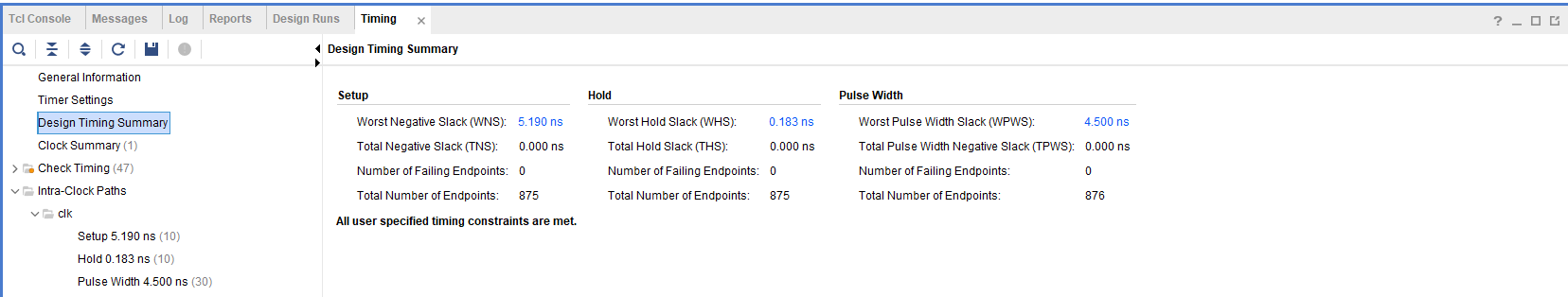


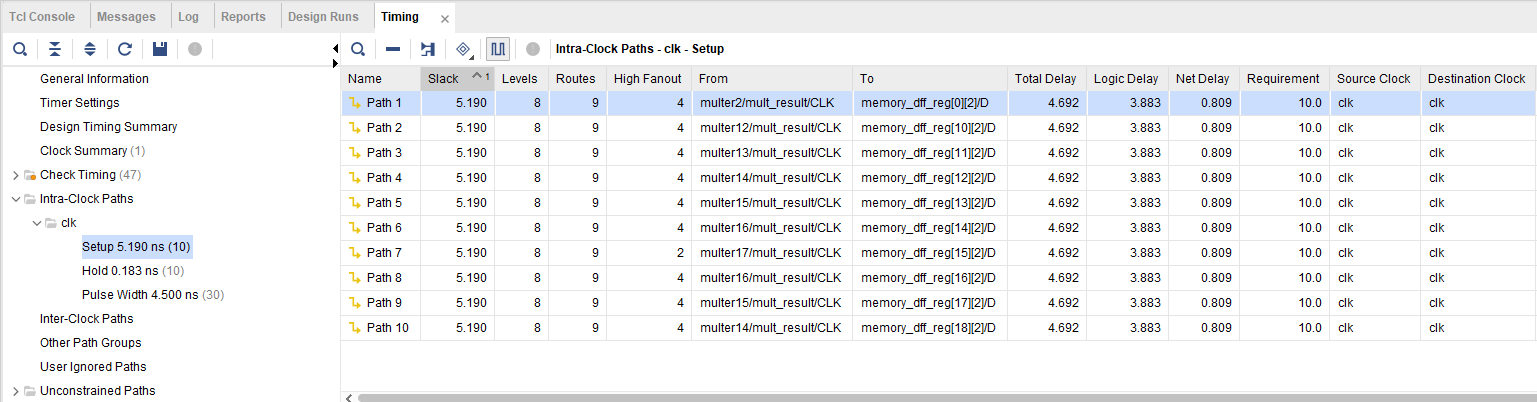
1. Find out the critical path of your design in Q6. Show the numbers of adders and multipliers in the critical path and list the timing information. (10%)

Setup time & critical path:

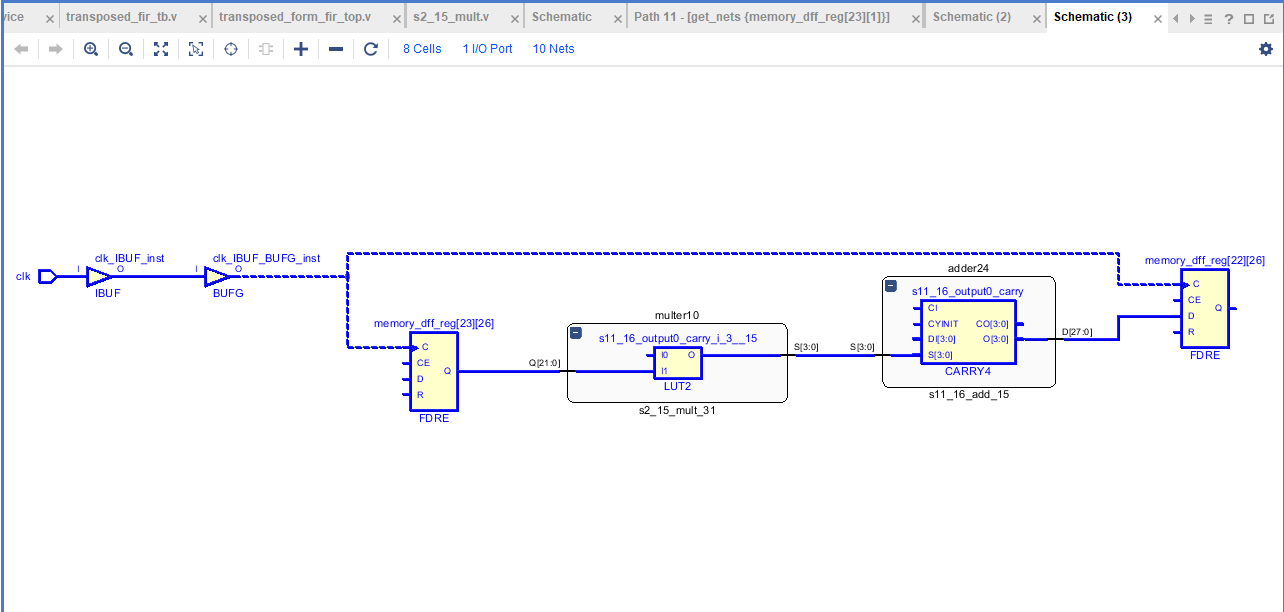
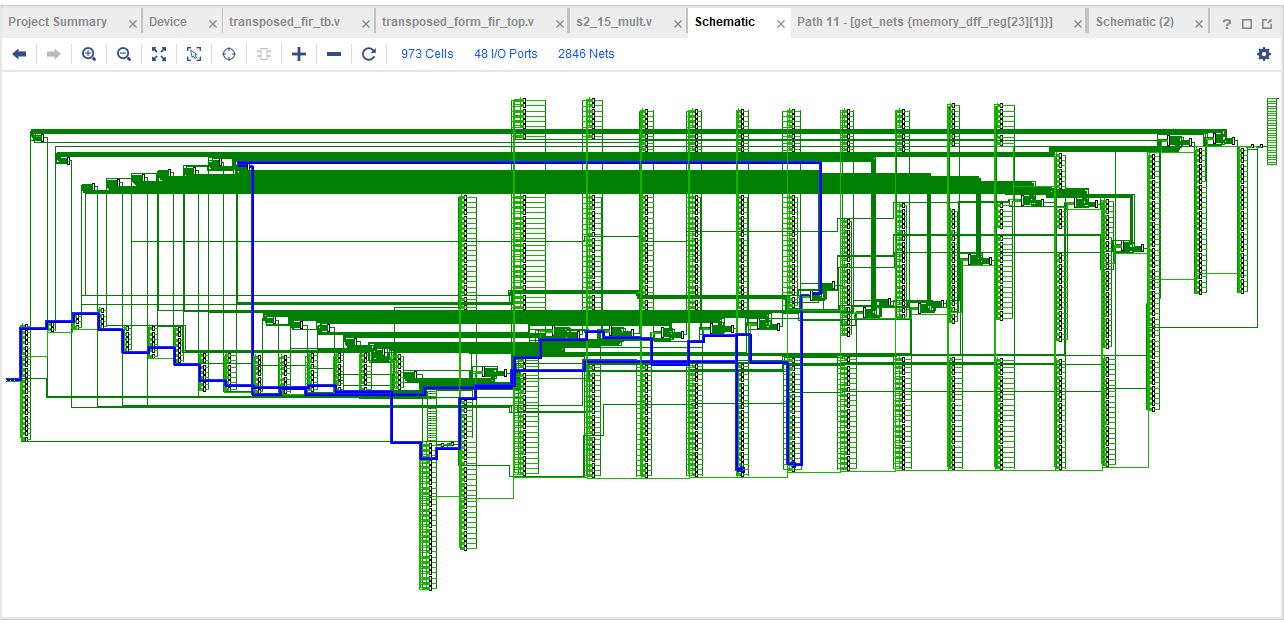


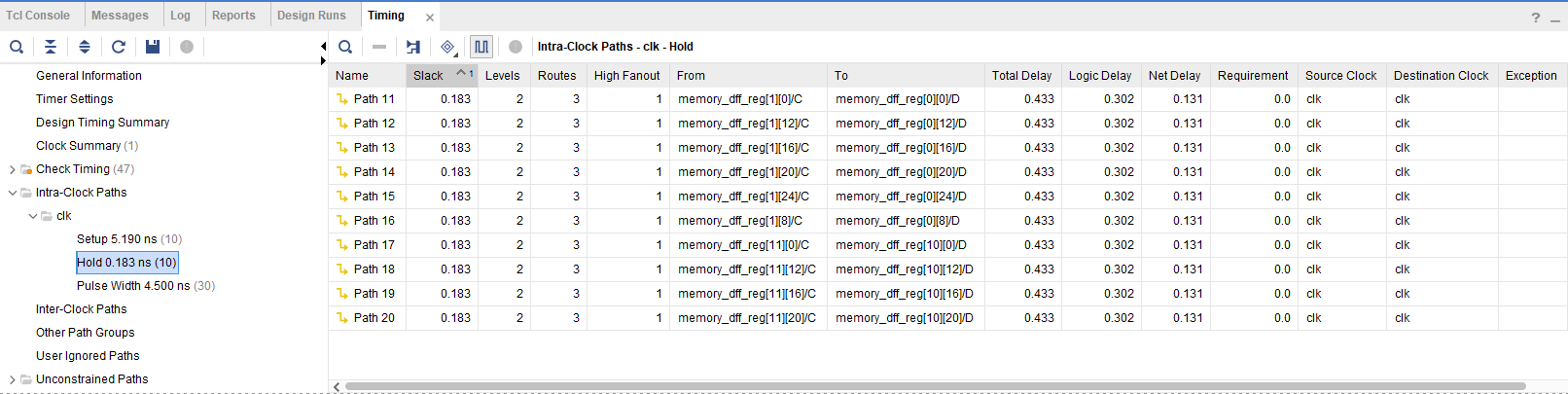
Print out the timing report.





Hold time & critical path:



Print out the timing report. 

Show the numbers of adders and multipliers in the critical path

One adder + one multiplier in setup time critical path.

One adder + one multiplier in hold time critical path.

Mark the critical path of your transposed form FIR in the block diagram. Also mark the input/output variable names and the word-lengths in the block diagram, which must be consistent with your Verilog codes.

