國 立 中 央 大 學

電 機 工 程 學 系

超大型積體電路設計

期中報告

指導老師:鄭國興

學生:林豪澤

系級:電機碩一

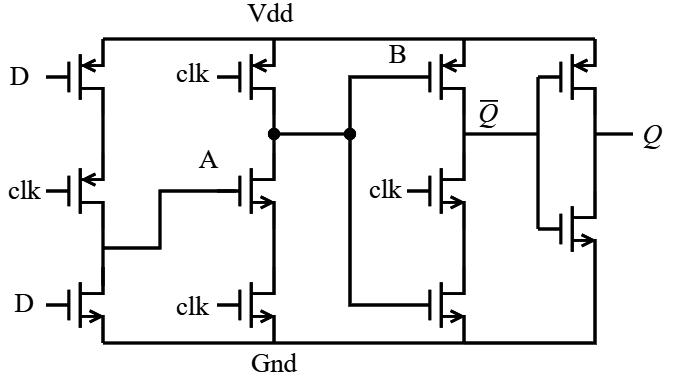
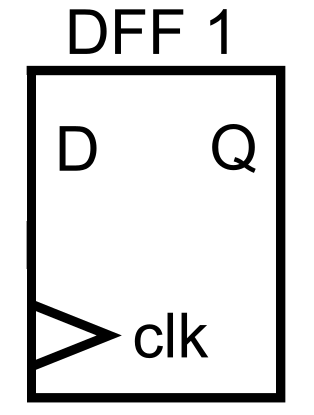
學號:111521035

中華民國一百一十一年十一月

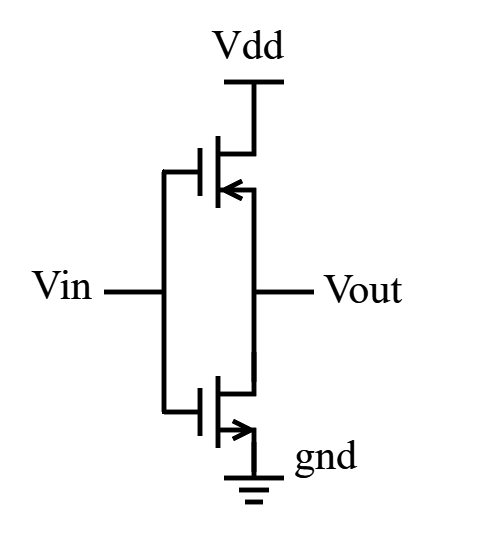
1. **電路架構**

電路圖(Gate-level or Transistor-level)與架構圖(Block diagram)

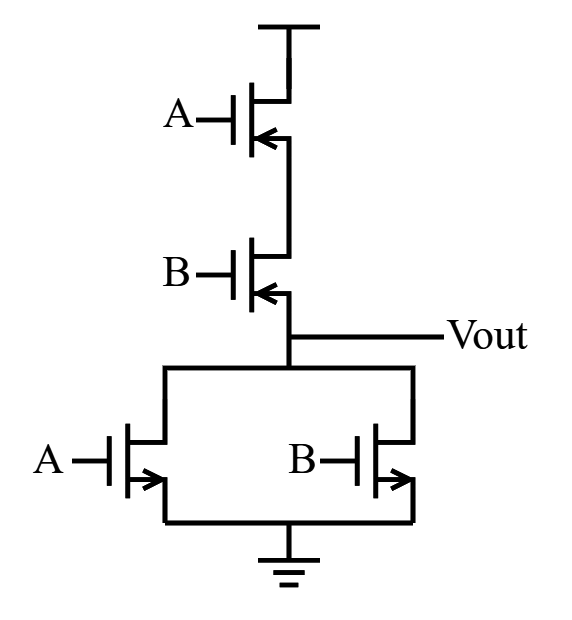
1. TSPC D Flip-Flop



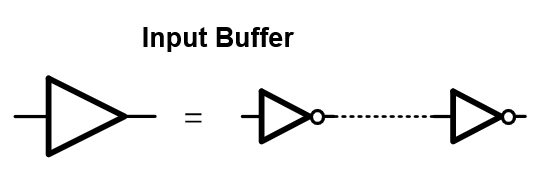
1. Inverter

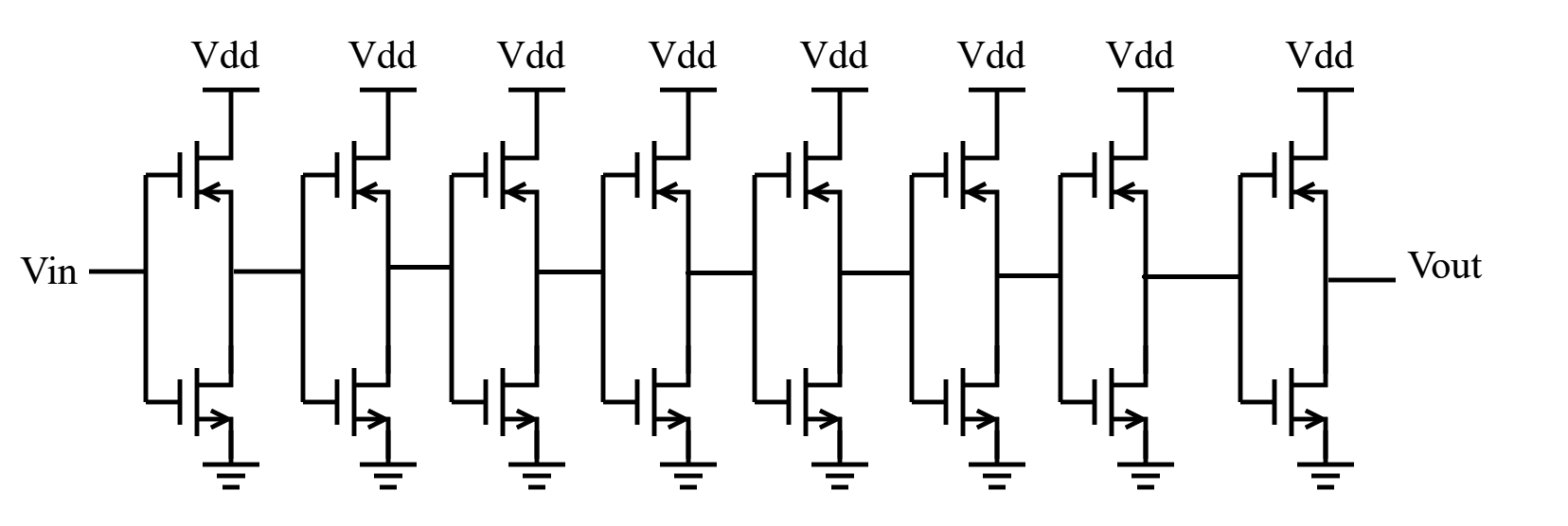


1. NOR

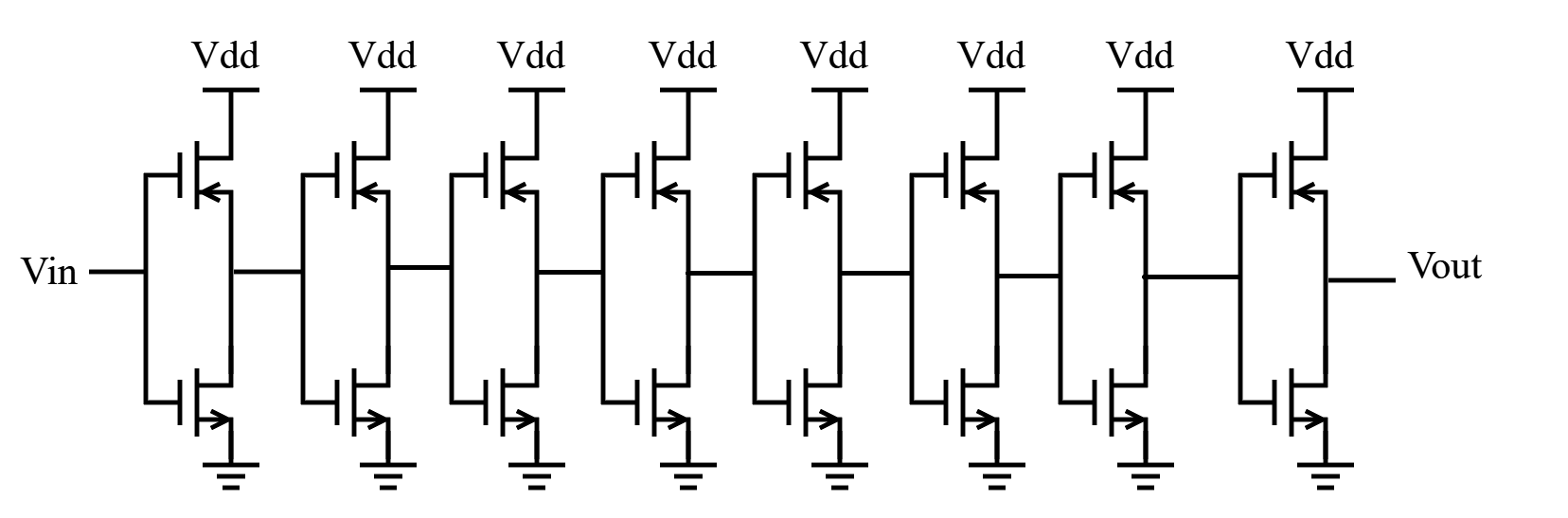


1. Input-buffer



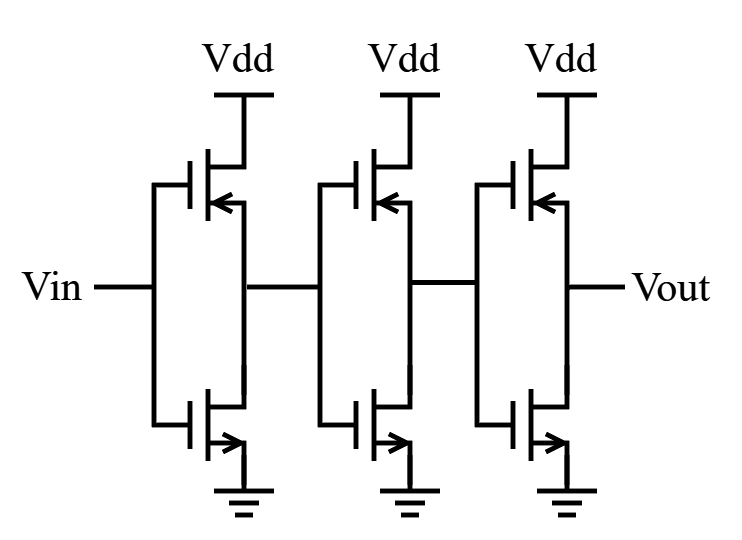


1. Tapper-buffer

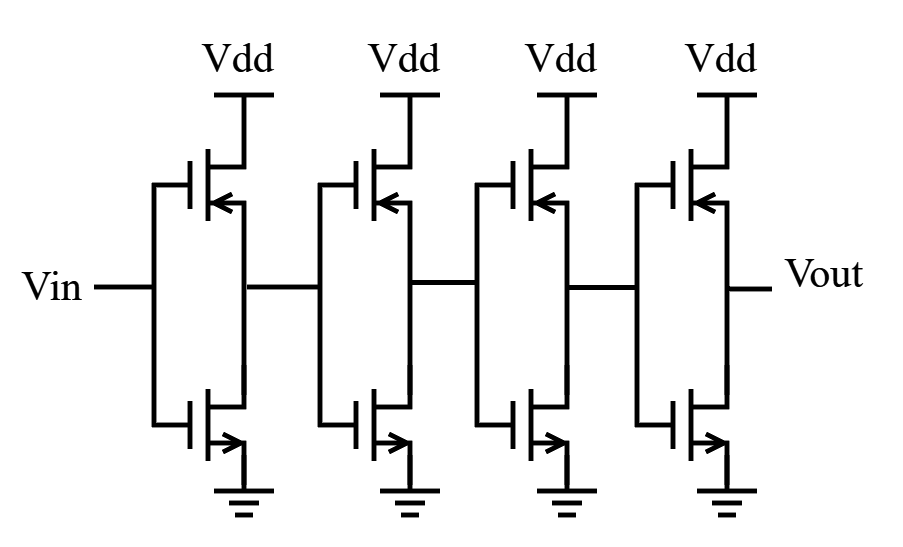


每次經過的inverter之 : 以自然對數e的比例成長，以瘩到最佳的推動後級的功能。

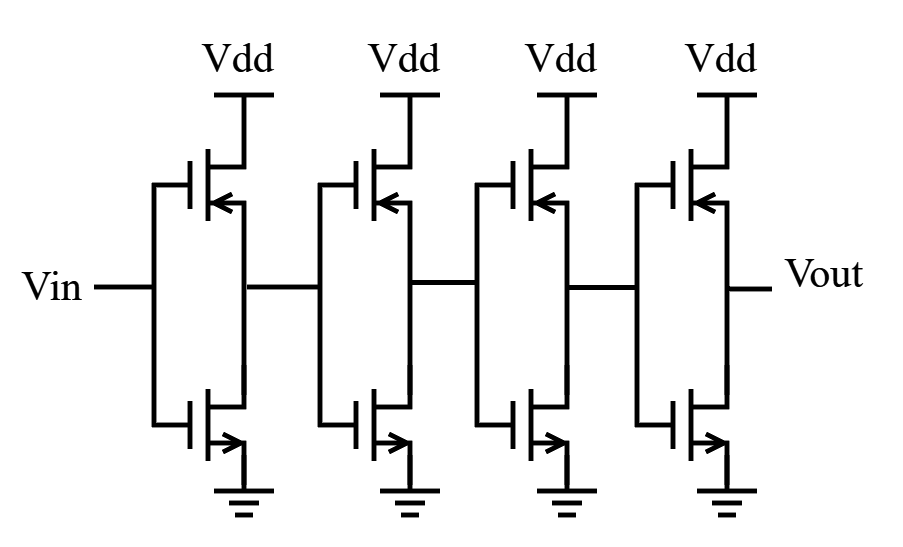
(5-1) tapper-buffer( clock div by 3)



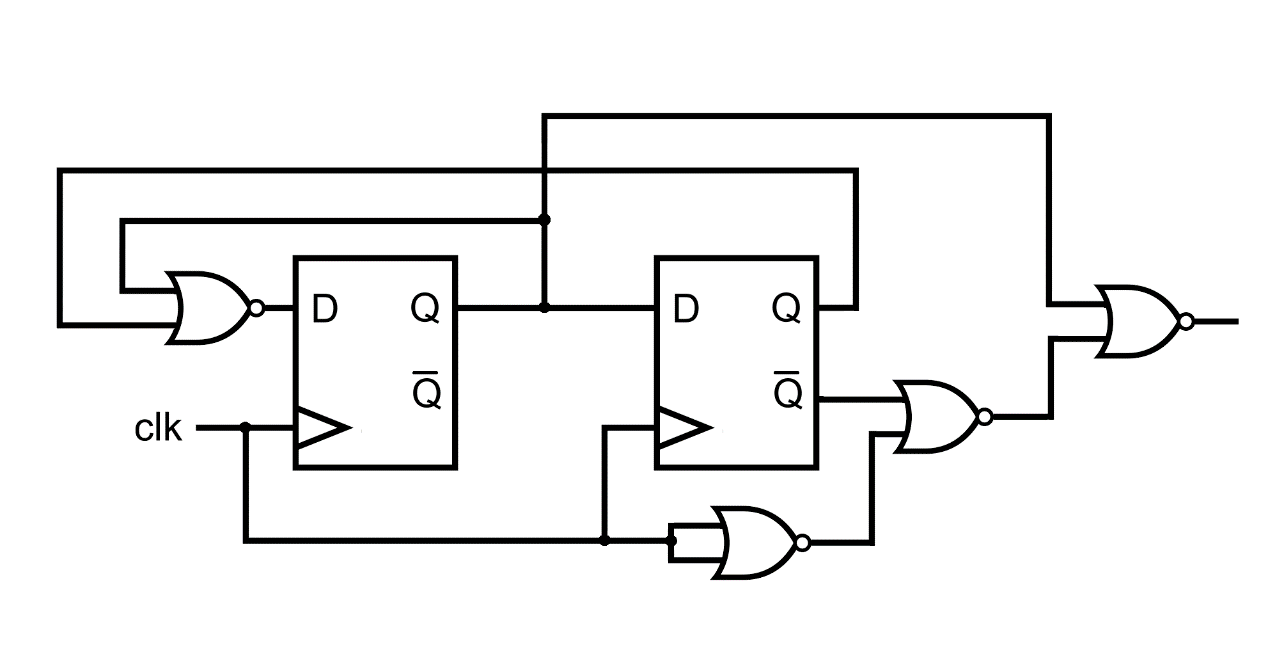
(5-2) tapper-buffer( clock div by 6)



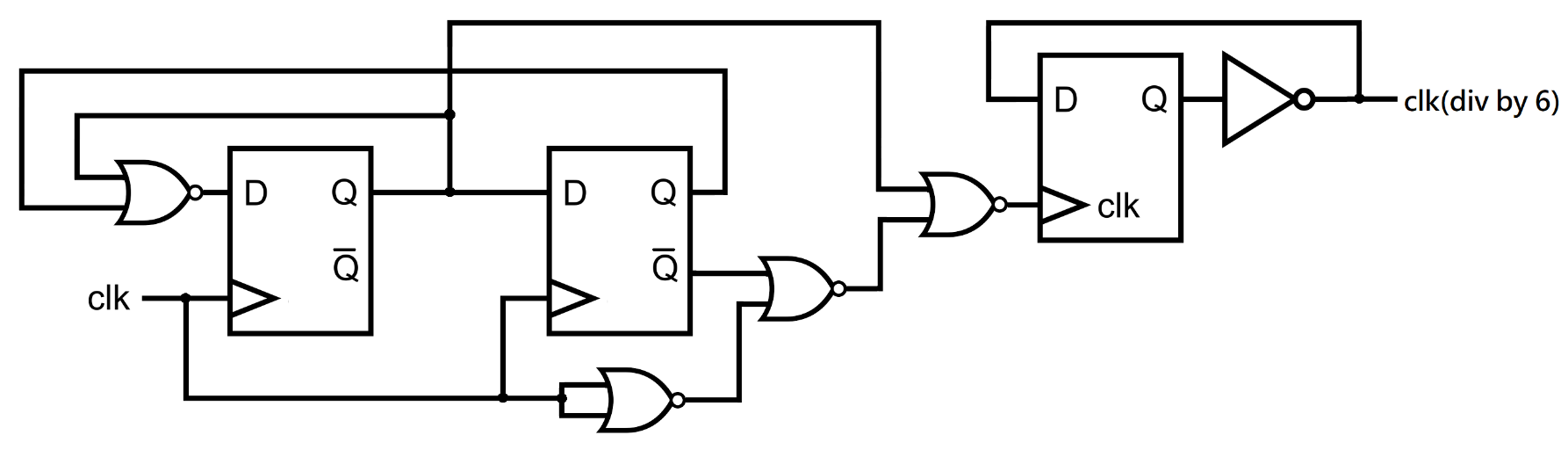
(5-3) tapper-buffer( clock div by 8)



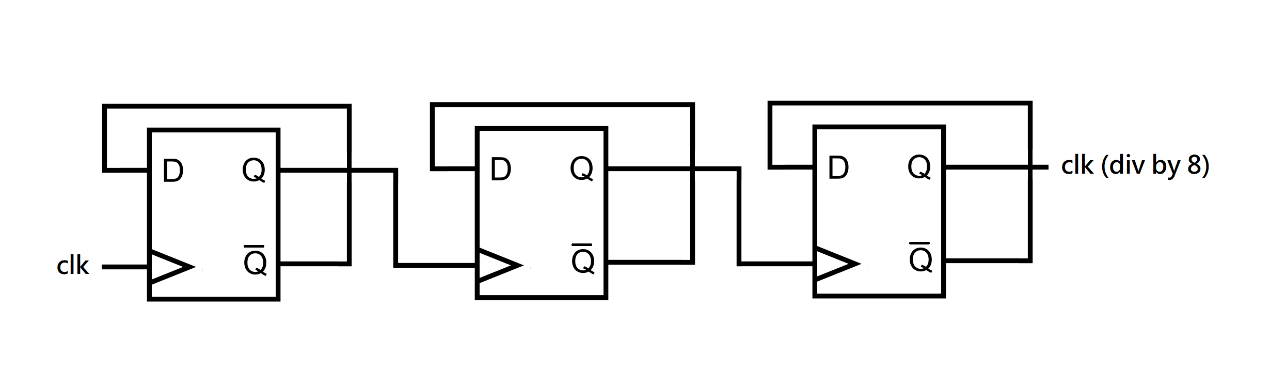
1. Clock div by 3



1. Clock div by 6



1. Clock div by 8



1. All circuit
2. **電路說明**

詳細解釋電路行為

1. **模擬結果**

波形圖(需標上訊號名稱)

數據：1.最高操作頻率(fmax) 2.功率消耗(power @fmax)

1. **參考資料**

[1] 數位積體電路設計-上課講義p263

[2] Divide by 3 and divide by 5 Circuits

https://pages.mtu.edu/~suits/electronics/Divide\_by\_3&5\_circuit.html