Memory Circuit Design Homeword #2

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1. Functionality of the Basic Gate

(a) NAND

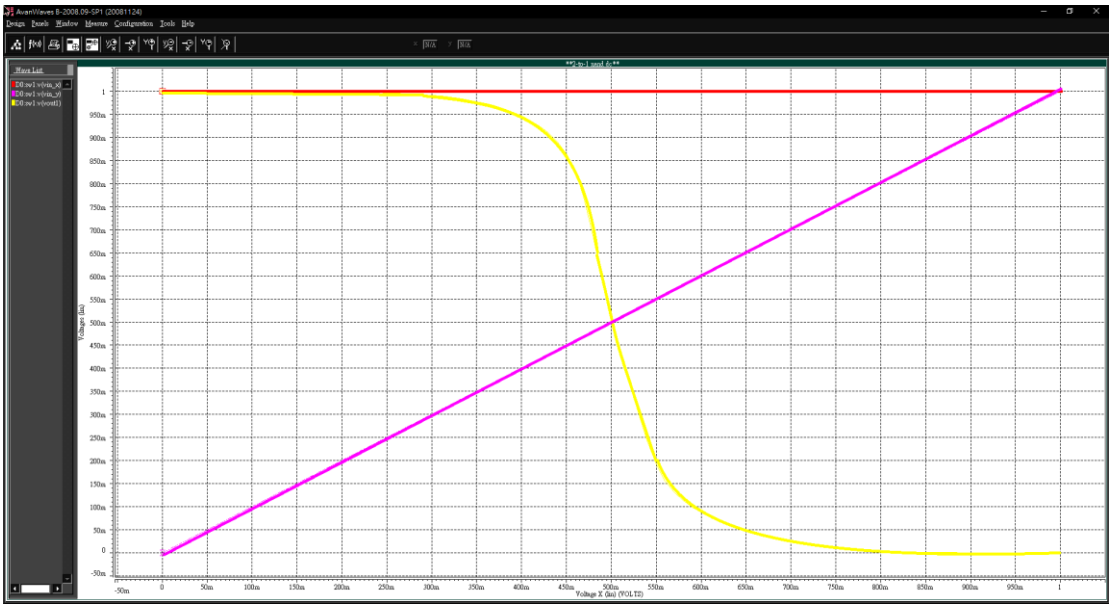
Ac:

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

訊號圖由上而下分別為 A、B 及 F。

模擬結果與真值表一致。

Dc:



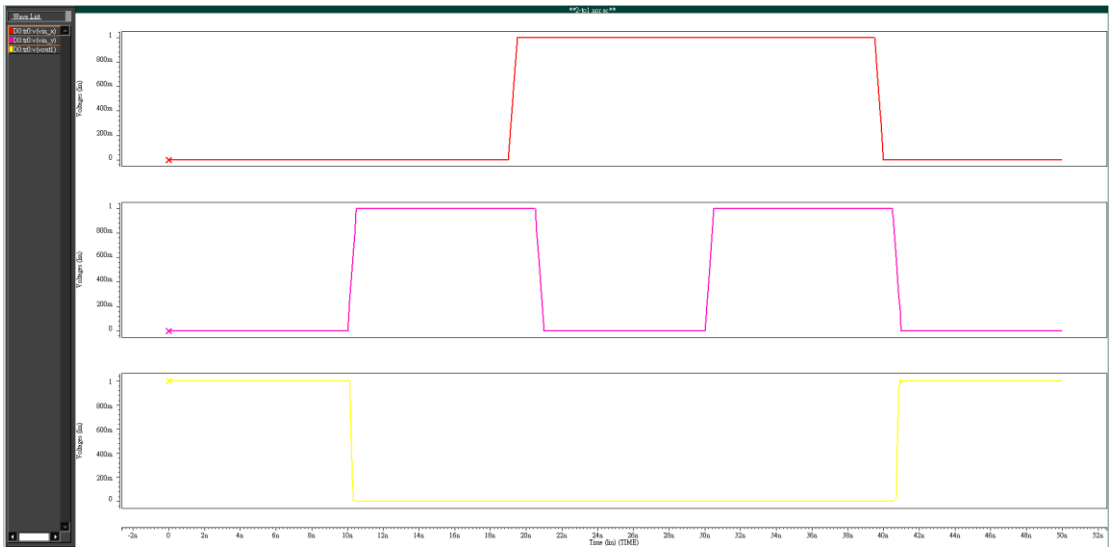
將 A 的電壓固定在 1V，使 B 從 0V 掃到 1V 可得輸出結果從 1V 反相為 0V。

```
**2-to-1 NAND DC**

.inc "C:\synopsys\65nm_bulk.pm"

MP_x vout1 vin_x vdd vdd pmos W=2.5u L=0.065u
MP_y vout1 vin_y vdd vdd pmos W=2.5u L=0.065u

MN_x vout1 vin_x net1 net1 nmos W=1u L=0.065u
MN_y net1  vin_y gnd  gnd  nmos W=1u L=0.065u

vdd vdd gnd DC 1V
vin_x vin_x gnd DC 1V
vin_y vin_y gnd pulse(0 1  2n  0.5n 0.5n 1n 4n)
$.tran 0.1ns 10ns

.OP
.dc vin_x 0V 1V 0.01V
.dc vin_y 0V 1V 0.01V
.option post

.probe v1(vout1)
.end

**end**
```

```
**2-to-1 NAND AC**

.inc "C:\synopsys\65nm_bulk.pm"

MP_x vout1 vin_x vdd vdd pmos W=2.5u L=0.065u
MP_y vout1 vin_y vdd vdd pmos W=2.5u L=0.065u

MN_x vout1 vin_x net1 net1 nmos W=1u L=0.065u
MN_y net1  vin_y gnd  gnd  nmos W=1u L=0.065u

vdd vdd gnd DC 1V
vin_x vin_x gnd pulse(0 1  21n  0.5n 0.5n 20n 40n)
vin_y vin_y gnd pulse(0 1  10n  0.5n 0.5n 10n 20n)
.tran 0.1ns 50ns

$.OP
$.dc vin_x 0V 1V 0.01V
$.dc vin_y 0V 1V 0.01V
.option post

.probe v1(vout1)
.end

**end**
```

(b) NOR

Ac:

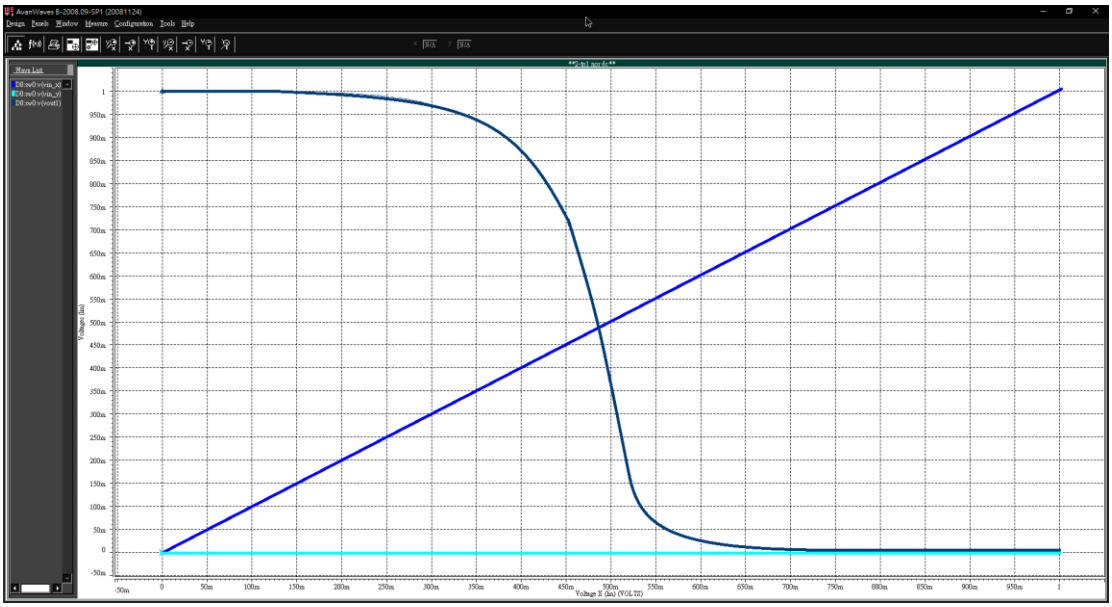


A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

訊號圖由上而下分別為 A、B 及 F。

模擬結果與真值表一致。

Dc:



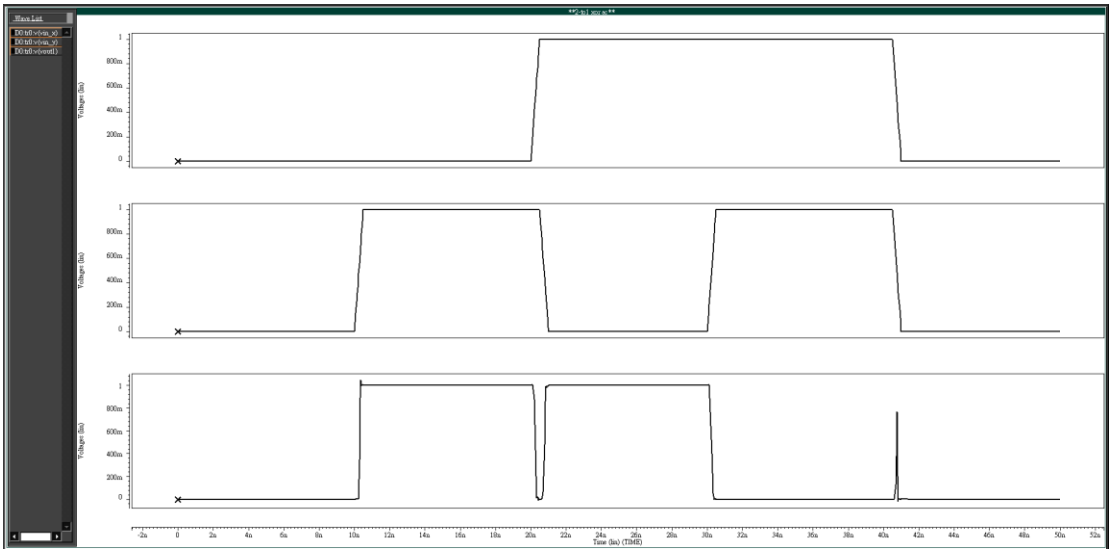
將 A 的電壓固定在 0V，使 B 從 0V 掃到 1V 可得輸出結果從 1V 反相為 0V。

```
**2-to1 NOR DC**

.inc "C:\synopsys\65nm_bulk.pm"

MP_x  net1 vin_x  vdd  vdd pmos W=2.5u L=0.065u
MP_y vout1 vin_y net1 net1 pmos W=2.5u L=0.065u

MN_x vout1 vin_x  gnd  gnd nmos W= 1u  L=0.065u
MN_y vout1 vin_y  gnd  gnd nmos W= 1u  L=0.065u

vdd vdd gnd DC 1V
vin_x vin_x gnd DC 0V
vin_y vin_y gnd pulse(0 1  2n 0.5n 0.5n 1n 4n)

.OP
.dc vin_x 0V 1V 0.01V
.dc vin_y 0V 1V 0.01V
.option post

.probe v1(vout1)
.end

**end**
```

```
**2-to1 NOR AC**

.inc "C:\synopsys\65nm_bulk.pm"

MP_x  net1 vin_x  vdd  vdd pmos W=2.5u L=0.065u
MP_y vout1 vin_y net1 net1 pmos W=2.5u L=0.065u

MN_x vout1 vin_x  gnd  gnd nmos W= 1u  L=0.065u
MN_y vout1 vin_y  gnd  gnd nmos W= 1u  L=0.065u

vdd vdd gnd DC 1V
vin_x vin_x gnd pulse(0 1  19n 0.5n 0.5n 20n 40n)
vin_y vin_y gnd pulse(0 1  10n 0.5n 0.5n 10n 20n)

.option post
.tran 0.1ns 50ns

.probe v1(vout1)
.end

**end**
```

(c) XOR

Ac:

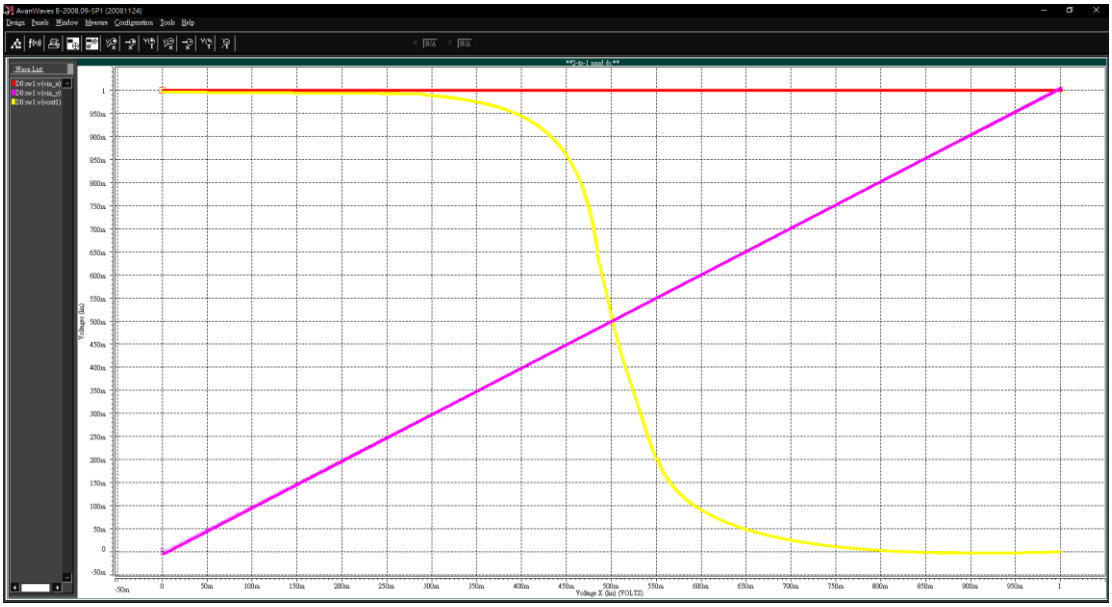


A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

訊號圖由上而下分別為 A、B 及 F。

模擬結果與真值表一致。

Dc:



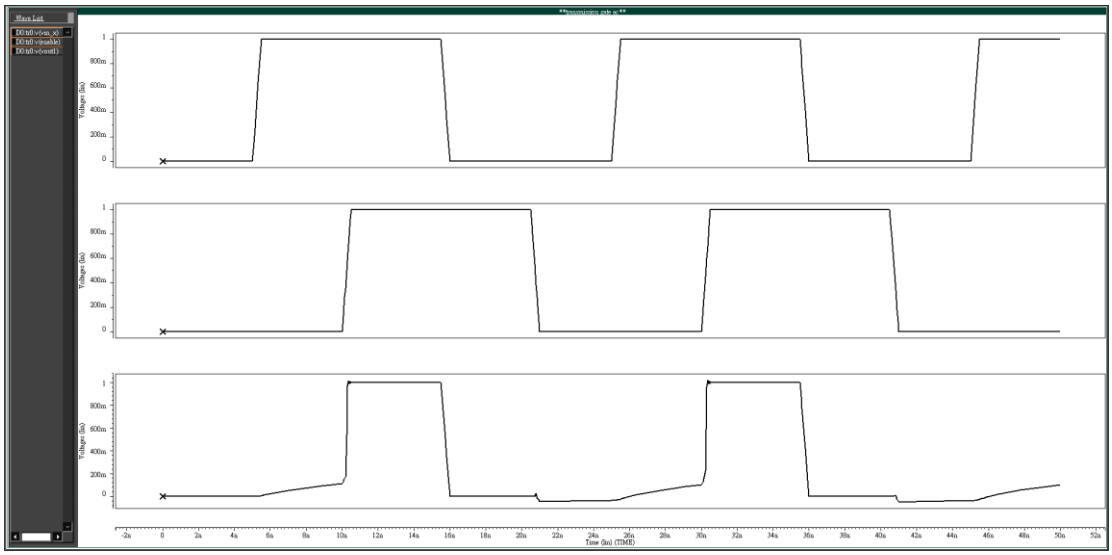
將 A 的電壓固定在 1V，使 B 從 0V 掃到 1V 可得輸出結果從 1V 反相為 0V。

```
**2-to1 XOR DC**

.inc "C:\synopsys\65nm_bulk.pm"

Xinv_x vin_x vin_xb vdd gnd inv
Xinv_y vin_y vin_yb vdd gnd inv

MP_x1  net1 vin_xb  vdd  vdd pmos W=2.5u L=0.065u
MP_y1  net1 vin_yb  vdd  vdd pmos W=2.5u L=0.065u
MP_x2 vout1  vin_y net1 net1 pmos W=2.5u L=0.065u
MP_y2 vout1  vin_x net1 net1 pmos W=2.5u L=0.065u

MN_x1 vout1  vin_x net2 net2 nmos W= 1u  L=0.065u
MN_y1  net2  vin_y  gnd  gnd nmos W= 1u  L=0.065u
MN_x2 vout1 vin_xb net3 net3 nmos W= 1u  L=0.065u
MN_y2  net3 vin_yb  gnd  gnd nmos W= 1u  L=0.065u

vdd vdd gnd DC 1V
vin_x vin_x gnd pulse(0 1 3.5n 0.5n 0.5n 3.5n 8n)
vin_y vin_y gnd pulse(0 1   2n 0.5n 0.5n   1n 4n)

.subckt inv in out vdd GND
    Mp1 out in vdd vdd pmos w=2.5u l=0.065u
    Mn1 out in GND GND nmos w=1u l=0.065u
.ends

.OP
.dc vin_x 0V 1V 0.01V
.dc vin_y 0V 1V 0.01V
.option post

.probe v1(vout1)
.end

**end**
```

```
**2-to1 XOR AC**

.inc "C:\synopsys\65nm_bulk.pm"

Xinv_x vin_x vin_xb vdd gnd inv
Xinv_y vin_y vin_yb vdd gnd inv

MP_x1  net1 vin_xb  vdd  vdd pmos W=2.5u L=0.065u
MP_y1  net1 vin_yb  vdd  vdd pmos W=2.5u L=0.065u
MP_x2 vout1  vin_y net1 net1 pmos W=2.5u L=0.065u
MP_y2 vout1  vin_x net1 net1 pmos W=2.5u L=0.065u

MN_x1 vout1  vin_x net2 net2 nmos W= 1u  L=0.065u
MN_y1  net2  vin_y  gnd  gnd nmos W= 1u  L=0.065u
MN_x2 vout1 vin_xb net3 net3 nmos W= 1u  L=0.065u
MN_y2  net3 vin_yb  gnd  gnd nmos W= 1u  L=0.065u

vdd vdd gnd DC 1V
vin_x vin_x gnd pulse(0 1 20n 0.5n 0.5n 20n 40n)
vin_y vin_y gnd pulse(0 1 10n 0.5n 0.5n   10n 20n)

.subckt inv in out vdd GND
    Mp1 out in vdd vdd pmos w=2.5u l=0.065u
    Mn1 out in GND GND nmos w=1u l=0.065u
.ends

.option post
.tran 0.1ns 50ns

.probe v1(vout1)
.end

**end**
```

2. Functionality of the Transmission Gate

Ac:

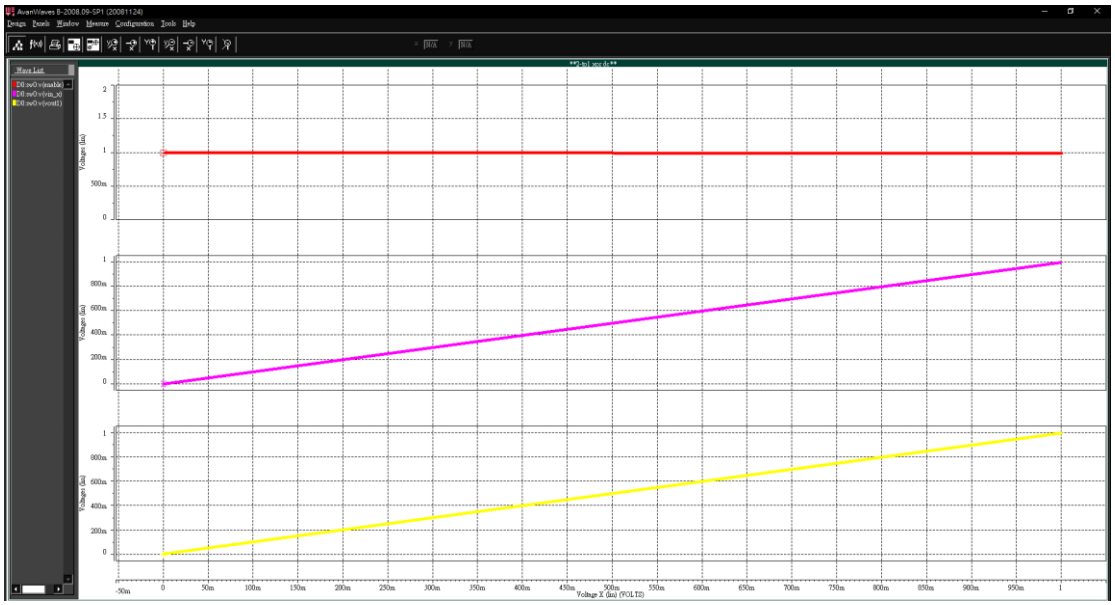


Enable	Out
1	Xin
0	out

訊號由上至下分別為 xin、enable 和 out。

可以觀察到輸出在 enable 為 1V 時才允許 xin 完整通過。

Dc:



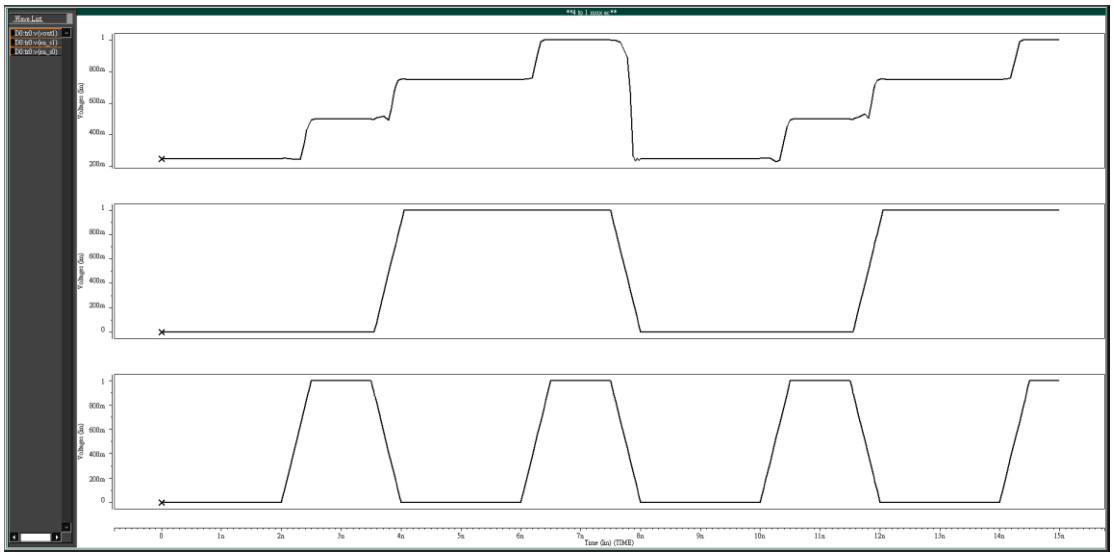
直流分析結果與假設的結果一致。

```
**2-to1 XOR DC**

.inc "C:\synopsys\65nm_bulk.pm"

Xenable enable enable_bar vdd gnd inv

MP1 vout1 enable_bar vin_x vin_x pmos W=2.5u L=0.065u
MN1 vin_x     enable vout1 vout1 nmos W=  1u L=0.065u

vdd vdd gnd DC 1V
venable enable gnd DC 1V
vin_x vin_x gnd DC 1V

.subckt inv in out vdd GND
    Mp1 out in vdd vdd pmos w=2.5u l=0.065u
    Mn1 out in GND GND nmos w=  1u l=0.065u
.ends

.OP
.dc vin_x 0V 1V 0.01V
.option post

.probe v1(vout1)
.end

**end**
```

```
**Transmission Gate AC**

.inc "C:\synopsys\65nm_bulk.pm"

Xenable enable enable_bar vdd gnd inv

MP1 vout1 enable_bar vin_x vdd   pmos W=2.5u L=0.065u
MN1 vin_x enable vout1 gnd   nmos W= 1u  L=0.065u

vdd vdd gnd DC 1V
venable enable gnd pulse( 0 1 10n 0.5n 0.5n 10n  20n)
vin_x   vin_x gnd pulse ( 0 1  5n 0.5n 0.5n    10n   20n)

.subckt inv in out vdd GND
    Mp1 out in vdd vdd pmos w=2.5u l=0.065u
    Mn1 out in GND GND nmos w=  1u l=0.065u
.ends

.tran 0.1ns 50ns
.option post

.probe v1(vout1)
.end

**end**
```

3. Functionality of the Basic Gate (4-to-1 Mux)

Ac:



S1	S0	F
0	0	0.25v
0	1	0.5V
1	0	0.75V
1	1	1V

訊號由上而下分別為 F、S1 及 S0。

此次模擬為了能看出是否有從四個輸出中選出特定的值，分別將 A, B, C 及 D 四個訊號的值訂為 0.25V, 0.5V, 0.75V, 1V。

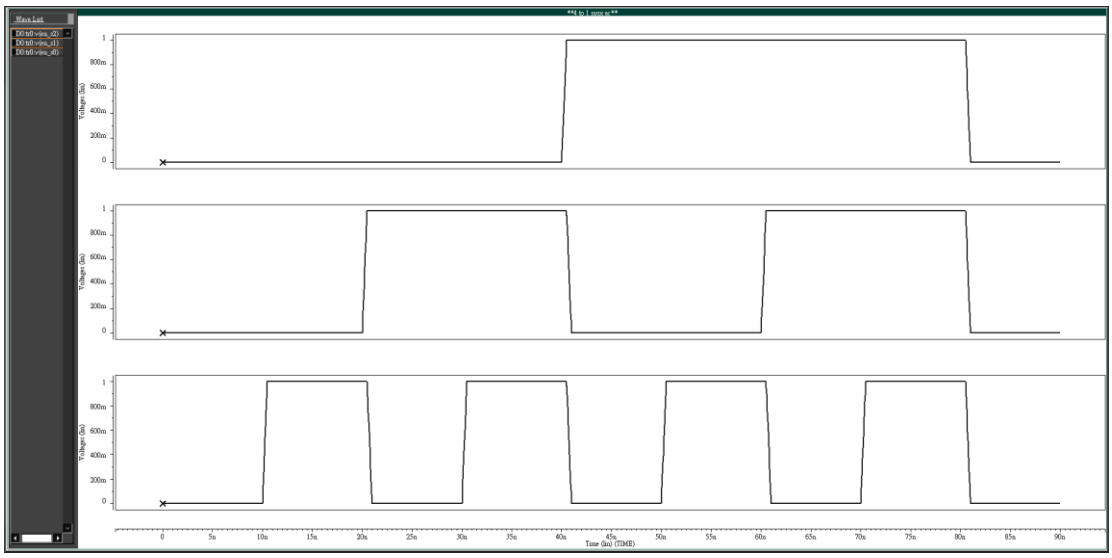
模擬結果與假設結果一致。

```
**4 to 1 mux ac**

.inc "C:\synopsys\65nm_bulk.pm"

$ circuit describe

Xain    va net1   en_s0  en_s0b vdd gnd tran_gate
Xbin    vb net1  en_s0b   en_s0 vdd gnd tran_gate
Xcin    vc net2   en_s0  en_s0b vdd gnd tran_gate
Xdin    vd net2  en_s0b   en_s0 vdd gnd tran_gate

Xs1_1   net1 vout1   en_s1  en_s1b vdd gnd tran_gate
Xs1_2   net2 vout1  en_s1b   en_s1 vdd gnd tran_gate

Xinv_s0  en_s0 en_s0b vdd gnd inv
Xinv_s1  en_s1 en_s1b vdd gnd inv

$ voltage soure and other setting
vdd vdd gnd DC 1V
ven_s0 en_s0 gnd pulse( 0 1    2n 0.5n 0.5n    1n 4n)
ven_s1 en_s1 gnd pulse( 0 1 3.55n 0.5n 0.5n 3.45n 8n)
va    va gnd dc 0.25v
vb    vb gnd dc 0.5v
vc    vc gnd dc 0.75v
vd    vd gnd dc 1v

$ inverter module
.subckt inv in out vdd GND
    Mp1 out in vdd vdd pmos w=2.5u l=0.065u
    Mn1 out in GND GND nmos w=  1u l=0.065u
.ends

$ transmission gate module
.subckt tran_gate in out en_p en_n vdd gnd
    Mp out en_p  in  vdd pmos W=2.5u L=0.065u
    Mn in  en_n out  gnd nmos W=  1u L=0.065u

    Xinv en en_b vdd gnd inv
.ends

.tran 0.1ns 15ns
.option post

.probe v1(vout1)
.end

**end**
```

4. Functionality of the Decoder (3-to-8 decoder)

Ac:

Input:



Output:

S2	S1	S0	F
0	0	0	Out1
0	0	1	Out2
0	1	0	Out3
0	1	1	Out4
1	0	0	Out5
1	0	1	Out6
1	1	0	Out7
1	1	1	Out8

由 S2 到 S0 分別代表 decoder 的輸入。

輸出結果與預期符合。

```
**decorder ac**

.inc "C:\synopsys\65nm_bulk.pm"

$ circuit describe

Xinv0 en_s0 en_s0b vdd gnd inv
Xinv1 en_s1 en_s1b vdd gnd inv
Xinv2 en_s2 en_s2b vdd gnd inv

Xand0 en_s0b en_s1b en_s2b vy0 vdd gnd and3
Xand1 en_s0  en_s1b en_s2b vy1 vdd gnd and3
Xand2 en_s0b en_s1  en_s2b vy2 vdd gnd and3
Xand3 en_s0  en_s1  en_s2b vy3 vdd gnd and3
Xand4 en_s0b en_s1b en_s2  vy4 vdd gnd and3
Xand5 en_s0  en_s1b en_s2  vy5 vdd gnd and3
Xand6 en_s0b en_s1  en_s2  vy6 vdd gnd and3
Xand7 en_s0  en_s1  en_s2  vy7 vdd gnd and3


$ voltage soure and other setting
vdd vdd gnd DC 1V
$ven_s0 en_s0 gnd pulse( 0 1    2n 0.5n 0.5n     1n     4n)
$ven_s1 en_s1 gnd pulse( 0 1  3.5n 0.5n 0.5n   3.5n     8n)
$ven_s2 en_s2 gnd pulse( 0 1  7.5n 0.5n 0.5n    30n    30n)
ven_s0 en_s0 gnd pulse( 0 1    10.5n 0.5n 0.5n     9n     20n)
ven_s1 en_s1 gnd pulse( 0 1    20n 0.5n 0.5n   19n     40n)
ven_s2 en_s2 gnd pulse( 0 1    39.5n 0.5n 0.5n    39n    80n)
$va   va gnd dc 0v
$vb   vb gnd dc 0.5v
$vc   vc gnd dc 1v

$ 3 to 1 AND gate
.subckt and3 ain bin cin out vdd gnd
    Mpa net1 ain  vdd vdd pmos W=2.5u L=0.065u
    Mpb net2 bin net1 vdd pmos W=2.5u L=0.065u
    Mpc out  cin net2 vdd pmos W=2.5u L=0.065u

    Mna out ain gnd gnd nmos W=1u L=0.065u
    Mnb out bin gnd gnd nmos W=1u L=0.065u
    Mnc out cin gnd gnd nmos W=1u L=0.065u
.ends

$ inverter module
.subckt inv in out vdd GND
    Mp1 out in vdd vdd pmos w=2.5u l=0.065u
    Mn1 out in GND GND nmos w=  1u l=0.065u
.ends
```

```
$ transmission gate module
.subckt tran_gate in out en_p en_n vdd gnd
    Mp out en_p  in  vdd pmos W=2.5u L=0.065u
    Mn in  en_n out  gnd nmos W=  1u L=0.065u

    Xinv en en_b vdd gnd inv
.ends

.tran 0.1ns 90ns
.option post

.probe v0(vy0)
.probe v1(vy1)
.probe v2(vy2)
.probe v3(vy3)
.probe v4(vy4)
.probe v5(vy5)
.probe v6(vy6)
.probe v7(vy7)
.end

**end**
```