

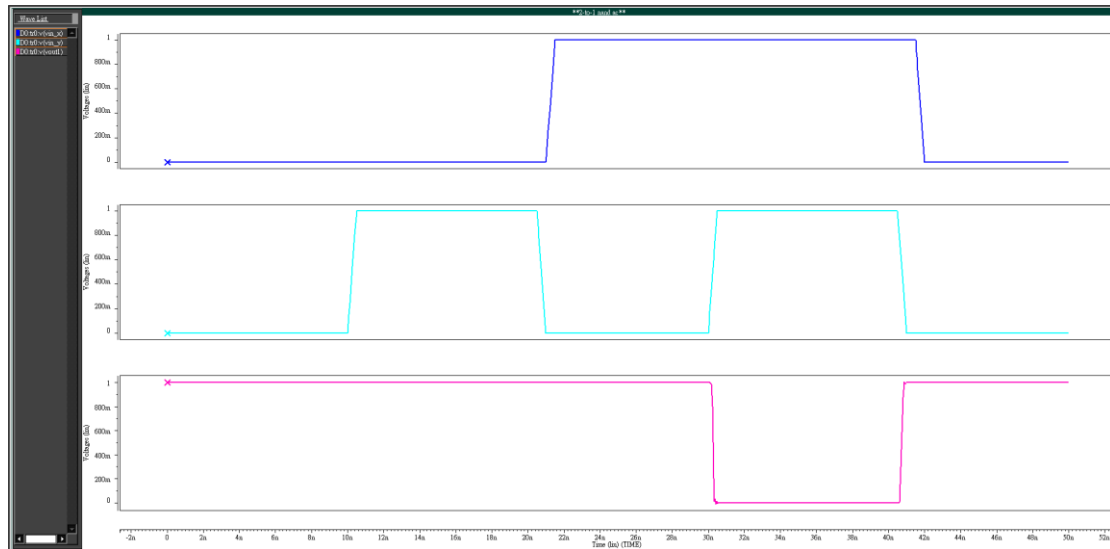
Memory Circuit Design Homework #2

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1. Functionality of the Basic Gate

(a) NAND

Ac:

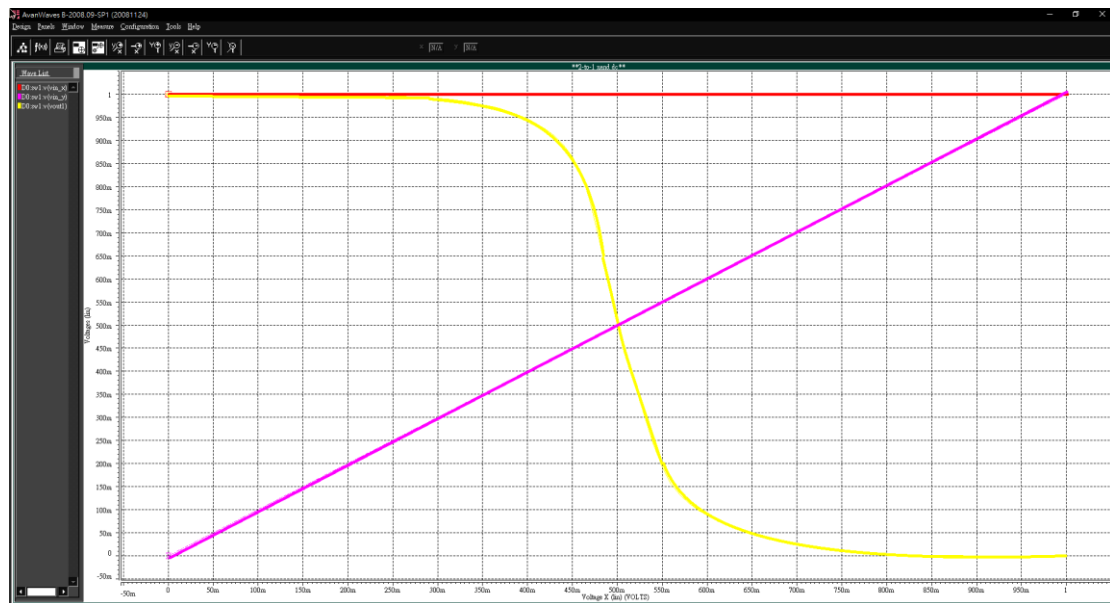


A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

訊號圖由上而下分別為 A、B 及 F。

模擬結果與真值表一致。

Dc:



將 A 的電壓固定在 1V，使 B 從 0V 掃到 1V 可得輸出結果從 1V 反相為 0V。

```

1  **2-to-1 NAND DC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  MP_x vout1 vin_x vdd vdd pmos W=2.5u L=0.065u
6  MP_y vout1 vin_y vdd vdd pmos W=2.5u L=0.065u
7
8  MN_x vout1 vin_x net1 net1 nmos W=1u L=0.065u
9  MN_y net1 vin_y gnd gnd nmos W=1u L=0.065u
10
11 vdd vdd gnd DC 1V
12 vin_x vin_x gnd DC 1V
13 vin_y vin_y gnd pulse(0 1 2n 0.5n 0.5n 1n 4n)
14 $.tran 0.1ns 10ns
15
16 .OP
17 .dc vin_x 0V 1V 0.01V
18 .dc vin_y 0V 1V 0.01V
19 .option post
20
21 .probe v1(vout1)
22 .end
23
24 **end**

```

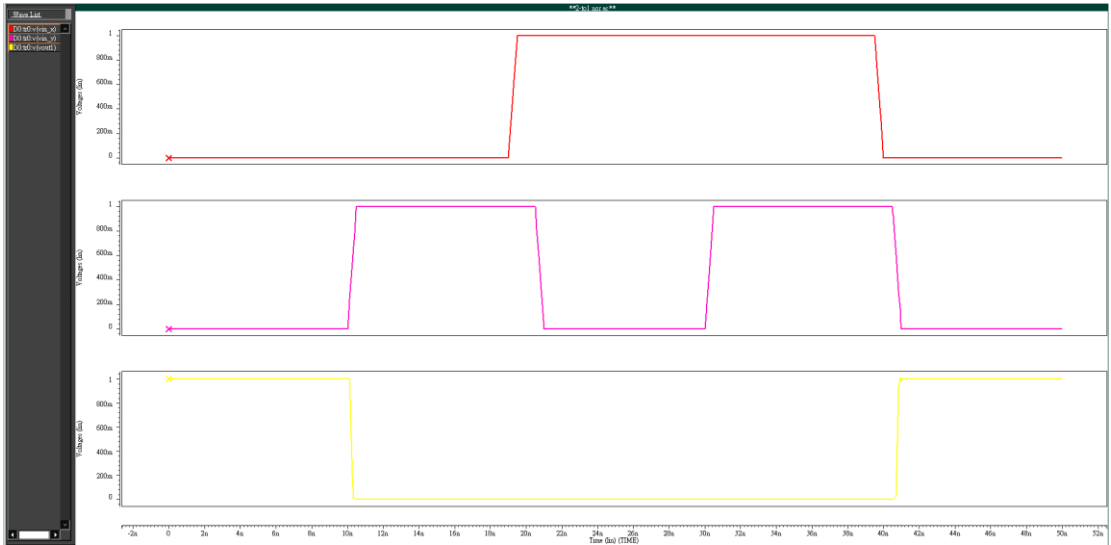
```

1  **2-to-1 NAND AC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  MP_x vout1 vin_x vdd vdd pmos W=2.5u L=0.065u
6  MP_y vout1 vin_y vdd vdd pmos W=2.5u L=0.065u
7
8  MN_x vout1 vin_x net1 net1 nmos W=1u L=0.065u
9  MN_y net1 vin_y gnd gnd nmos W=1u L=0.065u
10
11 vdd vdd gnd DC 1V
12 vin_x vin_x gnd pulse(0 1 21n 0.5n 0.5n 20n 40n)
13 vin_y vin_y gnd pulse(0 1 10n 0.5n 0.5n 10n 20n)
14 .tran 0.1ns 50ns
15
16 $.OP
17 $.dc vin_x 0V 1V 0.01V
18 $.dc vin_y 0V 1V 0.01V
19 .option post
20
21 .probe v1(vout1)
22 .end
23
24 **end**

```

(b) NOR

Ac:

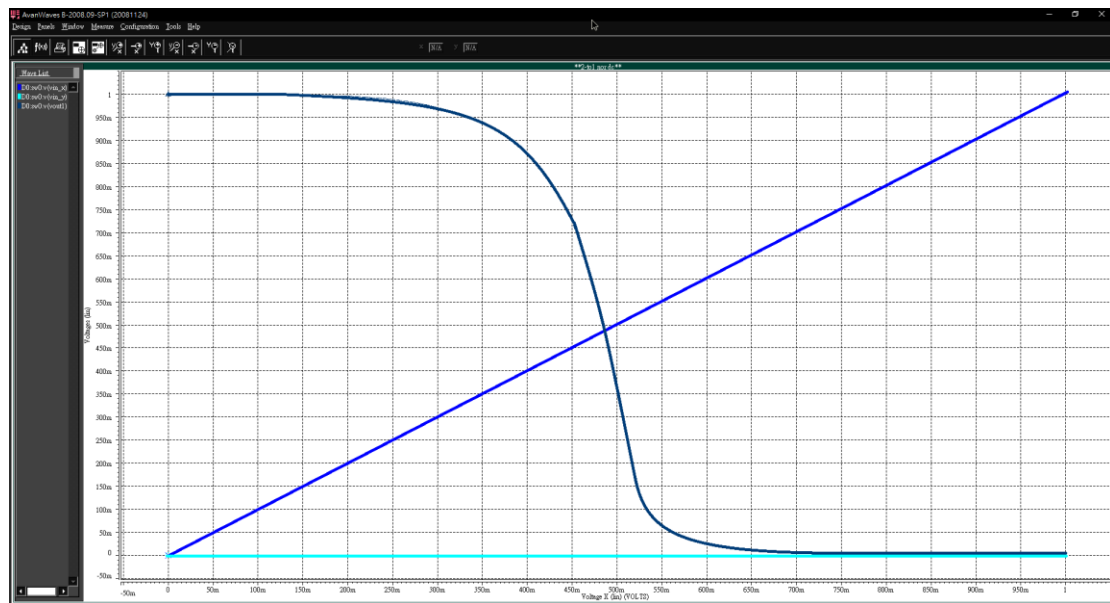


A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

訊號圖由上而下分別為 A、B 及 F。

模擬結果與真值表一致。

Dc:



將 A 的電壓固定在 0V，使 B 從 0V 掃到 1V 可得輸出結果從 1V 反相為 0V。

```

1  **2-tol NOR DC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  MP_x net1 vin_x vdd vdd pmos W=2.5u L=0.065u
6  MP_y vout1 vin_y net1 net1 pmos W=2.5u L=0.065u
7
8  MN_x vout1 vin_x gnd gnd nmos W= 1u L=0.065u
9  MN_y vout1 vin_y gnd gnd nmos W= 1u L=0.065u
10
11 vdd vdd gnd DC 1V
12 vin_x vin_x gnd DC 0V
13 vin_y vin_y gnd pulse(0 1 2n 0.5n 0.5n 1n 4n)
14
15 .OP
16 .dc vin_x 0V 1V 0.01V
17 .dc vin_y 0V 1V 0.01V
18 .option post
19
20 .probe v1(vout1)
21 .end
22
23 **end**

```

```

1  **2-tol NOR AC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  MP_x net1 vin_x vdd vdd pmos W=2.5u L=0.065u
6  MP_y vout1 vin_y net1 net1 pmos W=2.5u L=0.065u
7
8  MN_x vout1 vin_x gnd gnd nmos W= 1u L=0.065u
9  MN_y vout1 vin_y gnd gnd nmos W= 1u L=0.065u
10
11 vdd vdd gnd DC 1V
12 vin_x vin_x gnd pulse(0 1 19n 0.5n 0.5n 20n 40n)
13 vin_y vin_y gnd pulse(0 1 10n 0.5n 0.5n 10n 20n)
14
15 .option post
16 .tran 0.1ns 50ns
17
18 .probe v1(vout1)
19 .end
20
21 **end**
22

```

(c) XOR

Ac:

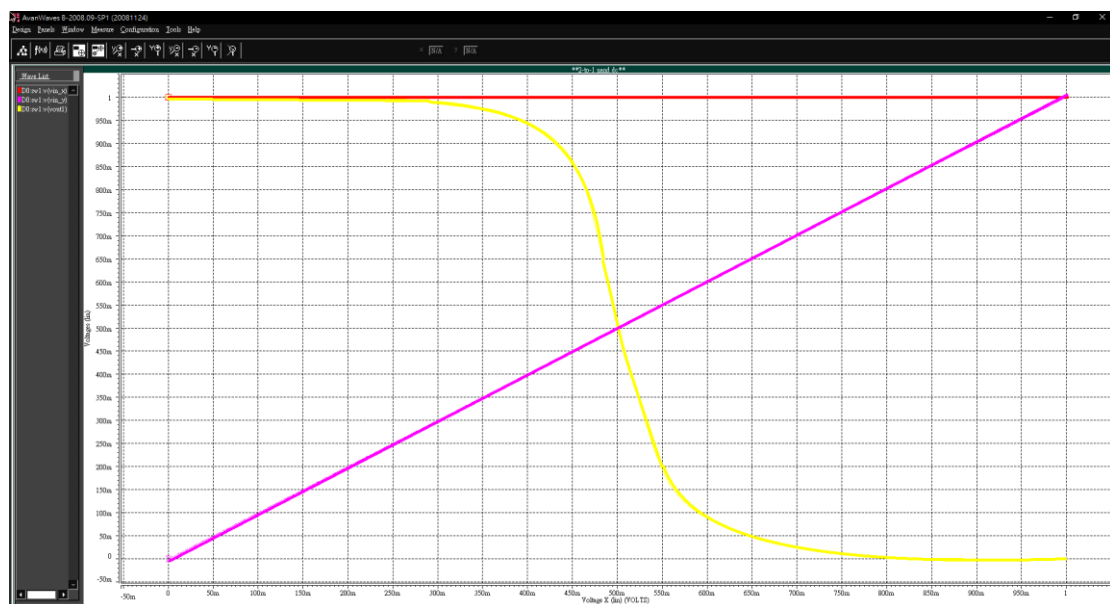


A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

訊號圖由上而下分別為 A、B 及 F。

模擬結果與真值表一致。

Dc:



將 A 的電壓固定在 1V，使 B 從 0V 掃到 1V 可得輸出結果從 1V 反相為 0V。

```

1  **2-to1 XOR DC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  Xinv_x vin_x vin_xb vdd gnd inv
6  Xinv_y vin_y vin_yb vdd gnd inv
7
8  MP_x1 net1 vin_xb vdd vdd pmos W=2.5u L=0.065u
9  MP_y1 net1 vin_yb vdd vdd pmos W=2.5u L=0.065u
10 MP_x2 vout1 vin_y net1 net1 pmos W=2.5u L=0.065u
11 MP_y2 vout1 vin_x net1 net1 pmos W=2.5u L=0.065u
12
13 MN_x1 vout1 vin_x net2 net2 nmos W= 1u L=0.065u
14 MN_y1 net2 vin_y gnd gnd nmos W= 1u L=0.065u
15 MN_x2 vout1 vin_xb net3 net3 nmos W= 1u L=0.065u
16 MN_y2 net3 vin_yb gnd gnd nmos W= 1u L=0.065u
17
18 vdd vdd gnd DC 1V
19 vin_x vin_x gnd pulse(0 1 3.5n 0.5n 0.5n 3.5n 8n)
20 vin_y vin_y gnd pulse(0 1 2n 0.5n 0.5n 1n 4n)
21
22 .subckt inv in out vdd GND
23     Mpl out in vdd vdd pmos w=2.5u l=0.065u
24     Mnl out in GND GND nmos w=1u l=0.065u
25 .ends
26
27 .OP
28 .dc vin_x 0V 1V 0.01V
29 .dc vin_y 0V 1V 0.01V
30 .option post
31
32 .probe v1(vout1)
33 .end
34
35 **end**

```



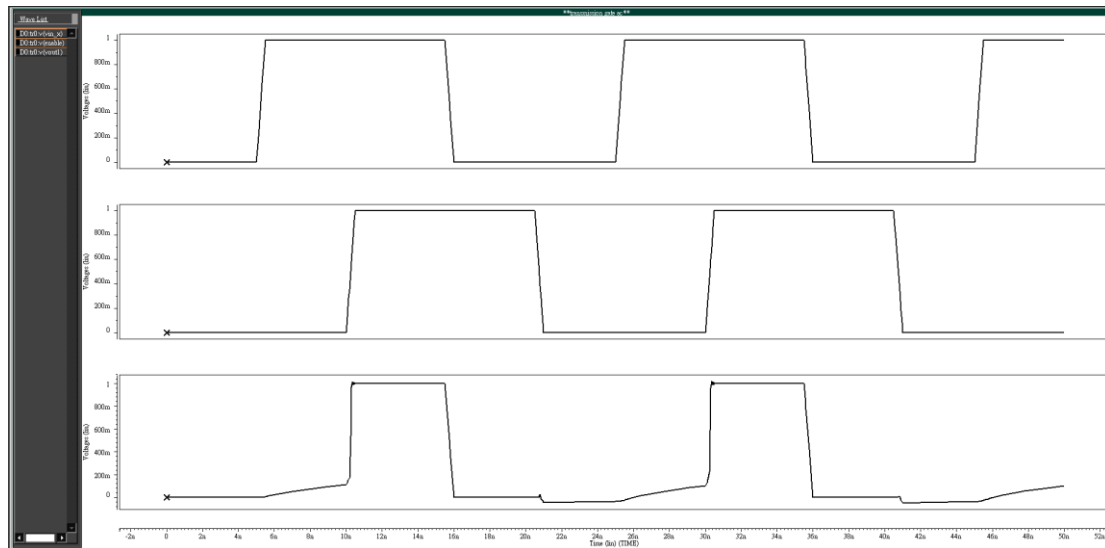
```

1  **2-tol XOR AC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  Xinv_x vin_x vin_xb vdd gnd inv
6  Xinv_y vin_y vin_yb vdd gnd inv
7
8  MP_x1 net1 vin_xb vdd vdd pmos W=2.5u L=0.065u
9  MP_y1 net1 vin_yb vdd vdd pmos W=2.5u L=0.065u
10 MP_x2 vout1 vin_y net1 net1 pmos W=2.5u L=0.065u
11 MP_y2 vout1 vin_x net1 net1 pmos W=2.5u L=0.065u
12
13 MN_x1 vout1 vin_x net2 net2 nmos W= 1u L=0.065u
14 MN_y1 net2 vin_y gnd gnd nmos W= 1u L=0.065u
15 MN_x2 vout1 vin_xb net3 net3 nmos W= 1u L=0.065u
16 MN_y2 net3 vin_yb gnd gnd nmos W= 1u L=0.065u
17
18 vdd vdd gnd DC 1V
19 vin_x vin_x gnd pulse(0 1 20n 0.5n 0.5n 20n 40n)
20 vin_y vin_y gnd pulse(0 1 10n 0.5n 0.5n 10n 20n)
21
22 .subckt inv in out vdd GND
23     Mp1 out in vdd vdd pmos w=2.5u l=0.065u
24     Mn1 out in GND GND nmos w=1u l=0.065u
25 .ends
26
27 .option post
28 .tran 0.1ns 50ns
29
30 .probe v1(vout1)
31 .end
32
33 **end**

```

2. Functionality of the Transmission Gate

Ac:

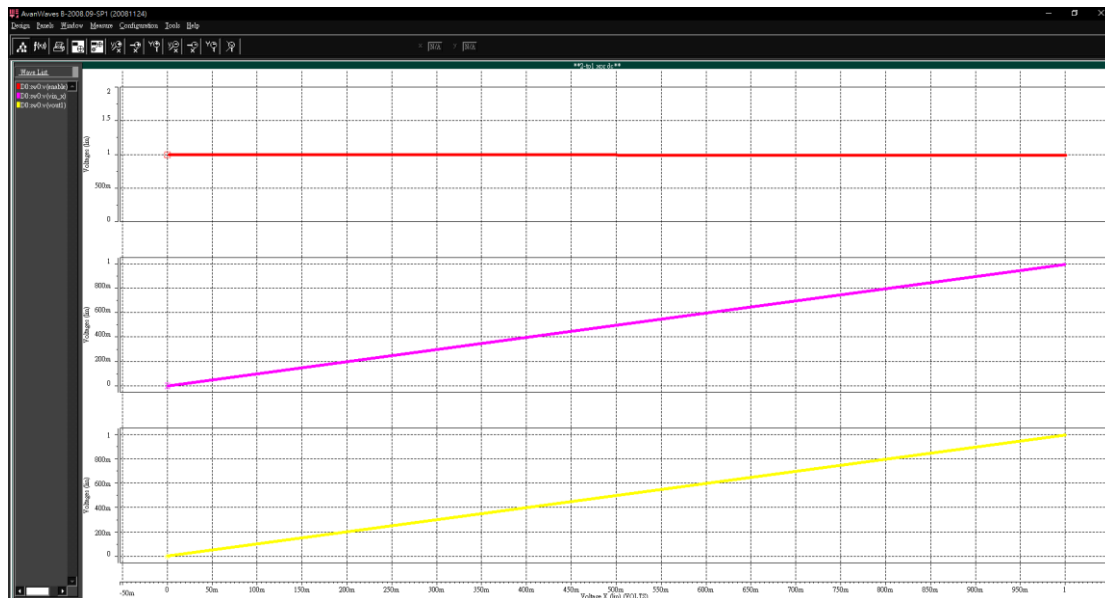


Enable	Out
1	Xin
0	out

訊號由上至下分別為 xin、enable 和 out。

可以觀察到輸出在 enable 為 1V 時才允許 xin 完整通過。

Dc:



直流分析結果與假設的結果一致。

```

1  **2-to1 XOR DC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  Xenable enable enable_bar vdd gnd inv
6
7  MP1 vout1 enable_bar vin_x vin_x pmos W=2.5u L=0.065u
8  MN1 vin_x      enable vout1 vout1 nmos W= 1u L=0.065u
9
10 vdd vdd gnd DC 1V
11 venable enable gnd DC 1V
12 vin_x vin_x gnd DC 1V
13
14 .subckt inv in out vdd GND
15     Mp1 out in vdd vdd pmos w=2.5u l=0.065u
16     Mn1 out in GND GND nmos w= 1u l=0.065u
17 .ends
18
19 .OP
20 .dc vin_x 0V 1V 0.01V
21 .option post
22
23 .probe v1(vout1)
24 .end
25
26 **end**

```

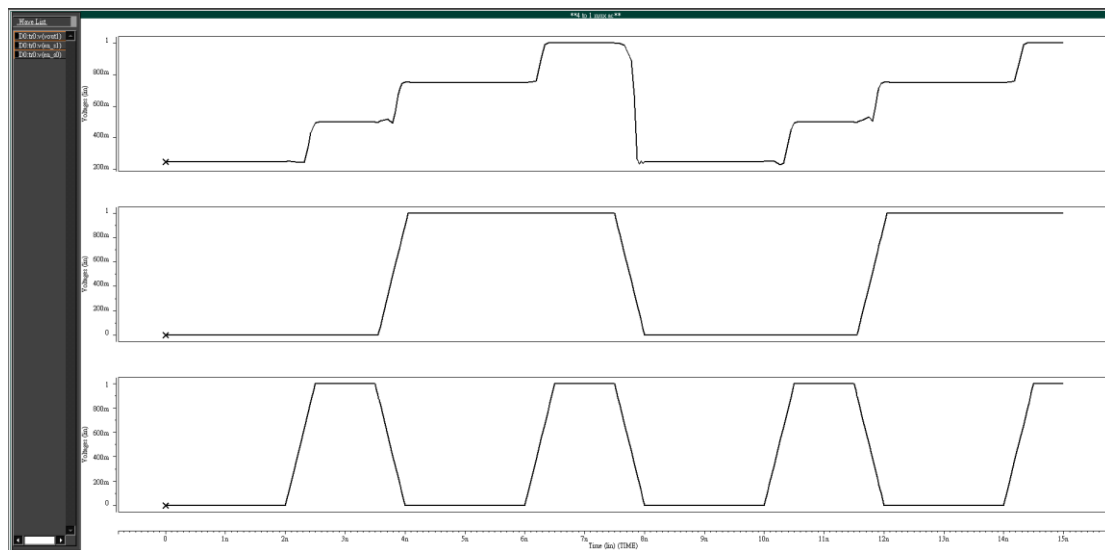
```

1  **Transmission Gate AC**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  Xenable enable enable_bar vdd gnd inv
6
7  MP1 vout1 enable_bar vin_x vdd      pmos W=2.5u L=0.065u
8  MN1 vin_x enable vout1 gnd      nmos W= 1u  L=0.065u
9
10 vdd vdd gnd DC 1V
11 venable enable gnd pulse( 0 1 10n 0.5n 0.5n 10n 20n)
12 vin_x  vin_x gnd pulse ( 0 1 5n 0.5n 0.5n 10n 20n)
13
14 .subckt inv in out vdd GND
15     Mp1 out in vdd vdd pmos w=2.5u l=0.065u
16     Mn1 out in GND GND nmos w= 1u l=0.065u
17 .ends
18
19 .tran 0.1ns 50ns
20 .option post
21
22 .probe v1(vout1)
23 .end
24
25 **end**

```

3. Functionality of the Basic Gate (4-to-1 Mux)

Ac:



S1	S0	F
0	0	0.25v
0	1	0.5V
1	0	0.75V
1	1	1V

訊號由上而下分別為 F、S1 及 S0。

此次模擬為了能看出是否有從四個輸出中選出特定的值，分別將 A, B, C 及 D 四個訊號的值訂為 0.25V, 0.5V, 0.75V, 1V。

模擬結果與假設結果一致。

```

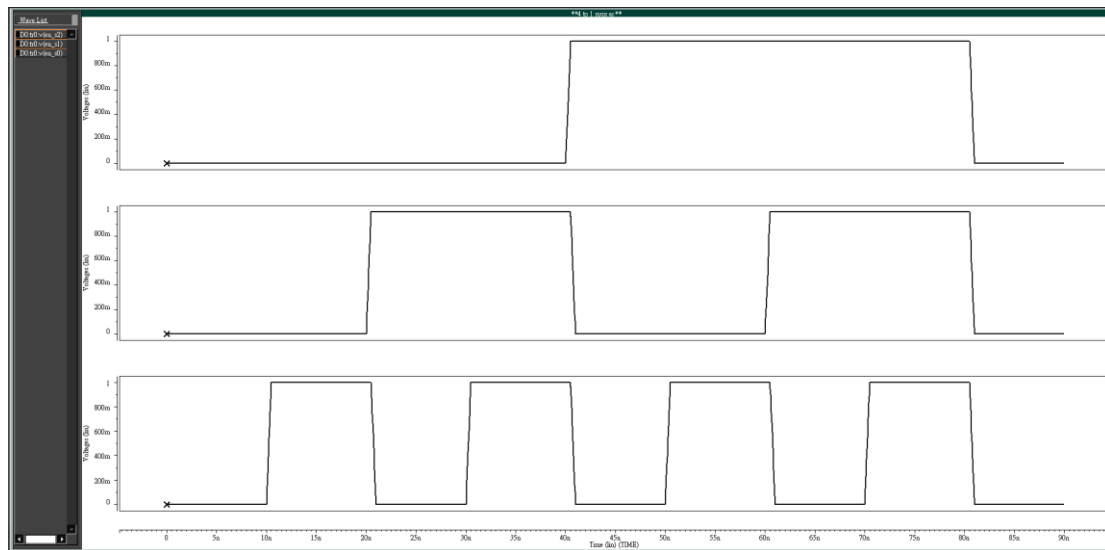
1  **4 to 1 mux ac**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  $ circuit describe
6
7  Xain    va net1    en_s0    en_s0b vdd gnd tran_gate
8  Xbin    vb net1    en_s0b    en_s0 vdd gnd tran_gate
9  Xcin    vc net2    en_s0    en_s0b vdd gnd tran_gate
10 Xdin    vd net2    en_s0b    en_s0 vdd gnd tran_gate
11
12 Xs1_1    net1 vout1    en_s1    en_s1b vdd gnd tran_gate
13 Xs1_2    net2 vout1    en_s1b    en_s1 vdd gnd tran_gate
14
15 Xinv_s0  en_s0 en_s0b vdd gnd inv
16 Xinv_s1  en_s1 en_s1b vdd gnd inv
17
18 $ voltage soure and other setting
19 vdd vdd gnd DC 1V
20 ven_s0 en_s0 gnd pulse( 0 1    2n 0.5n 0.5n    1n 4n)
21 ven_s1 en_s1 gnd pulse( 0 1 3.55n 0.5n 0.5n 3.45n 8n)
22 va     va gnd dc 0.25v
23 vb     vb gnd dc 0.5v
24 vc     vc gnd dc 0.75v
25 vd     vd gnd dc 1v
26
27 $ inverter module
28 .subckt inv in out vdd GND
29     Mp1 out in vdd vdd pmos w=2.5u l=0.065u
30     Mn1 out in GND GND nmos w= 1u l=0.065u
31 .ends
32
33 $ transmission gate module
34 .subckt tran_gate in out en_p en_n vdd gnd
35     Mp out en_p in vdd pmos W=2.5u L=0.065u
36     Mn in en_n out gnd nmos W= 1u L=0.065u
37
38     Xinv en en_b vdd gnd inv
39 .ends
40
41 .tran 0.1ns 15ns
42 .option post
43
44 .probe v1(vout1)
45 .end
46
47 **end**

```

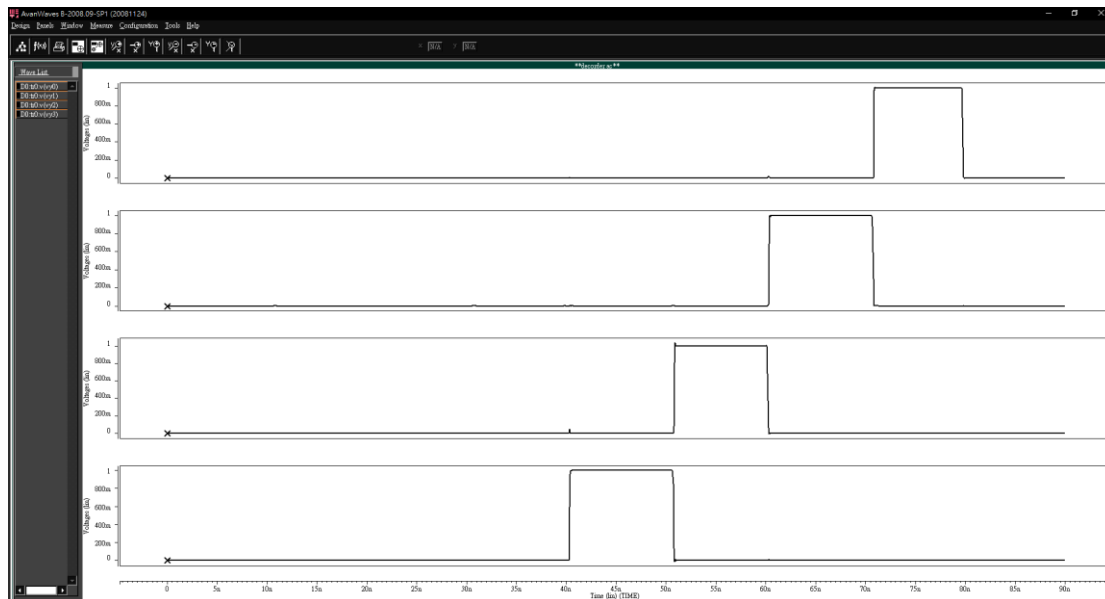
4. Functionality of the Decoder (3-to-8 decoder)

Ac:

Input:



Output:





S2	S1	S0	F
0	0	0	Out1
0	0	1	Out2
0	1	0	Out3
0	1	1	Out4
1	0	0	Out5
1	0	1	Out6
1	1	0	Out7
1	1	1	Out8

由 S2 到 S0 分別代表 decoder 的輸入。

輸出結果與預期符合。

```

1  **decoder ac**
2
3  .inc "C:\synopsys\65nm_bulk.pm"
4
5  $ circuit describe
6
7  Xinv0 en_s0 en_s0b vdd gnd inv
8  Xinv1 en_s1 en_s1b vdd gnd inv
9  Xinv2 en_s2 en_s2b vdd gnd inv
10
11 Xand0 en_s0b en_s1b en_s2b vy0 vdd gnd and3
12 Xand1 en_s0 en_s1b en_s2b vy1 vdd gnd and3
13 Xand2 en_s0b en_s1 en_s2b vy2 vdd gnd and3
14 Xand3 en_s0 en_s1 en_s2b vy3 vdd gnd and3
15 Xand4 en_s0b en_s1b en_s2 vy4 vdd gnd and3
16 Xand5 en_s0 en_s1b en_s2 vy5 vdd gnd and3
17 Xand6 en_s0b en_s1 en_s2 vy6 vdd gnd and3
18 Xand7 en_s0 en_s1 en_s2 vy7 vdd gnd and3
19
20
21 $ voltage source and other setting
22 vdd vdd gnd DC 1V
23 $ven_s0 en_s0 gnd pulse( 0 1 2n 0.5n 0.5n 1n 4n)
24 $ven_s1 en_s1 gnd pulse( 0 1 3.5n 0.5n 0.5n 3.5n 8n)
25 $ven_s2 en_s2 gnd pulse( 0 1 7.5n 0.5n 0.5n 30n 30n)
26 ven_s0 en_s0 gnd pulse( 0 1 10.5n 0.5n 0.5n 9n 20n)
27 ven_s1 en_s1 gnd pulse( 0 1 20n 0.5n 0.5n 19n 40n)
28 ven_s2 en_s2 gnd pulse( 0 1 39.5n 0.5n 0.5n 39n 80n)
29 $va va gnd dc 0v
30 $vb vb gnd dc 0.5v
31 $vc vc gnd dc 1v
32
33 $ 3 to 1 AND gate
34 .subckt and3 ain bin cin out vdd gnd
35 Mpa net1 ain vdd vdd pmos W=2.5u L=0.065u
36 Mpb net2 bin net1 vdd pmos W=2.5u L=0.065u
37 Mpc out cin net2 vdd pmos W=2.5u L=0.065u
38
39 Mna out ain gnd gnd nmos W=1u L=0.065u
40 Mnb out bin gnd gnd nmos W=1u L=0.065u
41 Mnc out cin gnd gnd nmos W=1u L=0.065u
42 .ends
43
44 $ inverter module
45 .subckt inv in out vdd GND
46 Mpl out in vdd vdd pmos w=2.5u l=0.065u
47 Mnl out in GND GND nmos w= 1u l=0.065u
48 .ends

```



```
50 $ transmission gate module
51 .subckt tran_gate in out en_p en_n vdd gnd
52     Mp out en_p in vdd pmos W=2.5u L=0.065u
53     Mn in en_n out gnd nmos W= 1u L=0.065u
54
55     Xinv en en_b vdd gnd inv
56 .ends
57
58 .tran 0.1ns 90ns
59 .option post
60
61 .probe v0(vy0)
62 .probe v1(vy1)
63 .probe v2(vy2)
64 .probe v3(vy3)
65 .probe v4(vy4)
66 .probe v5(vy5)
67 .probe v6(vy6)
68 .probe v7(vy7)
69 .end
70
71 **end**
```