Memory Circuit Design Homeword #2

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1. Functionality of the Basic Gate
2. NAND

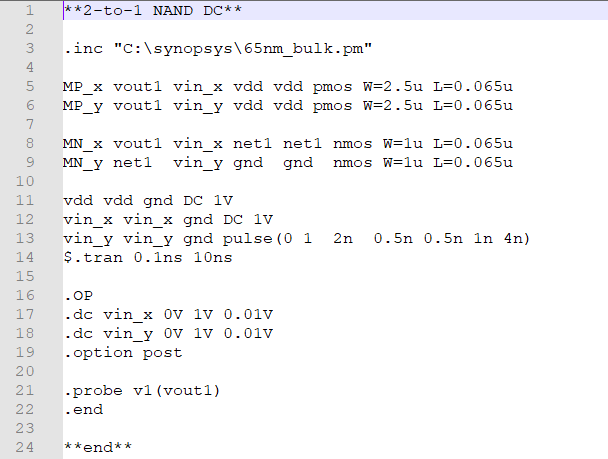
Ac:

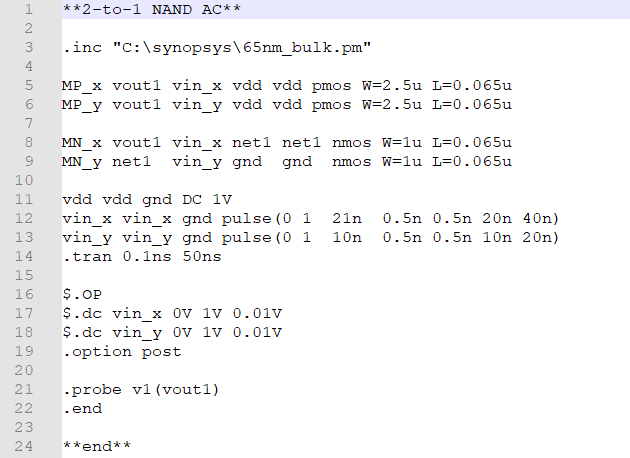


|  |  |  |
| --- | --- | --- |
| A | B | F |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Dc:







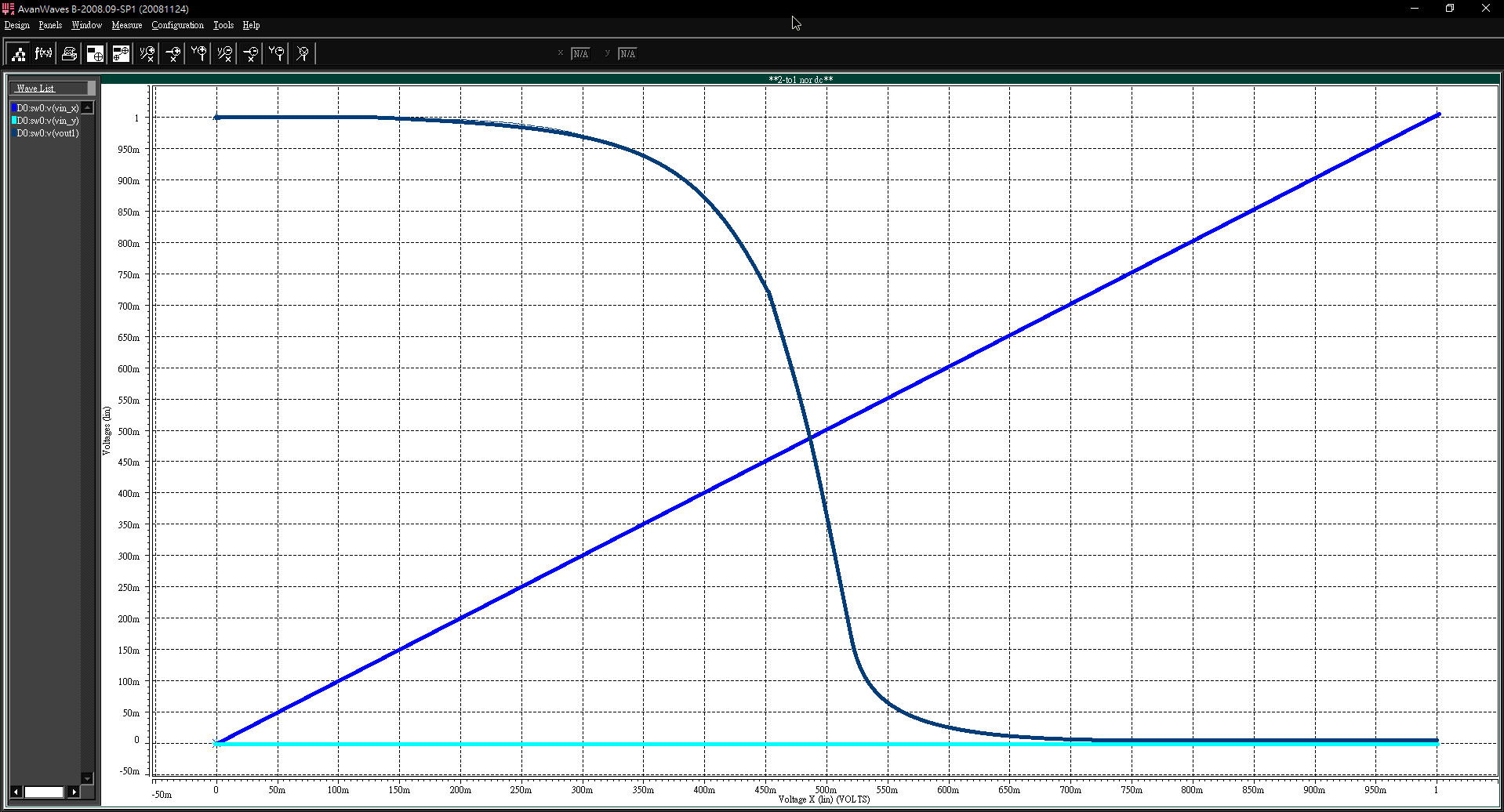
1. NOR

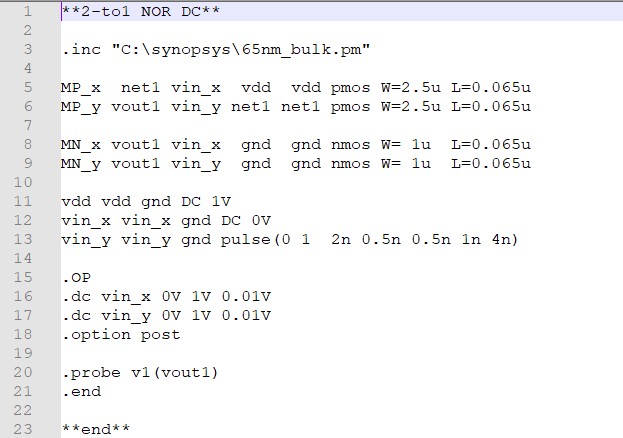
Ac:

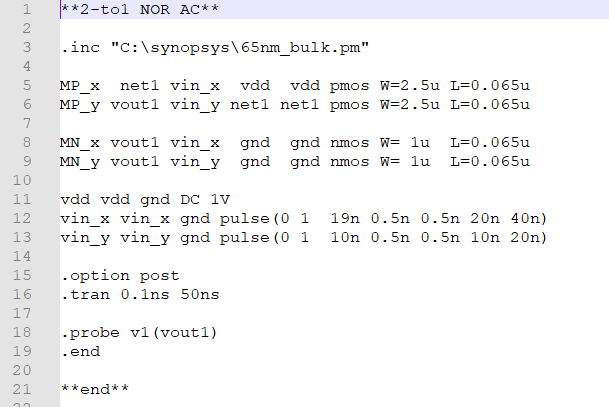


|  |  |  |
| --- | --- | --- |
| A | B | F |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Dc:

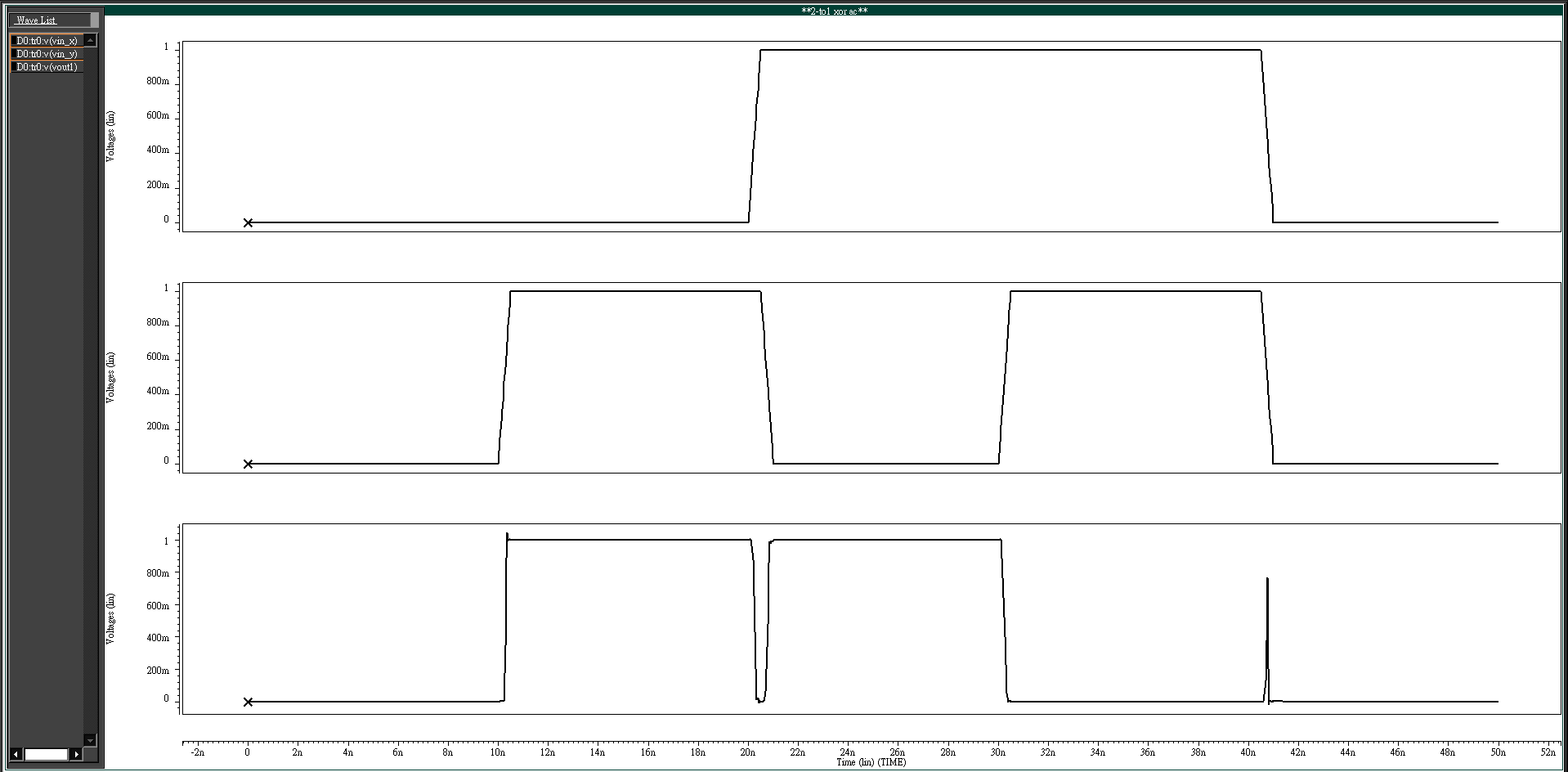






1. XOR

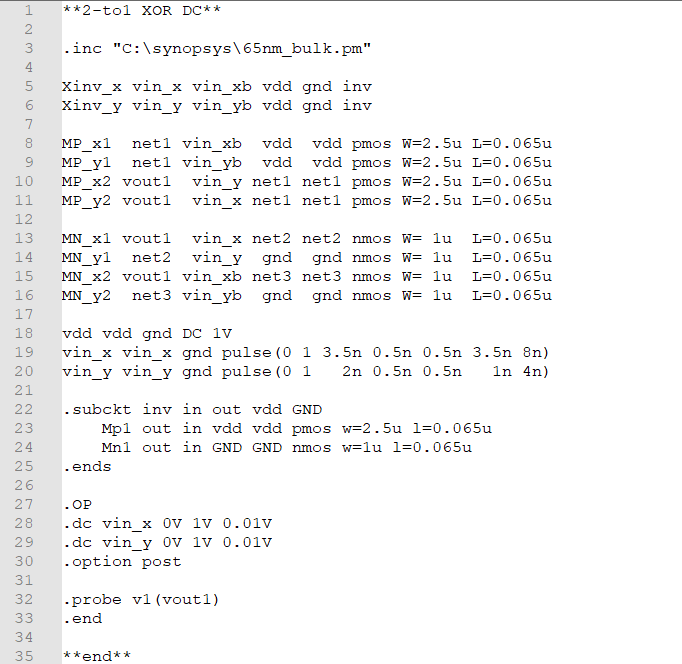
Ac:

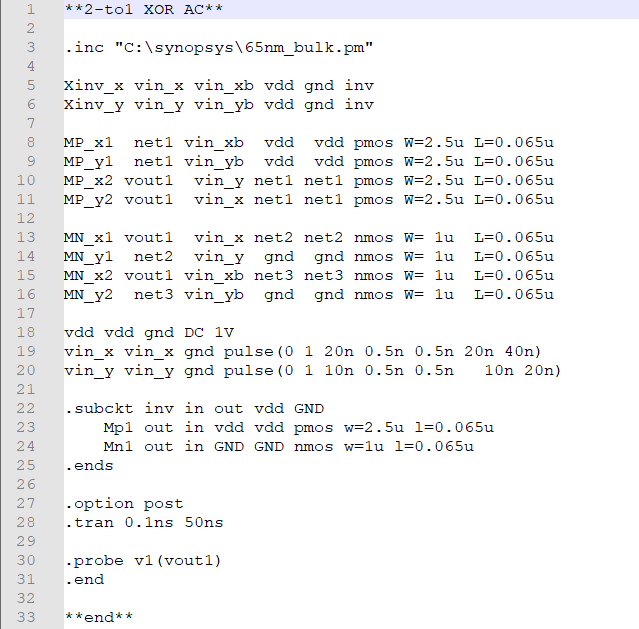


|  |  |  |
| --- | --- | --- |
| A | B | F |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Dc:

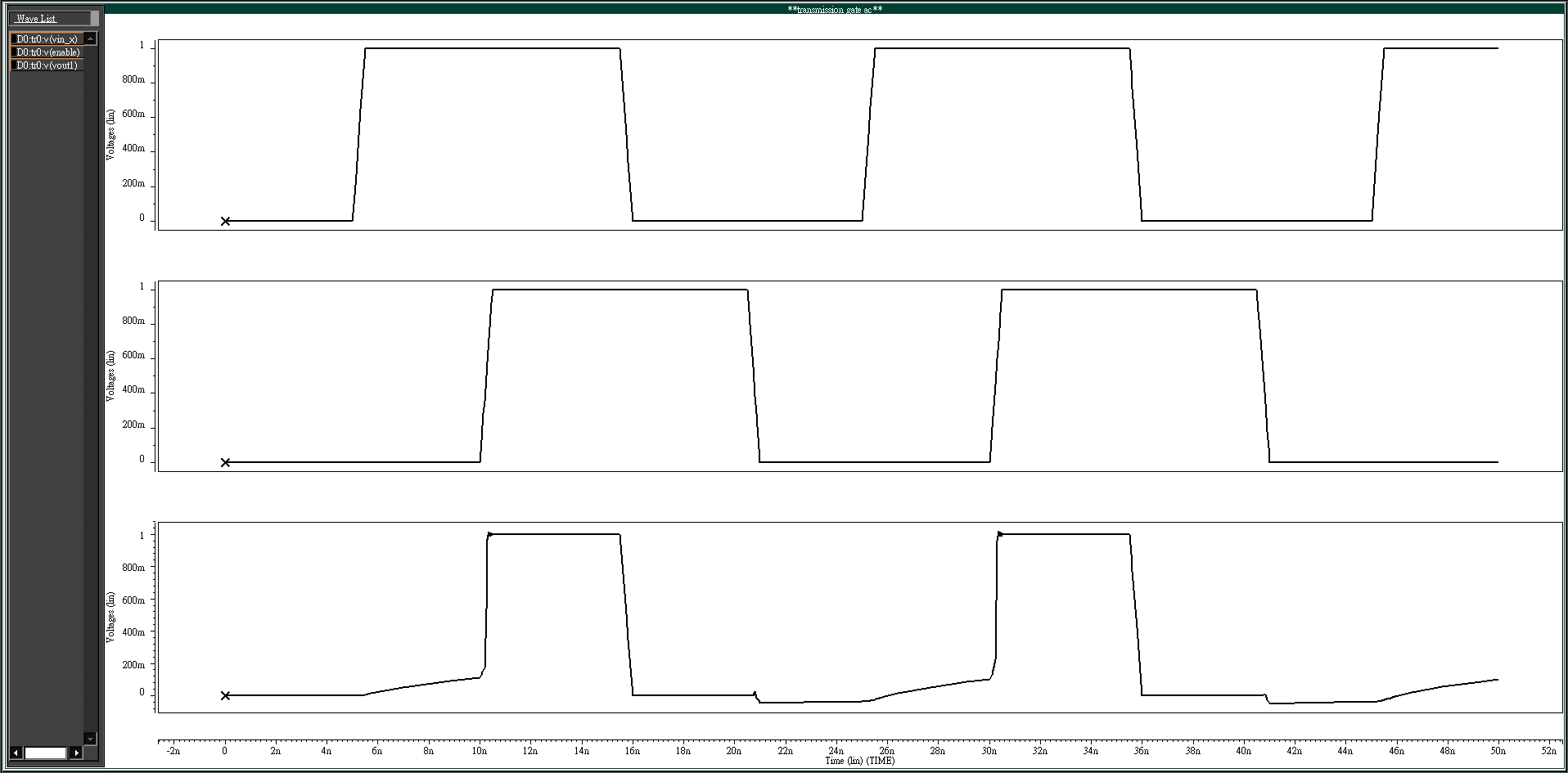






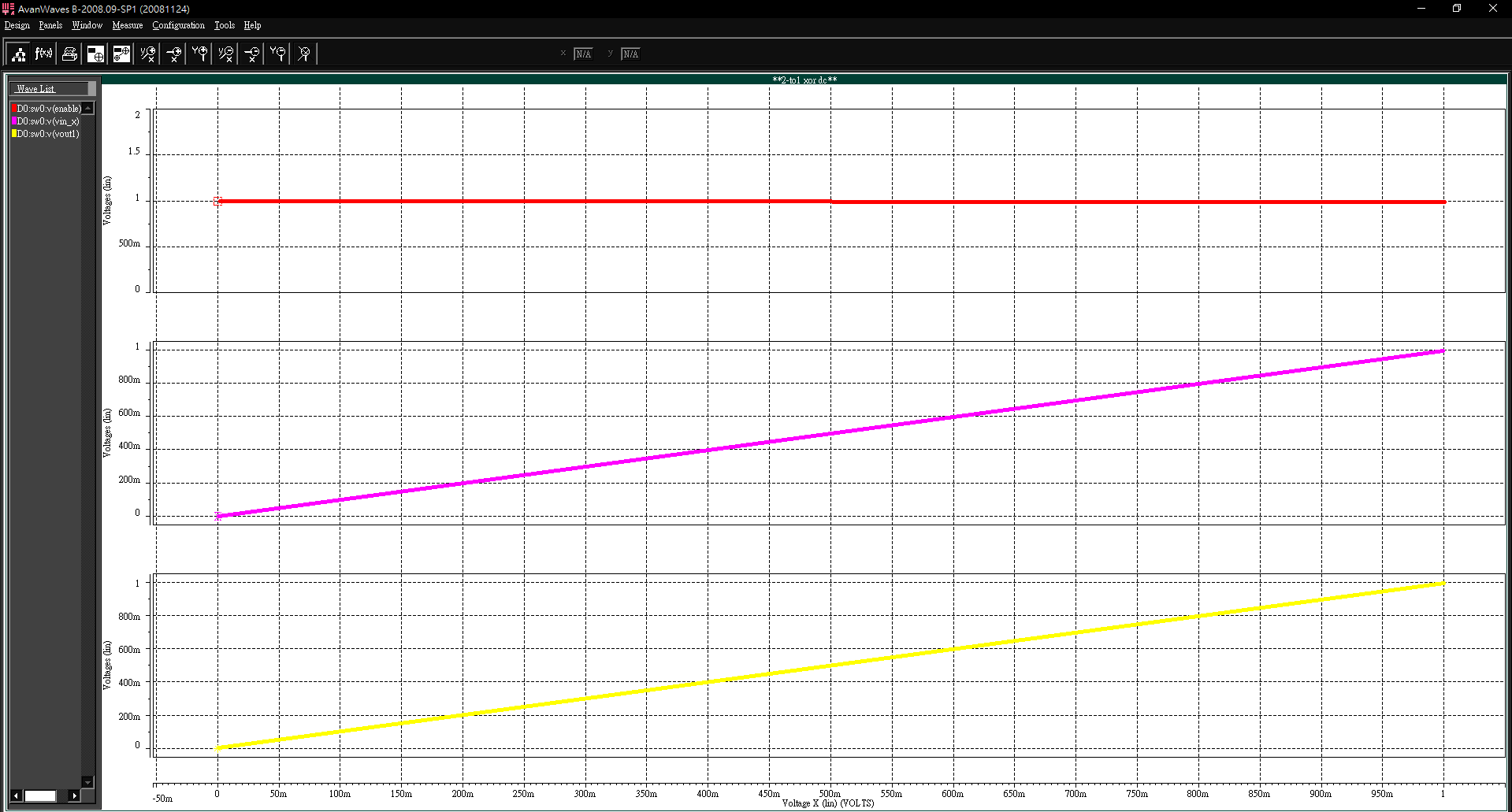
1. Functionality of the Transmission Gate

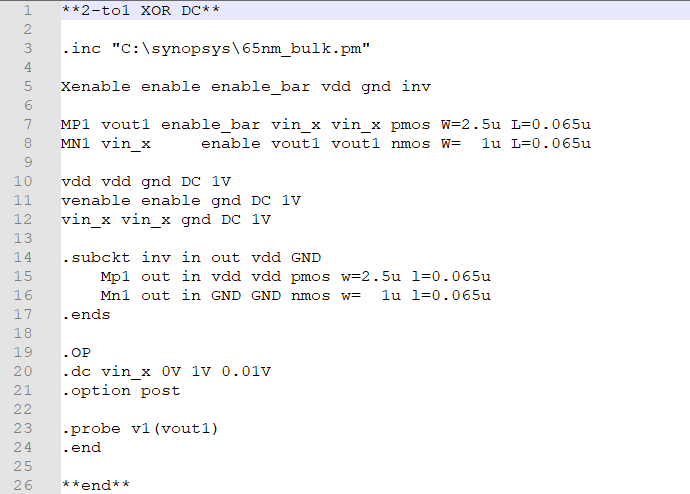
Ac:

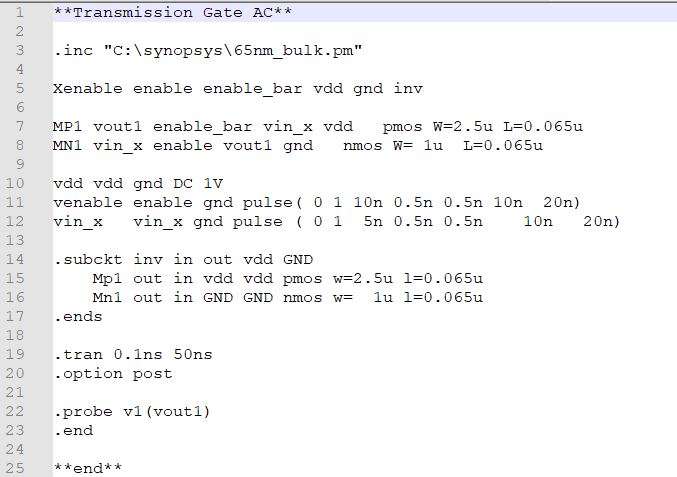


|  |  |
| --- | --- |
| Enable | Out |
| 1 | Xin |
| 0 | out |

Dc:

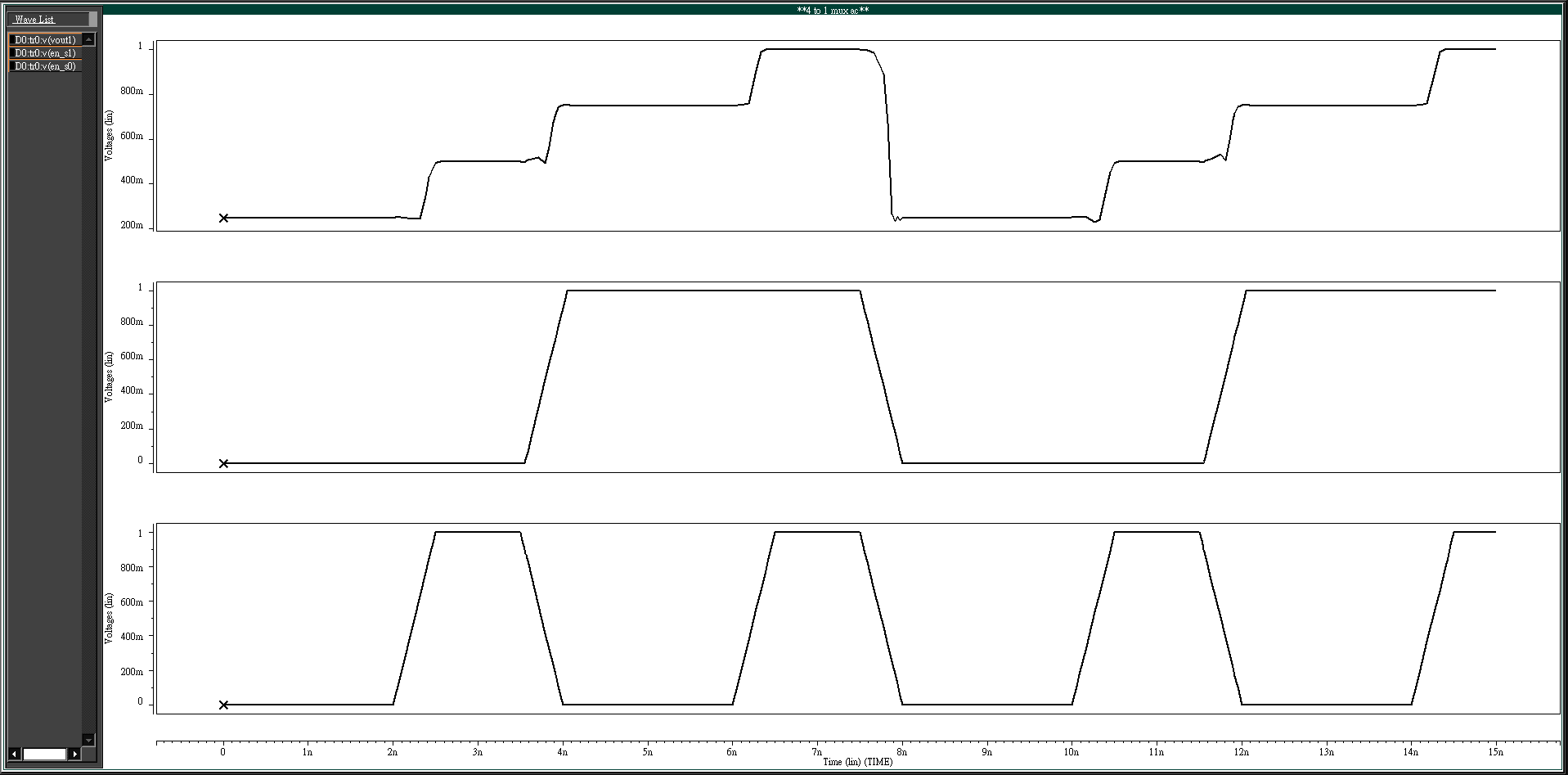




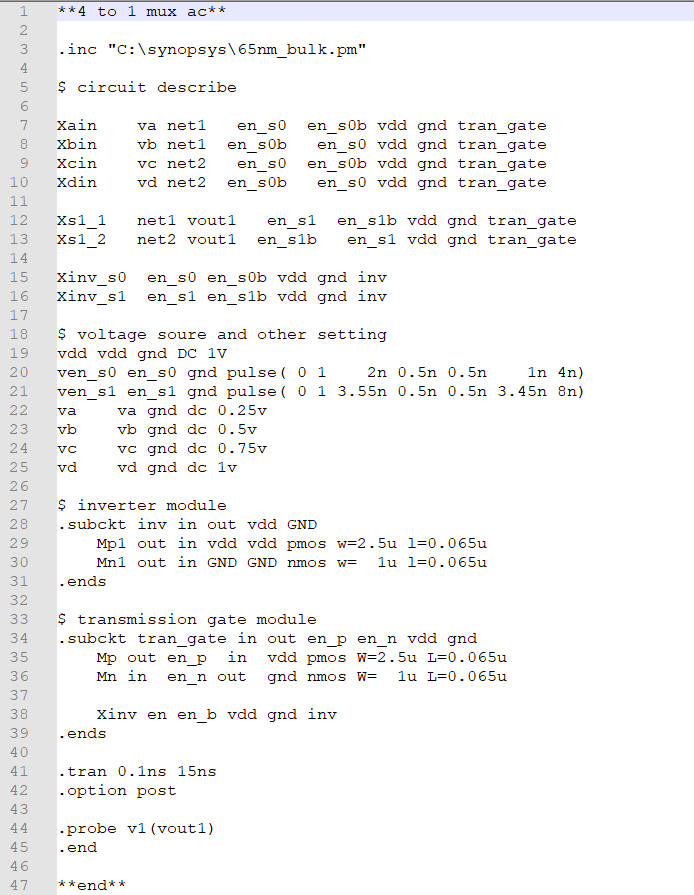


1. Functionality of the Basic Gate (4-to-1 Mux)

Ac:

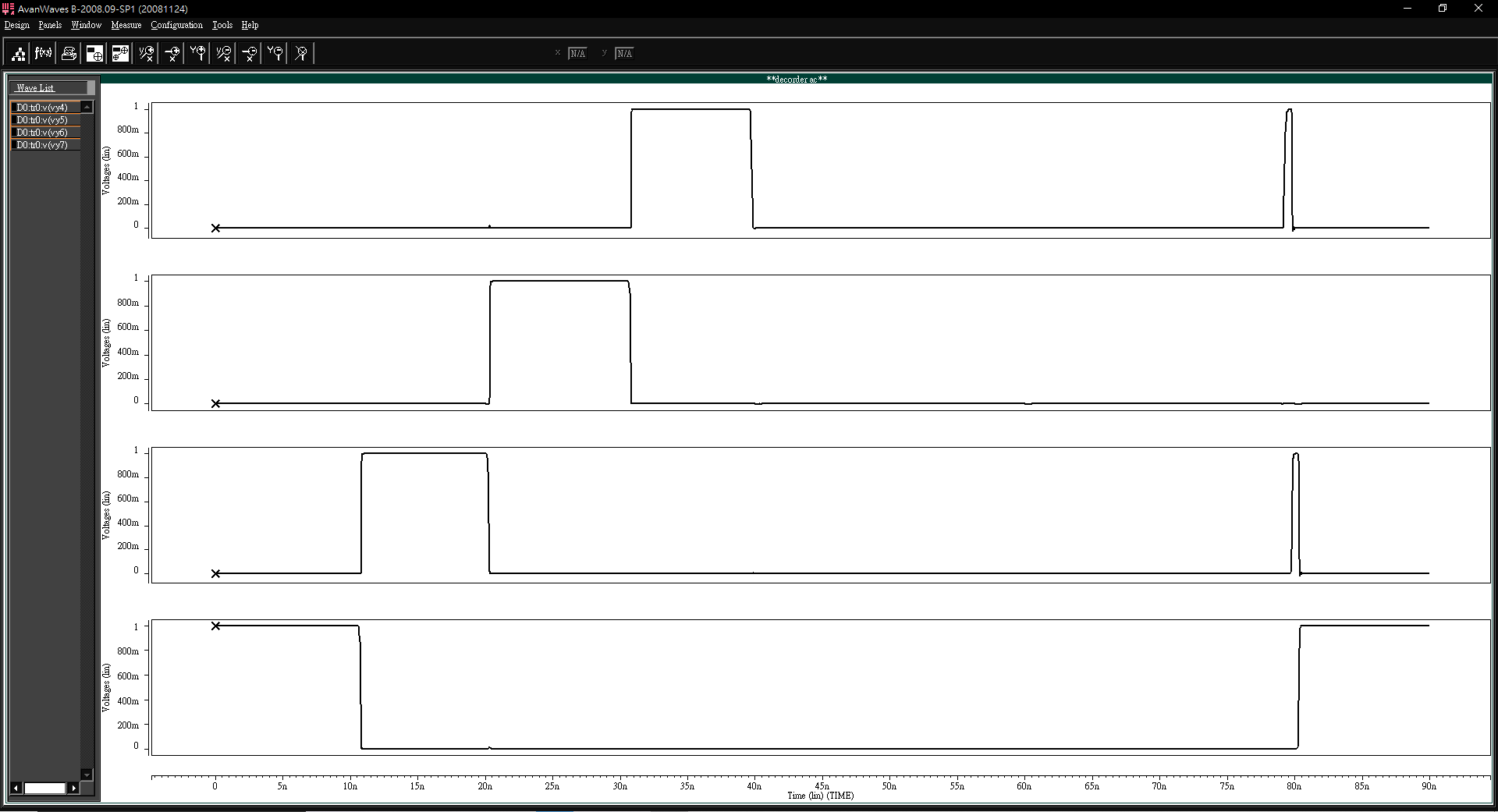
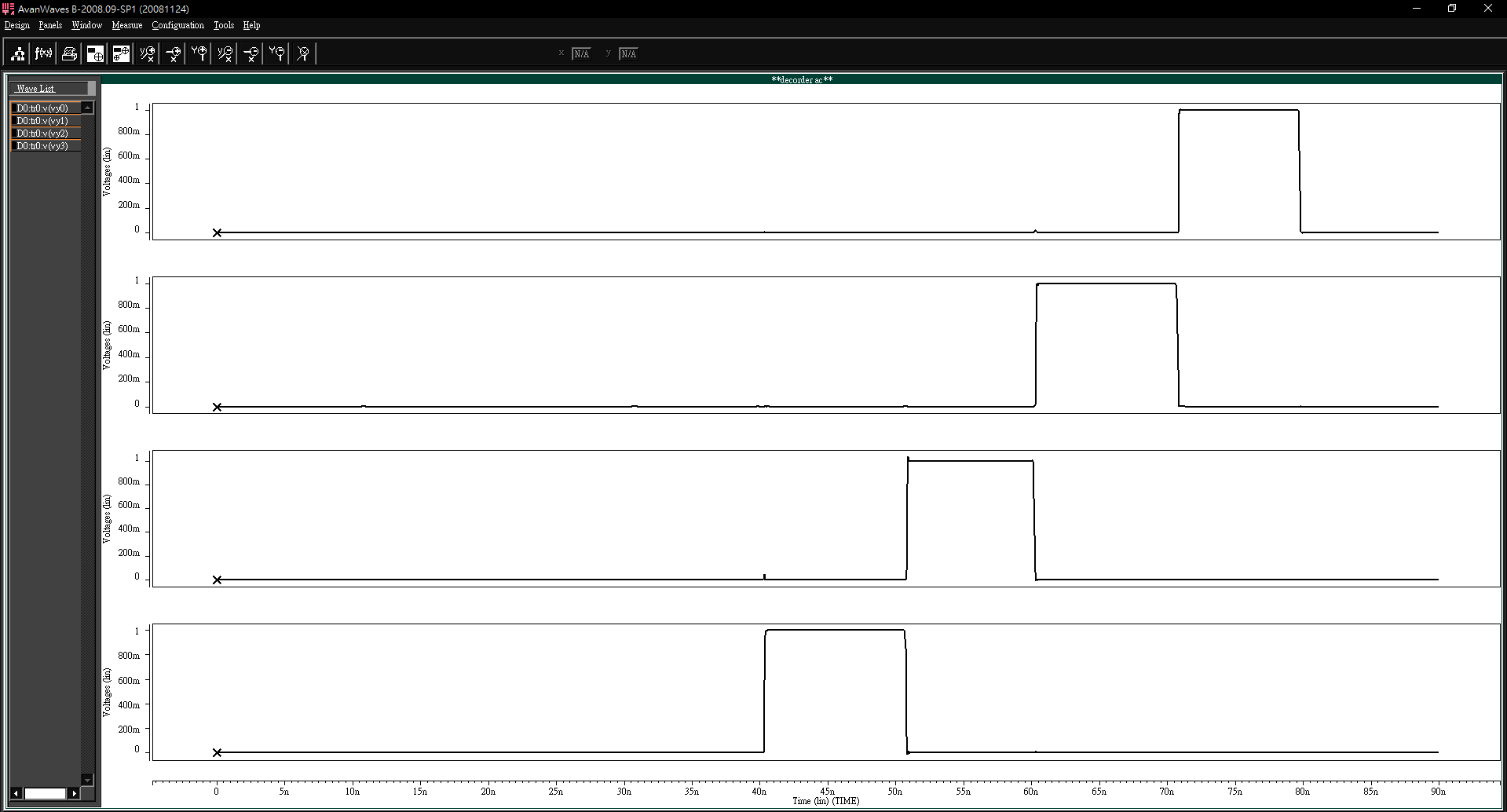
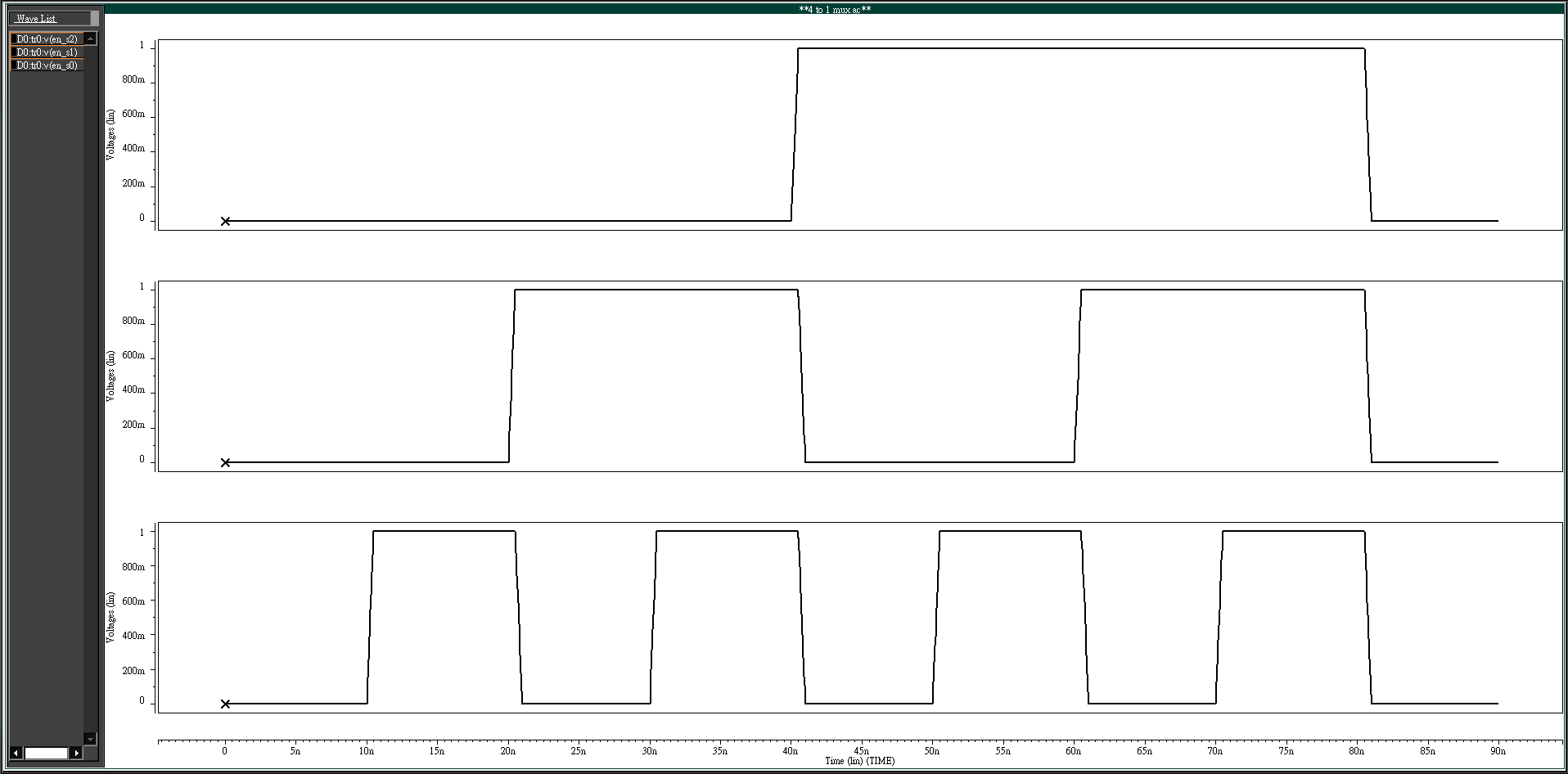


|  |  |  |
| --- | --- | --- |
| S1 | S0 | F |
| 0 | 0 | 0.25v |
| 0 | 1 | 0.5V |
| 1 | 0 | 0.75V |
| 1 | 1 | 1V |



1. Functionality of the Decoder (3-to-8 decoder)

Ac:



|  |  |  |  |
| --- | --- | --- | --- |
| S2 | S1 | S0 | F |
| 0 | 0 | 0 | Out1 |
| 0 | 0 | 1 | Out2 |
| 0 | 1 | 0 | Out3 |
| 0 | 1 | 1 | Out4 |
| 1 | 0 | 0 | Out5 |
| 1 | 0 | 1 | Out6 |
| 1 | 1 | 0 | Out7 |
| 1 | 1 | 1 | Out8 |

