Exam 29 November 2016, questions

Introduction To Electronics (Indian Institute of Technology Kanpur)

End-Semester Examination **Duration: 16:00 – 19:00 (3 hours)**
Nov. 17, 2014 **Max. Marks: 70**

Instructions: *Answer all **Ten** questions. There are **Seven** pages in this Question paper printed back to back.* ***Mention your Section number on your answer sheet***

1) **(a) Fig. 1(a),** shows current voltage characteristics of a two terminal device. There are five distinct regions of operation for this device. Determine the equivalent circuit for each one of these regions in terms of common circuit elements like resistors, voltage, current sources etc. [2]

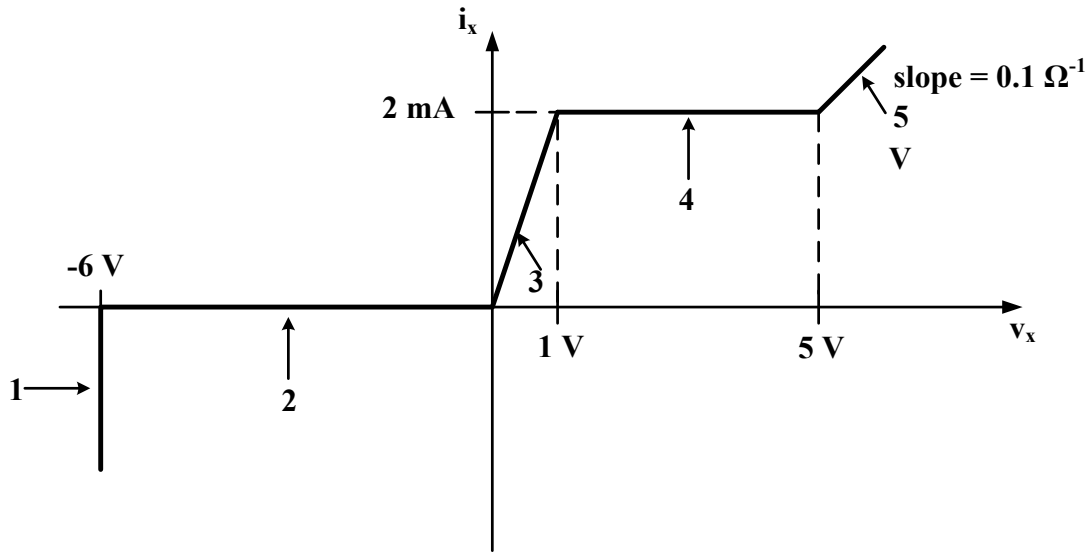


Fig. 1(a)

(b) In **Fig. 1(b)**, Find output voltage V_0 via (i) Superposition Theorem, and (ii) Nodal Analysis. [5]

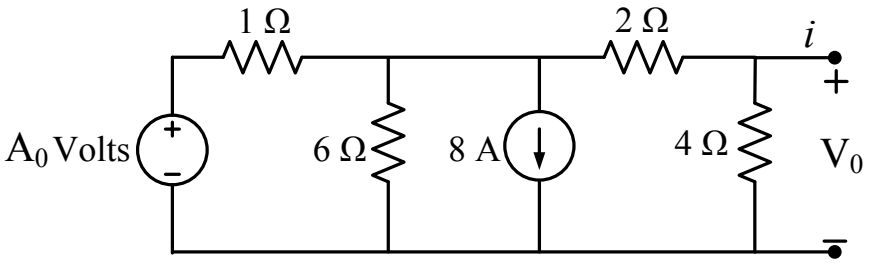


Fig. 1(b)

2) **(a)** In **Fig. 2(a)**, the switch S was at position A for a long time, and changes its position from A to B at time t = 0. Sketch and label $i_L(t)$, and determine the time instant at which it becomes equal to 5A. [4]

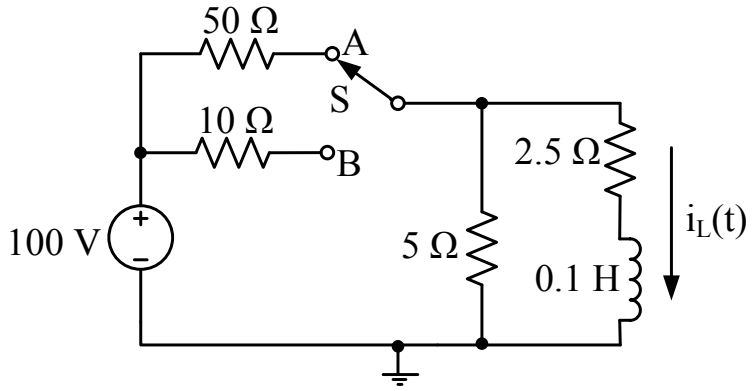


Fig. 2(a)

(b) The Bode magnitude plot of the transfer function $H(j\omega)$ is shown in **Fig. 2(b)**. $H(j\omega)$ consists of three asymptotes I, II and III as indicated in **Fig. 2(b)**. Determine the descriptions of each individual asymptote. Also identify and determine the description of the overall transfer function $H(j\omega)$. [4]

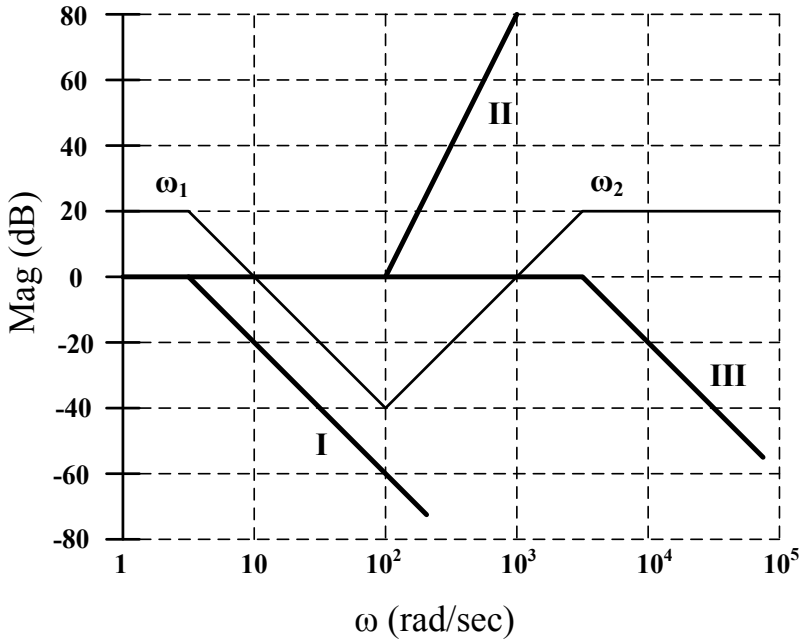


Fig. 2(b)

3) The circuit in **Fig. 3(a),** has the magnitude-frequency curve as shown in **Fig. 3(b)** (linear coordinates). The input voltage is

$$v_s(t) = V_s \cos(\omega t)$$

and

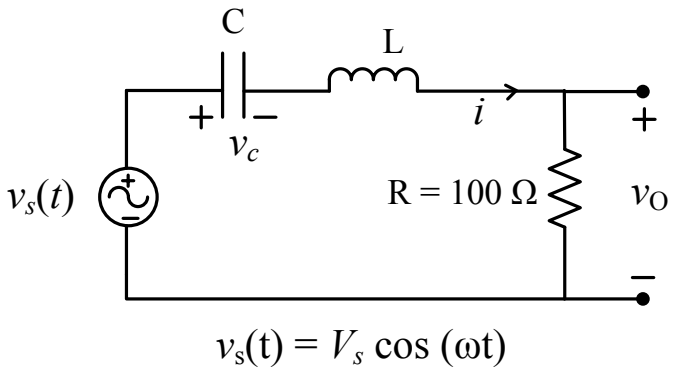
$$\omega_c = 1 \times 10^6 \ rad/s$$
$$\omega^+ = 1.05 \times 10^6 \ rad/s$$
$$\omega^- = 0.95 \times 10^6 \ rad/s$$

(a) Find the values of L and C.

(b) Sketch the $\angle V_0$ vs. ω.

(c) If $v_s = 10 \cos(10^6 t)$, calculate $v_c(t)$, $i(t)$, and $v_O(t)$.

(d) For $v_s = 10 \cos(10^6 t)$, Determine the total stored energy W_s and time-averaged power dissipated. [7]



$v_s(t) = V_s \cos(\omega t)$

Fig. 3(a)

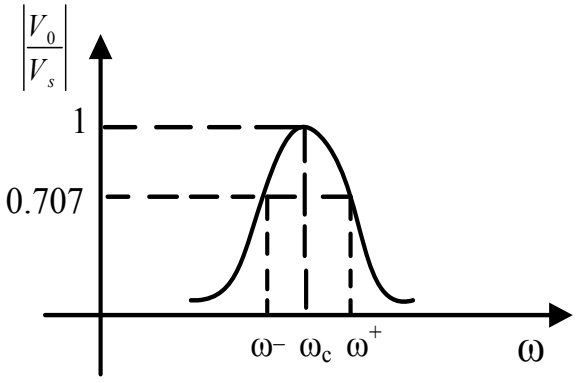


Fig. 3(b)

4) Sketch I_R and V_0 for the network of **Fig. 4** for the input shown. Assume $V_\gamma = 0.7$ V and resistance of the diode under conduction is zero. [7]

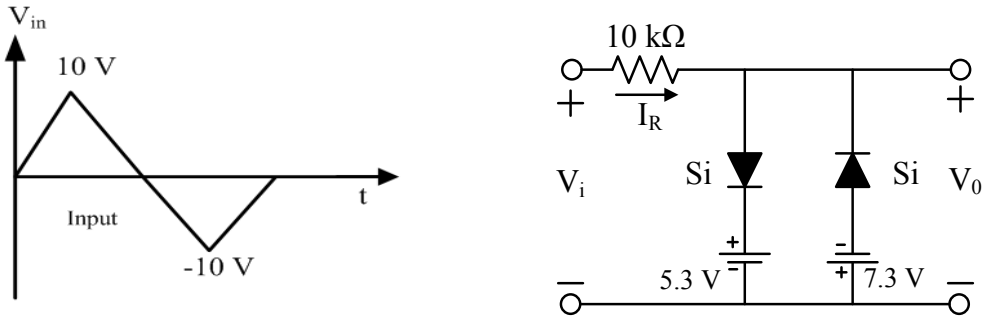


Fig. 4

5) **(a)** In the circuit shown in **Fig. 5(a),** determine the mode of operation of the transistor, the collector current I_C and the voltage at the emitter V_E. Assume that $V_{BE} = 0.7$ V both in active and saturation modes and $V_{CE,sat} = 0.2$ V. [3]

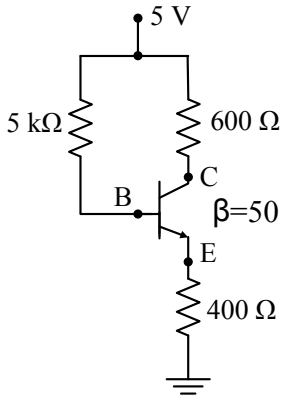


Fig. 5(a)

(b) Find the value of I_C shown in the **Fig. 5(b)** considering the transistor to be in the active mode. Given $R_1 = 20$ kΩ and $R_2 = 5$ kΩ. Assume $V_{BE} = 0.7$ V. [3]

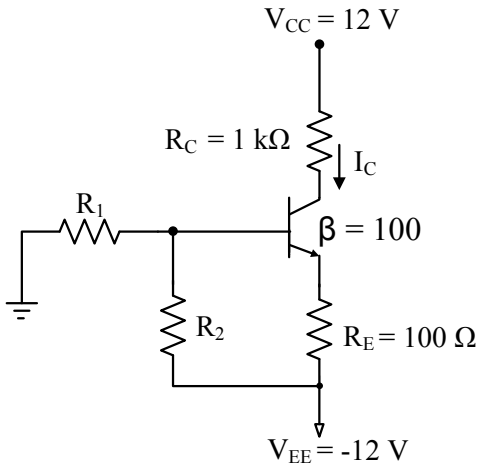


Fig. 5(b)

6) Determine V_{in} versus V_0 transfer characteristics of the ideal op-amp circuit shown in **Fig. 6.** It is given that $R_1 = R_2 = R_3 = 1$ kΩ, $V_{CC} = 12$ V and $V_{sat} = \pm 11$ V. Clearly show the output voltages, arrows and the trip points (values of the input signal at which the output state changes) on the V_{in} axis (X-axis). [7]

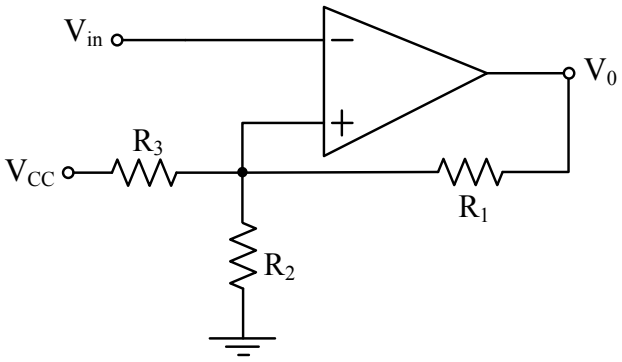


Fig. 6

7) **(a)** For the circuit in **Fig. 7(a)**, use superposition to find V_0 in terms of the input voltages V_1 and V_2. Assume an ideal op amp. Given

$V_1 = 10\sin(120\pi t) - 0.1\sin(2000\pi t), \quad volts$

$V_2 = 10\sin(120\pi t) + 0.1\sin(2000\pi t), \quad volts$

Find $\mathbf{V_0}$. [2]

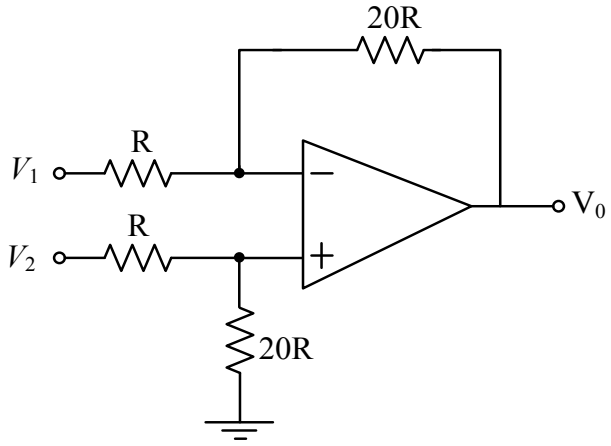


Fig. 7(a)

(b) Consider the instrumentation amplifier of **Fig. 7(b)**, with a common-mode input voltage +3 V (dc) and a differential input signal of 80 mV peak sine wave. Let $2R_1$ = 1 kΩ, R_2 = 50 kΩ, R_3 = R_4 =10 kΩ. Find voltage at nodes **A, B, C, D** in the circuit. Also find the output voltage $\mathbf{V_0}$. [5]

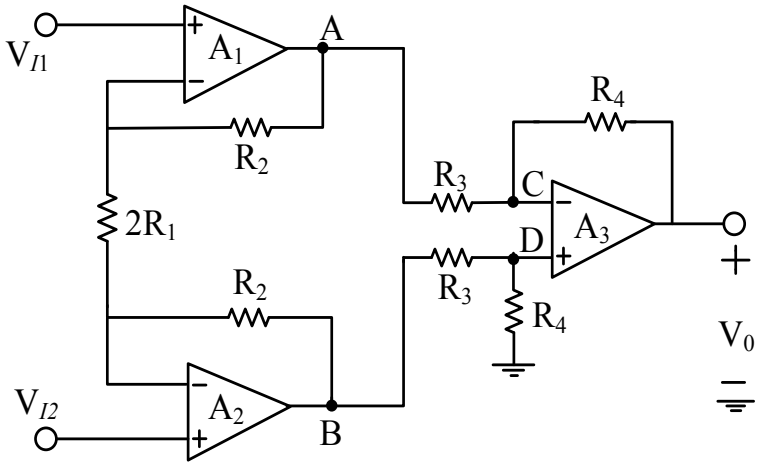


Fig. 7(b)

8) **(a)** Using K-map, express the following function both in minimized SOP and POS representations:

F(A,B,C,D) = $\sum_m(1,3,5,7,9,15) + \sum_X(4,6,12,13)$

where 'm' denotes minterms, and 'X' denotes 'don't care' condition. Implement the SOP representation using NAND Gates and the POS representation using NOR Gates. [4]

(b) A function F is defined such that it equals 1 when a 4-bit input code is equivalent to any of the decimal numbers 3, 6, 9, 12, or 15; equals 0 for input codes 0, 2, 8, and 10; and the other input values cannot occur. Determine a minimal SOP expression for the function F. Design and sketch this circuit, assuming that you have only AND and NOT gates. [3]

9) **(a) Fig. 8(a)** depicts a four input majority circuit module. The output Z of this circuit module is high if a majority of the inputs are high. Write a Boolean expression for Z in terms of A0, A1, A2, and A3. How would you use the four-input majority circuit module shown in **Fig. 8(a)** to implement a three-input majority circuit and a two input majority circuit? If either of these cannot be done, discuss why not. [2]

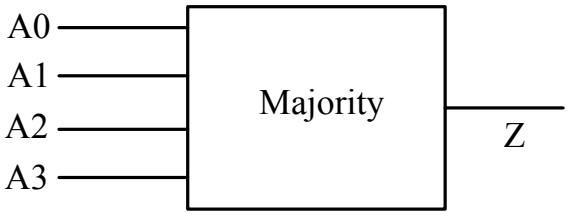


Fig. 8(a)

(b) Give a circuit realization of the combinatorial logic block shown in **Fig. 8(b)** to obtain the following truth table. Use only 2 input gates to realize the circuit. [3]

A	B	Q
0	0	$\bar{Q}_n$
0	1	1
1	0	Q_n
1	1	0

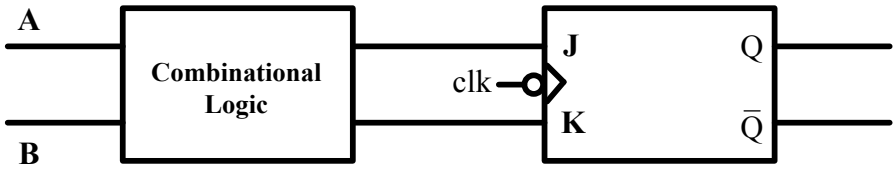


Fig. 8(b)

10) Design a synchronous counter using J-K flip flop that counts the following 5- state binary sequence : **4, 1, 3, 7, 6,** 4, 1, 3, **……** [9]