Nov. 19, 2019 **ESc201A** **End-Semester Examination** **Time: 09:00-12:00Hrs.**

Closed Book, Notes, & Mobiles. ***Put your Name, Roll No. & Section on all attached sheets. There are Eight questions for a total of 70 marks. Credit for each question is indicated on the left-hand margin. Show all necessary calculations. Best wishes for an excellent performance.***

1. The RC coupled amplifier of fig. 1 is biased to operate in the forward active region. Assume C_{in} and C_{out} to be very large.

[2] (a) Find the collector bias current (I_C) for $\beta_F = 89$.

[3] (b) Calculate the Mid-band Voltage Gain ($A_{v_1} = v_{o1}/v_i$).

[4] (c) If $C_E = 10\mu f$, the base-emitter junction capacitance $C_\pi = 50pf$, and the Base-collector capacitance $C_\mu = 5pf$, estimate the high and the low 3dB cutoff frequencies.

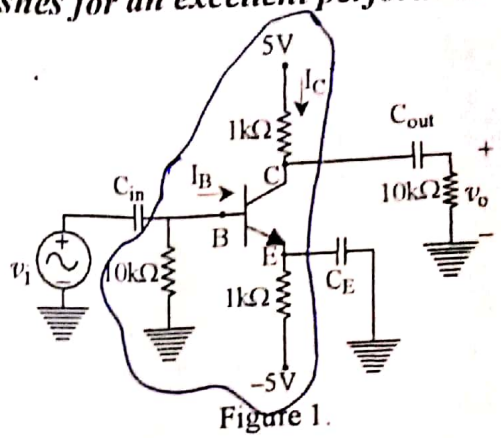

Figure 1.

2. For the circuit shown in fig. 2, assume that all the diodes have $V_{on}=0$ and the OpAmp to be ideal. Assume C_{in} to be very large. The circuit has been sitting idle for a long time and a 5V pulse appears at the input only at $t=0^+$. (*Remember that the voltage across a capacitor cannot change instantaneously*)

[2] (a) What are the voltages v_+ (at non-inverting input of OpAmp) and v_o (output) at $t = 0^-$?

[3] (b) At $t=0^+$, a 5V, 0.1ms pulse appears at the input. Find the output voltage v_o at $t = 0^+$.

[4] (c) If R=4kΩ and C=2μF, calculate the time for which the output voltage holds at the result found in (b) above.

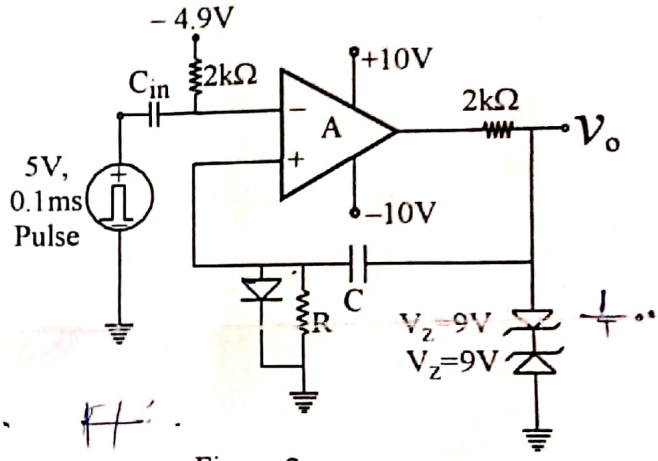

Figure 2.

3. The circuit shown in fig. 3 is supposed to oscillate sinusoidally at a frequency of 100 kHz.

[3] (a) Derive an expression for the closed loop gain $A_v\beta$ for the ideal OpAmp, where A_v is the non-inverting voltage gain and β is the positive feedback fraction (v_+/v_o).

[3] (b) If the given capacitance C=318.3pF, find the required value of R. Derive any expression that you need to use for the calculation

[3] (c) For stable oscillation, find the required value of R_f.

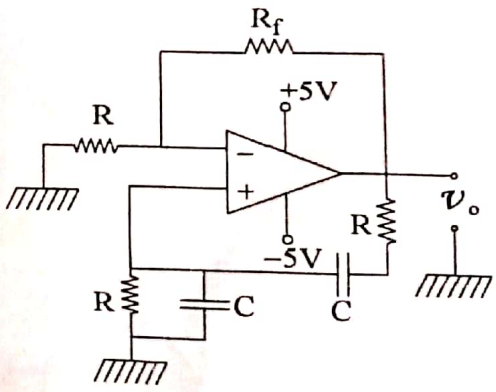

Figure 3.

[4] **4(a)** A 4-bit digital input (W{MSB}, X, Y, and Z{LSB}) has voltage levels +5V as '1' and 0V as '0', respectively. Construct and sketch a Digital-to-Analog Converter (DAC) using an ideal OpAmp, powered by a +5V supply and the other supply input grounded. You may use resistances R, 2R, 4R, ..., etc. along with the OpAmp. Derive an expression for the analog output voltage (v_o) as a function of the digital inputs. What is the quantization error (%) in the conversion?

ANSWERSCRIPTS WILL BE SHOWN at 11:15-12:15 AM on Nov. 23, 2019 (Saturday) in your respective Tutorial Rooms, EXCEPT for Section W2 which will be in Rm. T207 instead of T112.

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[4] **4(b)** F is a Boolean function of the Boolean variables A,B,C,D, & E, as shown in fig. 4(b). Find the Boolean expression of F(A,B,C,D,E) in its minimum Sum of Products (SOP) form. X is the enable input set at 1.

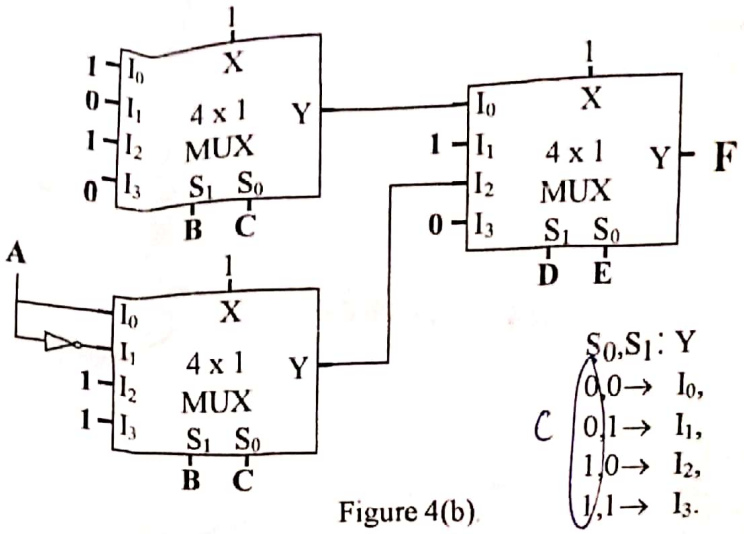


Figure 4(b)

5. Two numbers 85.125 and 32.5 are stored in 10-bit (7+3) binary registers with the 3 bits after the decimal point.

[3.5] (a) Show the two registers with the two binary numbers equivalent to 85.125 and 32.5.

[3.5] (b) Show the process of subtraction of the smaller number from that of the larger (show how smaller decided) using 2'-compliment method.

[2] (c) Using any extra number of 10-bit registers required, show the implementation of obtaining the 2'-compliment from the required register in (a), using gates and full-adders.

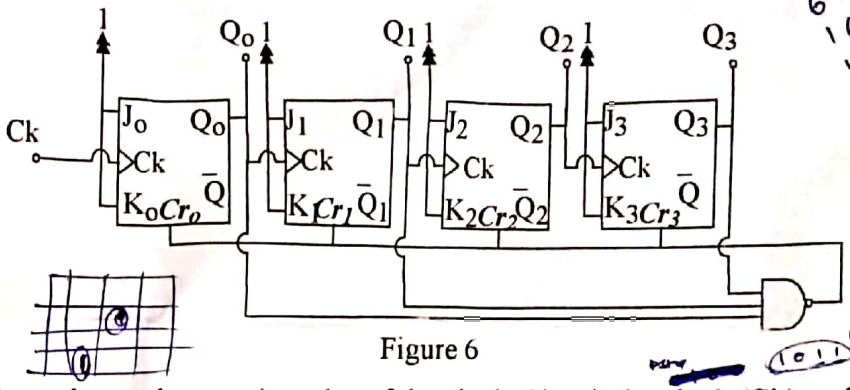
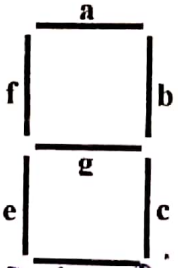


Figure 6

[8] **6.** A Ripple counter, shown in fig. 6, works on the negative edge of the clock. Sketch the clock (Ck) and the Q_0, Q_1, Q_2, Q_3, output pulses on the same time scale and hence write the sequence of states of the counter. The *Clear*(***Cr***)=0 sets a Flip-Flop to Q=0, $\bar{Q}$=1 state for *Preset*(P_r)=1(assumed here to be always set at this value). *Cr*=1 has no effect for P_r=1. If this counter, has a count of N, what is N ?

7. A Binary Coded Decimal (BCD) {**A**(MSB), **B**, **C**, and **D**(LSB)}input is to be displayed on the seven-segment display, shown in fig. 7. However, when the numbers **0**, **3**, **7**, **8**, and **9** appear, then only the number is to be displayed. For the other numbers, an inverted-C { ⊐ (a, b, c, and d to be illuminated)} is to be displayed.



[9] Establish the **combinational logic** and logical voltages (1 or 0) that are required to be connected to the segments **a**, **b**, **c**, **d**, **e**, **f**, and **g**, such that the above mentioned constrained-display can be realized with **a minimum number of gates**. *No Circuit Diagram is needed.*

8. A modulo-6 synchronous counter is to be designed with J-K flip-flops. The counter should start at 000.

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

[6] (a) From the J-K flip-flop truth table given on the right develop and sketch a clean circuit for the same with minimum number of J-K flip-flops and other gates.

[3] (b) This counter is to be converted to a **modulo-12 counter** using one extra T-Flip-Flop to this modulo-6 counter. Show the modification of this circuit required. The truth table for the T-Flip-Flop is obtained from the J-K truth table using J=K=1.

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