

End Semester Examination

Duration: 3 hrs

Date: 12.07.2016

Please confirm there are 5 pages in this question booklet (including the cover page).

- Maximum time : 3 hours
- There are **SIX** questions in this booklet.
- Marks are indicated against each question.
- This is a closed book examination, but you are allowed to use your own calculator.
- Draw the circuit whenever it will help you to solve the problem or explain the concept.
- Simplify the results analytically as far as possible before plugging in the values.
- No consultation is allowed among fellow students during the exam.

1 (a). The load resistance  $R_L$  in Fig. 1(a) is adjusted until it absorbs the maximum average power. Calculate the value of  $R_L$  and the maximum average power dissipated across the load  $R_L$ . [5]

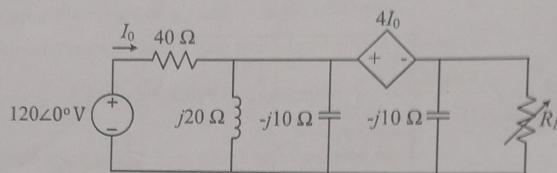


Fig. 1(a)

1 (b). For the circuit in Fig. 1(b), find the resonant frequency  $\omega_0$ .

[5]

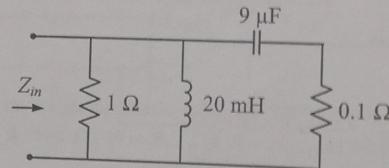


Fig. 1(b)

2 (a). For the circuit shown in Fig. 2(a), the switch S<sub>1</sub> is closed at  $t = 0$  sec and S<sub>2</sub> is closed at  $t = 4$  sec. Find the expression of current  $i$  for  $t < 4$  sec and  $t \geq 4$  sec. You can assume that the switch S<sub>1</sub> is open for  $t < 0$  and switch S<sub>2</sub> is open for  $t < 4$  sec.

[6]

1

(2)

$$V_{G1} = V_i^o \Rightarrow V_{DD} - \frac{g_{m1}}{g_{m2}} V_{G1} = V_o$$

$$A_v = \frac{V_o}{V_i^o} = \frac{V_{DD} - \frac{g_{m1}}{g_{m2}} V_{G1}}{\frac{V_{G1}}{g_{m1}}} = \frac{V_{DD}}{V_{G1}} - \frac{g_{m1}}{g_{m2}}$$

Department of Electrical Engineering, Indian Institute of Technology, Kanpur  
ESC201A: Introduction to Electronics

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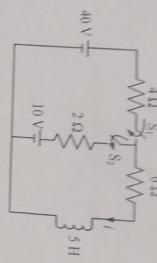


Fig. 2(a)

- 2 (b). For the circuit shown in Fig. 2(b), transistors  $\text{Q}_1$  and  $\text{Q}_2$  operate in the active region with  $I_{\text{AS}} = I_{\text{AS2}} = 0.7 \text{ V}$ ,  $\beta = 100$  and  $\beta_s = 50$ .

- Find the currents  $I_{\text{B1}}$ ,  $I_{\text{C1}}$ ,  $I_{\text{B2}}$ ,  $I_{\text{C2}}$  and  $I_{\text{Ic}}$ .
- Find the voltages  $V_{\text{o1}}$  and  $V_{\text{o2}}$ .

[5]

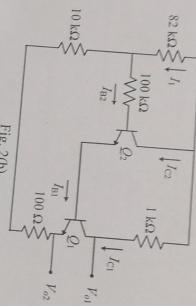
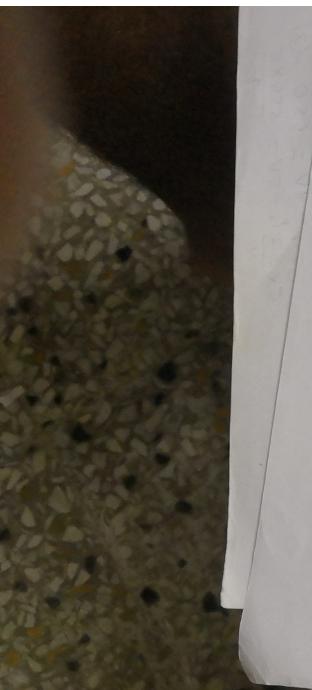


Fig. 2(b)

- 3 (a). A common source MOSFET amplifier circuit is shown in Fig. 3(a). It is given that:  $R_c = R_g = 40 \text{ k}\Omega$ ,  $R_b = 20 \text{ k}\Omega$ ,  $R_s = 12 \text{ k}\Omega$ ,  $R_e = 91 \text{ k}\Omega$  and  $R_{\text{og}} = 100 \Omega$ . The MOSFET parameters are  $V_t = 1 \text{ V}$ ,  $k'_n (W/L) = 1 \text{ mA/V}^2$  and  $V_F = 50 \text{ V}$ .

[8]



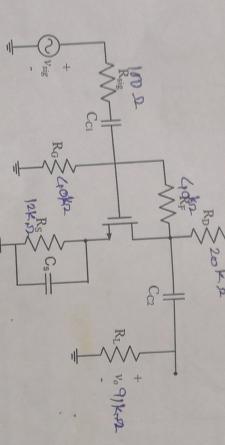


Fig. 3(a)

Show that the MOSFET operates in the saturation region.

- Determine the values of  $g_m$  and  $r_o$  at the bias point.
- Determine the total voltage gain from signal source to load ( $G_V$ ).
- Determine the total current gain from signal source to load ( $G_I$ ).  

$$|I_D| = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_T)^2$$

$$|I_D| = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_T)^2$$

3 (b) For the circuit given in Fig. 3(b), obtain an expression for  $\frac{v_o}{v_i}$ .

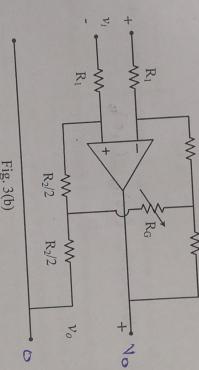


Fig. 3(b)

- 4 (a) A triangular wave is fed to an op-amp circuit as shown in Fig. 4(a). Plot (i) transfer characteristics  $v_o$  vs  $v_i$  and (ii) output voltage  $v_o$  with time. Indicate all the salient points in the graphs. Assume op-amp used in the circuit is ideal and its saturation voltage is  $V_{out} = \pm 16$  V. [6]

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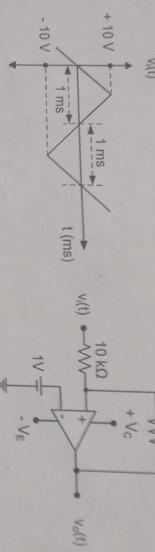


Fig. 4(a)

4 (b). In the circuit given in Fig. 4(b), the Zener diodes  $Z_1$  and  $Z_2$  have breakdown voltages of 6 V and 8 V respectively. Plot transfer characteristic  $V_o$  vs  $V_i$ . Assume op-amp used in the circuit is ideal and its saturation voltage is  $V_{sat} = \pm 12$  V. The cut-in voltage and forward resistance of each diode are 0.7 V and zero ohm respectively.

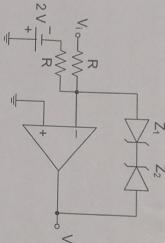


Fig. 4(b)

5 (a). Carry out the following operations using 2's complement arithmetic. Verify the result.  
 i)  $(4F)_{10} - (16)_{10}$ , ii)  ~~$(14)_{10} + (14)_{10}$~~   $(14)_{10} - (14)_{10}$

[2]

5 (b). Draw the logic diagram using only NOR gates to implement the following function:  
 $F(A, B, C, D) = (A \oplus B)'(C \oplus D)$ .

Assume that the complimented inputs are available.

[3]

5 (c) There is a four variable Boolean function, where the 4 variables, can be viewed as the 4 vertices of a tetrahedron, as shown in Fig. 5. The Boolean function takes value 1 when any 3 other two are again equal but different from the first two. Construct the Boolean function. Express it in standard Sum-of-Product (SOP) form and minimize the Boolean function using K-maps.

[7]



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