Supplier:	Robert Bosch GmbH
Name:	SMI720
Data Sheet::	1.2
Date of issue:	21.05.2015

Req_1

SMI720 Internal Data Sheet (Robert Bosch GmbH, Reutlingen, Germany)

Type:	SMI720
Part Number:	0 273 142 040

Owner	Revision	Date
AE/ESI3-Wang; AE/ESI1-Weidig		Wednesday, June 10, 2015

	AE/ESI	AE/ESE	CC-PS/EPY
Date:	26.05.2015	26.05.2015	27.05.2015
Signature:	Ullmann	Bischopink	Du

Req_2265

Change Documentation

Baseline	ID	Change
1.0		Initial Version
1.1	1	Pflichtenheft -> Internal Data Sheet
	2265	Change documentation included
	various	ISO26262 flagging included (column ISO26262, 'S=Safety Relevant')
1.2	2109 ff.	Information about internal latching of flags added.
ÄS: 1039R06715	981 / 2182	Recommendation to check ASIC-name of SMI720 during initialization.
	2267	ACC output in Earth's gravitational field added
	241	Correction of ADR(4:0) range in MOSI frame (including Bit22)
	2097	General description corrected with max/min values for digital I/O pins
	2228	Sensitivity of quadrature channel corrected
	1125	Included application circuit without C_VDD_IO (part of CR017)
	933 / 2269	Condition modified due to CR017 (voltage drop over series R of PSRR filter)
	205	Changed ball diameter BGA according to CR027
	1125/2080	Modification of CPUMP pin description because of CR028.
	208	Bromine level of <50 ppm included.
	342, 373	Measurement of hysteresis w/o slow offset cancelation.
	2099 ff.	Update of Reset-Levels according c-samples.
	2272/1004	Values for “damping slope” for ACC and ARS signal path added.
	1125/1159	A minimum C_VDD3 is necessary to prevent bouncing of VDD3 during startup.
	2076	Update of VDD1_8 pin specification.
	334 ff.	Update of t.b.d. parameters of ACC-channel according c-sample characterization.
	364 ff.	Update of t.b.d. parameters of ARS-channel according c-sample characterization.
	363,1959	Included reference to EMC report
	1339, 1349, 1672	Disable of pc_CP (CR028)
	1135, 1136,	Update of PSRR/EMC specification ACC according to CR026
	1920, 1921	Update of PSRR/EMC specification ARS according to CR026
	2112, 2183	Update of TIG720 revision IDs
	2121	Added comment for cyclic register check monitor configuration.
	2124, 2125	Update of values for external frequency monitoring.
	2141	Update of calculation method and limits for frequency monitoring.
	2167, 2242	Added comment for number of bite repetition configuration.
	2003, 987	Update of startup-time limit and startup-timing according to CR030.
	1721 – 1726	Update of flaglist according to CR028 and masking of dsp_..._lf_out limiter flag.
	1728, 1408	Update according CR029. No yrs_pll_unlock flag because of ICO_Limiter.
	1214	Update vibration robustness to CMG241M sensing element.
	1400,1421	Update of CPAR1_CAL monitor descriptions according to CR021.
	703	Link to EMC test specification and report for SMI720 c-samples added.
	981	EOP activation added into flow chart.
	1125, 1159	Option 1 / 2 added and comment on C_VDD_IO (only if Option 1 is used)

	205	AXI2 changed to Oblong-Pad according C-sample BLR qualification.
	1124, 2222	CMA511N introduced in 1124 and CMA511M changed to CMA511 in 2222.
	1375	Error counter behaviour in case of a single error flag event included.
	2132, 2160	Calculation for Temperature out of TEMP1 signal (nominal value).
	2282, 2283	Simplified block diagram (ACC / RATE) with clock frequencies added.
	1131, 1132,	Comment: This is currently no released operation mode for SMI720.
	1205, 1206	Comment: This is no released operation mode for SMI720.
	2111, 2187	Default value changed according customer request.
	1141	Remark deleted. C-sample qualification passed.
	1131, 1132	Values changed according c-sample qualification.
	2182	Recommendation to check ASIC_NAME of TIG720 extended.
	205, 206	Dimensions according CR031 and laser marking for series parts updated.
	2080	Minimum value for CPUMP voltage corrected.

Table of Contents

1. Introduction

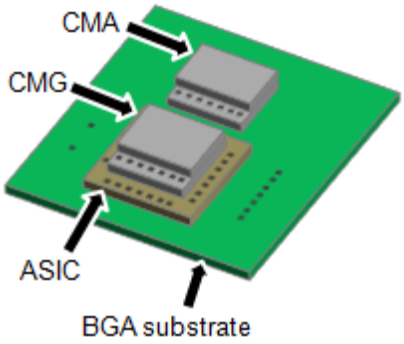
Req_3 This document describes properties, functions and target performance of the combined angular rate (Ω_x) and a single channel acceleration sensor (a_z) SMI720 for roll over detection of vehicles. This sensor specification is created on the basis of the requirement specification supplied by the customers (AE/ESE3 and CC-PS/EPY2, CC-PS/PJ-SMI7).

1.1 Scope of the Document

Req_5 The purpose of this document is to collect and structure the system requirements and configure the functional groups of the SMI720. Additionally, the document should ensure the traceability of the customer requirements.

1.2 System Overview

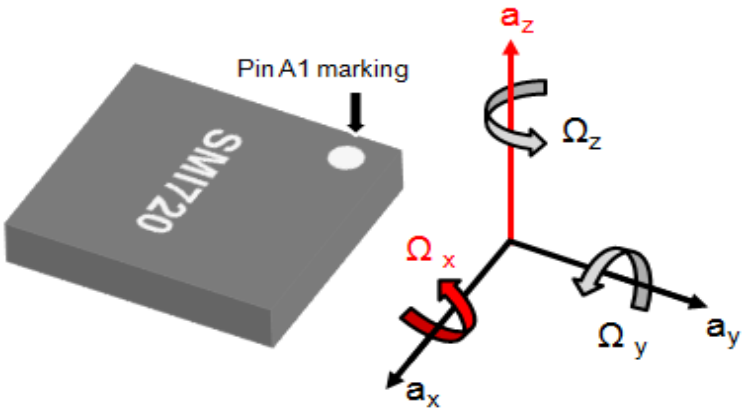
Req_1124 The SMI720 consists of a single channel angular rate sensing element, a single channel acceleration sensing element, and an ASIC packaged in a Ball Grid Array package (BGA). For the Ω_x angular rate sensing element, the CMG240M (up to A0B-sample state) or CMG241M (from A0C-sample state on) from SMI71x project will be used without any changes. For the acceleration sensing element the CMA511M was designed as a_z channel sensing element. During ramp-up CMA511M will be exchanged by CMA511N. The ASIC, the TIG720, will be developed as a "fast follower" of the TIG700 ASIC.



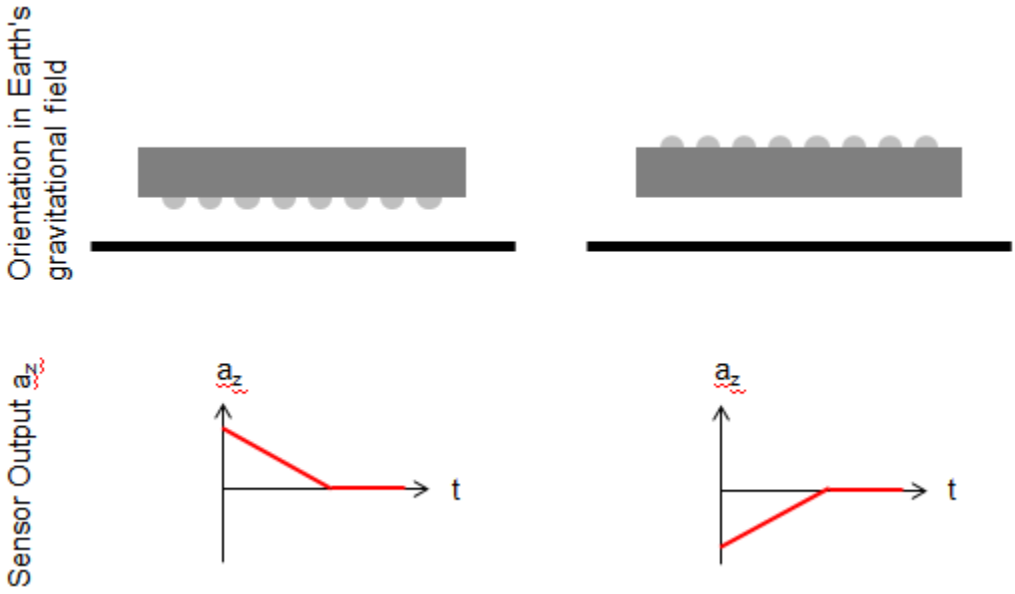
1.3 Definitions

1.3.1 Coordinate System

Req_12 The coordinate system used within this specification uses three axes. The x-, y-, and z- axes are perpendicular to each other and form a right-hand coordinate system. The z-axis is perpendicular to the mounting plane. The angular rate axes Ω_x, Ω_y and Ω_z are the rotations around the respective coordinate axes.



Req_2267



Sensor output of acceleration channel (a_z) in Earth's gravitational field.

1.3.2 Acceleration

Req_14 In the following, 1 g is equal to 9.81 m/s^2.

1.4 Disclaimer

Req_1178 This product is solely intended for use in airbag ECUs where the SMI720 is soldered onto a PCB. These ECUs are located within the car's passenger compartment or the car's trunk. The sensor does not have any robustness against any special medium. Its use is only permitted under the specified conditions and according to the environmental and loading conditions specified in this document.

Any change in the product's operating environment from the original scope of validation, or use in applications not approved by Robert Bosch GmbH, must be communicated to and released by Robert Bosch GmbH.

For any use of products outside the released applications, specified environments or installation conditions no warranty shall apply, and BOSCH shall not be liable for such products or any damage caused by such products. No repair of the product is allowed.

2. General

Req_101 The specified behavior in this document can only be guaranteed if the following requirements for "Storage", "Life Time", "Manufacturing at Customer Plant", "Maximum Ratings", and "Operating Ratings" are insured by the customer.

All these requirements can be considered in parallel.

If temperature ranges are given, for each range the worst case can be assumed.

Req_1913 All specified parameter limits reflect +/-4 sigma values with a confidence level of 90% if not noted otherwise. If a parameter is not normally distributed, the limits reflect an equivalent with the same percentage of reliability as +/- 4 sigma.

All parameter values noted as "t.b.d" will be specified during the course of the development.

2.1 Storage of Sensor Module

Req_103 The SMI720 can be stored for 1 year by the customer before it will be used in the production, as long as the temperature profile specified below and the MSL-3 requirements (see IPC/JEDEC J-STD-033C) are met during that time.

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	Storage Time	$T_{s\text{-}cold}$	–55 °C – +10 °C			50	h
Req_938		T_s	+10 °C – +40 °C			1	a
Req_939		$T_{s\text{-}warm}$	+40 °C – +70 °C			50	h

2.2 Storage in ECU

Req_1141 The ECU containing the SMI720 can be stored for 15 year by the customer before it will be installed.

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	Storage Time	T_1	-55 °C – - 40 °C			50	h
Req_1142		T_2	-40 °C – 10 °C			500	h
Req_1144		T_3	10 °C – 30 °C			Remaining time	
Req_1143		T_4	+30 °C – +70 °C			50	h

2.3 Life Time

Req_105 A life time of 17 years including 15000 operation hours are guaranteed for the mission profiles listed below excluding the Autoliv mission profile. For the Autoliv mission profile a life time of 20 years including 16000 operating hours can be guaranteed. The following mission profiles will be considered for calculating the required stress test within the qualification of SMI720: S

Non operating profiles:

Airbag12				Autoliv		
	Sum [h]	133920			Sum [h]	159340
from [°C]	to [°C]	(17a)		from [°C]	to [°C]	(20a)
-55	-50			-52.5	-47.5	
-50	-45			-47.5	-42.5	
-45	-40	0		-42.5	-37.5	
-40	-35			-37.5	-32.5	
-35	-30			-32.5	-27.5	
-30	-25			-27.5	-22.5	
-25	-20			-22.5	-17.5	
-20	-15			-17.5	-12.5	
-15	-10			-12.5	-7.5	
-10	-5			-7.5	-2.5	0
-5	0			-2.5	2.5	5320
0	5			2.5	7.5	15940
5	10			7.5	12.5	21240
10	15			12.5	17.5	23900
15	20	73656		17.5	22.5	23900
20	25			22.5	27.5	21240
25	30			27.5	32.5	10620
30	35			32.5	37.5	10620
35	40	26784		37.5	42.5	7960
40	45			42.5	47.5	2660
45	50			47.5	52.5	5320
50	55			52.5	57.5	7960
55	60	20088		57.5	62.5	2660
60	65			62.5	67.5	
65	70			67.5	72.5	
70	75			72.5	77.5	
75	80	12053		77.5	82.5	
80	85	1339		82.5	87.5	
85	90			87.5	92.5	
90	95			92.5	97.5	
95	100			97.5	102.5	
100	105			102.5	107.5	
105	110			107.5	112.5	
110	115			112.5	117.5	
115	120			117.5	122.5	
120	125			122.5	127.5	
125	130			127.5	132.5	
130	135	0		132.5	137.5	0

Operating profiles:

AB12	
Self-Heating incl.: 20 K	
T / °C	h
Sum	15000
40	8250
60	3000
80	2250
100	1350
105	150

Autoliv	
Self-Heating incl.: 10 K	
T / °C	h
Sum	16002
42.5	534
47.5	1600
52.5	2134
57.5	2934
62.5	3200
67.5	2400
72.5	1600
77.5	1334
82.5	266

Continental	
Self-Heating incl.	
T / °C	h
Sum	12000
23	720
60	7800
85	2400
95	960
105	120

In the operating profiles above, the self-heating of the ECU is already included. For qualification, a maximum of 15 K self heating within the package of SMI720 will be considered additionally. If characterization or evaluation results show a lower self heating of the SMI720, the lower value for the self heating will be considered for the qualification.

Req_1927

Parameter	Conditions	Min	Typ	Max	Unit
On/Off Cycles	Pure electrical, not considering temperature variations *)	-	-	300000	-

*) Measured at entire temp. range according to operation profiles, i.e. temp is swept over entire temp range until specified cycles are finished.

Req_1928

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Cycles	Cold start, temperature delta of 54 K	-	-	12410	-
	Warm start, temperature delta of 30 K	-	-	49640	-

2.4 Manufacturing at Customer Plant

Req_973 In general it is possible to do manufacturing in all AE plants, if the plant can handle BGA-packages (Ball Grid Array) on tape & reel and meet the conditions described within this chapter (for further details to the transport package see also chapter "Transport Package").

Details on the manufacturing at the customer plant are given in the "Recommendation of assembly of SMI7 family BGA package on PCB". Main points are given below in brief.

2.4.1 Mounting Position on PCB

Req_108 The positioning of the SMI720 on the PCB has to be chosen carefully with consideration of the mechanical constraints and vibration robustness. The customer has to consider the mechanical properties as well as layout design of the PCB and the ECU. If crosstalk between sensors or other mechanical distortions on a PCB arises which lead to a breach of specification, application hints will be provided by sensor development. The final positioning of the device should be characterized by vibration analysis of the ECU.

Req_963 It is allowed to mount the devices on both sides of the printed circuit board, but no overlap of the two footprints is allowed.

2.4.2 Soldering Process

Req_110 The sensor module is designed to withstand double side reflow solder processes using lead free solder material. It will withstand up to 3 solder cycles, if the solder process is compliant with the attached specifications for lead-free soldering: "Verfahrensvorschrift Fertigung 1 269 918 512 (18.11.2008)"

Due to the chosen BGA package for SMI720, the sensor will be solderable with a 120µm and 150µm solder mask thickness (Lochschablonendicke) (please refer to Chapter 1.3.1 within "Verfahrensvorschrift Fertigung 1 269 918 512") on 18-35 µm copper layers.

2.4.3 Coating/Lacquers

Req_2264 As for most BGA, no conformal coating or lacquers is recommended. Reason for this is reduced BLR lifetime and possible corrosion.

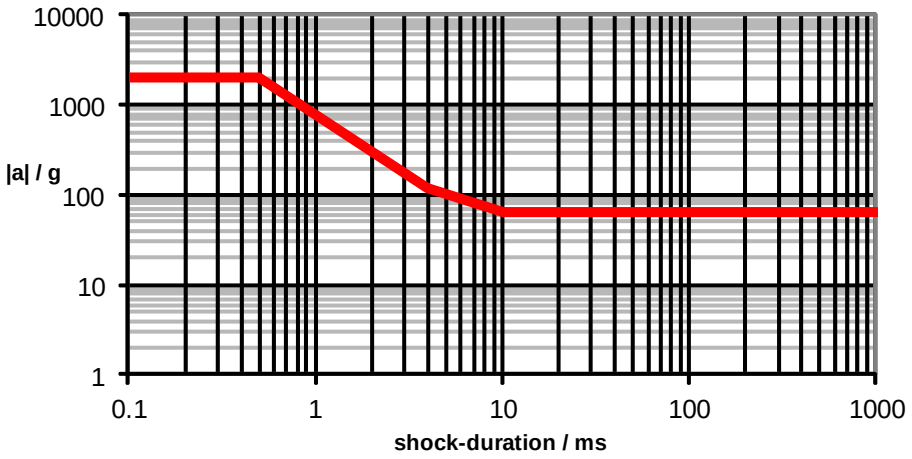
2.4.4 Mechanical Stress

Req_112 The strain in the plane of the sensor due to bending of the PCB has to be less than 500 µm/m to achieve described sensor performance. A strain of 1100 µm/m can be applied during manufacturing without sensor damaging.

Other stress effects within the PCB (geometry effects; humidity-changes; …) are not known and specified today. Therefore such effects cannot be covered within the described performance. If necessary, they have to be handled by change requests.

Vibration and/or mechanical shock during manufacturing has to be lower than shown in the graph below.

Max. Acceleration during Manufacturing



2.4.5 Module Configuration

Req_115 The SMI720 supports an auto detect mode for the SPI-Interface and therefore does not have to be configured at end of line testing. The customer specific configuration is done via an initialization sequence of SPI commands at each start up. The following parameters are configurable by the customer:

1) Error counter limits
2) SPI protocol settings via calibration command and autodetect mechanism (CPOL, CPHA, protocol)
3) Safety IDs
4) Filter flush time

A detailed description of the configuration procedure will follow in Chapter 5 (Functional Specification).

2.4.6 Final Test

Req_120 The standard start-up procedure (Chapter 5, Functional Specification) will be required at ECU-level (end of line) at room temperature. Additional tests, which during development may turn out to be necessary at end of line testing, will not take longer than one second and can be performed also at room temperature.

2.5 Maximum Ratings

Req_127 The parameters defined in the table below have to be guaranteed by the application, otherwise the device can be damaged or pre-damaged, so that the sensor behavior cannot be guaranteed to lie within the specification during the remaining life time.

Req_128

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage Supply (VDD_IO and VDD3)	VDD		−0,3		3,6	V
Req_920 Digital Pins (MOSI, MISO, SCLK, CSB, SCAN_OUT2, EXT_CLK)		Maximum is 3.6V	−0,3		VDDIO +0,3	V
Req_1179 VDD1_8		No supply, only externally buffered.	−0,3		2	V
Req_921 CPUMP		No supply, only externally buffered.	−0,3		30	V
Req_922 Mechanical Shock		T<0,5ms in x, y and z directions	−2000		+2000	g
Req_923 Ambient Temperature *)	T_{amb}		−50		+135	°C
Req_924 Temperature Gradient *)	T_{grad}		−20		+20	K/min
Req_925 Electrical Static Discharge		HBM (1.5k, 100pF, all pins)	2,000			kV
		MM (characterization of 0,25 kV)	0,200			kV
		CDM (corner pins 0,75 kV)	0,500			kV

*) sensor active or passive

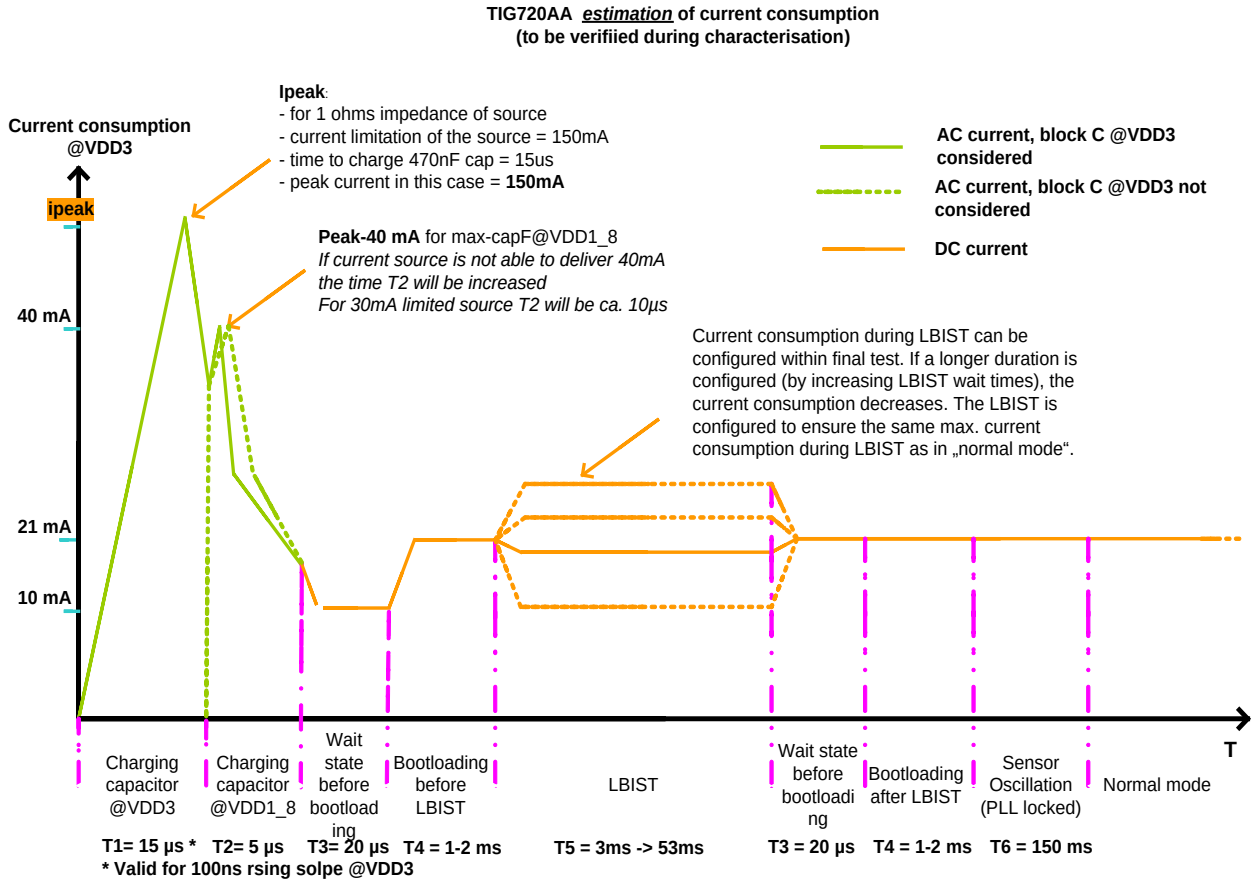
2.6 Operating Conditions

Req_131 The specification of the sensor is guaranteed only, if the conditions defined in this section are fulfilled and the device has passed the standard start-up procedure (Chapter 5, Functional Specification).

In case of a sensor internal failure, this is signaled by any of the following safe states: failure flag, corrupted CRC, or no communication.

Please refer to the chapter "Operation Conditions Safety" for required safety relevant measures within ECU.

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	Yaw Rate Channel (x)	FS_{yaw}		–300		+300	°/s
Req_931	Acceleration Channels (z)	FS_{acc}		–5		+5	g
Req_933	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	Voltage Supply	VDD3, VDD_IO	Sensor must be fully functional until Over- or Under Voltage Detection Flag is set. Voltage range at VDD3 and VDD_IO pin. Voltage drop over series R has to be considered.	3,13		3,47	V
Req_2269	Voltage Supply	VDD3, VDD_IO	Sensor must be fully functional until Over- or Under Voltage Detection Flag is set. VDD3 voltage range with considered voltage drop over series R of PSRR-Filter (max. R and max. current consumption).	3,176		3,47	V
Req_934	Supply Transient	VDD_{slew}	during power on and power off (1)			0.1	V/ns
			during operation (2)			0.01	V/s
Req_966	Humidity		-40°C ... +52°C			100	% rel. H.
			+52°C ... +64°C			H (4)	% rel. H.
			+64°C ... +105°C			0	% rel. H.
Req_935	Operation Temperature (ambient to SMI)	T_{op}	static	-40		+105	°C
			gradient	-6		+6	K/min
Req_1182	Supply Current	I_VDD3	during power on and power off (1)			150	mA
			during operation (2)			21	mA
		I_VDD_IO	during operation, depends on f_{SCK} (2)			2	mA



Current consumption at VDD3 during LBIST is always <21mA. This is ensured by LBIST configuration.

Req_937 (1) C_{load} = 470 nF @ VDD3 and 1Ohms impedance of the source and 150mA current limitation of the source

(2) PSRR requirements will be fulfilled independently from this specification

(3) This timing depends on the timing of the SPI sequences in the ECU. Above value assumes, that the respective SPI Commands are sent at the ideal time slots.

(4) H = 100 – 8,333 *(T-52°C)

3. Physical Specification

Req_201 This chapter describes the transport and device package, as well as the mechanical and electrical interface.

3.1 Transport Package

Req_203 The SMI720 is delivered on tape and reel. The package is compliant with the requirements for storage and handling. For details see also Chapter 2.

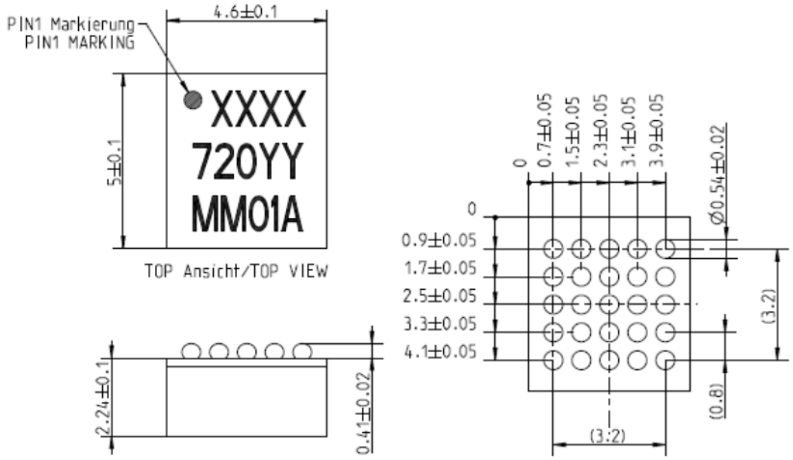
Req_1146 The sensor will be delivered within a dry package, which ensures one year storage after production and the specified floor time according to MSL-3.

Req_1148 Drop tests will be done in the transport package as well as on component level. For details please see chapter "Product Qualification".

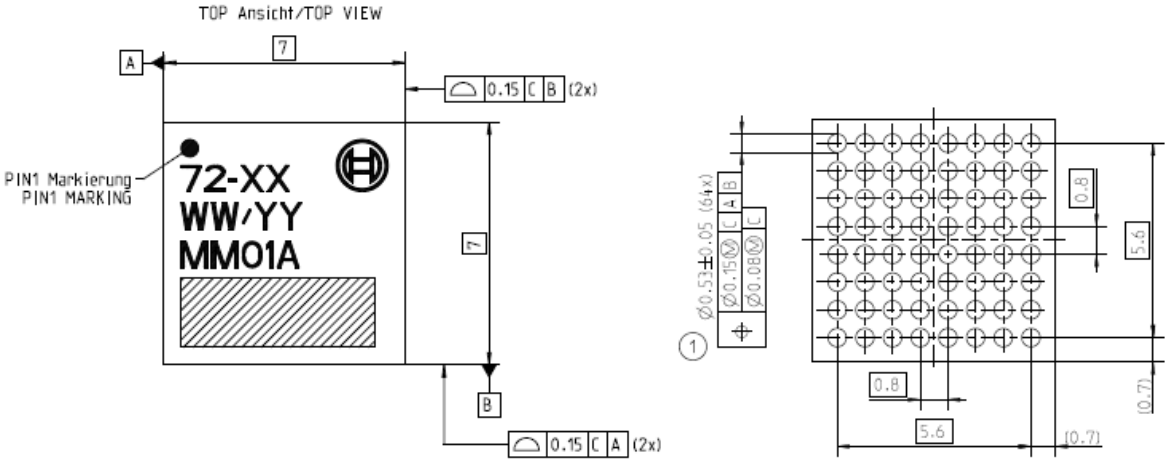
3.2 Mechanical Interface (Package)

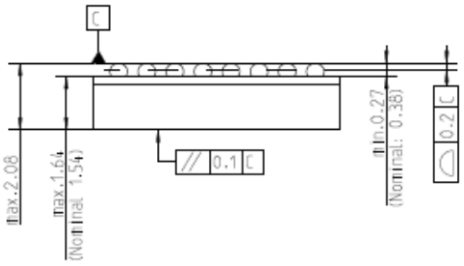
Req_205 For the SMI720, a Ball Grid Array (BGA) package as shown below is used.

a) Dimensions A0-samples in BGA 4.6x5 (will be discontinued)

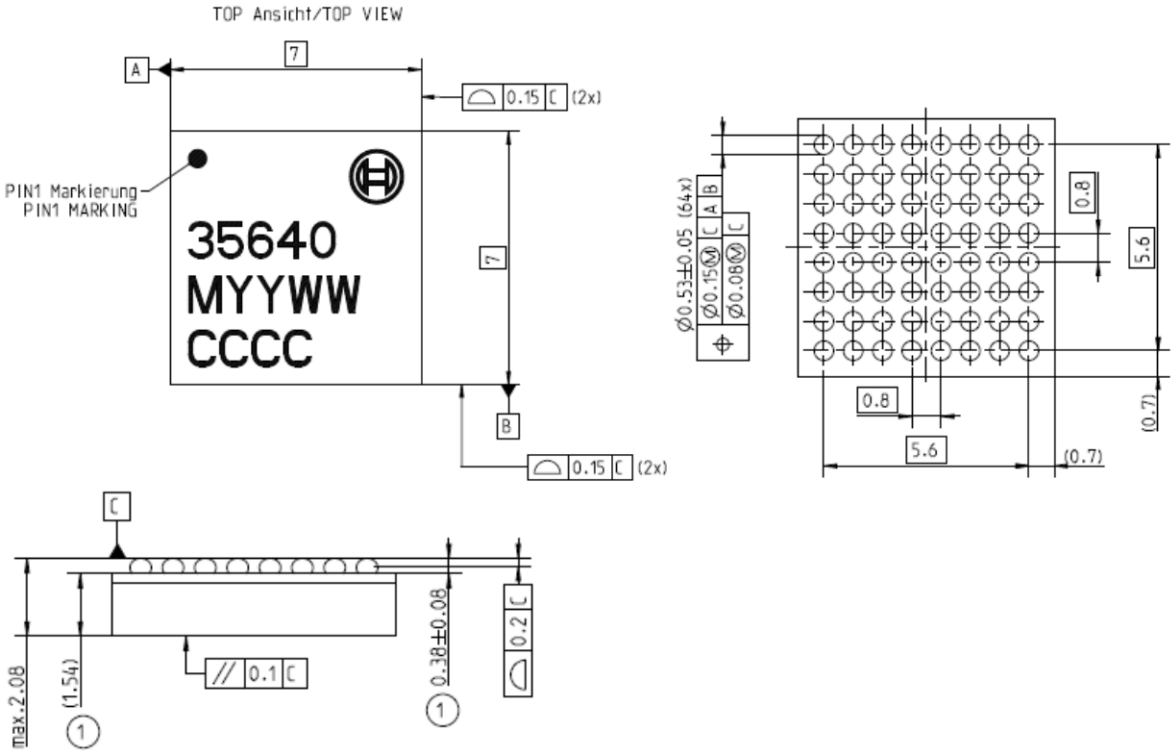


b) Dimensions from A0B-samples on in BGA 7x7 (see offer drawing 0 274 A01 044)





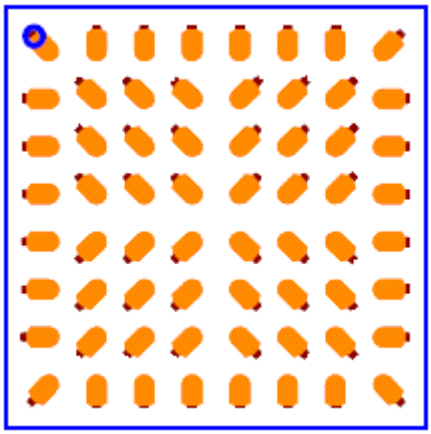
c) Dimensions for series parts in BGA 7x7 (see offer drawing 0 274 A01 111) according CR031.

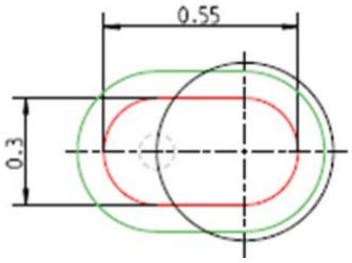


Weight w/o balls approx.: 0.164 g +/- 0.020 g

Weight w/- balls approx.: 0.195 g +/- 0.030 g

From A0B-samples on in BGA 7x7, the footprint below employing oblong-pads orientated as depicted below, arranged in a grid with 0.8 mm pitch is suggested to ensures a suitable X-ray inspection and a best orientation after soldering (Einschwimmverhalten). This footprint allows employing an 18-35 µm copper layer.





Oblong-Pad

Oblong-Pad 550µm was used for SMI720 BLR qualification. Cu-area for Oblong 550µm: 147000 µm².

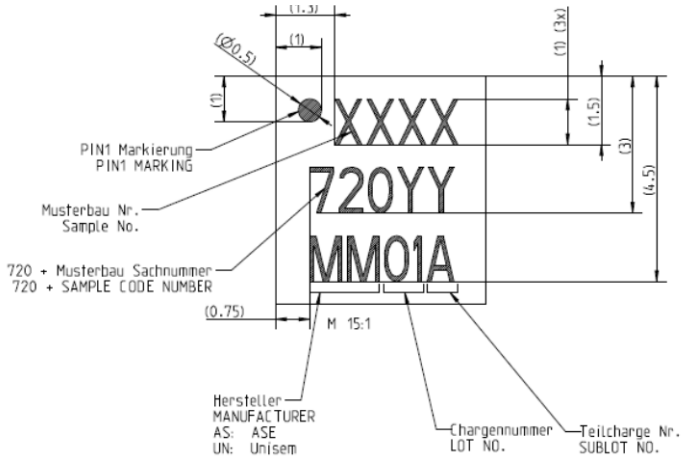
For Bosch internal use, the footprint needs to be released by AE/EAI. For external customers, Bosch does not release the footprint but only gives a recommendation.

The SMI720 footprint shown above will be qualified for the SMI720 to ensure a sufficient board level reliability with a 4 layer FR4 PCB. 2 and 6 layer PCB will be released if the BLR qualification with additional temperature cycles was passed (+10% temperature cycles in relation to a 4 layer PCB as discussed with AE/EAI for 6 layer PCB). Deviations to the qualified footprint and PCB must be qualified by the application separately.

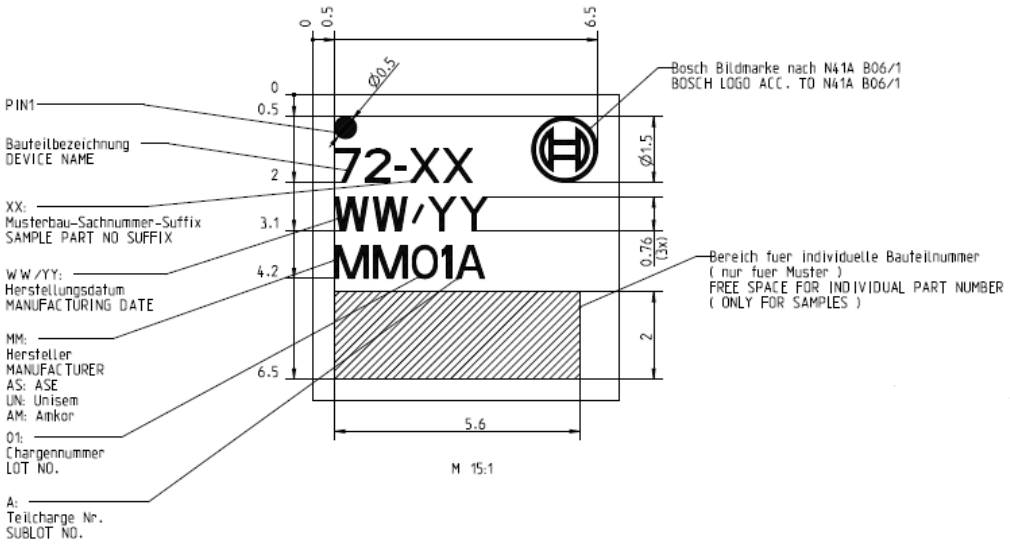
Req_206 To identify the product easily and for first level traceability there is basic information printed onto the top surface via a laser system. The laser marking specified below applies for samples and will be changed for series production.

Additional part information for unique identification is available via the SPI-Interface (see Section 4.3.7.2 for details).

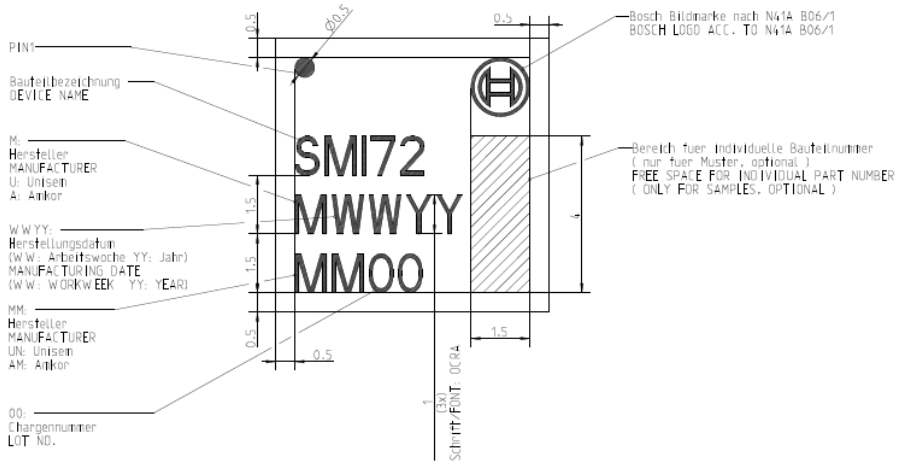
a) Laser marking A0 samples BGA4.6x5



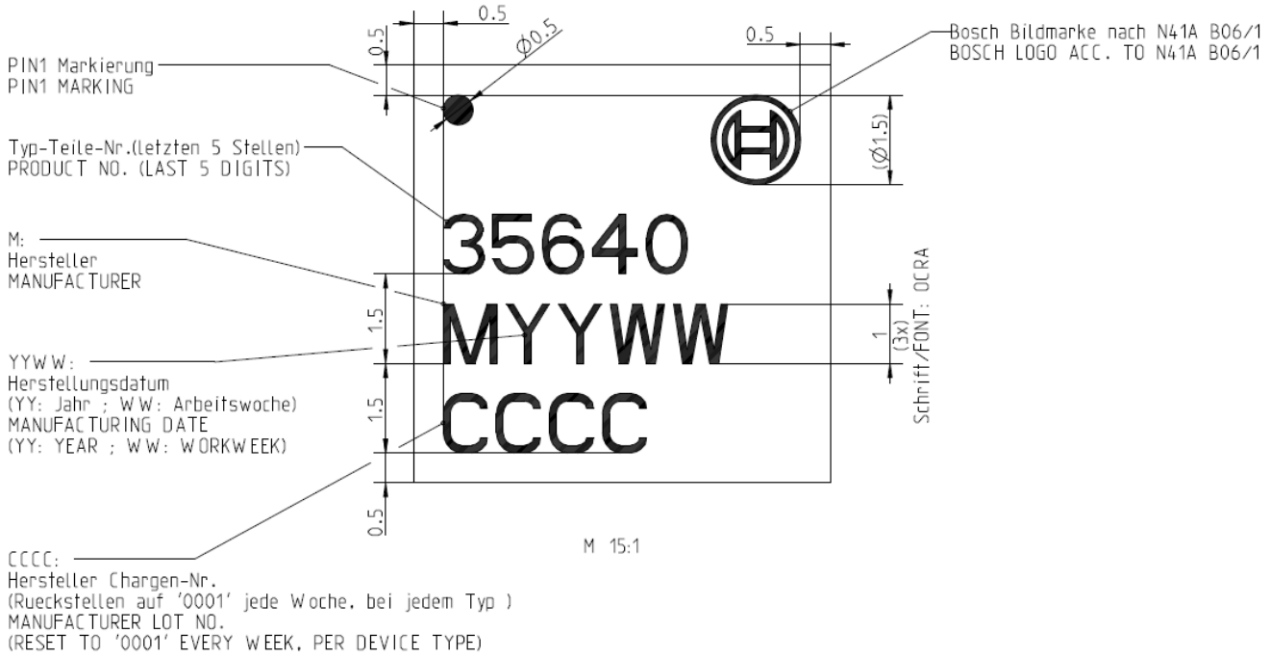
b) Laser marking from A0B-samples on in BGA 7x7



c) Laser marking from C-samples on

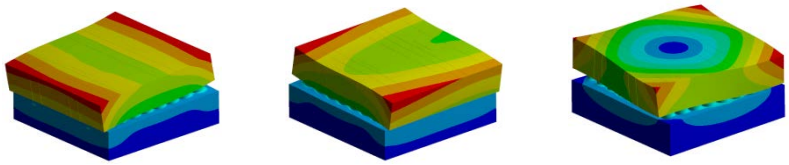


d) Laser marking for series parts



3.3 Vibration Behavior of Sensor Package

Req_2052 The figure below depicts the first three vibration modes of the SMI720 in BGA 7x7



1st vibration mode 2nd vibration mode 3rd vibration mode

All vibration modes are designed to have frequencies above 70 kHz.

Hint: Vibration performance of the sensor depends on the employed PCB material. In the design of the sensor, FR4 with the following material parameters and a thickness of 1,6 mm has been considered:

	E [MPa]			G [MPa]			n [-]			r [kg/m3]
	x	y	z	xy	xz	yz	xy	xz	yz	
FR4 (PCB)										
T = 22 °C	17850	17850	7055	6630	2250	2250	0.15	0.35	0.35	1800
T = 125 °C	16000	16000	5000	*6630*	*2250*	*2250*	0.15	0.35	0.35	1800

3.4 Recycling and Ecological Footprint

Req_208 The sensor is compliant to ROHS specification (EU-Richtlinie: 2011/65/EU). Additionally, the sensor module has less than 50 ppm (mass) of bromine (Br), which is garanteed by the assembly subcontractors.

4. Electrical Interface

Req_210 The sensor is designed for a 3.3V application. The device does not need an external reset, since there is a power on reset circuitry on chip, which ensures safe and stable initial conditions of the sensor after power on phase of the overall ECU. The software reset will trigger the same state within the ASIC as a hardware reset (resetting all registers and all parts within the ASIC to initial conditions).

Req_1149 The sensor behavior specified in this document includes the application circuitry specified in this chapter. If the customer deviates from the proposed application circuitry, the sensor behavior might differ from this specification. The customer is responsible for any deviation to this specification caused by a different application circuitry.

4.1 Pinning & Layout

Req_212 The pin out of the device will provide all pins that need to be connected by the customer at least twice to allow the customer to check the connection after soldering the device on the PCB during final test or to enable the customer to get a double functional connection of the sensor pins to the PCB (double pinning).

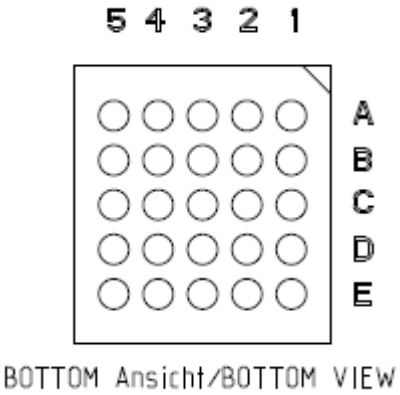
For SMI720 A0 samples in BGA 4.6x5: Corner pins (A1, A5, E1, E5) must not be used as a single connection for a functional pin. If only one connection for each pin is used by the customer, the functional pin which is not a corner pin must be connected to the PCB layer.

The orientation of the SMI720 is given by the layouts below, rotation is not possible.

The table below shows the position and function of all pins of the SMI720 A0 samples in BGA 4.6x5

Loc.	Function	Symbol	Type	Remark
A1	Not Connected	n/c		Backup for Reset_B
A2	Not connected	n/c		Backup for Reset_B
A3	Charge Pump	CPUMP	Analogue	Internal charge pump voltage
A4	External Clock	EXT_CLOCK	Digital In	Not to be used by the customer
A5	Not Connected	n/c		
B1	Ground	GND	Ground	Ground connection
B2	Ground	GND	Ground	Ground connection
B3	Charge Pump	CPUMP	Analogue	Internal charge pump voltage
B4	Chip Select	CS_B	Digital in	Chip select input for SPI communication
B5	Chip Select	CS_B	Digital in	Chip select input for SPI communication
C1	VDD3	VDD3	Power supply	Input for 3.3V supply voltage
C2	VDD3	VDD3	Power supply	Input for 3.3V supply voltage
C3	SCAN Out	SCANOUT2	Digital out	Not to be used by the customer
C4	SPI Clock	SCLK	Digital in	Clock input for SPI communication
C5	SPI Clock	SCLK	Digital in	Clock input for SPI communication
D1	VDD1_8	VDD1_8	Analogue	Internal voltage of the digital part
D2	VDD_IO	VDD_IO	Power Supply	Input for 3.3V SPI supply voltage
D3	MISO	MISO	Digital out	MISO output for SPI communication
D4	MOSI	MOSI	Digital in	MOSI input for SPI communication
D5	MOSI	MOSI	Digital in	MOSI input for SPI communication
E1	VDD1_8	VDD1_8	Analogue	Internal voltage of the digital part

E2	Ground	GND	Ground	Ground connection
E3	VDD_IO	VDD_IO	Power Supply	Input for 3.3V SPI supply voltage
E4	MISO	MISO	Digital out	MISO output for SPI communication
E5	Not Connected	n/c		Connection to GND recommended

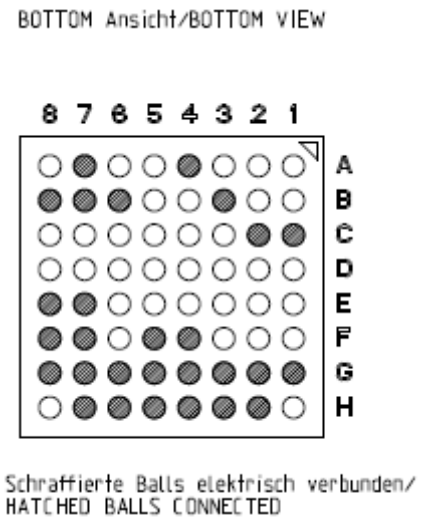


The table below shows the position and function of all pins of the SMI720 A0B samples and above in BGA 7x7

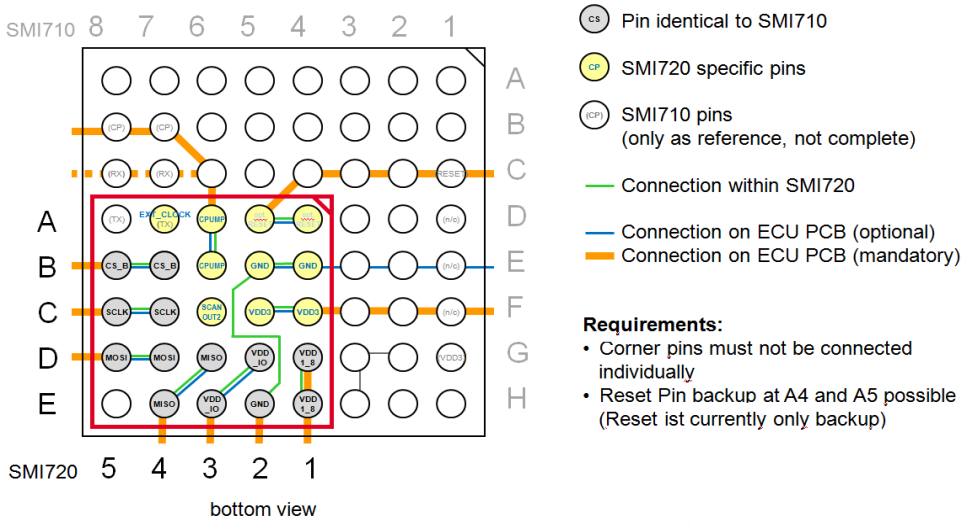
Loc.	Function	Symbol	Type	Remark
A4	SCAN Out	SCANOUT2	Digital out	Not to be used by the customer
A7	External Clock	EXT_CLOCK	Digital In	Not to be used by the customer
B3	SCAN Out	SCANOUT2	Digital out	Not to be used by the customer
B6	External Clock	EXT_CLOCK	Digital In	Not to be used by the customer
B7	Charge Pump	CPUMP	Analogue	Internal charge pump voltage
B8	Charge Pump	CPUMP	Analogue	Internal charge pump voltage
C1	Not Connected	n/c		Backup for Reset_B
C2	Not connected	n/c		Backup for Reset_B
E7	Chip Select	CS_B	Digital in	Chip select input for SPI communication
E8	Chip Select	CS_B	Digital in	Chip select input for SPI communication
F4	Anti Twist			F4 has internal short to F5
F5	Anti Twist			F5 has internal short to F4
F7	SPI Clock	SCLK	Digital in	Clock input for SPI communication
F8	SPI Clock	SCLK	Digital in	Clock input for SPI communication
G1	VDD3	VDD3	Power supply	Input for 3.3V supply voltage
G2	Ground (**)	GND	Ground	Ground connection
G3	Ground (**)	GND	Ground	Ground connection
G4	VDD1_8	VDD1_8	Analogue	Internal voltage of the digital part
G5	VDD_IO	VDD_IO	Power Supply	Input for 3.3V SPI supply voltage
G6	MISO	MISO	Digital out	MISO output for SPI communication
G7	MOSI	MOSI	Digital in	MOSI input for SPI communication

G8	MOSI	MOSI	Digital in	MOSI input for SPI communication
H2	VDD3	VDD3	Power supply	Input for 3.3V supply voltage
H3	Ground (**)	GND	Ground	Ground connection
H4	VDD1_8	VDD1_8	Analogue	Internal voltage of the digital part
H5	Ground	GND	Ground	Ground connection
H6	VDD_IO	VDD_IO	Power Supply	Input for 3.3V SPI supply voltage
H7	MISO	MISO	Digital out	MISO output for SPI communication
All other	Not Connected	n/c		Connection to GND recommended

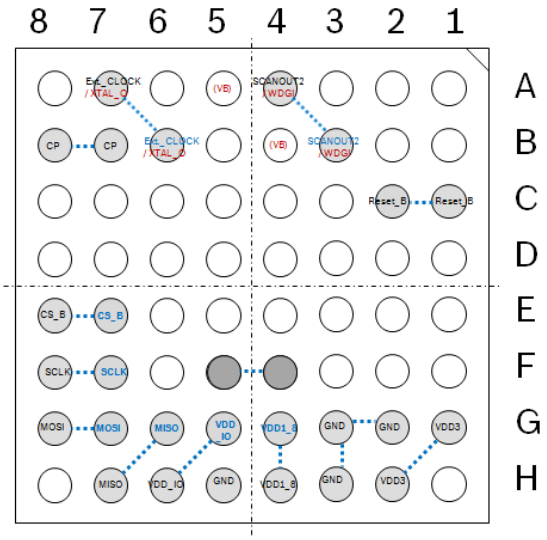
(**) Connection of balls G2, G3, H3 on PCB necessary



Req_213 The pin out of the SMI720 A0-samples in BGA4.6x5 allows a combined layout with SMI710 as depicted below.



The pin out of the SMI720 A0B samples and above in BGA 7x7 is compatible to the SMI710 footprint. Red colored Pin descriptions come from SMI710 pinout.



Due to Pin-FMEA reasons the EXT_CLOCK pin (XTAL_O at SMI710 footprint) and SCANOUT2 pin (WDGI at SMI710 footprint) must be connected to GND when the SMI720 is placed on a footprint which is also used for SMI710 and VB pin is connected to a source. If EXT_CLOCK and SCANOUT2 Pins are connected to GND, VB pin can be connected according to SMI710 specification.

Req_2235 Results of Pin-FMEA evaluation, if SMI720 is applied on SMI710 footprint:

	Pin-Number in 7x7 BGA	SMI710	SMI720	Connected to	Pin-FMEA evaluation for SMI720
1	D7/D8	Tx	N.C.	GND	ok
				3.3V	ok
2	C7/C8	Rx	N.C.	GND	ok
				3.3V	ok
3	B5/A6	XTAL_I	N.C.	GND	ok
4	B6/A7	XTAL_O	Ext_CLK	GND	For SMI720 it is required that EXT_CLOCK pin is
5	C1/C2	RESET_B	RESET	GND	Currently Reset_B Pin is n/c for SMI720. If due to unknown issues the RESET_B pin has to be connected for SMI720, a connection of this pin to GND results in a permanent reset (low active). No communication of SMI720.
				3.3V	ok
6	B3/A4	WDGI	SCANOUT2	GND	For SMI720 it is required that SCANOUT2 pin is connected to GND when SMI720 is used with a SMI710 footprint and VB pin is connected to a source.
				3.3V	No possible connection for SMI720. Due to Pin-FMEA reasons (neighbour situation to VB Pin) it is necessary to connect SCANOUT2 to GND potential.
7	B2/A3	PSI_P	N.C.	GND	ok
8	B1/A2	PSI_M	N.C.	GND	ok
K1	A5/B4	VB	N.C.	6.7V, 12V	Due to Pin-FMEA reasons the neighbour pins of SMI720 (EXT_CLOCK and SCANOUT2) must be connected to GND. SMI720 could be damaged if VB is connected to >=3.6V and shortened to a floating neighbour pin

4.1.1 Electrical Specification of Sensor Pins

Req_2097 All digital I/O pins must not be voltage driven above VDD_IO + 0.3V (maximum is 3.6V) or below GND - 0.3V. Otherwise a reverse current will flow from the digital I/O pin to VDD_IO or GND.

Req_2098 The voltage at pin MOSI may applied at any time before or after VDD_IO (since MOSI is data input; data input is registered only after CSB and SCLK; hence it is possible to apply MOSI before any other input without corrupting data in or out of ASIC).

The voltage at pins MISO, CSB and SCLK has to applied accordingly to ramping up or down of VDD_IO or when VDD_IO is already stable at specified value. These pins may never exceed above specified max voltage.

Req_1918

Parameter	IO	Special Function, Internal Structure
CS_B	IN	Low Active, Pull Up
SCLK	IN	Pull Up
MOSI	IN	Pull Up

MISO	OUT	Tristate if CSB=1 or Reset or first bits in CC32 frame are missing.
Ext_CLOCK	IN	Pull Down
SCANOUT2	OUT	Tristate

4.1.1.1 Electrical specification for VDD3

Req_2073 Specification of the pin VDD3 is given by the maximum limits, application circuitry and operating conditions.

4.1.1.2 Electrical specification for VDD1_8

Req_2076 VDD1_8 cannot be used as voltage supply output. The pin is only used for connecting a blocking capacitance.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage range	VDD1_8	full specification for sensor evaluation, voltage after end of boot sequence	1,5		2,1	V
Voltage monitoring range, high level	VDD1_8_MH	full specification for sensor evaluation, voltage after end of boot sequence	1,96		2,08	V

4.1.1.3 Electrical specification for VDD_IO

Req_2078 VDD_IO must be externally supplied. It powers the interface pins: CS_B, SCLK, MISO, MOSI, RESET_B and SCANOUT2, EXT_CLOCK.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage range	VDD_IO	full specification for sensor evaluation	3,13		3,47	V
mean current consumption during interface pins are active. (CS_B,SCLK,MISO and MOSI)	IVDD_IO	current consumption at VDD_IO depends on different parameters like SCKL frequency	1,44		2,0	mA
peak current at VDD_IO (limited due to internal resistor)	IVDD_IO_P	load at 100pF, 10ns rise / fall time			30	mA

4.1.1.4 Electrical specification for CPUMP

Req_2080 From functional point of view an external capacitor at CPUMP pin is not necessary. Nevertheless, due to lack of field experience, it is highly recommended to connect CPUMP pin to a blocking capacitor (please refer to Req_1125 / Req_1159). If no capacitor at CPUMP pin is applied, EMC performance is reduced due to earlier status-flag (CI)occurrence.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage range with / without internal load	VCPUMP	PLL frequency at minimum / maximum Minimum voltage with 120uA load, internal loads in power down	17	20	30	V
Maximal continues load current at CPUMP	ICP_max	no internal load, UDF_GEN, QUAD_GEN and OTP_reg in power down			120	µA

4.1.1.5 Electrical specification for CS_B

Req_2082 The CS_B pin has a pull up resistor of nominal (specified) from input to VDD_IO. CS_B is an input pin.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
pull up resistor	R_CSB_PU		70	100	130	kOhm
Input low voltage of CS_B pin	V_IL_CSB	VDD_IO between min/ max values	0		0,3 * VDD_IO	V
Input high voltage of CS_B pin	V_IH_CSB	VDD_IO between min/ max values	0,7 * VDD_IO		VDD_IO	V
Input low current of CS_B pin including pullup resistor and leakage current	I_IL_CSB	VDD_IO at 3,3V, input level at VSSD	23		43	µA
Input high current of CS_B pin	I_IH_CSB	VDD_IO between min/ max values	25		45	µA
Input voltage hysteresis at CSB_B	V_HY_CSB	VDD_IO between min/ max values	0,1			V
Input capacitance at CS_B	C_I_CSB	no external capacitive load, value without package, measured during characterization	1		6	pF

4.1.1.6 Electrical specification for SCLK

Req_2084 The SCLK has a pull up resistor of from input to VDD_IO. SCLK is an input pin.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
pull up resistor	R_SCLK_PU		70	100	130	kOhm
Input low voltage of SCLK pin	V_IL_SCLK	VDD_IO between min/ max values	0		0,3 * VDD_IO	V
Input high voltage of SCLK pin	V_IH_SCLK	VDD_IO between min/ max values	0,7 * VDD_IO		VDD_IO	V
Input low current of SCLK pin including pull-up resistor and leakage current	I_IL_SCLK	VDD_IO at 3,3V	23		43	µA
Input high current of SCLK pin	I_IH_SCLK	VDD_IO between min/ max values	25		45	µA
Input voltage hysteresis at SCLK	V_HY_SCLK	VDD_IO between min/ max values	0,1			V
Input capacitance at SCLK	C_I_SCLK	no external capacitive load, value without package, measured during characterization	1		6	pF

4.1.1.7 Electrical specification for MISO

Req_2086 MISO functions as output pin. When CS_B is inactive high, then MISO goes into the high impedance state.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output low voltage of MISO pin	V_OL_MISO	VDD_IO between min/ max values, output current @ +/- 4mA	0		0,2 * VDD_IO	V
Output high voltage of MISO pin	V_OH_MISO	VDD_IO between min/ max values, output current @ +/- 4mA	0,8 * VDD_IO		VDD_IO	V
Maximum rise time from maximum output low voltage to minimum output high voltage at MISO	T_R_MISO	maximum capacitive load, strong driver mode			15	ns
Maximum fall time from minimum output high voltage to maximum output low voltage at MISO	T_F_MISO	maximum capacitive load, strong driver mode			15	ns

Capacitive load at MISO	C_L_MISO	Strong driver mode			100	pF
Output capacitance at MISO during tri-state and active operation	C_MISO	no external capacitive load, value no external capacitive load, value without package, measured during characterization	1		6	pF
Output current during high impedance state at MISO pin	I_OUTZ_MISO	VDD_IO between min/ max values	-10		10	µA

4.1.1.8 Electrical specification for MOSI

Req_2089 MOSI functions only as input pin. MOSI has a pull-up resistor from input to VDD_IO.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
pull up resistor	R_MOSI_PU		70	100	130	kOhm
Input low voltage of MOSI pin	V_IL_MOSI	VDD_IO between min/ max values	0		0,3 * VDD_IO	V
Input high voltage of MOSI pin	V_IH_MOSI	VDD_IO between min/ max values	0,7 * VDD_IO		VDD_IO	V
Input low current of MOSI pin including pull-up resistor and leakage current	I_IL_MOSI	VDD_IO at 3,3V	23		43	µA
Input high current of MOSI pin	I_IH_MOSI	VDD_IO between min/ max values	25		45	µA
Input voltage hysteresis at MOSI	V_HY_MOSI	VDD_IO between min/ max values	0,1			V
Input capacitance at MOSI pin	C_I_MOSI	no external capacitive load, value without package, measured during characterization	1		6	pF

4.1.1.9 Electrical specification of EXT_CLOCK

Req_2091 Input signal used to provide clock input for digital scan test. Internal pull-down resistor, which cannot be disabled. **No function within customer application.** Pin has to be pulled to GND potential or floating (high z).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
pull down resistor	R_EXT_CLK_PU		70	100	130	kOhm
Input low voltage of EXT_CLOCK pin	EXT_CLOCK_VL	VDD_IO between min/ max values	0		0,3 * VDD_IO	V
Input high voltage of EXT_CLOCK pin	EXT_CLOCK_VH	VDD_IO between min/ max values	0,7 * VDD_IO		VDD_IO	V
Input voltage hysteresis at MOSI	V_HY_EXT_CLOCK	VDD_IO between min/ max values	0,1			V
input frequency	EXT_CLOCK_FEQ	no external capacitive load, value without package, measured during characterization			30	MHz

4.1.1.10 Electrical Specification for SCANOUT2

Req_2093 Output pin for digital scanout signal. Output has possible High impedance mode. **No function within customer application.** Pin has to be pulled to GND potential or floating (high z).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output low voltage of scanout2 pin	V_OL_SCANOUT2	VDD_IO between min/ max values	0		0,2 * VDD_IO	V
Output high voltage of scanout2 pin	V_OH_SCANOUT2	VDD_IO between min/ max values,	0,8 * VDD_IO		VDD_IO	V
Maximum rise time from maximum output low voltage	T_R_SCANOUT2				10	ns
Maximum fall time from minimum output high voltage	T_F_SCANOUT2	maximum capacitive load, strong driver mode			10	ns
Load capacitor allowed for above rise/fall time	C_L_SCANOUT2				30	pF

4.1.1.11 Electrical Specification for Reset_B (currently no option in SMI720)

Req_2095 Low level Reset input for ASIC. Internally pulled up by specified resistor. **For SMI720 just a fallback option. Currently not connected to external BGA pins.**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level Reset input for ASIC. Internally pulled up by specified Resistor.	R_RST_PU		140	200	260	kOhm
Input low voltage of RESET_B pin	RESET_B_IL	VDD_IO between min/ max values	0		0,2 * VDD_IO	V
Input high voltage of RESET_B pin	RESET_B_IH	VDD_IO between min/ max values,	0,8 * VDD_IO		VDD_IO	V
Input voltage hysteresis at RESET_B	V_HY_RESET		0,1			V
duration of active reset_b	Min_RST_B		100			ns
Load capacitor allowed for above rise/fall time	C_L_SCANOUT2				30	pF

4.1.2 Reset Levels

4.1.2.1 Reset at VDD1_8 (Power-On Reset)

Req_2100 The power on reset module (POR) generates an active low for the digital part of the TIG720. It is connected at the VDD1_8 power line. If the voltage falls below a certain level, it will generate a reset to all digital registers, which means that no clock dependent signal and control flow will be active.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
vdd1_8 voltage level for release of reset. Upper threshold voltage for por1_8	por1_8_H	Reset level of por1_8. Reset is released when upper threshold level reached, e.g. during power up.	1.6		1.8	V
vdd1_8 voltage level for setting of reset. Lower threshold voltage for por1_8	por1_8_L	Set level of por1_8. Reset is set when lower threshold level reached, e.g. during power down.	1.5		1.7	V

4.1.2.2 Reset at VDD3

Req_2103 The reset33 powers down all internal regulators in TIG720. As a consequence the VDD1_8 regulator will be in power-down too. The power-down of the VDD1_8 regulator results in a power-on reset.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Upper threshold voltage for reset_33	RST33_H	Reset level of reset_33. Reset is released when upper threshold level reached, e.g. during power up.	2,6	2,95	3,13	V
Lower threshold voltage for reset_33	RST33_L	Set level of reset_33. Reset is set when lower threshold level is reached, e.g. during power down.	2,3	2,7	3,05	V
Time below lower threshold RST33_L to guarantee a power down of the internal regulators.		A power down of the internal regulators is guaranteed, when VDD3 drops below the lower threshold RST33_L for the specified time. Default parts will power down the internal regulators earlier than specified here.	20			µs

4.1.2.3 Reset at VDD_IO

Req_2105 The reset at VDD_IO deactivates SPI-Communication when set. A deactivated SPI communication results in a high-Z mode at MISO pin.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Upper threshold voltage for release of reset at VDD_IO	VDD_IO_RST_H	The output driver is disabled during reset (high impedance). Reset level of reset_IO. Reset is released when upper threshold level reached, e.g. during power up.	2,22	2,7	3,0	V
Lower threshold voltage for set of reset at VDD_IO	VDD_IO_RST_L	The output driver is disabled during reset (high impedance). Set level of reset_IO. Reset is set when lower threshold level is reached, e.g. during power down.	1,6	2,0	2,6	V

4.2 Application Circuitry

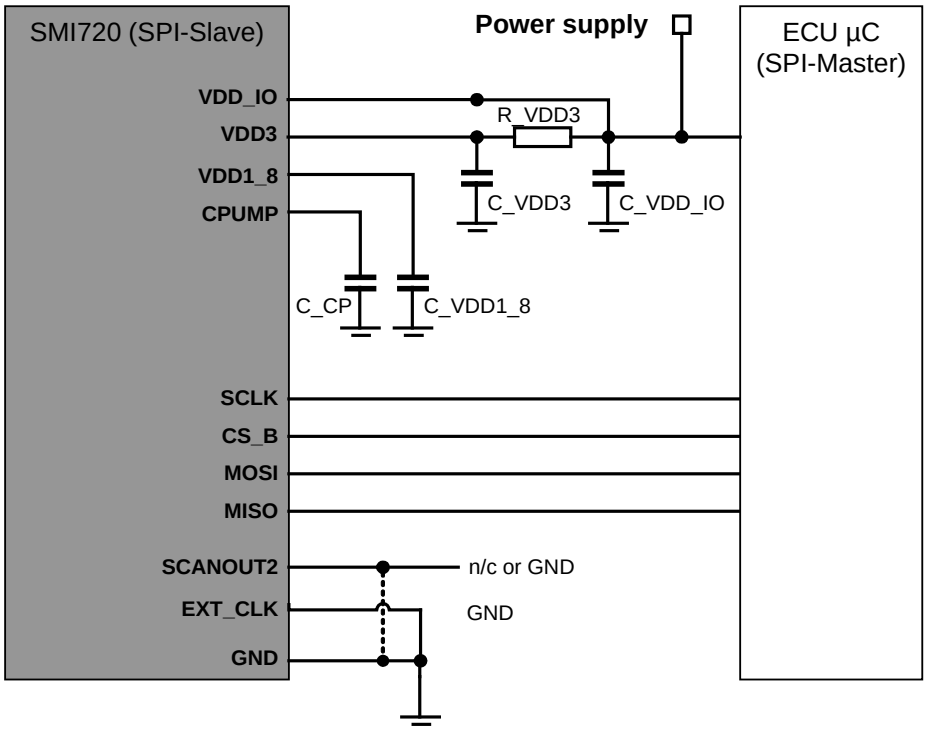
4.2.1 Application Circuit Schematic

Req_1125 All specifications are guaranteed if and only if the default circuitry as specified below is employed.

From functional point of view an external capacitor at CPUMP pin is not necessary. Nevertheless, due to lack of field experience, it is highly recommended to connect CPUMP pin to a blocking capacitor. If no capacitor at CPUMP pin is applied, EMC performance is reduced due to earlier status-flag (CI) occurrence.

All capacitors must be placed as close as possible to their corresponding sensor pin.The maximum ohmic connection of the buffer C to the VDD3 pin must be <=0.5Ohm.

Option 1:

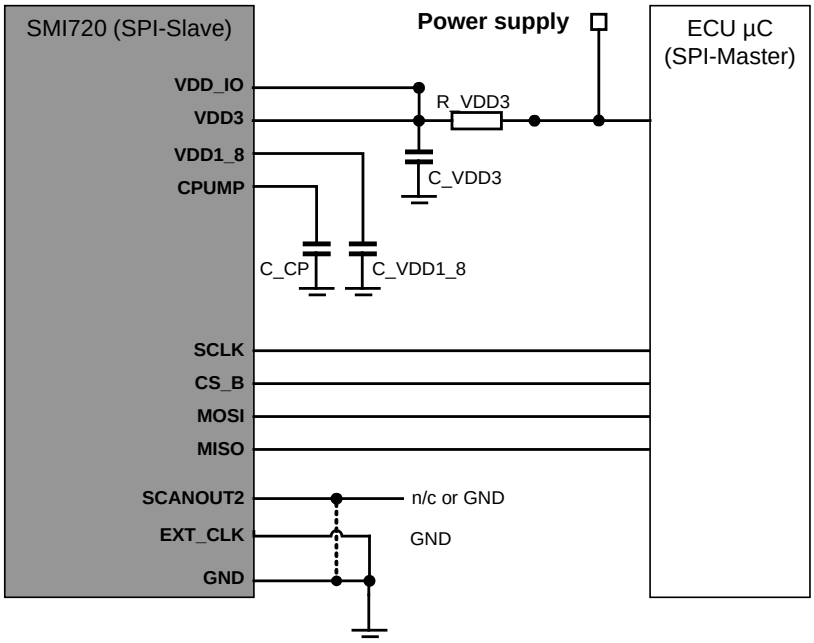


The low pass filter R_VDD3 and C_VDD3 is necessary to achieve the specified PSRR and EMC performance. If the supply voltage shows sufficiently low disturbances, the low pass filter is not required. In that case C_VDD_IO and/or C_VDD3 has to be applied anyhow to reduce SPI communication caused voltage ripple and to avoid bouncing of the VDD3 voltage during startup due to reset at VDD3. The total capacity of C_VDD_IO and C_VDD3 has to be at least 150nF (220nF - 30% tolerance) if no low pass filter is applied.

If C_VDD3 is applied, C_VDD_IO may be omitted. If C_VDDIO is not employed, VDD_IO needs to be connected directly to C_VDD3 (and VDD3) as depicted below. In this case, C_VDD3 serves also as blocking capacitor for VDD_IO.

Option 2:

Simulations with the filter configuration as depicted below show a significant higher supply noise at VDD3/VDD_IO, VDD_YAW and VDD1_8 compared to the filter configuration depicted above. During module characterization, no reproducible signal distortions caused by SPI-communication have been observed in different specific measurements to address these simulations. As these measurements have certain limitations regarding frequency step width and MISO-driver load, it is recommended to test the influence of the SPI-communication on sensor signals, error-flag behaviour and VDD3/VDD_IO voltage (close to sensor pins) at ECU-level with the applied 3.3V voltage source and real loads of the ECU at MISO pin again, if no C_VDD_IO is used. For backup reasons a PCB-layout is recommended with the ability to assemble a C_VDD_IO later on.



4.2.2 External Components

Req_1159 The external components have to fulfill the following requirements including all their tolerances. All capacitors have to be ceramic capacitors. Ensure sufficiently low resistance and impedance of the capacitors for optimum performance.

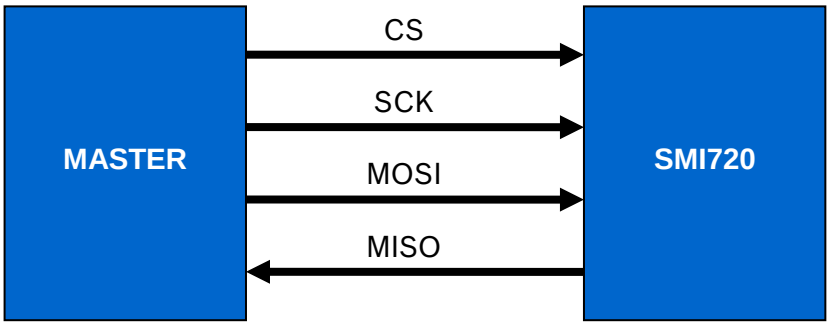
All specified capacitances can be realized by using more than one capacitor.

Name	Pin	Description	Min.	Typ.	Max.	Unit
C_CP	CP	Capacitance to buffer the CP Voltage. The voltage range for this capacitor has to be at least 40V.	39	100	167	nF
C_VDD1_8	VDD1_8	Capacitance to buffer the VDD1_8 voltage.	15	22	29	nF
C_VDD_IO	VDD_IO	Capacitance to buffer VDD_IO voltage. Only necessary if VDD_IO is connected to C_VDD3 via R_VDD3 (Option 1). Values within brackets are valid if R_VDD3 and C_VDD3 is not used.	70 (150)	100 (220)	1000 (1000)	nF
C_VDD3	VDD3	Necessary capacitance to buffer VDD3 voltage to avoid bouncing of VDD3 during startup. This capacitor is not necessary if C_VDD_IO of >150nF is applied and R_VDD3 is not used. Use at least 700 nF (typ. 1000 nF) to achieve PSRR and EMC performance as specified.	150	220	2600	nF
R_VDD3	VDD3	Optional resistor that forms with C_VDD3 a low pass filter to achieve PSRR and EMC performance as specified.	1.8	2.0	2.2	Ohm

4.3 SPI-Interface

Req_969 The SMI720 can handle two SPI dialects, the OpenSPI32 (out of frame) and the CC32IN (in frame). The required protocol, polarity and phase within the application must be configured during each startup by an auto calibration command.

The data word of the SPI-interface is 32bit wide.

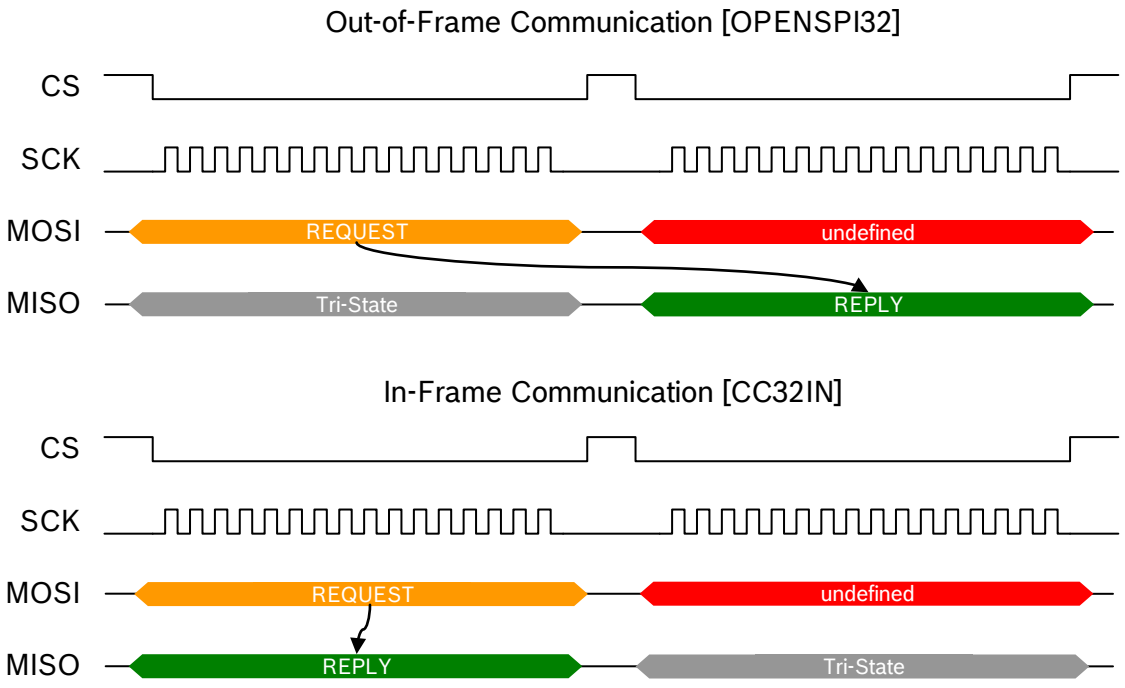


Signal lines of the SPI-Interface

The *Serial clock (SCK)* input represents the master clock signal. This clock determines the speed of data transfer and all receiving and sending is done synchronous to this clock. *Chip Select (CS)* activates the SPI interface. As long as CS is high, the sensor will not accept the clock signal or data input. The output SO is in high impedance. Whenever CS is in a low logic state, data can be transferred from the microcontroller and vice versa. Commands are transmitted through the *Serial Input (SI)* pin to the sensor and the sensor returns its response through the *Serial Output (SO)* pin.

4.3.1 Timing of Supported Protocols

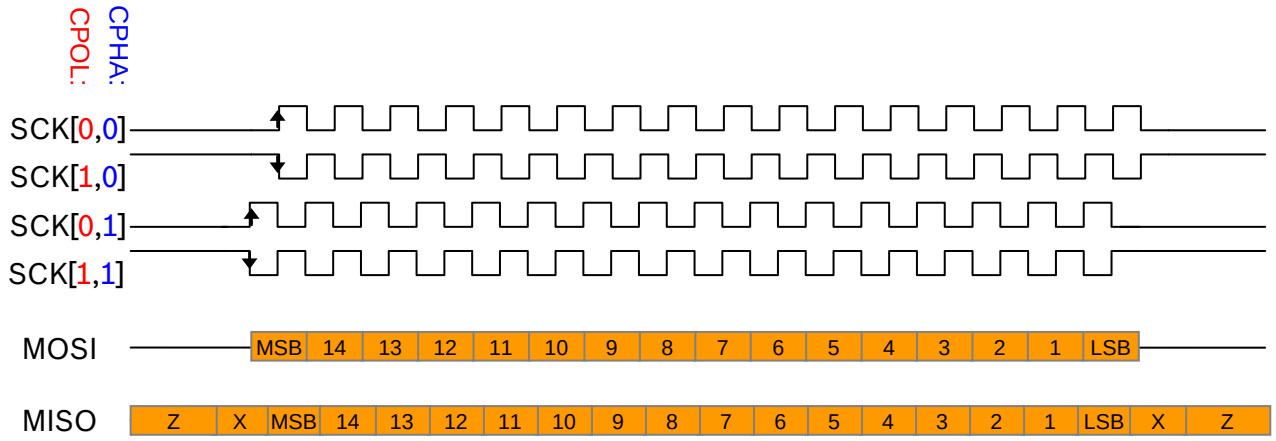
Req_219 If there is a request by the SPI-Master to the SMI720, it may respond with data in the current (CC32IN, in frame) or in the next frame (OpenSPI32, out of frame). If another slave with different BUSADR to SMI720 (except the broadcast BUSADR) is addressed by the master, the SMI720 will remain high impedant to avoid collisions on the SPI bus.



Timing of Supported Protocols

4.3.2 Definition of Polarity and Phase

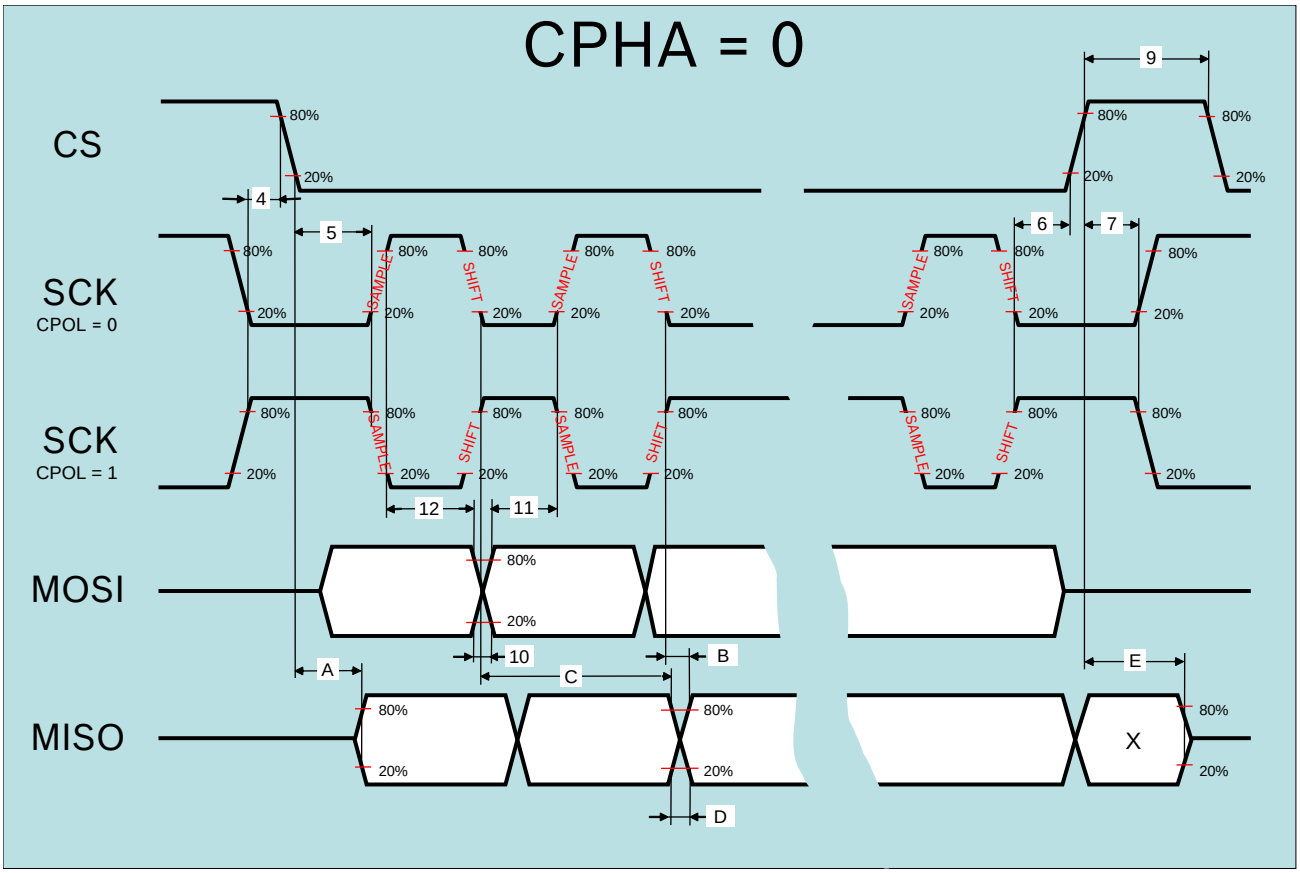
Req_910 The SMI720 will detect the polarity and the phase of the used customer protocol automatically. The picture below shows the possible combinations of polarity (CPOL) and phase (CPHA) on a 8-bit data message.



Possible combinations of polarity and phase

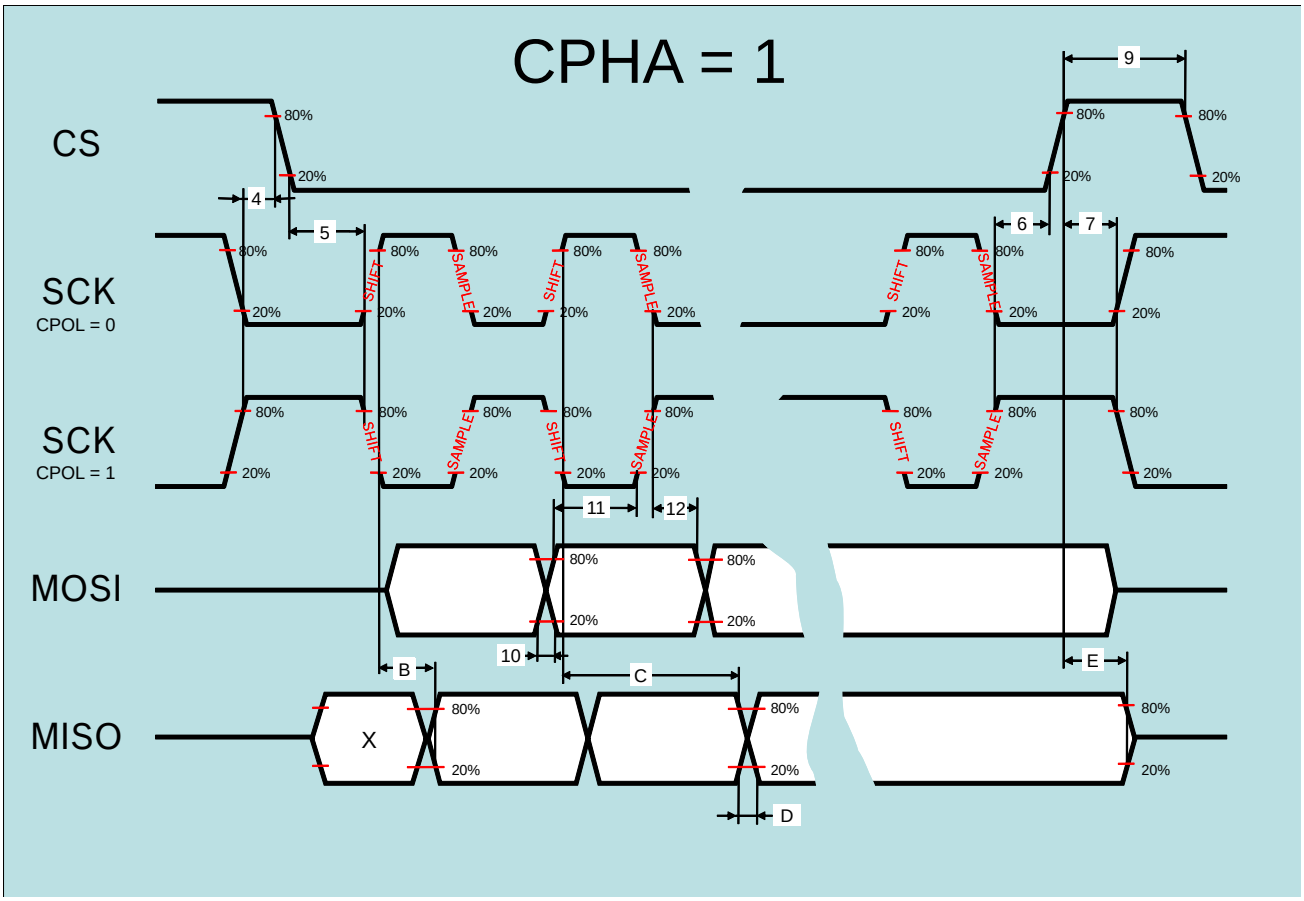
4.3.3 Detailed Timing Diagrams

Req_221



Timing for CPHA = 0

Req_222



Timing for CPHA = 1

Req_1076 Required over all tolerance for the SPI timings of the master within the application is +/-5%.

4.3.3.1 Requirements for Slave from Master Point of View

Req_1078 The data in the table below applies for an SPI clock frequency of 10 MHz (±5%).

	Parameter	Identifier	Condition	Min.	Typ.	Max.	Unit
	Data Valid Time	A	C_{load} < 100pF			40	ns
Req_1079		A	C_{load} < 90pF			32	ns
Req_1184		A	C_{load} < 80pF			30	ns
Req_1186		A	C_{load} < 70pF			29	ns
Req_1187		A	C_{load} < 60pF			28	ns
Req_1185		A	C_{load} < 50pF			27	ns
Req_1080		B	C_{load} < 100pF			40	ns
Req_1081		B	C_{load} < 90pF			32	ns
Req_1188		B	C_{load} < 80pF			30	ns

Req_1191		B	C_{load} < 70pF			29	ns
Req_1190		B	C_{load} < 60pF			28	ns
Req_1189		B	C_{load} < 50pF			27	ns
Req_1082	Data Hold Time	C	MISO data is guaranteed to be stable until the next SCK shift edge	half clock period + switch time			ns
Req_1083	MISO rise/fall time	D	C_{load} < 100pF			15	ns
Req_1084	Disable Lag Time	E	C_{load} < 100pF			50	ns

4.3.3.2 Requirements for Master from Slave Point of View

Req_1957 The SPI clock must be operated equal or below 10.5 MHz (including tolerances of the SPI master).

Req_2010 Parameter	Identifier	Condition	Min.	Typ.	Max.	Unit
SPI clock frequency		*)		10	10.5	MHz
Req_1087 SCK disable lead time	4	*)	10		-	ns
Req_1088 SCK enable lead time, CPHA = 0	5	*)	40		-	ns
Req_1089 SCK enable lead time, CPHA = 1	5	*)	10		-	ns
Req_1090 SCK enable lag time	6	*)	10		-	ns
Req_1091 SCK disable lag time	7	*)	10		-	ns
Req_1092 Sequential transfer delay, OpenSPI32 (out of frame)	9	*)	450		-	ns
Req_1093 Sequential transfer delay, CC32IN (in frame)	9	*)	200		-	ns
Req_1094 MOSI rise / fall time	10	*)	-		-	ns
Req_1095 MOSI data setup time	11	*)	10		-	ns
Req_1096 MOSI data hold time	12	*)	20		-	ns

*) Condition: C_{load} < 100 pF, SPI clock frequency ≤ 10.5 MHz

4.3.4 Auto Detect Function

Req_914 After power on, the auto detect function will be active until the SMI720 decodes a specific SPI-Message (Calibration Command) containing the protocol and phase information. The polarity of the SPI will be detected automatically. Protocol, polarity and phase will be fix for the whole power-on cycle until next reset or power-off. After having received a valid calibration command, the SPI (MISO) will react tri-state.

However, if protocol, polarity or phase has to be changed during a power-on cycle this can be done by write access to the RESET_VEKTOR register within the SPI pages.

Req_1193 The Calibration Command for CC32in and CPHA = 0 is 0xDC03E000 (bits 31:0).

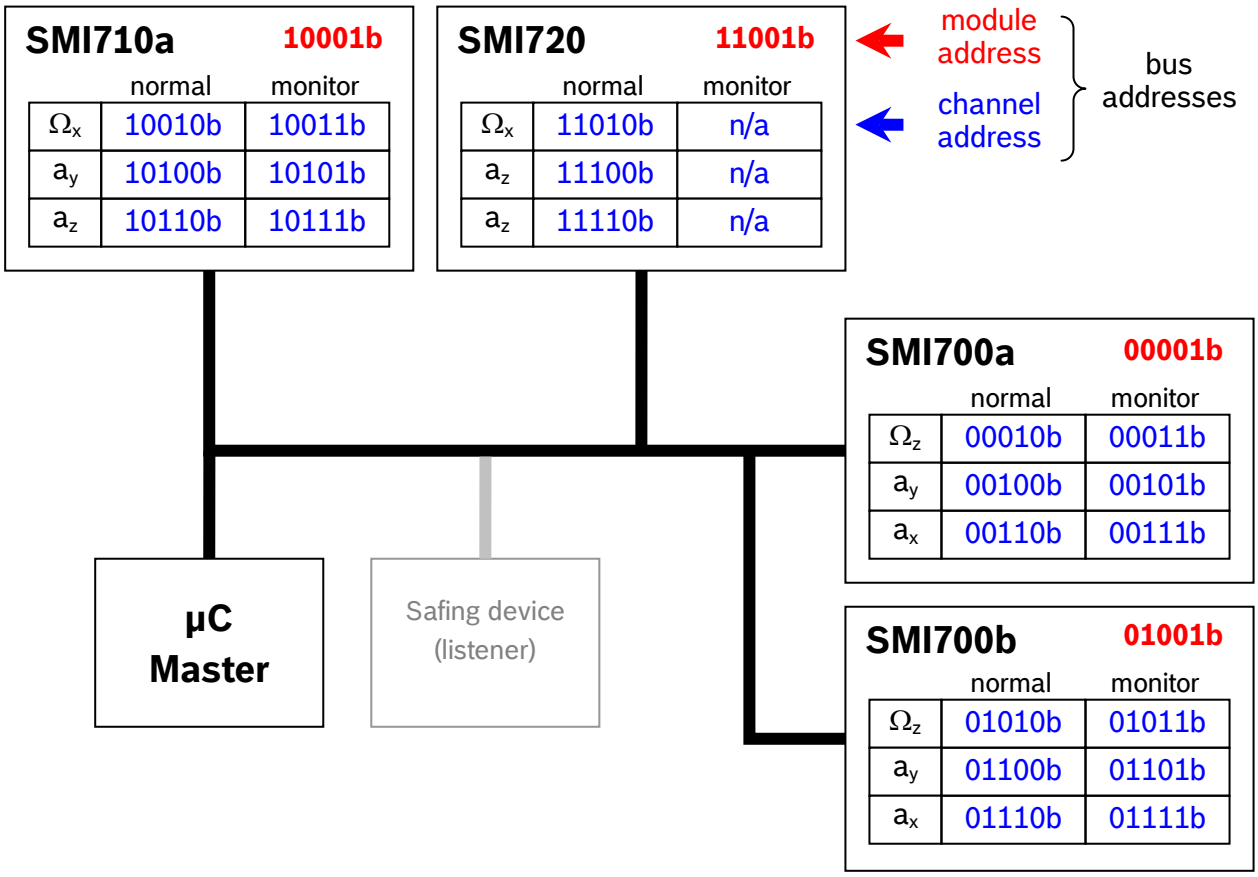
The Calibration Command for CC32in and CPHA = 1 is 0xDC001FFF (bits 31:0).

Req_1194 The Calibration Command for OpenSPI and CPHA = 0 is 0x219FE000 (bit 31:0).

The Calibration Command for OpenSPI and CPHA = 1 is 0x21801FFF (bit 31:0).

4.3.5 Single- and Multi Module Configuration

Req_975 The sensor can be used within a SPI-Bus-System with up to 4 SMI7XX-Modules using the same chip select line. To identify a specific device the two MSB [BUSADR(4:3)] are used. The three LSB [BUSADR(2:0)] are used to address the channel of the device. A typical configuration using 4 modules is shown below.



Req_224 The sensor might be applied on a SPI bus with several sensors on one chip select line. By using a specific addressing scheme different sensors can be addressed logically. Each sensor module has a specific bus address to communicate with. Each channel of a sensor module (i.e. rate LF and acceleration LF) has its own bus address. If measurement data of a sensor is requested, the channel address is used. The channel addresses are fix assigned to the sensor signals. It is possible to configure the BUSADR (4:3) by the customer during each sensor startup to a different value than 11b by writing a different value to Reset_Vector register via page mechanism (please refer to chapter 4.3.7.2). However, the configuration has to be done by using the initial configured module address of the SMI720 (11001b).

It is not possible to operate two sensors with the same BUSADR (4:3) on one CSB line. This failure which might lead to two sensors driving the same MISO line must be avoid by ECU design.

Req_259 Channel address BUSADR(2:0) = 000b [MODULE-BROADCAST] is forbidden, if there are more than one device connected to the same CHIP-SELECT-line. This combination can only be used in a **Single Module-System** or during production.

BUSADR(4)	BUSADR(3)	BUSADR(2)	BUSADR(1)	BUSADR(0)	Meaning
*	*	0	0	0	Module-broadcast
1	1	0	0	1	Module-address
1	1	0	1	0	RATE X, LF
1	1	0	1	1	not used
1	1	1	0	0	ACC Z, LF
1	1	1	0	1	not used
1	1	1	1	0	ACC Z, LF
1	1	1	1	1	not used
1	0	*	*	*	SMI710a
0	1	*	*	*	SMI700b
0	0	*	*	*	SMI700a

Req_915 The Safety-IDs are individually configurable via SPI commands during each startup of the ECU.

Sensor-Channel	BUS-Address (5 bit)	SID-Address (5 bit)
Angular Rate (x-Axis, LF)	11010b	configurable (default: 11010b)
Acceleration (z-Axis, LF)	11100b	configurable (default: 11110b)
Acceleration (z-Axis, LF)	11110b	configurable (default: 11110b)

Hints:

BUS-Addresses of acceleration channel: The two bus addresses '11100b' and '11110b' address the very same acceleration channel. This single acceleration channel has also one single SID.

Factory Addressing: Since 10bit address range will be too small for the complete sensor internal address range, this section proposes a way to address a wide space. After writing the password, the last address will be masked by an internal register representing the higher bits of the address. With this a paging mode can be used to cover a wider address space. If different commands are needed to speed up end of line calibration, they should be defined by the sensor manufacturer.

Req_227 Correct configuration of module ID BUSADR 4:3 of the SMI720 in an ECU SPI bus system must be guaranteed by the ECU system if those addresses will be changed. The channel addresses (BUSADR 2:0) cannot be changed by the customer.

4.3.6 OpenSPI32 Protocol

Req_231 The OpenSPI32 protocol is an out-of-frame SPI protocol. This means the logical response to a command is transmitted in the next clock cycle of a frame.

Req_233 The general format of the OpenSPI is defined as:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					x																						CRCR			*	
MISO	SID(4:0)					x	SD		x		BE	x																CRCA				

Req_234 The sensor data command is defined as:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					CAP(2:0)			MOD=0	*																		CRCR			*	
MISO	SID(4:0)					TE	SD=1		CI	BE	INI	*																SENSORDATA(15:0)			CI	CRCA

Req_235 The sensor module command is defined as:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					ADR(3:0)				W	*	W-DATA(15:0)																CRCR			*	
MISO	BUSADR(4:0)					TE	SD=0		*	BE	*	PAGE(2:0)			R-DATA(15:0)														CRCA				

Req_236 If the sensor receives a sensor command where MOD (bit 23) is set to "1" it will send the following answer at MISO within the next frame (Conti command).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					CAP(2:0)			MOD=1	*																		CRCR			*	
MISO	0	0	0	0	*	*	ST		SENSORDATA(15:0)																BUSADR(4:0)					CRCA				

Req_2024 *: in case of receiving a message, bits must be ignored
in case of transmitting a message, bits can be 0 or 1, but CRC has to be adapted accordingly.

Req_2025 X: this is a placeholder describing bits which are defined with the module and sensor data commands differently.

Req_258 BUSSADR(4:0): This is the 5bit bus address which addresses each sensor and all channels. The bus address can be either a module or a channel address.

Req_2035 CAP(2:0): defines for all modules on the bus the capture mechanism (details see also below)
011b: read current data and channel information (do not alter captured data)
010b: read captured data and channel information
(do not capture or alter captured data)
101b: sensor channels of any module on the bus will capture data and channel information of all channels. (Capture is also done in case of invalid BUSADR)
Only channel with valid BUSADR: read capture data of selected channel afterwards
else: reserved (illegal command)

Req_2022 MOD: Selects safing ASIC Mode
0: not selected (standard response)
1: selected (Conti command)

Req_2030 ADR(3:0): Address of data to be read or to be written (details see below)

Req_2029 W: Bit identifies if address access is a write or read access
0: read data from address
1: write data from address
(Writing to a read only register gives OE (off frame error) in next frame)

Req_2034 W-DATA(15:0): w=1: Data to be written at specific address
w=0: See section "Command Addressing" for details

Req_2050 SID(4:0): safety ID (=channel ID)
Default value: SID_az=11110b, SID_Ωx=11010b
This value depends on the sensor channel. Each sensor channels SID (rate and acceleration channel) is configurable to an arbitrary 5bit value by the customer

Req_2026 SENSORDATA(15:0): These are the 16bit sensor data given in 2's complement

Req_2020 TE: Time Error
0: OK
1: Sensor internal APB-bus-access not finished between 2 SPI-frames

Req_2028 SD: Sensor Data identifies the type of the response
0: represents a module command (non sensor data command)
1: represents a sensor data command

Req_2027 CI: Channel Information (status) bit
0: sensor channel sensor data fully valid
1: channel sensor data not valid
(sensor error, initialization, self test, fast offset cancelation running, ...)

A-samples: If captured data is read, CI is the captured CI.
C-samples: If captured data is read, CI is the disjunction (OR) of the captured CI and the current CI.

Req_2021 BE: Bus Error
0: OK
1: Internal bus-access-error or illegal address or register not writable

A general description of this error case could be: "Unknown command with correct CRC."

Req_252 INI: Signals if the sensor is in initialization or self test mode
0: sensor in normal operation
1: sensor is in initialization or self test mode
If captured data is read, then the INI-bit represents the state when data were captured.

Req_2037 PAGE(2:0): page number from which data is read or written to (details see below)

Req_2033 R-DATA(15:0): Data read from specific address. If W=1 and new data is written to a register, R-DATA holds the content of the address before writing to it.

Req_2023 ST: Sensor Status
00: not used
01: channel sensor data fully valid
10: channel sensor data not valid (self test or offset cancellation)
11: channel sensor data not valid (sensor error)
If captured data is read, then the ST-bits are the captured ST.

Req_2036 CRCR(2:0): CRC checksum over bits 31 to 5 (details on calculation see below)

Req_275 CRCA(2:0): CRC checksum over bits 31 to 3 (details on calculation see below)

Req_1983 The sensor will not send any response (high-impedance at MISO) for the following error conditions:
- CRCR is wrong
- sck-count-error: number of SCK-clocks not equal to 32
- CPOL-error: actual sampled SCK-level with rising-edge of CSB is not equal to CPOL
- bus address which is not used in SMI720

Please note: CPHA errors are not detected.

4.3.7 CC32IN SPI Protocol

Req_238 The CC32IN protocol is an in-frame SPI protocol. This means the logical response to a command is transmitted in the same clock cycle of a frame.

Req_240 The general format of the CC32IN is defined as:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					x																						CRCR			*	
MISO	TRI					OE	SD	x																						CRC/TF		

Req_241 The sensor data command is defined as:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					CAP(2:0)			*	ADR(4:0)					*													CRCR			*	

MISO	TRI	OE	SD=1	SID(4:0)	SENSORDATA(15:0)	CI	CRC/TF

Req_242 The sensor module command is defined as:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					ADR(3:0)				W	*	W-DATA(15:0)																CRCR			*	
MISO	TRI					OE	SD=0	MID(2:0)			PAGE(2:0)	R-DATA(15:0)																CRC/TF					

Req_971 *: in case of receiving a message, bits must be ignored
in case of transmitting a message, bits can be 0 or 1, but CRC has to be adapted accordingly.

Req_244 X: this is a placeholder describing bits which are defined with the module and sensor data commands differently.

Req_2031 BUSSADR(4:0): This is the 5bit bus address which addresses each sensor and all channels.
The bus address can be either a module or a channel address.

Req_283 CAP(2:0): defines for all modules on the bus the capture mechanism (details see also below)
011b: read current data and channel information (do not alter captured data)
010b: read captured data and channel information
(do not capture or alter captured data)
101b: sensor channels of any module on the bus will capture data and channel information of all channels. (Capture is also done in case of invalid BUSADR)
Only channel with valid BUSADR: read capture data of selected channel afterwards
else: reserved (illegal command)

Req_1199 ADR(4:0): Only used for backward compatibility in previous generations Bosch passive safety systems. Should be set to 00000b for all other systems.
If the 16 bit ADR is identical to a programmed channel address, the sensor will respond off-frame with a special 16-bit frame.
See section "Backward Compatibility: Special 16 bit Mode" for details.

Req_1202 ADR(3:0): Address of data to be read or to be written (details see below)

Req_254 W: Bit identifies if address access is a write or read access
0: read data from address
1: write data from address
(Writing to a read only register gives OE (off frame error) in next frame)

Req_256 W-DATA(15:0): w=1: Data to be written at specific address
w=0: See section "Command Addressing" for details

Req_245 TRI: this represents tri state bits which are bits which are high impedance at the MISO.

Req_1198 OE: Off frame error
0: no error has happened in previous frame

1: error has happened in previous frame
(Last write bus access on APB bus not successful or sclk-cycles not equal 32)
Note: If the next frame after a write is sensor-command the information of the write status will be lost. It will only be visible in an immediately following non-sensor command.

Req_251 SD: Sensor data identifies the type of the response
0: represents a module command (non sensor data command)
1: represents a sensor data command

Req_249 SID(4:0): safety ID (=channel ID)
Default value: SID_az=11110b, SID_Ωx=11010b
This value depends on the sensor channel. Each sensor channels SID (rate and acceleration channel) is configurable to an arbitrary 5bit value by the customer

Req_246 SENSORDATA(15:0): These are the 16bit sensor data given in 2's complement

Req_248 CI: Channel Information (status) bit
0: sensor channel sensor data fully valid
1: channel sensor data not valid
(sensor error, initialization, self test, fast offset cancelation running, ...)

A-samples: If captured data is read, CI is the captured CI.
C-samples: If captured data is read, CI is the disjunction (OR) of the captured CI and the current CI.

Req_247 MID(2:0): Module ID to identify which module responded
MID(2:1) = BUSADR(4:3)
MID(0) = BUSADR(0)
1: reaction on individual module command
0: reaction on broadcast command
(e.g. used during final measurement in order to simplify the communication)

Req_2038 PAGE(2:0): page number from which data is read or written to (details see below)

Req_2032 R-DATA(15:0): Data read from specific address. If W=1 and new data is written to a register, R-DATA holds the content of the address before writing to it.

Req_273 CRCR(2:0): CRC checksum over bits 31 to 5 (details on calculation see below)

Req_274 CRC/TF(2:0): CRC checksum over bits 26 to 3 (details on calculation see below)
If CRC of request (MOSI) was wrong or command is unknown or a read access on the sensor internal APB bus failed a transfer failure will be signaled by destroying the CRC of the response (MISO). The last bit of the valid CRC will be inverted.

Req_1984 The sensor will not send any response (high-impedance at MISO) for the following error conditions:
- CPOL-error : polarity of SCK-Pin is sampled at each falling-edge of CSB.
If the sampled value is not equal to the setting of CPOL error condition is set.
- bus address which is not used in SMI720

Please note: CPHA errors are not detected.

4.3.7.1 Backward Compatibility: Special 16 bit Mode

Req_279 The bits ADR(4:0) are foreseen for passive safety systems using old generations Bosch safing devices. ADR(4:0)must be set to 00000b for all other systems.

The BUSADR is ignored for these bits (all sensors on a bus listen to these bits and check it with the CRC). If this value is not equal 00000b (and MOSI CRC is correct) the next SPI frame will be ignored by all sensors (MOSI and number of clock pulses ignored). Only the sensors whose channel address equals this 16BITADR address, this channel responds in the next frame with the special 16bit frame. Only one channel can be read with this mechanism (if other channels are also necessary, they have to be “ordered” with another 32 bit message).

Req_280 If the 16 BITADR in the previous 32-bit frame is identical to a valid channel-address, the sensor will respond with a special 16 bit frame. The data on MOSI will be ignored by all sensors on the bus.

The 16-bit frame has the following format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*															
0	0	S	SID(2:0)			DATA*(15:6)									

S status of channel (as status of channel for normal channel commands)

SID(2:0) Safety ID (SID) = channel ID (lowest 3 bit)

DATA*(15:6) upper 10 bit of channel current data clipped to +/-480 LSB (referred to 10 bit).
No captured data will be read in backward compatibility mode.

4.3.8 Addressing in OpenSPI32 and CC32IN

4.3.8.1 Command Addressing

Req_262 Each module command consists of an address which is used to decode the command. The lower bits of the command are given in each command. The higher bits are sensor internally stored and can be altered with a special command. The higher bits are called page. Only the lowest 8 pages can be used during normal operation. All other pages are sensor internally and can only be accessed using password mechanisms.

Req_263 ADR(3:0) are the lower bits of the module command address of data to be read or written.

Since only 16 registers can be accessed with ADR(3:0), a paging mechanism is implemented.

Req_264 PAGE (2:0): identifies page number from which data is read or written to

0 = page 0 (0x0000)
1 = page 1 (0x0001)
2 = page 2 (0x0002)
3 = page 3 (0x0003)
4 = page 4 (0x0004)
5 = page 5 (0x0005)
6 = page 6 (0x0006)
7 = page 7 (0x0007)

If for any reason access to the full internal register range is required (e.g. because the needed information is not available within the pages) two passwords for the access to the full internal registers

range 0x4000_0000 - 0x4000_19FC can be provided to a Robert Bosch GmbH internal customer. The passwords must not be disclosed outside Robert Bosch GmbH.

Req_265 **Mechanism for page addressing:**

A subset of the internal address space of the SMI720 can be accessed without password. The addresses are defined by 8 pages (7:0) that are selected with a 3 bit index W-DATA (2:0). The mapping scheme is implemented in the SPI module. These addresses are reserved for this mapping purpose and will not be used otherwise. The 8 pages are selected by the offset W-DATA (2:0). The page change is activated by W-DATA 15 = 1 (Bit-Pos 20 = 1). W-DATA (9:3) needs to be zero, W-DATA (14:10) (Bit-Pos 19:15) are don`t care bits.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					ADR(3:0)				W	*	W-DATA 15	x	x	x	x	x	0	0	0	0	0	0	0	W-DATA(2:0)			CRCR			*	

If a page change has to be done, W-bit (Bit-Pos 22) has to be 0. Otherwise the command will be interpreted as write access to the currently selected register.

CC32IN SPI:

When changing a page, the response data (in frame) to the page changing request belong to the previous selected page register. For the next read/write access the new page and page ID is selected. Since a page switching command is also a valid "read" module command it is possible to read an address from the current page and switch to a new page within one command. Page switching will also be executed if the CRC of the requesting MOSI frame is wrong (however the detected wrong CRC will be indicated by a TF error).

Description of CC32 behaviour:

Bit 22: R/W command bit, "0" for module read command

Bit 20: W-DATA(15), "1" as identifier for page switching command (otherwise normale read command is executed)

Bits 19...8: W-DATA(9...3), must be "0". Otherwise an Off-frame Error (OE) will be signalized in the subsequent MISO frame and the page will not be changed (unless the "password for offset addressing" is provided).

Bits 7...5: W-DATA(2...0) New Page - Number of new page to be set.

OpenSPI32:

When changing a page, the response data (out of frame) to the page changing request belong to the new selected page register. Page switching will also be executed if the CRC of the requesting MOSI frame is wrong (however the detected wrong CRC will be indicated by a high impedance).

Description of openSPI32 behaviour:

Bit 22: R/W command bit, "0" for module read command

Bit 20: W-DATA(15), "1" as identifier for page switching command (otherwise normale read command is executed)

Bits 19...8: W-DATA(9...3), must be "0".

Bits 7...5: W-DATA(2...0) New Page - Number of new page to be set.

Mechanism with full access to the internal address space:

The full access to the internal address space can only be used if the passwords Offset_Addressing_Password1 and Offset_Addressing_Password2 within page 3 (ID 0xC and 0xD) have been sent.

The sensor internal 32-bit APB address is created by a fixed offset, which targets the inframe capable APB section of the bus structure (0x4000_0000 - 0x4000_19FC) and fields from the SPI request frames.

These fields are the offset-value, extracted from WDATA (9:0) in case W-bit equals "Read", and the 4-bit address ADR (3:0) from the SPI-command. W-bit has to be 0 and W-DATA15 = 1 if a Register of the internal address space is selected. W-DATA (14:10) (Bit-Pos 19:15) are don`t care bits.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	BUSADR(4:0)					ADR(3:0)				W	*	W-DATA 15	x	x	x	x	x	W-DATA(9:0)										CRCR			*	

The register address of the internal address space is generated in following way:

31 ... 16	15 ... 6	5 ... 2	1 ... 0
0x4000	W-DATA9 ... W-DATA0	ADR3 ... ADR0	00 bin

The new offset address becomes valid starting with the next SPI access.

When BUSADR(4:0) and ADR(3:0) are being received, the decoder will generate the internal address and will start the bus access to get the data in time to be sent out in R-DATA of the same frame, independent of the subsequent bits in MOSI.

If the passwords has not been provided the requested OFFS value >7 (WDATA9 - WDATA0) is ignored by the SPI and the last selected page is addressed. If the passwords have been sent successfully and a internal address is selected, the PAGE (2:0) bits in MISO response will be set to 7.

It can be tested by reading the currently selected page, if the passwords have been sent and understood incorrectly by the SMI720. The SPI changes the page address to 7dec if the full address space is accessed. The change of the initial page (except if page 7 was already selected) to page 7 can be observed by the SPI-master.

CC32IN SPI:

When changing a internal register address, the response data (in frame) to the register address changing request belong to the previous selected register address. For the next read/write access the new register address is selected. Since a page switching command is also a valid "read" module command it is possible to read an address from the current page and switch to a new page within one command. Page switching will also be executed if the CRC of the requesting MOSI frame is wrong (however the detected wrong CRC will be indicated by a TF error).

OpenSPI32:

When changing a internal register address, the response data (out of frame) to the register address changing request belong to the new selected register address. Page switching will also be executed if the CRC of the requesting MOSI frame is wrong (however the detected wrong CRC will be indicated by a high impedance).

The described paging mechanism is the same as used in SMI700/710.

Req_267 Data which were assumed to be used quite often during operation were placed in the first page (page 0).

Req_268 The data finally needed by a system will be as small as possible to minimize communication load (especially the error flags to be read during to discriminate errors application should be minimized, if possible less than 16 single bits). A cluster flag which summarizes the internal error state of the sensor was implemented.

Req_269 Three pointer which are individual configurable at final test of SMI720 were implemented to offer a flexible way to address internal registers which are currently not available within the pages. Changes of

the implemented register information within the pages need a redesign of the digital part which requires more than a metal mask.

Req_270 If the address is not the sensor module address (11001b) the sensor interprets the command as sensor channel command. If a invalid channel was selected the answer of the SMI720 will be high-Z.

4.3.8.2 Functions Provided via 32bit Pages

Req_288 The following functions and information are accessible over CC32 and open SPI protocol via the paging mechanism (additional to the sensor signals):

The following address pages contain information on the available functions and information and their addresses.

r/w describes if the register has only read access (r) or read and write access (r/w):

The tables below represent the sensor behavior in A-Sample state. In C-Sample state the page mapping will change according to CR018, CR019 and CR022.

For Offset values 0...7 the following pages are defined:

Page 0

Offset	r/w	ID	Function/Target Register
0	r	0x0	channel_status_hw_scon
0	r	0x1	Offset-controller state
0	r	0x2	Cluster Flag
0	r	0x3	Serial number of customer
0	r	0x4	Revision of ASIC (e.g. AA)
0	r/w	0x5	SID_RATE_LF config SID_ACC1_LF config
0	r/w	0x6	Reset Vector
0	r/w	0x7	Trigger Bite
0	r/w	0x8	Trigger Offset Controller
0	r/w	0x9	Trigger Reset
0	r/w	0xA	Trigger register CRC check
0	r/w	0xB	Write reference CRC for cyclic register check
0	r	0xC	Read actual CRC of cyclic register check
0	r	0xD	Max limit for external frequency monitoring
0	r	0xE	Min limit for external frequency monitoring
0	r	0xF	Auto Calibration Data

Page 1

Offset	r/w	ID	Function/Target Register
1	r	0x0	PLL_ICO_OUT
1	r	0x1	RATE_FEEDBACK
1	r	0x2	QUAD_I
1	r	0x3	DRV_DAC_OUT
1	r	0x4	QUAD_HF
1	r	0x5	TEMP1 (Temp1 Signal from DSP)
1	r	0x6	TEMP2 (Temp2 Signal from DSP)
1	r	0x7	scon_adc_ucm_yaw
1	r	0x8	scon_adc_ucm_acc1
1	r	0x9	scon_adc_temp1
1	r	0xA	scon_adc_temp2
1	r	0xB	scon_adc_det_cncp
1	r	0xC	scon_adc_fb_mux
1	r	0xD	scon_adc_udf_det
1	r	0xE	spi_counter @ PLL-frequency (actual counter value)
1	r	0xF	Cluster Flag

Page 2

Offset	r/w	ID	Function/Target Register
2	r	0x0	channel_status_hw_scon
2	r	0x1	error_flag_16_bank0
2	r	0x2	error_flag_16_bank1
2	r	0x3	error_flag_16_bank2
2	r	0x4	error_flag_16_bank3
2	r	0x5	error_flag_16_bank4
2	r	0x6	error_flag_16_bank5
2	r	0x7	error_flag_16_bank6

Page 3

Offset	r/w	ID	Function/Target Register
3	r/w	0x0	DSP-Flush-Time (read/write of the dsp flush-time)
3	r/w	0x1	YR_LF Counter config (read/write of the error counter limit)
3	r/w	0x2	QUAD_HF Counter config (read/write of the error counter limit)
3	r/w	0x3	ACC1_LF Counter config (read/write of the error counter limit)
3	r/w	0x4	ADDR_P1 (address pointer 1)
3	r/w	0x5	ADDR_P2 (address pointer 2)
3	r/w	0x6	ADDR_P3 (address pointer 3)
3	r/w	0x7	DEBUG_CONTROL

2	r	0x8	error_flag_16_bank7
2	r	0x9	error_flag_16_bank8
2	r	0xA	YR_LF counter value
2	r	0xB	QUAD_HF counter value
2	r	0xC	ACC1_LF counter value
2	r	0xD	SPI state (SPI errors)
2	r	0xE	*A-samples:* Offset-controller state *C-samples:* TEMP1 (duplicate page1 0x5)
2	r	0xF	Cluster Flag

3	r	0x8	DEBUG_OUT_1
3	r	0x9	DEBUG_OUT_2
3	r	0xA	DEBUG_OUT_1_2_CAPTURED
3	r	0xB	DEBUG_COUNTER_CAPTURED
3	r/w	0xC	PW 1 for offset addressing
3	r/w	0xD	PW 2 for offset addressing
3	r/w	0xE	password 1 for 64 bit SPI
3	r/w	0xF	password 2 for 64 bit SPI

Page 4

Offset	r/w	ID	Function/Target Register
4	r	0x0	Serial number programmed at electrical wafer sort part 1
4	r	0x1	Serial number programmed at electrical wafer sort part 2
4	r	0x2	Serial number programmed at electrical wafer sort part 3
4	r	0x3	Name of ASIC (TIG720)
4	r	0x4	Revision of ASIC (e.g. AA)
4	r	0x5	Serial number of SMI part 0
4	r	0x6	Serial number of SMI part 1
4	r	0x7	Serial number of SMI part 2
4	r	0x8	Serial number of customer
4	r	0x9	upper 16 bit of last read access
4		0xA	*A-samples:* Not used *C-samples:* DUMMY_ADDR_REG1
4		0xB	*A-samples:* Not used *C-samples:* DUMMY_ADDR_REG2
4		0xC	*A-samples:* Not used *C-samples:* TC Rate Bite |POS-NEG|
4		0xD	*A-samples:* Not used *C-samples:* TC Quad Bite |POS-NEG|
4		0xE	*A-samples:* Not used *C-samples:* TC ACC Bite |POS-NEG|
4		0xF	*A-samples:* Not used *C-samples:* Bite Config

Page 5

Offset	r/w	ID	Function/Target Register
5	r	0x0	LAST_BITE_ACC1_POS
5	r	0x1	LAST_BITE_ACC1_NEG
5	r	0x2	LAST_BITE_QUAD_YR_POS
5	r	0x3	LAST_BITE_QUAD_YR_NEG
5	r	0x4	LAST_BITE_QUAD_YR_ZERO
5	r	0x5	LAST_BITE_RATE_YR_POS
5	r	0x6	LAST_BITE_RATE_YR_NEG
5	r	0x7	LAST_BITE_RATE_YR_ZERO
5	r	0x8	New part value Quad Bite POS
5	r	0x9	New part value Quad Bite NEG
5	r	0xA	New part value Quad Bite |POS-NEG|
5	r	0xB	New part value Rate Bite |POS-NEG|
5	r	0xC	New part value ACC1 Bite |POS-NEG|
5	r	0xD	BITE_REP_CNT_YRS_ACC
5	r	0xE	Bite_state_yrs_acc
5	r	0xF	Cluster Flag

Page 6

Offset	r/w	ID	Function/Target Register
6		0x0	*A-samples:* Not used *C-samples:* EOP
6		0x1	
6		0x2	
6		0x3	
6		0x4	
6		0x5	
6		0x6	
6		0x7	
6		0x8	
6		0x9	
6		0xA	

Page 7

Offset	r/w	ID	Function/Target Register
7		0x0	
7		0x1	
7		0x2	
7		0x3	
7		0x4	
7		0x5	
7		0x6	
7		0x7	
7		0x8	
7		0x9	
7		0xA	

6		0xB	
6		0xC	
6		0xD	
6		0xE	
6		0xF	

7		0xB	
7		0xC	
7		0xD	
7		0xE	
7		0xF	

4.3.8.2.1 Register Information for Page 0

Req_2107

page	ID	r/w	Bit	function	description	default value
0	0x0	r	1:0	ACC1_LF_STATUS_HW_SCON	Mapped to CI of ACC-channel: 00: Run Mode (no error) 01: Temporary Error / SOC off 10: Permanent Error 11: INIT or BITE / FOC running	
0	0x0	r	3:2	Yaw_Quad_HF_STATUS_HW_SCON	Mapped to CI of RATE-channel: 00: Run Mode (no error) 01: Temporary Error / SOC off 10: Permanent Error 11: INIT or BITE / FOC running	
0	0x0	r	5:4	Yaw_Rate_LF_STATUS_HW_SCON	Mapped to CI of RATE-channel: 00: Run Mode (no error) 01: Temporary Error / SOC off 10: Permanent Error 11: INIT or BITE / FOC running	

Req_2110

page	ID	r/w	Bit	function	description	default value
0	0x1	r	0	rate_slow_offset_controller_active		
0	0x1	r	1	acc_slow_offset_controller_active		
0	0x1	r	2	rate_fast_offset_controller_active		
0	0x1	r	3	acc_fast_offset_controller_active		

Req_2109

page	ID	r/w	Bit	function	description	default value
0	0x2	r	15:0	cluster_flag		

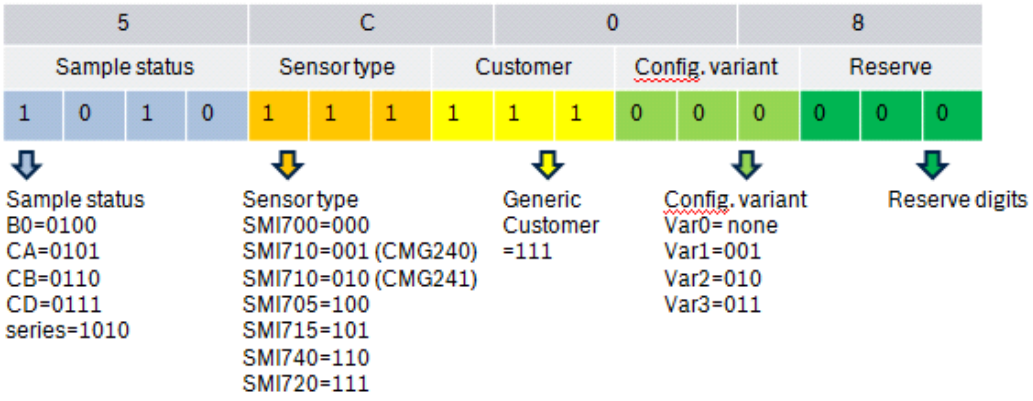
0	clu_ST_OR_FOC_RUNNING
1	clu_INIT
2	clu_MECH_OVERLOAD_ACC
3	clu_ST_FAILED
4	clu_PIN_OR_BOND_FAILURE
5	clu_TEMP
6	clu_SUPPLY
7	clu_EMC_PSRR
8	clu_MECH_OVERLOAD_RATE
9	clu_DIGITAL
10	clu_OTP_System
11	clu_DSP
12	clu_MEMORY
13	clu_ACC_DETECTION
14	clu_RATE_DETECTION
15	clu_RATE_DRIVE

Clear by read mechanism implemented. Cluster flag information is ASIC internally latched until next read access.

Req_2111

page	ID	r/w	Bit	function	description	default value
0	0x3	r	15:0	Serial number of customer		0xAFC0

For SMI720 a generic default value (0xAFC0) according to following definition is used for this register:



Req_2112

page	ID	r/w	Bit	function	description	default value
0	0x4	r	7:0	Revision-ID of TIG720	Revision of ASIC (0x00=AA, 0x10=BA, 0x11=BB, ..)	

For TIG720AA (SMI720 A0-samples) default value of the revision ID is 0x00.
For TIG720BA (SMI720 C0-samples) default value of the revision ID is 0x10.
For TIG720BB (SMI720 C0-samples) default value of the revision ID is 0x11.
For TIG720BC (SMI720 C1-samples) default value of the revision ID is 0x12.

Req_2114

page	ID	r/w	Bit	function	description	default value
0	0x5	r/w	4:0	SID_ACC		0x1E
0	0x5	r/w	9:5	SID_RATE		0x1A

Req_2115

page	ID	r/w	Bit	function	description	default value
0	0x6	r/w	0	BA3	Bit three of SPI sensor address BUSADR.	0x1
0	0x6	r/w	1	BA4	Bit four of SPI sensor address BUSADR.	0x1
0	0x6	r/w	2	SPI_AUTOCALIB_EN	Automatic calibration of SPI slave parameters.	0x1
0	0x6	r/w	3	SO_DRIVER*	SO pad driver strength.	0x1
0	0x6	r/w	4	SPI_CPOL	SPI clock polarity parameter CPOL.	0x0
0	0x6	r/w	5	SPI_CPHA	SPI clock phase parameter CPHA.	0x0
0	0x6	r/w	6	SPI_PROT_SELECT	SPI protocol CC32in (bit=0) or OpenSPI (bit=1).	0x0

*SO_DRIVER is configured by default to 0x1, which selects the strong driver mode. All SPI-timing specifications are only valid with a selected strong driver mode. The weak drive mode (SO_DRIVER = 0x0) is only implemented as a backup in case of EMC problems and is not intended to be used by the customer. The weak driver mode is not evaluated, therefore no SPI timings for this mode can be guaranteed.

Req_2118

page	ID	r/w	Bit	function	description	default value
0	0x7	r/w	1:0	bite_acc_control_code	00: BITE ACC off 01: Static BITE ACC_POS 10: Static BITE ACC_NEG 11: BITE Sequence ACC on	0x0
0	0x7	r/w	10:8	bite_yrs_control_code	000: BITE YRS off 001: Static BITE YRS_POS 010: Static BITE YRS NEG 011: Static BITE YRS Zero 1xx: BITE Sequence YRS on	0x0

A manual BITE-trigger request is available within CC32 and Open-SPI protocol. Manual BITE-trigger request will be able to trigger all possible BITE states (pos, neg, zero) constantly and the automatic BITE sequence for each channel.

Req_2119

page	ID	r/w	Bit	function	description	default value
0	0x8	r/w	1:0	HW_CTRL_RATE_OFF_EN	Offset-Controller Rate-channel: 00/11: Nop 01: fast offset cancelation ON 10: slow offset cancelation ON	0x0
0	0x8	r/w	3:2	HW_CTRL_ACC_OFF_EN	Offset-Controller ACC-channel: 00/11: Nop 01: fast offset cancelation ON 10: slow offset cancelation ON	0x0

The fast and slow offset controller is triggerable with CC32 and Open-SPI.

Req_2120

page	ID	r/w	Bit	function	description	default value
0	0x9	r/w	15:0	SOFT_RESET	Soft reset is activated by SPI if password value 0xB26C is written	0x0

A Reset will be triggerable with CC32 and Open-SPI. The SPI reset will lead to a full reset of TIG720, identically to a hard reset over reset pin.

Req_2121

page	ID	r/w	Bit	function	description	default value
0	0xA	r/w	0	CYC_CRC_CALC_EN	Cyclic CRC Calculate Enable. Once Enabled, service is calculating the CRC of registers until this bit is cleared.	0x1
0	0xA	r/w	1	CYC_CRC_COMP_EN	Cyclic CRC Compare Enable. If this bit is set, then block will compare the calculated CRC with reference CRC. The result will be reported as boot_cyc_invalid_crc flag.	0x1

This values must not be changed by the customer. The monitor is part of the safety-concept.

Req_2122

page	ID	r/w	Bit	function	description	default value
0	0xB	r/w	15:0	CYC_CRC_REF_CRC	Unsigned 16bit reference CRC for cyclic register check which is compared to the calculated CRC. If the reference and calculated value are not equal an error flag is set.	

Req_2123

page	ID	r/w	Bit	function	description	default value
0	0xC	r	15:0	CYC_CRC_CAL_CRC	Unsigned 16bit calculated CRC by cyclic register check over selected registers.	

Req_2124

page	ID	r/w	Bit	function	description	default value
0	0xD	r	15:0	**A-samples:** Frequ_Check_Max_Limit **C-samples:** Frequ_Check_reference_value	**A-samples:** Maximum limit for external frequency monitoring. The limit is referred to a difference of the spi_counter value within a time interval of 5ms. 16Bit unsigned. **C-samples:** Part individual reference value for CMG-frequency monitor (external). Unsigned 16Bit value, no fractional part.	

Typical value for c-samples could be 25000 dez = 0x61A8. This value will always stay between 23500 dez and 27500 dez (limits of process related distribution for the CMG-frequency).

Req_2125

page	ID	r/w	Bit	function	description	default value
0	0xE	r	15:0	A-samples: Frequ_Check_Min_Limit C-samples: Frequ_Check_tc	A- samples: Minimum limit for external frequency monitoring. The limit is referred to a difference of the spi_counter value within a time interval of 5ms. 16Bit unsigned. C-samples: Part individual temperature coefficient (TC) for calculation of temperature compensated reference value (CMG frequency monitor). Temperature coefficient for manual rate bite evaluation. Signed 16Bit value with 14Bit fractional part.	

This value has to be used as a signed value with 14 fractional bits. A calculation method for a correct interpretation could be:

```
if Frequ_Check_tc > (2^15 -1) then

        Frequ_Check_tc = (Frequ_Check_tc - 2^16)/2^15
else
        Frequ_Check_tc = Frequ_Check_tc / 2^15
end
```

A typical value when calculation was done for c-samples could be -0.029144287109375.

Req_2126

page	ID	r/w	Bit	function	description	default value
0	0xF	r	3:0	AutoCalibrationData		

0	SPI_CPOL	SPI clock polarity parameter CPOL.
1	SPI_CPHA	SPI clock phase parameter CPHA.
2	SPI_PROT_SELECT	SPI protocol CC32in (bit=0) or OpenSPI (bit=1).
3	SPI64_PROT_SELECT	SPI64 protocol is selected.

This register information shows the autocalibrated values of the SPI after successful written calib command.

4.3.8.2.2 Register Information for Page 1

Req_2127

page	ID	r/w	Bit	function	description	default value
1	0x0	r	8:0	PLL_ICO_OUT	Unsigned 9bit output to Oscillator DAC.	

Req_2128

page	ID	r/w	Bit	function	description	default value
1	0x1	r	3:0	RATE_FEEDBACK	Unsigned 4bit Output of the quantizer to the feedback path	

Req_2129

page	ID	r/w	Bit	function	description	default value
1	0x2	r	15:0	QUAD_I_VALUE	Signed 16bit value of QUAD_I (Output of quadrature controller)	

Req_2130

page	ID	r/w	Bit	function	description	default value
1	0x3	r	7:0	DRV_DAC_OUT	Unsigned 8bit Output to Drive DAC	

Req_2131

page	ID	r/w	Bit	function	description	default value
1	0x4	r	15:0	QUAD_HF	Signed 16bit Quad_HF signal of quadrature channel	

Req_2132

page	ID	r/w	Bit	function	description	default value
1	0x5	r	15:0	TEMP_SENSOR_1_VALUE	Signed 16bit value of temperature sensor 1 (DSP)	

To calculate a real temperature value the following equaion can be used (only nominal value, no specification guaranteed):

Temperature [°C] = 32.5°C + TEMP_SENSOR_1_VALUE [LSB] / 200 [LSB/°C]

Req_2133

page	ID	r/w	Bit	function	description	default value
1	0x6	r	15:0	TEMP_SENSOR_2_VALUE	Signed 16bit value of temperature sensor 2 (DSP)	

Req_2134

page	ID	r/w	Bit	function	description	default value
1	0x7	r	11:0	scon_adc_ucm_yaw	Unsigned 12bit value of Rate CM voltage over SCON ADC.	

Req_2135

page	ID	r/w	Bit	function	description	default value
1	0x8	r	11:0	scon_adc_ucm_acc1	Unsigned 12bit value of ACC CM voltage over SCON ADC.	

Req_2136

page	ID	r/w	Bit	function	description	default value
1	0x9	r	11:0	scon_adc_temp1	Unsigned 12bit value of temp1 voltage over SCON ADC.	

Req_2137

page	ID	r/w	Bit	function	description	default value
1	0xA	r	11:0	scon_adc_temp2	Unsigned 12bit value of temp2 voltage over SCON ADC.	

Req_2138

page	ID	r/w	Bit	function	description	default value
1	0xB	r	11:0	scon_adc_det_cncp	Unsigned 12bit value of cncp voltage over SCON ADC.	

Req_2139

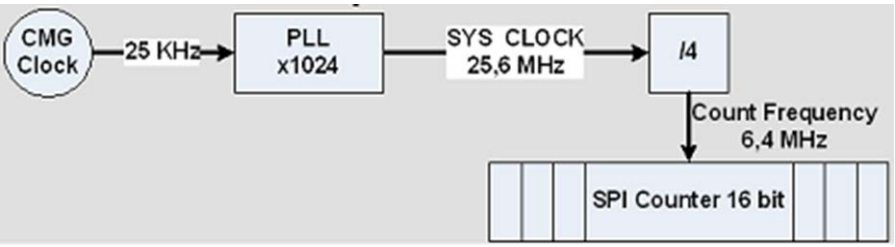
page	ID	r/w	Bit	function	description	default value
1	0xC	r	11:0	scon_adc_fb_mux	Unsigned 12bit value of fb voltage over SCON ADC.	

Req_2140

page	ID	r/w	Bit	function	description	default value
1	0xD	r	11:0	scon_adc_udf_det	Unsigned 12bit value of udf voltage over SCON ADC.	

Req_2141

page	ID	r/w	Bit	function	description	default value
1	0xE	r	15:0	SPI_COUNTER	Unsigned value of free running counter based on pll frequency.	



Calculation of the CMG frequency can be done by reading two SPI_COUNTER values [counter@t1;counter@t2] within a know time intervall Δt. Because of using a free running counter, the counter overflow has to be considered by calculation the CMG frequency evaluating if counter@t1 < counter@t2.

If counter@t1 < counter@t2 (no counter overflow): Δcounter = counter@t2-counter@t1

If counter@t1 > counter@t2 (counter overflow): Δcounter = 2^16-counter@t1+counter@t2

fcmg = (Δcounter)*4/(Δt*1024)

The calculations above assume, that the time intervall Δt is not larger than (including timing tolerances of the ECU):

(2^16*4) / (1024 * fCMG) = **9,31 ms** (@fCMG = 27,5 KHz)

A-samples: A time intervall Δt of 5ms is AE proposal, because it is used for the calculation of the frequency monitor limits. If the frequency monitoring is used by the customer and a Δt of 5ms is used for calculation of the Δcounter value, it has to be checked that

Frequ_Check_Min_Limit < Δcounter < Frequ_Check_Max_Limit.

C-samples: A time intervall Δt of 5ms is AE proposal, because it is used for the calculation of the frequency new part value and temperature coefficient.

If the frequency monitoring is used including a temperature compensation of the frequency reference value, following calculation method has to be implemented (best monitor performance):

1. Read fcmg new part value and temperature coefficient (please refer to 2124 and 2125).
2. Read TEMP_SENSOR_1_VALUE as signed 16bit value (please refer to 2132 or 2160).
3. Calculate **fcmg** by reading SPI_COUNTER value as mentioned above.
4. Calculate temperature compensated reference value Frequ_Check_reference_value_comp**:**
   Frequ_Check_reference_value_comp = Frequ_Check_reference_value + (Frequ_Check_tc*TEMP_SENSOR_1_VALUE)
5. Calculate difference between Frequ_Check_reference_value_comp and fcmg:
   fcmg_diff = fcmg - Frequ_Check_reference_value_comp
6. Compare fcmg_diff to following limits (temperature compensated reference value is used):
   -30Hz < fcmg_diff < +30Hz

If no temperature compensation for the frequency reference value is applied following calculation method has to be implemented (less monitor performance):

1. Read fcmg new part value (please refer to 2124).
2. Calculate **fcmg** by reading SPI_COUNTER value as mentioned above.
3. Calculate difference between Frequ_Check_reference_value and fcmg:
   fcmg_diff = fcmg - Frequ_Check_reference_value
4. Compare fcmg_diff to following limits (no temperature compensated reference value):

-100Hz < fcmg_diff < +100Hz

Disclaimer: Limits mentioned above include only sensor effects. ECU effects with influence on fcmg calculation (e.g. time jitter of the SPI) must be considered by the application seperately and possibly lead to larger tolerance limits. If a customer wants to use frequency monitoring, a approval of sensor development department (ESI) is required to check if the limits and calculation method for frequency monitoring are still valid. This monitor function is not necessary to reach the SMI720 safety goals.

Req_2142

page	ID	r/w	Bit	function	description	default value
1	0xF	r	15:0	cluster_flag		

0	clu_ST_OR_FOC_RUNNING
1	clu_INIT
2	clu_MECH_OVERLOAD_ACC
3	clu_ST_FAILED
4	clu_PIN_OR_BOND_FAILURE
5	clu_TEMP
6	clu_SUPPLY
7	clu_EMC_PSRR
8	clu_MECH_OVERLOAD_RATE
9	clu_DIGITAL
10	clu_OTP_System
11	clu_DSP
12	clu_MEMORY
13	clu_ACC_DETECTION
14	clu_RATE_DETECTION
15	clu_RATE_DRIVE

Clear by read mechanism implemented. Cluster flag information is ASIC internally latched until next read access.

4.3.8.2.3 Register Information for Page 2

Req_2143

page	ID	r/w	Bit	function	description	default value
2	0x0	r	1:0	ACC1_LF_STATUS_HW_SCON	Mapped to CI of ACC-channel: 00: Run Mode (no error) 01: Temporary Error / SOC off 10: Permanent Error 11: INIT or BITE / FOC running	
2	0x0	r	3:2	Yaw_Quad_HF_STATUS_HW_SCON	Mapped to CI of Rate-channel: 00: Run Mode (no error) 01: Temporary Error / SOC off 10: Permanent Error 11: INIT or BITE / FOC running	
2	0x0	r	5:4	Yaw_Rate_LF_STATUS_HW_SCON	Mapped to CI of Rate-channel: 00: Run Mode (no error) 01: Temporary Error / SOC off 10: Permanent Error 11: INIT or BITE / FOC running	

Req_2144

page	ID	r/w	Bit	function	description	default value
2	0x1	r	15:0	err_flag_16_bank0		

A-samples:

	err_flag_16_bank0
0	acc_clk_ovlp
1	acc1_clk_cnt
2	acc1_ds_lim
3	acc1_overload_det
4	acc1_seq_bite
5	pc_cp
6	pc_cs1
7	pc_shd
8	pc_vdd3_vdd1_8
9	pc_vssa
10	pc_vssd
11	pc_vss_IO
12	pe_flag_cic4_err
13	pe_flag_quad_2k_err
14	pe_flag_rate_1k_err
15	acc1_pe_flag_1k_err

C-samples:

	err_flag_16_bank0
0	acc_clk_ovlp
1	acc1_clk_cnt
2	acc1_ds_lim
3	acc1_overload_det
4	acc1_seq_bite
5	pc_cp
6	pc_cs1
7	pc_shd
9	pc_vssa
10	pc_vssd
11	pc_vss_IO
12	pe_flag_cic4_err
13	pe_flag_quad_2k_err
14	pe_flag_rate_1k_err
15	acc1_pe_flag_1k_err

Clear by read mechanism implemented. err_flag_16_bank0 information is ASIC internally latched until next read access.

Req_2145

page	ID	r/w	Bit	function	description	default value
2	0x2	r	10:0	err_flag_16_bank1		

	err_flag_16_bank1
0	yrs_agc_irregular
1	yrs_drv_adc
2	yrs_cpar1_cal_drive_int
3	yrs_drv_bp_lim
4	yrs_pll_lim
5	yrs_pll_unlock
6	yrs_quad_seq_bite
7	yrs_rate_adc
8	yrs_rate_pt2_lim
9	yrs_rate_quantizer
10	yrs_rate_seq_bite

Clear by read mechanism implemented. err_flag_16_bank1 information is ASIC internally latched until next read access.

Req_2146

page	ID	r/w	Bit	function	description	default value
2	0x3	r	13:0	err_flag_16_bank2		

	err_flag_16_bank2
0	yrs_rate_v_cm
1	yrs_rate_v_com
2	yrs_rate_v_fb
3	yrs_rate_v_tn
4	acc1_v_cm
5	yrs_quad_i_tol
6	yrs_quad_hf_tol
7	yrs_drv_cu_gain
8	yrs_cpar1_cal_rate
9	yrs_pll_tol
10	yrs_drv_pi_tol
11	ctm_range
12	ctm_diff
13	dsp_online_test

Clear by read mechanism implemented. err_flag_16_bank2 information is ASIC internally latched until next read access.

Req_2147

page	ID	r/w	Bit	function	description	default value
2	0x4	r	11:0	err_flag_16_bank3		

A-samples:

	err_flag_16_bank3
0	v_acc_high
1	v_acc_low
2	v_cp_high
3	v_cp_low
4	v_ctm_high
5	v_ctm_low
6	v_dig_high
7	v_yrs_high
8	v_yrs_low
9	vdd3_high
10	vdd3_low
11	otp_vprog_limit_exceed

C-samples:

	err_flag_16_bank3
0	v_acc_high
1	v_acc_low
2	v_cp_high
3	v_cp_low
4	v_ctm_high
5	v_ctm_low
6	v_dig_high
7	v_yrs_high
8	v_yrs_low
9	vdd3_high
10	vdd3_low

Clear by read mechanism implemented. err_flag_16_bank3 information is ASIC internally latched until next read access.

Req_2148

page	ID	r/w	Bit	function	description	default value
2	0x5	r	12:0	err_flag_16_bank4		

	err_flag_16_bank4
0	ahb_hang_up
1	spi_apb_slv
2	uc_sub_apb_slv
3	misc_apb_slv
4	main_ctrl_apb_slv
5	frontend_apb_slv
6	hw_scon_apb_slv
7	dsp_rom_apb_slv
8	dsp_ram_apb_slv
9	dsp_apb_slv
10	conf_apb_slv
11	lbist_err
12	reset

Clear by read mechanism implemented. err_flag_16_bank4 information is ASIC internally latched until next read access.

Req_2149

page	ID	r/w	Bit	function	description	default value
2	0x6	r	9:0	err_flag_16_bank5		

	err_flag_16_bank5
0	boot_bus_err
1	boot_cyc_bus_err
2	boot_cyc_invalid_crc
3	boot_device_unlocked
4	boot_invalid_command
5	boot_invalid_crc
6	boot_nval_bus_err
7	boot_readback_mismatch
8	boot_unrecoverable_err
9	boot_pll_assist_bus_err

Clear by read mechanism implemented. err_flag_16_bank5 information is ASIC internally latched until next read access.

Req_2150

page	ID	r/w	Bit	function	description	default value
2	0x7	r	8:0	err_flag_16_bank6		

	err_flag_16_bank6
0	dsp_pe_dsp_status_0_err
1	dsp_pe_dsp_status_1_err
2	dsp_pe_dsp_status_2_err
3	dsp_pe_flag_err
4	dsp_pe_irq_err
5	dsp_pe_quad_i_sqrt_udf_err
6	dsp_pe_ram_err
7	dsp_pe_sign_err
8	dsp_pe_sqrt_err

Clear by read mechanism implemented. err_flag_16_bank6 information is ASIC internally latched until next read access.

Req_2151

page	ID	r/w	Bit	function	description	default value
2	0x8	r	12:0	err_flag_16_bank7		

	err_flag_16_bank7
0	dsp_acc1_LF_adjust
1	dsp_ctm1_adjust
2	dsp_ctm2_adjust
3	dsp_rate_LF_adjust
4	dsp_quad_HF_adjust
5	dsp_adjust_data_err
6	dsp_gp_status
7	dsp_acc1_LF_in
8	dsp_acc1_LF_out
9	dsp_rate_LF_out
10	dsp_neg_flag_sqrt
11	dsp_quad_QI_lim
12	dsp_quad_sqrt_lim

Clear by read mechanism implemented. err_flag_16_bank7 information is ASIC internally latched until next read access.

Req_2152

page	ID	r/w	Bit	function	description	default value
2	0x9	r	14:0	err_flag_16_bank8		

	err_flag_16_bank8
0	dspmem_debugaccess_on
1	dsp_ram_decadd_err
2	dsp_ram_ifa13_err
3	dsp_ram_ifa13_su_err
4	dsp_rom_crc_err
5	dsp_rom_toggle_missing
6	dsp_ram_toggle_missing
7	dsp_ram_soaf_su_err
8	dsp_ram_soaf_err
9	dsp_ram_dpath_su_err
10	dsp_ram_dpath
11	dsp_soc_rate_inactive
12	dsp_soc_acc_inactive
13	dsp_foc_rate_active
14	dsp_foc_acc_active

Clear by read mechanism implemented. err_flag_16_bank8 information is ASIC internally latched until next read access.

Req_2154

page	ID	r/w	Bit	function	description	default value
2	0xA	r	7:0	ec0_yrs_lf	Unsigned 8bit value of rate error counter (current value).	

Req_2155

page	ID	r/w	Bit	function	description	default value
2	0xB	r	7:0	ec1_quad_hf	Unsigned 8bit value of quad error counter (current value).	

Req_2156

page	ID	r/w	Bit	function	description	default value
2	0xC	r	7:0	ec2_acc_lf	Unsigned 8bit value of acc error counter (current value).	

Req_2159

page	ID	r/w	Bit	function	description	default value
2	0xD	r	5:0	SPI state (ErrorStatus)	Status of SPI-errors	

	ErrorStatus	Status of SPI-errors
0	CPOL_ERR	SPI clock polarity error.
1	SCK_CNT_ERR	SPI: wrong number of SCK-clocks.
2	RX_CRC_ERR	CRC in received frame is wrong.
3	BUS_ERR	error on APB-bus.
4	BUS_TIME_ERR	APB-bus-acces not finished in 2 clock-cycles (CC32in).
5	WR_PAGE_ERR	page-address is written, which is not writable.

Req_2160 *A-samples:*

page	ID	r/w	Bit	function	description	default value
2	0xE	r	3:0	OFFSET_CONTROLLER_STATE	Status of SPI-errors	

	OFFSET_CONTROLLER_STATE	
0	rate_slow_offset_controller_active	Status of DSP rate slow offset controller (active if set)
1	acc_slow_offset_controller_active	Status of DSP acc slow offset controller (active if set)
2	rate_fast_offset_controller_active	Status of DSP rate fast offset controller (active if set)
3	acc_fast_offset_controller_active	Status of DSP acc fast offset controller (active if set)

C-samples:

page	ID	r/w	Bit	function	description	default value
2	0xE	r	15:0	TEMP_SENSOR_1_VALUE	Signed 16bit value of temperature sensor 1 (DSP)	

Req_2161

To calculate a real temperature value the following equaion can be used (only nominal value, no specification guaranteed):

Temperature [°C] = 32.5°C + TEMP_SENSOR_1_VALUE [LSB] / 200 [LSB/°C]

page	ID	r/w	Bit	function	description	default value
2	0xF	r	15:0	cluster_flag		

0	clu_ST_OR_FOC_RUNNING
1	clu_INIT
2	clu_MECH_OVERLOAD_ACC
3	clu_ST_FAILED
4	clu_PIN_OR_BOND_FAILURE
5	clu_TEMP
6	clu_SUPPLY
7	clu_EMC_PSRR
8	clu_MECH_OVERLOAD_RATE
9	clu_DIGITAL
10	clu_OTP_System
11	clu_DSP
12	clu_MEMORY
13	clu_ACC_DETECTION
14	clu_RATE_DETECTION
15	clu_RATE_DRIVE

Clear by read mechanism implemented. Cluster flag information is ASIC internally latched until next read access.

4.3.8.2.4 Register Information for Page 3

Req_2162

page	ID	r/w	Bit	function	description	default value
3	0x0	r/w	6:0	dsp_flush_time	DSP flush time setting used for flag control and channel status generation. **SMI720 A-samples:** Time setting corresponds to a range of 0 to 127ms in 1ms steps for dsp_flush_time after Bite and 0 to 255ms in 2ms steps for dsp_flush_time of the error_counters. **SMI720 C-samples:** Time setting corresponds to a range of 0 to 127ms in 1ms steps for dsp_flush_time after Bite and dsp_flush_time of the error_counters.	0x1C

SMI720 A samples: The dsp_flush_time can be configured to 14 LSB (0xE) after BITE, if the correct value of 28ms (+/-10%) for the error counter is needed (bug within TIG720AA). If no correction to 14LSB (0xE) is done, the dsp_flush_time for the error counter will be 56ms +/-10% by default (28LSB with a decrement of 0.5LSB/ cycle with a cycle time of 1kHz +/-10%).

SMI720 C-samples: The reqired default value of 28LSB will be configured at final test. This will result in a dsp_flush_time of 28ms +/-10% (28LSB with a decrement of 1LSB/ cycle with a cycle time of 1kHz +/-10%)

Req_2163

page	ID	r/w	Bit	function	description	default value
3	0x1	r/w	6:0	ec0_yrs_lf_config	Error counter limit setting used for rate error counter. Typically a value of 16LSB are configured, which ensures fault tolerant time span of <18ms (16ms + 10%).	0x10

If the customer changes the error counter limit to larger values than default, the metric calculations are not valid anymore. Lower values result in less system availability as a CI flag marks the sensor data as wrong earlier.

Req_2164

page	ID	r/w	Bit	function	description	default value
3	0x2	r/w	6:0	ec1_quad_hf_config	Error counter limit setting used for quad error counter. Typically a value of 16LSB are configured, which ensures fault tolerant time span of <18ms (16ms + 10%).	0x10

If f the customer changes the error counter limit to larger values than default, the metric calculations are not valid anymore. Lower values result in less system availability as a CI flag marks the sensor data as wrong earlier.

Req_2165

page	ID	r/w	Bit	function	description	default value
3	0x3	r/w	6:0	ec2_acc_lf_config	Error counter limit setting used for acc error counter. Typically a value of 16LSB are configured, which ensures fault tolerant time span of <18ms (16ms + 10%).	0x10

If f the customer changes the error counter limit to larger values than default, the metric calculations are not valid anymore. Lower values result in less system availability as a CI flag marks the sensor data as wrong earlier.

Req_2167

page	ID	r/w	Bit	function	description	default value
3	0x4	r/w	3:0	bite_config_max_rep	Sensor selftest BITE config maximum repetitions.	0x2
3	0x4	r/w	13:8	bite_config_phase_len	Sensor selftest BITE config - phase length	0x1A

bite_config_phase_len Parameter must not be changed by customer. This has to be ensured when this page adress is used to change the number of bite-repetitions with bite_config_max_rep parameter. Write acces to this page ID changes always the whole register information. Bit 13:8 has to be written to 0x1A even if only Bit 3:0 needs to be changed for a differnt number of bite repetitions. It is not recommended to reduce the number of bite repetitions because of a less sensor robustness.

Req_2168

page	ID	r/w	Bit	function	description	default value
3	0x5	r	15:0	ADDR_P2	Not used by customer	

Req_2169

page	ID	r/w	Bit	function	description	default value
3	0x6	r	15:0	ADDR_P3	Not used by customer	

Req_2170

page	ID	r/w	Bit	function	description	default value
3	0x7	r/w	7:0	ADDR_DEBUG_1	Configured address which is read via debug_out_1_value.	0x8
3	0x7	r/w	15:8	ADDR_DEBUG_2	Configured address which is read via debug_out_2_value.	0x9

Channel	Point	DBG Address	RAM Address
RATE	IN	0	32
ACC	IN	1	33
RATE	Adjusted	2	34
ACC	Adjusted	3	35
RATE	Prelim	4	36
ACC	Prelim	5	37
RATE	postfilter	6	38
ACC	postfilter	7	39
RATE	Offset_controller reg_val	8	40
ACC	Offset_controller reg_val	9	41
QUAD_I	QUAD_IN	10	42
QUAD_I	PreControl	11	43
QUAD_I	PostControl	12	44
QUAD_I	QUAD_I_SQRT	13	45
QUAD_I	QUAD_I	14	46
QUAD_HF	IN	15	47
QUAD_HF	Adjusted	16	48
Temperature 1	IN	17	49
Temperature 2	IN	18	50
Debug_Counter	16 Bit Counter (8333 Hz)	19	51
RATE	Offset_Controller fast_val	20	52
ACC	Offset_Controller fast_val	21	53

When DBG address is written to ADDR_DEBUG_1 or ADDR_DEBUG_2 the selected signal can be read via DEBUG_OUT_1_VALUE and DEBUG_OUT_2_VALUE.

Req_2171

page	ID	r/w	Bit	function	description	default value
3	0x8	r	15:0	DEBUG_OUT_1_VALUE	With debug_control default configuration the signed 16bit MSB sum value of fast and slow offset controller rate is read.	

Rate offset-controller-value multiplied with 6.125 gives the initial rate offset before FOC and SOC were applied.

Req_2172

page	ID	r/w	Bit	function	description	default value
3	0x9	r	15:0	DEBUG_OUT_2_VALUE	With debug_control default configuration the signed 16bit MSB sum value of fast and slow offset controller acc is read.	

ACC offset-controller-value multiplied with 22.25 gives the initial acc offset before FOC and SOC were applied.

Req_2173

page	ID	r/w	Bit	function	description	default value
3	0xA	r	15:0	DEBUG_OUT_1_2_CAPTURED	Captured debug_out_2 value at the time when debug_out_1 has been read, or captured debug_out_1 value at the time when debug_out_2 has been read. Signed or unsigned depends on debug_control configuration. With default configuration a 16bit signed value is read.	

Req_2174

page	ID	r/w	Bit	function	description	default value
3	0xB	r	15:0	DEBUG_COUNTER_CAPTURED	16bit unsigned captured debug counter value of DSP.	

Req_2175

page	ID	r/w	Bit	function	description	default value
3	0xC	r/w	15:0	Offset_Addressing_Password1	Password1 for full register access with offset addressing. Only for RB internal use.	

Req_2176

page	ID	r/w	Bit	function	description	default value
3	0xD	r/w	15:0	Offset_Addressing_Password2	Password2 for full register access with offset addressing. Only for RB internal use.	

Req_2177

page	ID	r/w	Bit	function	description	default value
3	0xE	r/w	15:0	SPI64_Password1	Password1 for switch to SPI64. Only for RB internal use.	

Req_2178

page	ID	r/w	Bit	function	description	default value
3	0xF	r/w	15:0	SPI64_Password2	Password2 for switch to SPI64. Only for RB internal use.	

4.3.8.2.5 Register Information for Page 4

Req_2179

page	ID	r/w	Bit	function	description	default value
4	0x0	r	15:0	ASIC_SERIAL_NR_0	ASIC serial number Bit 15:0 unsigned. This information is required for a single part traceability of the SMI720.	

Req_2180

page	ID	r/w	Bit	function	description	default value
4	0x1	r	15:0	ASIC_SERIAL_NR_1	ASIC serial number Bit 31:16 unsigned. This information is required for a single part traceability of the SMI720.	

Req_2181

page	ID	r/w	Bit	function	description	default value
4	0x2	r	15:0	ASIC_SERIAL_NR_2	ASIC serial number Bit 47:32 unsigned. This information is required for a single part traceability of the SMI720.	

Req_2182

page	ID	r/w	Bit	function	description	default value
4	0x3	r	15:0	ASIC_NAME	Name of Chip (TIG720).	0x720

It is strongly recommended to check the correct ASIC name of SMI720 (0x720) during initialization at ECU level or distinguish in another appropriate way that the used sensor is a SMI720 (e.g. by checking the CUSTOMER_SERIAL_NUMBER or SMI_SERIAL_NR). This recommendation is based on lessons learned from other sensor products.

Req_2183

page	ID	r/w	Bit	function	description	default value
4	0x4	r	7:0	REVISION_ID	Revision of ASIC (0x00=AA, 0x10=BA, 0x11=BB, ..)	

For TIG720AA (SMI720 A0-samples) default value of the revision ID is 0x00.
For TIG720BA (SMI720 C0-samples) default value of the revision ID is 0x10.
For TIG720BB (SMI720 C0-samples) default value of the revision ID is 0x11.
For TIG720BC (SMI720 C1-samples) default value of the revision ID is 0x12.

Req_2184

page	ID	r/w	Bit	function	description	default value
4	0x5	r	15:0	SMI_SERIAL_NR_0	SMI serial number Bit 15:0 unsigned. This information is required for a single part traceability of the SMI720.	

Req_2185

page	ID	r/w	Bit	function	description	default value
4	0x6	r	15:0	SMI_SERIAL_NR_1	SMI serial number Bit 31:16 unsigned. This information is required for a single part traceability of the SMI720.	

Req_2186

page	ID	r/w	Bit	function	description	default value
4	0x7	r	15:0	SMI_SERIAL_NR_2	SMI serial number Bit 47:32 unsigned. This information is required for a single part traceability of the SMI720.	

Req_2231 **SMI_SERIAL_NR (47:0), sample shop production from A0D-samples on (DKT):**

Sample / Series	SMI7 Type	Sample State # (last 5 digits)	Sample Lot #	Single Part # (laser print)
1 bit	3 bit	17 bit	17 bit	10 bit
Bit 47	Bit (46:44)	Bit (43:27)	Bit (26:10)	Bit (9:0)
Sample=0 / Series=1	**011b**	e.g. (0274B02) **008-04**	e.g. **29363** (I)	e.g. **239**

SMI7 Type (bin):

SMI700	001
SMI710	010
SMI720	**011**
SMI740	101
SMI750	110

SMI_SERIAL_NR (47:0), plan for production at MFS (SPEA):

Sample / Series	SMI7 Type	Part Number (last 5 digits)	Subcon	Production Lot #
1 bit	3 bit	17 bit	2 bit	25 bit
Bit 47	Bit (46:44)	Bit (43:27)	Bit (26:25)	Bit (24:0)
Sample=0 / Series=1	**011b**	e.g. (02731) **42040**	Unisem=01b/ Amkor=10b	6 or 7 numbers

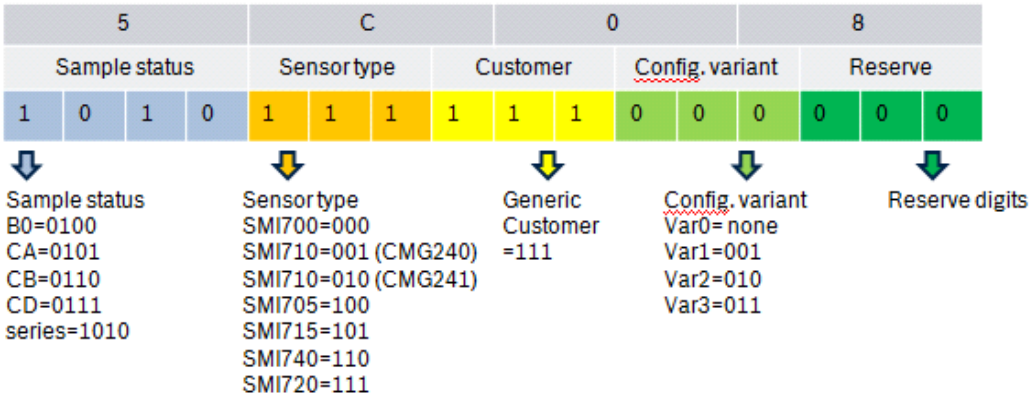
SMI7 Type (bin):

SMI700	001
SMI710	010
SMI720	**011**
SMI740	101
SMI750	110

Req_2187

page	ID	r/w	Bit	function	description	default value
4	0x8	r	15:0	CUSTOMER_SERIAL_NR		0xAFC0

For SMI720 a generic default value (0xAFC0) according to following definition is used for this register:



Req_2188

page	ID	r/w	Bit	function	description	default value
4	0x9	r	15:0	Upper 16bit of last read access.	Only used, if requested internal register information contains more than 16bit.	

Req_2237 *from C-samples on:*

page	ID	r/w	Bit	function	description	default value
4	0xA	r	15:0	DUMMY_ADDR_REG1	Only implemented for backup reasons. Currently not necessary for SMI720 application.	

Req_2238 *from C-samples on:*

page	ID	r/w	Bit	function	description	default value
4	0xB	r	15:0	DUMMY_ADDR_REG2	Only implemented for backup reasons. Currently not necessary for SMI720 application.	

Req_2239 *from C-samples on:*

page	ID	r/w	Bit	function	description	default value
4	0xC	r	15:0	tc_yrs_rate_seq_bite	Temperature coefficient for manual rate bite evaluation. Signed 16Bit value with 14Bit fractional part.	

Req_2240 *from C-samples on:*

page	ID	r/w	Bit	function	description	default value
4	0xD	r	15:0	tc_yrs_quad_seq_bite	Temperature coefficient for manual quad bite evaluation. Signed 16Bit value with 14Bit fractional part.	

Req_2241 *from C-samples on:*

page	ID	r/w	Bit	function	description	default value
4	0xE	r	15:0	tc_yrs_acc1_seq_bite	Temperature coefficient for manual acc bite evaluation. Signed 16Bit value with 14Bit fractional part.	

Req_2242 *from C-samples on:*

page	ID	r/w	Bit	function	description	default value
4	0xF	r/w	3:0	bite_config_max_rep	Configuration of the maximum number of automatically performed bite repetitions for acc-, rate- and quad-channel in case of a bite-fail.	0x2
4	0xF	r/w	13:8	bite_config_phase_len	Configuration of the bite-phase length for acc-, rate- and quad-channel. This value must not be changed. If the maximum number of bite repetitions has to be changed, this parameter needs to be written so the default value again.	0x1A

bite_config_phase_len Parameter must not be changed by customer. This has to be ensured when this page adress is used to change the number of bite-repetitions with bite_config_max_rep parameter. Write acces to this page ID changes always the whole register information. Bit 13:8 has to be written to 0x1A even if only Bit 3:0 needs to be changed for a differnt number of bite repetitions. It is not recommended to reduce the number of bite repetitions because of a less sensor robustness.

4.3.8.2.6 Register Information for Page 5

Req_2196

page	ID	r/w	Bit	function	description	default value
5	0x0	r	15:0	Last_Bite_ACC1_POS	Signed 16bit last measured value ACC Bite positive phase of a triggered bite sequence.	

Req_2197

page	ID	r/w	Bit	function	description	default value
5	0x1	r	15:0	Last_Bite_ACC1_NEG	Signed 16bit last measured value ACC Bite negative phase of a triggered bite sequence.	

Req_2198

page	ID	r/w	Bit	function	description	default value
5	0x2	r	15:0	Last_Bite_QUAD_POS	Signed 16bit last measured value Quad Bite positive phase of a triggered bite sequence.	

Req_2199

page	ID	r/w	Bit	function	description	default value
5	0x3	r	15:0	Last_Bite_QUAD_NEG	Signed 16bit last measured value Quad Bite negative phase of a triggered bite sequence.	

Req_2200

page	ID	r/w	Bit	function	description	default value
5	0x4	r	15:0	Last_Bite_QUAD_ZERO	Signed 16bit last measured value Quad Bite zero / off Phase of a triggered bite sequence.	

Req_2201

page	ID	r/w	Bit	function	description	default value
5	0x5	r	15:0	Last_Bite_RATE_POS	Signed 16bit last measured value Rate Bite positive phase of a triggered bite sequence.	

Req_2202

page	ID	r/w	Bit	function	description	default value
5	0x6	r	15:0	Last_Bite_RATE_NEG	Signed 16bit last measured value Rate Bite negative phase of a triggered bite sequence.	

Req_2203

page	ID	r/w	Bit	function	description	default value
5	0x7	r	15:0	Last_Bite_Rate_ZERO	Signed 16bit last measured value Rate Bite zero / off Phase of a triggered bite sequence.	

Req_2204

page	ID	r/w	Bit	function	description	default value
5	0x8	r	15:0	New part value of Last_Bite_QUAD_POS	Signed 16bit new part value of Quad Bite positive phase.	

Req_2205

page	ID	r/w	Bit	function	description	default value
5	0x9	r	15:0	New part value of Last_Bite_QUAD_NEG	Signed 16bit new part value of Quad Bite negative phase.	

Req_2207

page	ID	r/w	Bit	function	description	default value
5	0xA	r	15:0	New part value of Bite delta |Last_Bite_QUAD_POS - Last_Bite_QUAD_NEG|	Signed 16bit new part value of Quad Bite Delta positive phase – negative phase.	

Req_2208

page	ID	r/w	Bit	function	description	default value
5	0xB	r	15:0	New part value of Bite delta |Last_Bite_RATE_POS - Last_Bite_RATE_NEG|	Signed 16bit new part value of Rate Bite Delta positive phase – negative phase.	

Req_2209

page	ID	r/w	Bit	function	description	default value
5	0xC	r	15:0	New part value of Bite delta |Last_Bite_ACC1_POS - Last_Bite_ACC1_NEG|	Signed 16bit new part value of ACC Bite Delta positive phase – negative phase.	

Req_2211

page	ID	r/w	Bit	function	description	default value
5	0xD	r	3:0	bite_acc_repetition	Number of executed BITE sequence repetitions in ACC channel (unsigned).	0x0
5	0xD	r	7:4	bite_yrs_repetition	Number of executed BITE sequence repetitions in Quad and Rate channel (unsigned).	0x0

Req_2212

page	ID	r/w	Bit	function	description	default value
5	0xE	r	0	yrs_bite_active	Bite in quad and rate channel is active if bit is set. When bite is finished the bit is reset to 0, dsp_filter_flush_time after bite is not included.	0x0
5	0xE	r	1	acc_bite_active	Bite in acc channel is active if bit is set. When bite is finished the bit is reset to 0, dsp_filter_flush_time after bite is not included.	0x0

Req_2213

page	ID	r/w	Bit	function	description	default value
5	0xF	r	15:0	cluster_flag		

0	clu_ST_OR_FOC_RUNNING
1	clu_INIT
2	clu_MECH_OVERLOAD_ACC
3	clu_ST_FAILED
4	clu_PIN_OR_BOND_FAILURE
5	clu_TEMP
6	clu_SUPPLY
7	clu_EMC_PSRR
8	clu_MECH_OVERLOAD_RATE
9	clu_DIGITAL
10	clu_OTP_System
11	clu_DSP
12	clu_MEMORY
13	clu_ACC_DETECTION
14	clu_RATE_DETECTION
15	clu_RATE_DRIVE

Clear by read mechanism implemented. Cluster flag information is ASIC internally latched until next read access.

4.3.8.2.7 Register Information for Page 6

Req_2244 *From C-samples on:*

page	ID	r/w	Bit	function	description	default value
6	0x0	r/w	0	EOP (End of Programming)	If the EOP Bit is set to 1, the r/w page registers listed below are locked for write access. If a write access happened to a EOP locked r/w register no dedicated SPI failure handling is implemented. Reaction of the SPI is identically to a successful write access.	0x0

Page 0:
0x5 (SID);
0x6 (Reset vector)
0xA (Register CRC-check
0xB (Register CRC-check)
0x8 (Offset-controller)
Page 3:
0x0 (Flush-time),
0x1 (Error counter config)
0x2 (Error counter config)
0x3 (Error counter config)
0x4 (Address pointer)
0x5 (Address pointer)
0x6 (Address pointer)
0xC (Passwords for offset addressing)
0xD (Passwords for offset addressing)
Page 4:
0xA (DUMMY_ADDR_REG1)
0xB (DUMMY_ADDR_REG2)
0xC (tc_yrs_rate_seq_bite)
0xD (tc_yrs_quad_bite_pos_neg)
0xE (tc_acc1_bite_pos_neg)
0xF (bite_config)
Page6:
0x0 EOP (EOP is also protected to avoid a unwanted disable of the EOP)
There is no link between any sensor status (e.g. CI Bit) and the EOP functionality. No failure handling is implemented if a write access to a EOP locked register happened.

4.3.8.3 Register Information for Single Part Traceability

Req_2011 For a single part traceability of the SMI720 the customer has to provide the following register information:

Page 4			
Offset	**r/w**	**ID**	**Function/Target Register**
4	r	0x0	Serial number programmed at electrical wafer sort part 1
4	r	0x1	Serial number programmed at electrical wafer sort part 2
4	r	0x2	Serial number programmed at electrical wafer sort part 3
4	r	0x5	Serial number of SMI part 0
4	r	0x6	Serial number of SMI part 1
4	r	0x7	Serial number of SMI part 2

The single part traceability is required for the analysis of rejected parts.

4.3.9 Data Frame Protection by CRCs

Req_272 For all SPI cyclic redundant checks, the following CRC algorithm is used:

polynomial: $x^3 + x^1 + x^0 = 0x5$
start value: 111b
target value: 000b

Req_276 CRC test cases for commands and answers:

	Official testcases CC32IN command: Commands towards the sensor on MOSI								
	with correct CRC								
0x	0	0	0	0	0	0	0	4	*Read Device ID*
0x	0	0	4	0	0	0	1	0	*Read Revision ID*
0x	6	1	4	0	0	0	7	C	*Random command*
0x	0	0	0	0	0	0	0	4	*Zero command*
0x	0	8	0	0	0	0	1	c	*RD_ucTransfer1*

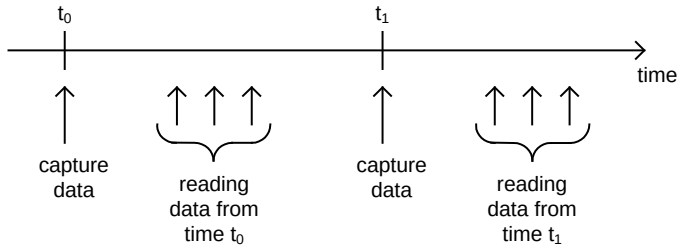
	Official testcases CC32IN answer: Commands towards the sensor on MISO								
	with correct CRC								
0x	F	E	0	F	F	F	F	6	*Sensor Data responce*
0x	F	C	0	7	F	F	F	7	*Module Answer*
0x	0	0	0	0	0	0	0	6	*Zero answer*
0x	F	F	F	F	F	F	F	C	*One answer*
0x	0	1	4	0	0	0	6	5	*Random answer*

Req_277

CRC implementation is the same as used in TIG700 and therefore the reference implementation of TIG700 is still valid.

4.3.10 Data Capture Mechanism

Req_282 The protocol features data capturing. This means sensor measurement data of all channels on one chip select line can be captured (stored sensor internally) at one point in time and read out at a later point in time. With this mechanism sensor data at one point of time of several sensors can be read subsequently. With this concept, the data of all channels can be measured at the same point in time.



In A-Samples, the CI bit returned with the captured data represents the CI state during capturing.

From C-Samples on, the CI bit returned with the captured data is only '0' (valid data) if the CI=='0' condition is met during capturing and reading captured data. This applies for both 32 bit SPI dialects.

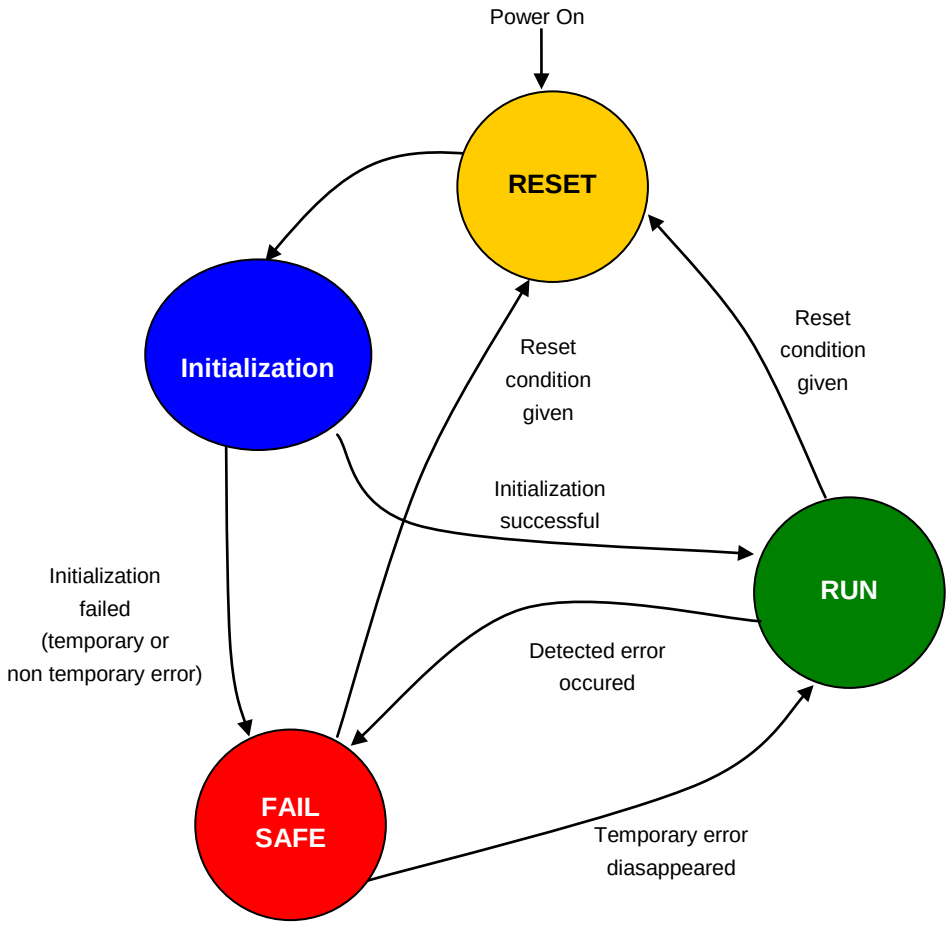
Req_284 CAP: Capture bits are interpreted from all modules on a chip select line (regardless the BUSADR, only checking if a valid CHANNELADR is given). These bits (only within channel commands) are broadcasting.

Req_285 Note: Sensor will capture data before being able to check CRC bits (for CAP = 'b101'). Therefore, CAP is defined as 3bit value with hamming distance of >= 2 (redundancy) of CAP = 'b101' with respect to CAP = 'b010' and CAP = 'b011'.

5. Functional Specification

5.1 Operating States

Req_979



5.1.1 Reset State

Req_1164 The reset state is the first state reached after power on, while the digital supply voltage is still below the reset limit. The state can also be reached from any other state via an SPI reset command or a under voltage reset. After the reset all internal blocks and registers are set to their initial default settings. There is no functional difference between an SPI and an under voltage reset regarding this point.

5.1.2 Initialization State

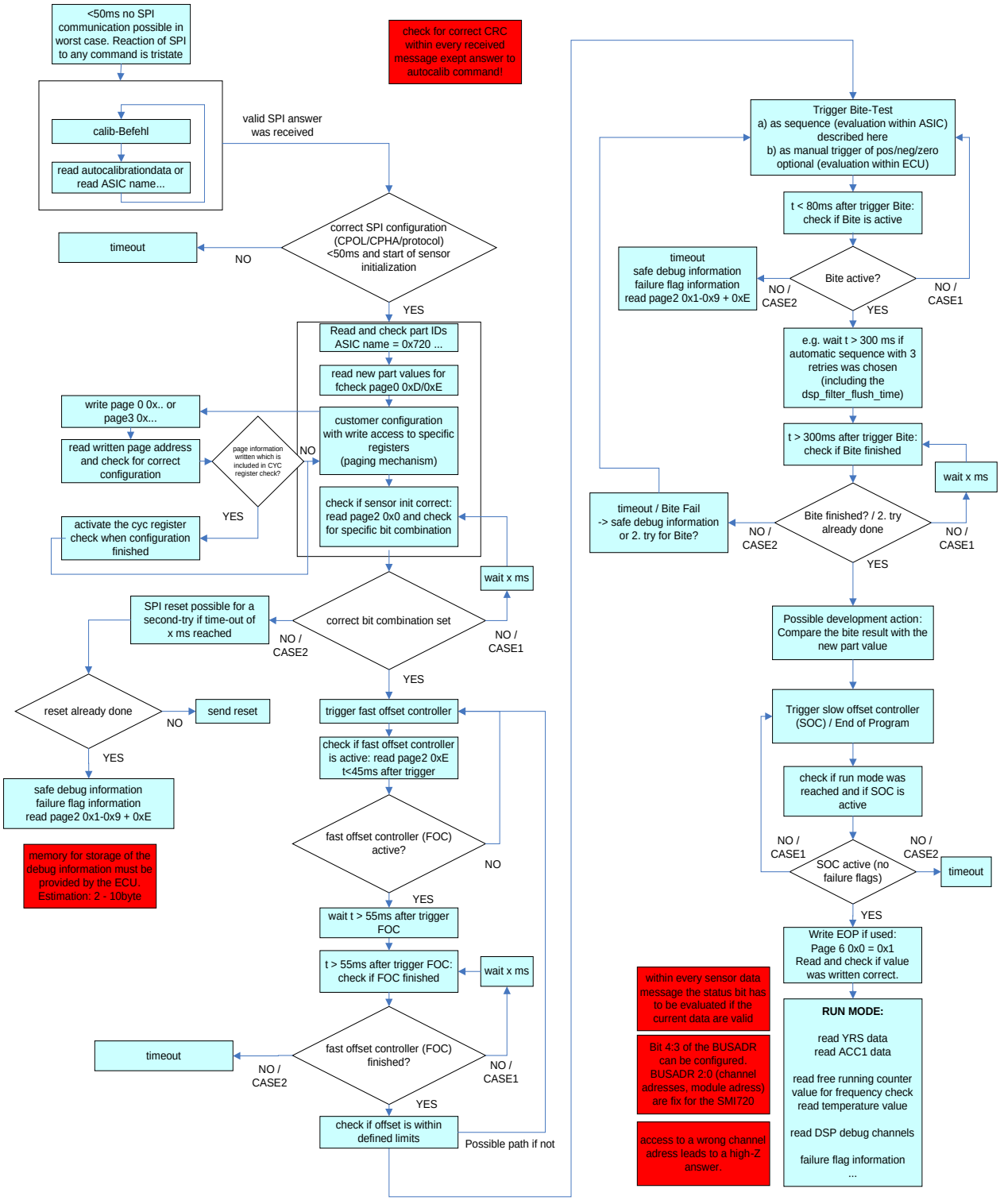
Req_981 The Initialization State can be separated into 5 different phases:

1) Sensor Initialization

2) Customer Configuration
3) Fast Offset Compensation
4) BITE (Rate and Acc)
5) Slow Offset Compensation

A first proposal for the initial software sequence within the ECU is shown below. This sequence is not final within the last detail but should give an overview how the initial software sequence has to be implemented for a correct initialization of the SMI720. Within the example a BITE sequence was triggered.

It is strongly recommended to check the correct ASIC name of SMI720 (page4 / ID 0x3 = 0x720) during initialization at ECU level. The recommendation is based on lessons learned from other sensor products.



5.1.2.1 *Internal Sensor Initialization*

Req_1167 In this phase, the sensor performs its self initialization, which comprises the following phases:

1) LBIST

2) Digital initialization
3) Excitation of mechanical oscillation

5.1.2.2 LBIST

Req_1169 The Logical Build In Self Test (LBIST) routine aims to detect stuck at faults of the digital part of the ASIC. The coverage of the LBIST test and final duration will be specified when characterized. Please refer also to the Chapter Safety.

5.1.2.3 Digital Initialization

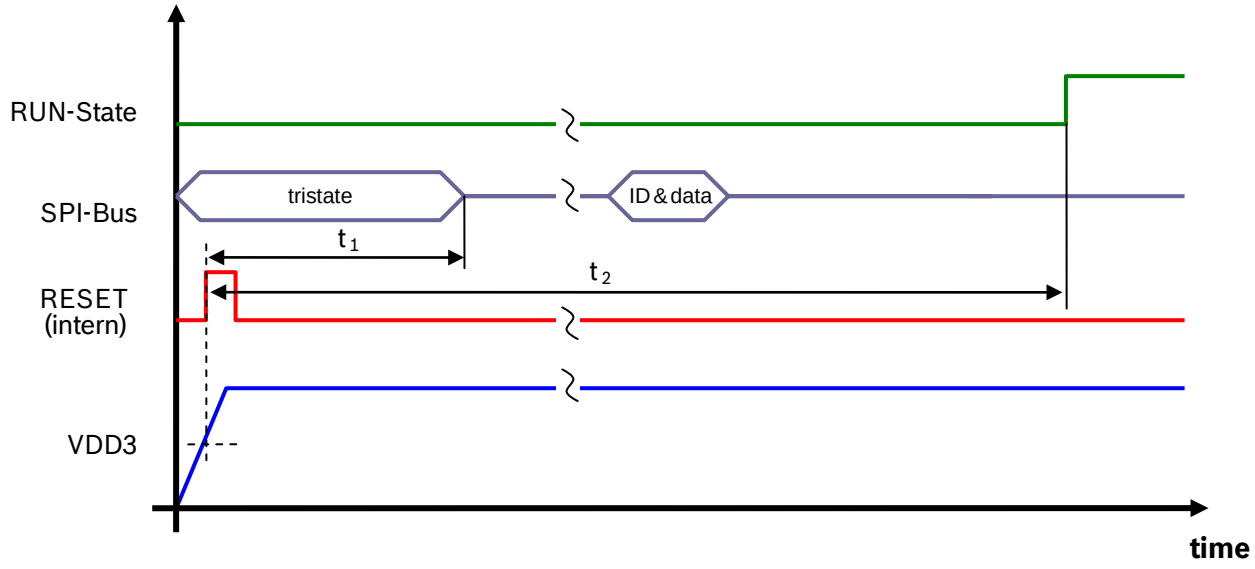
Req_1171 During the digital initialization the boot loader transfers all the default and calibration data from the OTP into the respective registers. Additionally, the entire memory and the correct function of the DSP is tested and checked for consistency (for details see Chapter Safety).

5.1.2.4 Excitation of the Mechanical Oscillation

Req_1174 At the heart of the initialization routines lies the excitation of the mechanical oscillation of the angular rate sensing element, as it not only enables the sensor to measure angular rate but also provides the system wide clock reference.

5.1.2.5 Startup Timing and Behavior

Req_984



Basic timing during startup-phase

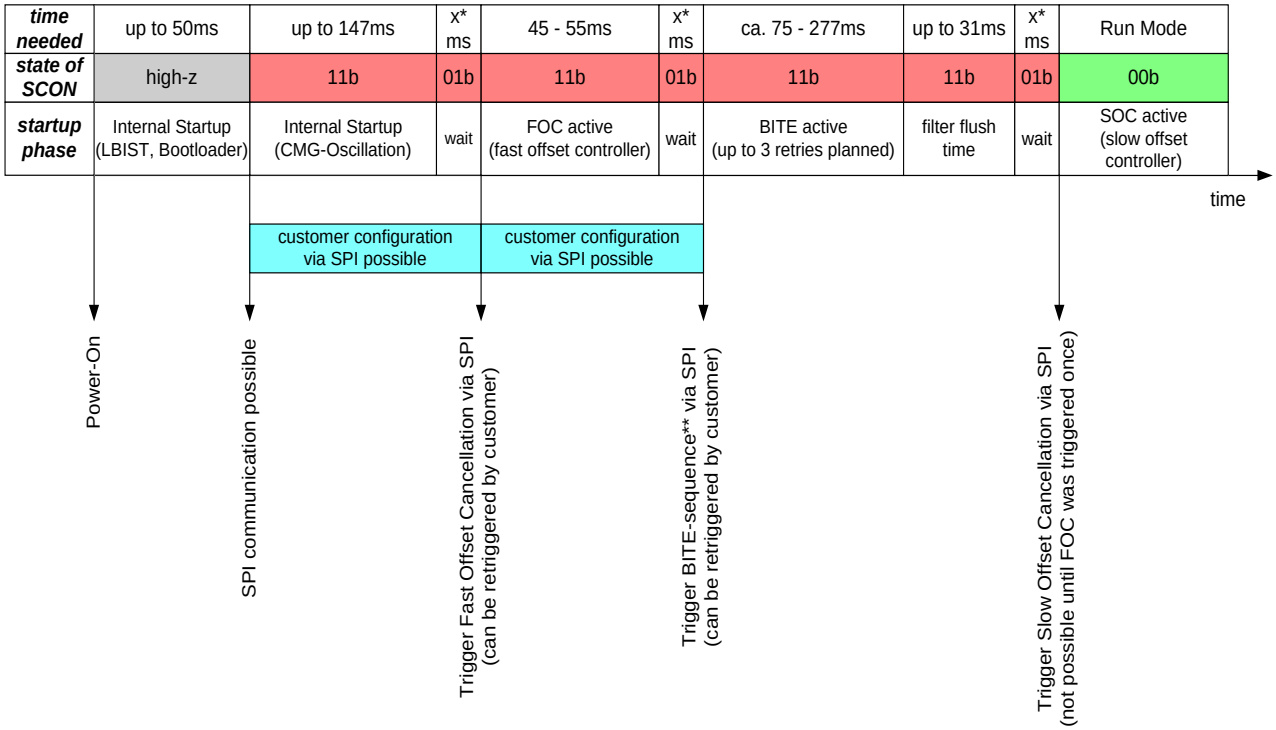
Req_2003

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Startup Timing	t_1	communication functional			50 (x)	ms
	t_2	full functionality (incl. 3 self tests cycles and fast offset cancellation)			560(+)	ms

(x) Communication earlier than the startup time t_1 "communication functional" will not lead to an illegal or misleading condition. There is no required minimum time before starting configuration/communication.

(+) Startup time depends also on timing for customer configuration, triggering offset-controller and BITE within the application.

Req_987



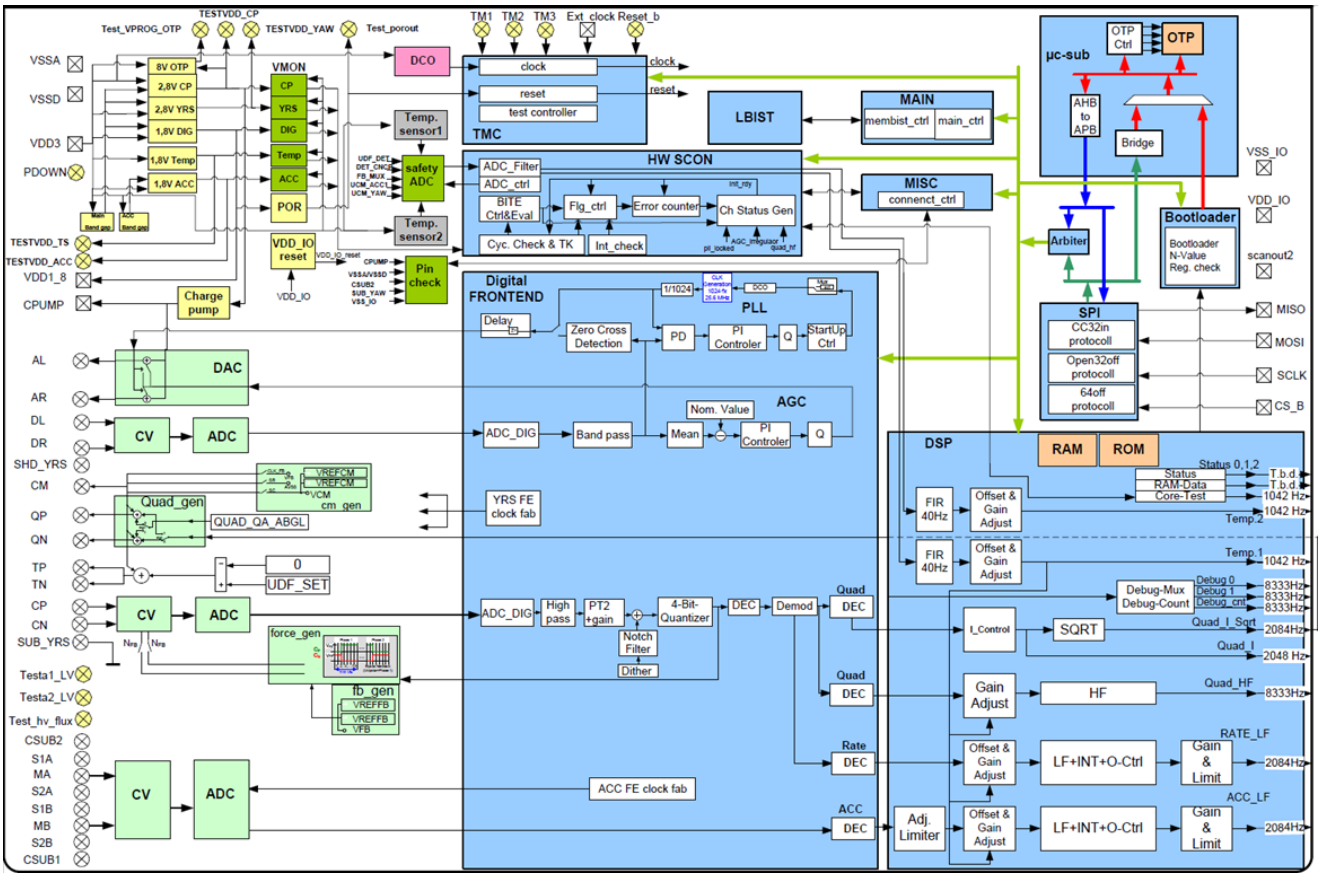
* depends on timing within the customer application
** also a completely manual BITE trigger is possible with customer individual timings

Phase within SMI720	State when phase is finished	Time (max.)	Duration (max.)
3,3V settled (Power = ON)	Release of Resets, Start LBIST, Bootloader, etc.	T=0	T=0
LBIST, Bootloader, CPUMP = in range, DSP-Tests finished	SPI- available, Frontend active	0 < T ≤ 50ms	<50ms
Settling of CMG-operation point	PLL-locked, AGC = in range, QUAD_HF = in range	50ms < T ≤ 197ms	<147ms
FOC active	Initial offset cancelled, FOC finished	197 ms < T ≤ 252 ms	<55ms
BITE active	BITE-test finished with max. two repetitions	252ms < T ≤ 529ms	<277ms
Filter-Flush-Time	Filter-Flush-Time elapsed	529ms < T < 560ms	<31ms
Trigger SOC	SOC active, Run-Mode	T = 560ms	T = 0ms

For absolute time limits best case ECU timing is assumed (no additional time slots due to customer configuration and required trigger commands are sent as soon as possible by customer software).

5.2 Signal Processing

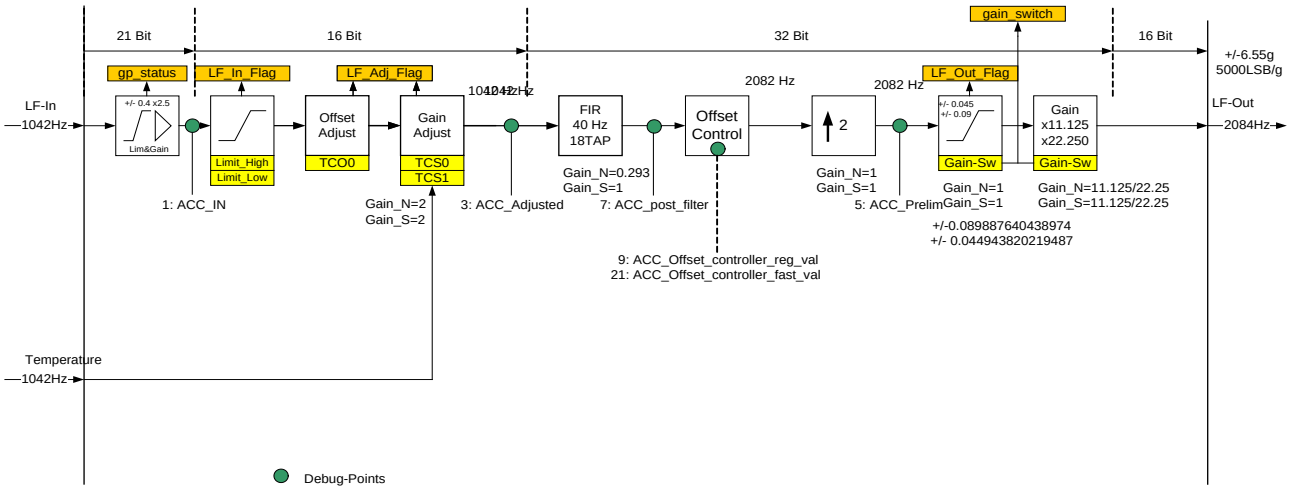
Req_1979 Block diagram of the TIG720:



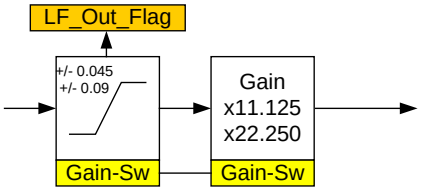
LF: LF-Filter
Int: Interpolator
O-Ctrl: Offset-Controller

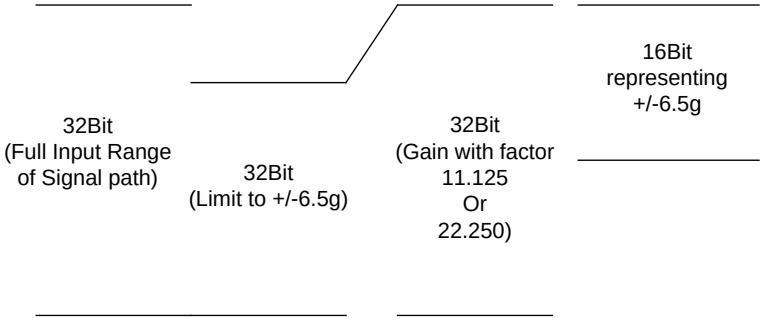
5.2.1 Acceleration Channel

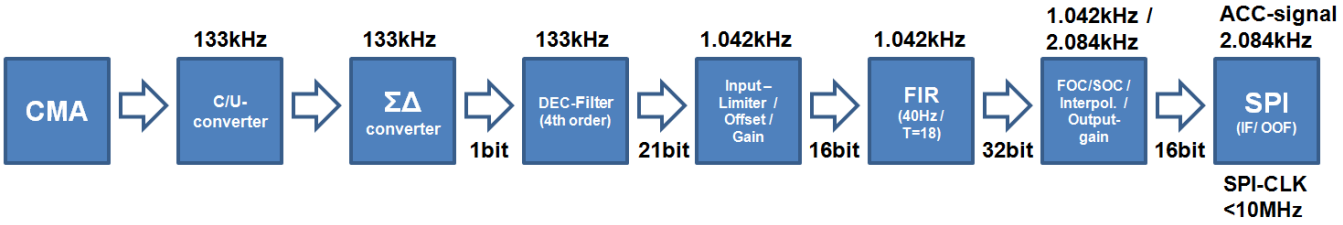
Req_2222 Signal processing of the acceleration channel within the DSP including bit width and signal update rate:



Explanation to understand how the 32bit DSP internal signal is mapped to the 16bit output signal. In SMI720 (with CMA511) only a gain of 22.250 is used:



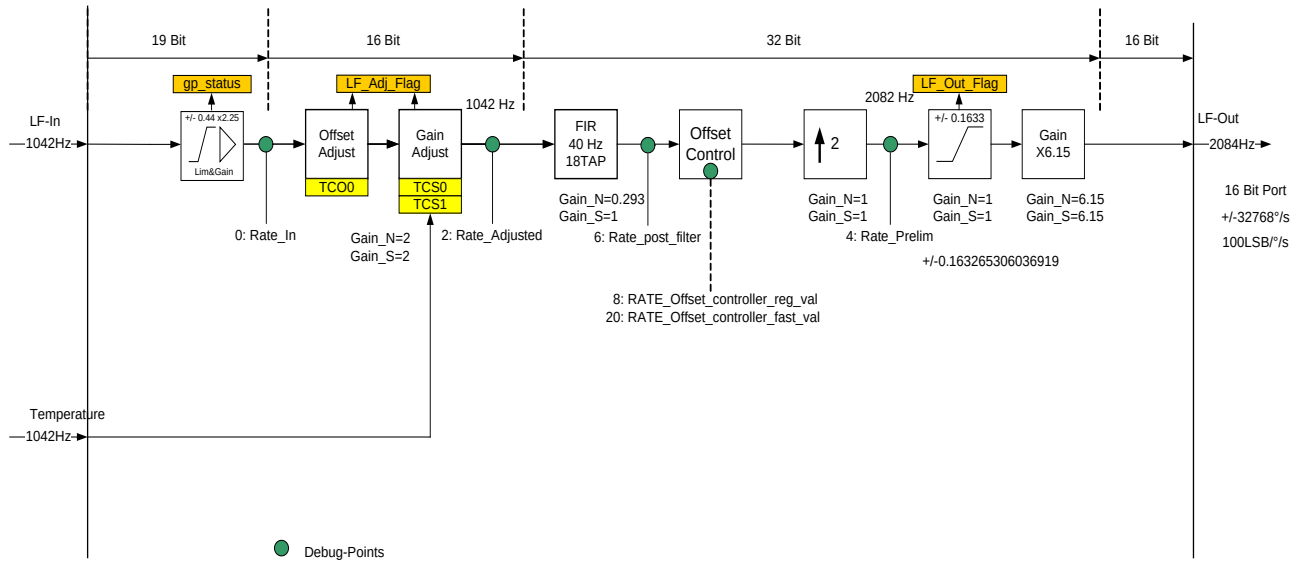




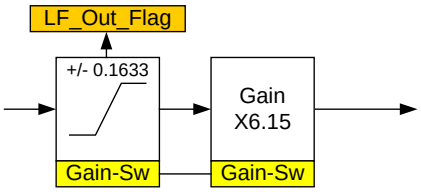
All clock frequencies are related to the nominal system clock of 25.6MHz (1024*f_CMG with f_CMG = 25kHz). SPI-clock depends on SPI-master.

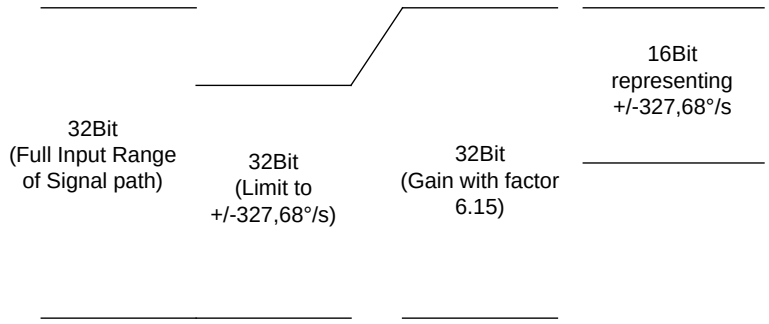
5.2.2 Angular Rate Channel

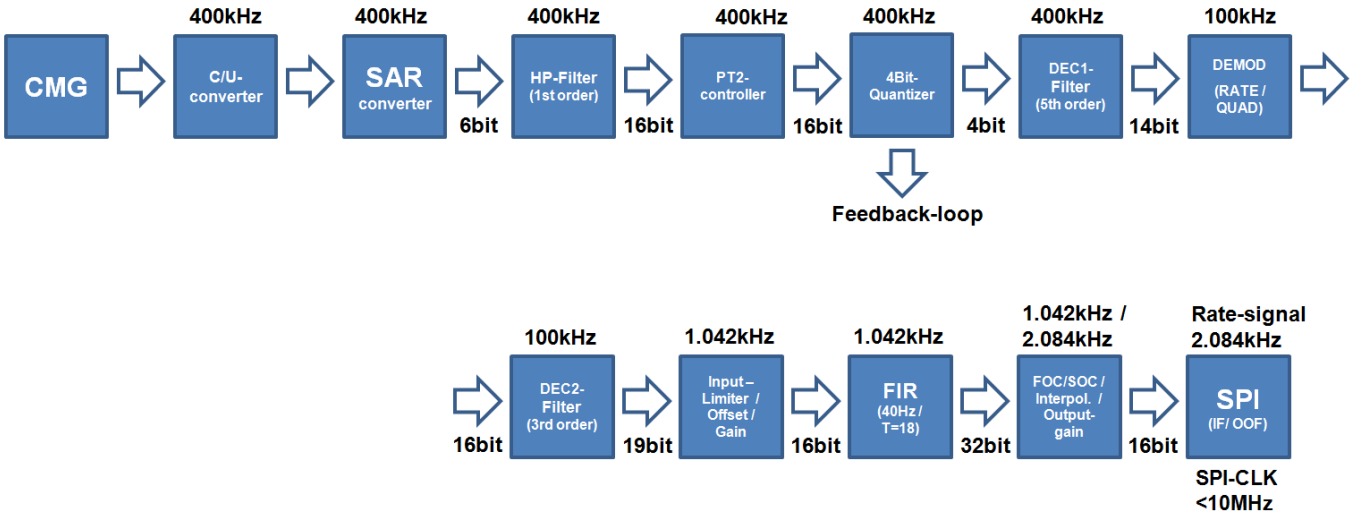
Req_2221 Signal processing of the rate channel within the DSP including bit width and signal update rate:



Explanation to understand how the 32bit DSP internal signal is mapped to the 16bit output signal:





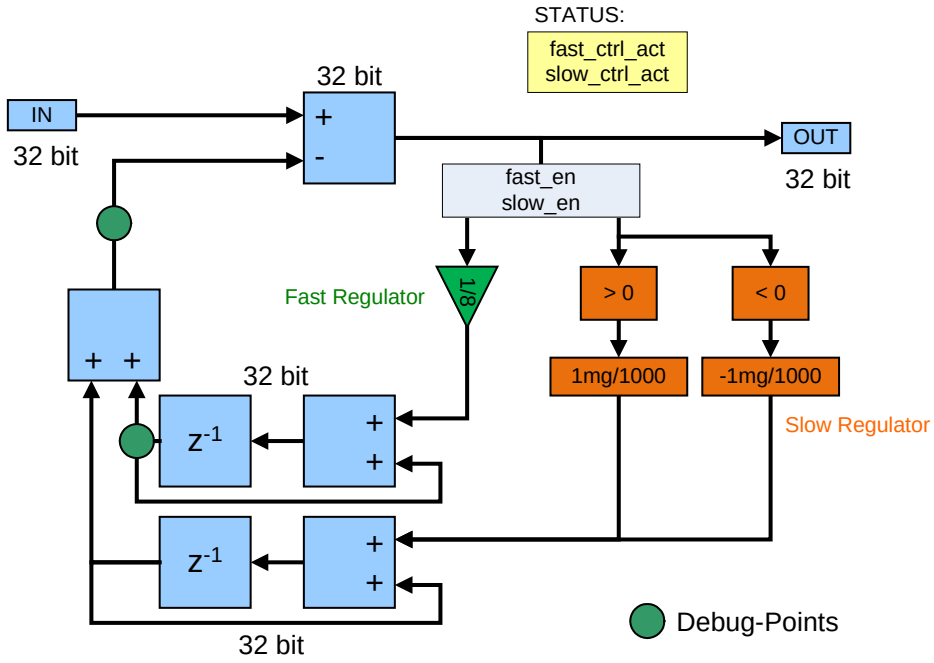


All clock frequencies are related to the nominal system clock of 25.6MHz (1024*f_CMG with f_CMG = 25kHz). SPI-clock depends on SPI-master.

5.2.3 Offset Cancelation

Req_1011 To reduce the existing offset depending on aging and temperature effects an offset controller will be implemented in the ACC and RATE path. The controllers are switchable between fast and slow mode. No symmetrical rounding is implemented within the DSP. Due to DSP internal rounding effects a theoretical constant offset error of +/-0.5LSB may be present.

Below the TIG720 concepts is shown (example for the acc signal path). The update rate of the slow offset controller is 1042Hz (+/-10%).



Comment: The +/- 1 mg/1000 indicate the internal constant increment / decrement of the slow offset controller. The value incremented or decremented leads to the specified controller speed.

ACC:

The slow controller is able to eliminate max. 1 mg/s. The theoretical residual offset of the controller is below 10 mg (without any noise influences, etc.).

The fast controller is able to eliminate offsets from +/- 3g in nominal 50 ms. The theoretical residual offset is below 10 mg. These values are depending on a DC input value. For example: If there is an acceleration of 80 mg in the last cycle of calculation, the result will be 10 mg of additional offset. The accuracy at the output depends on the input signal. The fast controller works nominal for 50 ms each trigger.

RATE:

The slow controller is able to eliminate max. 0.050 °/s/s. The theoretical residual offset of the controller is below 0.5 °/s (without any noise influences, etc.).

The fast controller is able to eliminate offsets from +/- 51 °/s in nominal 50 ms. The theoretical residual offset is below 0.171 °/s. These Values are depending on a DC-Input Value. For example: If there is a rate of 1.368 °/s in the last cycle of calculation, the result will be 0.171 °/s of additional Offset. The accuracy at the output depends on the input signal. The fast controller works nominal for 50 ms each trigger.

Debug Points:

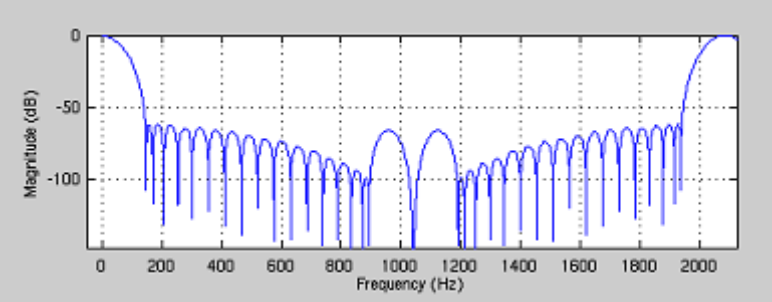
A reconstruction of the initial offset can be done by reading the offset controller values with the debug ports of the DSP via SPI pages. The value of the fast and the sum of fast and slow offset controller can be read. A corresponding configuration of the two available debug ports must be done via SPI pages. The following debug port addresses can be configured:

	DEBUG_CONTROL	
7...0	ADDR_DEBUG_1	Address for debug_1 value
15...8	ADDR_DEBUG_2	Address for debug_2 value

ACC fast offset controller : debug address 0x15
ACC sum of fast and slow offset controller : debug address 0x09
RATE fast offset controller : debug address 0x14
RATE sum of fast and slow offset controller : debug address 0x08

5.2.4 Interpolation Filter

Req_2225 Interpolation Filter was realized as 3rd Order filter with the following transfer function:
H(z)=[1 1]*[1 1]*[1 1] = [1 3 3 1] with a group delay of 1.5 * 1/2084Hz (nom +/-10%)

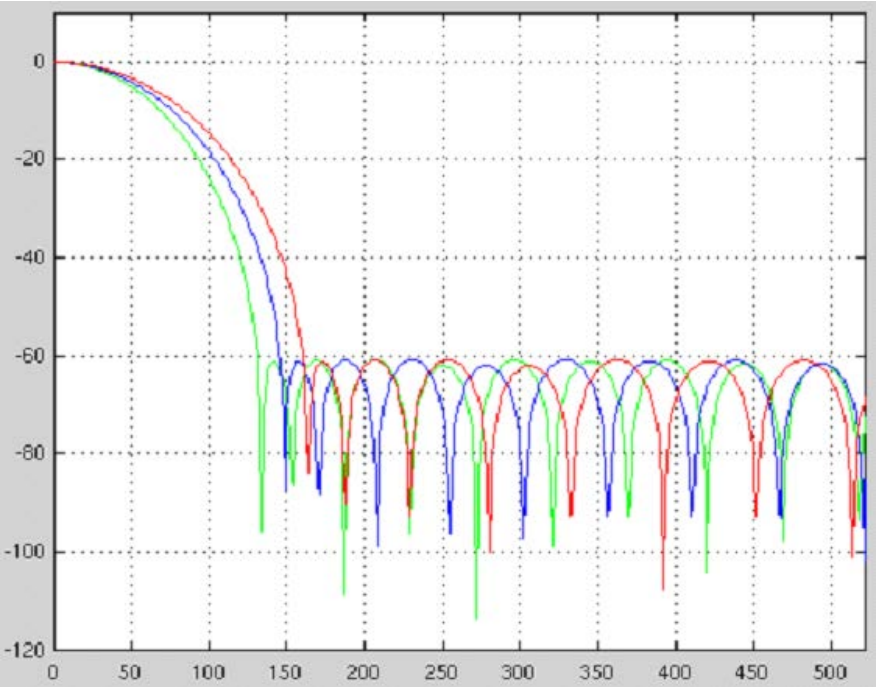


5.2.5 Output Filter (FIR-Implementation)

Req_1001 The output filter for angular rate and acceleration is implemented as an 18 tap FIR-Filter, according below transfer function. Nominal response of magnitude and phase is shown in the figures below.

$$H(z) = \frac{a_0 + a_1 \cdot z^{-1} + ... + a_{18} \cdot z^{-18}}{b_0}$$

Req_1113



LF filter parameters: [0.00238037; 0.00735474; 0.01669312; 0.03100586; 0.04974365; 0.07107544; 0.09188843; 0.10855103; 0.11779785; 0.11779785; 0.10855103; 0.09188843; 0.07107544; 0.04974365; 0.03100586; 0.01669312; 0.00735474; 0.00238037]

5.2.6 Group Delay and Matching of Channels

Req_2280 The following filter specification is valid for the complete sensor including mechanical, analog and digital filter elements.

Req_1005

Parameter	Conditions	Min	Typ	Max	Unit
Group Delay	delay of a sine wave with arbitrary frequency	*	*	14	ms
Step Response	Time until step response reaches stationary value	*	*	28	ms

Group Delay and Step Response were calculated for the whole signal path.

Parameter	Conditions	Min	Typ	Max	Unit
Phase Delay Difference	Any channel versus another	-4	-	4	ms
3db difference	Any channel versus another	-8	-	8	Hz

Req_1008

Parameter	Conditions	Min	Typ	Max	Unit
Update Rate	Rate, Acc	1875	2084	2293	Hz

Req_2223

Parameter	Conditions	Min	Typ	Max	Unit
CMG drive frequency	Internal clock is derived from CMG drive frequency. Therefore all sensor internal clock frequencies differ with a tolerance of +/-10% from nominal value. This parameter is just for information and no specified value. Frequency range might be changed during development.	22500	25000	27500	Hz

5.2.7 Filter Specification

Req_2279 The following filter specification is valid for the complete sensor including mechanical, analog and digital filter elements.

Req_1003

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Nominal Bandwidth	f_{3dB}		38	43	47	Hz
Req_1118 Variation of f_{3dB}	Δf_{f3db}		-10		+10	%
Req_1115 Pass Band Ripple	L_{max}	up to 10 Hz			|0.2|	dB
Req_1116 Stop Band Frequency	f_{stopp}	Damping of -60dB			165	Hz
Req_1117 Attenuation at 140Hz	L_{min}		35			dB
Req_2272 Damping Slope		ACC channel from f_{3dB} up to f_{stop}	-0,1293		-3,27	dB/Hz
Req_1004 Damping Slope		ARS channel from f_{3dB} up to f_{stop}	-0,1297		-3,26	dB/Hz

6. Technical Specification

Req_301 The technical specification contains the specifications which are guaranteed, if the device is handled and operated as defined in Chapter 2 "General"

6.1 Acceleration z-Channel

Req_2009

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement Range		Without electrical or mechanical clipping of complete signal path. Sensitivity, noise and linearity related specifications are only valid within the measurement range if not stated otherwise.	-5		+5	g
Req_336 Resolution					50	mg
Req_1134 Internal Headroom		DC stimulus, without electrical or mechanical clipping within the signal path until the final low pass filter. No flags will be set within this range except flags after the low pass filter	35			g
Req_1128 Zero Acceleration Offset		with active slow offset compensation in steady state	-10		10	mg
Req_1129		Directly after fast offset compensation (including startup drift) before active slow offset compensation is able to cancel residual error. Limits according SMI720 C-sample characterization. Final limits after C-sample validation.	-40		40	mg
Req_1131		Without fast or slow offset cancellation activated. Limits according SMI720 C-sample characterization and qualification. Comment: This is currently no released operation mode for SMI720.	-250		+250	mg
Req_1132		After fast offset cancellation but w/o slow offset cancellation activated. Limits according SMI720 C-sample characterization and qualification. Comment: This is currently no released operation mode for SMI720.	-500		+500	mg
Req_2220 Regulating Speed of the slow offset compensation			4.1	4.55	5.00	LSB/s

Req_1133

	Regulating Speed of the slow offset compensation		The given regulator speed applies for the nominal sensitivity of 5000 LSB/g. Sensitivity and nonlinearity error is not considered. For exact values please refer to regulation speed in LSB/s.	0.818	0.909	1	mg/s
Req_338	Output Width		at SPI-Output		16		Bit
Req_339	Output Range		at SPI-Output	-2^{15}		$+2^{15}-1$	LSB
Req_340	Sensitivity		nominal, referred to 16bit data word	n/a	5000	n/a	LSB/g
Req_341	Relative Sensitivity Error			-6		+6	%
Req_342	Hysteresis (x)		FOC/SOC not active; α< |1g|; @const. temperature.	-20		+20	mg
Req_1956	Cross Axis Sensitivity			-3,5		3,5	%
Req_343	Non Linearity		a < |5g|	-50		+50	mg
Req_345	Differential Non Linearity		Δa = 100mg	-5		+5	%
			Δa = 100mg	-5		+5	mg
Req_351	Voltage Dependence (x)		offset gradient	-20		+20	mg/V
Req_352			sensitivity gradient	-2.5		+2.5	%/V
Req_353			offset variation	-3.4		+3.4	mg
Req_354			sensitivity variation	-0.4		+0.4	%
Req_355	Temperature Dependence (x)		offset gradient	-10		+10	mg/K
Req_356			sensitivity gradient; step size =10K	-0.08		+0.08	%/K
Req_357			offset variation	-140		+140	mg
Req_358			sensitivity variation	-3		+3	%
Req_359	Noise		STD			12,5	mg
Req_360			peak-to-peak (6 x STD)			75	mg
Req_1135	Zero Acceleration Offset under EMC or PSRR test condition (+)		with active SOC in steady state	-50		+50	mg
Req_1136	Noise under EMC or PSRR test condition (+)		STD			20	mg
Req_361	Cross Axes Sensitivity		X- or Y-Axis	-3,5		+3,5	%
Req_362	Recovery Time		<500g or <1000°/s stimulus, duration >50ms. The output signal could be at clipping level, the acceleration signal path could be in			50 (*)	ms

		saturation and the acceleration sensing element could reach the mechanical clipping.				

Req_363 (x) w/o slow offset cancelation running.

(+) CR026

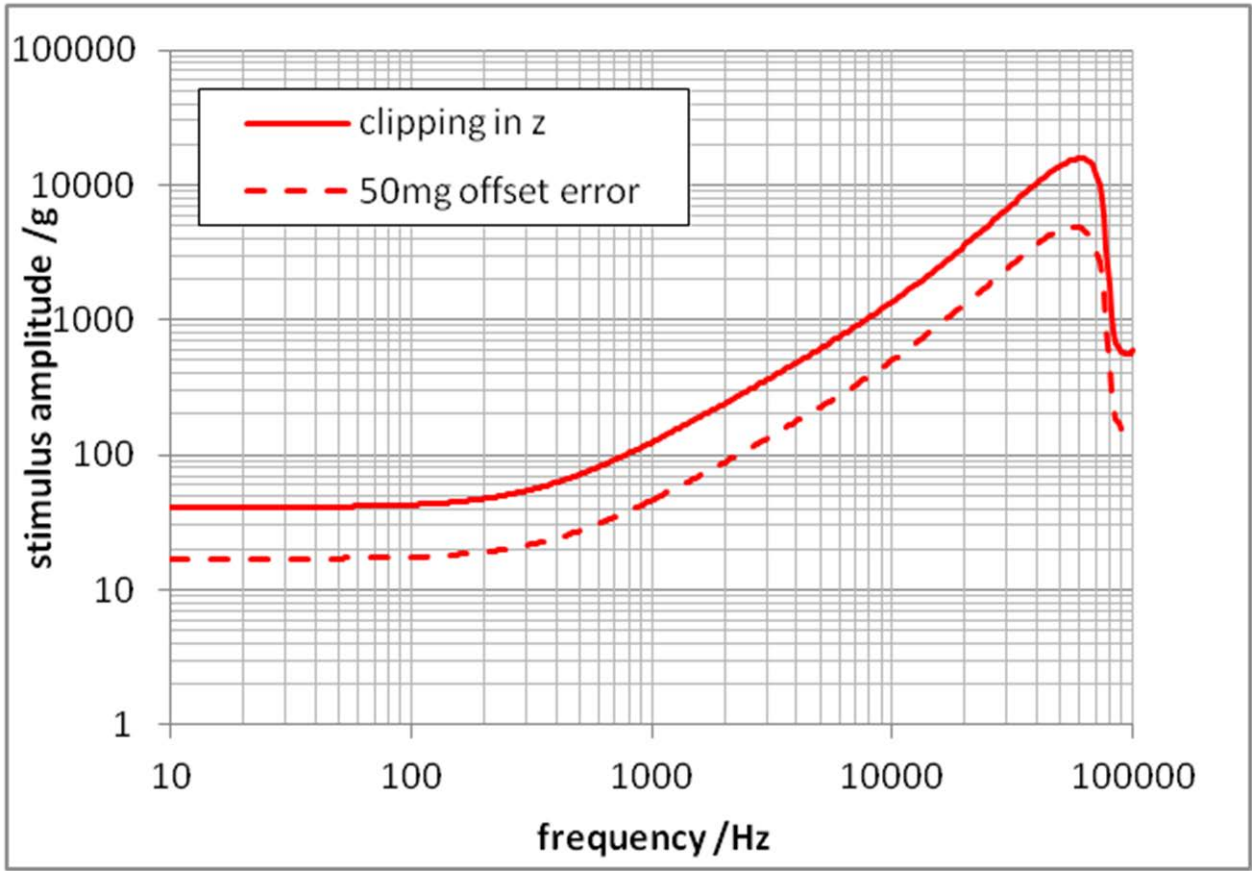
PSRR: Superimposed AC signal to power supply pins with amplitude +/-25mV. Frequency range: 50Hz - 1MHz. PSRR test will be performed up to 2 MHz. PSRR test will be performed with standard mean as well as a w.c. moving average mean (1000 samples total, moving average over 200 samples each, w.c. value of resulting 801 moving average values is taken). Std is calculated with 1000 samples.

EMC: Test conditions are specified in chapter "Product Qualification“ Req_703 (no w.c. moving average mean).

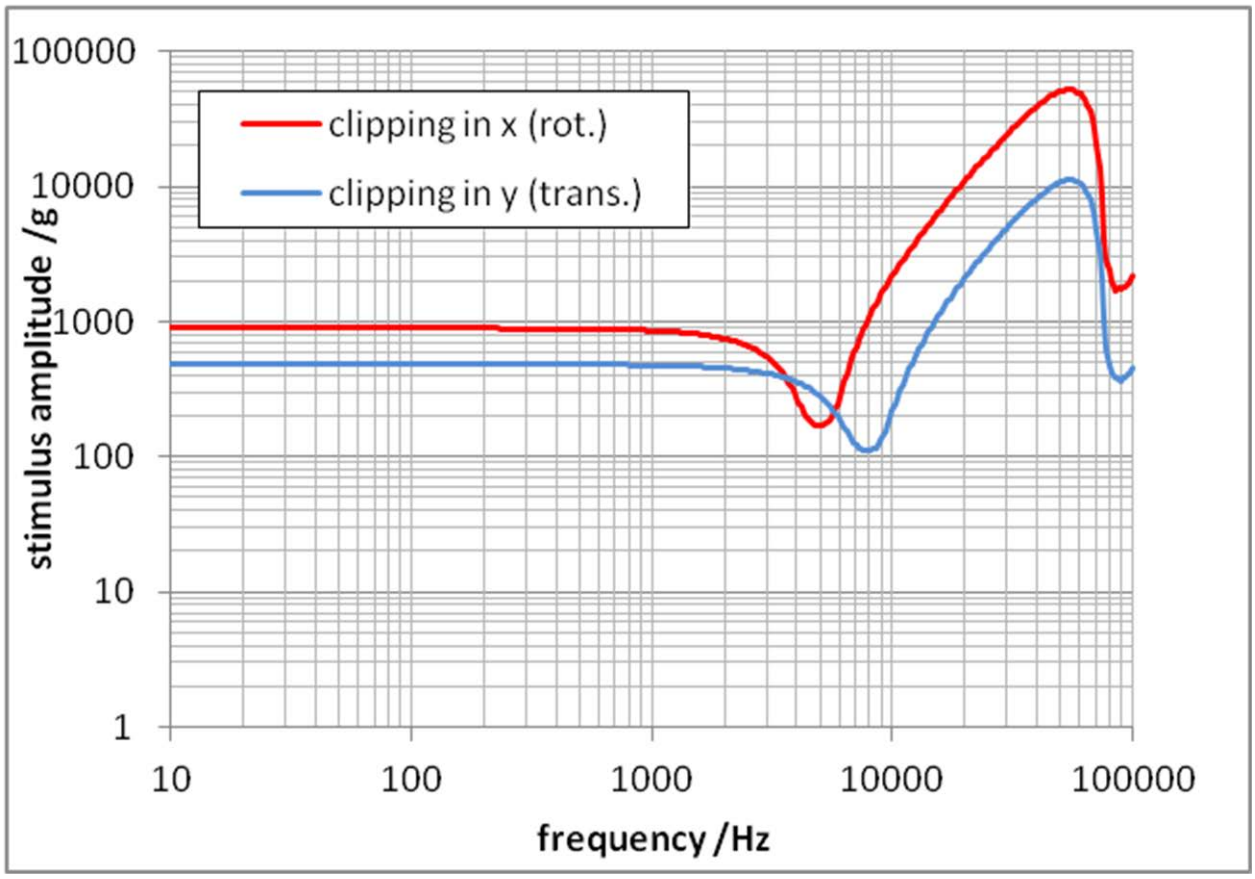
(*) Stimulus in any direction. If a DC stimulus of e.g. 500g or 1000°/s is present for a long time (minutes), a recovery to zero offset within 50 ms is not possible because of the slow offset controller. Recovery time is the time the sensor output signal returns to its real value (within specified limits) after exceeding the specified DC stimulus finishes. Proof by simulations and experiments as far as possible.

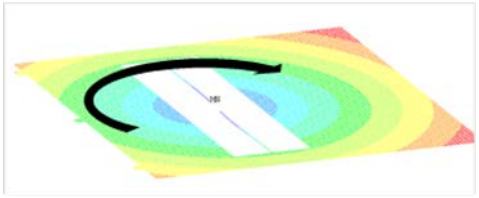
6.1.1 Vibration Robustness

Req_1106 50 mg offset error acceleration and clipping acceleration (hitting of stops in g-cell) in z-direction

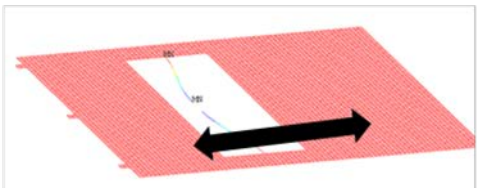


Req_1109 Clipping acceleration (hitting of stops in g-cell) in lateral direction





clipping direction 1:
rotational mode
(excitable especially in x-direction of SMI)



clipping direction 2:
translational mode
(excitable especially in y-direction of SMI)

Req_2008 The way failure flags will occur in an overload situation will be described after characterization of A-samples and discussed with the customers (the flag-limits are configurable).

6.2 Angular Rate Ω_x-Channel

Req_365

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement Range	Ω_x	Without electrical or mechanical clipping of complete signal path. Sensitivity, noise and linearity related specifications are only valid	-300		+300	°/s

			within the measurement range if not stated otherwise.				
Req_366	Resolution					+0,5	°/s
Req_367	Overload Range		DC stimulus, without electrical or mechanical clipping within the signal path until the final low pass filter. No flags will be set within this range except flags after the low pass filter	-1000		+1000	°/s
Req_1203	Zero Rate Offset		with active slow offset compensation in steady state	-1		+1	°/s
Req_1204			Directly after fast offset compensation before active slow offset compensation is able to cancel residual error	-1,5		+1,5	°/s
Req_1205			Without fast or slow offset cancellation activated. Limits according SMI720 C-sample characterization and qualification. Comment: This is no released operation mode for SMI720.	-7		+7	°/s
Req_1206			After fast offset cancellation but w/o slow offset cancellation activated. Limits according SMI720 C-sample characterization and qualification. Comment: This is no released operation mode for SMI720.	-14		+14	°/s
Req_2219	Regulating Speed of the slow offset compensation			4.1	4.55	5.00	LSB/s
Req_1207	Regulating Speed of the slow offset compensation		The given regulator speed applies for the nominal sensitivity of 100 LSB/°/s. Sensitivity and nonlinearity error is not considered. For exact values please refer to regulation speed in LSB/s.	0,0410	0,0455	0,050	°/s/s
Req_369	Output Width		at SPI-Output		16		Bit
Req_370	Output Range		at SPI-Output	-2^{15}		$+2^{15}-1$	LSB
Req_371	Sensitivity		nominal, referred to 16bit data word	n/a	100	n/a	LSB/°/s
Req_372	Sensitivity Error		relative error	-5		+5	%
Req_373	Hysteresis (x)		FOC/SOC not active; Ω < |300°/s|; step size = 5°/s.	-3°/s		+3°/s	°/s
Req_374	Non-Linearity		Ω < |150°/s|	-1		+1	°/s
Req_375			Ω < |300°/s|	-1		+1	°/s

Req_376	Differential Non-Linearity		Ω < |150°/s|; step size =5°/s	-20		+20	%
Req_377			Ω < |300°/s|; step size = 5°/s	-40		+40	%
Req_383	Voltage Dependence (x)		offset gradient	-0.2		+0.2	°/s/V
Req_384			sensitivity gradient	-4.2		+4.2	%/V
Req_385			offset variation; FOC/SOC not active; absolute offset variation due to voltage variation	-0.04°/s		+0.04°/s	°/s
Req_386			sensitivity variation	-0.7		+0.7	%
Req_387	Temperature Dependence (x)		offset gradient	-0.5		+0.5	°/s/K
Req_388			sensitivity gradient; step size =10K	-0.055		+0.055	%/K
Req_389			offset variation	-5		+5	°/s
Req_390			sensitivity variation	-3		3	%
Req_391	Noise		STD, A-samples STD, from C-samples on			1,5 0,7	°/s
Req_1920	Zero Rate Offset under EMC or PSRR test condition (+)		with active SOC in steady state	-1.5		+1.5	°/s
Req_1921	Noise under EMC or PSRR test condition (+)		STD			1.75	°/s
Req_392	Cross Axes Sensitivity			-3.5		3,5	%
Req_368	Recovery Time		<500g or <1000°/s stimulus, duration >50ms. The output signal could be at clipping level, but no failure flags (except dsp_rate_LF_out flag) are present, which means the rate signal path is not in saturation until the dsp-output limiter. Due to a DC shock of up to 500g the CMG drive structures could reach their mechanical limits. If this leads to an unlock of the PLL the recovery-time of <50ms could not be guaranteed because a new startup procedure is necessary which could take <150ms.			50 (*)	ms

Req_1959 (x) w/o slow offset cancelation running.

(+)CR026

PSRR: Superimposed AC signal to power supply pins with amplitude +/-25mV. Frequency range: 50Hz - 1MHz. PSRR test will be performed up to 2 MHz. PSRR test will be performed with standard mean as well as a w.c. moving average mean (1000 samples total, moving average over 200 samples each, w.c. value of resulting 801 moving average values is taken). Std is calculated with 1000 samples.

EMC: test conditions are specified in chapter "Product Qualification“ Req_703 (no w.c. moving average mean).

(*) Stimulus in any direction. If a DC stimulus of e.g. 500g or 1000°/s is present for a long time (minutes), a recovery to zero offset within 50 ms is not possible because of the slow offset controller. Recovery time is the time the sensor output signal returns to its real value (within specified limits) after exceeding the specified DC stimulus finishes. Proof by simulations and experiments as far as possible.

6.2.1 Vibration Robustness

Req_1214 Vibration sensitivities of the Rate channel. Due to reuse of the sensing element CMG240M till A0B-samples and CMG241M from A0C-samples on, the same vibration sensitivity as SMI710 is expected. From A0C samples on CMG241M will be employed. The vibration sensitivity of SMI720 with CMG241M is given below:

CMG241M

Störpfad	Frequenz [Hz]			Güte	Empfindlichkeit auf Vibrationsbelastung						Anschlagen aufgrund Vibrationsbelastung					
					Beschleunigungsanregung [g]			Drehratenanregung [°/s]			Beschleunigungsanregung [g]			Drehratenanregung [°/s]		
	Min.	Nom.	Max.	Max.	x	y	z	x	y	z	x	y	z	x	y	z
cQ-BITE Störbarkeit (1)	928 936	995 1040	1105 1148				13E-3 °/s/g 13E-3 °/s/g									
NF-Störbarkeit (2) F/Q-Störbarkeit F/Q-Störbarkeit NF-Störbarkeit (Antriebs-/Detektionsmode) NF-Störbarkeit (3, 4) 2F-Störbarkeit 53kHz-Störbarkeit (4)	3150 7500 11250 22500 41850 45000 46874	3500 8333 12500 25000 46500 50000 51880	3850 9167 13750 27500 51150 55000 57046	7000	2 °/s/g	2 °/s/g	180E-6 °/s/g 26-9 °/s/g 50E-6 °/s/g 2 °/s/g n.a. 6 °/s/g 5 °/s/g	0.5 °/s/°/s					5 g			40.0
Mode 3 Mode 4 Mode 5	35137 37629 41110	37250 39180 42585	39009 41304 44603	8122 1915 2081										26.4 °/s	25.8 °/s	
Mode 6 (5) Mode 7 (5) Mode 8 (5) Mode 9 (5) Mode 10 (5) Mode 11 (5) Mode 12 (5) Mode 13 (5) Mode 14 (5) Mode 15 (5) Mode 16 (5) Mode 17 (5) Mode 18 (5)	52346 52214 52593 59164 59427 59769 59498 74021 78995 82925 83967 85790 87184	53953 54040 54886 57894 61315 61703 61806 78116 81875 86289 87459 89812 91013	57527 57158 57135 61710 65366 65681 63417 82811 86548 90670 91989 94214 95443	18108 2648 2647 17279 3029 3043 2936 23187 4010 4210 4260 26580 28724								2.16 g	4.3 g 30.76 g	37.8 °/s	21.8 °/s	19.8 °/s 15 °/s 37.2 °/s
												3.54 g	11.64 g			

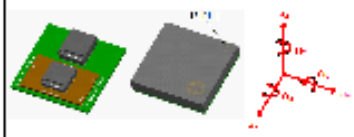
Fußnoten

(1) cQ-BITE in Serie vermutl. abgeschaltet (CR noch zu stellen)
(2) Angabe der Maximalstörbarkeit, genauer Verlauf im Tabellenblatt "NF-Störbarkeit" (aktuell noch A-Mu. Stand, Aktualisierung folgt)
(3) Wirkpfad vergleichbar mit NF-Störbarkeit um 3-fache Antriebsfrequenz herum
(4) Angabe nur zur Info, Frequenzen außerhalb spez. Bereich (>50kHz)
(5) Störbarkeit liegt immer zwischen 2f-Störbarkeit und paralleler Antriebsstörbarkeit (kein Überlapp), Werte nur experimentell bestimmt (kleine Stückzahl)

Erklärung Farbgebung

grün = Signalfehler <0.5°/s@250g oder <0.5°/s@100°/s; kein Anschlagen <250g oder <100°/s
gelb = Spezifikationsabweichung erwartet, Bewertung noch in Arbeit
rot = Signalfehler >0.5°/s@250g oder >0.5°/s@100°/s; Anschlagen <250g oder <100°/s

Achsenzuordnung AVT



x = CMG Sensierrichtung (auf Drehrate)
y = CMG Antriebsrichtung
z = CMG Detektionsrichtung

Sonstige Hinweise

Alle Angaben ohne AVT-Einflüsse, Werte gelten allein für CMG240M, die AVT-Überhöhung muss nachträglich verrechnet werden.

Alle Gütevorgaben beziehen sich auf absolute w.c. Werte (bei -40°C, min. Innendruck per Prozess)
Für Nominalgüten kann ein Faktor 0.7 angenommen werden, d.h. die Anschlagsbeschleunigungen erhöhen sich äquivalent um Faktor 1.4.
Die Einschwingzeit bis zum Anschlagen kann über 4*2*Güte/2/pi/Frequenz abgeschätzt werden.
Die Bandbreite der Moden im Frequenzbereich berechnen sich zu 2*pi*Frequenz/Güte.

Detaillierte mathematische Beschreibung der Vibrationsrichtlinie

Simulative Ermittlung des Anschlagens bei höheren Moden

6.3 Quadrature Channel

Req_2228

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sensitivity		nominal, referred to 16bit data word. Value is not calibrated at final test. This is the theoretical value derived from the different gains within rate- and quadrature-channel.	n/a	16,7	n/a	LSB/°/s

7. Safety Concept

7.1 Introduction

Req_501 Within this chapter, it is described how the safety requirements which arise from the ISO26262 (First edition 2011-11-15) are considered in the development of the SMI720. The requirements given in this document are valid for the sensor system (and not the top level system).

Req_502 In Section 7.2 the functional safety requirements as defined by CC and AE/SCS in the concept phase are documented. Any future changes in these requirements will be dealt with using the change request procedure used for all SMI720 change requests. Section 7.2 also contains some definitions. Section 7.3 describes the chosen safety architecture concept. In Section 7.4 the technical details of the safety concept are described (monitor functions and flags, error counters and error memory). Section 7.5 gives a forecast of metric values and section 7.6 specifies the criteria for safety validation of SMI720. Section 7.7 describes the flexibility and the validity of the safety concept.

Req_1359 The sensor module will provide angular (roll) rate and acceleration at the SPI interface. The notation "angular rate" is used synonymously for "roll rate" in general. The safety relevant functionality is the detection of faults (top events) within a certain time (Fault tolerant time interval, FTTI).

7.1.1 Definition of the Safety Element

Req_1223 The "element" is the sensor with its interface. (Denoted by "SMI720 Package" in the figure in Section 7.3.1) The "item" according to ISO26262 is the higher level system.

7.1.2 ASIL-Level and Decomposition

Req_509 All Error modes which affect angular rate and acceleration are developed according ASIL C (ISO 26262). There is no decomposition on element-level (sensor-level).

7.2 Definition of Functional Safety Requirements

7.2.1 Definition of Safe State

Req_507 The safe state is the operating mode of the sensor without an unreasonable level of risk. There are three possible states:

a) status flag set for corresponding channel

b) wrong checksum for response

c) no response

Wherever possible, a) will be used.

7.2.2 Definition of Errors

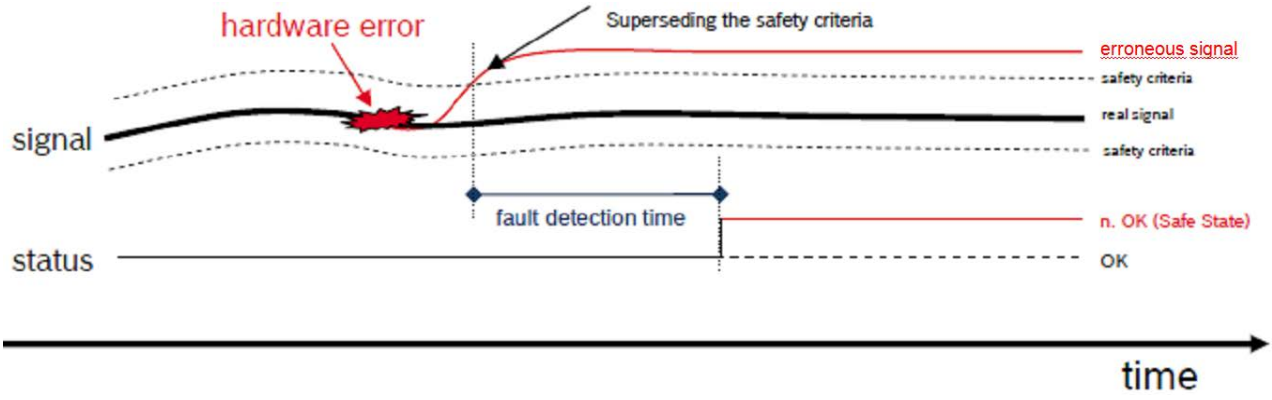
Req_576 Failure modes are defined by the customer in the following table.

The table should be read as follows:

The allowed residual failure rate which leads to an failure mode (F) may not be higher than the residual failure rate (R). The single point failure metric (S) to detect a fault within the fault tolerant time interval (FTTI) must be higher than SPFM. Systematic faults must be avoided according to an ASIL C.

Req_991

The target fault tolerant time interval (error detection time) is measured from the time, when the error criteria is superseded until the sensor is brought into any of its save states. The timing is depicted in the following figure.



Req_521 In general an error is present if the sensor does not comply with its specification. The following table specifies the error modes more precisely.

Req_522 If further error modes contribute to a significant deviation of the real signal to the signal at the sensor output, the sensor developer must notify about these error modes and the additional error mode must be updated within this specification.

Req_523 The following table should be read as follows:

The allowed residual failure rate which leads to an error E may not be higher than R.

The single point fail-ure metric to detect a fault within the time T must be higher than S.

Req_524 Example:

The allowed residual failure rate which leads to an rate offset jump higher than 14°/s may not be higher than 1e-8/h.

The single point failure metric to detect a fault within the 18ms must be higher than 90%.

Req_525 The symbol "+" denotes a logical OR, the symbol "*" denotes a logical AND, "!" denotes a logical NOT

7.2.2.1 Safety Top Events

Req_992 S

Error (E)	Critical Condition YAW-Rate	Symbol	FTTI	Critical Condition ACCELERATION	Symbol	FTTI
Offset Jump	> ±14°/s	R_1	18ms	> ±0.4g	A1	18ms
Offset Drift	> ±28 °/s / s	R_2	18ms	> ±8g / 1s	A2	18ms
Signal freeze		R_3	18ms		A3	18ms
Sensitivity Error	> ±7%	R_4	18ms	> ±7%	A4	18ms

Wrong Sign		R_5	50ms		A5	50ms
Phase Delay up to f_{3dB}	> 20ms	R_6	18ms	> 20ms	A6	18ms
Noise (STD)	> 2°/s	R_7	100ms	> 0.1g	A7	50ms

7.2.2.2 Quantitative and Qualitative Safety Targets for the Rate and Acceleration Channel

Req_527 S

Error (E)	Symbol	Residual Failure Rate (R)	Single Point Failure Metric (S)	Latent Point Failure Metric (L)
Offset Jump	R1, A1	-1e-8/h	90%	60%
Offset Drift	R2, A2	-1e-8/h	90%	60%
Signal freeze	R3, A3	-1e-8/h	90%	60%
Sensitivity Error	R4, A4	-1e-8/h	90%	60%
Wrong Sign	R5, A5	-1e-8/h	90%	60%
Phase Delay up to f_{3dB}	R6, A6	-1e-8/h	90%	60%
Noise (rms)	R7, A7	-1e-8/h	90%	60%
Any Error Event	R, A	-1e-8/h	90%	60%

Actual failure rates and failure metrics are calculated in the FMEDA-Sheet and will be documented in the safety analysis. Current calculation shows that the metric targets cannot be met.

Applicable for angular-rate failures: Above failures only concern rate failures, regardless of the state of the acceleration channel (R =R*(Az+!Az)= R*Az + R*!Az).

Applicable for acc failures: Above failures only concern acceleration failures, regardless of the state of the rate channel (A =Az*(R+!R)= Az*R + Az*!R).

7.2.2.3 Quantitative and Qualitative Safety Targets for Combined Error Events

Req_531

Error (E)	Critical Condition	Symbol	Residual Failure Rate (R)	Single Point Failure Metric (S)	Latent Point Failure Metric (L)
X_1	= R *A_z	X_1	-1e-9/h	97%	80%
X_2	= R+ A_z	X_2	*	*	*

Actual failure rates and failure metrics are calculated in the FMEDA-Sheet and will be documented in the safety analysis.

7.2.3 General Sensor Failure Monitoring

7.2.3.1 Memory Faults and Flipping Registers

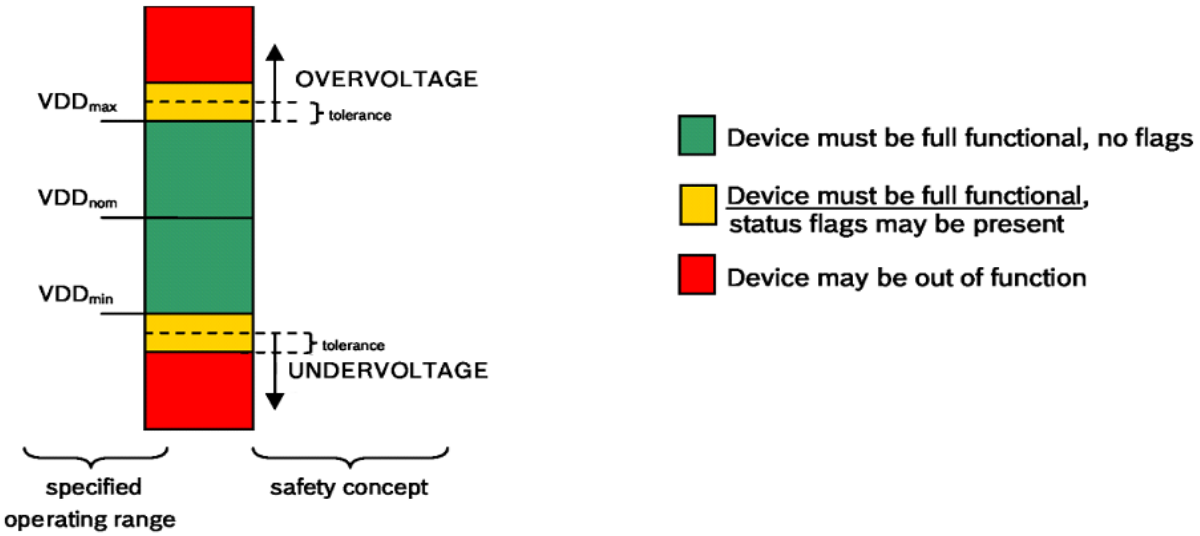
Req_578

Error (E)	Critical Condition	Symbol	FTTI	Remark
ROM (1,3,4)		M_1	18ms	Cyclic CRC and Parity
RAM (1,3,4)		M_2	18ms	Cyclic ifa13, soaf and checksum
OTP (1,3,4)		M_3	-	CRC check during start-up. No further OTP access when startup finished.
Req_582 Flipping Register (1,3,4)		M_4	18ms	Cyclic CRC, Parity or Check-Sum
Req_585 Interconnections (2,3,4)	short to ground short to supply short or neighbor	I_1	18ms	must be detected during operation
Req_588 External Components (3,4)	Resistors Capacitors Clock	C_1	18ms	must be detected during application
Req_590 Operating Conditions	Supply Voltage (3,4,5) Temperature (3)	O_3	18ms	Monitored temperature range may exceed the operating temperature range

Req_579 (1) only detection, no correction
Req_580 only detection, no correction
Req_583 only detection, no correction
Req_586 (2) Chip / Chip; Chip / Substrate; Substrate / Leadframe
Req_591 (3) in case of violation an error flag will be set

Req_592 (4) up to an active error flag the sensor will work according specification

Req_593 (5) definition of operating range and safety concept



Voltage Levels and Limits

7.2.3.2 Broken or Short Interconnections and External Errors

Req_1934 Opens of bonds and shorts between adjoining bonds were covered by the SMI720 safety concept. Opens of external pins and PCB lines, and shorts between external pins (balls of the BGA package) and PCB lines are not included in the metric calculations because this failure mode has to be systematically avoided by the system design of the ECU. A under and over voltage monitor at VDD3 is implemented.

7.2.4 Safety Documentation

Req_2066 All safety activities are documented in the SMI720 safety plan (see outgoing link).

Req_1968 Metric calculation will be done with Excel within an FMEDA. In general the metric calculation is alterable by the internal customer (delivery of unprotected excel files). The FMEDA reveals deep knowledge of the system design. It will be handled according to C/MSA-Zentralanweisung R05/06.1.

Req_1974 Metric calculation will be done in the same way as SMI700/SMI710. Thus, it does not include ESD, EMV and vibration influences. A hardware fault leading to a unwanted behavior of the sensor (e.g. broken EMV capacitor, malfunction detection of vibration, ...) is considered by design and application.

Req_1967 An FTA is done with FaultTree+ tool. The FTA reveals deep knowledge of the system design and may not be handed over to the customer. It will be handled according to C/MSA-Zentralanweisung R05/06.1.

Req_1969 An FMEA is done with IQFMEA tool. The FMEA reveals deep knowledge of the system design and may not be handed over to the customer. It will be handled according to C/MSA-Zentralanweisung R05/06.1.

Req_2068 FTA, FMEA and metric calculation will be documented in a way to be understandable for a sensor user. If needed, presentation/explanations will be provided.

7.2.5 Forecast Values for Safety Failure Rates and Metric Calculation

Req_1904 Residual failure rates and metric values are estimated on the basis of a preliminary FMEDA and FTA. First estimation of the metric values are currently in discussion and will be documented here when discussed with the customer.

The following failures (in sum: >100) have been considered up to now regarding their occurrence probability, their monitoring (direct and indirect) and their impact on the individual top events:

CMA failures (leakage, particles, mechanical breaks)

CMG failures (leakage, particles, mechanical breaks)

Chip-to-chip bond failures (bond rupture and shortage to neighbor bonds)

Acceleration frontends (failures of all blocks in both acceleration channels)

Angular rate frontend (failures of all blocks in drive and detection path)

Digital part of ASIC (DSP, bus system, interfaces, memory)

External bond failures (bond ruptures and shortages to neighbor bonds)

Voltage regulators

Charge pump, temperature sensors, oscillator

SPI Master Functionality and interfaces

POR

SCON-ADC

The following failure modes* for external components and open pins were used:

Capacitor@CP: 50% open, 50% short

Capacitor@1.8V: 50% open, 50% short

* distribution according to Berulini, except "drift" which has not been considered separately.

External components of the PSRR/EMC prefilter are not considered in SMI720-metric calculation.

Req_532 The metrics (absolute and relative) will be calculated and achieved on the basis of the input data given in the "Siemens handbook" (SN29500). The temperature profile will be assumed as specified in this specification as operating/non operating conditions.

Req_1966 For parts where there are no Siemens database (SN92500) values, Bosch error data base values are used. These values are scaled accordingly. The scaling is done in the same manner as done within SMI700/10 project.

Req_1965 Calculation of figures of each measurement axis is done by estimating/characterization the effect of an hardware failure to each top event. The sum does not need to fit the total failure rate of each channel. This is expected to be a reasonable way to calculate the failure rate for each top event and correlated and uncorrelated failures, but increases the failure rate in average.

Example: If a broken resistor can lead to an offset jump and/or to a sensitivity error, the failure rate of the broken resistor may be estimated as e.g. a probability

80% with effect on offset jump, 40% with effect on sensitivity drift and 50% with effect on noise or

50% with effect on offset jump, 90% with effect on sensitivity drift and 40% with effect on noise according to the best estimation.

Req_2245 For the calculation method and input parameters for metric calculation see Safety Analysis Report chapter 5.

7.2.5.1 Metric Calculations for the Rate Channel

Req_2062 Metric calculation for all rate channel top events is done for FTTI = 18ms for all top events. The table shows the envelope over all three temperature profiles.

Error (E)	Symbol	Residual Failure Rate (R)	Single Point Failure Metric (S)	Latent Point Failure Metric (L)
Offset Jump	R1	0.26e-8/h	99.1%	99.6%
Offset Drift	R2	0.27e-8/h	99.0%	99.6%
Signal freeze	R3	0.20e-8/h	99.3%	99.6%
Sensitivity Error	R4	0.30e-8/h	98.9%	99.6%
Wrong Sign	R5	0.06e-8/h	99.6%	99.3%
Phase Delay up to f_{3dB}	R6	0.05e-8/h	99.7%	99.4%
Noise (STD)	R7	0.27e-8/h	99.0%	99.6%
Any Error Event	R	0.45e-8/h	98.4%	99.6%

7.2.5.2 Metric Calculations for the Acceleration Channel

Req_2059 Metric calculation for all acceleration channel top events is done for FTTI = 18ms for all top events. The table shows the envelope over all three temperature profiles.

Error (E)	Symbol	Residual Failure Rate (R)	Single Point Failure Metric (S)	Latent Point Failure Metric (L)
Offset Jump	A1	0.98e-8/h	94.3%	99.4%
Offset Drift	A2	0.23e-8/h	98.7%	99.4%
Signal freeze	A3	0.72e-8/h	95.8%	99.4%
Sensitivity Error	A4	1.62e-8/h	90.6%	99.3%
Wrong Sign	A5	0.07e-8/h	99.6%	99.3%
Phase Delay up to f_{3dB}	A6	0.05e-8/h	99.7%	99.3%
Noise (STD)	A7	0.45e-9/h	97.2%	99.3%
Any Error Event	A	2.07e-8/h	88.0%	99.3%

7.2.5.3 Metric Calculation for Combined Error Events

Req_2065 Metric calculation for combined error events is done for FTTI = 18ms. The table shows the envelope over all three temperature profiles.

Error (E)	Critical Condition	Symbol	Residual Failure Rate (R)	Single Point Failure Metric (S)	Latent Point Failure Metric (L)
X_1	= R * A_z uncorr	X_1	0.95e-9/h	99.4%	99.3%
X_2	= R+ A_z	X_2	*	*	*

7.3 Safety Architecture Concept

Req_1227 This chapter will give a comprehensive architectural view on the SMI720 scope. It does not focus on the functional design of different blocks and their functional interactions, but focuses on their relation to safety topics.

Capital descriptors are the unique identifiers of the SMI720 scope which will be used in the safety analysis and metric calculation which is documented in an FMEDA.

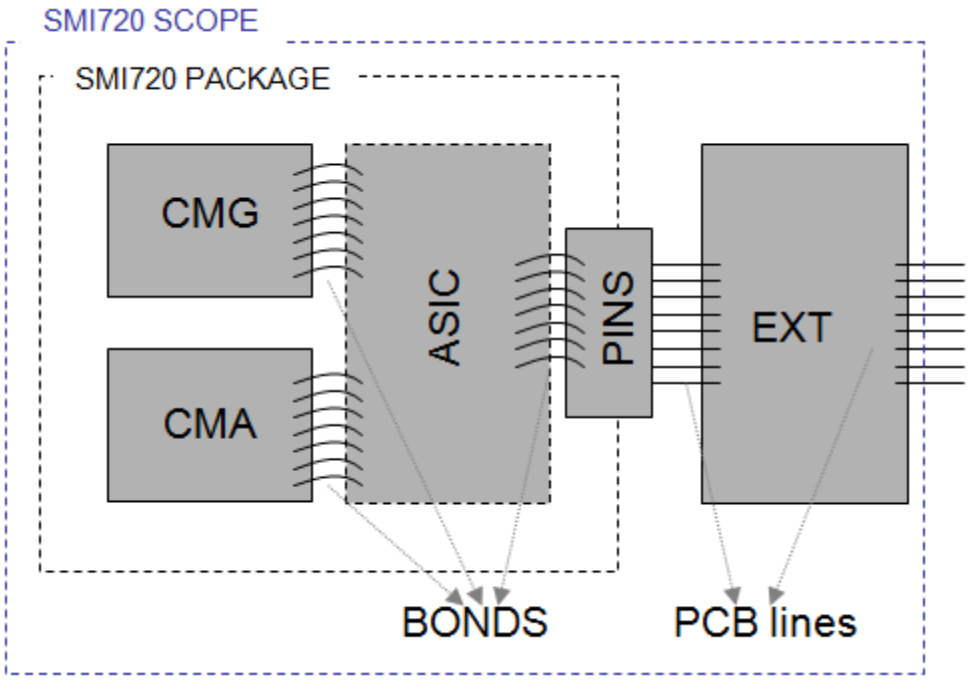
Atomic building blocks are visualized with a solid border line whereas building blocks consisting of sub blocks are marked with a dashed border line. For each atomic building block the failure modes used in the hardware metric calculations are described.

The function of transmitting data between different blocks is assigned directly to the block itself. The interface between blocks does not exist as own distinct block. Some interfaces are shown for the main signal path interfaces but not all interactions from blocks to blocks can be shown in this architectural overview.

Req_1228 In the following, the architecture will be described in detail. The failure mechanisms considered in the metrics calculation and their effect on the Top Events in is described, as well as the assumed monitoring mechanisms which are described in detail in.

7.3.1 System Architecture Overview

Req_1230 The following figures give an overview of the SMI720 safety scope:



Req_1231 The SMI720 consists of the following signal paths:

- Angular Rate (Ωx)
- Acceleration 1 (z low g)

Both channels are evaluated with a low-frequency filter with typ. 43Hz 3dB corner frequency.

Each signal path originates in its own micromechanical sensor structure, the acceleration sensor element (CMA); the angular rate sensor element is a separate chip (CMG). All micromechanical sensor elements are connected to one and the same ASIC using wire bonds (BONDS).

Req_1232 The SMI720 scope consists of the SMI720 package and the external circuitry as defined in the application descriptions. The Printed Circuit Board (PCB) lines are assumed to be non destructible and are not considered within the safety scope of the SMI720.

The external circuitry (EXT) stands for all external components like resistors, capacitances as given in the application descriptions. The SMI7 package consists of pins (PINS) connecting the package to the PCB, the integrated circuit (ASIC), and the micromechanical elements (CMA, CMG). All components are connected together with BOND connections.

The package itself is not considered explicitly in the following but its influence on the different elements is taken into account.

7.3.1.1 CMG

Req_1234 The CMG block is the micromechanical element to measure angular rate. A moving core is placed inside a hermetically sealed package. There are three failure modes:

Req_1235 CMG_PARTICLE:

This failure mode describes a particle which is inside the cavity, might touch or stuck the moving parts.

Req_1236 CMG_SPRING:

This failure mode describes that a spring of the core is broken or damaged. A damaged spring might lead to signal deviations.

Req_1237 CMG_LEAK:

This failure mode describes a leakage within the cavity. The leakage leads to a variation of the inside pressure and damping characteristics which may lead to a signal deviation.

Req_1238 All three failure modes may have impact on the angular rate offset, sensitivity and noise.

Req_1239 Monitoring is mainly done via monitoring S

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_drv_pi_tol, yrs_pll_unlock, yrs_pll_lim, yrs_drv_adc),
- the voltage at the TN electrode (yrs_rate_V_TN) and the common mode voltage (yrs_rate_V_com)
- the operation point of the Quadrature controller (yrs_quad_I_tol)

optional:

- the frequency (see external CMG_f_check).

Req_1240 The monitoring of the CMG is possible since the angular rate detection circuit is a closed circuit with feedback to the CMG, such that failures somewhere in the loop will be detected by several monitors. Therefore, a good diagnostic coverage can be guaranteed for the CMG.

7.3.1.2 CMA

Req_1242 The CMA block is the micromechanical element to measure acceleration in z-directions. It has the following three failure modes:

Req_1243 CMA_LEAK:

This failure mode describes a leakage within the cavity. The leakage leads to an variation of the inside pressure and damping characteristics which may lead to offsets or sensitivity deviations of the acceleration.

Req_1244 CMA_CORE1PARTICLE:

This failure mode describes a particle which is inside the cavity, might touch or stuck the moving parts and may influence acceleration offset and sensitivity.

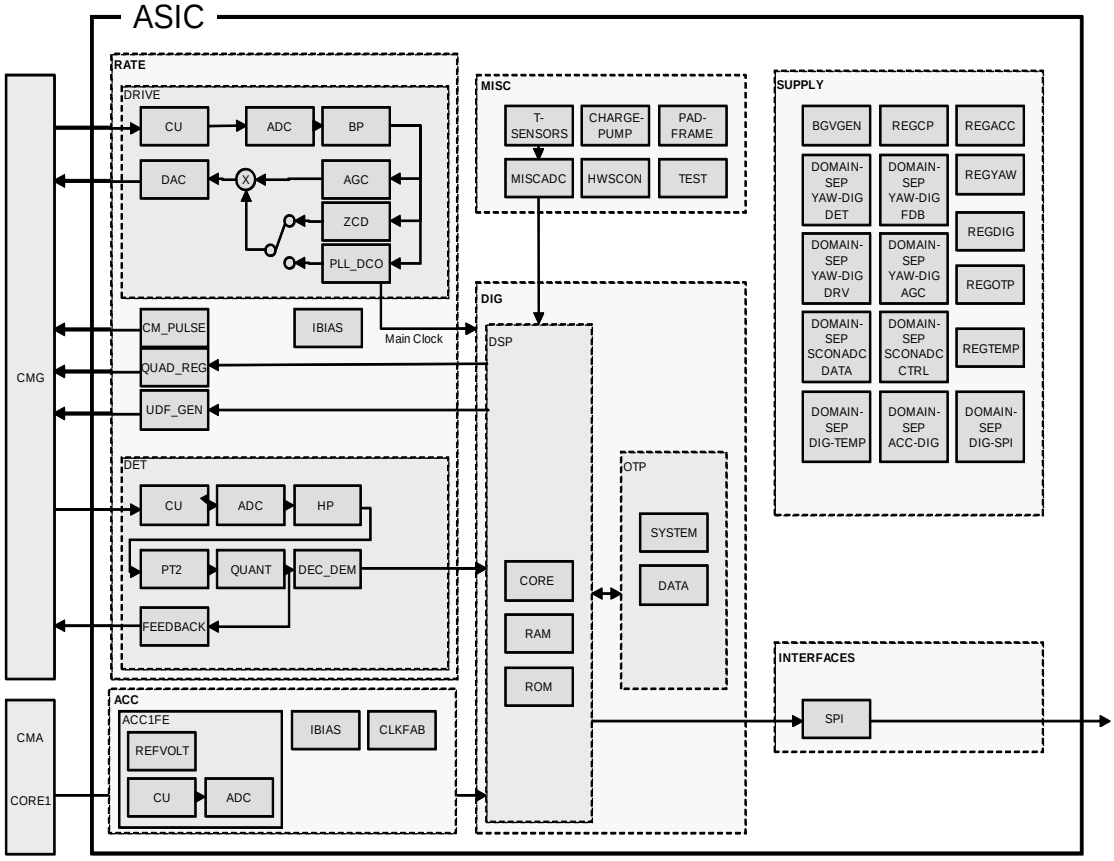
Req_1245 CMA_CORE1BROKENMECH:

This failure mode describes that a spring of the core or the CMA itself is broken or damaged. A damaged spring may influence acceleration offset and sensitivity, similar to a broken CMA because of changed ohmic resistances of the connection lines within the CMA.

Req_1246 Due to the extremely high requirements concerning vibration robustness of the sensor, the sensor is strongly damped. This prohibits the implementation of a continuously running self test including mechanical excitation of the sensor at frequencies outside the required band width. Without such kind of test, it is not possible to distinguish between an external acceleration and a failure within the sensor. Any monitoring needs to be done externally by plausibilization versus the external conditions (e.g., plausible roll rate). S

7.3.1.3 ASIC

Req_1248 The following figure gives an overview of the modules within the ASIC:



Req_1249 The ASIC consists of the main signal path for angular rate and acceleration. The micromechanic elements are controlled by the analog frontends for angular rate (RATE) and acceleration (ACC) which convert the analog to digital signals.

The digital part (DIG) consist of the main signal processing capabilities and is responsible for the whole control of the sensor and parts of the interfaces.

The interfaces (INTERFACES) transmit the sensor data as master or slave to the outside.

The supply power of the ASIC modules is regulated and controlled by different voltage regulators (SUPPLY).

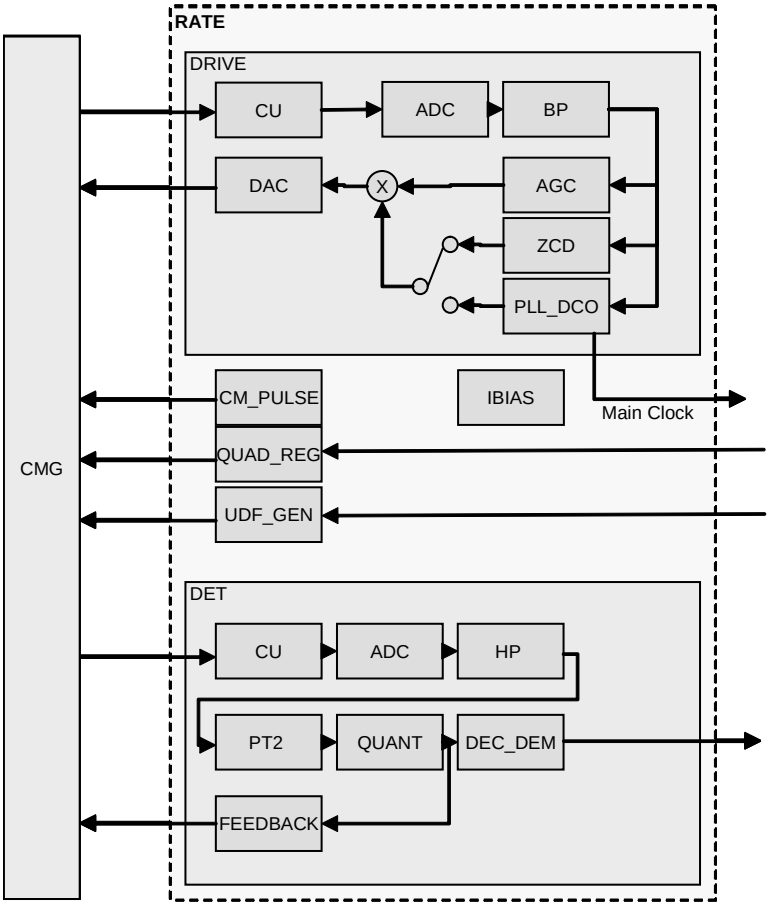
A remaining part of the ASIC (MISC) consist of additional control and test logic, safety functions, the charge pump and the temperature sensors.

The modules are complex integrated circuitry. Failures could exist in connections, gate oxides or resistors and capacitances. No distinct failure modes are distinguished for these atomic blocks, but the effects of malfunctioning of each block is considered.

All modules will be described in detail below, including the effects of failures in these blocks.

7.3.1.3.1 ASIC_RATE

Req_1251 The following figure shows the rate frontend block (and the CMG):



Req_1252 The Rate frontend consists of an amplitude control loop (AGC), a phase-locked loop (PLL) for clock recovery of the ASIC's main clock from the micromechanical oscillator (CMG), and an electromechanical delta-sigma loop to measure the Coriolis force using force feedback to the sensor element.

Amplitude control is realized by measuring the capacitance change at the drive electrodes, i.e. the displacement of the mechanical oscillation, using C/V conversion (CU) and adjacent A/D conversion (ADC). Any offset of the time discrete, quantized signal is cancelled by a band-pass filter (BP) without introducing phase delay in the signal band around 25kHz. In the AGC block, the amplitude of the sinusoidal drive signal is extracted and the amplitude offset with respect to the reference value is compensated by a PI controller. The controller value is finally modulated again with the drive frequency (from PLL) and applied to the sensor element by multiplication of a DC voltage offset to an AC rectangular voltage (DAC) driving the mechanical oscillator in terms of an electrostatic force.

Clock recovery during start-up and normal operation is done by the PLL. Phase/frequency offsets are calculated by sinusoidal multiplication and adjacent low-pass filtering of the drive signal with a reference signal from the digitally controlled oscillator (DCO). The phase error is compensated by a PI controller driving the DCO.

The zero-crossing-detection unit (ZCD) is a backup solution for start-up clock recovery inherited from former angular rate sensor generations. In such a backup configuration, during start-up, clock recovery is done by a hit-and-count algorithm. The oscillation period of the sinusoidal drive signal is obtained by counting the high-frequency clocks at 400kHz between two rising zero crossings of the signal. During this phase the DCO on the ASIC is kept at a fixed frequency. At certain amplitude of the drive signal, clock recovery is then switched to the PLL. The ZCD unit is disabled by default and does not influence the safety concept.

The delta-sigma loop of the detection unit captures the capacitance change, i.e. the displacement, of the Coriolis structure of the mechanical sensor element (CU). It is quantized by an A/D converter (ADC) and filtered to the desired transfer function by high-pass (HP) and band-pass filters (PT2). The feedback signal is reduced in quantization by a 4 Bit quantizer (QUANT), whereas this quantization is spread over time using pulse-width modulation in the feedback D/A converter (FEEDBACK). This results in a linear electrostatic force at the sensor element.

Additional components cover measurement pulse generation as the input voltage of C/V conversion (CM_PULS), force generation to compensate the quadrature error (QUAD_REG) – the crosstalk from drive to Coriolis displacement by non-ideal springs, and force generation used for electrostatic spring-softening in the Coriolis structure (UDF_GEN) to match the frequency of the Coriolis oscillator to the drive oscillator, which results in optimal suppression of quantization noise in the delta-sigma loop.

The failure effects of these blocks are:

Req_1253 All RATE_DRIVE blocks:

Malfunction may affect offset, sensitivity and noise of the angular rate.

Req_1254 All RATE_DET blocks:

Malfunction may affect offset, sensitivity and noise of the angular rate.

Req_1255 RATE_IBIAS:

Malfunction may affect offset, sensitivity and noise of the angular rate.

Req_1256 RATE_CM_PULSE:

Malfunction may affect offset, sensitivity and noise of the angular rate.

Req_1257 RATE_QUAD_REG:

Malfunction may affect offset, sensitivity and noise of the angular rate.

Req_1258 RATE_UDF_GEN:

Malfunction may affect offset, sensitivity and noise of the angular rate.

Req_1259 Monitoring of the DRIVE path is mainly done via monitoring S

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_drv_pi_tol, yrs_pll_unlock, yrs_pll_lim, yrs_drv_adc),
- the special CU and ADC gain test (overlayed pulse with 1/32 of the sensor frequency, flag yrs_drv_cu_gain),
- the under voltage detection of the charge pump (see flag v_cp_low),
- the quadrature controller (see flag dsp_quad_QI_lim),
- a possible overload of the drive ADC (see flag yrs_drv_adc).

Req_1260 Monitoring of the DET path is mainly done via monitoring S

- the limiter of the PT2 filter (see flag yrs_rate_pt2_lim),
- a possible overload of the quantizer (see flag yrs_rate_quantizer),
- the mean rate (DC level, operating point) of CU and ADC stage (see flag yrs_cpar1_cal_rate),
- the voltage at the TN electrode (see flag yrs_rate_V_TN),
- the feedback force (see flag yrs_rate_V_fb),
- a possible overload of the rate detection ADC (see flag yrs_rate_adc)
- the common mode (CN_CP) voltage (see flag yrs_rate_V_com).

Req_1261 Monitoring of the CM_PULSE module is mainly done via monitoring S

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_pll_unlock),
- the under voltage detection of the charge pump (see flag v_cp_low),
- the quadrature controller (see flag dsp_quad_QI_lim),

- the UCM-voltage, measuring the pulse on CM (see flag yrs_rate_V_CM).

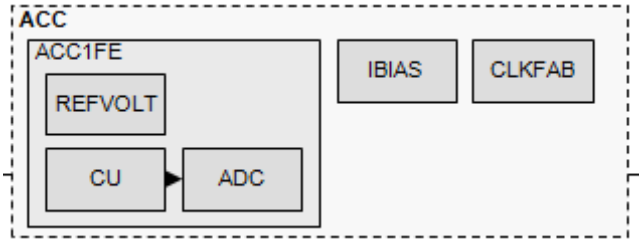
Req_1262 Monitoring of the QUAD_REG module is mainly done via monitoring S
- the operation point of the Quadrature controller (see flag yrs_quad_I_tol),
- the under voltage detection of the charge pump (see flag v_cp_low).

Req_1263 Monitoring of the module UDF_GEN is mainly done via monitoring S
- the voltage at the TN electrode (see flag yrs_rate_V_TN).

Req_1264 Monitoring of the IBIAS module is mainly done via monitoring S
- the drive force necessary to obtain the goal oscillation amplitude (see flag yrs_drv_pi_tol),
- the CU and ADC gain test (see flag yrs_drv_cu_gain),
- the drive phase and amplitude (see flag yrs_pll_unlock),
- the operation point of the Quadrature controller (see flag yrs_quad_I_tol),
- the deviation from required quadrature (0°/s) (see flag yrs_quad_HF_tol),
- the voltage at the TN electrode (see flag yrs_rate_V_TN),
- the feedback force (see flag yrs_rate_V_fb),
- the UCM-voltage, measuring the pulse on CM (see flag yrs_rate_V_CM).

7.3.1.3.2 ASIC_ACC

Req_1267 The following figure shows the acceleration frontend block.



Req_1268 The acceleration frontend contains a bias current generation (IBIAS) and a separate block (CLKFAB) which derives the ACC frontend clock from the angular rate clock (generated by the DCO, see below).

The signal processing which transforms the micromechanic deflection into a digital value is as follows.

First, the capacitance in the ACC core (which depends on the acceleration-induced deflection) is converted to a voltage signal (CU) before being converted into a digital signal by a sigma/delta convertor (ADC). An individual reference voltage (REFVOLT) is used to guarantee a good functioning of the transformation of the capacitance into a digital value.

The ACC FE functions within spec in the frequency range of 133,3kHz +/- 15%. Therefore, short-time frequency changes (including an unlocking of the Angular rate PLL) do not influence the ACC FE, hence, these flags are not related to ACC functionality.

The failure effects of these blocks are:

Req_1269 IBIAS:

Malfunction may affect offset, sensitivity and noise of both acceleration channels.

Req_1270 CLKFAB:

Malfunction may affect offset, sensitivity, sign and noise of both acceleration channels.

Req_1271 ACC1FE_CU:

Malfunction of ACC1FE_CU may affect offset, sensitivity and noise of acceleration channel 1.

Req_1272

ACC1FE_ADC:

Malfunction of ACC1FE_ADC may affect offset, sensitivity, sign and noise of acceleration channel 1.

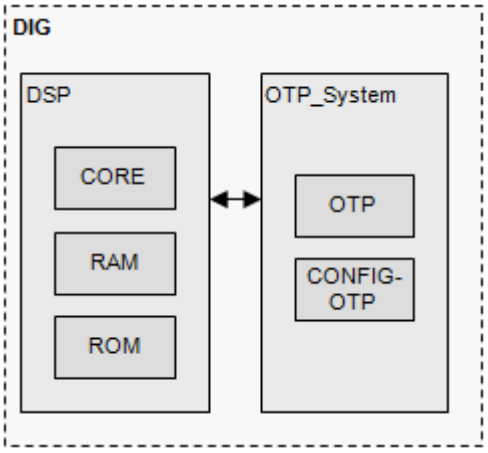
Req_1273 ACC1FE_REFVOLT:

Malfunction of ACC1FE_REFVOLT may affect offset and noise of acceleration channel 1.

Req_1274 Monitoring of the reference voltage and the bias is done via the monitoring of the voltage used to evaluate the capacitive changes of the CMA (acc1_V_cm,). The ADC is monitored by a bit train monitor detecting an implausible sequence of zeros ore ones (acc1_ds_lim). In addition, large signal peaks (which may be real, but may also be an indicator for an ADC malfunctioning) can be detected with an "energy flag" (acc1_overload_det,) which integrates the signal for a given time. These flags are no failure flags but indicator flags only. S

7.3.1.3.3 ASIC_DIG

Req_1276 The following figure shows the Digital block:



Req_1277 The digital block consists of the Digital Signal Processor (DSP) and the OTP-System.

In the DSP module, the angular rate and acceleration signals as well as the temperature signals are being calibrated and filtered. This is done by the DSP CORE using the filter code in the ROM and calibration and configuration data stored in the RAM (set by the boot loading process).

In addition, the temperature signal is calibrated.

Acceleration and the Angular Rate are filtered

- with low pass filters (40Hz, "low frequency"),

In addition, the quadrature controller of the angular rate path is located in the DSP.

The OTP-System consists of Main Ctrl, Bus System, boot loader, N-Value-function and OTP memory block:

In the OTP-System, several routines are implemented:

- the Boot Loader service which transfers OTP configuration and calibration data into the front ends, the DSP

- the HW-SCON including

  - the generation of several flags

  - the debouncing of the flags and setting of the general status flag, including the writing of the failure

The tasks are dealt by a scheduler with a timing raster of 500µs.

For SPI slave applications, the acceleration and angular rate signals are directly transferred to the SPI module.

The failure effects of the DSP module is:

Req_1278 DSP_CORE, DSP_RAM, DSP_ROM:

Malfunction may affect offset, sensitivity, sign, phase and noise of both acceleration channels and the angular rate channels.

Req_1280 Monitoring of the DSP_CORE module is mainly done via monitoring S

- the DSP online test (answering of test requests triggered by the µC software, see flag dsp_online_test),
- the program flow via checking the signature of program code (see flag dsp_pe_sign_err)
- the validity of the registers internal to the DSP via parity check of all registers (see flag dsp_pe_flag_err)
- the interrupt module within the DSP (see flag dsp_pe_irq_err)
- diverse limiters in the signal pathes of ACC1_LF, RATE_LF, Quadrature, Temperature
  (see dsp_..._in-flags at the input of the DSP,
  see dsp_..._adjust-flags after calibration,
  see dsp_..._out-flags at the output of the DSP)

Req_1281 Monitoring of the DSP_RAM module is mainly done via monitoring S

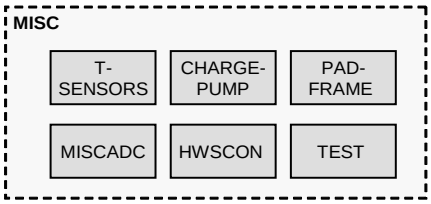
- the parity within each RAM cell (see flag dsp_pe_ram_err)
- the RAM address decoder (see flag dsp_ram_soaf_err)
- structural tests of the RAM cells (see flag dsp_ram_ifa13_err)
- the additional checksum test of the RAM cells containing configuration or calibration data (see flags dsp_adjust_data_err,)

Req_1286 Monitoring of the OTP-System and the OTP-CONFIG modules is mainly done via monitoring S

- the CRC check of the OTP (data and code OTP, cyclic_register_CRC)

7.3.1.3.4 ASIC_MISC

Req_1288 The following figure shows the MISC (miscellaneous) block:



Req_1289 The MISC block contains the CHARGEPUMP which provides high voltages (18-20V) for the angular rate frontend and also for the programming of the OTP.

The MISCADC is a analog/digital-converter which is used to digitize 6 analog monitoring signals for the SCON (resulting in flags yrs_rate_V_TN, yrs_rate_V_com, yrs_rate_V_fb, yrs_rate_V_CM, acc1_V_cm,) and is also being used to convert the analog voltages of the two temperature sensors (TSENSORS) into a digital signal.

The HWSCON (Hardware Safety Controller) includes the memory checks, the checks of the bus system, the pin checks, the over and under voltage checks, and the Power-On-Reset. In addition, the area needed for filtering of the MISCADC is taken into account in the HWSCON area.

Additional test logic which is only being used during wafer-level testing (and which is, therefore, not safety relevant) such as a screening aid for the regulators and a test multiplexer is summarized in the module TEST.

The PADFRAME corresponds to the area of the pads and the corresponding wiring.

The failure effects of the MISC modules are:

Req_1290 TSENSORS:

The temperature sensors are being used to correct the sensitivity and offset of acceleration and angular rate sensors over temperature. Therefore, offset and sensitivity as well as noise of angular rate and acceleration may be affected when the temperature sensors fail.

They are also being used to correct some monitors over temperature, but this does not have effects on the top events.

Req_1291 MISCADC:

Since the MISCADC is used to digitize the temperature signals, the effects are the same as for failed TSENSORS.

Req_1292 CHARGEPUMP:

In normal operation, the charge pump is only being used for the angular rate. A failed charge pump may therefore affect angular rate offset, sensitivity and noise.

Req_1293 PADFRAME:

Failures of the pads are not considered explicitly, but are taken into account via the bond failures (shortages and ruptures).

Req_1294 HWSCON:

Since currently, the MISCADC filtering is considered in the HWSCON area, the effects are the same as for the MSICADC. Besides that, failures in the HWSCON do not directly affect any of the top events.

Req_1295 TEST:

The functions summarized in TEST do not have impact on the top events.

Req_1296 Monitoring of the TSENSORS is mainly done via redundancy check of both temperature sensors versus each other (see flag ctm_diff). If a failure in a temperature sensor yields a signal that is out of the measurement range, this would be found via the flag ctm_range. In addition, a failure of the temperature sensor would indirectly be found via all temperature-dependent monitors. S

Req_1297 Monitoring of the MISCADC is done indirectly via all monitors (including the temperature checks) that are digitized by the MISCADC (see flags yrs_rate_V_TN, yrs_rate_V_com, yrs_rate_V_fb, yrs_rate_V_CM, acc1_V_cm, ctm_range, ctm_diff). Since the monitored voltage signals relate to different band gaps (acc band gap for acc1_V_cm, main band gap for all others and the ADC itself), the monitoring is considered to be good. S

Req_1298 Monitoring of the CHARGEPUMP is mainly done via monitoring S

- the voltage at the TN electrode (see flag yrs_rate_V_TN),

- the quadrature controller which will first try to compensate, but then saturate (see flag dsp_quad_QI_lim),

- the phase and amplitude of the drive path (see flag yrs_agc_irregular)

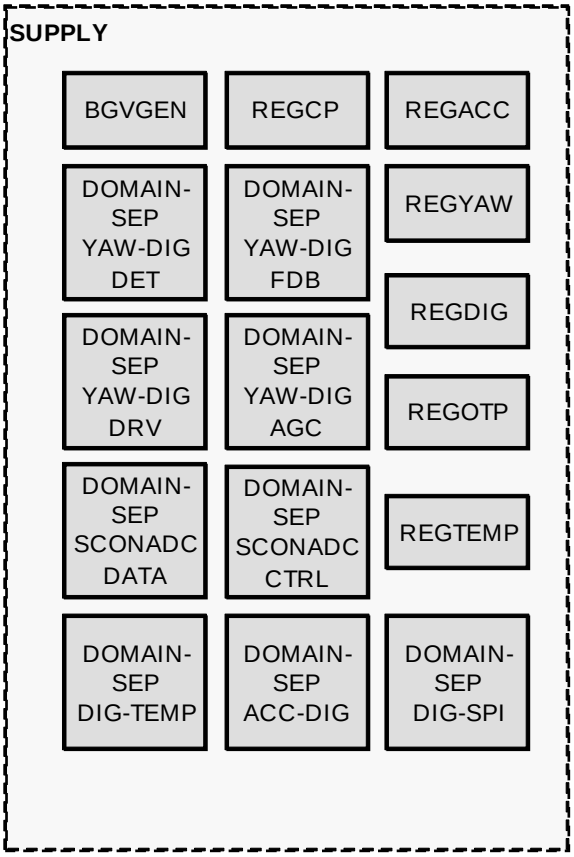
Req_1299 Continuous monitoring of the HWSCON is not necessary since there are no effects on the top events (except for the adc filtering whose monitoring is the same as for the TSENSORS and the MISCADC); nevertheless, the HWSCON is indirectly monitored by all flags that are handled by this module. In addition, it is scanned by the LBIST during startup to detect latent faults. S

Req_1300 Since the failure modes of the PADFRAME are taken into account via the bonds, no explicit monitoring is necessary.

Req_1301 Since the TEST functions do not have impact on the top events, no monitoring is necessary.

7.3.1.3.5 ASIC_SUPPLY

Req_1303 The following figure shows the Supply block:



Req_1304 In the SUPPLY block (see also, all supplies are summarized.

This voltage is further reduced

- by the charge pump regulator (REGCP) to ~2.9V, supplying the charge pump (ASIC_MISC_CHARGEPUMP),
- by the acceleration regulator (REGACC) to ~1.8V, supplying both acceleration frontends (ASIC_ACC),
- by the angular rate regulator (REGYAW) to ~2.8V, supplying the rate frontend (ASIC_RATE except DCO),
- by the temperature regulator (REGTEMP) to ~1.8V, supplying the temperature sensors (ASIC_MISC_TSENSORS),
- by the digital regulator (REGDIG) to ~1.85V, supplying the digital part (ASIC_DIG and ASIC_RATE_DRIVE_PLL_DCO) and
- by the otp regulator (REGOTP) to ~8V, being used for OTP programming.

The BGVGEN is the main band gap, used as reference voltage for all regulators except for the ACC regulator (REGACC) which has his own bandgap.

The module DOMAINSEP represents approx. 400 domain separators in which the data transfer between 1.8V and 3.3V is done. All data transferred between analog and digital part passes these domain separators.

The failure effects of the SUPPLY modules are:

Req_1305 BGVGEN:

A failure of the main band gap will result in a complete malfunction of the frontends and also of the digital part.

Req_1306 DOMAINSEP YAW-DIG DET:

Failures in the transfer between digital and analog part in YAW DET signal path may induce malfunction of the sensor and hence may affect angular rate top event.

Req_1960 DOMAINSEP YAW-DIG FDB:

Failures in the transfer between digital and analog part in YAW Feedback (closed loop) signal path may induce malfunction of the sensor and hence may affect angular rate top event.

Req_1935 DOMAINSEP YAW-DIG DRV:

Failures in the transfer between digital and analog part in YAW DRV loop may induce malfunction of the sensor and hence may affect angular rate top event.

Req_1961 DOMAINSEP YAW-DIG AGC:

Failures in the transfer between digital and analog part in YAW loop feedback over AGC may induce malfunction of the sensor and hence may affect angular rate top event.

Req_1936 DOMAINSEP SCONADC DATA:

Failures in the transfer between HW SCON and digital part (DATA) may induce malfunction of the sensor and hence may affect angular rate and acc top event.

Req_1962 DOMAINSEP SCONADC CTRL:

Failures in the transfer between HW SCON and digital part (CTRL) may induce malfunction of the sensor and hence may affect angular rate and acc top event.

Req_1937 DOMAINSEP ACC-DIG:

Failures in the transfer between analog and digital part in ACC signal path may induce malfunction of the sensor and hence may affect acc top event.

Req_1938 DOMAINSEP DIG-TEMP:

Failures in the transfer between digital part and T-Sensor may induce malfunction of the sensor and hence may affect angular rate and acc top event.

Req_1939 DOMAINSEP DIG-SPI:

Failures in the transfer between digital part and SPI Interface may induce malfunction of the sensor and hence may affect angular rate and acc top event.

Req_1308 REGCP:

Failures of the charge pump regulator will induce a malfunction of the angular rate measurement.

Req_1309 REGACC:

Failures of the acceleration frontend regulator will induce a malfunction of the acceleration measurement.

Req_1310 REGYAW:

Failures of the angular rate regulator will induce a malfunction of the angular rate measurement and also of the MISCADC (and hence, possibly also on the temperature correction of the acceleration signals).

Req_1311 REGDIG:

Failures of the regulator of the digital part may affect the DSP, the main clock (via the DCO) and the interfaces and hence have impact on all top events.

Req_1312 REGOTP:

This regulator is only being used for the OTP programming and has hence no effects on the top events (since the only programming that may take place during use is the storage of a failure event in the failure memory, which is not safety relevant).

Req_1313 REGTEMP:

Failures in this regulator may affect the temperature measurement and hence offset and sensitivity as well as noise of angular rate and acceleration.

Req_1314 Monitoring of the BGVGEN is mainly done via S

- the monitoring of the voltage used to evaluate the capacitive changes of the CMA (see flags acc1_V_cm); this monitoring references to a different band gap situated in the ACC frontend,
- the power-on-reset (POR).

Req_1315 Monitoring of the DOMAINSEP is mainly done indirectly via all flags of the frontends which all need to pass these separators. S

Req_1316 Monitoring of the PREREG is done via S

- over and under voltage detection (see flags VDD3_high, VDD3_low at the output of this regulator)
- indirectly via all other voltage monitoring flags (see below)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply

Req_1317 Monitoring of the REGCP is done via S

- over and under voltage detection (see flags V_CP_high, V_CP_low)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply in the angular rate frontend.

Req_1318 Monitoring of the REGACC is done via S

- over and under voltage detection (see flags V_ACC_high, V_ACC_low)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply in the acceleration frontend.

Req_1319 Monitoring of the REGDIG is done via S

- overvoltage detection (see flag V_DIG_high) and the under voltage detection (Power-On Reset, POR)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply in the DSP, the main clock (via the DCO) and the interfaces.

Req_1320 Monitoring of the REGOTP is not necessary since it has no effects on the top events. S

Req_1321 Monitoring of the REGTEMP is done via S

- over and under voltage detection (see flags V_CTM_high, V_CTM_low)

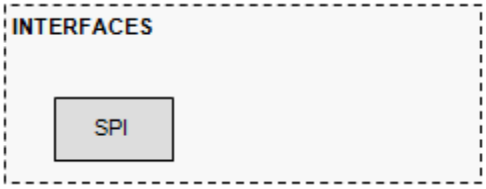
In addition, a failure of the temperature sensor would indirectly be found via all temperature-dependent monitors

Req_2067 Monitoring of the REGYAW is done via S

- over and under voltage detection (see flagsV_YRS_high, V_YRS_low)
- indirectly via dedicated flags that indicate a malfunction in the angular rate drive and detection path.

7.3.1.3.6 ASIC_INTERFACES

Req_1323 The following figure shows the interface block:



Req_1324 The ASIC contains one interface:

- a SPI interface (usually SPI slave, but alternatively useable as SPI master interface in some applications).

The failure modes are:

Req_1325 SPI:

A failure of the SPI module may induce wrong sensor signals and therefore affect all angular rate and acceleration top events in SPI slave applications and the data transfer top event in SPI master applications.

Req_1328 Monitoring of the SPI interface is done via S

- a working communication (including check of polarity, phase, number of clock cycles, validity of contained addresses)
- check of the CRC (3 bit, see chapter 4.3.7.3) included in the SPI message

7.3.1.4 BONDS

Req_1332 There are three different parts which are connected by chip to chip or chip to substrate bonds. Chip to Chip bonds are the bonds from the ASIC to the acceleration element (BONDS_CMA) and the angular rate element (BONDS_CMG). The bonds from the ASIC to the substrate pins (BONDS_PINS) are chip to substrate bonds.

In the following each single bond is denoted by the placeholder "*". For each bond connection, there are two different failure modes.

BONDS_CMA_*_OPEN, BONDS_CMG_*_OPEN, BONDS_PINS_*_OPEN:

This failure mode describes that the bond is open.

BONDS_CMA_*_SC_*, BONDS_CMG_*_SC_*, BONDS_PINS_*_SC_*:

This failure mode describes that two bonds are shorted to each other.

These are the potential effects of bond failures:

Req_1333 BONDS_CMA1_*_OPEN, BONDS_CMA1_*_SC_*:

may affect acceleration1 offset, sensitivity and noise.

Req_1335 BONDS_CMG_*_OPEN, BONDS_CMG_*_SC_*:

may affect angular rate offset, sensitivity and noise.

Req_1336 BONDS_PINS_*_OPEN, BONDS_PINS_*_SC_*:

may affect almost all top events via different mechanisms, except

BONDS_PINS_VSSA_SC_VSSD (no effect since VSSA and VSSD are shortened anyway within the package.

For details, pls refer to the FTA/metrics calculation.

Req_1337 S

Monitoring of acceleration bond ruptures and shortcuts (BONDS_CMA_*_OPEN, BONDS_CMA_*_SC_*) are mainly monitored by:

- the pin check module to detect ruptures of the substrate pins (see flag pc_cs1)

- the monitoring of the voltage used to evaluate the capacitive changes of the CMA (see flags acc1_V_cm) in case of bond shortages.

Req_1976 Monitoring an open bond connection to VDD_IO is not possible by SMI720 in every case (identically to SMI700/SMI710 and SMI5x sensors). Behavior if VDD_IO is open is described below:

Case1: Sensor is selected

- VDD_IO is supplied by MOSI and SCKL via back gate diode
- Depending on the driving capability of source at MOSI/SCLK an load capacitance at MISO timing of MISO would be corrupted
- This cannot be safely detected by CRC (only 3 bit CRC)
- In addition this situation may be detected by low voltage detection at VDD_IO (in this case the MISO will be set to high impedance)

Case2: Sensor is not selected

- MISO is set to high impedance (silence on the bus)
- VDD_IO is supplied by MOSI, SCKL, and CS
- Other sensors in the system may have additional load via MISO pin
- Timing of MISO of other sensors in system would be corrupted
- This cannot be safely detected by CRC of others sensors

Req_1338 Monitoring of angular rate bond ruptures and shortcuts (BONDS_CMG_*_OPEN, BONDS_CMG_*_SC_*) are mainly monitored by: S

- the pin check module to detect ruptures of the substrate pins (see flag pc_shd),

- the voltage at the TN electrode (yrs_rate_V_TN) and the common mode voltage (yrs_rate_V_com)

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_drv_pi_tol, yrs_pll_unlock, yrs_pll_lim, yrs_cpar1_cal_drive_int),

- the operation point of the Quadrature controller (see flag yrs_quad_I_tol),

- a possible overload of the rate detection ADC (see flag yrs_rate_adc),

- the voltage at the TN electrode (yrs_rate_V_TN) and the common mode voltage (yrs_rate_V_com),

- the quadrature controller (see flag dsp_quad_QI_lim)

Req_1339 Monitoring of pin bond ruptures and shortcuts (BONDS_PINS_*_OPEN, BONDS_PINS_*_SC_*) are mainly monitored by: S

- the pin check module to detect voltage level differences between VSSA, VSSD (see flags pc_vssa, pc_vssd) that may indicate ruptures or shortages,

- a power-on reset (POR) in case of a shortcut in the supply pins

- the functioning of the communication via the interfaces.

For details, pls refer to the FTA/metrics calculation.

7.3.1.5 EXT

Req_1341 SMI720 needs, for proper functionality, several external electrical parts such as capacitors and resistors.

The blocking caps for VDD1_8 and CPUMP are necessary parts.

The components are:

EXT_C_CP: blocking cap at the charge pump

EXT_C_VDD18: blocking cap at VDD1_8

EXT_C_VDD3: blocking cap at VDD3

The effects of OPENs and SHORTs are:

Req_1342 EXT_C_VDD18_OPEN:

Loss or malfunction of the blocking caps at VDD1_8 may affect proper functionality of the digital signal processor and can affect offset, sensitivity and noise of acceleration and angular rate.

Req_1343 EXT_C_VDD18_SHORT, EXT_C_VDD3_SHORT:

Shortage of these capacitors means a short-circuit of the supply, therefore the whole chip will stop operation. All top events are affected.

Req_1344 EXT_C_CP_SHORT:

Shortage of the charge pump may affect offset and sensitivity of the angular rate.

Req_1349 Monitoring of an open or shortened charge pump capacitor (EXT_C_CP_OPEN, EXT_C_CP_SHORT) is mainly done via S

- monitoring the phase and the amplitude of the angular rate (see flags pll_unlock and yrs_agc_irregular)
- the voltage at the TN electrode (see flag yrs_rate_V_TN)
- no communication any more (due to under voltage)

Req_1350 Monitoring an open blocking cap for VDD1_8 (EXT_C_VDD18_OPEN) is mainly done via S

- the overvoltag detection of the digital supply voltage (see flag v_dig_high) and the undervoltage reset at VDD1_8.
- the potential malfunction of the digital part.

A-samples: In TIG720AA a dedicated flag for the ripple detection of VDD1_8 was implemented (flag pc_vdd3_vdd1_8) which was not functional at all. Because of a sufficient diagnostic coverage in case of a top event relevant EXT_C_VDD18_OPEN this monitor was droped for SMI720 C-samples (TIG720BA).

7.3.1.6 PINS

Req_1356 For this BGA package, each pin consists of the solder joint between the substrate printed circuit board of the SMI720 and the printed circuit board of the top level hardware. All pins are described in section {REF:4.1 Pinning & Layout} of the datasheet. In the following each single pin is denoted by the placeholder "*". There are two failure modes known for the PINs. S

PINS_*_open:

This failure mode assumes that the connection is totally open between SMI720 and the external printed circuit board.

PINS_*_SC_*:

This failure mode describes the error that a pin has a shortcut to another pin

The effects of open pins are the same as in chapter "BONDS".

Req_1987 The results of the PIN-FMEA were provided to the customer. The reaction of the SMI720 in case of pin opens or shorts to their neighbours, VDD3 and GND are described within the SMI720 Pin-FMEA. The results of the Pin-FMEA need to be considered for ECU design.

7.4 Outline of the Monitoring Concept

Req_1361 The SCON continuously monitors each functional block, detecting HW failures which could result in incorrect signals being transmitted over SPI and marking these signals with error flags. In order to detect these failures the SCON has dedicated HW (AD-Converter, registers); the evaluation of errors and S

running of algorithms/tests is also done in hardware. It is not possible to separate the HW associated with the different channels and the functional safety requirements must be applied for all functional blocks related to the different Top Events.

Using a metric calculation (based on FTA/FMEDA methods) in the concept phase it has been determined whether such failures exist and the corresponding failure rates and SPFM will be evaluated. The SCON monitors are based on the SMI700 architecture, with limitations, since the SMI720 has no microcontroller with additional monitor functionality. Nevertheless the SMI720 safety concept is designed to provide comparable diagnostic coverage.

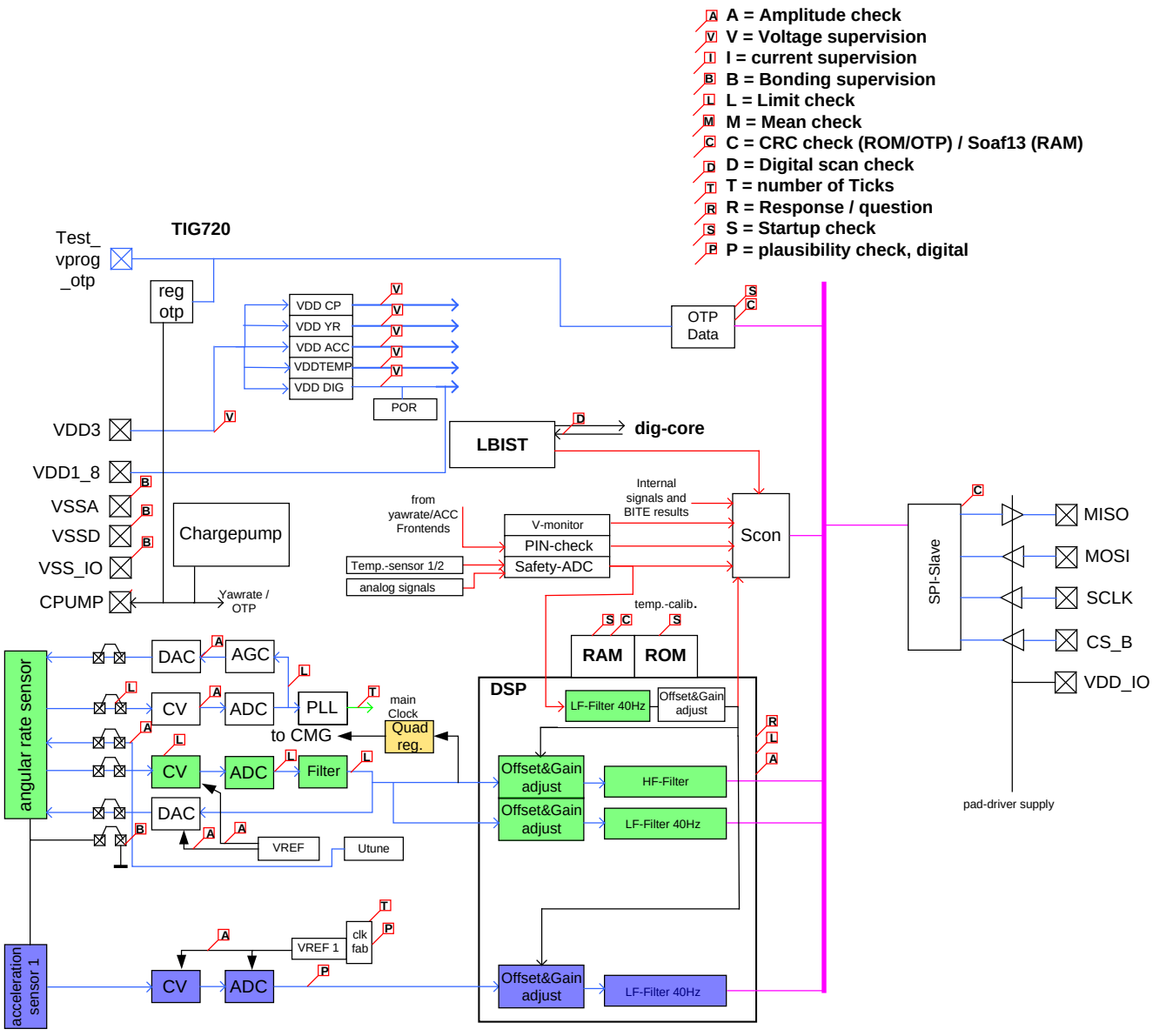
The HW-SCON checks the DSP continuously (dsp_pe, dsp_pe_sign, dsp_pe_irq, dsp_online_test).

The temperature range is checked via two redundant temperature sensors (see flag ctm_range, ctm_diff).

In the case of an error being detected, the SMI720 communicates this to the next system level (normally the ECU of the affected system). If possible (i.e. if the technical fault allows) the sensor will continue to communicate, marking the affected signals as incorrect (Channel Information). This emergency operation mode allows the System ECU to assess the fault, and if compatible with the system safety goals the remaining signals may continue to be used.

The SMI720 does not switch itself off automatically (except for too low voltage in the digital core which will lead to a power-on reset); it is the task of the system ECU to decide on the basis of the SMI720 error flags which signal information to use. For this reason no assumptions have been made with respect to system or driver actions. Signals marked with an error channel status are to be considered incorrect, and not to be used for safety relevant systems.

Req_1362



Monitor overview in the TIG720

7.4.1 Startup Monitoring

7.4.1.1 Memory Tests

Req_1365 During startup, the memories will be tested first. The RAMs will get a structural test at startup (SOAF, IFA13). S

The DSP-ROM and OTP will be checked initially with a one shot CRC to detect bad programming of OTP cells.

For further information on RAM Testing see {REF:Req_1763}.

Once LBIST is configured, the system starts LBIST. The digital circuit is scanned. After LBIST, the system generates again a reset and bootloading is started. The system will know that the LBIST has been started once and disables the LBIST this time. For further information on LBIST see 7.4.1.2.

After initial memory tests, the continuous memory tests are being started, e.g. continuous SOAF and IFA13 and parity checks for the RAMs. For details, refer to {REF:Req_1763}.

Cyclic register check is done on special registers with influence on safety relevant top events.

7.4.1.2 LBIST

Req_1367 At each startup, a structural digital scan test is carried out, called LBIST. It checks the whole digital part except the Test Mode Controller (i.e., Clock Multiplexer and Scan Mode configuration), since this part is necessary to control the LBIST itself, and some digital gates in the ACC Frontends (i.e. the ACC clock fab). Variable pattern sequences can be generated. S

The test will be carried before startup of the sensor frontends and the boot loading of the system. The configuration of the LBIST will be performed by the boot loader routine by config tuples of type 16bit. At the end of the LBIST configuration the last tuple will initiate the LBIST procedure by writing LBIST_START. When the LBIST is completed, the Test Controller will issue a reset to the system, which will reboot the boot loader. The boot loader will again configure the LBIST and try to start it, but the LBIST will ignore the request and thus the program execution and start of the system will continue.

Compared to the externally controlled LBIST used during wafer-level testing, this integrated LBIST is less powerful. The integrated LBIST checks for stuck-at faults with an estimated fault coverage of ~63%.

Since it is being carried out only once at startup, it is only being used for latent faults.

7.4.1.3 Startup of Continuous Monitoring

Req_1369 Concerning startup behavior, the flags can be split into the following categories: S

Frontend and DSP flags:

Right from the start, the Frontends and the DSP will start generating flags (interrupted by the LBIST) which will be handled "transparent" (no accumulation) by the HW-SCON.

After boot loading, the Software releases the frontends ("FE release", ~ 20ms), leading to the initiation process in the Frontend (frequency finding etc).

In this phase, the HW SCON starts monitoring signals and setting internal flags. This phase ends with a locked PLL (yrs_pll_unlock = 0) and regulated AGC (yrs_agc_irregular = 0) (“FE locked”)

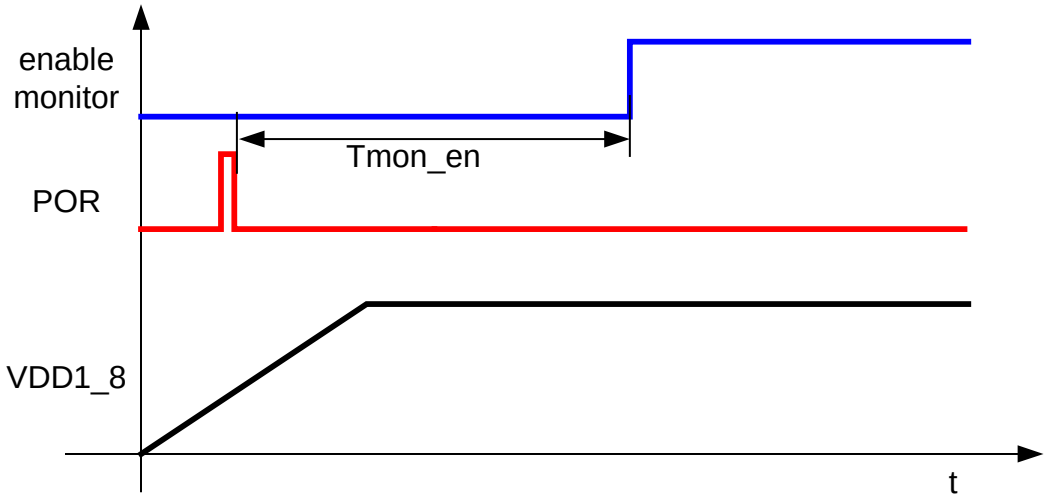
At this time, the HW SCON starts accumulating the flags (= removes transparency from all flags that were transparent before).

When, in addition, the quadrature regulator is ok (yrs_quad_I_tol = 0, set by the SW), ("FE ready", ~150ms), the SCON starts evaluating the flag's effect on the failure counters and hence, on the Channel Information flags (2bit-Status).

Supply flags:

The supply monitoring flags will not be set prior to "FE release" (Bootloading accomplished). They will remain transparent until "FE ready", similar to the Frontend and DSP flags.

The over/under voltage monitors will be active at least 50 msec (Tmon_en) after power on reset has created the reset pulse.



Only the low voltage monitor of the digital core (on the 1,8V line behind regulator), leading to a Power-On-Reset, is active from the start on and cannot be disabled.

DSP online test (carried out by SCON) starts with "FE release" and is not transparent.

The **memory tests** are active from the start on (interrupted by the LBIST).

The **pin checks** are dependent on the clock and do therefore not start earlier than "FE release".

The **Bite** flags can only be set during Bite phase.

7.4.2 SCON Error Handling

7.4.2.1 SCON Incoming Flags

Req_1372 From the SCON point of view, there are three sources of error flags: S

1) flags deriving directly from the LBIST, frontends, DSP, internal bus or bootloader (set by HW)
2) flags or resets which are generated by over- and undervoltage detection circuits
3) flags resulting from SCON-based checks of selected signals and BITE-test (set by HW-SCON)

All sources of the flags are responsible to set and remove the flags according to their correct status.

The flags are collected into the following clear-on-read registers:

1) The “internal flag list” (error_flag_16_bankX with X=8:0) which can be read out by SPI interface in order to get detailed information which flags were active and caused the CI-flag.
2) The “16bit Info cluster” which can be read out by SPI interface in order to get an overview which classes of failures were active (definition of the classes see table)

1) and 2) are cleared as soon as the read request has been received by the sensor. If any succeeding error in the communication occurs, e.g. CRC error in the SPI response frame due to disturbances, the information is lost and cannot be recovered.

All internal flags are feed into three error counters which debounce the flags with temporary weight. Flags with a permanent weight have a direct feed through to the CI flag and will not disappear if set.

7.4.2.2 Error Counters and Channel Status Flags

Req_1374 Every flag may act as an input for all failure counters. These error counters work like low pass filters, S

so that errors flags at the interfaces do not toggle around the limits.

The flag list for the SCON will be read out and evaluated by the SCON with 1kHz. It is predefined in TIG720 which flag can act on which failure counter (see table …). Each flag may have the following weights (initialized by OTP):

11 the flag is masked and does not act on failure-counters 0-2

01 the flag acts with weight 1 on the assigned failure counters 0-2

10 the flag acts with weight 2 on the assigned failure counters 0-2

00 the flag acts immediately and permanently on the failure counters 0-2

The failure counters will be increased with the maximum weight of the assigned and active flags (see below).

Once a flag with weight “00” acts on a failure counter, the counter will be set to a value above the limit and will not be decreased again, resulting in a permanent CI flag until the next reset.

The SCON holds three 8 bit registers for the error counters called

ec0_yrs_lf

ec1_quad_hf

ec2_acc_lf

The registers are read-only and capable of in SPI protocols: CC32IN, Open32 and SPI64.

The reset value for the registers is 0x00000000.

The error counters are configurable, so that the error latency timing defined at the beginning of this chapter is not exceeded, and an error is transmitted as long as corrupted data is still present in the filter chain (filter flush time). For that purpose, the limit (ec x_...._config, page3 ID 0x1-0x3) and the hold time (dsp_flush_time, page3 ID 0x0) need to be configurable individually via the boot loading process and via customer SPI.

As soon as the limit of a counter is exceeded, the corresponding channel status flags (CI) are set to 1. When passing the limit or in occurrence of an additional active SCON flag when being above the limit, the counter is increased such that the automatic decrease of the counter passes the limit after the “Hold time”.

The channel information (CI) bits can have the following values:

0: channel sensor data fully valid

1: channel sensor data not valid --> if one or more of the following cases happen :

1) temporary or permanent sensor error

2) initialization is running

3) self test is running

4) fast offset cancelation is running

5) slow offset cancelation is not running

Req_1375 **Schematic flow of the SMI720 internal error counter with active temporary or permanent flag weight:**

The hold time of each error counter is defined by the dsp_flush_time (page3 / ID 0x0).

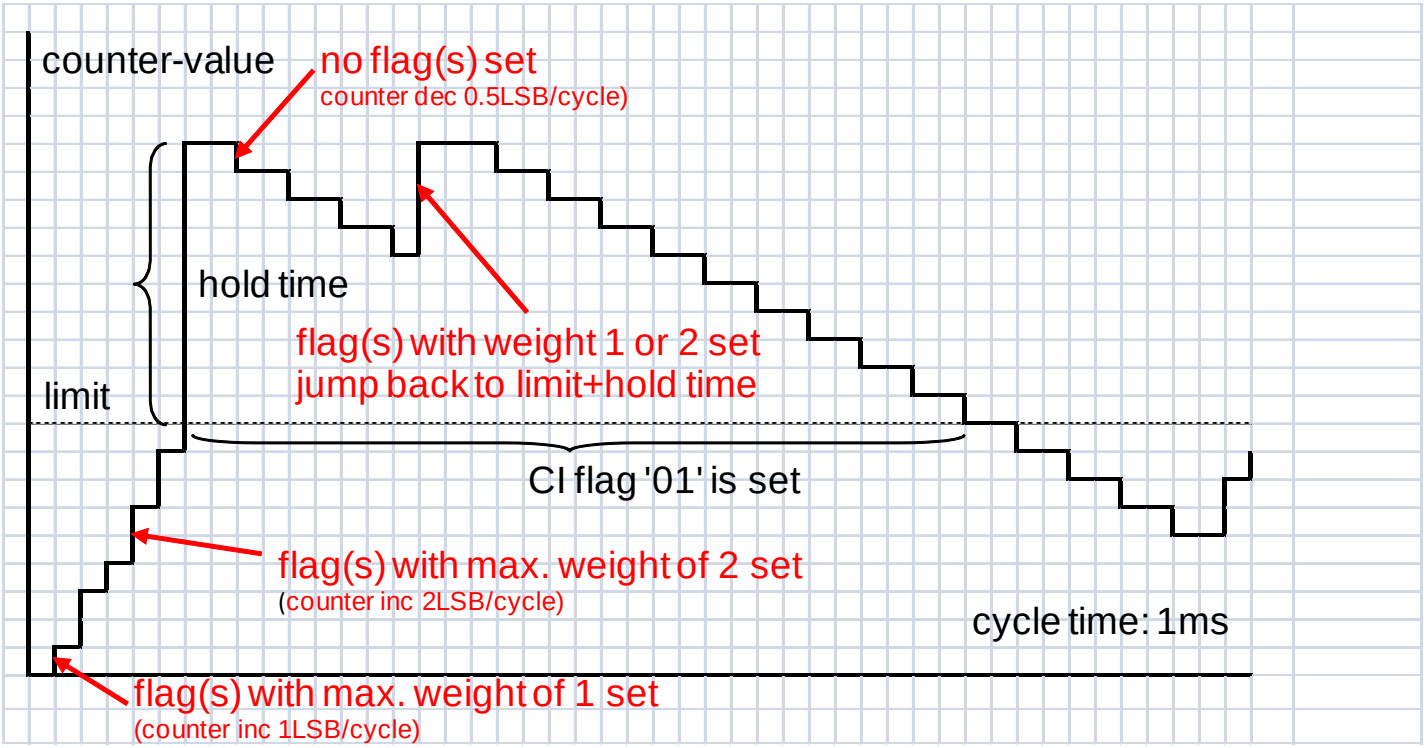
Example: When dsp_flush_time is configured with 10LSB a CI bit remains set (after the error event disapeared) for the time of

- SMI720 A-samples: 20ms +/-10% (because of a decrement with 0.5LSB/cycle above the error counter limit, cycle time = 1ms+/-10%)
- SMI720 C-samples: 10ms +/-10% (because of a decrement with 1LSB/cycle above the error counter limit, cycle time = 1ms+/-10%)

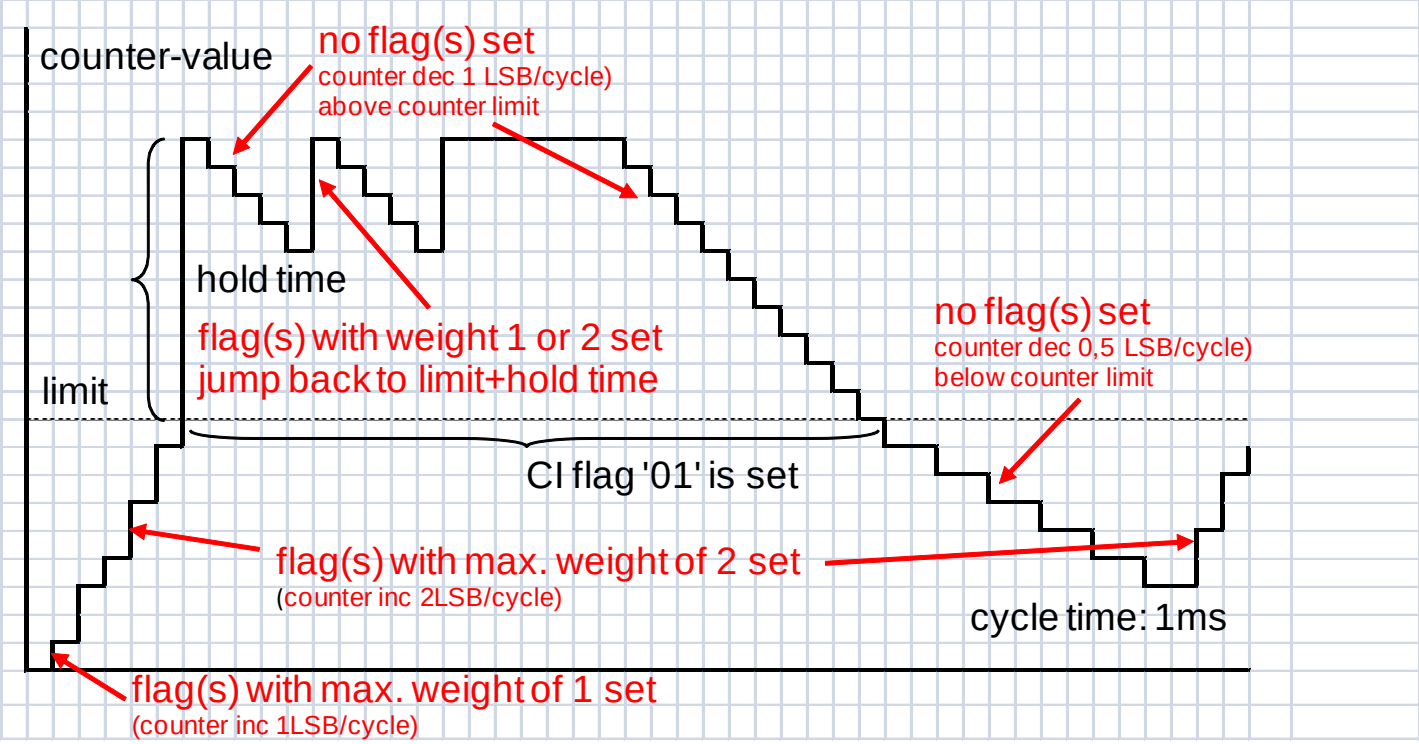
The limit of each error counter is defined by ec0_yrs_lf_config (page3 / ID 0x1), ec1_quad_hf (page3 / ID 0x2), ec2_acc_lf_config (page3 / ID 0x3). To ensure the maximum fault tolerant time span of 18ms, all error counter limits are configured to 16LSB as default value (smallest increment = 1LSB/cycle / cycle time of 1ms +/-10%). If those values are increased by the customer (>16LSB), the fault tolerant time span of 18ms could not be guaranteed anymore. If the limit values are reduced by the customer (<16LSB), the SMI720 get a lower robustness, because the limit of the error counter in case of a single failure event will be reached earlier.

Deviation of SMI720 A-samples: To ensure a fault tolerant time span of 18ms each error counter has to be configured to a value of 8LSB by the ECU when BITE test is finished.

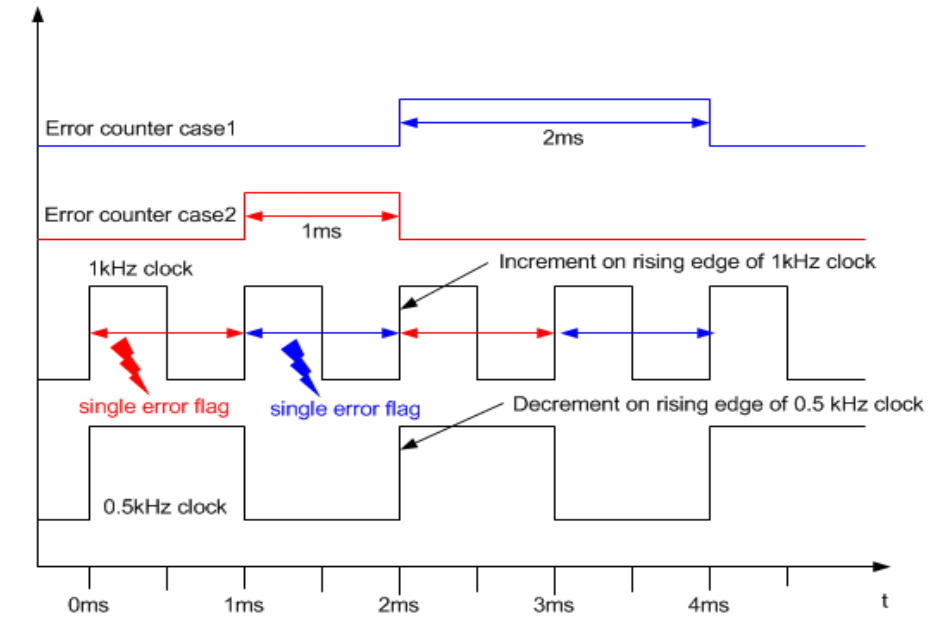
Behavior of SMI720 A-samples (with TIG720AA):



Behaviour of SMI720 C-samples (with TIG720BA):

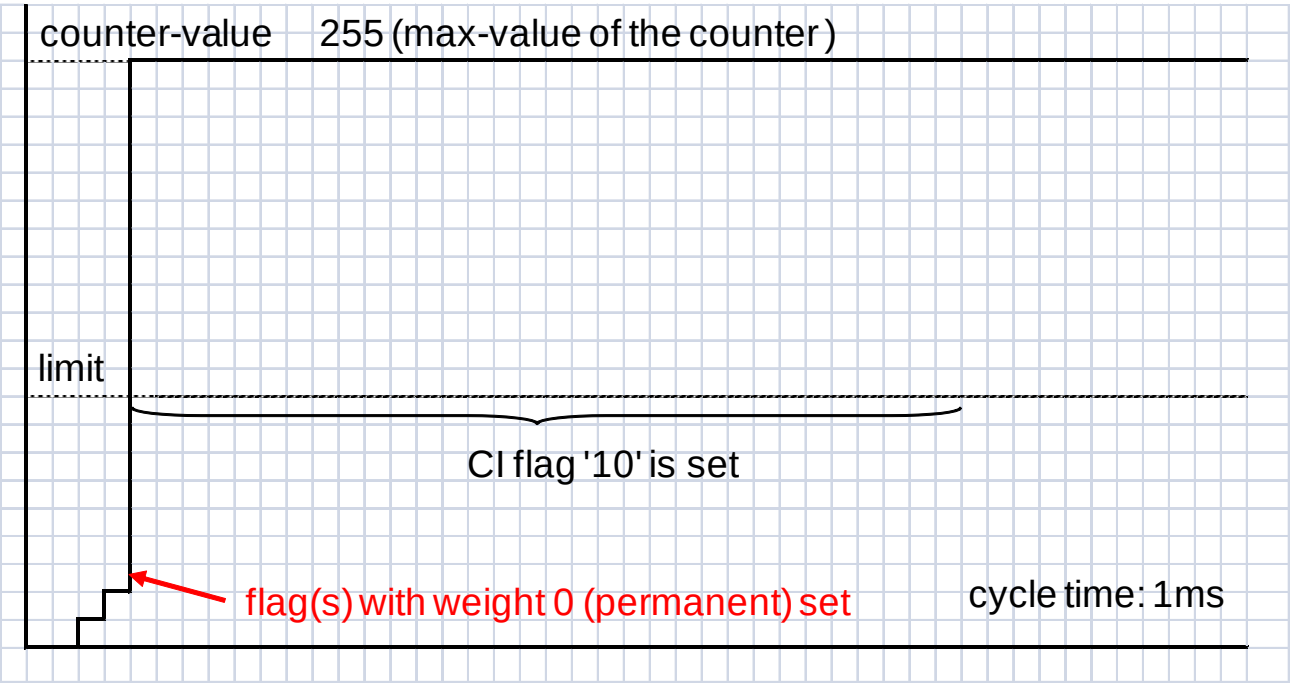


Due to different clocks for incrementing and decrementing the error counter, the error counter could stay in case of a single, temporary error flag occurance for 1ms or for 2ms at a constant value unequal to zero. Incrementing the error counter has always priority compared to decrementing the error counter. The error counter behaviour is shown here:



50% chance for case1 for error counter behaviour 1LSB of error counter is set for 2ms if only one error flag occurs.

50% chance for case2 for error counter behaviour 1LSB of error counter is set for 1ms if only one error flag occurs.



Req_1376 The failure counters are: S

ec0_yrs_lf

ec1_quad_hf

ec2_acc_lf

When an error counter has reached its limit and signals an error on the interface, only the affected signals are marked invalid. The system counter works on all signals.

The assignment of the flags to the failure counters is done by design.

The counter status of all failure counters is to be readable via the interfaces (also CC32in and openSPI32).

The 1bit-CI-status is hard-connected to the DSP. Whenever sensor data of a specific channel is requested via the bus by any interface, the 16bit-data is delivered together with the corresponding 1bit-CI-status. This way, it is assured that the CI status always corresponds to the data.

7.4.2.3 Overview of the SCON Error Flag Handling

Req_1378 For the links between failure flags and error counters please refer to chapter 7.4.4 "Overview of flag effects".

7.4.2.4 Error Memory

Req_1381 TIG720 will not provide an error memory for storage of diagnostic information in the case of an ECU failure. Diagnostic information of failure flag or the internal state of the SMI720 has to be provided by the ECU (e.g. debug bytes).

7.4.3 List of all Monitors

Req_1389 In sum, approximately 90 internal monitors are running continuously, with corresponding failure flags.

The frequencies of the individual monitors are given in the tables below.

Req_1390 The flags are being handled (and partly generated) by the SCON. The following table lists all planned monitor flags including a description of their purpose, their source and their handling (HW/SW partitioning). A second table lists the effects on failure counters, the CI (Channel Information) flags and the 16bit summing cluster.

Req_1391 If flags are handled by the SCON-SW, the following evaluation types are being used:

1. Range Check: f_min <= f(t) <= f_max
2. Tolerance Check: |f(t) - f_ref| < f_tol
3. Symmetric Range Check: |f(t)| < f_max
4. Difference Check: |f_1(t) -f_2(t)| < f_diff
5. Temperature dependent Tolerance Check(TDTC):
   tol - |f(t)-f_ref_comp| with f_ref_comp = fref + T_1 * tc
   f_ref_comp is the reference value at temperature T1

If the incoming signal exceeds the limit, an error flag will be generated by SCON.

6. DSP online BIST

7.4.3.1 Angular Rate Drive Monitors

7.4.3.1.1 yrs_agc_irregular

Req_1394 S

Flag Name:	yrs_agc_irregular
Goal:	Oscillation amplitude of CMG out of limits (goal: 8µm, goal tolerance: ~1%), measured at input of PI
Test:	Test: The AGC_irregular-Flag is set to zero in case - the AGC is enabled (done by the startup process) and CMG has reached its target amplitude (see below) AND - the PLL is locked (yrs_pll_unlock = 0). Otherwise, the flag is set to 1. If the nominal amplitude is reached will be tested as below: |HW-av.64(DRV_ERR)| < DRV_AGC_LIM DRV_ERR = difference of current amplitude DRV_AMP and the nominal amplitude DRV_AMPL_REF
Programmable by Customer:	-
Frequency:	Average of 64 ~25kHz-oscillations -> ~400Hz
Source of flag:	ARS Frontend HW

7.4.3.1.2 yrs_drv_pi_tol

Req_1396 S

Flag Name:	yrs_drv_pi_tol
Goal:	Drive force which is necessary to obtain the goal oscillation amplitude of the CMG is out of limits, measured at output of PI.

Test:	Test: Temperature dependent Tolerance Check (TDTC) of register YRS_DRV_PI_TOL_REG (11...0) (HW-averaged 16x) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	ARS Frontend via SCON

7.4.3.1.3 yrs_drv_bp_lim

Req_1398 S

Flag Name:	yrs_drv_bp_lim
Goal:	Overload flag of the band pass limiter in the drive path.
Test:	Flag is set by HW if Min/Max of filter range is reached or exceeded.
Programmable by Customer:	-
Frequency:	~400kHz
Source of flag:	ARS Frontend HW

7.4.3.1.4 yrs_cpar1_cal_drive_int

Req_1400 S

Flag Name:	yrs_cpar1_cal_drive_int
Goal:	Compare Offset controller value (drive frontend) to new part value.
Test:	Test: Tolerance Check of register YRS_CPAR1_CAL_DRIVE_INT (6:0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	ARS Frontend via SCON

Monitor has to be modified in TIG720BA because of a new signal width of CPAR1_CAL_DRIVE_INT.

7.4.3.1.5 yrs_drv_cu_gain

Req_1402 S

Flag Name:	yrs_drv_cu_gain
Goal:	Test (only) the gain of drive CU and ADC stage by applying an additional pulse with 1/32 of the sensor frequency (~780Hz) prior to the CU and demodulation/average after ADC.
Test:	Test: Tolerance Check of register YRS_DRV_CU_GAIN_REG (14…0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~25kHz/32 = ~0.8kHz
Source of flag:	ARS Frontend via SCON

7.4.3.1.6 yrs_pll_lim

Req_1404

Flag Name:	yrs_pll_lim
Goal:	Detect PLL Frequency is at regulator limit
Test:	Flag is set by HW if PLL regulator value (limited to 9bit = 0…511) is reached
Programmable by Customer:	-
Frequency:	~ 400kHz
Source of flag:	ARS Frontend HW

S

7.4.3.1.7 yrs_pll_tol

Req_1406

Flag Name:	yrs_pll_tol
Goal:	Compare PLL regulator value to new part value
Test:	Test: Tolerance Check of register (phase) YRS_PLL_TOL_REG (12…0) (HW-averaged 16x) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	ARS Frontend via SCON

S

7.4.3.1.8 yrs_pll_unlock

Req_1408

Flag Name:	yrs_pll_unlock
Goal:	PLL is unlocked, which means: Phase error (output of phase detector is above limit; goal: ~1°)
Test:	Test: Phase error: |HW-Average64(PLL_PD_ERR)| < PLL_PFD_LockLim (Average of 64 ~25kHz-Oscillations -> ~400Hz) PLL_PD_ERR = actual phase - PLL_PHASE_REF DCO output: Limiter Flags (Hi/Lo) (~25kHz)
Programmable by Customer:	-
Frequency:	400kHz if oscillator control value reaches upper or lower limit; for phase errors: Average of 64 oscillations with 400kHz/16 = ~25kHz -> ~400Hz
Source of flag:	ARS Frontend HW

S

7.4.3.1.9 yrs_drv_adc

Req_1410

Flag Name:	yrs_drv_adc

S

Goal:	Overload flag of the ADC in the drive path.
Test:	Drive-ADC overload w/ HW-precounter; The A/D converter samples every drive/rate period with 16 samples, i.e. at 16 x 25kHz = 400kHz. The precounter is configured such that an permanent overload will trigger the flag after 16 sensor cycles.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	ARS Frontend HW

7.4.3.2 Angular Rate Detection Monitors

7.4.3.2.1 yrs_quad_I_tol

Req_1413

Flag Name:	yrs_quad_I_tol
Goal:	Compare quadrature regulator to new part value.
Test:	Test: Tolerance Check of register QUAD_I_VALUE(15…0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	DSP via SCON

S

7.4.3.2.2 yrs_quad_HF_tol

Req_1415

Flag Name:	yrs_quad_HF_tol
Goal:	Deviation from required quadrature (0°/s) at input of controller. Value is sensitive to external vibration.
Test:	Test: Symmetric Range Check of register QUAD_HF_LIMITED(15…0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	DSP via SCON

S

7.4.3.2.3 yrs_rate_pt2_lim

Req_1417

Flag Name:	yrs_rate_pt2_lim
Goal:	Overload flag of the Controller in the Rate path
Test:	After the additional gain at the controller output the clipping will be detected (flag will be set by HW).
Programmable by Customer:	-
Frequency:	~400kHz
Source of flag:	ARS Frontend HW

S

7.4.3.2.4 yrs_rate_quantizer

Req_1419

Flag Name:	yrs_rate_quantizer
Goal:	Overload flag of the quantizer (the quantizer reduces the resolution of the PT2 output to a 4bit signal).
Test:	Quantizer overload w/ HW-precounter; The Quantizer samples every drive/rate period with 16 samples, i.e. at 16 x 25kHz = 400kHz. The precounter is configured such that an permanent overload will trigger the flag after 16 sensor cycles.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	ARS Frontend HW

S

7.4.3.2.5 yrs_cpar1_cal_rate

Req_1421

Flag Name:	yrs_cpar1_cal_rate
Goal:	Compare Offset controller value (rate frontend) to new part value.
Test:	Test: Tolerance Check of register YRS_CPAR1_CAL_RATE (6:0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~400kHz/256 = ~1.6kHz
Source of flag:	ARS Frontend via SCON

S

Monitor has to be modified in TIG720BA because of a new signal width of CPAR1_CAL_RATE.

7.4.3.2.6 yrs_rate_adc

Req_1423

Flag Name:	yrs_rate_adc
Goal:	Overload flag of the rate ADC
Test:	Rate-ADC overload w/ HW-precounter; The A/D converter samples every drive/rate period with 16 samples, i.e. at 16 x 25kHz = 400kHz. The precounter is configured such that an permanent overload will trigger the flag after 16 sensor cycles.
Programmable by Customer:	-
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	ARS Frontend HW

S

7.4.3.2.7 yrs_rate_V_TN

Req_1425

Flag Name:	yrs_rate_V_TN
Goal:	UDF-Voltage at TN-electrode
Test:	Test: Tolerance Check of register SCON_ADC_UDF_DET(11..0) (1/16-buffered) (~4,57mV/LSB)

S

	Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~0.5kHz
Source of flag:	MISC via SCON-ADC and SCON

7.4.3.2.8 yrs_rate_V_com

Req_1427

Flag Name:	yrs_rate_V_com
Goal:	Common Mode voltage monitor for rate CU (Cn-Cp-check; goal: check vs ~1% deviation)
Test:	Test: Tolerance Check of register SCON_ADC_DET_CNCP(11..0) (~0,43 mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~0,1kHz (sampled at 10KHz , filtered 1st order at cut off frequency of 100Hz to reject possible vibration issues at 1KHz)
Source of flag:	MISC via SCON-ADC and SCON

S

7.4.3.2.9 yrs_rate_V_fb

Req_1429

Flag Name:	yrs_rate_V_fb
Goal:	Sensor feedback force monitor (check vs new-part values)
Test:	Test: Tolerance Check of register SCON_ADC_FB_MUX(11..0) (~0,71mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~0,5kHz
Source of flag:	MISC via SCON-ADC and SCON

S

7.4.3.2.10 yrs_rate_V_CM

Req_1431

Flag Name:	yrs_rate_V_CM
Goal:	UCM-voltage (measures pulse on CM of YR-FE)
Test:	Test: Tolerance Check of register SCON_ADC_UCM_YAW(11..0) (~0,71mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	-
Frequency:	~100Hz due to low-pass filtering
Source of flag:	MISC via SCON-ADC and SCON

S

7.4.3.2.11 pe_flag_rate_1k_err

Req_1435

Flag Name:	pe_flag_rate_1k_err
Goal:	Parity prediction of YR LF decimation filter
Test:	see goal
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	ARS Frontend HW

S

7.4.3.2.12 pe_flag_quad_2k_err

Req_1439

Flag Name:	pe_flag_quad_2k_err
Goal:	Parity prediction of Quad LF decimation filter
Test:	see goal
Programmable by Customer:	-
Frequency:	~2kHz
Source of flag:	ARS Frontend HW

S

7.4.3.2.13 pe_flag_cic4_err

Req_1441

Flag Name:	pe_flag_cic4_err
Goal:	Parity prediction of CIC (Cascaded Integrator Comb) filter (which is a form of a FIR decimation filter) in the Rate Detection path
Test:	see goal
Programmable by Customer:	-
Frequency:	~4kHz
Source of flag:	ARS Frontend HW

S

7.4.3.3 Acceleration Frontend Monitors

7.4.3.3.1 acc1_clk_cnt

Req_1444

Flag Name:	acc1_clk_cnt
Goal:	Check ACC clock frequency 130kHz
Test:	HW counts 25MHz-pulses within n ACC-130kHz-pulses. Resulting number is checked by HW vs goal (fixed Value and fixed tolerance)
Programmable by Customer:	-
Frequency:	~130kHz
Source of flag:	ACC Frontend

S

7.4.3.3.2 acc_clk_ovlp

Req_1448 S

Flag Name:	acc_clk_ovlp
Goal:	The ACC frontend works with Switched capacitor technique. The frontend implementation comprises of two 180°-Phase shifted clocks, PHI1 and PHI2. To make sure error free transfer of the charge from one capacitor of the other, PHI1 and PHI2 clocks must not be set high simultaneously.
Test:	This is checked via AND-Gate (HW), which set a high signal when both the clocks are high i.e. overlapping. A R/S FF (flag acc_clk_ovlp) is set to indicate an invalid state of the clock fab.
Programmable by Customer:	-
Frequency:	on occurrence (~130kHz)
Source of flag:	ACC Frontend

7.4.3.3.3 acc1_V_cm

Req_1450 S

Flag Name:	acc1_V_cm
Goal:	Check FE voltage Ucm of ACC1 in order to check bonds
Test:	Test: Tolerance Check of register SCON_ADC_UCM_ACC1(11..0) (~0,43mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~0,5kHz
Source of flag:	via SCON-ADC and SCON

7.4.3.3.4 acc1_ds_lim

Req_1454 S

Flag Name:	acc1_ds_lim
Goal:	Overload detection of ACC1 ADC
Test:	In order to detect an overload state of the sigma-delta converter, a consecutive train of digital ones or zeroes is observed and accumulated. If an overload condition is detected, the flag acc1_ds_lim is raised.
Programmable by Customer:	-
Frequency:	~130kHz/16
Source of flag:	ACC Frontend

7.4.3.3.5 acc1_overload_det

Req_1458 S

Flag Name:	acc1_overload_det
Goal:	Disturbance detection of ACC1 signal
Test:	In order to detect disturbances in the ACC1 signal ("high energy peaks"), a weighted counter is used to sum up consecutive bit trains of same polarity. A second counter sums up the upper 8 bit values of the first

	counter and compares it every millisecond with a limit, before resetting the counter to zero. If the limit is exceeded, the flag will be set. This flag is not a failure flag, but an vibration indication flag.
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	ACC Frontend

7.4.3.3.6 acc1_pe_flag_1k_err

Req_1462

Flag Name:	acc1_pe_flag_1k_err
Goal:	Parity prediction of ACC1 LF decimation filter
Test:	see goal
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	ACC Frontend

S

7.4.3.4 Frequency Check (optional)

7.4.3.4.1 external CMG_f_check

Req_1471

External Test:	external CMG_f_check
Goal:	CMG frequency check vs. external time reference (ECU)
Test:	Two consecutive ASIC counter values are compared with an external time reference. Evaluation is done in ECU. Remark: Check is technically possible, but not required.
Programmable by Customer:	-

7.4.3.5 Voltage Levels and Regulators

7.4.3.5.1 VDD3_high

Req_1478

Flag Name:	VDD3_high
Goal:	Check upper voltage limit at VDD3-Pin
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	Analog Regulator

S

7.4.3.5.2 VDD3_low

Req_1480

Flag Name:	VDD3_low
Goal:	Check lower voltage limit at VDD3-Pin

S

Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	Analog Regulator

7.4.3.5.3 V_CTM_high

Req_1482

Flag Name:	V_CTM_high
Goal:	Check upper voltage limit behind regulator for T-Sensors
Programmable by Customer:	-
Frequency:	continously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

S

7.4.3.5.4 V_CTM_low

Req_1484

Flag Name:	V_CTM_low
Goal:	Check lower voltage limit behind regulator for T-Sensors
Programmable by Customer:	-
Frequency:	continously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

S

7.4.3.5.5 V_CP_high

Req_1486

Flag Name:	V_CP_high
Goal:	Check upper voltage limit behind regulator for charge pump
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

S

7.4.3.5.6 V_CP_low

Req_1488

Flag Name:	V_CP_low
Goal:	Check if charge pump voltage is >16V.
Test:	Inverse bit to "cp_ok" = charge pump ok
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

S

7.4.3.5.7 V_YRS_high

Req_1490 S

Flag Name:	V_YRS_high
Goal:	Check upper voltage limit behind regulator for YR FE
Programmable by Customer:	-
Frequency:	Continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.5.8 V_YRS_low

Req_1492 S

Flag Name:	V_YRS_low
Goal:	Check lower voltage limit behind regulator for YR FE
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.5.9 V_ACC_high

Req_1494 S

Flag Name:	V_ACC_high
Goal:	Check upper voltage limit behind regulator for ACC FE
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.5.10 V_ACC_low

Req_1496 S

Flag Name:	V_ACC_low
Goal:	Check lower voltage limit behind regulator for ACC FE
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.5.11 V_DIG_high

Req_1498 S

Flag Name:	V_DIG_high
Goal:	Check upper voltage limit behind regulator for digital core
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.5.12 V_DIG_low = POR (no flag)

Req_1500 S

Flag Name:	V_DIG_low = POR (no flag)
Goal:	Check lower voltage limit behind regulator for digital core Reset Flag is set after reset
Programmable by Customer:	-
Frequency:	none (on occurrence)
Source of flag:	analog -> POR

7.4.3.6 Temperature Checks

7.4.3.6.1 ctm_range

Req_1503 S

Flag Name:	ctm_range
Goal:	Temperature is checked vs absolute operation condition limits
Test:	Test: Range Check of register TEMP_SENSOR_1_VALUE (15…0) (~200LSB/K) Flag is set if lower or upper limit is reached or exceeded (details see {REF:F07_9495}).
Programmable by Customer:	-
Frequency:	~60Hz, signal bandwidth 4LSB/sec
Source of flag:	SCON-ADC via SCON

7.4.3.6.2 ctm_diff

Req_1505 S

Flag Name:	ctm_diff
Goal:	Plausibility check of the temperature by checking the difference to a 2nd temperature sensor
Test:	Test: Difference Check of registers TEMP_SENSOR_1_VALUE (15…0), TEMP_SENSOR_2_VALUE (15…0) (~200K/LSB) Flag is set if the amount of the temperature difference equals or exceeds the tolerance.
Programmable by Customer:	-
Frequency:	~60Hz, signal bandwidth 4LSB/sec
Source of flag:	SCON-ADC via SCON

7.4.3.7 DSP Flags

7.4.3.7.1 dsp_adjust_data_err

Req_1508 S

Flag Name:	dsp_adjust_data_err
Goal:	Check integrity of DSP gain adjust data

Test:	Main Adjust Data not corresponding to Checksum Value
Programmable by Customer:	-
Frequency:	~800Hz
Source of flag:	DSP

7.4.3.7.2 dsp_pe_flag_err

Req_1512

Flag Name:	dsp_pe_flag_err
Goal:	Check validity of internal DSP registers
Test:	HW: sDSP parity check of internal Registers
Programmable by Customer:	-
Frequency:	~20kHz
Source of flag:	DSP

S

7.4.3.7.3 dsp_pe_sign_err

Req_1514

Flag Name:	dsp_pe_sign_err
Goal:	Monitoring the program flow
Test:	HW: sDSP signature check
Programmable by Customer:	-
Frequency:	~800Hz
Source of flag:	DSP

S

7.4.3.7.4 dsp_pe_irq_err

Req_1516

Flag Name:	dsp_pe_irq_err
Goal:	Monitoring of the interrupt module
Test:	HW: sDSP irq-module check
Programmable by Customer:	-
Frequency:	~800Hz
Source of flag:	DSP

S

7.4.3.7.5 dsp_ram_ifa13_err

Req_1518

Flag Name:	dsp_ram_ifa13_err
Goal:	Check DSP RAM
Test:	ram_ifa13_err: HW-RAMCHECK of the RAM cells

S

Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

7.4.3.7.6 dsp_ram_ifa13_su_err

Req_2249

Flag Name:	dsp_ram_ifa13_su_err
Goal:	Check DSP RAM
Test:	ram_ifa13_err: HW-RAMCHECK of the RAM cells startup error flag of extra hardware to test the content of RAM. Only active when ifa13 test fails.
Programmable by Customer:	-
Frequency:	startup test
Source of flag:	DSP

S

7.4.3.7.7 dsp_ram_soaf_err

Req_1520

Flag Name:	dsp_ram_soaf_err
Goal:	Check DSP address decoder
Test:	ram_soaf_err: HW-RAMCHECK of the address decoder
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

S

7.4.3.7.8 dsp_ram_soaf_su_err

Req_2251

Flag Name:	dsp_ram_soaf_err
Goal:	Check DSP address decoder
Test:	ram_soaf_err: HW-RAMCHECK of the address decoder startup error flag of extra hardware to test the content of RAM. Only active when soaf test fails.
Programmable by Customer:	-
Frequency:	startup test
Source of flag:	DSP

S

7.4.3.7.9 dsp_ram_dpath_err

Req_1522

Flag Name:	dsp_ram_dpath_err
Goal:	Check internal bus structures in the data path of the RAM.

S

Test:	This test performs simple write and read operations on a single, fixed address.
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

7.4.3.7.10 dsp_ram_dpath_su_err

Req_2253 S

Flag Name:	dsp_ram_dpath_su_err
Goal:	Check internal bus structures in the data path of the RAM.
Test:	Startup test: This test performs simple write and read operations on a single, fixed address.
Programmable by Customer:	-
Frequency:	startup test
Source of flag:	DSP

7.4.3.7.11 dsp_pe_ram_err

Req_1524 S

Flag Name:	dsp_pe_ram_err
Goal:	Check parity of DSP RAM
Test:	HW: sDSP ram parity_check (parity monitoring of the RAM cells)
Programmable by Customer:	-
Frequency:	~20kHz
Source of flag:	DSP

7.4.3.7.12 dsp_pe_sqrt_err

Req_1526 S

Flag Name:	dsp_pe_sqrt_err
Goal:	Check parity in DSP SQRT Module
Test:	HW: sDSP parity check of SQRT Module
Programmable by Customer:	-
Frequency:	~800Hz
Source of flag:	DSP

7.4.3.7.13 dsp_neg_flag_sqrt

Req_1528 S

Flag Name:	dsp_neg_flag_sqrt
Goal:	Negative Input at SQRT Module
Test:	HW: sDSP checks if input of SQRT Module is negative

Programmable by Customer:	-
Frequency:	~800Hz
Source of flag:	DSP

7.4.3.7.14 dsp_rom_crc_err

Req_1530

Flag Name:	dsp_rom_crc_err
Goal:	DSP ROM check
Test:	rom_crc_error: ROMCHECK To check the ROM a special hardware is implemented into the design. The ROM is checked by a CRC algorithm. The hardware contains a shift register and a calculation of a CRC polynomial. The hardware can be triggered by a special assembler command. Each time the command is set one value is read out of the ROM and stored into a hardware register. Because of the DSP independent hardware the DSP can run while the hardware will calculate the polynomial. In this way the usage of assembler code and the usage of cycles to calculate the CRC is as few as possible.
Programmable by Customer:	-
Frequency:	~3.2Hz
Source of flag:	DSP

S

7.4.3.7.15 dsp_ram_toggle_missing

Req_1532

Flag Name:	dsp_ram_toggle_missing
Goal:	DSP RAM toggle is missing
Test:	HW-SCON checks wether DSP RAM Toggle bit is missing
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

S

7.4.3.7.16 dsp_rom_toggle_missing

Req_1534

Flag Name:	dsp_rom_toggle_missing
Goal:	DSP ROM toggle is missing
Test:	HW-SCON checks whether DSP ROM Toggle bit is missing
Programmable by Customer:	-
Frequency:	~3.2Hz
Source of flag:	DSP

S

7.4.3.7.17 dsp_pe_dsp_status_0_err

Req_1536

Flag Name:	dsp_pe_dsp_status_0_err
Goal:	DSP parity check of status register 0
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

S

7.4.3.7.18 dsp_pe_dsp_status_1_err

Req_1538

Flag Name:	dsp_pe_dsp_status_1_err
Goal:	DSP parity check of status register 1
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

S

7.4.3.7.19 dsp_pe_dsp_status_2_err

Req_1540

Flag Name:	dsp_pe_dsp_status_2_err
Goal:	DSP parity check of status register 2
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

S

7.4.3.7.20 dsp_pe_quad_i_sqrt_udf_err

Req_1542

Flag Name:	dsp_pe_quad_i_sqrt_udf_err
Goal:	DSP parity check of DSP-out-registers QUAD_I and SQRT_UDF
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

S

7.4.3.7.21 dsp_gp_status

Req_1544

Flag Name:	dsp_gp_status

S

Goal:	HW-Limiter flag of all primary-Input Limiters of the DSP (YR, Quad and ACC)
Test:	see goal
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.7.22 dsp_sqrt_lim_flag

Req_1546

Flag Name:	dsp_sqrt_lim_flag
Goal:	Limiter of Output Value of SQRT calculation
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

S

7.4.3.7.23 dspmem_debugaccess_on

Req_1548

Flag Name:	dspmem_debugaccess_on
Goal:	DSP info flag: DSP is in Debug Mode
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

S

7.4.3.7.24 dsp_online_test

Req_1550

Flag Name:	dsp_online_test
Goal:	Control the continuing signal processing in the DSP.
Test:	A Built In Self Test (BIST) is implemented in the DSP to control the continuing signal processing in the DSP, consisting in answering 16 control questions.
Programmable by Customer:	-
Frequency:	~32Hz
Source of flag:	DSP

S

7.4.3.7.25 dsp_acc_LF_adjust

Req_1554

Flag Name:	dsp_acc_LF_adjust

S

Goal:	ACC1: Combined Flag from Limiter of Offset and Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz but with a latency of the filter signal delay concerning errors arising in the signal path in front of the filter
Source of flag:	DSP

7.4.3.7.26 dsp_rate_LF_adjust

Req_1562

Flag Name:	dsp_rate_LF_adjust
Goal:	RATE: Combined Flag from Limiter of Offset and Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

S

7.4.3.7.27 dsp_quad_HF_adjust

Req_1564

Flag Name:	dsp_quad_adjust
Goal:	QUAD: Limiter Flag of Gain-Adjust-Block
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

S

7.4.3.7.28 dsp_ctm1_adjust

Req_1566

Flag Name:	dsp_ctm1_adjust
Goal:	Temperature 1: OR-Binding of Input-Limiter in HF and Input-Limiter of LF Chanel (2 Flags)
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

S

7.4.3.7.29 dsp_ctm2_adjust

Req_1568

Flag Name:	dsp_ctm2_adjust

S

Goal:	Temperature 2: OR-Binding of Input-Limiter in HF and Input-Limiter of LF Chanel (2 Flags)
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.7.30 dsp_acc1_LF_out

Req_1572

Flag Name:	dsp_acc1_LF_out
Goal:	ACC1: Flag from Limiter before Output-Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

S

7.4.3.7.31 dsp_rate_LF_out

Req_1580

Flag Name:	dsp_rate_LF_out
Goal:	RATE: Flag from Limiter before Output-Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

S

7.4.3.7.32 dsp_acc1_LF_in

Req_1584

Flag Name:	dsp_acc1_LF_in
Goal:	ACC1: Flag from Input Limiter in LF-Path
Test:	Check vs and clip the signal to asymmetrically adjustable limits (in order to prevent asymmetrical clipping). This limit should be the "bottleneck"; no subsequent limiters should be activated prior to this limiter.
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

S

7.4.3.7.33 dsp_quad_QI_lim

Req_1590 S

Flag Name:	dsp_quad_QI_lim
Goal:	QUAD: Limiter of I-Control
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~2kHz
Source of flag:	DSP

7.4.3.7.34 dsp_ram_decadd_err

Req_2018 S

Flag Name:	dsp_ram_decadd_err
Goal:	Error of DECADD test (init an online) Error signal of the DECADD test; 1 after reset; will switch to 0 after test in startup sequence is finished; during online phase will only switch to 1 if an error will be detected by the DECADD test; otherwise it will be 0 during online phase; if an error was detected and the signal is set to 1 it will be 1 until the complete DECADD test sequence is finished without detection of an error.
Test:	see „goal“
Programmable by Customer:	-
Frequency:	
Source of flag:	DSP

7.4.3.8 Bus Error Flags

7.4.3.8.1 misc_apb_slv

Req_1599 S

Flag Name:	misc_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within MISC module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	MISC

7.4.3.8.2 main_ctrl_apb_slv

Req_1601 S

Flag Name:	main_ctrl_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within Main Control module

	address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Main_Ctrl

7.4.3.8.3 dsp_apb_slv

Req_1603

Flag Name:	dsp_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within DSP address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

S

7.4.3.8.4 dsp_ram_apb_slv

Req_1605

Flag Name:	dsp_ram_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within DSP address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

S

7.4.3.8.5 dsp_rom_apb_slv

Req_1607

Flag Name:	dsp_rom_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within DSP address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

S

7.4.3.8.6 hw_scon_apb_slv

Req_1609

Flag Name:	hw_scon_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within SCON-HW module address range

S

Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	HW_SCON

7.4.3.8.7 conf_apb_slv

Req_1611

Flag Name:	conf_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within CONFIG module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Config_reg

S

7.4.3.8.8 frontend_apb_slv

Req_1615

Flag Name:	frontend_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within frontend address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Frontend

S

7.4.3.8.9 spi_apb_slv

Req_1619

Flag Name:	spi_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within SPI module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	SPI

S

7.4.3.8.10 uc_sub_apb_slv

Req_1625

Flag Name:	uc_sub_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within boot loader address range
Programmable by Customer:	-

S

Frequency:	for each bus transfer
Source of flag:	boot loader

7.4.3.8.11 ahb_hang_up

Req_1629 S

Flag Name:	ahb_hang_up
Goal:	Detect dead lock on AHB bus
Test:	Non-terminated Read/Write access on AHB bus
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

7.4.3.9 LBIST

7.4.3.9.1 lbist_err

Req_1632 S

Flag Name:	lbist_err
Goal:	LBIST/Scan during Power on
Test:	see LBIST description
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	Main_Ctrl

7.4.3.10 Pin Checks

7.4.3.10.1 pc_vssa

Req_1660 S

Flag Name:	pc_vssa
Goal:	Voltage difference between VSSA,VSSD and VSS_IO to each other. (due to bond ruptures).
Test:	HW-Check: Difference > 300mV
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.10.2 pc_vssd

Req_1662 S

Flag Name:	pc_vssd
Goal:	Voltage difference between VSSA,VSSD and VSS_IO to each other. (due to bond ruptures).

Test:	HW-Check: Difference > 300mV
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.10.3 pc_vss_IO

Req_2255

Flag Name:	pc_vss_IO
Goal:	Voltage difference between VSSA,VSSD and VSS_IO to each other. (due to bond ruptures).
Test:	HW-Check: Difference > 300mV
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

S

7.4.3.10.4 pc_shd

Req_1666

Flag Name:	pc_shd
Goal:	To check SHD,SUBSTR CMG bond connection, a small test current is injected into SHD. If SHD or SUBSTR bond is open, then a voltage rise at the injection point is recognized and the appropriate fault flag is set.
Test:	Injection current for CS1 and SHD pins: 1-3µA
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

S

7.4.3.10.5 pc_cs1

Req_1668

Flag Name:	pc_cs1
Goal:	To check CS1,CS2 bond connection, a small test current is injected into CS1. If CS1 or CS2 bond is open, then a voltage rise at the injection point is recognized and the appropriate fault flag is set.
Test:	Injection current for CS1 and SHD pins: 1-3µA
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

S

7.4.3.10.6 pc_cp

Req_1672 S

Flag Name:	pc_cp (masked, no influence on CI)
Goal:	Voltage ripple for detection connection rupture of outside blocking capacitor at CP The flag pc_cp is raised in case of a detected bond rupture. In case of applying an external AC-voltage with an amplitude above 100 mV (for example EMC disturbances) and a frequency above 100 KHz CP, the flag pc_cp may also be activated.
Test:	HW-Check: Ripple > 20mVpeak (high-pass filtered with ~100kHz)
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.11 Electromechanical Self Tests (BITEs)

7.4.3.11.1 yrs_rate_seq_bite

Req_1678 S

Flag Name:	yrs_rate_seq_bite
Goal:	Bite sequence "Rate" failed in rate test
Test:	Test: Symmetric Range Check of register RATE_BITE_POS_NEG (15…0). Flag is set as soon as limits are reached or exceeded. The register RATE_BITE_POS_NEG will be set by the SW itself by calculating the rate difference between "positive BITE excitation" and "negative BITE excitation": RATE_BITE_POS_NEG = RATE_HF_LIMITED (t = end of positive BITE) (15...0) - RATE_HF_LIMITED (t = end of negative BITE) (15...0)
Programmable by Customer:	-
Frequency:	on request
Source of flag:	SCON

7.4.3.11.2 yrs_quad_seq_bite

Req_1680 S

Flag Name:	yrs_quad_seq_bite
Goal:	Bite sequence "Rate" failed in quad test
Test:	Test: This flag evaluates the Quadrature signal during the yaw rate BITE sequence. The flag is set if one of the following three conditions (sub-flags) is set: yrs_quad_bite_pos_zero yrs_quad_bite_neg_zero

	yrs_quad_bite_pos_neg yrs_quad_bite_pos_zero is the result of a Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Zero_BITE_QUAD (15...0) = QUAD_HF_LIMITED (t = end of positive BITE) (15...0) - QUAD_HF_LIMITED (t = end of zero BITE) (15...0) yrs_quad_bite_neg_zero is the result of a Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Zero_BITE_QUAD (15...0) = QUAD_HF_LIMITED (t = end of negative BITE) (15...0) - QUAD_HF_LIMITED (t = end of zero BITE) (15...0) yrs_quad_bite_pos_neg is the result of a Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Zero_BITE_QUAD (15...0) = QUAD_HF_LIMITED (t = end of positive BITE) (15...0) - QUAD_HF_LIMITED (t = end of negative BITE) (15...0)
Programmable by Customer:	-
Frequency:	on request
Source of flag:	SCON

7.4.3.11.3 acc1_seq_bite

Req_1682

Flag Name:	acc1_seq_bite
Goal:	Bite sequence ACC1 failed
Test:	Test: Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Neg_BITE_ACC1 (15…0) The value Pos_Neg_BITE_ACC1 will be set by the SCON itself by calculating the difference between "positive BITE excitation" and "negative BITE excitation": Pos_Neg_BITE_ACC1 = ACC1_LF_LIMITED (t = end of positive BITE) (15...0) - ACC1_LF_LIMITED (t = end of negative BITE) (15...0)
Programmable by Customer:	-
Frequency:	on request
Source of flag:	SCON

S

7.4.3.12 Bussystem / Boot Loader Error

7.4.3.12.1 boot_invalid_crc

Req_1940 S

Flag Name:	boot_invalid_crc
Goal:	Initial check, CRC check of OTP: CRC error during initial check of Data OTP (CRC check at check command fails)
Test:	see goal
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	SCON

7.4.3.12.2 boot_invalid_command

Req_1946 S

Flag Name:	boot_invalid_command
Goal:	Initial check, Bootloader Check: unknown command type
Test:	see goal
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	SCON

7.4.3.12.3 boot_readback_mismatch

Req_1947 S

Flag Name:	boot_readback_mismatch
Goal:	Initial check, Bootloader Check: register / block command readback has returned different data
Test:	see goal
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	SCON

7.4.3.12.4 boot_unrecoverable_err

Req_1705 S

Flag Name:	boot_unrecoverable_err
Goal:	Bootloader Check: invalid state in bootloader state machine
Test:	see goal
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	SCON

7.4.3.12.5 boot_device_unlocked

Req_1952 S

Flag Name:	boot_device_unlocked
Goal:	Bootloader Check: OTP not locked, bootloader reaches STOP command or end of OTP
Test:	
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	SCON

7.4.3.12.6 boot_bus_err

Req_1953 S

Flag Name:	boot_bus_err
Goal:	Bootloader Check: Internal bus check, AHB /APB bus error occurred
Test:	
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	SCON

7.4.3.12.7 boot_nval_bus_err

Req_2257 S

Flag Name:	boot_bus_err
Goal:	Bus check when nval function is active: Internal bus check, nval function bus error occurred
Test:	
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	SCON

7.4.3.12.8 boot_pll_assist_bus_err

Req_2259 S

Flag Name:	boot_bus_err
Goal:	Bus check when pll_assist function is active: Internal bus check, pll_assist function bus error occurred
Test:	
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	SCON

7.4.3.12.9 boot_cyc_invalid_crc

Req_1954

Flag Name:	boot_cyc_invalid_crc
Goal:	
Test:	A cyclic check of 34 selected registers is implemented in TIG720. The 34 registers were selected for the cyclic check because corrupted data within those registers can result in a top event of the SMI720. Additionally, 9 registers can be added later to the cyclic register check within final test of the SMI720.
Programmable by Customer:	-
Frequency:	-
Source of flag:	SCON

S

7.4.4 Overview of Flag Effects

Req_1721

In the following table, the flags and their effects are summarized. The first 3 columns describe the effects on the failure counters, followed by information about direct influence on status, direct effect on status for channel or if a POR (Power-On Reset) of the sensor is triggered. There is no mechanism for disabling the running SPI interface. The SPI interface will only be released if initial CRC checks of data otp are successful.

In the 16 columns on the right-hand side, it is described on which bit of the 16bit-Summary-Cluster the flag is acting.

All single flags and the cluster flags are ASIC internally latched. During initialization some flags will be set regulary. Therefore a clear by read of all err_flag_bankx registers and cluster register has to be done when initialization sequence is finished to reset all single flag information to zero when run-mode is reached.

A-samples: Two more flags were listed but not functional/used within SMI720 A-samples. Those flags were not implemented in TIG720BA and therefore not listed in the flaglist anymore:

pc_vdd3_vdd1_8 => monitor not functional, diagnostic coverage by other implemented monitors

otp_vprog_limit_exceed => not used as monitor, only implemented in TIG720AA for production purpose

C-samples:

pc_CP => masked (CR028)

dsp_acc_lf_out => masked due to customer request (documented in customer OPL, no CR)

dsp_rate_lf_out => masked due to customer request (documented in customer OPL, no CR)

Req_1722

S

Flag Name	Weight on EC's (reset values)	Effect on Status for Channel: rate_channel: Effect on Error Counter (EC): EC_YRS_LF	Effect on Status for Channel: rate_channel: Effect on Error Counter (EC): EC_QUAD_HF	Effect on Status for Channel: acc_channel: Effect on Error Counter (EC): EC_ACC_LF	Direct influence on status	Direct effect on Status for channel	POR	16bit Cluster Flags: F16_RATE_DRIVE (15)	F16_RATE_DETECTION (14)	F16_ACC_DETECTION (13)	F16_MEMORY (12)	F16_DSP (11)	F16_OTP_System (10)	F16_DIGITAL (9)	F16_MECH_OVERLOAD_RATE (8)	F16_EMC_PSRR (7)	F16_SUPPLY (6)	F16_TEMP (5)	F16_PIN_OR_BOND_FAILURE (4)	F16_ST_FAILED (3)	F16_MECH_OVERLOAD_ACC (2)	F16_INIT (set until 3 INIT conditions fulfilled) (1)	F16_ST_OR_FOC_RUNNING (0)
YR Drive								15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
yrs_agc_irregular	01	1	1					1							1	1							
yrs_drv_pi_tol	01	1	1					1							1	1							
yrs_drv_bp_lim	01	1	1					1							1	1							
yrs_cpar1_cal_drive_int	01	1	1					1							1	1							
yrs_drv_cu_gain	01	1	1					1							1	1							
yrs_pll_lim	01	1	1					1							1	1							
yrs_pll_tol	01	1	1					1							1	1							
yrs_pll_unlock	01	1	1					1							1	1							
yrs_drv_adc	01	1	1					1							1	1							
YR Detection																							
yrs_quad_I_tol	01		1						1						1	1							
yrs_quad_HF_tol	01		1						1						1	1							
yrs_rate_pt2_lim	01	1	1						1						1	1							
yrs_rate_quantizer	01	1	1						1						1	1							
yrs_cpar1_cal_rate	01	1	1						1						1	1							
yrs_rate_adc	01	1	1						1						1	1							
yrs_rate_V_TN	01	1	1													1							
yrs_rate_V_com	01	1	1													1							
yrs_rate_V_fb	01	1	1													1							
yrs_rate_V_CM	01	1	1													1							
pe_flag_rate_1k_err	00	1							1					1									
pe_flag_quad_2k_err	00		1						1					1									
pe_flag_cic4_err	00	1	1						1					1									

Req_1723 S

Flag Name	Weight on EC's (reset values)	Effect on Status for Channel: rate_channel	Effect on Status for Channel: acc_channel	Effect on Error Counter (EC): EC_YRS_LF	Effect on Error Counter (EC): EC_QUAD_HF	Effect on Error Counter (EC): EC_ACC_LF	Direct influence on status	Direct effect on Status for channel	POR	16bit Cluster Flags: F16_RATE_DRIVE	F16_RATE_DETECTION	F16_ACC_DETECTION	F16_MEMORY	F16_DSP	F16_OTP_System	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMC_PSRR	F16_SUPPLY	F16_TEMP	F16_PIN_OR_BOND_FAILURE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC	F16_INIT (set until 3 INIT conditions fulfilled)	F16_ST_OR_FOC_RUNNING
ACC																									
acc_clk_cnt	00					1						1				1									
acc_clk_ovlp	00					1						1				1									
acc_V_cm	01					1						1						1							
acc_ds_lim	01					1						1											1		
acc_overload_det	01					1						1											1		
acc_pe_flag_1k_err	00					1						1				1									
Voltage Regulators																									
VDD3_high	01	1	1	1															1						
VDD3_low	01	1	1	1															1						
V_CTM_high	01	1	1	1															1	1					
V_CTM_low	01	1	1	1															1	1					
V_CP_high	01	1	1																1						
V_CP_low	01	1	1																1						
V_YRS_high	01	1	1								1								1						
V_YRS_low	01	1	1								1								1						
V_ACC_high	01					1						1							1						
V_ACC_low	01					1						1							1						
V_DIG_high	01	1	1	1															1						
V_DIG_low									1																
Temperature Check																									
ctm_range	01	1	1	1																1					
ctm_diff	01	1	1	1																1					

Req_1724 S

Flag Name	Weight on EC's (reset values)	Effect on Status for Channel: rate_channel	Effect on Status for Channel: acc_channel	Effect on Error Counter (EC): EC_YRS_LF	Effect on Error Counter (EC): EC_QUAD_HF	Effect on Error Counter (EC): EC_ACC_LF	Direct influence on status	Direct effect on Status for channel	POR	16bit Cluster Flags: F16_RATE_DRIVE	F16_RATE_DETECTION	F16_ACC_DETECTION	F16_MEMORY	F16_DSP	F16_OTP_System	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMC_PSRR	F16_SUPPLY	F16_TEMP	F16_PIN_OR_BOND_FAILURE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC	F16_INIT (set until 3 INIT conditions fulfilled)	F16_ST_OR_FOC_RUNNING
DSP incl. DSP-Mem																									
dsp_adjust_data_err	00			1	1	1								1											
dsp_pe_flag_err	00			1	1	1										1									
dsp_pe_sign_err	00			1	1	1										1									
dsp_pe_irq_err	00			1	1	1										1									
dsp_ram_ifa13_err	00			1	1	1							1	1											
dsp_ram_ifa13_su_err	00			1	1	1								1											
dsp_ram_soaf_err	00			1	1	1							1	1											
dsp_ram_soaf_su_err	00			1	1	1								1											
dsp_ram_dpath	00			1	1	1								1											
dsp_ram_dpath_su_err	00			1	1	1								1											
dsp_pe_ram_err	00			1	1	1								1											
dsp_pe_sqrt_err	00				1						1					1									
dsp_neg_flag_sqrt	00				1						1					1									
dsp_rom_crc_err	00			1	1	1							1	1											
dsp_ram_toggle_missing	00			1	1	1								1											
dsp_rom_toggle_missing	00			1	1	1								1											
dsp_pe_dsp_status_0_err	00			1	1	1										1									
dsp_pe_dsp_status_1_err	00			1	1	1										1									
dsp_pe_dsp_status_2_err	00			1	1	1										1									
dsp_pe_quad_i_sqrt_udf_err	00				1						1					1									
dsp_gp_status	00			1	1	1										1									
dsp_quad_sqrt_lim	00				1						1					1									
dspmem_debugaccess_on	00			1	1	1										1									
dsp_online_test	00			1	1	1										1									
dsp_acc_LF_adjust	00					1						1				1									
dsp_rate_LF_adjust	00			1							1					1									
dsp_quad_HF_adjust	00				1						1					1									
dsp_ctm1_adjust	00			1	1	1										1				1					
dsp_ctm2_adjust	00			1	1	1										1				1					
dsp_acc_LF_out	11					1						1											1		
dsp_rate_LF_out	11			1							1						1								
dsp_acc_LF_in	01					1						1											1		
dsp_quad_QI_lim	01				1						1						1								
dsp_ram_decadd_err	00			1	1	1								1											

Req_1725 S

Flag Name	Weight on EC's (reset values)	Effect on Status for Channel: rate_channel	Effect on Status for Channel: acc_channel	Effect on Error Counter (EC): EC_YRS_LF	Effect on Error Counter (EC): EC_QUAD_HF	Effect on Error Counter (EC): EC_ACC_LF	Direct influence on status	Direct effect on Status for channel	POR	16bit Cluster Flags: F16_RATE_DRIVE	F16_RATE_DETECTION	F16_ACC_DETECTION	F16_MEMORY	F16_DSP	F16_OTP_System	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMC_PSRR	F16_SUPPLY	F16_TEMP	F16_PIN_OR_BOND_FAILURE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC	F16_INIT (set until 3 INIT conditions fulfilled)	F16_ST_OR_FOC_RUNNING
Bus																									
misc_apb_slv	00	1	1	1												1									
main_ctrl_apb_slv	00	1	1	1												1									
dsp_apb_slv	00	1	1	1												1									
dsp_ram_apb_slv	00	1	1	1												1									
dsp_rom_apb_slv	00	1	1	1												1									
hw_scon_apb_slv	00	1	1	1												1									
conf_apb_slv	00	1	1	1												1									
frontend_apb_slv	00	1	1	1												1									
spi_apb_slv	00	1	1	1												1									
uc_sub_apb_slv	00	1	1	1												1									
ahb_hang_up	00	1	1	1												1									
Digital Test																									
lbist_err	00	1	1	1												1						1			

Req_1726 S

Flag Name	Weight on EC's (reset values)	Effect on Status for Channel: rate_channel	Effect on Status for Channel: acc_channel	Effect on Error Counter (EC): EC_YRS_LF	Effect on Error Counter (EC): EC_QUAD_HF	Effect on Error Counter (EC): EC_ACC_LF	Direct influence on status	Direct effect on Status for channel	POR	16bit Cluster Flags: F16_RATE_DRIVE	F16_RATE_DETECTION	F16_ACC_DETECTION	F16_MEMORY	F16_DSP	F16_OTP_System	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMC_PSRR	F16_SUPPLY	F16_TEMP	F16_PIN_OR_BOND_FAILURE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC	F16_INIT (set until 3 INIT conditions fulfilled)	F16_ST_OR_FOC_RUNNING
PinChecks																									
pc_vssa	01	1	1	1														1			1				
pc_vssd	01	1	1	1														1			1				
pc_vss_IO	01	1	1	1														1			1				
pc_shd	01	1	1								1							1			1				
pc_cs1	01			1								1						1			1				
pc_cp	11	1	1															1			1				
BITEs																									
yrs_rate_seq_bite	00						10b	RATE & QUAD			1											1			
yrs_quad_seq_bite	00						10b	RATE & QUAD			1											1			
acc_seq_bite	00						10b	ACC				1										1			
yrs_bite_active	00						11b	RATE & QUAD																	1
acc_bite_active	00						11b	ACC																	1
µC-Errors (OTP-System)																									
boot_invalid_crc	00	1	1	1									1												
boot_invalid_command	00	1	1	1											1										
boot_readback_mismatch	00	1	1	1											1										
boot_unrecoverable_err	00	1	1	1											1										
boot_device_unlocked	00	1	1	1											1										
boot_cyc_bus_err	00	1	1	1											1										
boot_bus_err	00	1	1	1											1										
boot_nval_bus_err	00	1	1	1											1										
boot_pll_assist_bus_err	00	1	1	1											1										
boot_cyc_invalid_crc	00	1	1	1									1		1										
Offset-Controller																									
dsp_foc_rate_active	00						11b	RATE																	1
dsp_foc_acc_active	00						11b	ACC																	1
dsp_soc_rate_inactive	00						01b	RATE			1														
dsp_soc_acc_inactive	00						01b	ACC				1													
Initialization																									
init_rdy							11b	RATE & QUAD & ACC																1	
reset																									

7.4.5 Safety Control of Frequency

Req_1728 The main frequency of the sensor (incl. ARS, ACC, Digital Core incl. DSP) is defined by the PLL. The PLL-Frequency is proportional (*1024) to the CMG resonance frequency of the drive loop. S

As soon as the PLL unlocks (phase 3) because of an phase error, the flag yrs_pll_unlock is set.

An external check of the frequency can be done by evaluating the internal counter and comparing it with an external time reference. This is called external_CMG_f_check. This check is not mandatory.

7.4.6 Safety Control of Temperature

Req_1735 Limits for the temperature range monitoring will be defined for c-samples because of design changes in TIG720BA. S

7.4.7 Safety Control of Memory Elements

Req_1749 In addition to the DSP monitoring (see flags "dsp_...") and the Bus monitoring (see flags "apb_..."), the whole digital signal path is covered by a parity:

- there is a Parity Prediction for all decimation filters within the fast digital circuit.
- within DSP all data is covered with parity.
- during transport via the internal Bus, the sensor signals are also covered with a parity.

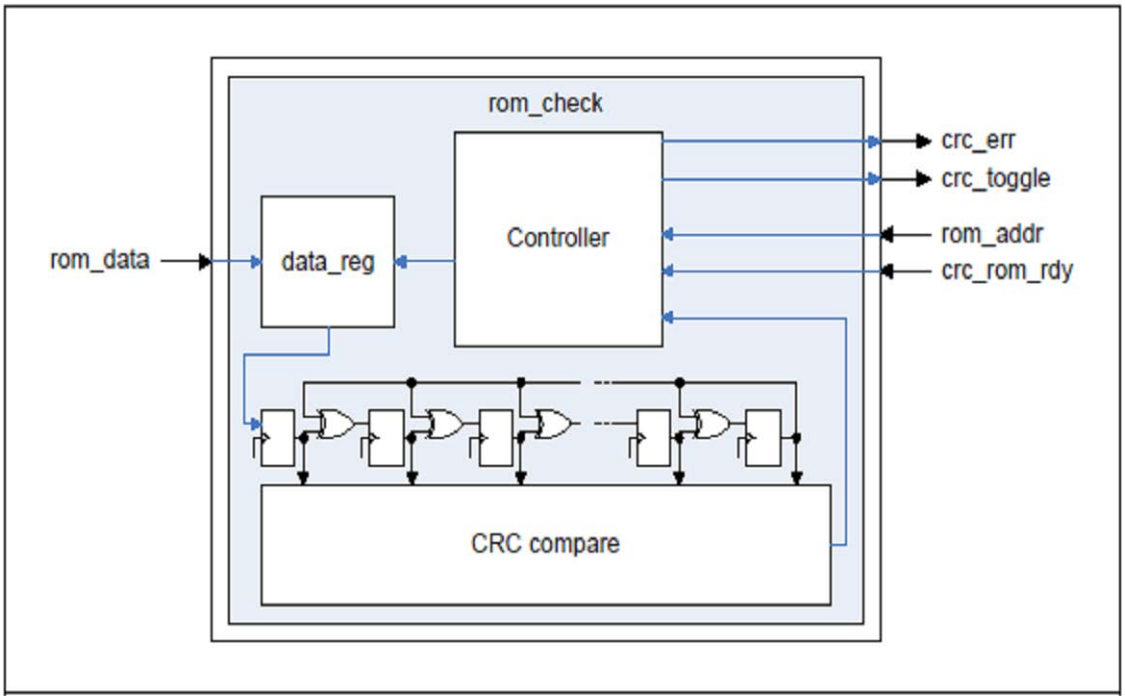
7.4.7.1 Safety Control of OTP

Req_1755 A CRC check of the OTP is done for all programmed and CRC-secured OTP words during bootloading (Startup of the SMI720).

7.4.7.2 Safety Control of DSP-ROM

Req_1757 The ROM for the DSP is continuously tested during the active phase of the DSP.
The following figure shows a scheme of the ROM-check module for DSP-ROM.

Req_1758



ROM-check module for DSP-ROM

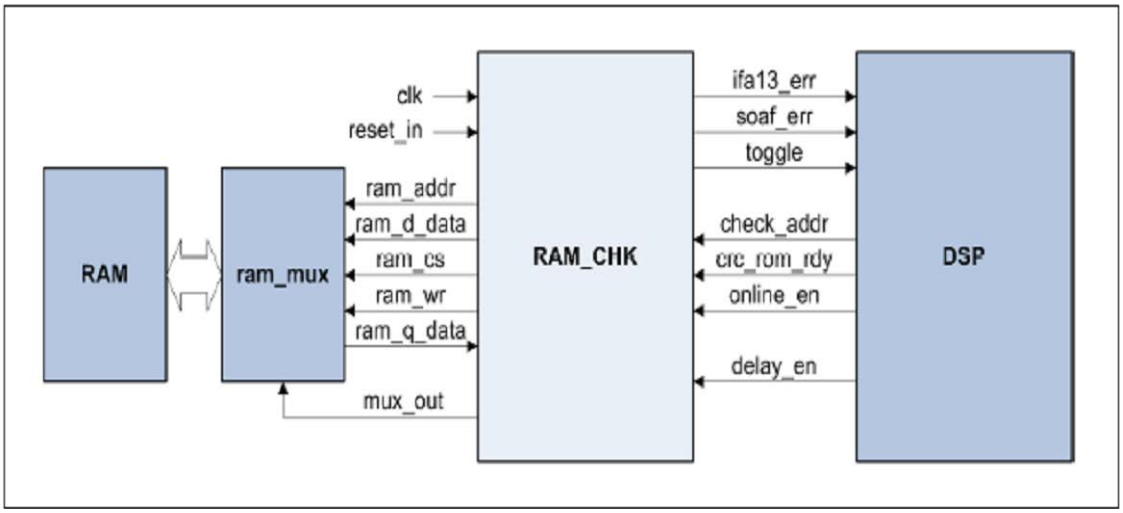
Req_1759 The ROM-check module includes two functional blocks, a LSFR with XOR feedback to implement the CRC algorithm and a controller block to manage the execution and generate all status flags. Besides the shift register a data register is implemented to store the value of the ROM cell currently processed.

7.4.7.3 Safety Control of DSP-RAM

Req_1761 The RAM for the DSP is continuously tested during the active phase of the DSP.

The following figure shows the DSP-RAM check architecture.

Req_1762



DSP-RAM check architecture

Req_1763 The following test is performed for RAM testing:

IFA9/13 (Inductive Fault Analysis) and SOAF (Stuck-at-Open Address Decoder Fault).

During start-up the IFA9/13 algorithm is performed like common MARCH test on the whole memory. In online mode, the IFA9/13 algorithm behaves like a test of a 2-cell memory. Instead of observing the whole memory and therefore writing and reading all cells, the test is performed with two cells, the base cell and the neighbor cell. The state of the memory is not altered by the test.

Each DSP RAM cell content is protected by a continuously running parity check.

In addition, the calibration data which is transferred at startup from OTP into the DSP RAM, will be secured by additional CRC algorithm.

7.4.8 Safety Control of SPI Interface

Req_1765 Whenever a communication error is detected at the interface, the interface will react immediately with an intentionally destroyed CRC/parity or react high impedant.

For a detailed description of the SMI failure handling please refer to chapter 4.3 "SPI interface".

7.4.9 Electromechanical Angular Rate and Acceleration Self Tests (BITE)

Req_1767 SMI720 has the possibility to carry out electromechanical self tests, which stimulate each channel of the sensor elements electrically, resulting in mechanical excitations of each channel of the sensor similar to external mechanical stimulations. Thus, the whole signal chain can be tested. S

The sensor provides SCON routines for a BITE sequence as well as for static BITE excitations.

7.4.9.1 BITE Sequence

Req_1769 The BS and YR BITEs are triggered in parallel according to the scheme below. The BS BITEs timing raster and the DRS timing raster will be identical and will be “absolute timed” having a programmable duration between 3ms and 192ms per sequence. Actually the time interval is configured to 26ms (+/- S

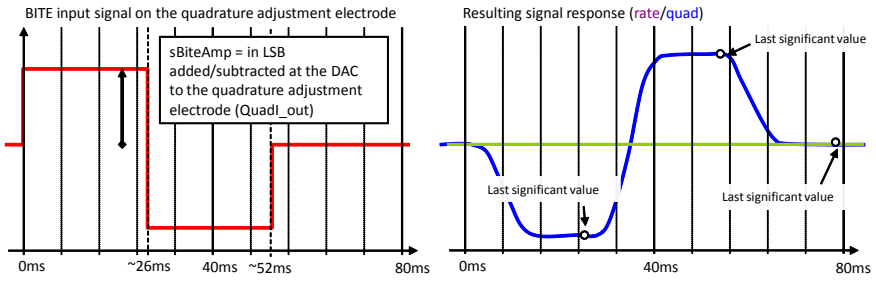
10%). This value can be changed to C-sample phase if necessary and if the startup-time is still within specification.

If the tests are not passed, they will be repeated automatically up to a programmable number N times. If the test is still not passed even after having repeated the sequence N times, corresponding failure flags will be activated. N can be configured during final test (actually N=2 is configured) or via SPI (module command).

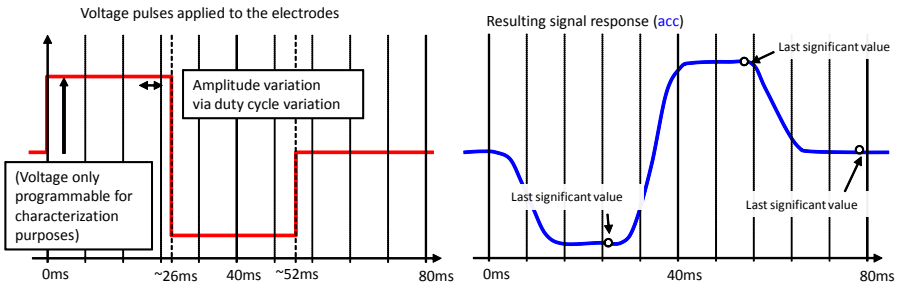
The BITE sequence applied to the channels plotted on the left-hand side, the resulting signal on the right-hand side:

Req_1770 S

Yaw Rate:



Acceleration:



The last significant value is the mean value of 4 samples. All SCON calculations are based on this value.

7.4.9.1.1 Angular Rate/Quad BITE Sequence

Req_1772 S

The YR/Quad BITE sequence consists of 3 possible pulses (ZERO, POS, NEG). The pulses are introduced in the quadrature control circuit and measured at the quadrature HF output and rate domain at the LF output of the DSP, respectively. The minimum step size will be 150°/s for each positive and negative pulse.

The BITE sequence is positive, negative, and zero pulse.

The quadrature controller is stopped during BITE and the output value is hold during the BITE-trigger.

The angular rate BITE sequence lasts for a programmable time. It contains a positive, a negative, and a zero offset phase. The settling time of these phases can be set to:

POS (1 - 64 ms)

NEG (1 - 64 ms)

ZERO (1 - 64 ms)

The SCON samples the BITE value after the individual settling times have expired.

7.4.9.1.2 Acceleration BITE Sequence

Req_1774 The acceleration BITE sequence consists of a positive (ACC1_LF_POS) and a negative (ACC1_LF_NEG) excitation. Test is passed if |ACC1_LF_POS - ACC1_LF_NEG| is within temperature dependent limits. It has been shown by analysis of all available field failures that the separate evaluation of POS and NEG (relative to zero) did not reveal more failures than the evaluation of |POS-NEG|. S

Temperature dependent trimming is done during the production tests. During production test trim settings are done to obtain at least 3g BITE differential amplitude between pos or neg BITE (difference).

The AMPLITUDE of the self-test is programmable by trimming the duty cycle of the excitation voltage.

The acceleration BITE sequence lasts for a programmable time. It contains a positive and a negative phase. The settling time of these phases can be set to:

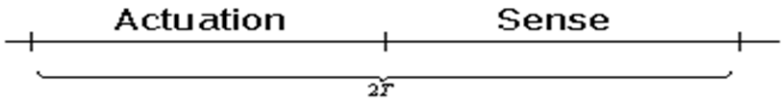
POS (1 - 64 ms)

NEG (1 - 64 ms)

The SCON samples the BITE value after the individual settling times have expired.

When the self-test is switched on the sample frequency of the front end is reduced to half, i.e. the sample-time is 2*Ts. Each Self-Test period consists of an actuation or excitation phase and a sense or measurement phase. These phases are of equal duration i.e. Ts, shown in the following figure:

Req_1775 S



Acceleration BITE

7.4.9.1.3 BITE Control

Req_1777 Signals are taken from LF or HF output channels of the DSP S

QUAD_HF

RATE_LF

ACC1_LF

Req_1779 For each of the angular rate and acceleration sensors there are two kinds of BITE operations available: Static BITE and BITE sequence. ACC BITE and ARS BITE are triggered by register HW_SCON_Config.bite_control (Page: 0; ID: 0x7) as follows. S

ACC = HW_SCON_Config.bite_control.bite_acc_control_code = "00" ; ACC BITE off

ACC = HW_SCON_Config.bite_control.bite_acc_control_code = "01" ; ACC Static BITE positive phase on

ACC = HW_SCON_Config.bite_control.bite_acc_control_code = "10" ; ACC Static BITE negative phase on

ACC = HW_SCON_Config.bite_control.bite_acc_control_code = "11" ; ACC BITE Sequence on

ARS = HW_SCON_Config.bite_control.bite_yrs_control_code = "000" ; ARS BITE off

ARS = HW_SCON_Config.bite_control.bite_yrs_control_code = "001" ; ARS Static BITE positive phase on

ARS = HW_SCON_Config.bite_control.bite_yrs_control_code = "010" ; ARS Static BITE negative phase on

ARS = HW_SCON_Config.bite_control.bite_yrs_control_code = "011" ; ARS Static BITE zero offset phase on

ARS = HW_SCON_Config.bite_control.bite_yrs_control_code = "1XX" ; ARS BITE Sequence on

Type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
logic	0	0	0	0	0	ARS			0	0	0	0	0	0	ACC	

Static BITE (manually triggered):

Static BITEs in any combinations (YR/QUAD + ACC) can be triggered via SPI any time during normal operation. The main use will be for characterization purposes; nevertheless, CI will be set to b1 in the corresponding channels. No evaluation of the BITE amplitudes takes place, nor will the amplitudes be stored in the registers.

The excitations of static BITEs will remain triggered as long as no switch off command is sent as a **separate SPI request**. Similar to the BITE sequence, after having switched off the BITE excitations, the SCON waits for the filters to be flushed, and assures that the yrs_quad_HF_tol will not start earlier than the programmed filter_flush_time after BITE is switched off (since the quad regulator needs this time to be fully functional again). This means that the earliest time to remove the b1 condition from the YR and ACC channels is the programmed filter_flush_time.

A manual evaluation of the BITE-tests can be done in the following way:

| (POS deflection RATE_LF - NEG deflection RATE_LF) - (ref_yrs_rate_seq_bite + tc_yrs_rate_seq_bite*TEMP1) | < BITE_YRS_RATE_POS_NEG_TOL

| (POS deflection QUAD_HF - NEG deflection QUAD_HF) - (ref_yrs_quad_bite_pos_neg + tc_yrs_quad_bite_pos_neg*TEMP1) | < BITE_YRS_QUAD_POS_NEG_TOL

| (POS deflection QUAD_HF - ZERO deflection QUAD_HF) - ref_yrs_quad_bite_pos_zero | < BITE_YRS_QUAD_POS_ZERO_TOL

| (NEG deflection QUAD_HF - ZERO deflection QUAD_HF) - ref_yrs_quad_bite_neg_zero | < BITE_YRS_QUAD_NEG_ZERO_TOL

| (POS deflection ACC1_LF - NEG deflection ACC1_LF) - (ref_acc1_bite_pos_neg + tc_acc1_bite_pos_neg*TEMP1) | < BITE_ACC_POS_NEG_TOL

BITE-test	input	type	tolerance*
BITE_YRS_RATE_POS_NEG_TOL	RATE_LF	manual evaluation ECU	3600 LSB
BITE_YRS_QUAD_POS_NEG_TOL	QUAD_HF	manual evaluation ECU	15%
BITE_YRS_QUAD_POS_ZERO_TOL	QUAD_HF	manual evaluation ECU	-
BITE_YRS_QUAD_NEG_ZERO_TOL	QUAD_HF	manual evaluation ECU	-
BITE_ACC_POS_NEG_TOL	ACC1_LF	manual evaluation ECU	45%

Remark: All tc_... parameters must be interpreted as a signed 16bit value with 14 fractional bits.

BITE Sequence (manually triggered):

A BITE sequence including the repetitions and evaluation and setting of the corresponding flags by the TIG720 itself can also be triggered by a SPI command.

Acceleration BITE Sequence consists of one or more sequences. Each sequence covers 3 subsequent phases with the sensor excited at positive level for the 1st phase, at negative level for the 2nd phase and without excitation for the 3rd phase. At the end of each phase the mean value of 4 samples is calculated and used for the SCON evaluation.

Angular rate BITE Sequence consists of one or more sequences. Each sequence covers 3 subsequent phases with the sensor excited at positive level for the 1st phase, at negative level for the 2nd phase

and at zero offset level for the 3rd phase. At the end of each phase the mean value of 4 samples is calculated and used for the SCON evaluation.

Sensor internal BITE evaluation is done in the following way:

| (BITE_YRS_RATE_POS - BITE_YRS_RATE_NEG) - BITE_YRS_RATE_POS_NEG_REF | < BITE_YRS_RATE_POS_NEG_TOL

| (BITE_YRS_QUAD_POS - BITE_YRS_QUAD_NEG) - BITE_YRS_QUAD_POS_NEG_REF | < BITE_YRS_QUAD_POS_NEG_TOL

| (BITE_YRS_QUAD_POS - BITE_YRS_QUAD_ZERO) - BITE_YRS_QUAD_POS_ZERO_REF | < BITE_YRS_QUAD_POS_ZERO_TOL

| (BITE_YRS_QUAD_NEG - BITE_YRS_QUAD_ZERO) - BITE_YRS_QUAD_NEG_ZERO_REF | < BITE_YRS_QUAD_NEG_ZERO_TOL

| (BITE_ACC_POS - BITE_ACC_NEG) - BITE_ACC_POS_NEG_REF | < BITE_ACC_POS_NEG_TOL

with

BITE_YRS_RATE_POS_NEG_REF = TEMP * TEMP_COEFF_YRS_RATE_POS_NEG + (uncompensated BITE_YRS_RATE_POS_NEG_REF)

BITE_YRS_QUAD_POS_NEG_REF = TEMP * TEMP_COEFF_YRS_QUAD_POS_NEG + (uncompensated BITE_YRS_QUAD_POS_NEG_REF)

BITE_YRS_QUAD_POS_ZERO_REF = TEMP * TEMP_COEFF_YRS_QUAD_POS_ZERO + (uncompensated BITE_YRS_QUAD_POS_ZERO_REF)

BITE_YRS_QUAD_NEG_ZERO_REF = TEMP * TEMP_COEFF_YRS_QUAD_NEG_ZERO + (uncompensated BITE_YRS_QUAD_NEG_ZERO_REF)

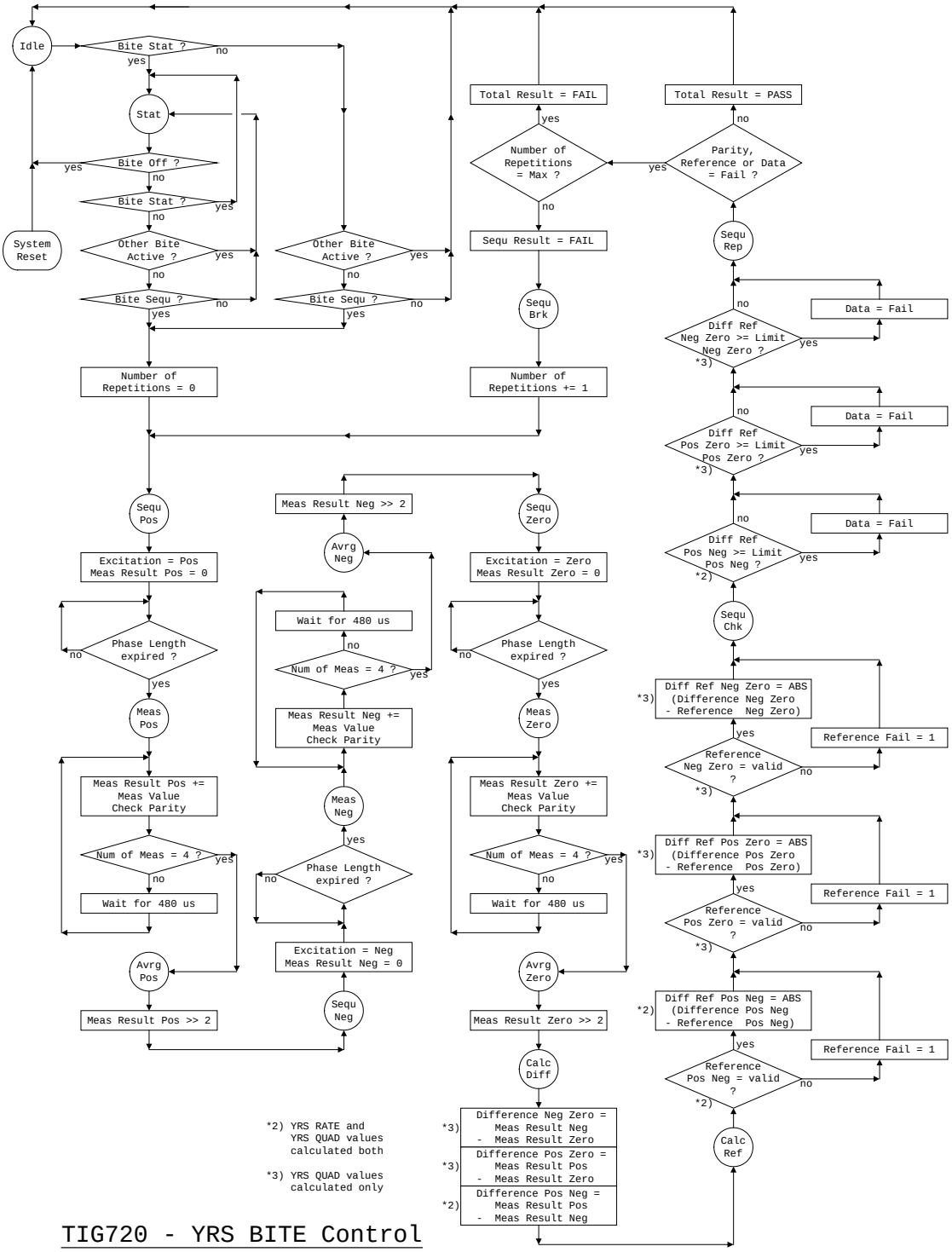
BITE_ACC_POS_NEG_REF = TEMP * TEMP_COEFF + (uncompensated BITE_ACC_POS_NEG_REF)

BITE-test	input	type	tolerance*
BITE_YRS_RATE_POS_NEG_TOL	RATE_LF	sensor internal evaluation	3600 LSB
BITE_YRS_QUAD_POS_NEG_TOL	QUAD_HF	sensor internal evaluation	15%
BITE_YRS_QUAD_POS_ZERO_TOL	QUAD_HF	sensor internal evaluation	45%
BITE_YRS_QUAD_NEG_ZERO_TOL	QUAD_HF	sensor internal evaluation	45%
BITE_ACC_POS_NEG_TOL	ACC1_LF	sensor internal evaluation	45%

*A-samples: Tolerances are used for SMI720 A-samples and represent not the final state for series production. Some effects with influence on BITE-tests were identified during A-sample phase. Measures for SMI720 C-samples were implemented.

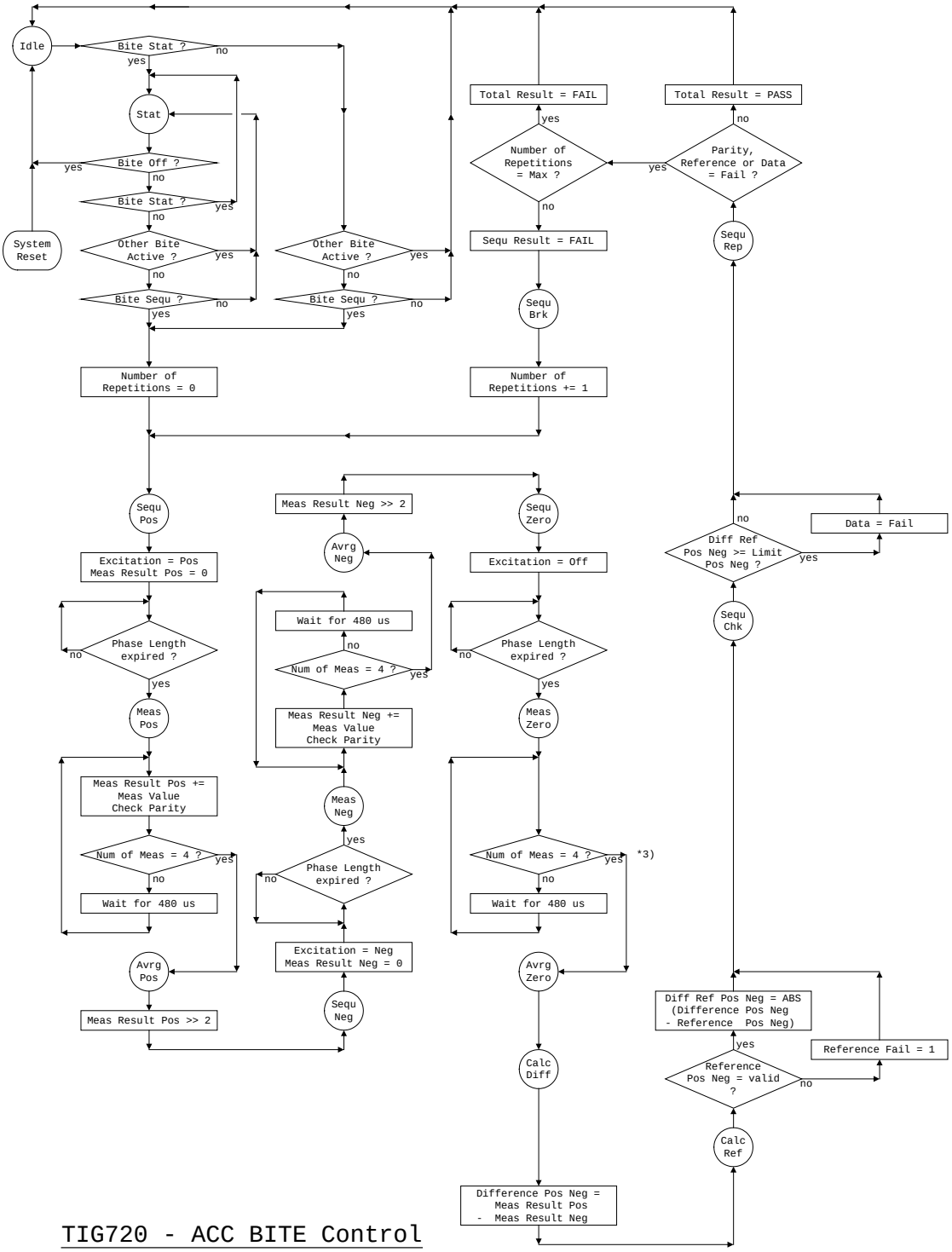
If one of the previously described checks fails, the current sequence will be repeated if the number of repetitions has not reached its maximum. YRS BITE will be marked as "Failed" if the maximum number of repetitions is reached, i.e. a flag is set that is forwarded to HW SCON Flag Control Unit. In case the BITE is repeated, the flag is reset if the BITE execution has been successful.

Req_1781 The following flowchart shows YRS BITE Sequence Hardware Control Flow. BITE Sequence operation is processed according to the states that are included.



TIG720 - YRS BITE Control

Req_2230 The following flowchart shows ACC BITE Sequence Hardware Control Flow. BITE Sequence operation is processed according to the states that are included.



TIG720 - ACC BITE Control

7.4.9.1.4 Programmable Parameters

Req_1783 Programmable parameters are S

- the number of repetitions until BITE sequences are discontinued (0: single run, ..., 15: up to 15 runs).

- the BITE tolerances will be defined during characterization of the SMI720 A-samples.
  yrs_rate_seq_bite Tolerance pos-neg,
  yrs_quad_seq_bite Tolerances pos-zero, neg-zero, pos-neg
  acc1_seq_bite Tolerance pos-neg
- the flush time after BITE (and for the three error counter) can be programmed between 0ms and 127ms.

7.4.9.1.5 Read-out possibilities of the BITE sequence values

Req_1785 The values that lead to the final flag status (valid or invalid) are stored in a register and are readable via all interfaces (incl. CC32in w/o password).

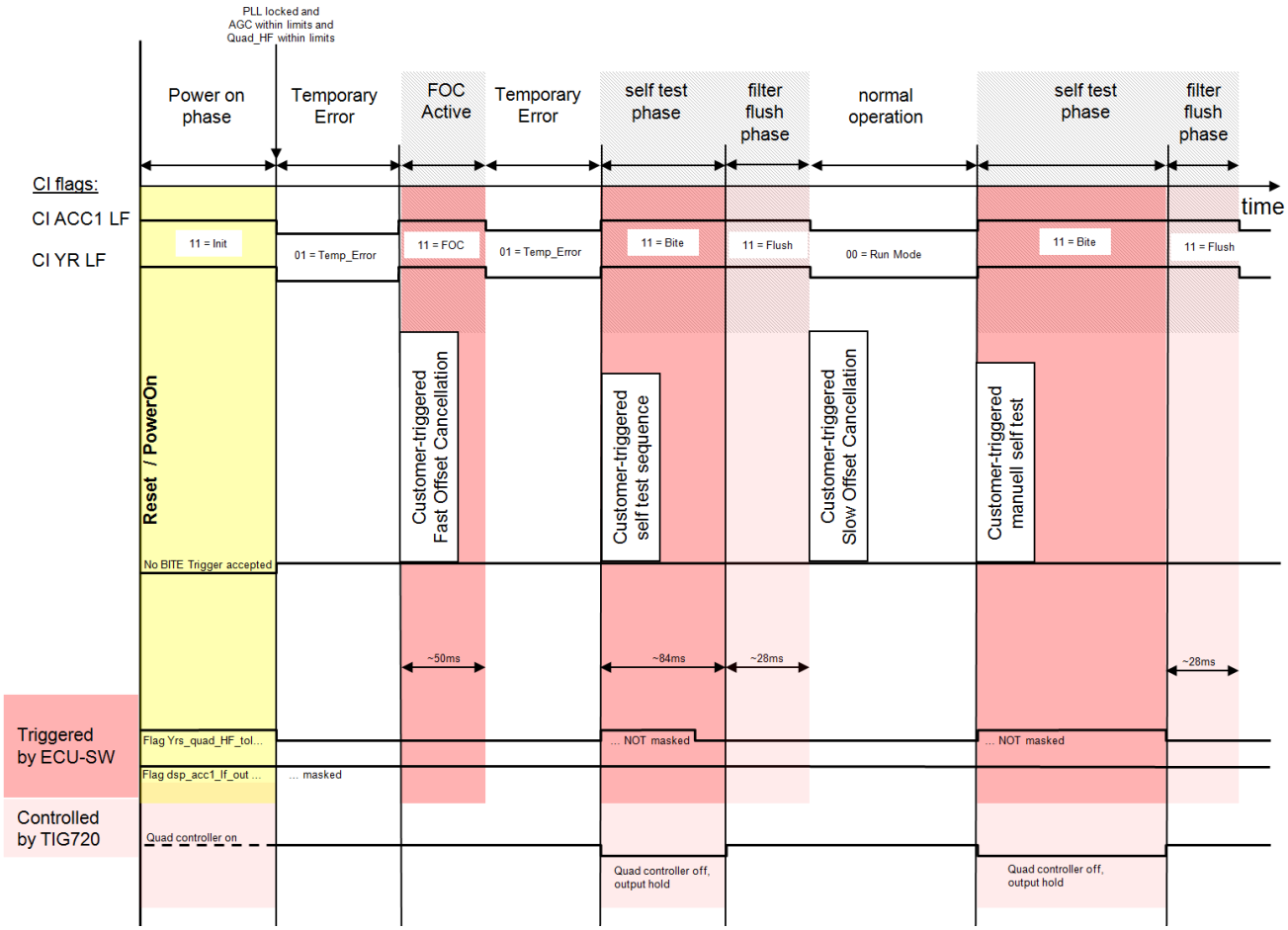
LastBite_Acc1_Pos
LastBite_Acc1_Neg
LastBite_QUAD_YR_Pos
LastBite_QUAD_YR_Neg
LastBite_QUAD_YR_Zero
LastBite_RATE_YR_Pos
LastBite_RATE_YR_Neg
LastBite_RATE_YR_Zero

7.4.9.1.6 Triggering of the BITE at startup

Req_1808 In order to guarantee the integrity of the safety concept, the customer needs to trigger the BITE sequence or a manual BITE for ARS and ACC at least once per power-on cycle.

7.4.9.2 Timing Overview of BITE Sequence and Static BITE

Req_1814 S



Timing of BITEs and flags. *The BITE sequence at startup is optional and can be deactivated (see reset vector).

7.4.9.3 Continuous Quadrature BITE (cQ-BITE)

Req_1816 No implementation of an continuous electromechanical self test foreseen due to inacceptable influence on sensor performance.

7.4.9.4 Acceleration Continuous BITE

Req_1887 No implementation of an continuous electromechanical self test foreseen due to inacceptable influence on sensor performance.

7.4.10 ACC Disturbance Detection

Req_1889 The acc disturbance detection is not a sensor failure flag. The disturbance detection is designed to detect high speed vibration events in the high bandwidth sigma delta modulator bit streams.

A weighted counter is used to sum up consecutive bit trains of same polarity. The weight can be calibrated in 8 steps with 3 bits with the following formula:

Req_1890 Weight (inc_value) = 1/(2^inc_value) with inc_value = 0 ... 7

Req_1891 The start_value is a 16 bit value, which determines the start of the incremental adder.

Req_1892 The incremental is done with the formula:

y(0) = start_value

y(N+1) = Y(N) * (1 + Weight(inc_value))

N is increased as long as the bit stream delivers a constant row of zeros or ones. If the SD bit stream switches from 0 to 1 (or 1 to 0) the counter value is transferred to the second counter and the first counted is reset and starts over again.

Req_1893 A second counter sums up the upper 8 bit values of the first counter and compares it with a programmable limit.

(Name: acc1_overload_limit)

Req_1894 Range of start value: 1...65535

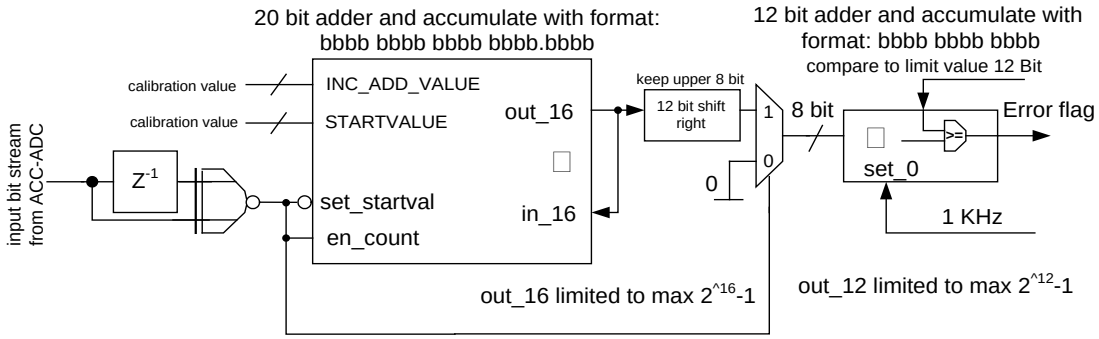
Req_1895 Range of increment value: 1...1/128

Req_1896 Range of error limit: 0...4095

Req_1897 Time of $T_{errorsample}$: 1ms

Req_1898 The error flag has the name acc1_overload_det.

Req_1899 Picture of disturbance detection:

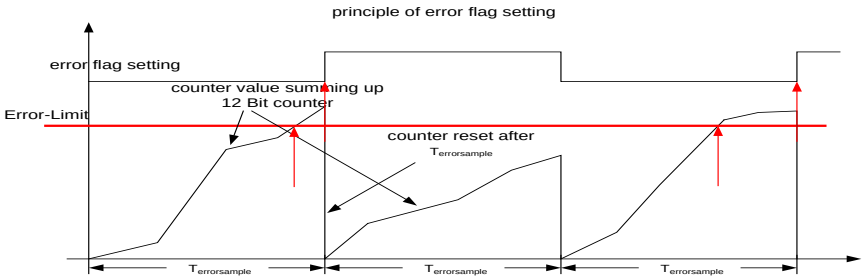


Y^0 = STARTVALUE

$Y^{n+1} = Y^n * (1 + INC\_ADD\_VALUE)$

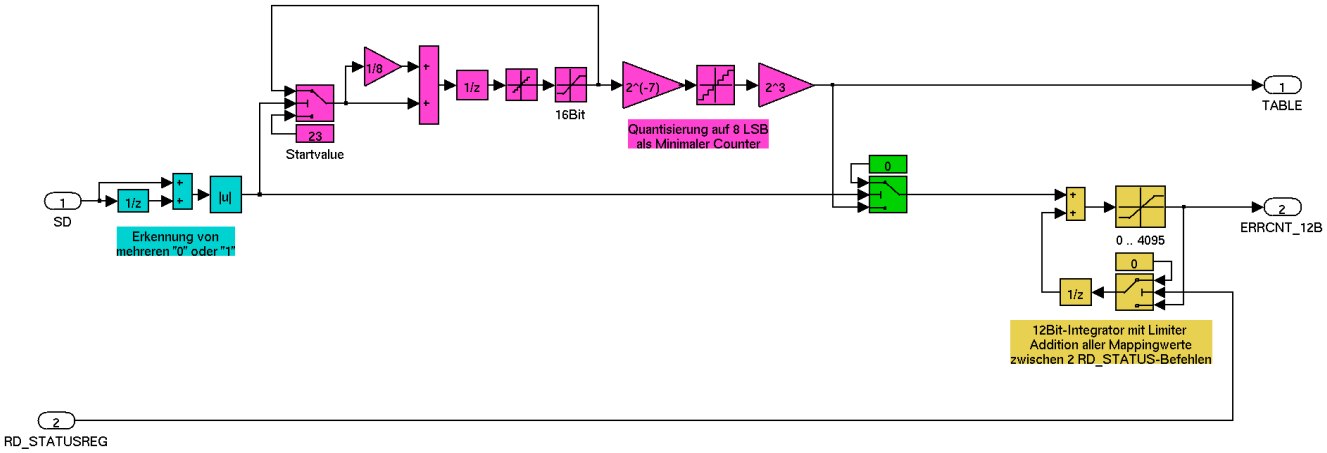
$Y^{n+1} = LIMIT(Y^{n+1}) <= 65535$

Req_1900 Error flag behavior:



Error condition is latched within one time interval $T_{errorsample}$ and then indicated throuout the next time interval.

Req_1901



7.4.11 Operating Conditions Safety

Req_2055 Communication errors like wrong CRC/parity are assumed to be detected by the communication partners by 100%. S

The wrong CRC/parity may be set by the sensor intentionally to indicate malfunctioning, but may also be a result of timing or amplitude problems of the communication signal.

A wrong CRC/parity may therefore indicate a malfunctioning of the sensor communication interfaces in a double way.

The error indicators of the SPI protocols for CC32in-SPI and for OpenSPI need to be evaluated by the communication partners since they may indicate a problem of the communication transfer (like missing clock pulses) or a fault of the sensor SPI interface.

The error bits included in the SPI message (CI-flags = channel information) have to be evaluated by the ECU judging the validity of the corresponding sensor signal. If the CI-flag indicates an error of the SMI720 the sensor data of the corresponding channel is not valid. Measures within the ECU must be implemented to avoid a malfunction of the system due to wrong sensor data caused by an internal error of the SMI720.

The channel information of the SPI is the relevant information to determine if the sensor data are valid or not. All other failure information of the SMI720 (e.g. cluster-flag or single failure flag information) must not be used by the ECU-system to evaluate if the sensor signal are valid.

Req_2056 The following parameters are configurable by the customer (see Section 2.4.4). Provided metric calculation is only valid for the following settings: S

1) Error Counter Limits [16 LSB, i.e. 16ms +-10%]
2) SPI Driver Strength [strong]
3) SPI Protocol Settings via auto detect (CPOL, CPHA, protocol) [all settings valid]
4) Safety IDs [all settings valid, needs to be monitored by customer]
5) Filter Flush Time [>= 28 LSB, i.e. 28 ms +-10%]
6) BITE repetitions [>= 1]

Req_1351 Monitoring an open blocking cap for VDD3 and VDD_IO is not possible by SMI720, as these pins need to be connected to an ECU power supply.

Req_2226 During each startup within ECU Lifetime the Power-On-Test and Built-in-Self-Test has to be performed to ensure the sensor function within specification. LBIST is used for selected multiple point faults considered in latent metric calculations. S

7.5 Safety Validation

Req_1906 All failure modes that are accessible via experiment will be checked via experiment, together with their corresponding monitors (e.g., bond ruptures / short cuts, temperature or supply voltage out of range, …). However, the largest part of the failure modes will not or inadequately be accessible by experiment (e.g., CMA particles, spring breaks in CMA/CMG, failures in the ASIC). Therefore, design considerations, failure injection methods and simulations will be used, together with adequate reviewing, for the validation of the safety concept. A complete validation plan will be worked out with and provided to the customer (safety function which were already validated by SMI710/SMI700 and were 100% carried over to SMI720 may not be validated in SMI720 again).

7.6 Flexibility and Validity of the Safety Concept

Req_1908 It is technically possible to change the debouncing or filter_flush_time settings on customer-level for application-specific needs. However, changing any settings in the debouncing characteristics or filter_flush_time must not be done without evaluating the effects on the safety concept. S

In general, the sensor will be delivered in one configuration including surveillance limits, debouncing settings etc for the default filter settings, and a set of recommended filter_flush_time (for the failure counters and BITE) that will be described in the data sheet.

8. Simulation Models

Req_601 To support our customers during the development and application, Bosch provides different simulation models. The models are useful to investigate the overall system function assuming nominal conditions. The user of the models has to consider that there can be deviations between the model and the real life because of simplified modeling of the device.

Req_602 The models which Bosch will provide are:

EDIF (Digital Model) for simulation of the SPI-interface

System Simulation Model (fast): overall system simulation

System and Vibration Simulation model: e.g. simulation of mechanical overload or vibration

8.1 EDIF-Model

Req_604 **Use:** The EDIF net list is used for sensor emulation in system integration tests like HIL (HW in the loop) or SW-Releases.

Req_605 **Features:**

The features of the supplied EDIF-Model are described in the attachment "QuaTe_EDIF_Description_TIG720A_d120910_v1_1".

8.2 System Simulation Model (fast)

Req_614 **Use:** The fast system simulation model is a transient model for sensor emulation in airbag algorithm development.

Req_615 **Features:**

- Interface with VDA-AK interface (see Anforderungen_Sensor_Simulationmodel_V21)
- File format: *.dll (OEM use possible)
- Additional file format: MATLAB Simulink (internal use only)
- Calculation speed: simulation time will be at least 50 times faster than signal duration
- No timeout limitation for very long input data streams (up to 1 minute)
- The model will be verified by experiments
- Description of validity range of the model, description of sensor performance out of this validity range (verbal description in customer model documentation)
- Customer documentation will be provided
- The filter chain will be implemented highly detailed (incl. rounded coefficients, correct signal bit width, etc.)
- Total signal delay will be modeled to a precision of at least 5%
- Failure flags, signal path detail and error handling will be included in the model similar to the SMI710 project
- Matlab sensor model can be executed with Matlab version 2010 and 2011

8.3 System and Vibration Simulation Model (detailed)

Req_625 **Use:** The system and vibration simulation model is a transient model intended to assess the vibration performance of SMI720 within the sensor effect chain of vehicle, ECU sensor and algorithm.

Req_626 **Features:**

- File format: MATLAB (internal use only)
- Calculation speed with error flags and error counters:
  ~25 s calculation time for 10 s simulation (depending on PC hardware)
- Handles up to 1 sec long input data streams
- The model will be verified by experiments
- Description of validity range of the model, description of sensor performance out of this validity range (verbal description in customer model documentation)
- Customer documentation will be provided
- The vibration sensitivity will be modeled including mechanical, electrical and clipping effects.
- Failure flags, signal path detail and error handling will be included in the model similar to the SMI710 project (see SMI70_710_Anforderungen_Wirkkettenmodell_v3_0 for details)
- MATLAB sensor model can be executed with MATLAB version 2010 and 2011

9. Product Qualification

Req_701 The test plan is available in DOORS (see link, 30_TestSpecification/CharList SMI720). The C-sample test plan will be aligned with the customers. The test reports will be provided to the customers.

Req_702 Together with the D-Samples (PPAP) Bosch will deliver qualifications report with final results.

Req_703 The EMC performance of the SMI720 will be checked according to the test plan **13TE015_EMC_Messplan_SMI720_130226**.

The final test plan of C-samples will be discussed with the customers based on A-sample results.

For EMC test conditions and detailed results see report **EMC-C-Samples 14F3335 and 13T3121_EMC_Messplan.**

Req_1977 The PSRR of SMI720 will be qualified in the following way:

An AC signal will be superimposed to the sensor power supply with an amplitude of +/-25mV and its frequency is swept between 50 Hz and 1 MHz (max. step width 200 Hz). For this stimulus, the sensor signals will stay within the specified limits.

Additionally, a stimulus of +/-100mV between 50 Hz and 1 MHz will be characterized with SMI720 and the results will be provided to the customer (specifications are not valid for this stimulus).

The PSRR characterization will be carried out with and without a low-pass filter in the voltage supply.

Req_704 The C-samples will be qualified according to the qualification plan ***ERPA 2982*** (incl. ESD, etc.) according to AEC/Q100. Drop test (1.2 m guided) will be included.