

# Data Sheet CG904, CG903, CG902 Airbag System ASIC

Version 1.1

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# Data sheet CG904, CG903, CG902

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1.1	30.07.2015	official release

Changes to the prior version are highlighted in yellow color.

Typical values as well as Min and Max values are based on simulations and the first silicon samples. Values have to be approved by the final characterization until QGC4.

The identifiers of the electrical characteristics are subject to change.

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## 1. General

### 1.1 Overview

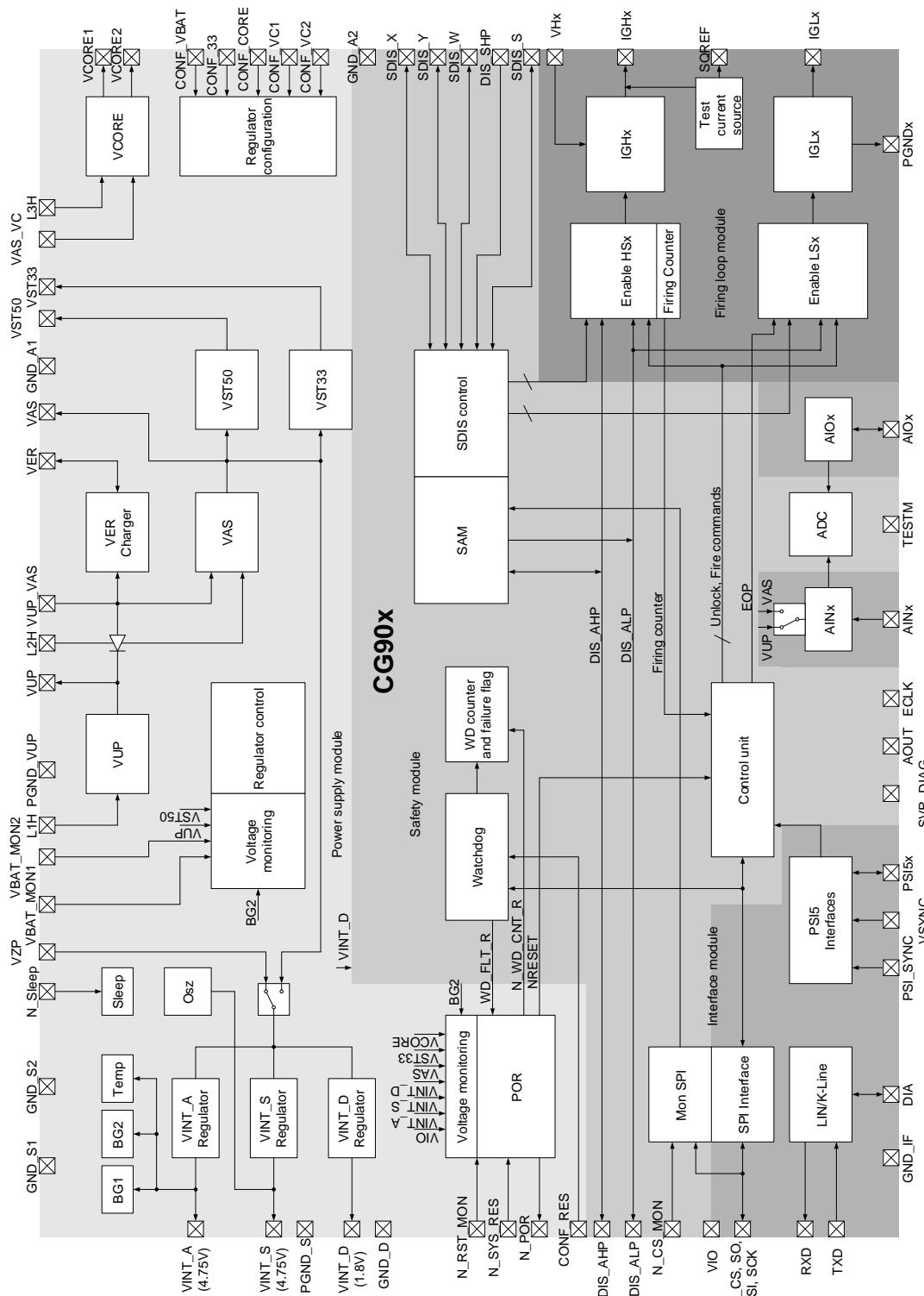
The airbag system ASIC chipset is a solution for airbag safety applications that consists of the three system ASICs CG904, CG903, and CG902. The ASICs connect to the vehicle battery and provide multiple voltages required to supply a typical airbag application. The family concept of the chipset with pin-compatible ASICs allows its use in high-end airbag systems with a varying number of firing loops and sensor interfaces according to the PSI5 industry standard. Communication with the system ASICs is established by the SPI standard.

#### Features:

- Pin-compatible ASICs CG904, CG903, and CG902
- Operation from a central supply  $V_{ZP} = 5.2 \text{ V} \dots 18 \text{ V}$  (typical)
- Support for a complete airbag system architecture with
  - power supplies for energy reserve and squib firing (24 V and 33 V),
  - peripheral sensors (6,7 V),
  - ECU internal sensors and CAN (5,0 V),
  - local analog and digital supply (3,3 V), and
  - microcontrollers (3,3 V or 1,29 V)
- Programmable converter slope shaping and frequency jitter for improved EMC performance for all switching regulators
- Watchdog, power-on-reset, sleep mode, and overtemperature shutdown functionality
- Support for 16 (CG904), 12 (CG903), and 8 (CG902) fully-integrated firing loops
- Support for 6 (CG904), 4 (CG903), and 2 (CG902) peripheral sensor interfaces (PSI5 1.3)
- Sophisticated safety concept and fail-safe design
- Extensive and high-precision self-diagnostic capabilities
- 32-bit serial peripheral interface (SPI) frame with 16 bit for incoming and outgoing data
- 10 configurable analog input (AIN) channels for switch and hall sensor evaluation
- 2 configurable and general-purpose analog I/O channels
- LIN 2.1 interface programmable as a general-purpose digitally programmed current sink with PWM functionality

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## 1.2 Block Diagram



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## 1.3 Pinning

The airbag system ASICs are available in a TQFP128epad package. With its small body of 14x14mm<sup>2</sup> in size, 1.0mm in height and a fine pitch of 0.4mm this package reduces the necessary space on the PCB to a minimum and offers a low thermal resistance. Furthermore, all ASICs are pin compatible.

### 1.3.1 Pinning CG904 TQFP128epad

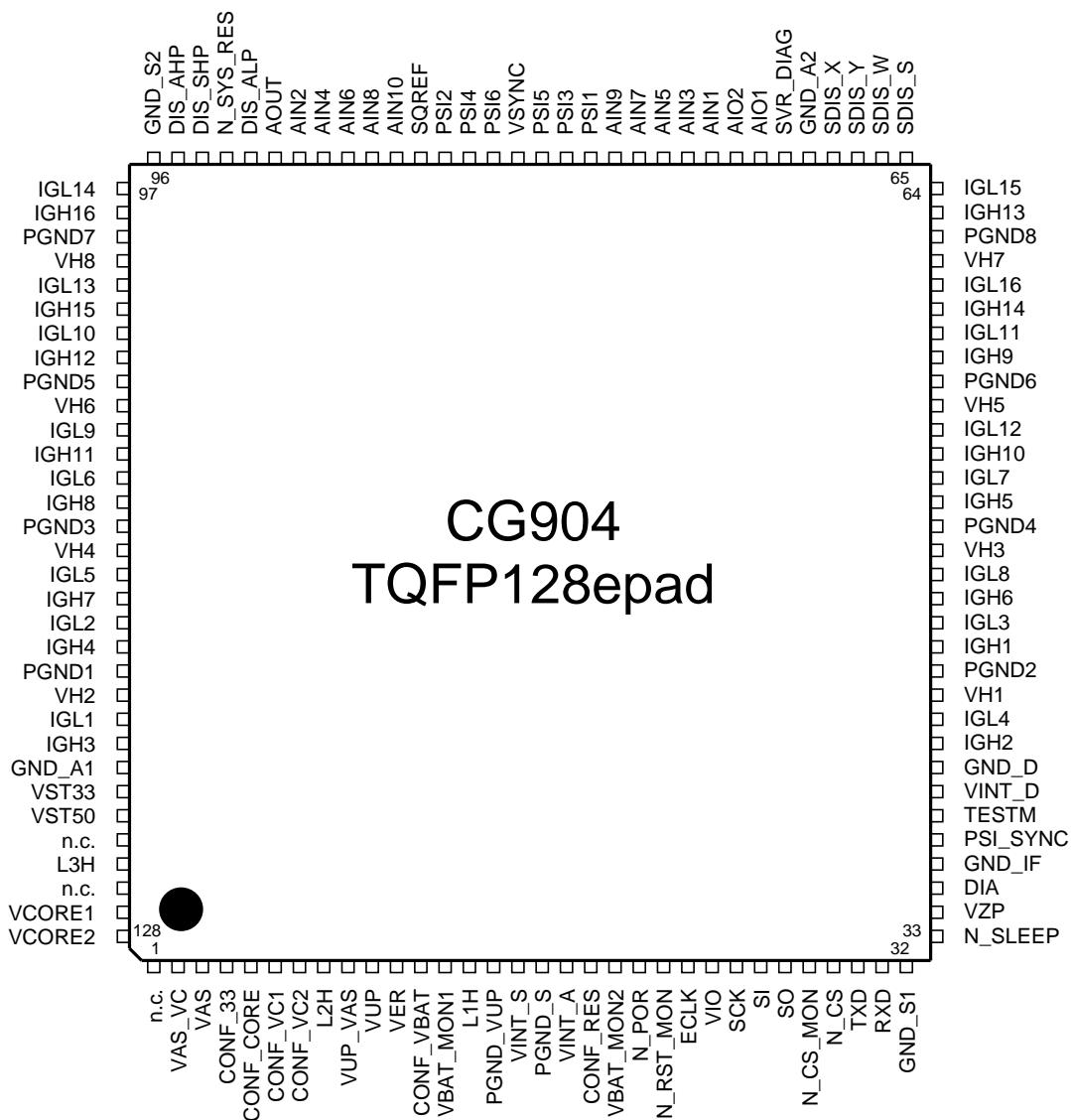


Figure: CG904 TQFP128epad package

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## 1.3.2 Pinning CG903 TQFP128epad

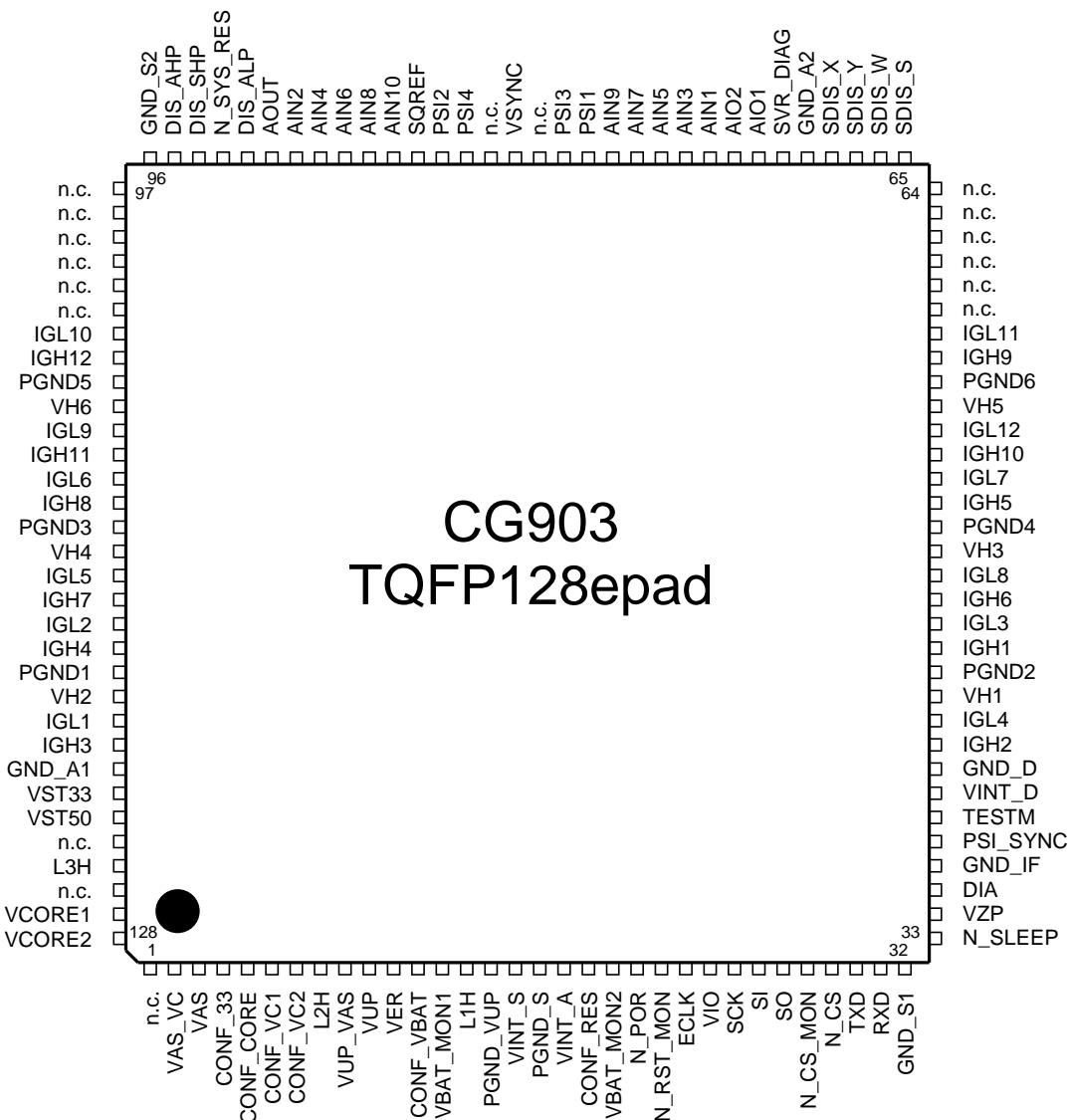


Figure: CG903 TQFP128epad package

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### 1.3.3 Pinning CG902 TQFP128epad

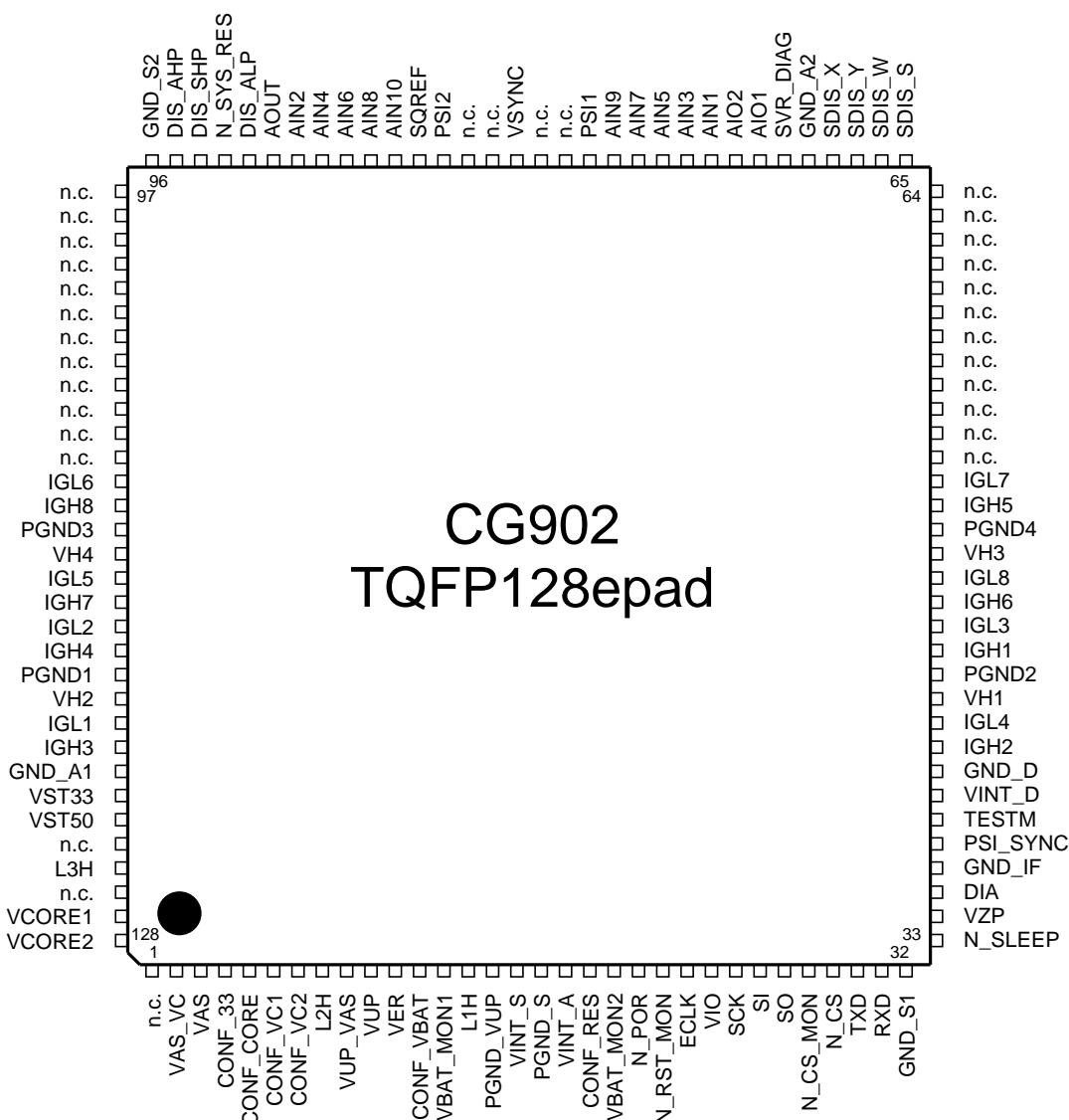


Figure: CG902 TQFP128epad package

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## 1.4 Pin Description

<b>pin</b>	<b>name</b>	<b>direction</b>	<b>description</b>	<b>module</b>
1	n.c.	open	not connected	-
2	VAS_VC	power	power supply for VCORE	POM
3	VAS	power	stabilized analog supply 6,7 V	POM
4	CONF_33	input	configuration 3,3V regulator	POM
5	CONF_CORE	input	configuration core regulator	POM
6	CONF_VC1	input	configuration core regulator voltage	POM
7	CONF_VC2	input	configuration core regulator voltage	POM
8	L2H	power	coil 2 VAS high side connection	POM
9	VUP_VAS	power	power supply for VAS	POM
10	VUP	power	up converter output	POM
11	VER	power	energy reserve output	POM
12	CONF_VBAT	input	configuration boost converter on threshold	POM
13	VBAT_MON1	input	battery voltage monitoring	POM
14	L1H	power	coil 1 VUP high side connection	POM
15	PGND_VUP	ground	ground	POM
16	VINT_S	power	internal supply for switch regulator 4,75V	POM
17	PGND_S	ground	ground	POM
18	VINT_A	power	internal analog supply 4,75V	POM
19	CONF_RES	input	configuration reset behavior	SAM
20	VBAT_MON2	input	battery voltage monitoring	POM
21	N_POR	output	power on reset	POM
22	N_RST_MON	input	external reset monitoring	POM
23	ECLK	input	system clock 4MHz	System
24	VIO	power	internal I/O supply 3,3V	POM
25	SCK	input	SPI clock input	SPI
26	SI	input	SPI slave input	SPI
27	SO	bi-dir	SPI slave output (SO monitor internal)	SPI
28	N_CS_MON	input	chip select monitor	SPI
29	N_CS	input	chip select ASIC	SPI
30	TXD	input	transmit data	LIN
31	RXD	output	receive data	LIN
32	GND_S1	ground	ground	-

Table: Pin description TQFP128epad package bottom side

### Application Note:

All not connected pins (n.c.) must be connected to ground or remain unconnected.

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<b>pin</b>	<b>name</b>	<b>direction</b>	<b>description</b>	<b>module</b>
33	N_SLEEP	input	sleep control	POM
34	VZP	power	central protected supply	POM
35	DIA	dedicated	LIN bus	LIN
36	GND_IF	ground	ground	LIN
37	PSI_SYNC	input	PSI sync pulse synchronization	PSI
38	TESTM	input	ASIC test mode activation	System
39	VINT_D	power	internal digital supply 1,8V	POM
40	GND_D	ground	ground	POM
41	IGH2	dedicated	high side power stage 2	FLM
42	IGL4	dedicated	low side power stage 4	FLM
43	VH1	power	supply voltage high side power stage	FLM
44	PGND2	ground	power stage ground	FLM
45	IGH1	dedicated	high side power stage 1	FLM
46	IGL3	dedicated	low side power stage 3	FLM
47	IGH6	dedicated	high side power stage 6	FLM
48	IGL8	dedicated	low side power stage 8	FLM
49	VH3	power	supply voltage high side power stage	FLM
50	PGND4	ground	power stage ground	FLM
51	IGH5	dedicated	high side power stage 5	FLM
52	IGL7	dedicated	low side power stage 7	FLM
53	IGH10 *)	dedicated	high side power stage 10	FLM
54	IGL12 *)	dedicated	low side power stage 12	FLM
55	VH5 *)	power	supply voltage high side power stage	FLM
56	PGND6 *)	ground	power stage ground	FLM
57	IGH9 *)	dedicated	high side power stage 9	FLM
58	IGL11 *)	dedicated	low side power stage 11	FLM
59	IGH14 **)	dedicated	high side power stage 14	FLM
60	IGL16 **)	dedicated	low side power stage 16	FLM
61	VH7 **)	power	supply voltage high side power stage	FLM
62	PGND8 **)	ground	power stage ground	FLM
63	IGH13 **)	dedicated	high side power stage 13	FLM
64	IGL15 **)	dedicated	low side power stage 15	FLM

\*) pin is not connected in CG902

\*\*) pin is not connected in CG903/CG902

Table: Pin description TQFP128epad package right side

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<b>pin</b>	<b>name</b>	<b>direction</b>	<b>description</b>	<b>module</b>
65	SDIS_S	bi-dir	special disable switch evaluation	SAM
66	SDIS_W	bi-dir	special disable w-channel	SAM
67	SDIS_Y	bi-dir	special disable y-channel	SAM
68	SDIS_X	bi-dir	special disable x-channel	SAM
69	GND_A2	ground	ground	-
70	SVR_DIAG	dedicated	input test sink for SVR test	FLM
71	AIO1	dedicated	analog I/O	AIO
72	AIO2	dedicated	analog I/O	AIO
73	AIN1	dedicated	analog input	AIN
74	AIN3	dedicated	analog input	AIN
75	AIN5	dedicated	analog input	AIN
76	AIN7	dedicated	analog input	AIN
77	AIN9	dedicated	analog input	AIN
78	PSI1	dedicated	PSI channel	PSI
79	PSI3 *)	dedicated	PSI channel	PSI
80	PSI5 **)	dedicated	PSI channel	PSI
81	VSYNC	power	supply voltage for PSI sync pulse	PSI
82	PSI6 **)	dedicated	PSI channel	PSI
83	PSI4 *)	dedicated	PSI channel	PSI
84	PSI2	dedicated	PSI channel	PSI
85	SQREF	dedicated	squib reference resistor	FLM
86	AIN10	dedicated	analog input	AIN
87	AIN8	dedicated	analog input	AIN
88	AIN6	dedicated	analog input	AIN
89	AIN4	dedicated	analog input	AIN
90	AIN2	dedicated	analog input	AIN
91	AOUT	output	analog output multiplexer	System
92	DIS_ALP	bi-dir	disable all low side power stages	FLM
93	N_SYS_RES	input	system reset	System
94	DIS_SHP	input	disable special high side power stages	FLM
95	DIS_AHP	bi-dir	disable all high side power stages	FLM
96	GND_S2	ground	ground	-

\*) pin is not connected in CG902

\*\*) pin is not connected in CG903/CG902

Table: Pin description TQFP128epad package top side

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<b>pin</b>	<b>name</b>	<b>direction</b>	<b>description</b>	<b>module</b>
97	IGL14 **)	dedicated	low side power stage 14	FLM
98	IGH16 **)	dedicated	high side power stage 16	FLM
99	PGND7 **)	ground	power stage ground	FLM
100	VH8 **)	power	supply voltage high side power stage	FLM
101	IGL13 **)	dedicated	low side power stage 13	FLM
102	IGH15 **)	dedicated	high side power stage 15	FLM
103	IGL10 *)	dedicated	low side power stage 10	FLM
104	IGH12 *)	dedicated	high side power stage 12	FLM
105	PGND5 *)	ground	power stage ground	FLM
106	VH6 *)	power	supply voltage high side power stage	FLM
107	IGL9 *)	dedicated	low side power stage 9	FLM
108	IGH11 *)	dedicated	high side power stage 11	FLM
109	IGL6	dedicated	low side power stage 6	FLM
110	IGH8	dedicated	high side power stage 8	FLM
111	PGND3	ground	power stage ground	FLM
112	VH4	power	supply voltage high side power stage	FLM
113	IGL5	dedicated	low side power stage 5	FLM
114	IGH7	dedicated	high side power stage 7	FLM
115	IGL2	dedicated	low side power stage 2	FLM
116	IGH4	dedicated	high side power stage 4	FLM
117	PGND1	ground	power stage ground	FLM
118	VH2	power	supply voltage high side power stage	FLM
119	IGL1	dedicated	low side power stage 1	FLM
120	IGH3	dedicated	high side power stage 3	FLM
121	GND_A1	ground	ground	-
122	VST33	power	stabilized supply 3,3 V	POM
123	VST50	power	stabilized supply 5,0 V	POM
124	n.c.	open	not connected	-
125	L3H	power	coil 3 VCORE high side connection	POM
126	n.c.	open	not connected	-
127	VCORE1	power	core converter output	POM
128	VCORE2	power	core converter output	POM

\*) pin is not connected in CG902

\*\*) pin is not connected in CG903/CG902

Table: Pin description TQFP128epad package left side

## Application Note:

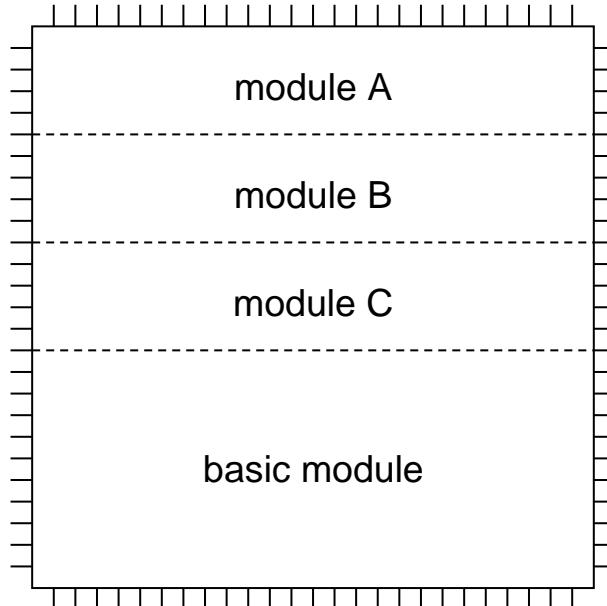
All not connected pins (n.c.) must be connected to ground or remain unconnected.

# Data sheet CG904, CG903, CG902

## 1.5 Family Concept

The ASICs CG904, CG903 and CG902 are pin compatible. The CG904 defines the superset for all ASICs. Pins not available for the ASICs CG903 or CG902 are left unconnected (n.c.). All pins are pin compatible including the channel numbers.

Each module consists of 4 firing loop channels and 2 external sensor interfaces (PSIx).



The difference between the 3 system ASICs are related to the amount of firing loops and PSI channels available:

system ASIC	firing loops	PSI channels
CG904	16	6
CG903	12	4
CG902	8	2

### Application Note:

All not connected pins (n.c.) must be connected to ground or remain unconnected except pins related to the family concept (VHx, IGHx, IGLx, PGNDx, PSIx).

## 2. Functional Description Power Module (POM)

The power module (POM) of the airbag system ASIC is designed to provide several basic supply functions.

First, the POM guarantees a constant supply of the energy reserve (VER) which is mainly used for airbag ignition. This is done with full current control in charge up mode as well as in charge maintenance mode. The autarky function known from former airbag systems is given by the feedback functionality of the VER charger. The condition of the energy reserve capacitor can be tested by SPI controlled build-in tests.

The second main feature is the general system supply of the ECU. Several low voltage regulators are available. Their output voltages are constantly monitored and connected to an internal reset generation, thus any critical voltage supply condition leads to a power-on reset and sets the microcontroller into a safe state.

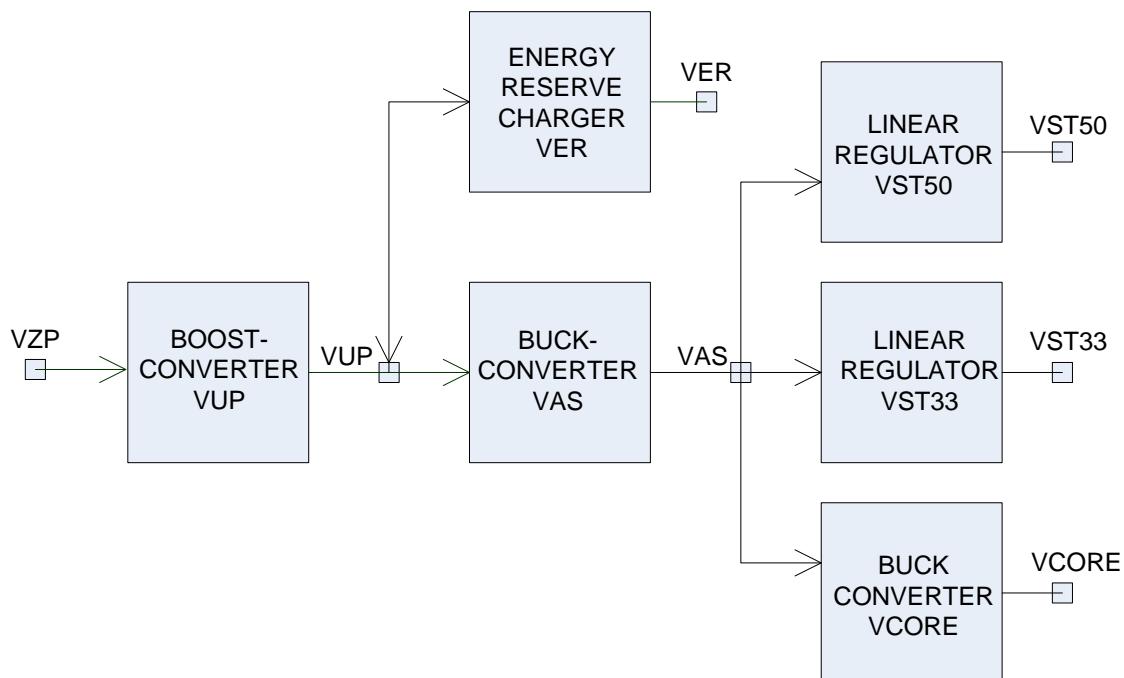
A more detailed list of features is given below.

### Features:

- Trimmed bandgap references for voltage regulation and voltage monitoring
- Trimmed internal reference current
- Trimmed internal oscillator with 1.875MHz
- VUP boost converter from VZP=5.2V...18V to VUP=33V/24V with 1.875MHz
- VER charger with programmable current levels
- VER test current functionality for capacitor tests
- SPI control of supply test functions, supply status, VUP programming (output voltage and current limitation)
- Monitoring of battery voltage by dedicated VBAT\_MON pins
- VAS buck converter VUP=10V...36V to VAS=6.7V with 1.875MHz
- VCORE buck converter VAS=6.7V to VCORE=3.3V/1.29V with 1.875MHz ( $\mu$ C supply)
- Programmable converter slope shaping and frequency jitter for improved EMC performance for all switching regulators
- VST50 linear regulator VAS to VST50=5V (CAN supply, ECU internal sensors)
- VST33 linear regulator VAS to VST33=3.3V (analog & digital supply)
- VCORE/VST33 configuration by dedicated CONF pins
- Voltage monitoring of low voltage pins and power-on reset logic
- Sleep mode control with  $I_{sleep} \leq 60\mu A$
- Overtemperature shut down of VUP converter
- VIO pin to externally connect a 3,3V supply to define internal logic levels.

# Data sheet CG904, CG903, CG902

## General Supply Structure:



The preceding picture shows the general supply concept.

It consists of six output voltages maximum, which are adjustable by configuration pins and SPI programming.

The energy from the battery is first transformed by a boost converter to the stabilized high voltage VUP. From this level the complete system is supplied by two branches.

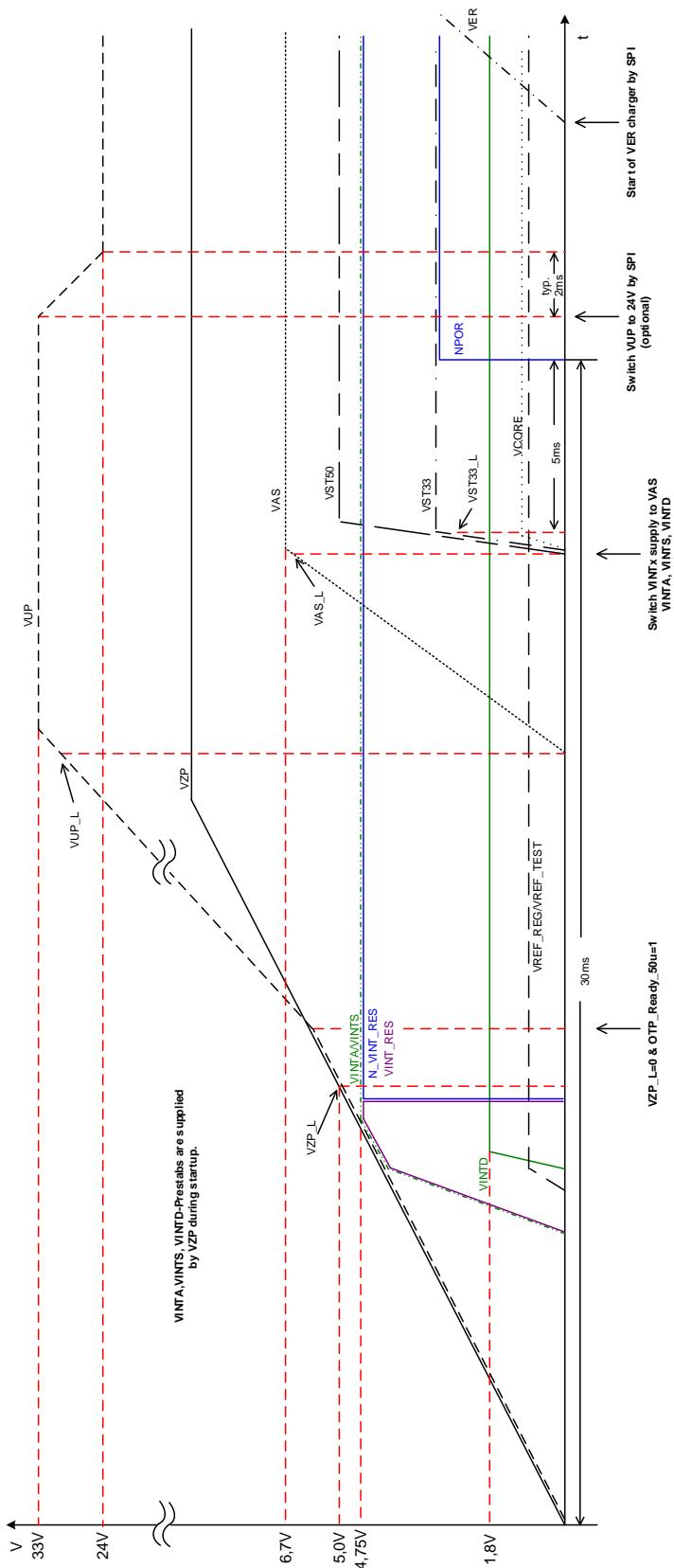
The high voltage branch is the energy reserve charger VER. The VER charge current is not set automatically and has to be programmed by SPI command after the reset release. Then the energy reserve capacitor is charged by this current and will provide the energy for the airbag ignition.

The main low voltage branch is a buck converter producing the output voltage VAS. This output supplies several regulators, the PSI interfaces and the AIN interfaces. The regulators VST50, VST33 and VCORE are connected in parallel. VST33 and VCORE can be switched off by the pins CONF\_33 and CONF\_CORE respectively.

When VZP is cut off (autarky mode) the supply of the complete system is guaranteed as long as the VER capacitor is charged. In this case the supply current is flowing backwards through the VER charger to VUP.

# Data sheet CG904, CG903, CG902

## Power On Diagram:

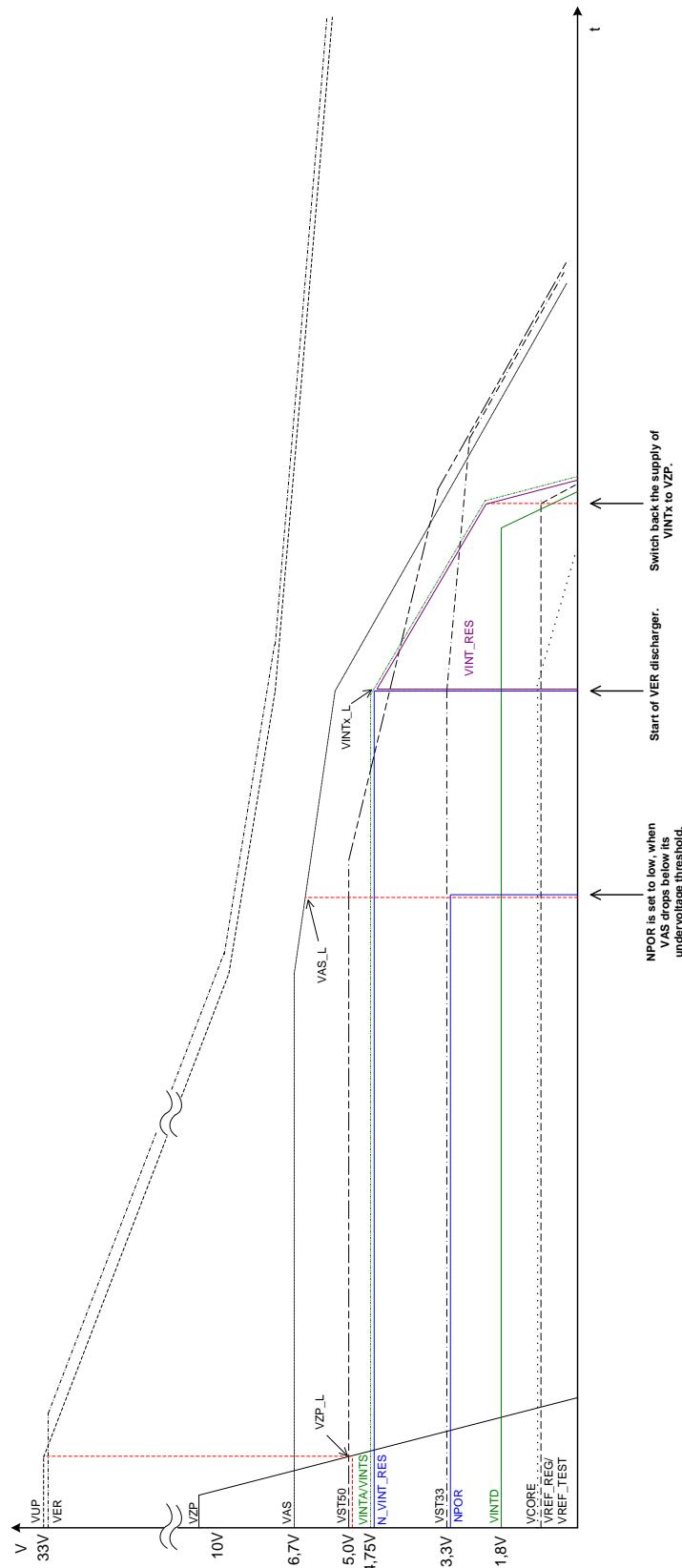


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# Data sheet CG904, CG903, CG902

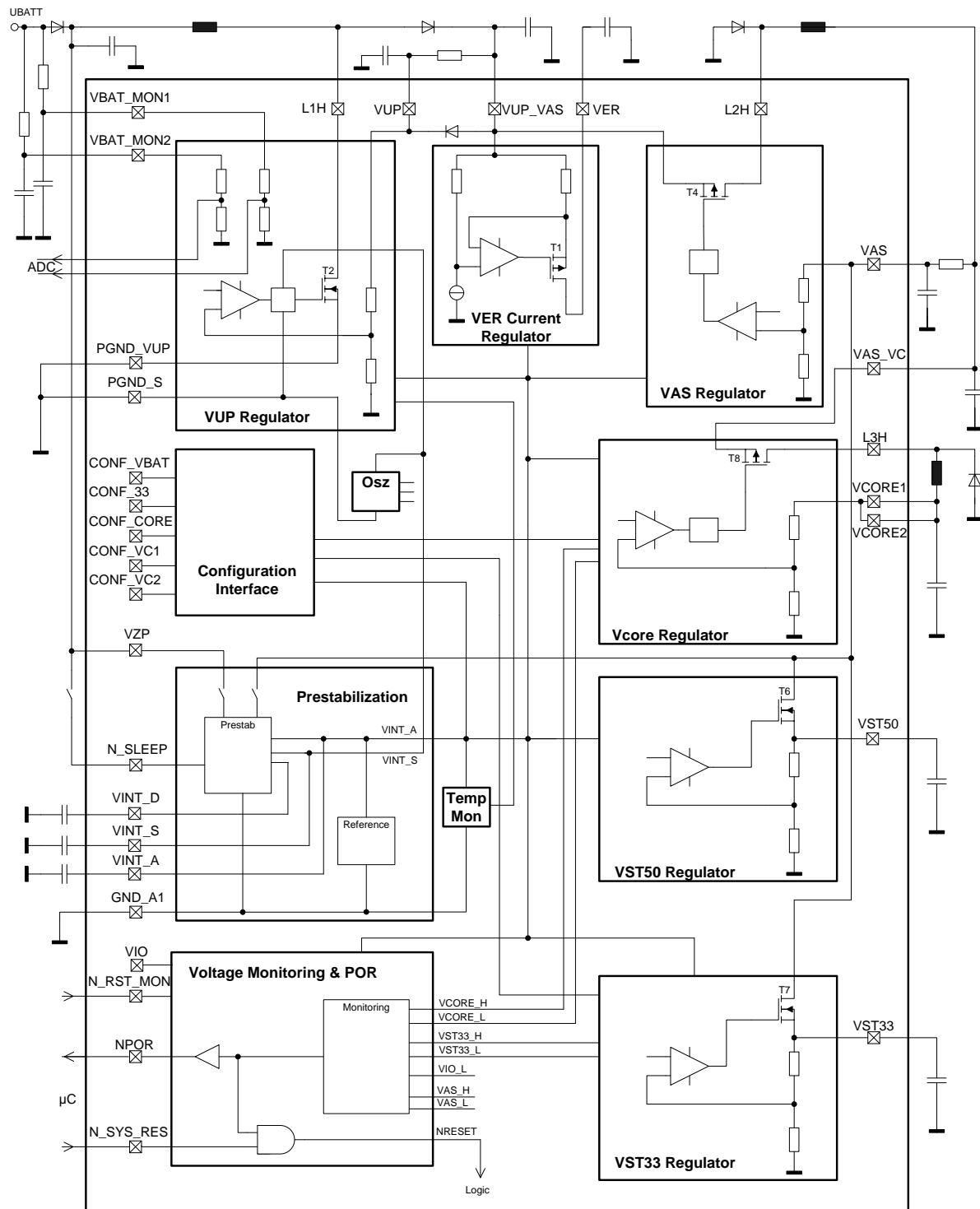
## Power Down Diagram:



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# Data sheet CG904, CG903, CG902

## POM Block Diagram:



The RC filters between VUP/VUP\_VAS and VAS/VAS\_VC are optional.

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# Data sheet CG904, CG903, CG902

## 2.1 Pre-stabilization, Bandgap, Current Reference & Oscillator

### 2.1.1 Pre-stabilization VINT\_A, VINT\_S, VINT\_D

The supply voltages VINT\_A, VINT\_S and VINT\_D are the internal low voltage supplies for every circuit of this ASIC. These regulators consist of an OTA, a powerstage and a feedback loop. At startup condition the VINT\_X are supplied by VZP via the p-channel transistors TP1 and TP2. When the VAS regulator has crossed its undervoltage threshold these transistors are switched off by the signal VAS\_L after a certain delay time. The VINT\_X voltages will now be supplied by the VAS regulator by closing the internal supply voltage switch TP3.

The switch-back process from VAS supply to VZP supply (e.g. in case of a short circuit at VAS or during power down) is triggered by an internal low voltage reset (VINT\_A\_RST) at VINT\_A at 2.5V. That means on the one hand that always a NPOR reset will occur during this process. On the other hand, the system has a very good robustness against short spikes or undervoltage situations at VAS.

The VINT\_X voltages are internally monitored for under- and overvoltage condition. A low active reset N\_VINT\_RST combines all under- and overvoltage comparators and keeps all circuits in a defined state.

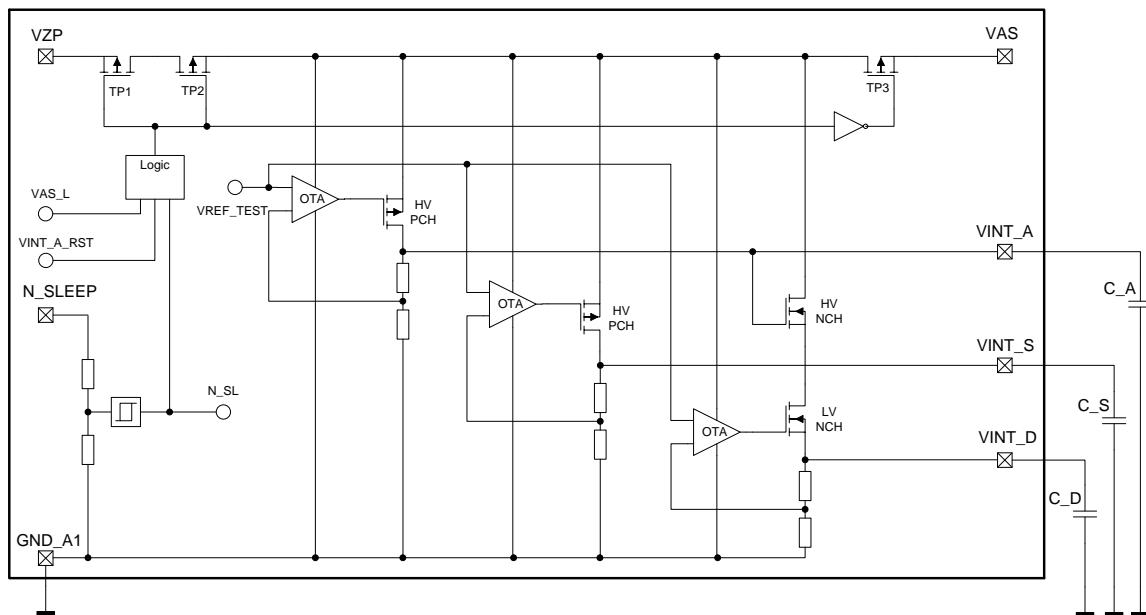
The VINT\_A voltage is used as supply for all analog circuits.

VINT\_S is a dedicated supply for the driver stage of the boost converter VUP and the oscillator because of the high current spikes engendered by these circuits.

The VINT\_D pin finally provides a supply voltage for the digital part of the ASIC.

The VINT\_X-regulators are used as ASIC internal supplies. It is not allowed to connect external loads to these pins. An external current at VINT\_X-pins will load the regulator voltages and may decrease them until the undervoltage monitoring circuit response leads to a reset condition.

The structure of the pre-stabilization is shown in the following picture:



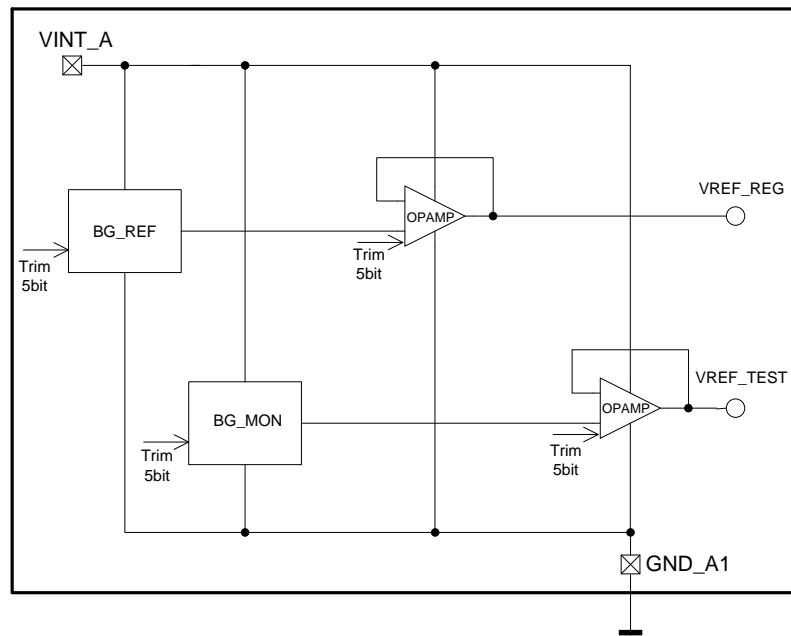
For further information concerning the sleep mode see chapter 2.11.

# Data sheet CG904, CG903, CG902

## 2.1.2 Voltage Reference: Bandgap

The voltage reference structure consists of two independent bandgaps and two impedance converters. Each bandgap and impedance converter is calibrated by 5bit to guarantee a high precision of the output voltage and a very low temperature coefficient.

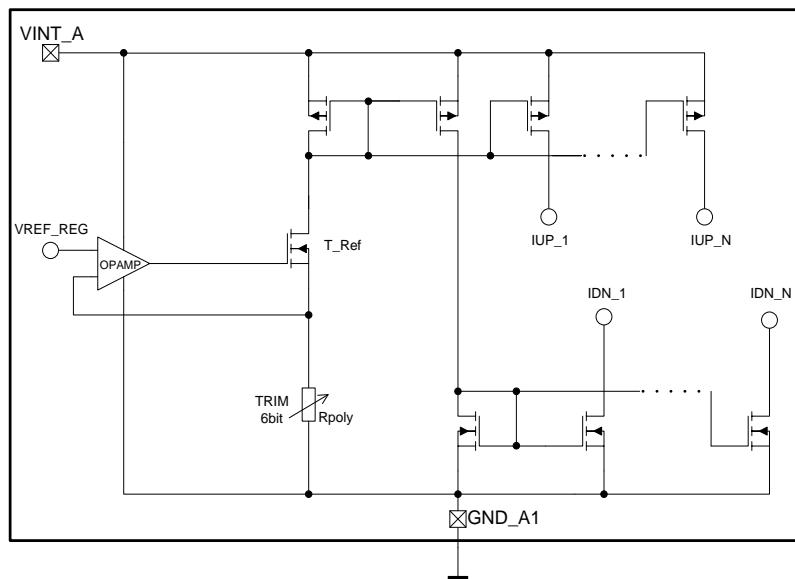
For system robustness two decoupled voltage references are implemented. The VREF\_REG voltage is used for the voltage regulation of VUP, VAS, VST50, VST33, VCORE and the reference current definition. The VREF\_TEST voltage is used for voltage monitoring functions at VZP, VUP, VER, VAS, VST50, VST33, VCORE, VINT\_X, VIO and voltage regulation at VINT\_X.



# Data sheet CG904, CG903, CG902

## 2.1.3 Current Reference IREF

The generation of the current reference is done internally. The high precision is reached by a 6-bit trimming and usage of different poly resistors. Therefore, an external reference resistor is no longer needed. The reference current is used in nearly every circuit, for example the basic clock frequency, the temperature monitoring, the LIN interface current, the VER charge current, AINx measurement current, the AI0x driver current, R-loop measurement and ignition current definition.



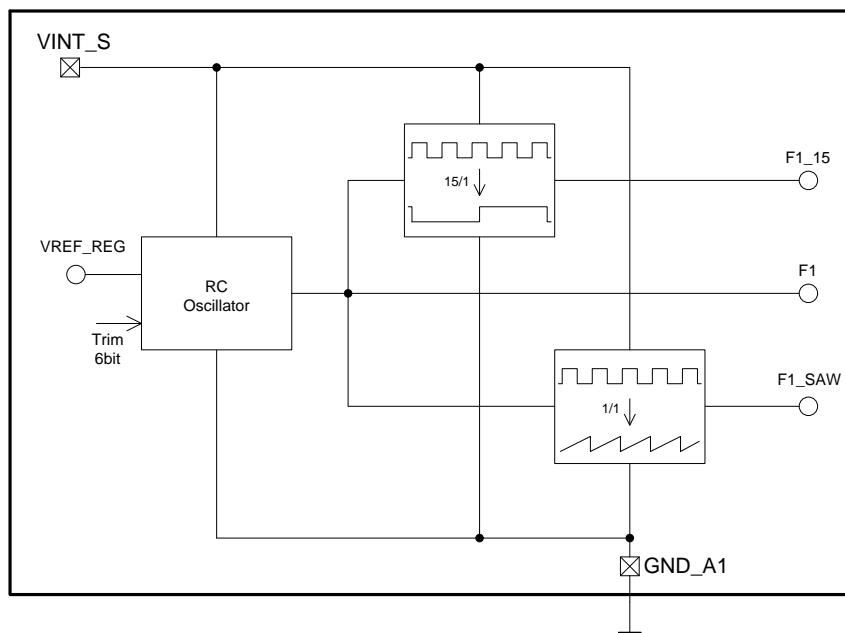
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## 2.1.4 Oscillator

The internal RC-oscillator uses poly-substrate capacitors and a 6bit trimmed reference current. It provides a main square wave clock signal F1 for the switching regulators, the watchdog functionality and the OTP circuit. Furthermore, there is another square wave signal F1\_15 which is used for digital time filter functions.

The third output of the oscillator block is the sawtooth signal F1\_SAW which is needed in the PWM generation for the buck converters.



# Data sheet CG904, CG903, CG902

## 2.1.5 Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.1-1	VINT_A	output voltage	VZP or VAS $\geq$ 5.2 V	-3%	4.75	+3%	V
2.1-2	VINT_S	output voltage	VZP or VAS $\geq$ 5.2 V	-3%	4.75	+3%	V
2.1-3	VINT_D	output voltage	VZP or VAS $\geq$ 5.2 V	-3%	1.8	+3%	V
2.1-4	VINT_A	input current	N_POR=High		34		mA
2.1-5	VINT_S	input current	N_POR=High		2.5		mA
2.1-6	VINT_D	input current	N_POR=High		1.5		mA
2.1-7	VZP	input current	power-on (including VINT_X current consumption)			50	mA
2.1-8	VZP	input current	typical supply (VINT_X supplied by VAS)			1	mA
2.1-9	internal	output voltage	bandgap VREF_REG, VINT_A>4V	-1%	1.25	+1%	V
2.1-10	internal	output voltage	monitor bandgap VREF_TEST, VINT_A>4V	-1%	1.25	+1%	V
2.1-11	internal	reference current	VINT_A in band	-3%	100	+3%	uA
2.1-12	VAS/VZP	filter time	switch-over VAS supply <-> VZP supply		10		us
2.1-13	internal	oscillator frequency F1	square wave	-5%	1875	+5%	kHz
2.1-14	internal	oscillator frequency F1_15	square wave	-5%	125	+5%	kHz
2.1-15	internal	oscillator frequency F1_SAW	sawtooth for L2H, L3H (VAS and VCORE regulator)	-5%	1875	+5%	kHz
2.1-16	internal	frequency jitter	jitter mode active			+/-9%	
2.1-17	internal	jitter period	jitter mode active		57		us

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
VINT_A	capacitance	ceramic capacitor C_A	75	220	385	nF
VINT_A	ESR	series resistance of C_A			100	mΩ
VINT_S	capacitance	ceramic capacitor C_S	75	100	275	nF
VINT_S	ESR	series resistance of C_S			100	mΩ
VINT_D	capacitance	ceramic capacitor C_D	75	100	125	nF
VINT_D	ESR	series resistance of C_D			100	mΩ

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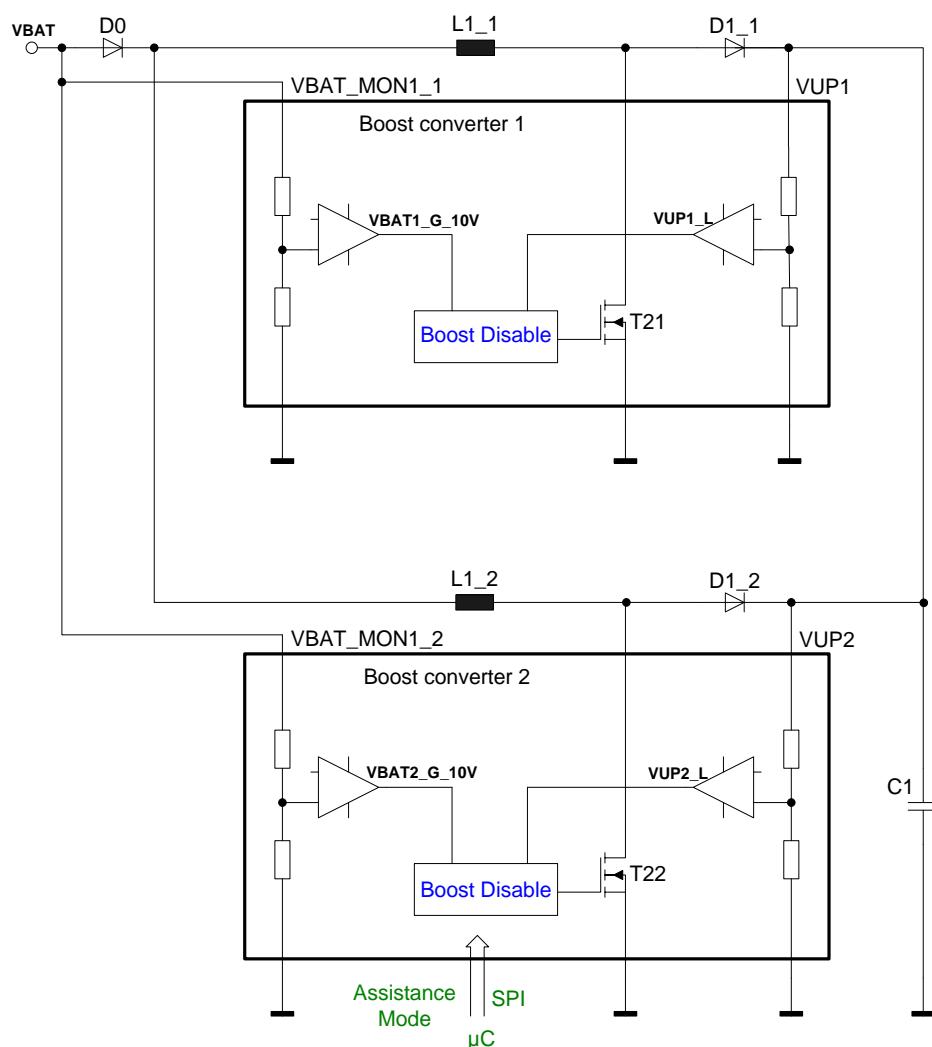
## 2.2 VBAT / VZP / VUP Monitoring

### 2.2.1 VBAT Monitoring and Assistance Mode

The ASIC provides two dedicated pins (VBAT\_MON1, VBAT\_MON2) for battery voltage monitoring. Both pins can be measured via the internal ADC by using the appropriate SPI command (see chapter 2.14).

Additionally, the pin VBAT\_MON1 controls the assistance mode feature. This mode offers a way to determine the power consumption in two- or more-ASIC systems with coupled boost converters. If one ASIC is programmed to be in assistance mode by SPI, then the boost converter of this ASIC is switched off when VUP > VUP\_L and VBAT > VBAT\_G\_10V (COMP1).

The following diagram explains the coupling of two boost converters and the internal assistance mode functionality.



# Data sheet CG904, CG903, CG902

## 2.2.2 VZP Monitoring

The monitoring functionality at VZP includes two comparator thresholds. The comparator COMP2 defines the VZP\_L\_5V threshold and determines the voltage level at which the boost converter starts switching. This means that below this level the VUP regulator remains disabled. This threshold can be set to two different values by the pin CONF\_VBAT to specify if the system is a 6V- or 7V-battery voltage system. The status of CONF\_VBAT will be read during start up and locked after the OTP read-out is done.

The status of COMP2 can be found in the POM\_STATUS register (see chapter 2.14).

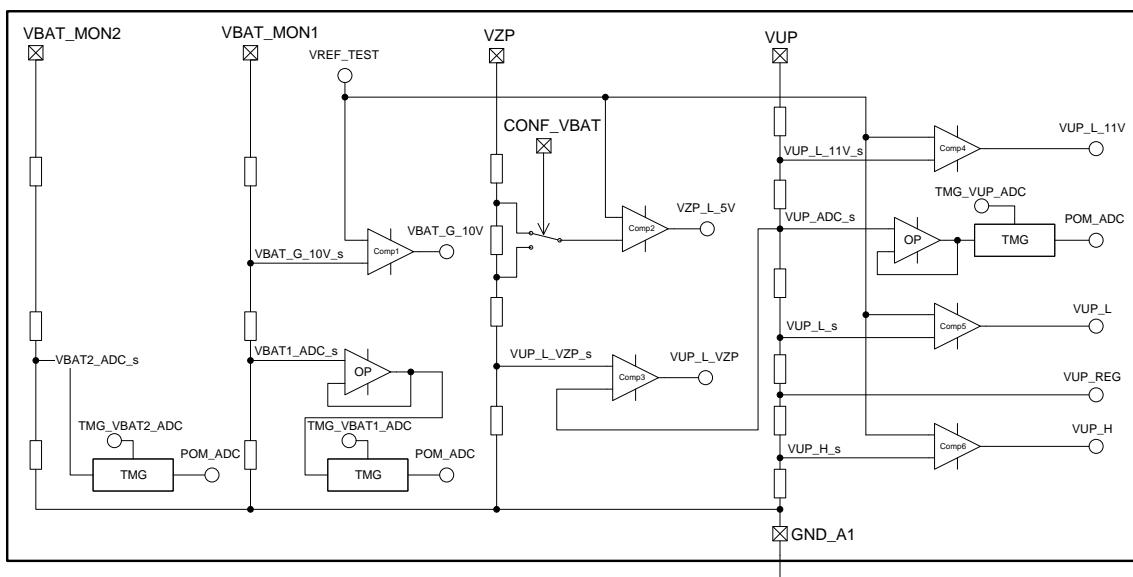
The second comparator at VZP (COMP3) compares the VZP voltage with the VUP voltage. This information is then used to switch off the VAS converter in sleep mode applications (see chapter 2.11).

## 2.2.3 VUP Monitoring

The voltage divider at VUP provides several comparator thresholds and the possibility for an ADC measurement of the VUP voltage. Furthermore, it is used in the feedback loop of the VUP regulation circuit.

COMP4 is needed for the synchronization of the PSI Interfaces and for reset suppression during power down (see chapter 2.9).

The over- and undervoltage comparators COMP5 and COMP6 influence the startup and the VER charger behavior and define the permissible VUP output voltage range.



# Data sheet CG904, CG903, CG902

## 2.2.4 Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.2-1	VBAT_MON1	threshold	COMP1: VBAT_G_10V	9.5	10	10.5	V
2.2-2	VBAT_MON1	divider factor	for ADC measurements at 5.3V<VBAT<36V	-3%	13.2	+3%	
2.2-3	VBAT_MON1	divider resistance		-30%	215	+30%	kΩ
2.2-4	VBAT_MON2	divider factor	for ADC measurements at 5.3V<VBAT<36V	-1.5%	13.2	+1.5%	
2.2-5	VBAT_MON2	divider resistance		-30%	200	+30%	kΩ
2.2-6	VZP	threshold	COMP2: VZP_L_5V, CONF_VBAT=1	4.85	5.0	5.25	V
2.2-7	VZP	threshold	COMP2: VZP_L_5V, CONF_VBAT=0	5.7	5.75	6.1	V
2.2-8	VZP	hysteresis		30		100	mV
2.2-9	VZP / VUP	threshold VUP-VZP	COMP3: VUP_L_VZP, VUP fall	2.5		4	V
2.2-10	VZP / VUP	threshold VUP-VZP	COMP3: VUP_L_VZP, VUP rise	4		5.5	V
2.2-11	VUP	threshold	COMP4: VUP_L_11V	11.5		12.5	V
2.2-12	VUP	threshold	COMP5: VUP_L in 33V mode	31		33	V
2.2-13	VUP	threshold	COMP5: VUP_L in 24V mode	22.25		23.75	V
2.2-14	VUP	filtertime	COMP5: VUP_LF, L->H transition	5		15	us
2.2-15	VUP	threshold	COMP6: VUP_H in 33V mode	33		35	V
2.2-16	VUP	threshold	COMP6: VUP_H in 24V mode	23.75	24.5	25.25	V
2.2-17	VUP	filtertime	COMP6_VUP_HF, L->H transition	5		20	us
2.2-18	VUP	divider factor	for ADC measurement at 5.3V<VUP<36V	-3%	13.2	+3%	
2.2-19	CONF_VBAT	pull up current	V_CONF_VBAT < 2V at OTP_READY=L	100			uA
2.2-20	CONF_VBAT	pull up current	V_CONF_VBAT < 2V at OTP_READY=H	20			uA

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
VBAT_MONx	ext. capacitance	RC network for robustness against negative voltage spikes		100		nF
VBAT_MONx	ext. resistance	RC network for robustness against negative voltage spikes		10		kΩ
VBAT_MON1	ADC Offset	VBAT=0V		20		LSB
VBAT_MON2	ADC Offset	VBAT=0V		2		LSB

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## 2.3 DC/DC Boost Converter VUP

The boost converter VUP is used to provide a 33V/24V voltage level to charge up the energy reserve capacitor at VER and to supply the buck converter VAS. The input voltage of the boost converter is VZP which is the polarity protected (D0) battery voltage. The stability of this converter is assured by a Type-II-compensation with internal compensation network and current mode control. The switching frequency is defined by the internal clock signal F1.

At startup condition the output capacitor C1 is directly precharged by an inrush current coming from UBAT. After the OTP has been read out the lowside transistor T2 starts switching and C1 is charged to the standard voltage level of 33V.

The charging of the VUP capacitor C1 up to higher values is guaranteed by the current limitation of T2, which means that - when T2 is switched on - the current in L1 is increasing until T2 is switched off by the current limitation. The current is then freewheeling via D1 and charging the capacitor at VUP. After a defined period of time, based on the internal oscillator clock, the transistor T2 is switched on again and the current in L1 starts to increase again.

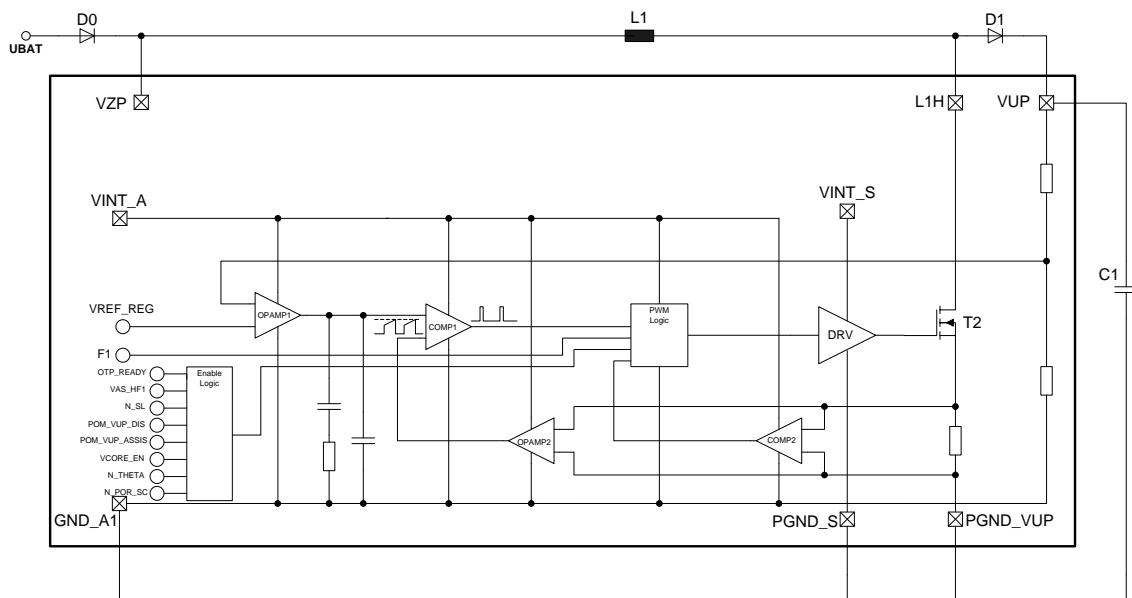
When the goal value at VUP is reached, the voltage will be regulated by a pulse width modulation (PWM). The output of the regulation OPAMP1 is compared with the output of the current mode OPAMP2 which provides the voltage equivalent of the current in the powerstage T2. The comparator COMP1 then generates the PWM signal.

To make sure that T2 is always switching after a defined time, the PWM signal is limited to typically 10%.

The goal value of the VUP output can be set down to 24V by SPI command after reset release. The current limitation at T2 has two different levels and can also be set to a lower level by SPI command.

The low level of the current limitation fulfills the requirement for a reduced charge up current and can be used with 1A freewheeling diodes. The high level of the current limitation should only be used for high end airbag systems with very high current consumptions.

To switch off the boost converter there are a couple of internal signals which are depicted in the following schematic. These signals are OTP\_READY (read out of OTP is finished), VAS\_HF1 (time filtered overvoltage at VAS), N\_SL (sleep mode is activated), POM\_VUP\_DIS (autarky test is activated), POM\_VUP\_ASSIS (assistance mode is activated), VCORE\_EN (invalid configuration at CONF\_VC1/2 pins), N\_THETA (overtemperature situation) and N\_POR\_SC (N\_POR shorted externally to high and internally driven to low).



# Data sheet CG904, CG903, CG902

## 2.3.1 VUP Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.3-1	VUP	output voltage	24V mode, 18V $\geq$ VZP $\geq$ 5.2V	23.0	23.75	24.75	V
2.3-2	VUP	output voltage	33V mode, 18V $\geq$ VZP $\geq$ 5.2V	32	33	34	V
2.3-3	VUP	output current	24V mode, 18V $\geq$ VZP $\geq$ 5.2V			220	mA
2.3-4	VUP	output current	33V mode, 18V $\geq$ VZP $\geq$ 5.2V			170	mA
2.3-5	internal	current limitation	T2, low level	1.2		1.8	A
2.3-6	internal	current limitation	T2, high level	1.75		2.75	A
2.3-7	internal	RDSon	T2 (excluding bond resistance)			0.6	$\Omega$
			T2 (including bond resistance)			0.7	$\Omega$
2.3-8	L1H	duty cycle limit	undervoltage VUP	4		14	%
2.3-9	L1H	frequency	converter switching frequency	-5%	1875	+5%	kHz

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
L1H	inductance L1	option 1	-40%	22	+40%	$\mu$ H
L1H	ind. L1 resistance	option 1			0.28	$\Omega$
VUP, PGND_VUP	capacitance	ceramic capacitor for option 1 capacitance for VUP>20V incl. voltage derating	9			$\mu$ F
VUP	capacitor ESR	ceramic capacitor for option 1 at 1 MHz			20	$m\Omega$
L1H	inductance L1	option 2	-40%	10	+40%	$\mu$ H
L1H	ind. L1 resistance	option 2			0.28	$\Omega$
VUP, PGND_VUP	capacitance	ceramic capacitor for option 2 capacitance for VUP>20V incl. voltage derating	6			$\mu$ F
VUP	capacitor ESR	ceramic capacitor for option 2 at 1 MHz			20	$m\Omega$
L1H, VUP	freewheeling diode D1	Schottky diode		0.3		V
VUP, L1H	efficiency	VZP=5.2V, IER<170mA, 33V mode, slope shaping off	60			%
VUP, L1H	efficiency	VZP=14V, IER<170mA, 33V mode, slope shaping off	85			%
VUP, L1H	efficiency	VZP=14V, IER<170mA, 33V mode, slope shaping on	80			%
VUP, L1H	efficiency	VZP=5.2V, IER<220mA, 24V mode, slope shaping off	65			%
VUP, L1H	efficiency	VZP=14V, IER<220mA, 24V mode, slope shaping off	86			%
VUP, L1H	efficiency	VZP=14V, IER<220mA, 24V mode, slope shaping on	81			%

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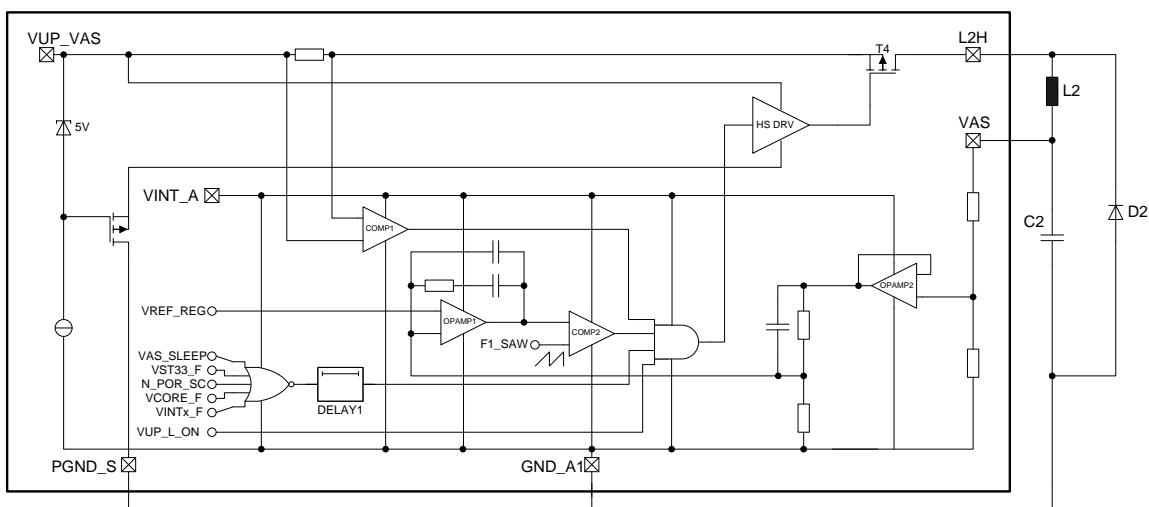
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## 2.4 DC/DC Buck Converter VAS

The buck converter is designed to generate the main analog supply. VAS is used as input voltage for the linear regulator VST50, VST33, the buck converter VCORE, the analog input pins AINx and the PSI interface.

The VAS regulator is supplied by the pin VUP\_VAS which offers the possibility to connect an external EMC network at the input of this converter.

The highlights of this buck converter are Type-III-compensation with internal compensation network and voltage mode control, a very high switching frequency (internal clock signal F1) and the usage of a p-channel powerstage to avoid any bootstrap functionality. Additionally, the buck converter is short circuit protected to ground by current limitation.



The buck converter starts switching when VUP has crossed its undervoltage threshold VUP\_L and triggered the startup-FF which sets the signal VUP\_L\_ON. Until the output voltage has reached the nominal value the current limitation controls the switching behavior of the regulator by switch off T4 through COMP1 and releases it after a defined period of time.

Once the output capacitor is charged to this value, the down-converting is based on a pulse width modulation (PWM) of T4 and external freewheeling via the diode D2.

The definition of the PWM signal is done by the regulator amplifier (OPAMP1) using the reference voltage VREF\_REG and the VAS feedback. To be able to use low voltage elements for the compensation network, the feedback divider was split in two parts and separated by an impedance converter (OPAMP2). The output of OPAMP1 is compared (COMP2) with the sawtooth signal F1\_SAW. The generated PWM signal is then transformed to a high voltage level and triggers the highside driver stage.

The input signals VST33\_F, VCORE\_F and VINT\_X\_F are used to switch off the buck converter in case of overvoltage at the respective output voltages (see chapter 2.8). Additionally the VAS converter will be switched off by NPOR\_SC, when the pin N\_POR is externally shorted to high and internally driven to low (see chapter 2.9).

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During sleep mode the VAS regulator must be switched off because its input voltage VUP\_VAS is constantly supplied via the external components L1 and D1 of the boost converter. This is done with the VAS\_SLEEP signal which is set by a combination of the VUP\_L\_VZP comparator output and the N\_SL signal. For more details see chapter 2.1.1 and 2.11.

The stability of the regulator circuit depends on the external components (inductor, capacitor and its ESR), for which reason the external components must be chosen as described in the electrical characteristics.

## 2.4.1 VAS Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.4-1	VAS	output voltage	VUP_VAS>8.5V (guaranteed by design); VUP_VAS>10V (tested in series production)	6.5	6.7	6.9	V
2.4-2	VAS	output current	including current at VINT_X, min. current is given by internal load	10		700	mA
2.4-3	internal	current limitation	T4	1.0		1.8	A
2.4-4	VAS	load response	I_VAS: 200mA -> 300mA, 300mA -> 200mA (not tested in series production)	-100		100	mV
2.4-5	VAS	line response	dVUP/dt: +/- 15V/50us	-250		250	mV
2.4-6	VUP_VAS, L2H	RDSon	T4 (excluding bond resistance)			2.0	$\Omega$
			T4 (including bond resistance)			2.2	$\Omega$
2.4-7	L2H	frequency	converter switching frequency	-5%	1875	+5%	kHz
2.4-8	VAS	input current	internal VAS current including internal VINT_X current consumption		40	50	mA
2.4-9	VAS	filtertime	DELAY1: overvoltage condition at VST33, VST50, VCORE, VINT_X or request for sleep mode (VAS_SLEEP)	50	75	100	us

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
VAS, L2H	inductance L2	all systems	-40%	22	+40%	$\mu$ H
VAS, L2H	ind. L2 resistance	all systems			0.28	$\Omega$
L2H, GND	freewheeling diode D2	Schottky diode		0.3		V
VAS, GND	capacitance	ceramic capacitor	12	20		$\mu$ F
VAS; GND	capacitor ESR	ceramic capacitor, 1 MHz			20	$m\Omega$
VAS	ripple voltage				20	mV
VAS	efficiency	VUP=33V, I_VAS=300mA, slope shaping off	75			%
VAS	efficiency	VUP=33V, I_VAS=300mA, slope shaping on	70			%
VAS	efficiency	VUP=24V, I_VAS=300mA, slope shaping off	77			%
VAS	efficiency	VUP=24V, I_VAS=300mA, slope shaping on	72			%

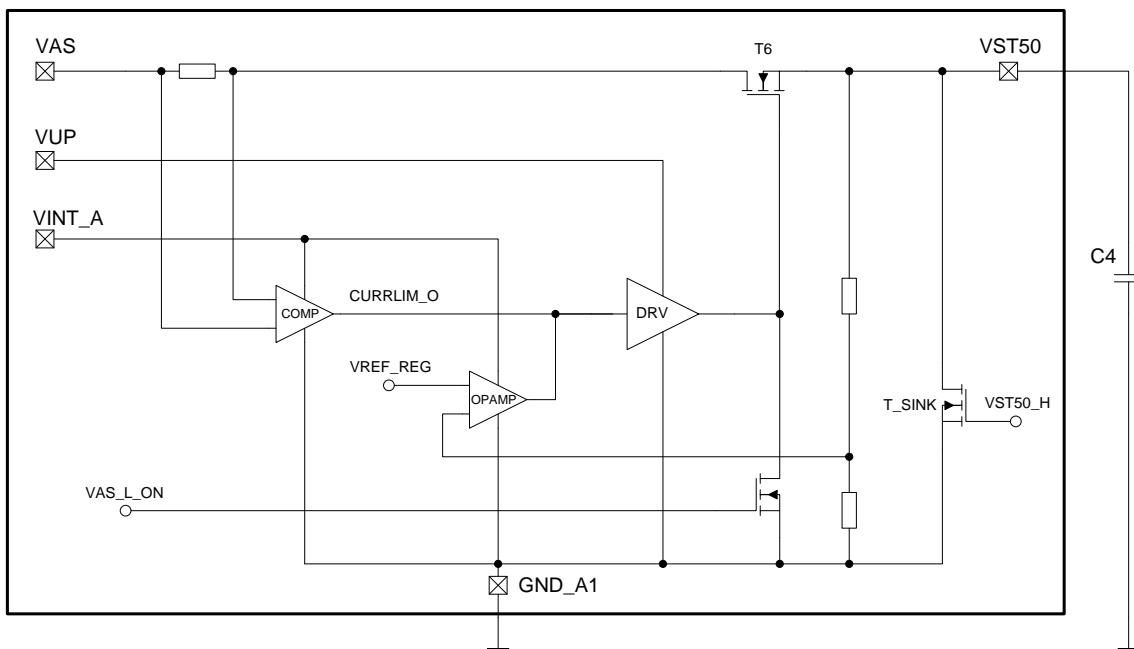
## 2.5 Linear Regulator VST50

The VST50 voltage supply is guaranteed by a linear regulation. Its input voltage is VAS, the output voltage is VST50. The regulator is controlled by the VAS voltage comparator (see chapter 2.8) and is switched on by the signal VAS\_L\_ON. If VINT\_RST becomes high during operation (VINT\_X out of band, filtered), the regulator is deactivated. For a good startup behavior and for short circuit protection this voltage regulator is equipped with a current limitation.

The driver circuit of the n-channel DMOS regulation transistor T6 is supplied by VUP voltage to guarantee a low drop voltage even for low VAS voltages (e.g. 5.5V). The regulator is designed for ceramic output capacitors and works without any external series resistor.

In combination with the given startup behavior of VUP and VAS the overshoot of this regulator is very small and therefore produces no stress for other connected circuits.

The VST50 voltage supply is internally used to generate the quiescent voltage levels at the IGHx/IGLx pins. Due to this fact a current feedback during ignition is possible which can increase the output voltage of VST50. To limit the voltage in this case a current sink (T\_SINK) is implemented which is activated by the VST50 overvoltage signal.



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## 2.5.1 VST50 Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.5-1	VST50	output voltage	VUP $\geq$ 10V, VAS $\geq$ 5.5 V	4.9	5.0	5.1	V
2.5-2	VST50	output current	min. current is given by internal load	10		90	mA
2.5-3	VST50	current limitation		95		130	mA
2.5-4	VST50	RDSon				4	$\Omega$
2.5-5	VST50	load response	I_VST50: 20mA $\rightarrow$ 70mA, 70mA $\rightarrow$ 20mA	-80		80	mV
2.5-6	VST50	line response	dVAS/dt $\leq$ +/- 50V/ms	-60		60	mV
2.5-7	VST50	power-on overshoot	VAS: 0V $\rightarrow$ 7V, dVAS/dt $\leq$ 25V/ms	0		60	mV
2.5-8	VST50	current sink	T_SINK triggered by VST50_H	50		140	mA

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
VST50	capacitance	ceramic cap (2.2uF, 4.4uF)	1.3		7.5	$\mu$ F
VST50	ESR	ceramic cap (2.2uF, 4.4uF)			20	$m\Omega$
VST50	ESL	ceramic cap (2.2uF, 4.4uF)	1		2	nH
VST50	additional cap	decoupled with R $\geq$ 0.1 $\Omega$	0		12	$\mu$ F

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## 2.6 Linear Regulator VST33

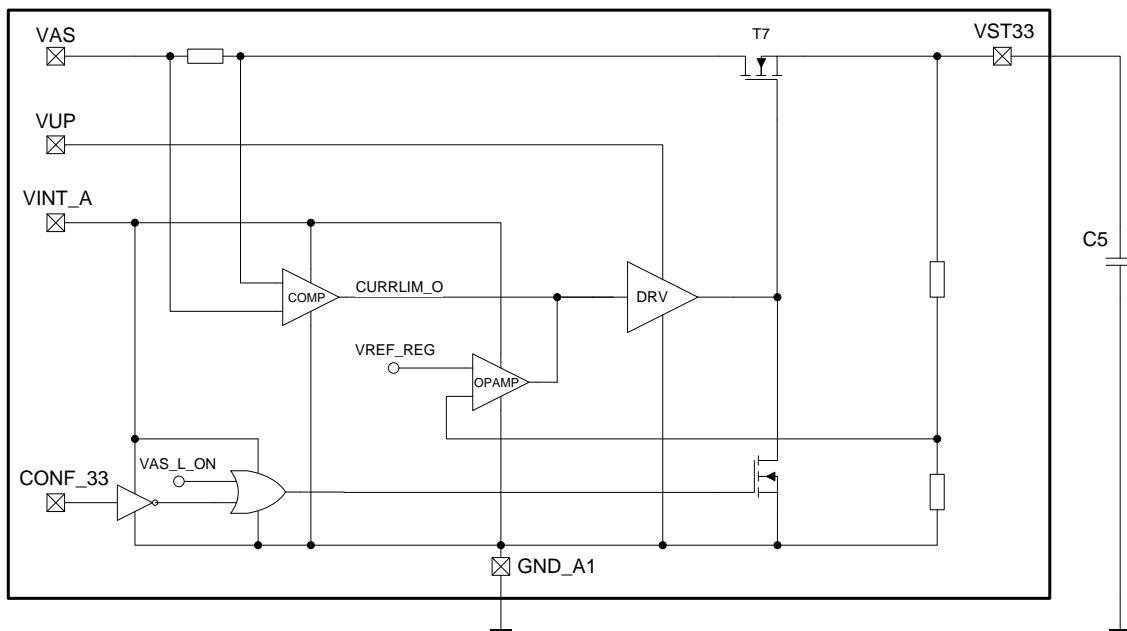
The VST33 voltage supply is guaranteed by a linear regulation. Its input voltage is VAS, the output voltage is VST33. The regulator is controlled by the VAS voltage comparator (see chapter 2.8) and is switched on by the signal VAS\_L\_ON. If VINT\_RST becomes high during operation (VINT\_X out of band, filtered), the regulator is deactivated. For a good startup behavior and for short circuit protection this voltage regulator is equipped with a current limitation.

The driver circuit of the n-channel DMOS regulation transistor T7 is supplied by VUP voltage to guarantee a low drop voltage even for low VAS voltages (e.g. 5.5V).

The regulator is designed for ceramic output capacitors and works without any external series resistor.

In combination with the given startup behavior of VUP and VAS the overshoot of this regulator is very small and produces therefore no stress for other connected circuits, especially the microcontroller.

If not needed the VST33 regulator can be deactivated by the pin CONF\_33 to save the capacitor C5. The status of this pin will be read during start up and locked after the OTP read-out is done.



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## 2.6.1 VST33 Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.6-1	VST33	output voltage	VUP $\geq$ 10V, VAS $\geq$ 4.5 V	3.234	3.3	3.366	V
2.6-2	VST33	output current		10		150	mA
2.6-3	VST33	current limitation		155		250	mA
2.6-4	VST33	RDSon				1.5	$\Omega$
2.6-5	VST33	load response	I_VST33: 50mA -> 100mA, 100mA -> 50mA	-60		80	mV
2.6-6	VST33	line response	dVAS/dt $\leq$ 50V/ms	-60		60	mV
2.6-7	VST33	power-on overshoot	VAS: 0V -> 7V, dVAS/dt $\leq$ 25V/ms	0		60	mV
2.6-8	VIO	$I_{VIO}$	VIO current consumption			5	mA
2.6-9	CONF_33	pull up current	V_CONF_33 < 2V at OTP_READY=L	100			uA
2.6-10	CONF_33	pull up current	V_CONF_33 < 2V at OTP_READY=H	20			uA

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
VST33	capacitance	ceramic cap (2.2uF, 4.4uF)	1.3		7.5	$\mu$ F
VST33	ESR	ceramic cap (2.2uF, 4.4uF)			20	$m\Omega$
VST33	ESL	ceramic cap (2.2uF, 4.4uF)	1		2	nH
VST33	additional cap	decoupled with R $\geq$ 0.1 $\Omega$	0		12	$\mu$ F

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## 2.7 DC/DC Buck Converter VCORE

The buck converter VCORE is a dedicated supply for microcontrollers. It can be enabled by the configuration pin CONF\_CORE and its output voltage is selectable by the pins CONF\_VC1/2:

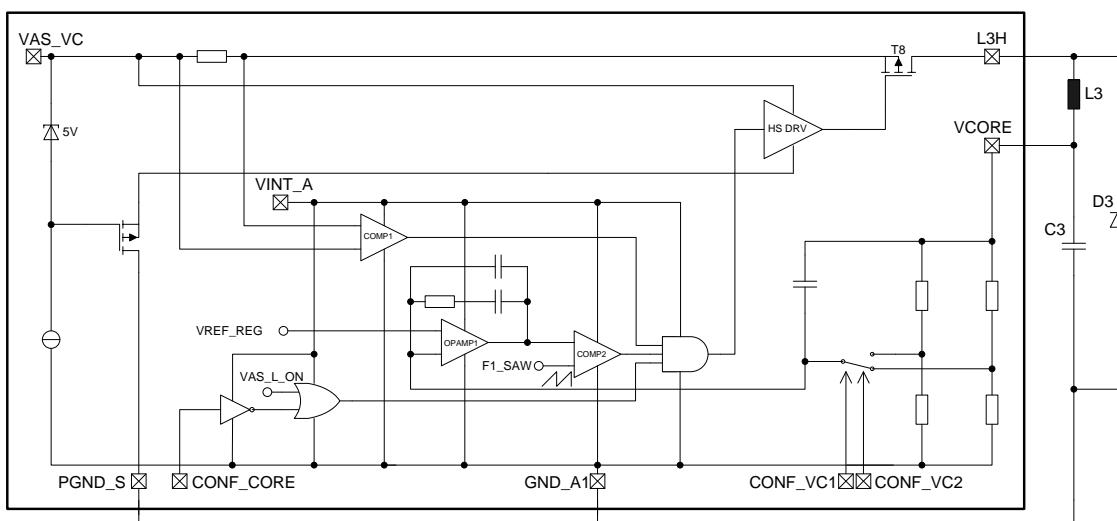
CONF_VC1	CONF_VC2	VCORE
0	1	1.29V
1	0	3.3V

The status of these pins will be read during start up and locked after the OTP read-out is done. The other combinations are not allowed and will disable the VUP converter - and thus the system start up - if applied. If VINT\_RST becomes high during operation (VINT\_X out of band, filtered), the regulator is deactivated.

The VCORE regulator is supplied by the pin VAS\_VC which offers the possibility to connect an external EMC network at the input of this converter.

The highlights of this buck converter are Type-III-compensation with internal compensation network and voltage mode control, a very high switching frequency (internal clock signal F1) and the usage of a p-channel powerstage to avoid any bootstrap functionality. Additionally, the buck converter is short circuit protected to ground by current limitation.

The general structure and functionality of the buck converter is comparable to the VAS converter.



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## 2.7.1 VCORE Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.7-1	VCORE	output voltage	3.3V mode, VAS $\geq$ 6.2 V	3.234	3.3	3.366	V
2.7-2	VCORE	output voltage	1.29V mode, VAS $\geq$ 4.5 V	1.24	1.29	1.34	V
2.7-3	VCORE	output current	static output current			600	mA
2.7-4	internal	current limitation	T8	0.805		1.6	A
2.7-5	VCORE	load response	I_VAS: 200mA $\rightarrow$ 300mA, 300mA $\rightarrow$ 200mA (not tested in series production)	-25		25	mV
2.7-6	VCORE	line response	dVAS/dt: +/- 50V/ms (not tested in series production)	-50		50	mV
2.7-7	VAS_VC, L3H	RDSon	T8 (excluding bond resistance)			3.6	$\Omega$
			T8 (including bond resistance)			3.8	$\Omega$
2.7-8	L3H	frequency	converter switching frequency	-5%	1875	+5%	kHz
2.7-9	VCORE	input current	internal VCORE current in 1.29V mode			5	mA
2.7-10	VCORE	input current	internal VCORE current in 3.3V mode			8	mA
2.7-11	CONF_CORE, CONF_VC1, CONF_VC2	pull up current	V_CONF_XX < 2V at OTP_READY=L	100			uA
2.7-12	CONF_CORE, CONF_VC1, CONF_VC2	pull up current	V_CONF_XX < 2V at OTP_READY=H	20			uA

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
VCORE, L3H	inductance L3	all systems	-40%	22	+40%	$\mu$ H
VCORE, L3H	ind. L3 resistance	all systems			0.28	$\Omega$
L3H, GND	freewheeling diode D3	Schottky diode		0.3		V
VCORE, GND	capacitance	ceramic capacitor	12	20		$\mu$ F
VCORE, GND	capacitor ESR	ceramic capacitor, 1 MHz			20	$m\Omega$
VCORE	ripple voltage				20	mV
VCORE	efficiency	VAS=6.7V, I_VCORE=300mA, 1.29V mode slope shaping off	55			%
VCORE	efficiency	VAS=6.7V, I_VCORE=300mA, 1.29V mode slope shaping on	52			%
VCORE	efficiency	VAS=6.7V, I_VCORE=300mA, 3.3V mode slope shaping off	65			%
VCORE	efficiency	VAS=6.7V, I_VCORE=300mA, 3.3V mode slope shaping on	62			%

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## 2.8 Voltage Monitoring

In this paragraph the monitoring functionality of the low voltage supplies is described. This monitoring is done for a safe reset generation and a good startup behavior.

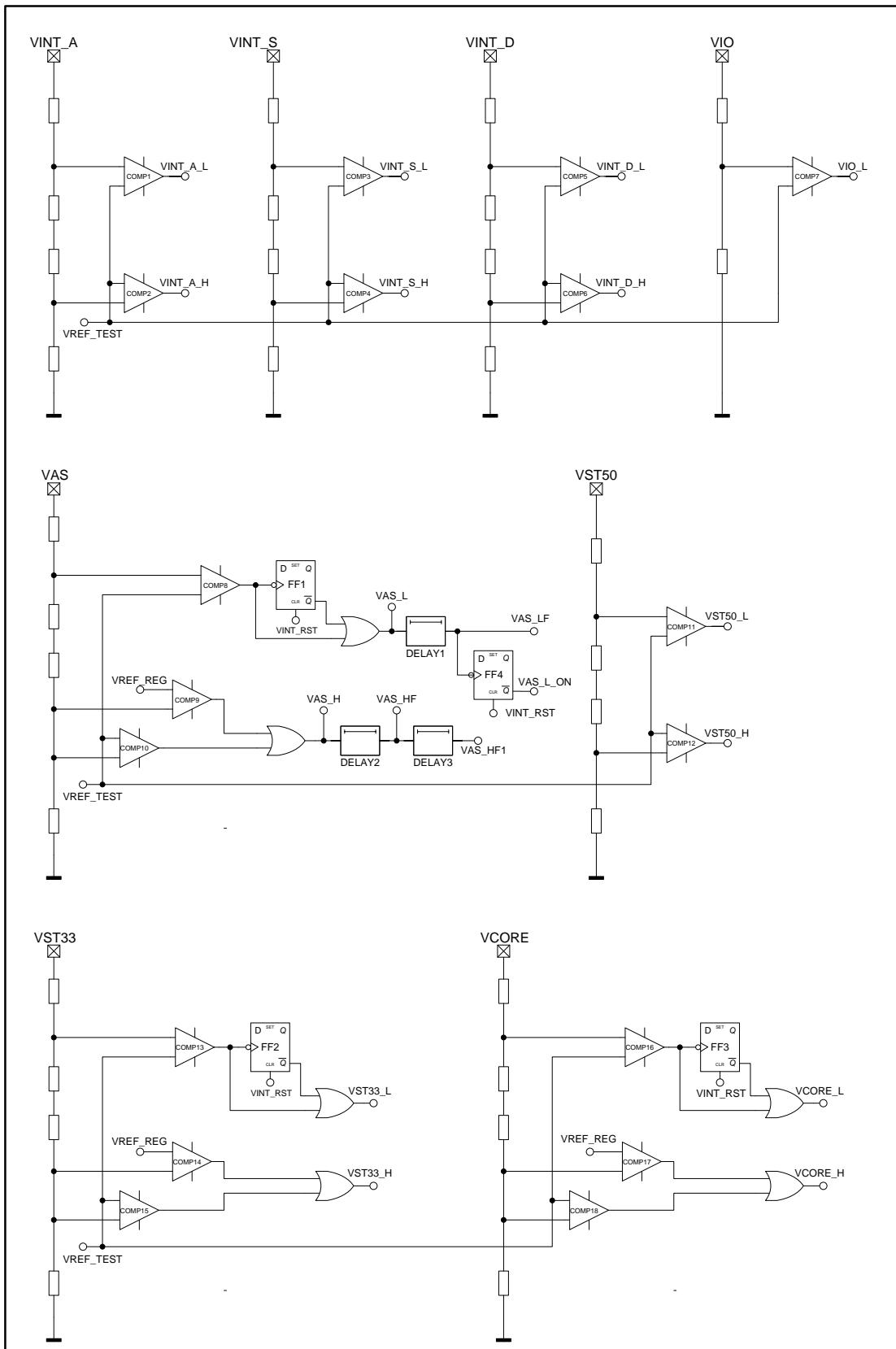
VAS, VST33, VCORE and VIO have an influence on the NPOR reset (see chapter 2.9). The status of VST50 can be found in the POM\_STATUS register and has no influence on the NPOR. The voltage at VAS also defines the time when VST50, VST33 and VCORE will be enabled. This is done by FF4 which sets the signal VAS\_L\_ON to high when the VAS\_L threshold is crossed. FF4 will be reset by the internal reset signal VINT\_RST. This leads to a large hysteresis to avoid any unwanted shut downs of the VSTxx/VCORE regulators and to guarantee a proper voltage ramp down when the ECU is switched off.

For VAS, VST33 and VCORE some extra features are implemented to assure the correct functionality of the voltage band monitoring. The undervoltage comparators are followed by extra flipflops (FF1-3) which detect that the comparators change their state from high to low during every start up.

The overvoltage comparators are not triggered under normal operation conditions. To be sure that they will work correctly in a failure situation they are implemented in a redundant way.

The details of all voltage thresholds can be found in the following picture and the electrical characteristics at the end of this section.

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## 2.8.1 Voltage Monitoring Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.8-1	VINT_A	threshold	COMP1: VINT_A_L undervoltage comparator	4.5		4.75	V
2.8-2	VINT_A	threshold	COMP2: VINT_A_H overvoltage comparator	4.75		5.0	V
2.8-3	VINT_S	threshold	COMP3: VINT_S_L undervoltage comparator	4.5		4.75	V
2.8-4	VINT_S	threshold	COMP4: VINT_S_H overvoltage comparator	4.75		5.0	V
2.8-5	VINT_D	threshold	COMP5: VINT_D_L undervoltage comparator	1.60		1.8	V
2.8-6	VINT_D	threshold	COMP6: VINT_D_H overvoltage comparator	1.8		1.95	V
2.8-7	VIO	threshold	COMP7: VIO_L undervoltage comparator	3.0		3.2	V
2.8-8	VAS	threshold	COMP8: VAS_L undervoltage comparator	6.3		6.7	V
2.8-9	VAS	filtertime	DELAY1: VAS_L -> VAS_LF only rising edge	115		150	us
2.8-10	VAS	threshold	COMP9: VAS_H redundant overvoltage comparator	6.7		7.11	V
2.8-11	VAS	threshold	COMP10: VAS_H overvoltage comparator	6.7		7.11	V
2.8-12	VAS	filtertime	DELAY2: VAS_H -> VAS_HF only rising edge	230		280	us
2.8-13	VAS	filtertime	DELAY3: VAS_HF -> VAS_HF1 rising and falling edge	50		100	us
2.8-14	VST50	threshold	COMP11: VST50_L undervoltage comparator	4.75		5.0	V
2.8-15	VST50	threshold	COMP12: VST50_H overvoltage comparator	5.0		5.25	V
2.8-16	VST33	threshold	COMP13: VST33_L undervoltage comparator	3.13		3.3	V
2.8-17	VST33	threshold	COMP14: VST33_H redundant overvoltage comparator	3.3		3.47	V
2.8-18	VST33	threshold	COMP15: VST33_H overvoltage comparator	3.3		3.47	V
2.8-19	VCORE 3.3V	threshold	COMP16: VCORE_L undervoltage comparator in 3.3V mode	3.13		3.3	V
2.8-20	VCORE 3.3V	threshold	COMP17: VCORE_H redundant overvoltage comparator in 3.3V mode	3.3		3.47	V
2.8-21	VCORE 3.3V	threshold	COMP18: VCORE_H overvoltage comparator in 3.3V mode	3.3		3.47	V
2.8-22	VCORE 1.2V	threshold	COMP16: VCORE_L undervoltage comparator in 1.29V mode	1.20		1.29	V
2.8-23	VCORE 1.2V	threshold	COMP17: VCORE_H redundant overvoltage comparator in 1.29V mode	1.29		1.38	V
2.8-24	VCORE 1.2V	threshold	COMP18: VCORE_H overvoltage comparator in 1.29V mode	1.29		1.38	V

### Application Note:

In the extended supply range between the guaranteed supply voltage and the reset threshold the analog and digital functionality is fully given. However, the exact values of the parameters cannot be guaranteed.

The output voltage of VAS, VST50, VST33, VCORE and VINT\_X and the corresponding over- and undervoltage thresholds have a ratio metrical behavior. Therefore, the overvoltage threshold is always larger than the regulated output voltage and the undervoltage threshold is always lower than the regulated output voltage.

## 2.9 Reset Generation

The reset generation block has two main functions:

Firstly, to provide the ECU with a power on reset signal N\_POR. This signal is set to high after a defined delay time (DELAY\_NPOR) when all low voltage supplies, which are mentioned in the following picture, reached their operating ranges. This leads also to a release of the ASIC internal digital reset N\_RESET when N\_SYS\_RES is high. The high level on N\_POR is current limited and can externally be forced to low level.

Secondly, to give the microcontroller the possibility to reset the digital logic by the N\_SYS\_RES signal without any influence on the power on reset.

If the microcontroller decides to reset the internal logic the N\_SYS\_RES is set to low. After the delay time DEL\_N\_SYS\_RES the signal N\_RESET is activated.

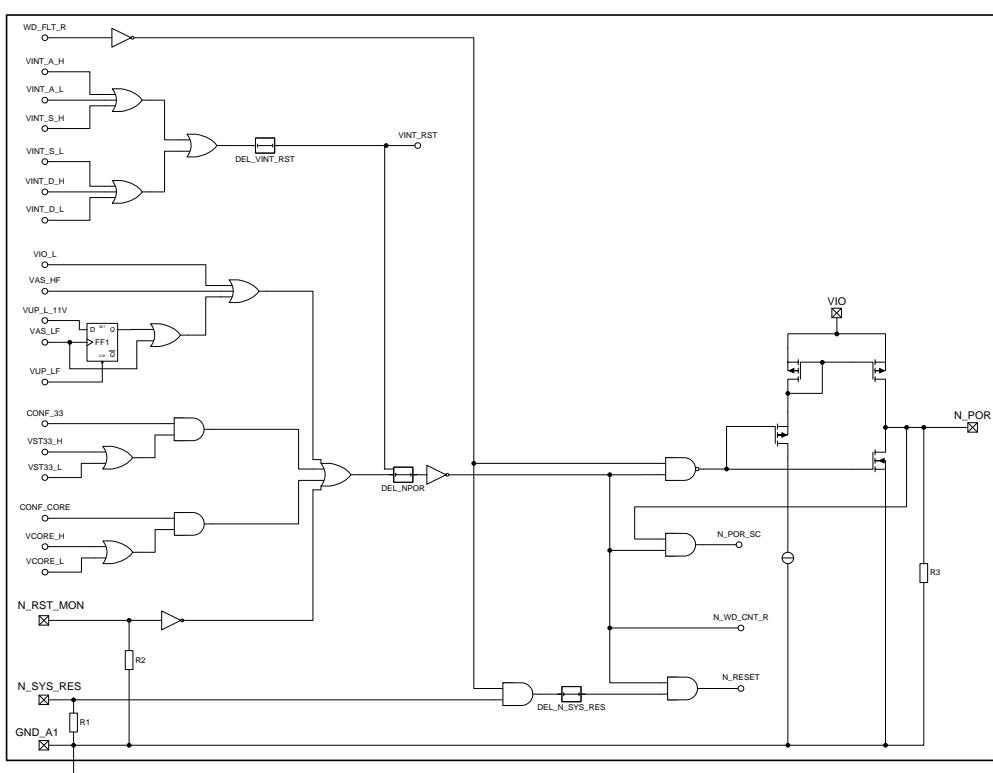
Additionally, the WD logic has the possibility to generate a power on reset via the input WD\_FLT\_R without affecting the low voltage supplies. This means that the microcontroller can be reset by the WD logic. The duration of the reset is defined by the delay of N\_SYS\_RES.

To suppress a re-release of the N\_POR during power down, when the loads (e.g. microcontroller current consumption) are switched off and the voltage at VAS rises up again, the flipflop FF1 is implemented. This flipflop suppresses the low state of VAS\_L if the voltage at VUP is lower than the threshold VUP\_L\_11V. A re-release of the N\_POR is now only possible if VUP rises up again and crosses the undervoltage level VUP\_L.

In case of an external short to high at N\_POR, while the monitoring wants to set the pin to low, the VUP and the VAS regulator are switched off by N\_POR\_SC.

In case of an erroneous ramp-up of the prestabilized supply voltages, further ramp-up of other system supply voltages is prevented, and the ASIC will stay in a reset state.

Deactivated voltage regulators are not monitored.



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## 2.9.1 Reset Generation Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.9-1	N_POR	filtertime	DEL_N_POR: power-on delay rising edge	4.5		5.5	ms
2.9-2	N_POR	filtertime	DEL_N_POR: power-on delay falling edge	20		35	us
2.9-3	N_SYS_RES	filtertime	DEL_N_SYS_RES: input delay rising edge	35		52	us
2.9-4	N_SYS_RES	filtertime	DEL_N_SYS_RES: input delay falling edge	90		115	us
2.9-5	VINT_X	filtertime	DEL_VINT_RST: delay rising edge		10		us
2.9-6	VINT_X	filtertime	DEL_VINT_RST: delay falling edge		10		us
2.9-7	N_POR	output voltage	output current N_POR = 300uA (N_POR = high)	0.8*VIO		VIO	V
2.9-8	N_POR	output voltage	output current N_POR = -2mA (N_POR = low)	0		0.2*VIO	V
2.9-9	N_SYS_RES	pulldown resistor	R1	25	50	75	kΩ
2.9-10	N_RST_MON	pulldown resistor	R2	25	50	75	kΩ
2.9-11	N_POR	pulldown resistor	R3	25	50	75	kΩ
2.9-12	N_RST_MON	threshold	input low voltage			0.3 * VIO	V
2.9-13	N_RST_MON	threshold	input high voltage	0.7 * VIO			V

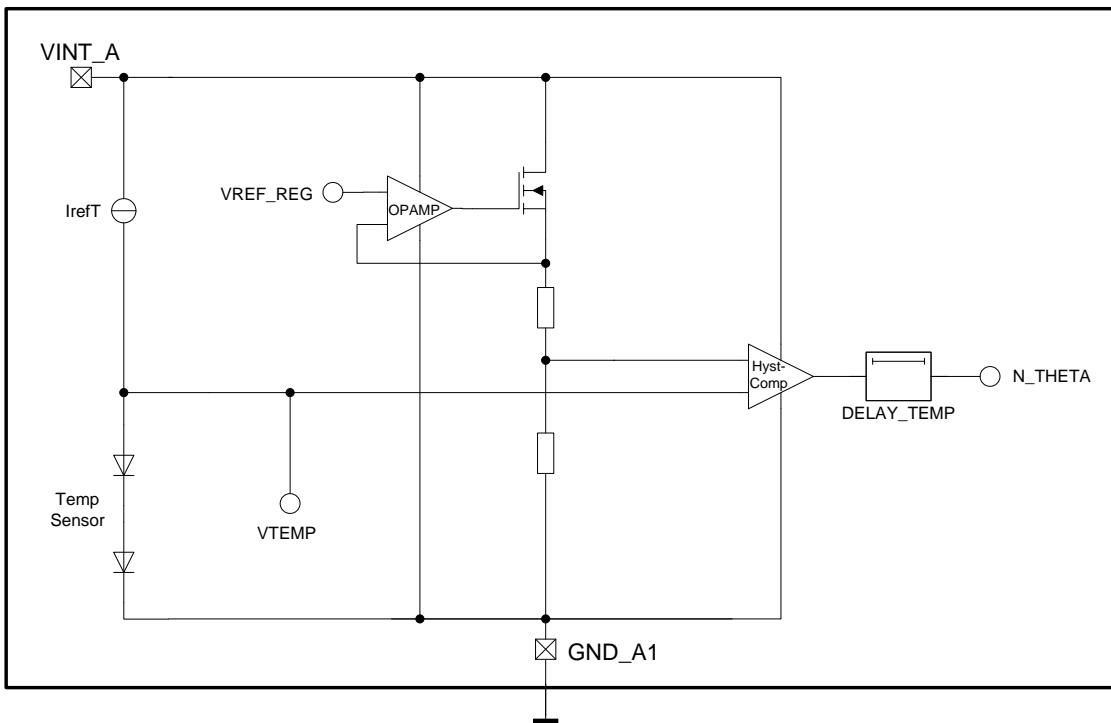
### Application Note:

Please consider, the duration of the internal reset (N\_RESET) is longer than the external reset at pin N\_POR and N\_SYS\_RES due to the delay time of N\_SYS\_RES (DEL\_N\_SYS\_RES).

## 2.10 Temperature Control

The internal temperature monitoring prevents the ASIC from overheating in case of thermal overload caused by too high power dissipation. For this purpose the function deactivates the boost converter transistor T2 (see chapter 2.3).

That means the internal supply VINT\_X, bandgap, clock generator, reference current, voltage monitoring, N\_POR, N\_SYS\_RES structure, sleep control, temperature monitoring, VAS, VST50, VST33, VCORE, PSI, LIN, FLM and SAM are still full functional, only the major power dissipation (T2) is shut down. This guarantees that the energy reserve is always completely discharged when an overtemperature situation appears.



With a defined current IrefT a chip temperature measurement double-diode produces a voltage which is proportional to the chip temperature. The high measurement preciseness is achieved by using the internal trimmed reference current IREF as the base for IrefT. The temperature dependent voltage VTEMP is connected to the central ADC and can be read out by SPI command. The actual status of the signal N\_THETA can be found in the POM\_STATUS register (ot bit).

The purpose of the overtemperature shutdown is to protect the ASIC against a massive destruction for a short period of time. The shutdown is only active when an external failure exists, e.g. a short circuit at VAS or VSTxx. In this case the ASIC is working in a not specified temperature range ( $>150^{\circ}\text{C}$ ) outside the guaranteed tolerances.

### 2.10.1 Temperature Control Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.10-1	internal	threshold	N_THETA: temp monitoring switch off	167		197	°C
2.10-2	internal	hysteresis	N_THETA: temp monitoring switch off	20		25	°C
2.10-3	internal	voltage range	VTEMP: $-40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$	0.6		1.8	V
2.10-4	internal	filtertime	N_THETA: temp monitoring switch off	0.5		1.5	ms

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## 2.11 Sleep Control

The input signal N\_SLEEP offers the possibility to shut down or wake up all internal functions. In the normal operation mode the N\_SLEEP input must be pulled-up to VZP.

If an external CAN transceiver is used, N\_SLEEP should be connected to the CAN transceiver transistor, controlled by the CAN wake-up output, so it can be switched to battery or VZP voltage in wake up condition.

The activation of the sleep mode has three impacts on the ASIC. First, the boost converter VUP is shut down by disabling its powerstage transistor T2 by the internal signal N\_SL (see picture in chapter 2.1.1). Second, the supply of the VINT\_X voltages is steadily switched to VAS and third, the buck converter VAS and the VER charger will be switched off (VAS\_SLEEP) when the VUP voltage has reached the threshold of COMP3 (VUP\_L\_VZP, see chapter 2.2).

The current consumption at VZP will be higher than the maximum sleep current as long as the VER voltage can supply the ECU. The current consumption is reduced to the given values when an internal reset is activated.

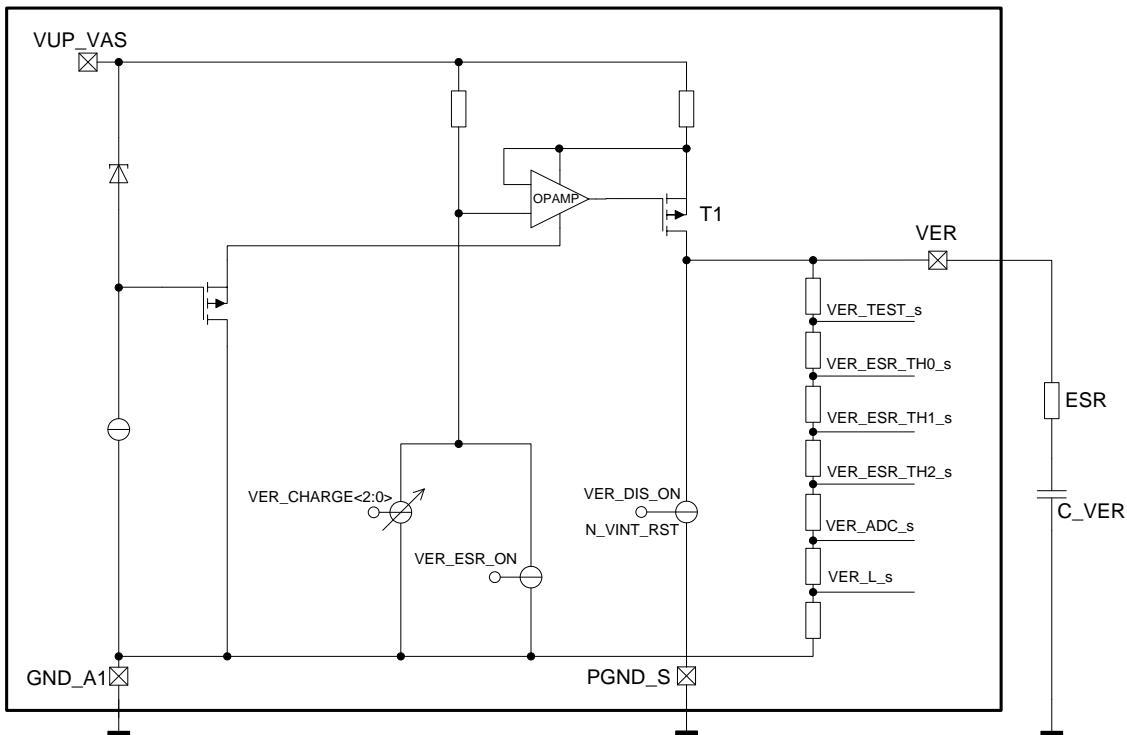
The actual status of N\_SLEEP can be read out with the SPI instruction *POM\_STATUS* (sl bit).

### 2.11.1 Sleep Control Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.11-1	VZP, L1H, VUP, VUP_VAS, VSYNC, DIA, VBAT_MONX	input current sum	sleep mode active (N_SLEEP = low) and system shutdown	0	30	60	uA
2.11-2	VZP, L1H, VUP, VUP_VAS, VSYNC, DIA, VBAT_MONX	input current sum	sleep mode active (N_SLEEP = low) and system shutdown with 14V at battery supplied pins at room temperature	0		20	uA
2.11-3	N_SLEEP	threshold	sleep mode active	0		1.5	V
2.11-4	N_SLEEP	threshold	sleep mode inactive	2.8		36	V
2.11-5	N_SLEEP	input current	N_SLEEP ≤ 20V			50	uA

## 2.12 VER Charger and Discharger

The VER charger is used to charge up the energy reserve capacitor connected to the pin VER. The charge current can be programmed in a range of 20mA up to 120mA by an internal 3-bit reference current sink (VER\_CHARGE<2:0>). This reference current is multiplied by a resistor ratio producing the output current which is regulated by the powerstage T1 and the appropriate OPAMP.



When the boost converter VUP is in over voltage condition ( $V_{UP} > V_{UP\_H}$ ) and the VER voltage is above  $VER\_L$ , the charging process will be stopped immediately. After the deactivation of the VER charger due to the VUP overvoltage condition two cases can be distinguished:

- If the overvoltage condition at VUP remains and the VER voltage drops below  $VER\_L$ , the VER charger will be activated after the filter time for the detection of the  $VER\_L$  threshold has passed. Thus, the capacitor connected to VER is charged until the voltage rises above  $VER\_L$ . Then, the VER charger is deactivated once again after the detection filter time has passed, and the process repeats so that the VER voltage stays around  $VER\_L$ .
- After the VUP voltage drops to less than  $V_{UP\_H}$  level again, the charging process will automatically be started again with the previously programmed current.

The second condition which can stop the charger is  $V_{UP} < V_{UP\_L\_11V}$  and  $VER < VER\_TEST$ . The charging process will not start again automatically when this condition is not valid anymore and has to be re-enabled by SPI. This interrupt is only active until VER has crossed the  $VER\_TEST$  level for the first time

When the capacitor  $C_{VER}$  is fully charged the powerstage will remain in conducting condition to assure an automatic feedback ability from VER to VUP in case of an autarky condition.

During autarky mode ( $V_{ZP} < V_{ZP\_L}$  and  $VER > VER\_TEST$ ) the charger is set to maximum current under any condition.

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During sleep mode the charger is switched off by the signal VAS\_SLEEP.

The VER discharge current sink is triggered by the internal VER\_DIS\_ON signal (in case of controlled discharging during capacitance tests) or by the internal reset N\_VINT\_RST to fully discharge the capacitor at power down.

Once VER has exceeded VER\_L, the charging current is reduced to 20 mA automatically regardless of the programmed charging current once the voltage at VER drops below VER\_TEST. The charging current is switched back to the programmed value in steps of 20 mA once VER rises above VER\_TEST.

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## 2.12.1 VER Charger and Discharger Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.12-1	VER	charge current	VER_CHARGE<2:0> = 001	-20%	20	+20%	mA
2.12-2	VER	charge current	VER_CHARGE<2:0> = 010	-10%	40	+10%	mA
2.12-3	VER	charge current	VER_CHARGE<2:0> = 011	-10%	60	+10%	mA
2.12-4	VER	charge current	VER_CHARGE<2:0> = 100	-10%	80	+10%	mA
2.12-5	VER	charge current	VER_CHARGE<2:0> = 101	-10%	100	+10%	mA
2.12-6	VER	charge current	VER_CHARGE<2:0> = 11x	-10%	120	+10%	mA
2.12-7	VER	discharge current	3V<VER<VER_TEST	15		35	mA
2.12-8	VER	discharge current	VER_TEST<VER<36V	3		7	mA
2.12-9	VER	filtertime	VER_LF	60		110	us
2.12-10	VUP_VAS, VER	resistance	Autarky mode	3.5		6.5	Ω

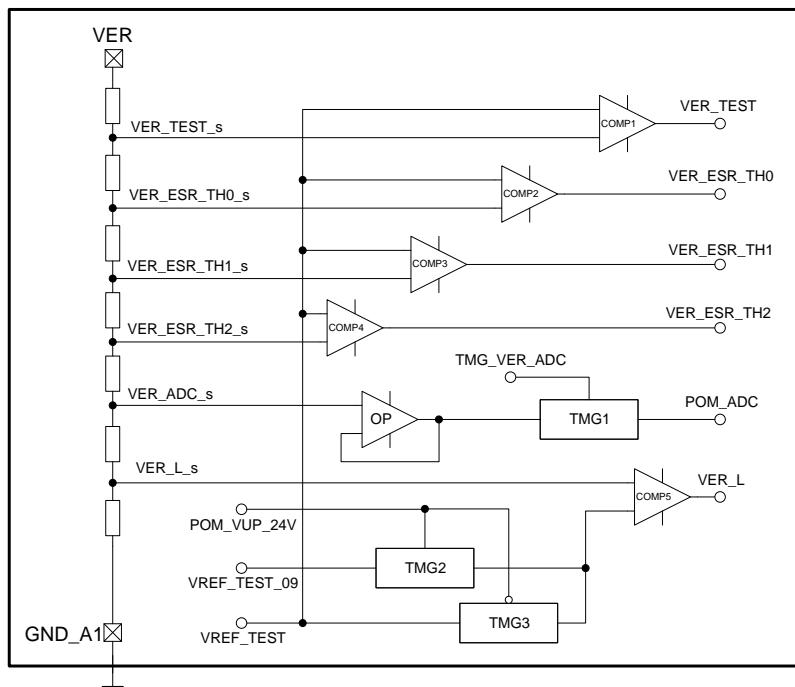
### **Application Note:**

For VER autarky currents higher than 400mA an external Schottky diode between VER and VUP must be used.

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## 2.13 POM Built-In Tests

There are several built-in tests which are triggered by the software and which use the VER charger circuit (see chapter 2.12). Additionally, a lot of monitoring functions are implemented which are shown in the following picture.



The tests can be started after the VER capacitor has been charged up to the VER\_TEST voltage level (COMP1) by the SPI command POM\_VER\_CURR. This level will be obtained by switching off the charger until the VER\_TEST signal changes to low by the internal losses and then charging with 20mA up to VER\_TEST level again.

The ESR and the cap tests are initial tests and can only be performed at the VER\_TEST level before the VER charging is set up to 33V/24V (bit vlm).

The cycl cap test and the autarky test can only be performed at VER>VER\_L and will automatically be interrupted if the firing stage is enabled by DIS\_SHP or DIS\_AHP or if the VZP voltage drops below the threshold VZP\_L.

The available tests are described in the next sections followed by an overview of a standard test sequence.

### 2.13.1 VER ESR Test

The VER ESR test is implemented to make sure that the ESR of the external VER capacitor is not too large to influence the airbag ignition by its voltage drop. This test is software controlled and should be executed at every startup.

After the VER\_TEST level is reached the ESR test can be started by the SPI command POM\_START\_BIST with the respective mode bits (mode = 01).

There are 3 relevant return bits in this SPI command for the ESR test:

If the return bit 'ta' is high, then a POM built-in test is already running.

If the return bit 'vel' is high, then the VER voltage has reached the VER\_L level.

And if the return bit 'bc' is high, then the VER\_TEST voltage level has not been reached yet or the bit 'vlm' in the SPI command POM\_VER\_CURR has been set.

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If one of the return bits is active (*ta*=1 or *vel*=0 or *bc*=1), then the request is ignored, otherwise the ESR test is launched.

In the first step then, the VER discharge sink is activated until *VER\_TEST* changes to low. After charging up again with 20mA until *VER\_TEST* changes to high, the ESR test current is flowing for 50us creating a voltage drop proportional to the resistance. This voltage drop is monitored by three comparators (COMP2/3/4) and if the threshold voltages are exceeded, when the ESR current is flowing, the corresponding bits (*et0/1/2* in SPI command *POM\_READ\_BIST*) are set. Multiple executions of this test are possible and recommended for a high system robustness. Detailed information concerning the SPI bits are described in chapter 2.14.

## 2.13.2 VER Cap Test

The VER cap test is implemented to initially make sure that the external VER capacitor is large enough to supply all connected airbag firing loops. This test is software controlled and should be executed at every startup after the ESR test.

Using the same SPI command *POM\_START\_BIST* the capacitor test must be started with a load current (*i\_bist*) and a charging time (*t\_bist*). It can be started with or without a preceding discharge to VER test level depending on the failure handling of the system and the number of possible test executions. The mode without discharge is '10' and with discharge '11'. If the test is started with the discharge mode set to '10', the test starts with the charging of the VER capacitor directly. If the test is started with the discharge mode set to '11', the voltage at the VER pin is first discharged to a voltage equal to the VER test level, after which the charging of the VER capacitor is started. One LSB '*t\_bist*' corresponds to 6 ms charging time and one LSB '*i\_bist*' corresponds to 20mA load current. If one of the return bits '*ta*', '*vel*' and '*bc*' is high, then the request is ignored, otherwise the cap test is launched.

The duration of this test is much longer than the ESR test and utilizes the ADC measurement to monitor the change of the output voltage at VER. This result can again be found in the *POM\_READ\_BIST* register. The bit '*delta\_ver*' is the voltage difference at VER which is caused by the charge current. One LSB '*delta\_ver*' corresponds to the VER divider factor times the ADC resolution (please see chapter 4.8 starting on page 144).

If the voltage change during this test is higher than 3.5V, the test will be interrupted immediately and the "ER missing" bit will be set (*delta\_ver* is set to zero). As a consequence the cap test will not be executed when the VER voltage is higher than 33V/24V-3.5V.

Detailed information concerning the SPI bits are described in chapter 2.14.

## 2.13.3 VER Cyclic Cap Test

The VER cycle cap test is implemented to make sure that during normal operation the VER capacitor is still connected to the pin.

Therefore, the VER discharger is enabled (while the charging is disabled) for 10ms by the SPI command *POM\_CYCL\_CAP*. This leads to a decrease of the VER voltage. In failure cases the *VER\_L* comparator (COMP5) is activated. The test will immediately be interrupted, the charger enabled and a failure flag can be found with the next *POM\_CYCL\_CAP* command.

To start the VER cycle cap test the bit 'on' in the spi command *POM\_CYCL\_CAP* must be set to high and the bit 'aut' to low.

There are 4 relevant return bits in this SPI command for the cycle cap test:

If the return bit '*ta*' is high, then a POM built-in test is already running.

If the return bit '*bc*' is high, then the *VER\_L* voltage level has not been reached yet. If the return bits '*ta*' and '*bc*' are low, the VER cycle cap test is launched, otherwise the request is ignored.

If the VER cycle cap test is aborted, because the VER voltage drops below the threshold *VER\_L*, then the return bit '*res*' is set to high.

The VER cycle cap test is immediately aborted, if the VZP voltage drops below the threshold *VZP\_L* or if the firing stages are enabled by *DIS\_SHP* or *DIS\_AHP*. In this case the return bit '*err*' is set to high.

For information the actual status of the VER charger is given by the bit '*sty*' which complies with the bit 15 of the *POM\_STATUS* command.

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Detailed information concerning the SPI bits are described in chapter 2.14.

## 2.13.4 VER Autarky Test

The autarky test uses the same command like the cycl cap test and disables the boost converter VUP for the programmed time (aut\_time). This again leads to a decrease of the VER (and VUP) voltage and in failure cases a failure flag depending on VER\_L will be set.

To start the autarky test the bit 'aut' in the spi command POM\_CYCL\_CAP must be set to high and the bit 'on' to low. Moreover, the duration for disabling the boost converter VUP must be transferred by 'aut\_time', one LSB corresponds to 1024us of disabling time.

There are 4 relevant return bits in this SPI command for the autarky test:

If the return bit 'ta' is high, then a POM built-in test is already running.

If the return bit 'bc' is high, then the VER\_L voltage level has not been reached yet. If the return bits 'ta' and 'bc' are low, the autarky test is launched, otherwise the request is ignored.

If the autarky test is aborted, because the VER voltage drops below the threshold VER\_L, then the return bit 'aky' is set to high and the boost converter VUP is immediately reenabled.

The VER autarky test is immediately aborted, if the VZP voltage drops below the threshold VZP\_L or if the firing stages are enabled by DIS\_SHP or DIS\_AHP. In this case the return bit 'err' is set to high.

For information the actual status of the VER charger is given by the bit 'sty' which complies with the bit 15 of the POM\_STATUS command.

Detailed information concerning the SPI bits are described in chapter 2.14.

## 2.13.5 POM automatic measurements

The automatic measurements are implemented to monitor the voltages at VBAT\_MON1/2, VUP, VER and the temperature monitoring diode.

This automatic measurement can be enabled by the bit 'on' in the SPI command POM\_START\_AUTO. If the automatic measurement is switched on, the values for VBAT\_MON1/2 are updated every 2ms and the values for VUP, VER and temperature diode every 3ms. The measurement is done by the internal ADC.

The current values can be read out via the SPI commands POM\_READ\_AUTO1...5.

Detailed information concerning the SPI commands are described in chapter 2.14.

## 2.13.6 POM built-in Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
2.13-1	VER	test current	ESR test	-10%	930	+10%	mA
2.13-2	VER	test time	ESR test switch on time		50		us
2.13-3	VER	threshold	COMP1: VER_TEST	10.7	11.0	11.1	V
2.13-4	VER	hysteresis	COMP1: VER_TEST	70		200	mV
2.13-5	VER	threshold	COMP2: VER_ESR_TH0	11.2	11.4	11.6	V
2.13-6	VER	threshold	COMP3: VER_ESR_TH1	11.4	11.6	11.8	V
2.13-7	VER	threshold	COMP4: VER_ESR_TH2	11.6	11.8	12.0	V
2.13-8	VER	output current	VER Cap test	see 2.11	see 2.11	see 2.11	mA
2.13-9	VER	threshold	COMP5: VER_L in 24V mode	22.25		23.75	V
2.13-10	VER	threshold	COMP5: VER_L in 33V mode	31		33	V
2.13-11	VER	divider factor	for ADC measurement at 5.3V<VER<36V	-3%	13.2	+3%	

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## 2.14 POM SPI instructions

Program power supply:

### **SPI instruction PROG\_POM**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	24v	ast	iup	
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	24v	ast	iup

iup : I\_VUP : VUP current limitation : 0 = high level, 1 = low level (default 0)

ast : ASSIST : assistance mode : 1 = VUP off for VUP>VUP\_L and VBAT>10V (default 0)

24v : 0 = VUP 33V, 1 = VUP 24V (default 0)

Set VER load current:

### **SPI instruction POM\_VER\_CURR**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	dis	ver_current	vlm		
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

vlm : VER load mode : 0 = loading up to 11V, 1 = loading up to 33V/24V (default 0)

ver\_current : 000...110: 0...120mA, 20mA steps (default 000, ver current off, 11x=120mA)

dis : discharge mode : 1 = discharge VER on (disables VER loading), 0 = off (default 0)

Configure cyclic capacitance test:

### **SPI instruction POM\_CYCL\_CAP**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-									aut	on
SPI output data	0	0	0	0	0	0	0	0	0	0	sty	aky	err	ta	bc	res

on : 1 = cyclic capacitance test on, 0 = cyclic capacitance test off (default 0)

aut : 1 = autarky test on, 0 = autarky test off (default 0)

aut\_time : autarky test time 0...255 steps, 1024us per step

res : result of last cyclic capacitance test : 0 = OK, 1 = error (bit is latched, clear by new start)

bc : busy charge : 1 = VER is too low (VER<VER\_Lf) and the ER-charger is still active

ta : test active : 1 = POM BIST running

err : error flag : 1 = autarky test / cycl. capacitance test canceled (by VZP\_L=1 or internal FLM-enable signal), 0 = test valid (bit is latched, clear by new start)

aky : result of autarky test : 1 = error, 0 = OK (bit is set at the end of autarky test)

sty : ER steady information : 1 = ER charge current flowing, 0 = ER fully charged (steady state)

The cyclic capacitance test (on=1) and the autarky test (aut=1) cannot be started simultaneously. In case on=1 and aut=1 is set, no test is started.

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Read power supply status:

## **SPI instruction POM\_STATUS**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	sty	vin	nok	sl	erc	ot	c6	c5	c4	c3	1	c1	vet	vzl	v50	vel

vel : VER\_Lf : 1 = VER low (bit is latched (high level), clear by read (default=0))

v50 : VST50\_NB : 1 = VST50 not in band (bit is latched, clear by read)

vzl : VZP\_L : 1 = VZP low (bit is latched, clear by read)

vet : VER\_TEST : 1 = VER > VER test level

c1, c3, c4, c5, c6 : level of pin CONF\_33, CONF\_CORE, CONF\_VC1, CONF\_VC2, CONF\_VBAT

ot : over temperature : 1 = temperature too high, VUP switched off (bit is latched, clear by read)  
 erc : ER\_CHARGE : VUP<11.5V (vu-Comparator of PSI) & VER\_TEST=0 (bit is latched, clear by read). This bit can only be set until a charger current was programmed (POM\_VER\_CURR) and VER\_TEST=1.

sl : sleep mode : 0 = normal mode, 1 = sleep mode request

nok : voltage monitor for VUP, VAS, VINT\_X, VST33 and VCORE : 1 = at least one of the monitored voltages VUP, VAS, VST33 or VCORE is in an out-of-band condition or VINT\_X is in an overvoltage condition (time filtering of 430...620 ns), 0 = voltages in range (bit is latched, clear by read)

vin : VINT supply : 1 = VINT supplied from VZP, 0 = VINT supplied from VAS

sty : ER steady information : 1 = ER charge current still flowing, 0 = ER fully charged, steady state

Control dc/dc converter:

## **SPI instruction POM\_CONVERTER**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	hlf	sw	jit	ctrl	off
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

off : 1 = switch off slope shaping control, 0 = switch-on slope shaping control (default 0)

ctrl (off=0): 1 = automatic slope shaping control (on for VBAT > 10V), 0 = always on (default 1)

jit: jitter of converter clock : 1 = jitter active, 0 = no jitter (default 0)

sw (jit=1): sweep jitter of converter clock: 1 = jitter sweep active, 0 = inactive (default 0)

hlf (jit=1): 1 = reduces jitter amplitude to half, 0 = full jitter amplitude (default)

The slope shaping reduces the recovery current spike of the external freewheeling diode.

Start power supply build-in self test:

## **SPI instruction POM\_START\_BIST**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SPI input data	-	-	-	-	-	-	mode	t_bist					i_bist				
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	vzl	ta	vel	bc

i\_bist : BIST current : 000...110: 0...120mA, 20mA steps

t\_bist : BIST time : 0...186ms, 6ms steps

mode : 00 = no BIST, 01 = ESR BIST, 10 = CAP BIST, 11 = CAP + Discharge BIST

bc : busy charge : 1 = VER is too low (VER<VER\_TEST) or vlm is/was 1 (POM\_VER\_CURR)

vel : VER\_Lf : 1 = VER low (bit is not latched)

ta : test active : 1 = POM BIST running

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vzl : VZP\_I : 1 = VZP low (bit is latched, cleared by either POM\_START\_BIST or POM\_READ\_BIST)

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Read power supply build-in self test results:

## **SPI instruction POM\_READ\_BIST**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	et0	ta	vet	mis	ch	vzl	vel	et2	et1	delta_ver						

delta\_ver :

0...72: differential voltage of VER before and after ER capacity test (48.39mV/LSB)

73...126: unused

127 : result invalid (VER start value too high)

et1 : ESR test 1 : 1 = VER > ESR\_START + 0.6V (bit is latched, clear by read)

et2 : ESR test 2 : 1 = VER > ESR\_START + 0.8V (bit is latched, clear by read)

vel : VER\_Lf : 1 = VER low (bit is latched (low level), clear by read (default=1))

vzl : VZP\_L : 1 = VZP low (bit is latched, clear by read)

ch : charge error : 1 = no ER charge current flowing (bit is latched, clear by read)

mis : ER missing : 1 = ER capacitance is missing (bit is latched, clear by read)

vet : VER\_TEST : 1 = VER test level

ta : test active : 1 = BIST running

et0 : ESR test 0 : 1 = VER > ESR\_START + 0.4V (bit is latched, cleared by read)

The bits vel and vzl are cleared by either POM\_START\_BIST or POM\_READ\_BIST

Start power supply automatic measurements:

## **SPI instruction POM\_START\_AUTO**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	on
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

on : 1 = automatic measurement on, 0 = automatic measurement off

Read power supply automatic measurement results:

## **SPI instruction POM\_READ\_AUTO1...5**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	adc_result									

adc\_result : ADC result from automatic measurement

channel 1 : VBAT\_MON1 (every 2 ms)

channel 2 : VBAT\_MON2 (every 2 ms)

channel 3 : VUP (every 3 ms)

channel 4 : VER (every 3 ms)

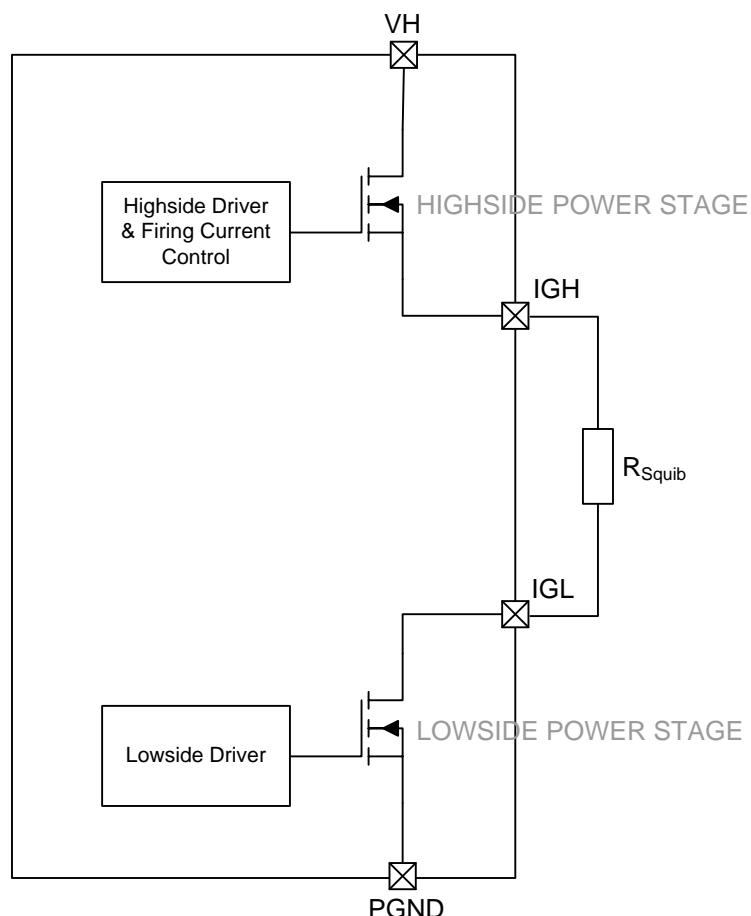
channel 5 : temperature (every 3 ms), to be used for ASIC production test only

The channel is coded within the least 3 bits of the instruction.

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### 3. Functional Description Firing Loop Module (FLM)

A typical firing loop consists of a highside and a lowside power stage connected through a squib resistor at the firing pins (ignition highside IGH, ignition lowside IGL). Squib firing is only possible if both highside and lowside power stages are switched on. In case of firing, the current provided by the highside voltage ( $V_H$ ) flows through the squib to the power ground terminal (PGND). The current is controlled by the highside power stage.



The firing loop module contains highside and lowside power stages for DC-firing and loop monitoring functionality. It allows a simple airbag application using a highly sophisticated safety concept.

For the airbag system ASIC CG904 16 firing loops are implemented, for CG903 12 firing loops and for CG902 8 firing loops.

# Data sheet CG904, CG903, CG902

## Features:

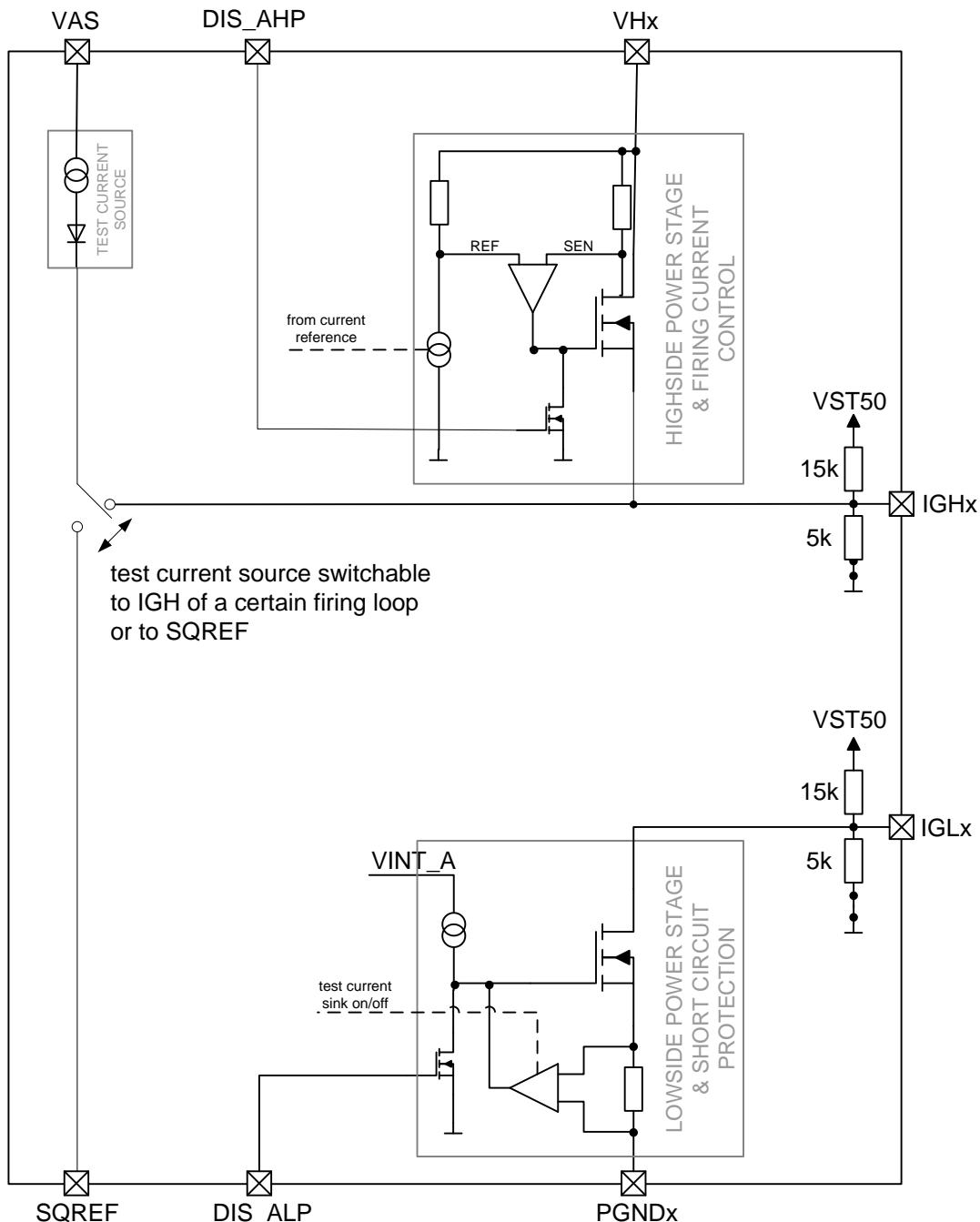
- 16 firing loops (CG904), 12 firing loops (CG903) or 8 firing loops (CG902)
- highside and lowside drivers and power stages fully integrated
- highside and lowside power stages short-circuit protected
- hardware switch-off of power stages
- general disable for power stages
- special disable of dedicated power stages
- independent control and power supply of highside and lowside power stages
- different firing modes programmable by SPI:
  - static mode I: 1.85 A for 0.7 ms
  - static mode II: 1.75 A for 0.5 ms
  - static mode III: 1.2 A for 2 ms
  - dynamic mode V: 1.75 A for 0.7 ms, automatic extension to 1.2 A for 2.0 ms possible
  - dynamic mode VI: 1.5 A for 1.5 ms, automatic extension up to 3.0 ms possible
- high resolution firing current counters (40 kHz, 7 bit), independent of firing current
- automatic high precision loop diagnosis:
  - detection of leakage to battery, ground and between firing loops
  - VH voltage measurement and SVR diagnosis by the internal ADC
  - squib resistance measurement for determining the ohmic part
  - test current level and duration for squib resistance measurement programmable via SPI
  - squib detection test for detecting an open load
  - safe power stage diagnosis test
  - connector capacitor diagnosis
- sophisticated safety concept
- maximum distance between highside and lowside power stages due to cross placement on chip
- only 1 external resistor necessary for the squib reference (SQREF)

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# Data sheet CG904, CG903, CG902

## Block Diagram:

Focusing on the basic principle, a block diagram of the firing loop module is presented next showing only one exemplary firing loop. It includes a highside power stage with firing current control, a lowside power stage and driver, a test current source and voltage dividers for diagnosis functions.

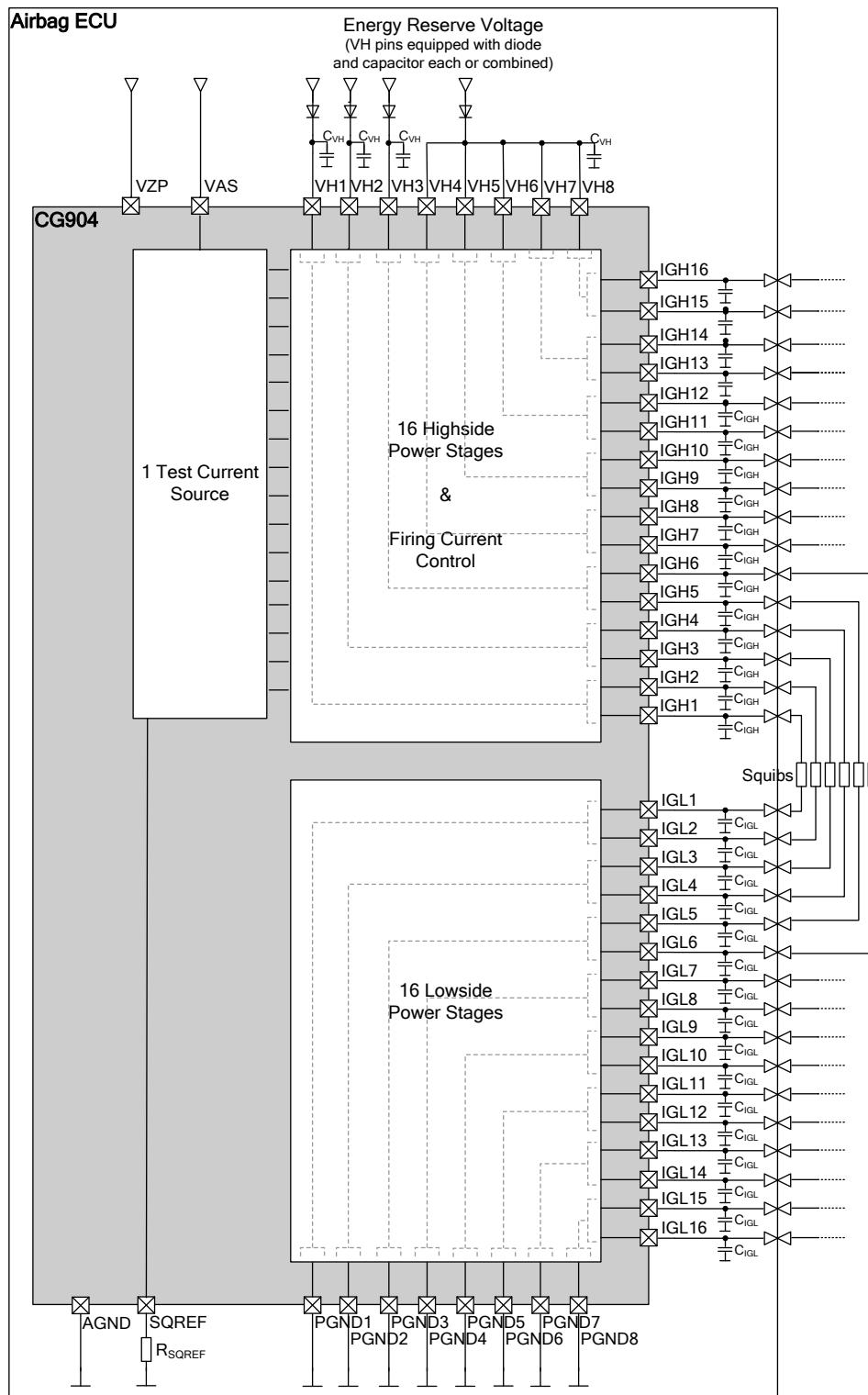


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# Data sheet CG904, CG903, CG902

## Application Diagram:

The following diagram shows the pin application of the firing loop module. Furthermore, the supply of two firing loops by one VHx and one PGNDx is depicted:



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## 3.1 Squib Highside Power Stage & Driver

The firing current is controlled by the high side power stage. Firing current and duration, i.e. the firing mode, can be programmed via SPI command *PROG\_FLM\_MODE* (please see chapter 3.1.4).

Switching-on of a high side power stage is triggered by SPI whereas switching-off can be done either via SPI during an ongoing firing or hardware-triggered by the ASIC itself at the end of firing (auto-switch-off function). This auto-switch-off function is always active and cannot be disabled.

However, firing of a loop is only possible if programming is completed by the SPI command *EOP* (end of programming, please see chapter 4.1.6) which enables unlocking the low side power stages.

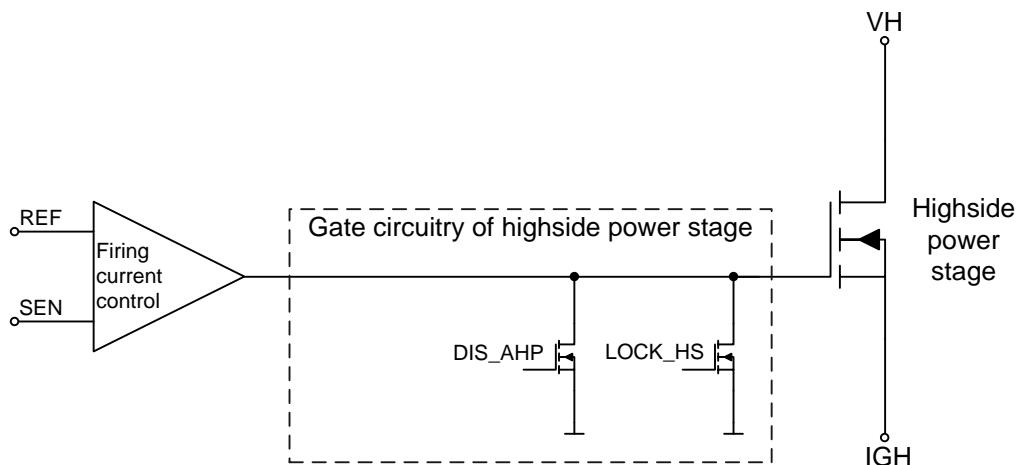
After programming, high side power stage switch-off can be guaranteed by the hardware and can be done by the ASIC itself. After the high side was switched on, the power stage has to be switched off before it can be switched on again. This can be done explicitly by SPI command *FLM\_HS\_ON* (please see chapter 3.1.4) or indirectly by locking the power stages. Apart from that, switching-off of power stages by SPI command is always possible even if the auto-switch-off time has not been reached yet. In case of an additional switch-on command during the firing of a loop, the firing time is not extended and the auto-switch-off timer is not reset. The timer is only reset when the high side power stage is switched off by SPI command *FLM\_HS\_ON* or locked by SPI command *FLM\_UNLOCK* (please see chapter 3.4.5).

### 3.1.1 Squib Highside Lock

In order to provide highest safety against unwanted deployment, the high side gate driver is equipped with a locking mechanism shown in the figure below. The following two conditions have to be fulfilled for switching-on the high side power stage:

- system reset (inactive high) releases locking mechanism *LOCK\_HS* in case of correct ASIC supply voltages.
- internal safety module releases locking mechanism *DIS\_AHP* depending on crash data.

Both signals *LOCK\_HS* and *DIS\_AHP* are generated internally by the ASIC.



### 3.1.2 Firing Current Counter

The firing current is controlled by each highside power stage. The detection threshold for the firing counter is independent of the firing current level and firing channel. Therefore two counters are used covering the firing modes 1.2 A, 1.75 A and the low energy actuator mode (LEA) with 1.5A. Both counters have a bit width of 7 bits, are independent and able to count simultaneously. For each loop there are two dedicated firing counters. These counters provide the firing current duration of each loop (25  $\mu$ s per LSB) and can be read out with the SPI command *FLM\_READ\_FIRE\_CNT* (please see chapter 3.1.5). The firing counters are cleared by reset (power-on or system reset) and by the SPI instruction *FLM\_CLEAR\_FIRE\_CNT*.

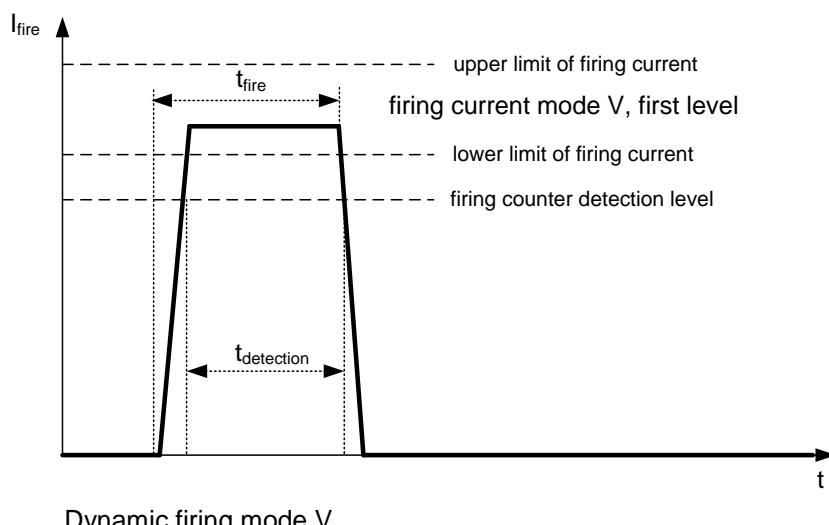
In case of choosing firing mode V and VI, the content of the firing current counters are used to decide if firing has to be extended.

#### Application Note:

The firing current counters must not be read out during firing, but only after. Otherwise, the value might be corrupted but firing is not influenced.

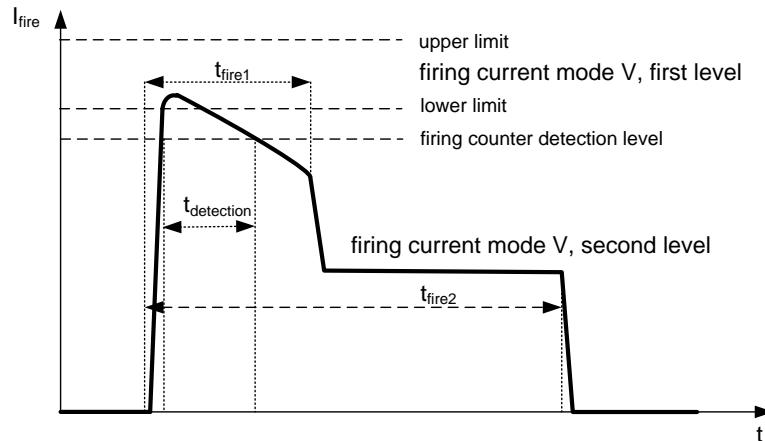
### 3.1.3 Dynamic Firing Mode (Firing Mode V and VI)

Firing modes V and VI feature a dynamic adjustment due to the actual driven firing current. The following figure shows a typical firing current waveform. Mode V's first level firing current (minimal 1.75 A) is turned off after the minimum time of 700  $\mu$ s ( $t_{fire}$ ) if the minimal firing current is detected for at least 700  $\mu$ s ( $t_{detection}$ ).



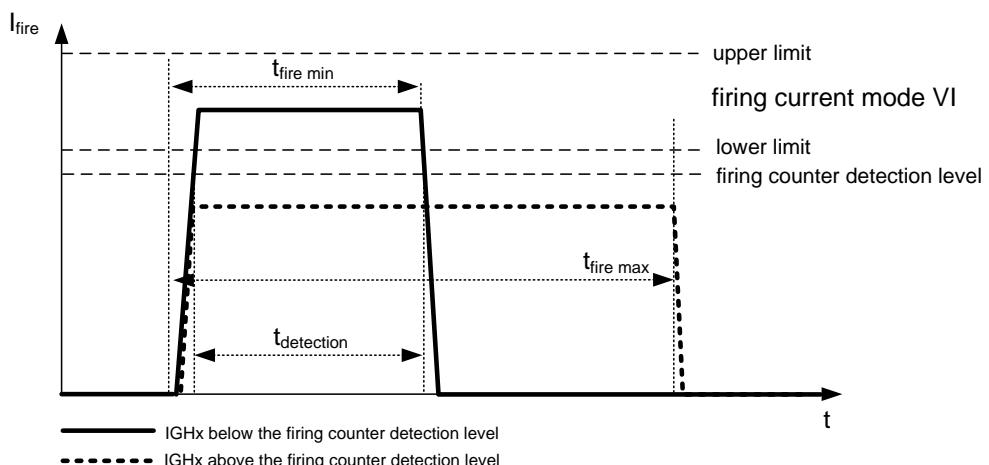
# Data sheet CG904, CG903, CG902

If the minimal firing current cannot be driven at mode V's first level ( $t_{fire1}$  up to 1 ms) for at least 700  $\mu$ s ( $t_{detection}$ ), the ASIC automatically extends firing to 2000  $\mu$ s ( $t_{fire2}$ ) after 1ms and thereby reduces the firing current to mode V's second level (minimal 1.2 A) as shown in the figure below.



Dynamic firing mode V in case fire time prolongation

Mode VI's firing current (minimal 1.5A) is turned off after the minimum time of 1500 $\mu$ s ( $t_{fire min}$ ) if the minimal firing current is detected for at least 1500 $\mu$ s ( $t_{detection}$ ). If the minimum firing current is not sufficient, the firing current is turned off after 3000 $\mu$ s at the latest.



Dynamic firing mode VI

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## 3.1.4 Squib Highside SPI Instructions

Program firing loop mode:

### **SPI instruction PROG\_FLM\_MODE**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	fire_mode_m4				fire_mode_m3				fire_mode_m2			fire_mode_m1				
SPI output data	fire_mode_m4				fire_mode_m3				fire_mode_m2			fire_mode_m1				

fire\_mode\_mx : fire mode firing loop module x (default = 0001)

x000 : firing mode I 1.85A / 0.7ms

x001 : firing mode II 1.75A / 0.5ms

x010 : firing mode III 1.2A / 2ms

x100 : firing mode V 1.75A / 0.7...1.0ms + 1.2A / 2ms remaining (VW mode)

x101 : firing mode VI 1.5A / 1.5ms...3ms (LEA mode)

0xxx : all four loops of a quad module are configured with the same firing mode.

1xxx : the lower two loops of a quad module (bits 0,1,4,5,8,9,12,13) are set to firing mode VI independent from the higher two loops of this quad module (bits 2,3,6,7,10,11,14,15).

All undefined modes are mapped to firing mode I.

Switching of firing loop highside power stages:

### **SPI instruction FLM\_HS\_ON**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cx : 1 = switch-on highside firing loop x, 0 = switch-off highside firing loop x

Read fire counter:

### **SPI instruction FLM\_READ\_FIRE\_CNT1...16**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	fire_counter_hl							0	fire_counter_ll						

fire\_counter\_ll : fire counter low level (1.2A current threshold)

fire\_counter\_hl : fire counter high level (1.5A current threshold in LEA mode else 1.75A)

The fire counter channel address is coded within the least 4 bits of the instruction.

The fire counter values are invalid during firing and must be read after firing only.

Clear firing current counter:

### **SPI instruction FLM\_CLEAR\_FIRE\_CNT**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Clears all firing current counters

The clearing of the firing current counters takes up to 12.5us. Clearing of the firing counters is only possible if all highsides are locked (e.g. by SPI command *FLM\_UNLOCK*).

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## 3.1.5 Squib Highside Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
3.1-1	IGHx	Idle voltage	High side power stage is switched off	1.19	1.25	1.31	V
	IGHx	Firing mode I	firing mode I, 7V<=VHx <= 24V				
3.1-2		-I <sub>Fmode I</sub>	output current , Rsquib =2Ohm	2.0		2.4	A
3.1-3		ton <sub>Fmode I</sub>	ton <sub>Fmode I</sub>	700		820	us
	IGHx	Firing mode II	firing mode II, 7V<=VHx <= 27V				
3.1-4		-I <sub>Fmode II</sub>	output current , Rsquib =2Ohm	2.0		2.4	A
3.1-5		ton <sub>Fmode II</sub>	ton <sub>Fmode II</sub>	500		630	us
	IGHx	Firing mode III	firing mode III, 7V<=VHx <= 20V				
3.1-6		-I <sub>Fmode III</sub>	output current , Rsquib =2Ohm	1.4		1.65	A
3.1-7		ton <sub>Fmode III</sub>	ton <sub>Fmode III</sub>	2000		2130	us
	IGHx	Firing mode V	firing mode V, 7V<=VHx <= 20V				
3.1-8		-I <sub>Fmode Va</sub>	output current level a, Rsquib =2Ohm	2.0		2.4	A
3.1-9		ton <sub>Fmode Va</sub>	ton <sub>Fmode Va</sub>	700		1120	us
3.1-10		-I <sub>Fmode Vb</sub>	will be enabled if IGHx < IGHx_min after t <sub>on_a</sub> output current, Rsquib =2Ohm level b		1.4	1.65	A
3.1-11		ton <sub>Fmode Vb</sub>	After 1ms the firing counter is checked: If the value of the firing counter is smaller than 28 (700us) the switch on time will be prolonged to ton <sub>Fmode Vb</sub>				
		ton <sub>Fmode Vb</sub>	ton <sub>Fmode Vb</sub>	2000		2130	us
	IGHx	Firing mode VI	firing mode VI, 7V<=VHx <= 20V Low energy actuator (LEA) mode.				
3.1-12		-I <sub>Fmode VI</sub>	output current, Rsquib =2Ohm	1.8		2.15	A
3.1-13		ton <sub>Fmode VI</sub>	ton <sub>Fmode VI</sub>	1500		3000	us
	VHx, IGHx	VDS(on)	Voltage drop across high side driver IGHx				
3.1-14			VHx-VIGHx @IGHX=1.2A			2.5	V
3.1-15			VHx-VIGHx @IGHX=1.75A			3.0	V
	VHx, IGHx	Reverse voltage drop VD	Voltage drop, if VHx is unsupplied				
3.1-16			VD=VIGHx-VHx @IGHx=1.2A	0.5			V
3.1-17	IGHx	Slew rate of firing current	corresponding selected firing mode C <sub>IGHxmin</sub> , C <sub>IGLxmin</sub>			1	A/us
			Measure of 10% - 90% value of maximum range of the firing current.				
	IGHx	Current level detection threshold for firing counter	7V<=VHx <= 27V Value of the actual output current corresponding to the choosen firing mode level.				
3.1-18			low level	1.2		-I <sub>Fmode I</sub>	A
3.1-19			high level (firing mode VI)	1.5		-I <sub>Fmode hVI</sub>	A
3.1-20			high level (firing mode not VI)	1.75		-I <sub>Fmode h</sub>	A
3.1-21		Sample time of the firing counter	Time base derived from external ECLK frequency.		25		us
	VHx	Total current consumption of all VH pins	7V < VUP < 27V No firing request.				
3.1-22			VHx < 27V			3	mA
3.1-23			VHx < 18V			2	mA
3.1-24	IGHx,	ton_d <sub>IGHx</sub>	Delay time between end of SPI instruction FLM_HS_ON (setting respective bits from 0 to 1) and actuation switch on level of the high side power stage. This additional delay is realized internally *)	32		48	us

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	IGHx	Switching time					
3.1-25		turn-on time firing current	0 % $\Rightarrow$ 90 %, $R_{\text{Squib}} = 2 \Omega$			50	us
3.1-26		turn-off time firing current	100 % $\Rightarrow$ 10 %, $R_{\text{Squib}} = 2 \Omega$			20	us
3.1-27	IGHx	V_IGHx	static maximum voltage			18	V
3.1-28	IGHx	I_IGHx	neg. current (without ASIC malfunction, not to be tested in series production)			-100	mA

\*) Voltage measurement at IGLx itself gives longer switch on times depending on external application.

## Application Note:

pin	parameter	condition / recommendation	min	typ	max	unit
IGHx	$L_{\text{IGH}}$	Maximum inductance allowed between IGHx and IGLx (Firing modes I, II, II, V, VI)	0		74	uH
		Inductance of low energy actuator mode (LEA, Firing mode VI)	1.2		3	mH
IGHx	$C_{\text{IGHx}}$	Capacitance at IGH	60		125	nF
IGHx	$R_{\text{IGHx-IGLx}}$	Ohmic resistance between IGHx and IGLx			10	Ohm

Further firing conditions require additional measures on system ECU and have to be defined individually.

When dimensioning the capacitances at the VHx pins please be aware of the following points:

- The maximum  $dV_{\text{VHx}}/dt$  must not be exceeded
- In case of an unsupplied ASIC and shorted ignition pins (e.g. to battery voltage), the dynamic reverse current through the high side power stage depends on  $C_{\text{VHx}}$

## 3.2 Squib Lowside Power Stage & Driver

In principle, the low side power stage acts as a switch towards ground within the firing loop. It is switched on by the SPI command *FLM\_LS\_ON* (please see chapter 3.2.2) and starts in enabled current limitation mode. If no short circuit is detected for a certain time, the current limitation mode will be disabled (please see chapter 3.2.3), but the detection circuit for the current limitation is kept active. If a short circuit is detected afterwards, the current limitation mode for the low side power stage will be enabled again until the low side power stage is switched off or locked. This short circuit detection runs separately for each low side power stage.

After the on-time, the low side power stage is switched off automatically (auto switch off function). Additional switching-on of the low side power stage does not reset the running auto-switch-off timer. The timer is only reset when the low side power stage is switched off by a SPI command *FLM\_LS\_ON* (please see chapter 3.2.2) or locked by the SPI command *FLM\_UNLOCK* (please see chapter 3.4.5).

To ensure safe and unobstructed operation during firing sequence of the low side power stage, firing and diagnosis cannot be done simultaneously. Therefore, the low side power stage can only be switched on for firing if none of the low side power stages are in diagnosis mode, or if a firing request is recognized, the diagnosis will be interrupted.

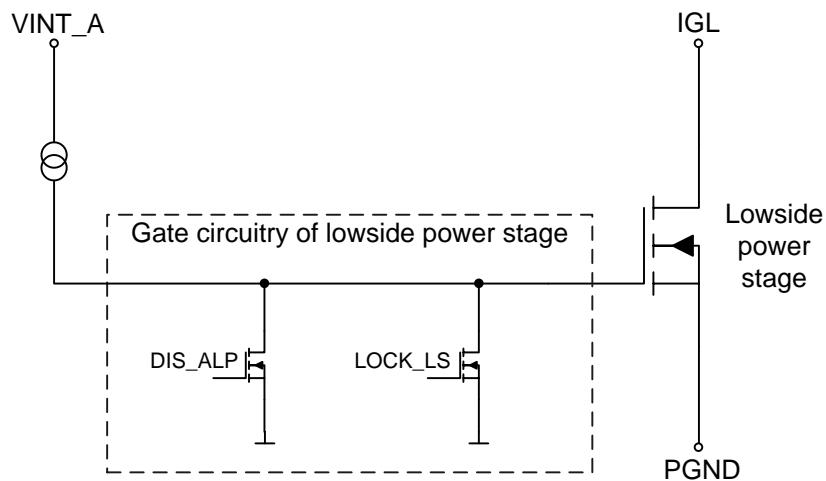
Switching-on of a low side power stage is triggered by SPI whereas the switching-off can be done either via SPI command *FLM\_LS\_ON* during an ongoing firing or hardware-triggered by the ASIC itself at the end of firing (auto-switch-off function). This auto-switch-off function is always active and cannot be disabled.

Once the low side power stage was switched on, the power stage has to be switched off before it can be switched on again. Switch-off is done by SPI command *FLM\_LS\_ON* or by locking the low side power stages.

Apart from that, switching-off of power stages by SPI command is always possible even if the auto-switch-off time has not been reached yet. In case of an additional switch-on command during the firing of a loop, the firing time is not extended and the auto-switch-off timer is not reset. The timer is only reset when the low side power stage is switched off by SPI command *FLM\_LS\_ON* or locked by SPI command *FLM\_UNLOCK*.

### 3.2.1 Squib Lowside Lock

The lowside power stage is also equipped with a locking mechanism:



The following two conditions have to be fulfilled before the lowside power stage can be switched on:

- Internal system reset (inactive high) releases locking mechanism **LOCK\_LS** only if the ASIC supply voltage are in correct regions
- internal safety module releases locking mechanism **DIS\_ALP** depending on watchdog status

In an active squib measurement mode the lowside power stages are also used as sinks for the test current.

### 3.2.2 Squib Lowside SPI Instructions

Switching of firing loop lowside power stages:

#### **SPI instruction FLM\_LS\_ON**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cx : 1 = switch-on lowside firing loop x, 0 = switch-off lowside firing loop x

# Data sheet CG904, CG903, CG902

## 3.2.3 Squib Lowside Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
3.2-1	IGLx	Idle voltage	Low side power stage is switched off	1.19	1.25	1.31	V
3.2-2	IGLx, PGNDx	RDS(ON)	Low side powers stage is switched on -40°C < Ta < 150°C	0.2	0.6	1.6	Ω
3.2-3	IGLx,	$t_{on\_d\ IGLx}$	Delay time between end of SPI instruction FLM_LS_ON (setting respective bit from 0 to 1) and actuation switch on level of the low side power stage. This additional delay is realized internally *)	16		32	us
	IGLx	Current limitation					
3.2-5	IGLx	short circuit voltage detection level at IGLx	voltage threshold just at the moment of switch on the low side	1.4		1.8	V
3.2-6	IGLx	short circuit voltage detection level at IGLx	voltage threshold during switch on the low side	5.3		5.7	V
3.2-7	IGLx	short circuit detection filter time	the time in which the short circuit threshold must be exceeded in order to recognize the short-circuit during switch on the low side		48		μs
3.2-8	IGLx	current limitation during firing mode I, II, III and V $IGLx_{cl\ I}$	Low side powers stage is switched on current limitation ( $IGLx < 18V$ )	1.2			A
	IGLx	Switch on time	Switch on time during the firing sequence				
3.2-9		$t_{on\ IGLx\ cl\ I}$	Firing mode I, II, III, V	2400		2550	us
3.2-10	IGLx	current limitation during firing mode VI $IGLx_{cl\ VI}$	Low side powers stage is switched on current limitation ( $IGLx < 18V$ )	1.5			A
	IGLx	Switch on time	Switch on time during LEA sequence				
3.2-11		$t_{on\ IGLx\ cl\ VI}$	Firing mode VI	3200		3350	us
3.2-12		$t_{on\ IGLx\ cl\ VI\ short}$	Firing mode VI continuous short	1700		1850	us
	IGLx	Switching time					
3.2-13		turn-on time $t_{on\ IGLx}$	100 % ⇒ 10 % (by SPI instruction LS_ON)		5	15	us
3.2-14		turn-off time $t_{off\ IGLx}$	0 % ⇒ 90 % (by SPI instruction LS_ON), no capacitance at IGLx		8	15	us
3.2-15	IGLx	$V_{IGLx\_max}$	static maximum voltage			18	V
3.2-16	IGLx	$I_{IGLx\_neg}$	neg. current (without ASIC malfunction, not to be tested in series production)			-100	mA

\*) Voltage measurement at IGLx itself gives longer switch on times depending on external application.

## Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
IGLx	$C_{IGLx}$	Capacitance at IGLx	60		125	nF

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## 3.3 Firing Sequence

Please consider the steps listed below for safe operation of loop firing.

Start firing:

1. ensure the supply voltages to be applied (no system reset)
2. program the firing mode with SPI command *PROG\_FLM\_MODE*
3. finish correct programming of power stages with SPI command *EOP*
4. no watchdog fault active (DIS\_ALP low)
5. crash data monitored over plausibility threshold (DIS\_AHP low)
6. unlock lowside and highside power stage by SPI command *FLM\_UNLOCK*
7. turn on lowside power stage by SPI command *FLM\_LS\_ON*
8. turn on highside power stage by SPI command *FLM\_HS\_ON*

Stop firing:

1. turn off highside power stage by SPI command *FLM\_HS\_ON* or by auto switch-off (automatic timing control active)
2. Only in case of manual switch-off: wait for at least 50 µs
3. turn off lowside power stage by SPI command *LS\_ON* or by auto switch-off (automatic timing control active)

The highside power stage has sufficient delay to the lowside power stage so that the SPI command *FLM\_LS\_ON* and *FLM\_HS\_ON* can be sent without time delay one after the other.

With inductances in the firing path, switching-off the highside and lowside power stages simultaneously can cause dangerous self-inductance voltages at IGL. Therefore it is mandatory to switch off the highside power stage first with the appropriate switch-off command and to wait for more than 50 µs before switching off the lowside power stage. If a power stage is locked (*UNLOCK*) or disabled (*DISABLE*) during firing, the firing sequence is stopped immediately. To activate the power stages again, the above sequence has to be programmed anew.

### Application Note:

While firing, the potential at the firing pins (IGHx and IGLx) increases and forces a current into VST50 through the voltage divider path (max. 20mA when firing all power stages simultaneously).

## 3.4 Safety Concept

### 3.4.1 Fail-Safe Design

In case of an active power on reset ( $N_{POR}=0$ ):

- All power stages are barred.
- Even if no supply voltages are present, an additional circuit provides proper barring of the power stages when the voltage at  $VHx$  or  $VST50$  exceeds 3 V. In order to unbar the power stages, the power on reset has to be high.
- The voltage at the ignition pins ( $IGH$ ,  $IGL$ ) is 1.25 V nominal.
- The test current source and test current sinks are switched off.
- The disable register bits are set to low level and can be programmed.
- The firing current counters contain the value 0.
- Firing mode II is set by default.
- Auto-switch-off function of highside and lowside power stages is implemented.
- Test current source is set to level A (40 mA) by default.

The safety relevant functions (e.g. to disable the power stages) are supplied independently by different supply voltages ( $VH$  and  $VINT\_A$ ). The highside power stage is supplied by the voltage at  $VHx$ , whereas the lowside power stages are supplied by  $VINT\_A$ .

### 3.4.2 General Disable

The three external pins  $DIS\_AHP$  (disable of all highside power stages),  $DIS\_SHP$  (disable special highside power stages) and  $DIS\_ALP$  (disable of all lowside power stages) allow direct disabling of the power stages completely independent of the SPI.

The highside power stages 1-4 are disabled by  $DIS\_AHP$  and  $DIS\_SHP$ , all further highside power stages 5-16 are disabled by  $DIS\_AHP$  only. With  $DIS\_SHP$  set to low the first four highside power stages are released independent of  $DIS\_AHP$ . With  $DIS\_AHP$  set to low all highside power stages are released independent of  $DIS\_SHP$ . Therefore, the first 4 highside power stages can be released by  $DIS\_SHP$  set to low while all further highside power stages are still locked by  $DIS\_AHP$  being high.

Commands for unlocking and activation of the power stages are only accepted if the respective disable pin is set to low. If a general disable pin is set to high during the activation of a power stage, the power stages will be disabled and locked immediately.

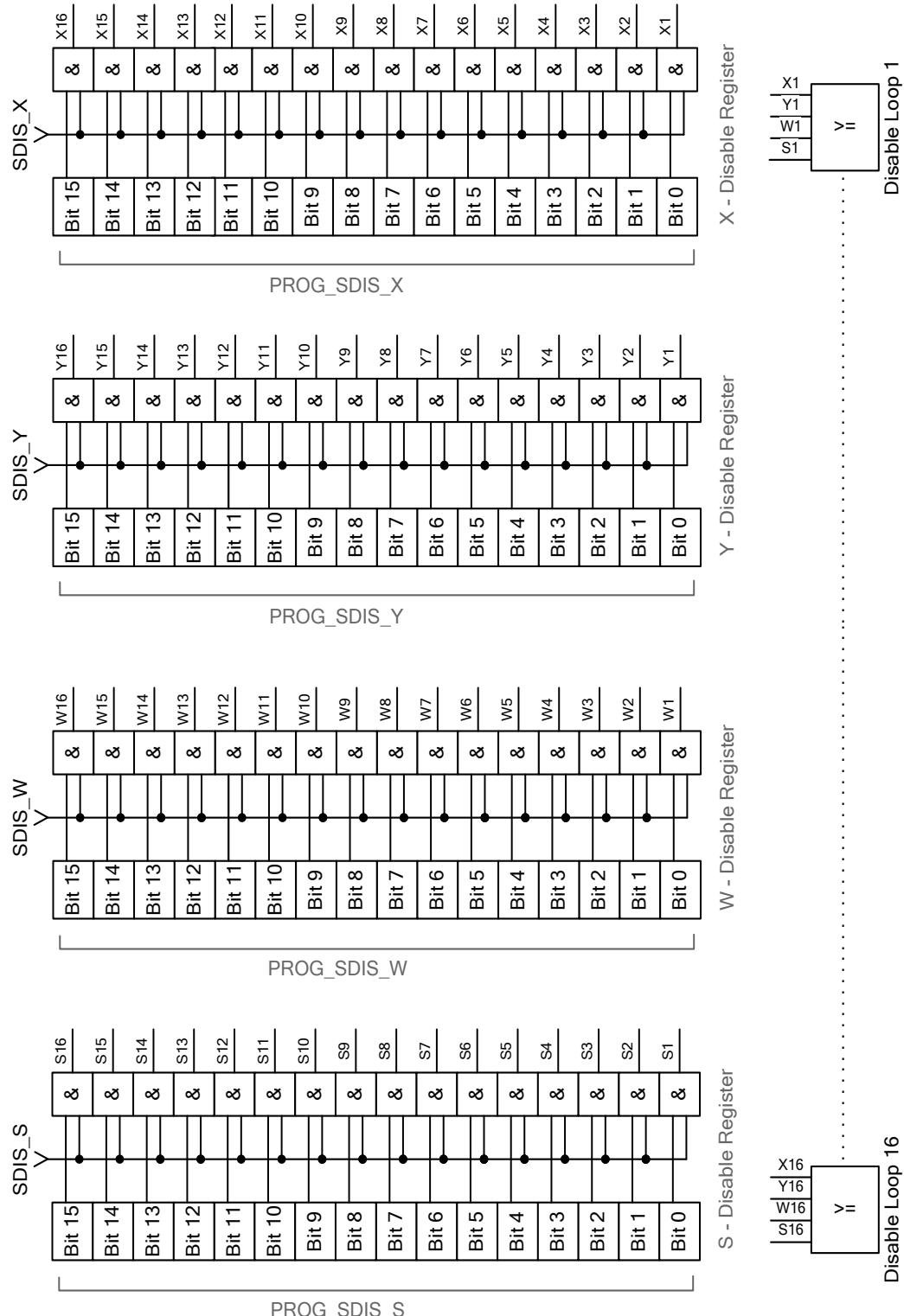
For the electrical characteristics of disable pins please see chapter "Disable Lines" on page 171.

### 3.4.3 Disable of dedicated Power Stages

For disabling of dedicated power stages (up to 16), four disable registers are implemented and programmable via SPI. If a bit of a disable register is set to logic high, the respective power stage can be disabled by these four corresponding signals:

- $SDIS\_X$  has effect on the  $SDIS\_X$  disable register. It is programmed by SPI command  $PROG\_SDIS\_X$ .
- $SDIS\_Y$  has effect on the  $SDIS\_Y$  disable register. It is programmed by SPI command  $PROG\_SDIS\_Y$ .
- $SDIS\_W$  has effect on the  $SDIS\_W$  disable register. It is programmed by SPI command  $PROG\_SDIS\_W$ .
- $SDIS\_S$  has effect on the  $SDIS\_S$  disable register. It is programmed by SPI command  $PROG\_SDIS\_S$ .

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After sending an *EOP* command, the disable registers are locked. A release can only be forced with a power on reset at pin N\_POR. Before sending an *EOP* command, all lowside power stages are disabled, but highside power stages can still be activated. Consequently, the commands for unlocking of lowside power stages are rejected.

## Application Note:

The special disable signals SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S have no effect during firing, because they are only checked with a SPI command HS\_ON at start of firing. Please pay attention when firing with multiple firing commands HS\_ON. The special disable lines can change between the firing commands due to new crash data and lead to firing breaks although using SPI command HS\_ON.

The actual status of the disable registers can be read out via SPI-commands for verification. A programming example is given here:

1. Program special disable registers with SPI command PROG\_SDIS\_X, PROG\_SDIS\_Y, PROG\_SDIS\_W and PROG\_SDIS\_S
2. Verify special disable registers with SPI command PROG\_SDIS\_X, PROG\_SDIS\_Y, PROG\_SDIS\_W and PROG\_SDIS\_S
3. Complete programming sequence and lock disable registers by EOP command

### 3.4.4 Lock and Unlock of Power Stages

In order to unlock the highside power stages, DIS\_AHP (DIS\_AHP or DIS\_SHP for the first four highside power stages) must be low. The lowside power stages can only be unlocked if the DIS\_ALP signal is low and EOP2 is set. Unlocking is done with SPI command FLM\_UNLOCK. The commands for unlocking are ignored when DIS\_AHP/DIS\_ALP are high (DIS\_AHP and DIS\_SHP for the first four power stages). The power stages are immediately locked again when DIS\_AHP/DIS\_SHP/DIS\_ALP return to high.

The SPI command FLM\_STATUS shows the current state of all DIS and SDIS pins (bits 'dx'). Furthermore, SPI command FLM\_STATUS shows the unlock state in the bit 'ull' for the lowside power stages and in the bit 'uh' for the highside power stages.

### 3.4.5 FLM Safety SPI Instructions

Program special x-disable influence:

#### SPI instruction PROG\_SDIS\_X

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

cx = 1 : firing loop x is set under control of SDIS\_X (default 0)

Program special y-disable influence:

#### SPI instruction PROG\_SDIS\_Y

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

cx = 1 : firing loop x is set under control of SDIS\_Y (default 0)

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Program special w-disable influence:

## **SPI instruction PROG\_SDIS\_W**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

cx = 1 : firing loop x is set under control of SDIS\_W (default 0)

Program special switch-disable influence:

## **SPI instruction PROG\_SDIS\_S**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

cx = 1 : firing loop x is set under control of SDIS\_S (default 0)

Lock/Unlock firing loop power stages:

## **SPI instruction FLM\_UNLOCK**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	hs ls
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

hs: 0 = highside power stages locked (default), 1 = highside power stages unlocked

ls: 0 = lowside power stages locked (default) , 1 = unlock of lowside power stages unlocked

The lock status can be read out by SPI command *FLM\_STATUS*.

## 3.5 Squib Diagnosis

The firing loop module contains a number of features for high precision firing loop diagnoses:

- automatic short detection on all IGH and IGL pins to detect short circuits or leakage resistors to battery or ground
- automatic voltage measurement on the VHx pins
- a test to ensure the ignitability of the power stage
- automatic cross coupling test to detect short circuits between the firing loops
- automatic connector capacitor test to check the capacity in the firing loops
- automatic determination of the squib resistance
- automatic squib detection test to find an open load

SPI commands for starting and configuring these diagnoses are PROG\_FLM\_CONF, FLM\_START\_DIAG, and FLM\_DIAG\_MASK.

With SPI command PROG\_FLM\_CONF the short detection mode, the test current level and the turn-on time for the squib resistance measurement can be adjusted. By setting a continuous short detection mode, the automatic short detection on all IGH and IGL pins is activated.

The automatic short detection runs until another diagnosis is started by SPI command FLM\_START\_DIAG. In this case, the automatic short detection and its processing is interrupted so that the requested diagnosis can be started. With the end of the requested diagnosis, the automatic short detection is restarted.

Generally, only one diagnosis can be run at a time so as to avoid resource conflicts within the ASIC. For this reason, the request for a new diagnosis is ignored if any diagnosis other than the automatic short detection is already running. A running diagnosis is indicated by the ‘run’ bit in SPI command FLM\_START\_DIAG or, in general, by the status bit ‘BSY1’ in any of the other SPI commands. A running diagnosis can be stopped early with SPI command FLM\_START\_DIAG set to mode “0000” (stop diagnosis).

Furthermore, each running diagnosis is immediately interrupted, when a regular ignition is requested. The regular ignition is detected after EOP2 is set, the highside power stage is unlocked and either one of the SPI commands FLM\_LS\_ON or FLM\_HS\_ON are received.

With the SPI command FLM\_DIAG\_MASK individual channels can be excluded from certain diagnoses.

### 3.5.1 Detection of Short Circuits and Leakage Resistors

Detection of short circuits or leakage resistors at the firing pins is crucial for proper squib firing. Therefore, the quiescent potential at all 32 IGH and IGL pins is checked by two integrated comparators. Each firing pin is equipped with a voltage divider providing a defined quiescent potential of nominal 1.25 V. Short circuits or leakage resistors lead to voltages at IGH or IGL that are different from this value. This deviation can be detected by the comparators, where one of the comparators detects deviations to larger and one to smaller values than the quiescent potential.

There are two detection thresholds that can be selected for the comparator which detects voltages larger than the quiescent potential. The selection is made with the short detection mode ‘sd\_mde’ in SPI command PROG\_FLM\_CONF. Simultaneously with the programming of ‘sd\_mde’, the automatic short circuit detection is deactivated or activated in case a threshold is set. If the detection is activated and not interrupted by another diagnosis, all IGH and IGL pins are checked over a period of 550 µs after which the automatic short circuit detection is restarted automatically.

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The continuously updating values can be read out with the following SPI commands:

FLM\_READ\_SHORT1 returns the short information: potentials lower than undervoltage threshold on IGH pins

FLM\_READ\_SHORT2 returns the short information: potentials higher than overvoltage threshold on IGH pins

FLM\_READ\_SHORT3 returns the short information: potentials lower than undervoltage threshold on IGL pins

FLM\_READ\_SHORT4 returns the short information: potentials higher than overvoltage threshold on IGL pins

(all bits indicate the current state at the pins)

## 3.5.2 Voltage measurement on VHx pins

The power supply to the VHx pins is critical part to the firing of the squibs.

In order to control the supply on the VHx pins, there is an automatic voltage measurement at the VHx pins. This diagnosis measures the voltage of a resistive divider at the VHx pin through an internal ADC.

This automatic measurement can be started for a single VH pin or for all eight VHx pins. To start the diagnosis, SPI command FLM\_START\_DIAG is used with diagnose mode "0001". Configuration bits 'conf' define which VHx is measured. With the lower three configuration bits, a single VHx measurement can be selected. When the fourth bit is set, all eight VHx pins are measured in succession. A measurement on all eight VHx pins needs a maximum time of 4.25ms and terminates automatically. If only a single channel is selected, the measurement needs a maximum time of 0.75ms and terminates automatically.

The result of the voltage measurement of VHx can be read out with SPI command FLM\_READ\_VHx. The measured voltage at the VHx pin is stored in bits 'adc\_data'. The valid bit 'vd' shows whether the voltage was measured again since the last read out.

1 LSB = 47,6mV VH voltage

## 3.5.3 SVR diagnosis with voltage measurement at VHx pins

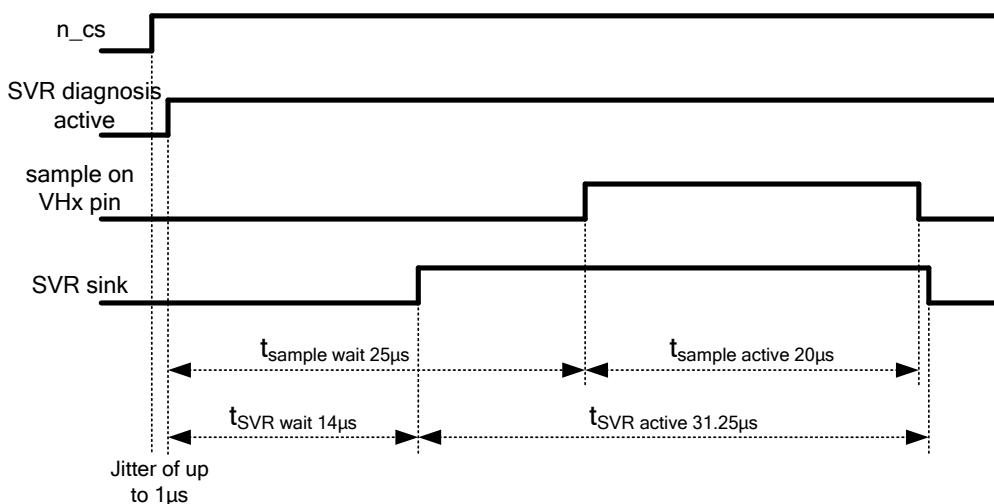
The SVR (safety voltage regulator) act like a switch between VER supply and VHx supply and is controlled by the uController in the air bag system. The SVR diagnosis test the switch on and switch off function of the SVR. This diagnosis measures the voltage at a VHx pin with the help of the internal ADC, similar to the VHx pin voltage measurement diagnosis. The difference with this SVR diagnosis is the detection method of the voltage at the VHx pin. The voltage at the VHx pin is sampled immediately at the start of this diagnosis, after a very short time. The sampled voltage is measured by the ADC at a later time. Furthermore, it is possible to switch on a current sink at the SVR pin during the sampling at the VHx pin.

The SVR diagnosis can be started with SPI command FLM\_START\_DIAG in diagnose mode "0010". The lower three configuration bits 'conf' define which VHx is measured. When the fourth bit is set, the current sink at the SVR pin is activated and the voltage at the VHx pin is sampled. The current sink output is accessible at pin SVR\_DIAG and must be connected to the VHx lines which are supplied by the SVR.

If the measurement is started via SPI (rising edge on N\_CS), it can come to a jitter of up to 1µs due to synchronization effects. 25µs after the start of the diagnosis, the voltage at VHx pin is sampled with a separate sample module for 20µs. This separate sample module stores the

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voltage until the internal ADC measures the voltage from the separate sample module. The SVR diagnosis needs a maximum time of 750 $\mu$ s and terminates automatically. When the SVR sink is additionally activated, the SVR sink is switched on after 14 $\mu$ s and stays active for 31.25 $\mu$ s.



The result of the voltage measurement of VHx can be read out with SPI command FLM\_READ\_SVR. The measured voltage value at the VHx pin is binary coded stored in bits 'adc\_data'. The valid bit 'vd' shows whether the voltage was measured again since the last read out.

## 3.5.4 Power Stage diagnosis

The functionality of the firing power stages is very important for the airbag system. To test the firing power stages without risk, the power stage diagnosis was implemented. The diagnosis ensures that the output stages are only switched on for a duration long enough to be tested but short enough to guarantee that they do not lead to an ignition.

The power stage diagnosis can be started with SPI command FLM\_START\_DIAG in diagnose mode "0011". Configuration bits 'conf' are used to define which firing power stage is validated. With the lower four configuration bits, a firing loop channel can be selected. If the fifth bit is set to 1, the lowside power stage of the selected loop is validated, otherwise the highside power stage is validated.

With the start of the diagnosis the internal comparators are switched to the selected firing power stage, the shortened ignition is activated and SPI command FLM\_HS\_ON or FLM\_LS\_ON is awaited. Then the uController needs to start an ignition cycle to complete the power stage test. In this state, the bit 'tso' is set, showing that the power stage diagnosis is active and a real ignition is prevented by a fast switch-off of the power stage. The bit 'tso' can be read out with SPI commands FLM\_READ\_PST or FLM\_STATUS.

It is strongly recommended, to verify the bit 'tso' before an SPI command is sent to turn on a power stage. If this bit is not set, ignition occurs in full lengths. Otherwise a regular ignition is interrupted prematurely by the diagnosis. The activation of the power stage diagnosis mode is done with the processing of the SPI command FLM\_START\_DIAG without further delay.

As soon as the SPI commands FLM\_HS\_ON or FLM\_LS\_ON are received from uController, the selected firing power stage is diagnosed. For this purpose, the selected power stage is checked

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for short circuits in advance with IGHx and IGLx voltage comparators. Should a short circuit be detected, the ignition is immediately interrupted and terminated with the corresponding fault entry in the diagnosis result.

If no short circuit is detected in advance, the power stage is switched on. During switch on, the voltage at the power stage pin is continuously monitored. If, in the course of this diagnosis, the voltage at the tested pin decreased under or increases over the short detection thresholds around the quiescent potential in highside or lowside diagnosis, respectively, a short circuit is detected and the power stage is immediately switched off.

If the low side power stage output IGLx fall below under a voltage threshold during a determined time and the corresponding high side power output stage IGHx increase over a voltage threshold during a determined time, the power stage will be regarded as functional and will be switched off immediately. If none of the lowside or highside diagnosis thresholds are crossed within the maximum activation time, the power stage is switched off to ensure safety.

In order to detect a functioning highside power stage, the threshold of 4,3V is expected to be crossed within 85 $\mu$ s (highside time out) after switching on the power stage.

In order to detect a functioning lowside power stage, the threshold of 0,5V is expected to be crossed within 35 $\mu$ s (lowside time out) after the switching on the power stage.

The power stage test ends with switch off the chosen high and low side power stages and must be started again for a new power stage diagnosis. The result of the power stage diagnosis can be read out with SPI command FLM\_READ\_PST. It is sensible to read this result directly after the start of the diagnosis. In this case, the bit 'tso' will be set, which indicates that the power stage diagnosis is active, the 'short\_info' bit shows that a short circuit is already present at start of the diagnosis and the output stage where not activated.

After the diagnosis is finished the 'tss' bit indicates whether the output stages were switched off prematurely. The bits 'diag\_result' indicate the reason for early switch-off and thus reflect the status of the firing power stage.

## 3.5.5 Cross coupling diagnosis

In addition to short circuits to other voltage potentials, shorts circuits between the firing pins are critical. To find these, a cross coupling diagnosis is implemented in the ASIC. This diagnosis monitors all firing loops and while this diagnosis is running, the quiescent voltage potential at the firing loops are sequentially stimulated to detect influences on other firing loops. In order to secure larger systems with more than one system ASIC, this diagnosis is available in two modes. There is a master mode in which an ASIC stimulates and monitors itself, and there is a slave mode in which the ASIC monitors itself only.

The cross coupling diagnosis in master mode can be started with SPI command FLM\_START\_DIAG in diagnose mode "0100". This diagnosis stimulates all 16 channels sequentially. Individual channels can be excluded from being stimulated with SPI command FLM\_DIAG\_MASK.

With the start of the diagnosis, the firing loops are tested in advance for short circuits and leakage resistors at IGHx and IGLx. If a short circuit is detected at a firing loop, this firing loop is excluded from the diagnosis and is not stimulated. If no short circuit is detected the test proceed in stimulation of this firing loop automatically. The test current sink is now activated on the first low side powers stage for 200us.

Subsequently, the quiescent voltage of all other firing loops is monitored, as is the case during the detection of short circuits. Once a firing loop that has not been stimulated is detected to be influenced, the result is displayed as a short circuit in the monitored firing loop. This procedure is repeated across all 16 channels.

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As long as the cross coupling diagnosis is running, the FRB (bit 23) and BSY1 (bit24) flags in the SPI status and “run” bit in the FLM\_STATUS is set to logic 1. If the electrical stimulations of the output powers stages are passed, the FRB flag in the SPI status is set to logic 0, while the BSY1 flag stays at logic1. The cross coupling test sequence is now in waiting situation as long as the uController requests the results which are stored in FLM\_READ\_CC.

This is the condition, in which the cross coupling diagnosis is finished. The BSY1 flag in the SPI status will be set to logic 0, so that other test sequences can be started.

A firing request interrupt the cross coupling diagnosis immediately.

The cross coupling diagnosis in slave mode can be started with SPI command FLM\_START\_DIAG in diagnose mode “0101”. This diagnosis does not stimulate the channels; it only monitors the quiescent voltage on all firing loops. It is similar to the master mode in that when the voltage at a monitored firing pin falls below the detection threshold a short circuit is detected and displayed in the result as a short circuit to the monitored firing loop.

The cross coupling diagnosis in slave mode does not terminate automatically. It is terminated by SPI command FLM\_READ\_CC, as is the case in the diagnosis in master mode. The FLM run bit (“FRB” in the SPI status or “run” in FLM\_STATUS) is not set to high during the diagnosis in slave mode. Therefore, the diagnosis can be terminated at any given time.

The cross coupling diagnosis in master mode needs a maximum time of 66ms for the stimulation of firing pins. With the end of the diagnosis (through SPI command FLM\_READ\_CC) the ‘BSY1’ bit in the SPI status bits is set to low and it is possible to start a new diagnosis.

The result of cross coupling diagnosis can be read out with SPI command FLM\_READ\_CC. A set bit to logic high indicates that this firing loop has been influenced during the diagnostic time.

Additionally, the detected shorts circuits to potentials higher and lower than the quiescent voltage potential are latched in the registers from SPI commands FLM\_READ\_SHORTx and therefore do not reflect the current state, as long as the cross coupling diagnosis is active. The registers will not be deleted if they are read out by SPI commands FLM\_READ\_SHORTx at this time. With the end of the cross coupling diagnosis (through SPI command FLM\_READ\_CC), these registers reflect the current state and are replaced by the next short detection check (back-to-normal behavior).

The detection of cross coupled channels uses the same thresholds than the detection of short circuits and leakage resistors.

## 3.5.6 Connector capacitor diagnosis

The connector capacitor diagnosis allows determining the timing behavior which results because of a capacitive load on a firing loop. A respective test current sink is switched on and switched off again to IGLx. The time needed to reach a voltage level of 0,9V (threshold of short to minus comparator) after switching off again is measured.

The connector capacitor diagnosis can be started with SPI command FLM\_START\_DIAG in diagnose mode “0110”. This diagnosis stimulates all 16 channels sequentially. Individual channels can be excluded with the SPI command FLM\_DIAG\_MASK from the stimulation.

With the start of the diagnosis, the firing loops are tested in advance for short circuits and leakage resistors at the IGHx and IGLx. If a short circuit is detected at a firing loop, then this firing loop is excluded from the diagnosis and is not stimulated. If no short circuit is detected the test proceed automatically.

The test current sink of the first low side power stage is now switched on for a certain time. During switch on both IGHx and IGLx a capacitance at these pins are discharged and charged again after switch off to the former quiescent voltage with the input resistance of the voltage

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divider at IGHx and IGLx. The time that is needed to cross the threshold voltage is measured. If the voltages don't cross the threshold voltage, the measurement stops after 1ms. This procedure is repeated across all 16 firing loops channels and their respective IGH and IGL pins.

As long as the connector capacitance diagnosis is running, the "FRB" bit (FLM run bit) in the SPI status bits and the "run" bit in the SPI command FLM\_STATUS are set. With the end of the stimulation of all channels, these bits are both set back to low. This diagnosis, however, is not terminated automatically. The diagnosis is terminated by SPI command FLM\_READ\_CAP when the FLM run bit is low.

The complete connector capacitor diagnosis over all firing loops needs a maximum time of 21ms. The actual run time is strongly dependent on the capacitive loads. The larger the load, the longer the run time. With the end of the diagnosis (through SPI command FLM\_READ\_CAP) the 'BSY1' bits in the SPI status bits is set to low, and it is possible to start a new diagnosis.

The result of the connector capacitor diagnosis can be read out with SPI command FLM\_READ\_CAP. The return values are the maximum ('cap\_time\_max') and minimum ('cap\_time\_min') recorded time over all stimulated loops. One LSB corresponds to 4 $\mu$ s.

Additionally, the detected shorts circuits to potentials higher and lower than the quiescent potential are latched in the registers from SPI commands FLM\_READ\_SHORTx and do not reflect the current state, as long as the connector capacitor diagnosis is active. The registers will not be deleted when they are read out by SPI commands FLM\_READ\_SHORTx at this time. With the end of the connector capacitor diagnosis (through SPI command FLM\_READ\_CAP), these registers reflect the current state and are replaced by the next short detection check (back-to-normal behavior).

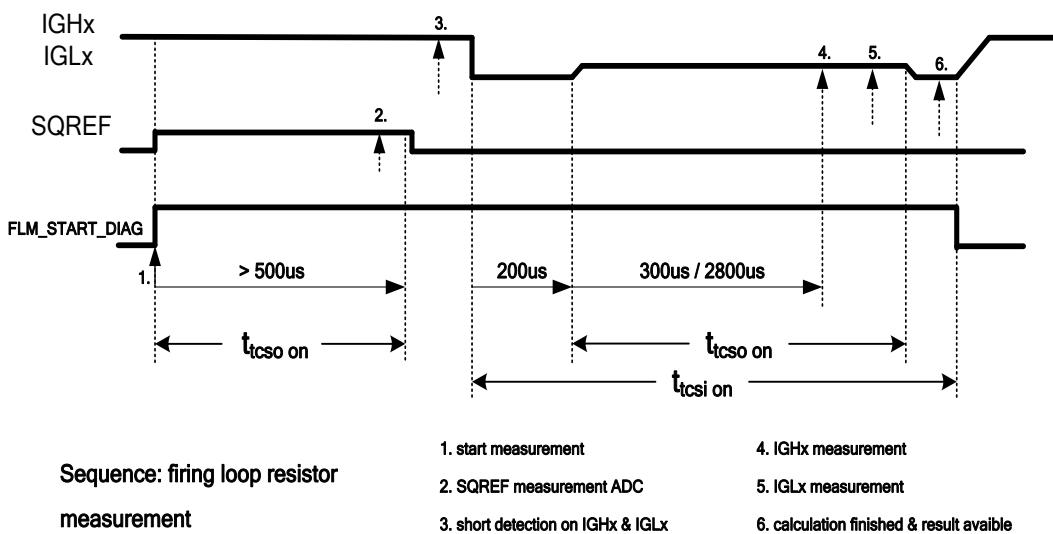
## 3.5.7 Firing loop resistor measurement

Monitoring of the firing loop resistance is important for a reliable and safe operation of an airbag system. A known test current (small compared to the firing current) is therefore sent through the squib resistor and through a known reference resistor. The used loop consists of a test current source, the squib resistor and a test current sink (lowside power stage). The resulting voltage drop across the squib resistor is measured by the internal ADC at the firing pins with an internal typical amplification factor of 5. The result is proportional to the measurement of the know reference resistor and can be read out via SPI to display the information about the value of the squib resistance. The result is a digital relationship between the know test resistance and the squib resistance.

This ASIC contains one test current source and a current limitation mode for the 16 lowside power stages (working as test current sinks) for the measurement of the squib resistance at 16 firing loops. For each firing loop resistor measurement, the test current source is activated via pin SQREF and the voltage drop across the squib resistors is put into relation to the voltage drop across the SQREF resistor.

Block diagram for firing loop squib resistance measurement:

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There are two current levels of test current programmable by SPI command PROG\_FLM\_CONF with the 'tcl' bit (nominal 40mA or 60mA). Also, in the SPI command PROG\_FLM\_CONF the bit 'tr' can be set to increase the measurement cycle time. This extends the time between the activation of the test current and the measurement by the internal ADC. This is recommended when the ignition circuits include very high inductances (e.g. LEA module).

The firing loop resistor measurement can be started with SPI command FLM\_START\_DIAG in diagnose mode "1000". This diagnosis is sequentially on all 16 channels. Individual channels can be excluded from the measurement with SPI command FLM\_DIAG\_MASK. The excluded channels are neither stimulated nor measured.

With the start of the diagnosis, the first step is to switch on the test current source with the current flowing out of the SQREF pin and to measure the voltage drop over the external SQREF resistor with the internal ADC. The following step is a short detection test at the first firing loop, as in the case of the short circuit or leakage resistor diagnosis at the firing pins. If a short circuit is detected at a firing loop, then this firing loop is excluded from the diagnosis and is not stimulated. Otherwise the ASIC stimulates this firing loop automatically.

The next step of the ASIC is to activate the test current sink on the first lowside power stage. Subsequently, the test current source is switched to the first highside power stage pin with the selected test current after  $200\mu s$ . A waiting period follows to allow for settling. This period is  $300\mu s$  long in the default state (bit 'tr' is low in SPI command PROG\_FLM\_CONF). When the 'tr' bit is set to high, the waiting duration is  $2800\mu s$  to get through the settling process. Subsequent to the waiting period, the voltages at highside and lowside power stage pins are measured by the internal ADC.

Finally, the measurement results are evaluated and the test current source and test current sink are switched off. This procedure is repeated across all 16 channels.

The firing loop resistor measurement needs a maximum time of 17.5ms or 65.5ms in case the measurement cycle is increased via bit 'tr' in SPI command PROG\_FLM\_CONF and terminates automatically.

The results of the firing loop resistor measurement can be read out with SPI command FLM\_READ\_RES1...16. The calculated resistance value at each firing loop is stored in the bits 'res\_value'. One LSB corresponds to the 1/1024 part of the resistor on the SQREF pin. The valid bit 'vd' shows whether the voltage was measured again since the last read out.

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If the measurement is not completed due to an implausible event, there is a fail code that depends on the event in four bits 'flt' in SPI command PROG\_FLM\_CONF. These fail codes have the following meaning and are sorted by priority.

Implausible event at voltage measurement on SQREF pin:

- flt: 0010 <= the measured voltage at SQREF pin is to low
- flt: 0011 <= the measured voltage at SQREF pin is to high

Short circuit at the firing loop pins:

- flt: 1000 <= lowside has a shorted-circuit to ground and the voltage at VZP is higher VZP\_L
- flt: 1100 <= lowside has a shorted-circuit to ground and the voltage at VZP is lower VZP\_L
- flt: 1001 <= lowside has a shorted-circuit to plus and the voltage at VZP is higher VZP\_L
- flt: 1101 <= lowside has a shorted-circuit to plus and the voltage at VZP is lower VZP\_L
- flt: 1010 <= highside has a shorted-circuit to ground and the voltage at VZP is higher VZP\_L
- flt: 1110 <= highside has a shorted-circuit to ground and the voltage at VZP is lower VZP\_L
- flt: 1011 <= highside has a shorted-circuit to plus and the voltage at VZP is higher VZP\_L
- flt: 1111 <= highside has a shorted-circuit to plus and the voltage at VZP is lower VZP\_L

Implausible event at voltage measurement on firing loop pin:

- flt: 0100 <= the measured voltage at highside pin is too high
- flt: 0101 <= the measured voltage at lowside pin is too high
- flt: 0111 <= the measured voltage at lowside pin is higher than at highside pin
- flt: 0110 <= the calculated firing loop resistor is more than two times greater than the resistor at the pin SQREF

## 3.5.8 Firing loop squib detection diagnosis

Checking the connection in the firing loop is important for reliable and safe operation of an airbag system, if not already done by the monitoring of the firing loop. This diagnosis is used to investigate the connection between the highside power stage pin and the lowside power stage pin, but it does not determine the resistance.

This diagnosis has a similar sequence as the firing loop resistor measurement, but the test current is not activated and the evaluation is performed with a comparator instead of the internal ADC. The connection in the firing loop is checked by switching the test current sink to the lowside pins and monitoring the highside pins through a comparator.

The firing loop squib detection can be started with SPI command FLM\_START\_DIAG in diagnose mode "1001". This diagnosis is run sequentially on all 16 channels. Individual channels can be excluded from the diagnosis with SPI command FLM\_DIAG\_MASK. The excluded channels are neither stimulated nor monitored.

With the start of the diagnosis, the firing loops are tested for short circuits and leakage resistors at the firing pins. If a short circuit is detected at a firing loop, then this firing loop is excluded from the diagnosis and is not stimulated. Otherwise the ASIC stimulates this firing loop automatically. In the next step, the test current sink is activated on the first lowside power stage. Subsequently, the voltage at the first highside power stage pin is monitored with internal comparator after 200µs. Finally, the test current sink is switched off and the procedure is repeated across all 16 channels.

The firing loop squib detection needs a maximum time of 4ms and terminates automatically. The result of the firing loop squib detection can be read out with SPI command FLM\_READ\_SQB. If the 'cx' bit is set to high the connectivity could not be confirmed.

### 3.5.9 Combined diagnosis

To simplify the cyclic diagnoses, a combined diagnosis is provided. There is a choice of two possible combinations.

The first possibility is the combination of the automatic voltage measurement on all VHx pins and the automatic firing loop resistor measurement. This diagnosis combination can be started with SPI command FLM\_START\_DIAG in diagnose mode "1010". The diagnoses are exactly as described above in the case of separately started diagnoses, both the voltage measurement on all VHx pins and the firing loop resistor measurement. They are executed sequentially one by one and the results can be read out as described in the respective diagnosis chapter. The combined diagnosis needs a maximum time of 21.5ms or 69.25ms when the measurement cycle time is increased with the bit 'tr' in SPI command PROG\_FLM\_CONF and terminates automatically.

The second possibility is the combination of the automatic voltage measurement on all VHx pins and the automatic firing loop squib detection. This diagnosis combination can be started with SPI command FLM\_START\_DIAG in diagnose mode "1011". The diagnoses are exactly as described above in the case of separately started diagnoses, both the voltage measurement on all VHx pins and the firing loop squib detection. They are executed sequentially one by one and the results can be read out as described in the respective diagnosis chapter. The diagnosis needs a maximum time of 8.25ms and terminates automatically.

### 3.5.10 Diagnosis self test

To verify the functionality of the short circuit detection at the firing pins, there are two other diagnostic modes. With these diagnoses short circuits can be stimulated, to check the analog comparators monitoring the thresholds around the quiescent potential, their connection to the digital circuitry and the digital evaluation.

To verify the detection of short circuits to voltage potentials higher than the quiescent voltage potential, the diagnosis is started with SPI command FLM\_START\_DIAG in diagnose mode "1101". And to verify the detection of short circuits to voltage potentials lower than the quiescent potential, the diagnosis is started in diagnose mode "1100".

If one of the two self tests diagnoses is started, the running short circuit detection at the firing pins is not interrupted. Internally, the firing pins are stimulated to potentials higher and lower than the quiescent potential. By reading out the corresponding SPI commands FLM\_READ\_SHORTx, it can be checked if a short circuit is detected correctly.

This diagnosis does not end automatically; it must be terminated with SPI command FLM\_START\_DIAG in diagnose mode "0000".

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## 3.5.11 LEA diagnosis

The diagnosis for low energy actuators (LEA) allows the detection of the polarity reversal of the free-wheeling diode.

The evaluation is automatically performed during the firing loop resistor measurement. The assessment is based on the voltage at IGHx while the test current source is activated. When the free-wheeling diode polarity is detected to be correct, the corresponding cx bit in the SPI command FLM\_READ\_IGH is set to high. If the voltage at the IGHx pin was not sufficiently high, the polarity reversal is detected, and the corresponding cx bit is set to low.

## 3.5.12 Squib Diagnosis SPI Instructions

Read firing loop module status:

### SPI instruction FLM\_STATUS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
SPI output data	0	0	0	tss	tso	run	dh	ull	ulh	d6	d5	d4	d3	d2	d1	d0

dx : 0 = corresponding powerstages are not disabled, 1 = active disabled

x=6...0 : DIS\_ALP / DIS\_AHP / DIS\_SHP / SDIS\_X / SDIS\_Y / SDIS\_W / SDIS\_S

ulh : highside is unlocked

ull : lowside is unlocked

dh : DIS\_AHP history flag (read and clear)

run : diagnosis (cross coupling test or connector capacitor test) is running

tso : powerstage testmode is active

tss : powerstage testmode auto switch-off (during power stage test) is set (read and clear)

Program firing loop configuration:

### SPI instruction PROG\_FLM\_CONF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	tr	tcl	sd_mde
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	tr	tcl	sd_mde

sd\_mde : short detection mode

00/11 = continuous short detection diagnosis not running (default)

01 = short detection threshold voltage = 2.5V (to fulfill requirements typ. 20kOhm/14V)

10 = short detection threshold voltage = 4.0V (to fulfill all other requirements)

tcl : test current level : 0 = low current level (40mA), 1 = high current level (60mA), (default = 0)

tr : turn-on time for FLM resistance measurement : 0=short (default), 1=long (for LEA mode)



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Start firing loop diagnosis:

## **SPI instruction FLM\_START\_DIAG**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	conf					mode			
SPI output data	0	0	0	tss	tso	run	dh	ull	ulh	d6	d5	d4	d3	d2	d1	d0

mode:

0000 = stop diagnosis

0001 = VHx measurement (VHx measured by ADC)

conf = VHx measurement selection (single channel or all channels)

6...4 : VHx selection, 7 : 1 = all

0010 = SVR test mode

conf = VHx measurement selection (single), SVR\_DIAG current sink on/off

6...4 : VHx selection, 7 : 1 = SVR\_DIAG current sink on

0011 = Power stage test mode (enables highside test and lowside test)

conf = loop and highside/lowside information

8 : 0 = highside, 1 = lowside

7...4 : channel selection 1...16

0100 = Cross coupling test master mode (channels can be masked by FLM\_DIAG\_MASK)

0101 = Cross coupling test slave mode / buffered short detection (runs continuously)

0110 = Connector capacitor test mode (channels can be masked by FLM\_DIAG\_MASK)

1000 = firing loop resistor measurement (channels can be masked by FLM\_DIAG\_MASK)

1001 = firing loop squib detection test (channels can be masked by FLM\_DIAG\_MASK)

1010 = start mode 0001 and mode 1000

1011 = start mode 0001 and mode 1001

1100 = short circuit diagnosis to test the detection of low voltages (runs continuously)

1101 = short circuit diagnosis to test the detection of high voltages (runs continuously)

1111 = manual diagnosis mode (this is intended for the ASIC internal production test only)

The SPI instruction FLM\_START\_DIAG is ignored in case of an undefined mode.

During firing, all diagnosis are stopped immediately (except the power stage test).

For SPI output data definition please see SPI instruction FLM\_STATUS (read-and-clear flags are cleared by SPI instruction FLM\_STATUS only).

Set firing loop diagnosis mask:

## **SPI instruction FLM\_DIAG\_MASK**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cx : 1 = firing loop x disabled for automatic measurement (default 0)

This mask refers to the diagnosis modes defined by SPI instruction FLM\_START\_DIAG.

This mask does not refer to the short detection diagnosis and to the power stage test.

This instruction is ignored during a busy FLM diagnosis (BSY1, FLM busy).



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Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_RES1...16**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	fit				vd	res_value										

Diagnosis result for diagnosis mode 1000 and 1010 (resistor measurement):

res\_value : calculated resistance value ((V\_IGH - V\_IGL) / V\_SQREF, 1 LSB=R\_SQREF/1024)

vd : valid : 1 = data are valid, 0 = data are old or invalid

fit (sorted by priority):

0010 = SQREF too low (ADC value < 200)

0011 = SQREF too high (ADC value > 1000)

1x00 = lowside shorted to ground, x: 0=VBAT OK, 1=VBAT too low

1x01 = lowside shorted to battery, x: 0=VBAT OK, 1=VBAT too low

1x10 = highside shorted to ground, x: 0=VBAT OK, 1=VBAT too low

1x11 = highside shorted to battery, x: 0=VBAT OK, 1=VBAT too low

0100 = highside voltage too high (ADC value > 1000)

0101 = lowside voltage too high (ADC value > 400)

0111 = lowside voltage >= highside voltage

0110 = res\_value too high (internal divider overflow, result  $\geq 2$ )

0000 = no fault

The channel address is coded within the least 4 bits of the instruction.

Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_VH1...8**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	0	0	0	0	0	0	vd	adc_data								

Diagnosis result for diagnosis mode 0001, 1010 and 1011 (VH measurement):

adc\_data : adc result (VH voltage divider, 1 LSB = 47.6mV)

vd : valid : 1 = adc data are valid, 0 = adc data are old or invalid

The channel address is coded within the least 3 bits of the instruction.

Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_CAP**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	cap_time_max								cap_time_min							

Diagnosis result for diagnosis mode 0110 (connector capacitor test):

cap\_time\_min: minimal time of cap test of all loops (default FF)

cap\_time\_max: maximal time of cap test of all loops (default 0)

The registers will be cleared by starting a new cap test (set to default values).

The instruction FLM\_READ\_CAP stops the connector capacitor test. The time base is 4us.

The result values are invalid during test and must be read after test only.

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Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_PST**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	vzl	0	0	tss	tso	run	0	0	short_info			diag_result				

Diagnosis result for diagnosis mode 0011 (power stage test):

short\_info (actual status):

7 : highside short to battery

6 : highside short to ground

5 : lowside short to battery

4 : lowside short to ground

diag\_result (tso = 1, during power stage test):

3...0 : 0000

diag\_result (tso = 0, after power stage test):

3 : short to battery during test detected

2 : short to ground during test detected

1 : time out

0 : power stage test OK

run : diagnosis (cross coupling test or connector capacitor test) is running

tso : powerstage testmode is active

tss : powerstage testmode auto switch-off (during power stage test) is set (read and clear)

vzl : 1 = VZP too low, 0 = VZP OK (status at the moment of shortcut evaluation)

diag\_result will be cleared by starting a new power stage test.

Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_SVR**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	0	0	0	0	0	vd	adc_data									

Diagnosis result for diagnosis mode 0010 (SVR test):

adc\_data : adc result (VH voltage divider, 1 LSB = 47.6mV)

vd : valid : 1 = adc data are valid, 0 = adc data are old or invalid

Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_CC**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

Diagnosis result for diagnosis mode 0100 and 0101 (cross coupling test):

cx : 0 = no error, 1 = cross coupling error in channel x

The instruction FLM\_READ\_CC stops the cross coupling test (in master mode only if run bit=0).

The registers will be cleared by starting a new cross coupling test.

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Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_SQB**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

Diagnosis result for diagnosis mode 1001 and 1011 (squib detection test):  
cx : 0 = squib detected, 1 = squib detection error in channel x

The registers will be cleared by starting a new squib detection test.

Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_SHORT1...4**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

FLM\_READ\_SHORT1 : 0 = no error, 1 = highside short to ground  
FLM\_READ\_SHORT2 : 0 = no error, 1 = highside short to battery  
FLM\_READ\_SHORT3 : 0 = no error, 1 = lowside short to ground  
FLM\_READ\_SHORT4 : 0 = no error, 1 = lowside short to battery

c0...c15: FLM channel (IGx1...IGx16)

During diagnosis mode 0100 and 0101 (cross coupling test modes) and 0110 (connector capacitor test mode): information buffered. In any other diagnosis mode diag\_result is the actual status.

The diagnosis register address is coded within the least 2 bits of the instruction.

Read firing loop diagnosis result:

## **SPI instruction FLM\_READ\_IGH**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI output data	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

c0...c15: FLM channel (IGx1...IGx16) : 1 = V\_IGH > 0.9V

Active during diagnosis mode 1000 and 1010 (firing loop resistor measurement) and test current source switched on.



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## 3.5.13 Squib Diagnosis Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
3.5-1	IGHx, IGLx quiescent voltage	quiescent voltage	no diagnosis active	1.19	1.25	1.31	V
3.5-2		R <sub>PU_IGxx</sub>	pull-up resistor to VST50	12	15	18	kΩ
3.5-3		R <sub>DN_IGxx</sub>	pull-down resistor to GND	4	5	6	kΩ
3.5-4		R <sub>o_IGxx</sub>	equivalent input resistance	3.0	3.75	4.5	kΩ
3.5-5	IGHx, IGLx currents sources	I <sub>TCS1</sub>	test current source level A	54	60	66	mA
3.5-6		I <sub>TCS2</sub>	test current source level B	36	40	44	mA
3.5-7		t <sub>set1</sub>	settling time PROG_FLM_CONFIG bit [3]=0		300		us
3.5-8		t <sub>set2</sub>	settling time (for LEA mode) PROG_FLM_CONFIG bit [3]=1		2800		us
3.5-9		I <sub>TCSI</sub>	test current sink	85		120	mA
3.5-10		T <sub>d_TCS</sub>	time delay between sink and source		200		us
3.5-11	IGHx, IGLx voltage comparators	V <sub>TH1-A</sub>	voltage threshold for short circuit (sd_mde=01 in PROG_FLM_CONF)	2.35	2.5	2.65	V
3.5-12		V <sub>TH1-B</sub>	voltage threshold for short circuit (sd_mde=10 in PROG_FLM_CONF)	3.8	4	4.2	V
3.5-13		t <sub>f_ TH1</sub>	filter time		8		us
3.5-14		V <sub>TH2</sub>	voltage threshold for highside power stage test	4.05	4.3	4.55	V
3.5-15		t <sub>f_ TH2</sub>	filter time		1		us
3.5-16		V <sub>TH3</sub>	voltage threshold for short circuit, cap test and cross coupling test	0.85	0.9	0.95	V
3.5-17		t <sub>f_ TH3</sub>	filter time		8		us
3.5-18		V <sub>TH4</sub>	voltage threshold for lowside power stage test and squib detection test	0.45	0.5	0.55	V
3.5-19		t <sub>f_ TH4</sub>	filter time		1		us
3.5-20	IGHx, IGLx leakage resistance measurement	R <sub>L1</sub>	leakage resistor detection range for voltage threshold 1 (2.5V) U <sub>leakage</sub> = 14V	12		25	kΩ
3.5-21		R <sub>L2</sub>	leakage resistor detection range for voltage threshold 2 (4.0V) U <sub>leakage</sub> = 12V U <sub>leakage</sub> = 8V U <sub>leakage</sub> = 18V	3 0.5 0.5		7 15 15	kΩ kΩ kΩ
3.5-22		R <sub>L3</sub>	leakage resistor detection range for voltage threshold 4 (0.9V) U <sub>leakage</sub> = 0 V	3		7	kΩ
3.5-23	IGHx, IGLx, time measurement	t <sub>IGHx_PS</sub>	maximum switch on time to reach voltage threshold 3 (4.3V) during highside power stage test		85		us
3.5-24		t <sub>IGLx_PS</sub>	maximum switch on time to reach voltage threshold 5 (0.5V) during lowside power stage test		35		us
3.5-25	SQREF measurement	res RR	resistor ratio resolution related to R <sub>SQREF</sub> (R <sub>SQREF</sub> /1024)		1/1024		
3.5-26	VHx measurement	voltage measurement ADC	voltage range			36	V
3.5-27		min res VHx	resolution 1LSB		47.6		mV
3.5-28	SVR_DIAG	test current		46.8	52	57.2	mA
3.5-29		turn-on delay				1	us

### Application Note:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
SQREF	resistor	R <sub>SQREF</sub>		10		Ω

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## 4. Functional Description Interface Module (IM)

The interface module combines all functionality for control and data interchange. The SPI interface connects the airbag system ASIC with the micro controller, sensors etc. The PSI module establishes the connection to external sensors. The system control pins define the system behavior and provides the external clock to the ASIC. For local network interconnect the LIN module can be used or switched to a general purpose interface with direct control and PWM support. The modules AIN and AIO combined with the measuring unit and the ADC are I/O pins with and without supply for highside and lowside applications and configurable in a wide range.

### 4.1 Serial Peripheral Interface SPI

The serial peripheral interface (SPI) establishes a communication link between the system's micro controller and the airbag system ASIC. The airbag system ASIC always operate in slave mode whereas the controller provides the master function.

The airbag system ASIC provides a separate chip select signal (N\_CS) which has to be connected directly with the micro controller. SCK, SO and SI are bus signals which are connected to all SPI controlled ICs on the ECU and to the controller simultaneously.

Applying an active chip select signal (low) at N\_CS the according IC is selected by the SPI master. SI is the data input (slave in), SO the data output (slave out). Via SCK (serial clock) the SPI clock is provided by the SPI master.

In case of an inactive chip select signal (high) the data output SO of the according IC has high impedance (tri-state). It is not allowed to activate more than one N\_CS signal at a time (except of the monitor SPI chip select N\_CS\_MON, see chapter 5.2 starting on page 153).

#### 4.1.1 SPI communication

A SPI communication transmits instruction and data from the controller to the selected slave and the status and data from the slave to the controller concurrently. There is no difference between a read and write access except of the data being transmitted.

The SPI supports combined read write cycles using a single SPI frame to receive data from the uC (write access) and to send data to the uC (read access). Therefore the controller sends the data after the SPI instruction, beginning with the MSB, while the slave - after having received the SPI instruction - sends the corresponding data to the controller, also starting with the MSB.

The airbag system ASIC supports a 32 bit SPI frame including 10 bit instruction, 16 bit data and 3 bit CRC for incoming data (SI) and status bits, safety identifier (SID), 16 bit data and 3 bit CRC for outgoing data (SO):

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	instruction										pe	16 bit input data										CRC	-									
SO	general status		S	SID / add. status		16 bit output data										gs	CRC															

Frame format features:

- 10 bit SPI instruction
- programming enable bit (pe)
- 16 bit input and output data
- 3 bit CRC for input and output signal
- 6 general status flags
- sensor data flag (S)
- 5 bit safety ID / 5 additional status flags
- global status flag (gs)

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## 4.1.2 SPI characteristics

During active reset conditions the SPI is driven into its default state. When reset becomes inactive, the state machine enters into a wait state for the next instruction. During active reset conditions the output SO has high impedance.

If the chip select signal at N\_CS is inactive (high) the state machine is forced to enter the wait state, i.e. the state machine waits for the following instruction. During inactive chip select (N\_CS is high) the output SO has high impedance.

During active state of the chip select signal N\_CS (low) the rising edge of the serial clock signal SCK will be used to drive the output data at SO. Input data at SI is latched with the falling edge of SCK. Further processing of the data according to the instruction (e.g. modification of internal registers) will be triggered by the rising edge of the N\_CS signal.

Simultaneously to the receipt of an SPI instruction the airbag system ASIC transmits status bits via the output SO to the controller. These status bits indicate regular or irregular operation of the ASIC. A general flag indicating an invalid instruction or a transmission failure of the last SPI access is included.

Instructions with a simultaneous read and write access are supported. Unused bits within the read data are ignored, the written data is defined by the SPI instruction set.

Every instruction (10 bit) and all data are protected with a 3 bit CRC. In case of a CRC error the instruction is detected as invalid.

An instruction is invalid, if one of the following conditions is fulfilled:

- an unused instruction code is detected (see tables with SPI instructions)
- the CRC is invalid
- in case the actual transmission is not completed in terms of internal data processing (violation of the minimum access time)
- number of sck clock pulses are not 32

If an invalid instruction is detected any modifications on registers are rejected and the transfer failure flag (TFF) in the next following check byte will be set. Therefore, no clear-on-read operations will be performed as well.

Additionally, in case of an unused instruction code the data byte transmitted will be "00<sub>hex</sub>".

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## 4.1.3 SPI Instruction Format

The SPI instructions include 10 bits with the MSB indicating a READ\_SENSOR instruction. Therefore all SPI instructions but READ\_SENSOR start with a leading 0. The READ\_SENSOR instruction is a single-bit instruction having a 1 in the MSB. In case a SPI instruction have a channel coding included, the channel is coded within the least significant bits of the instruction.

## 4.1.4 SPI Status Bits

### General status bits:

31: TFF transfer failure flag	0 = OK, 1 = failure in previous SPI communication
30: TST test active flag	0 = OK, 1 = ASIC in test mode
29: EOP end of programming	0 = EOP1 and EOP2 set, 1 = EOP1 and/or EOP2 not set
28: WDF watchdog fault	0 = OK, 1 = watchdog fault occurred
27: DIS2 disposal flag 2	0 = OK, 1 = disposal function active
26: DIS1 disposal flag 1	0 = OK, 1 = disposal function active

### Application note:

The general status bits need up to two ECLK clock cycles to change. Therefore, the very next SPI command may pass the old value of the status bit.

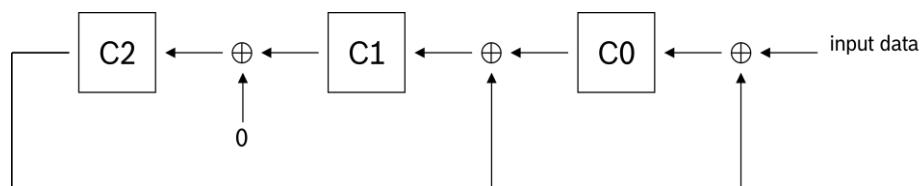
### Additional status bits:

24: FRB FLM run bit	1= FLM CAP test or FLM cross coupling test is running
23: BSY1 FLM busy	0 = ready to start new task, 1 = task in progress
22: BSY2 AIN/AIO busy	0 = ready to start new task, 1 = task in progress
21: BSY3 POM busy	0 = ready to start new task, 1 = task in progress
20: BSY4 others busy	0 = ready to start new task, 1 = task in progress

## 4.1.5 SPI CRC generation

The airbag system ASIC SPI is protected with a 3 bit CRC for the incoming data (bits 31 to 5 included) and with a 3 bit CRC for the outgoing data (bits 26 to 3 included). For the incoming data the CRC is generated inside the uc and checked inside the airbag system ASIC to be consistent. For the outgoing data the CRC is generated inside the airbag system ASIC and can be checked within the uc.

The CRC is generated by using the polynomial  $X^3 + X + 1$  with the binary start value "111":



The data word is fed (LSB first) into the shift registers of the CRC check and is supplemented with three leading zeros (as MSBs). In case of a CRC error within the incoming data, the last CRC bit of the outgoing data will be inverted.

# Data sheet CG904, CG903, CG902

## 4.1.6 SPI Default Instructions

Read device identifier:

### SPI instruction READ\_DEV\_ID

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

device\_id CG904: C4<sub>hex</sub> = 1100 0100<sub>bin</sub>

CG903: C3<sub>hex</sub> = 1100 0011<sub>bin</sub>

CG902: C2<sub>hex</sub> = 1100 0010<sub>bin</sub>

Read revision identifier:

### SPI instruction READ\_REV\_ID

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

revision\_id = 0100<sub>bin</sub> (depending on silicon version)

Read mask identifier:

### SPI instruction READ\_MASK\_ID

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

mask\_id = 0100<sub>bin</sub> (depending on silicon version)

### Application Note:

The mask identifier can change without notice. To be used for ASIC production test only!

End of programming:

### SPI instruction EOP

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	e2	e1
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TM	E2 E1

e1 / E1 = 1: release SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S signals from 0 (EOP1)

e2 / E2 = 1: all programmable SPI registers will be locked (EOP2)

TM : level of pin TESTM (should always be zero)

The e2 bit sets e1 as well.

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## 4.1.7 SPI General Instructions

<b>SPI instruction</b>	<b>description</b>	<b>binary code</b>	<b>module</b>
READ_DEV_ID		0000000000	SPI
READ_REV_ID		0000000001	SPI
READ_MASK_ID		0000000010	SPI
EOP		00000000110	SPI
WD2_TRIGGER		00000000100	WD
WD3_TRIGGER		00000000101	WD
WD_STATUS		00000000111	WD
AIO1_PWM		0001000010	AIO
AIO2_PWM		0001000011	AIO
AIO1_STATUS		0001000000	AIO
AIO2_STATUS		0001000001	AIO
AIO_LIN_EN		0001000101	AIO, LIN
AINO_START_AUTO		0000001011	AINO
AINO_READ_AUTO1...12		010001----	AINO
AINO_START_BIST		0000001100	AINO
AINO_READ_BIST1...7		0100100---	AINO
ADC_START_AINO		0000111001	ADC
ADC_READ_AINO		0000111101	ADC
READ_MON_ID		0000001111	MON
DISPOSAL		0000010000	SAM
DEMAND_TEST		0000010001	SAM
THRES_TEST_DATA		0000010010	SAM
THRES_TEST_SID		0000010011	SAM
TEST_PLP_THRES		0000110010	SAM
TEST_PLP_DATA		0000110011	SAM
END_ENABLE		0000010100	SAM
DISABLE_STATUS		0000110101	SAM
FLM_STATUS		0000010101	FLM
FLM_HS_ON		0000010110	FLM
FLM_LS_ON		0000010111	FLM
FLM_TEST_MAN		0000011000	FLM
FLM_TEST_TG		0000011001	FLM
FLM_UNLOCK		0000011010	FLM
FLM_READ_FIRE_CNT1...16		010011----	FLM
FLM_CLEAR_FIRE_CNT		0000011011	FLM
FLM_DIAG_MASK		0000011100	FLM
FLM_START_DIAG		0000011101	FLM
FLM_READ_RES1...16		010100----	FLM
FLM_READ_VH1...8		0101010---	FLM
FLM_READ_CAP		0101011000	FLM
FLM_READ_PST		0101011100	FLM
FLM_READ_SVR		0101011010	FLM
FLM_READ_CC		0101011011	FLM
FLM_READ_SQB		0101011001	FLM
FLM_READ_SHORT1...4		01011010--	FLM
FLM_READ_IGH		0001000110	FLM
PSI_SUPPLY		0000011110	PSI
PSI_READ_LEV		0000110100	PSI
PSI_READ_DATA1...32		1----0000	PSI
PSI_SYNC_GEN		0000011111	PSI
PSI_SYNC_MASK		0000100000	PSI

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PSI_IQ_STATUS		0000100001	PSI
PSI_TEST_CONS		0000100010	PSI
PSI_START_CC		0000100011	PSI
PSI_READ_CC		0000100100	PSI
PSI_READ_SC		0000100101	PSI
POM_CYCL_CAP		0000100110	POM
POM_STATUS		0000100111	POM
POM_CONVERTER		0001000111	POM
POM_VER_CURR		0000101000	POM
POM_START_BIST		0000101001	POM
POM_READ_BIST		0000101010	POM
POM_START_AUTO		0000101011	POM
POM_READ_AUTO1...5		0101110---	POM
LIN_PWM		0001000100	LIN
LIN_STATUS		0000110110	LIN

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## 4.1.8 SPI Programming Instructions

All SPI programming registers accessed by the SPI programming instructions *PROG ...* are locked by the EOP2 flag set with the SPI instruction *EOP*. The lock can be cleared by reset only. This locking mechanism can be used to protect the registers against uncontrolled changes. The lock should be activated after the initialization of the ASIC is completed.

Please note that all programming instructions are only active if the programming enable bit is set (*pe=1*). To verify the programming, the *pe* bit should be set to zero (*pe=0*). The *pe* bit will be ignored for all non PROG instructions.

The successful programming by the SPI programming instructions *PROG ...* can be verified using the same SPI instruction. The output data format is identical to the input data format. Unused bits are returned as zero.

<b>SPI instruction</b>	<b>description</b>	<b>binary code</b>	<b>module</b>
PROG_AINO_CONF1...12		011001----	AINO
PROG_AIO1		0110001110	AIO
PROG_AIO2		0110001111	AIO
PROG_SAF_CH1...16		011010----	SAM
PROG_SDIS_X		0110000001	SAM
PROG_SDIS_Y		0110000010	SAM
PROG_SDIS_W		0110000011	SAM
PROG_SDIS_S		0110000100	SAM
PROG_SAFETY		0110000101	SAM
PROG_SW_MODE		0110000110	SAM
PROG_SW_UP_THRES		0110000111	SAM
PROG_SW_LOW_THRES		0110001000	SAM
PROG_XY45		0110001001	SAM
PROG_PLP_LONG		0110111000	SAM
PROG_FLM_CONF		0110001010	FLM
PROG_FLM_MODE		0110001101	FLM
PROG_PSI_SID1...24		01110----	PSI
PROG_PSI_LINE1...6		0110110---	PSI
PROG_PSI_MODE		0110001011	PSI
PROG_POM		0110001100	POM
PROG_LIN		0110000000	LIN

## 4.1.9 SPI Monitor Instructions

<b>SPI instruction</b>	<b>description</b>	<b>binary code</b>	<b>module</b>
READ_DEV_ID		0000000000	SAM
READ_SENSOR		1-----	SAM
DEMAND_TEST		0000010001	SAM
READ_DEV_ID_16		0000000	SAM
READ_SENSOR_16		1----0	SAM
DEMAND_TEST_16		0011100	SAM

The SPI instruction *PSI\_READ\_DATA* is a subset of the SPI instruction *READ\_SENSOR*.

The airbag system ASIC is able to monitor SPI frames with 16, 17 and 32 bits.

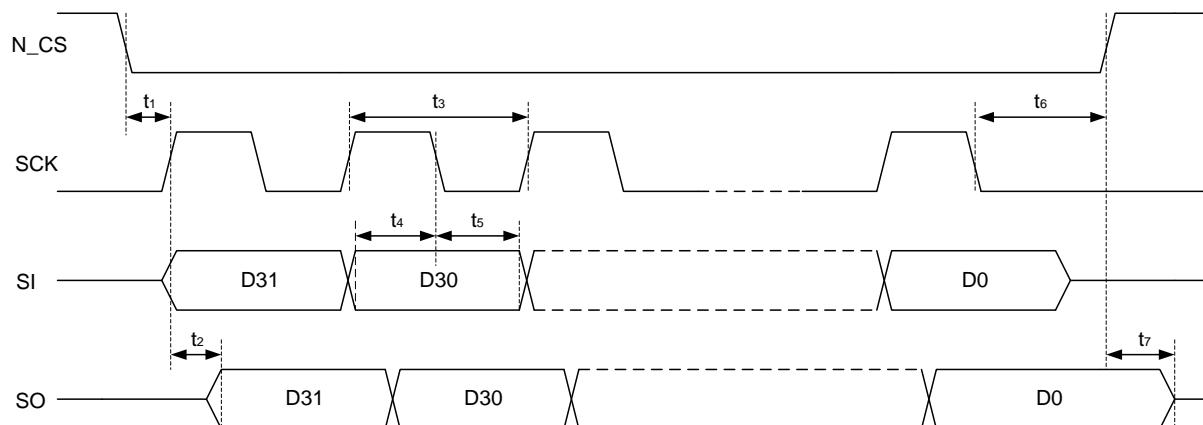
# Data sheet CG904, CG903, CG902

## 4.1.10 SPI timing

The timing of the SPI is defined as follows:

- the change at output (SO) is forced by the rising edge of the SCK signal
- the input signal (SI) is latched on the falling edge of the SCK signal
- the data received during a write access is written into the internal registers at the rising edge of the N\_CS signal, if exactly 32 SPI clock pulses have been counted during N\_CS active (low)

SPI Timing Diagram (32 bit frame):



t1: enable lead time  
t2: data valid time  
t3: cycle time  
t4: data setup time  
t5: data hold time  
t6: enable lag time  
t7: disable time

For the detailed electrical characteristics please see the following chapter.

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## 4.1.11 SPI Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
4.1-1	SO, N_CS, N_CS_MON	pull-up current	pull-up current of SO can be switched off	50	75	100	uA
4.1-2	SI, SCK	pull-down current		50	75	100	uA
4.1-3	SI, SO, SCK, N_CS, N_CS_MON	threshold	input low voltage			0.3 * VIO	-
4.1-4	SI, SO, SCK, N_CS, N_CS_MON	threshold	input high voltage	0.7 * VIO			-
4.1-5	SI, SO, SCK, N_CS, N_CS_MON	hysteresis	input voltage	0.5		1.5	V
4.1-6	SI, SCK, N_CS, N_CS_MON	pad capacity	(not to be tested in series production)			6	pF
4.1-7	SO	output voltage	output low voltage, I_SO = 2mA			0.2 * VIO	V
4.1-8	SO	output voltage	output high voltage, I_SO = -2mA	0.8 * VIO			V
4.1-9	SO	pad capacity	(not to be tested in series production)			10	pF
4.1-10	SCK	frequency	cycle time (t <sub>3</sub> )		10	+5%	MHz
4.1-11	N_CS, SCK	delay time	enable lead time (t <sub>1</sub> )	100			ns
4.1-12	SCK, N_CS	delay time	enable lag time (t <sub>6</sub> )	100			ns
4.1-13	SCK, SO	delay time	data valid time, falling edge (t <sub>2</sub> ) SCK rising $\Rightarrow$ SO 20%, C = 90pF			32	ns
4.1-14	SCK, SO	delay time	data valid time, rising edge (t <sub>2</sub> ) SCK rising $\Rightarrow$ SO 80%, C = 90pF			32	ns
4.1-15	SCK, SI	delay time	data setup time (t <sub>4</sub> )	14			ns
4.1-16	SCK, SI	delay time	data hold time (t <sub>5</sub> )	20			ns
4.1-17	N_CS, SO	delay time	disable time (t <sub>7</sub> )			100	ns
4.1-18	N_CS	delay time	inter-communication time	100			ns
4.1-19	N_CS, SCK	delay time	disable lead time	60			ns
4.1-20	SCK, N_CS	delay time	disable lag time	60			ns

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## 4.2 Peripheral Sensor Interface PSI

All sensor interfaces in the airbag system ASIC CG90x are implemented according to the PSI5 standard v1.3. The interface is designed to connect peripheral acceleration sensors (PAS), up-front sensors (UFS) and pressure sensors (PPS) directly to the airbag system using a point-to-point or bus topology. Synchronous and asynchronous communication modes are supported.

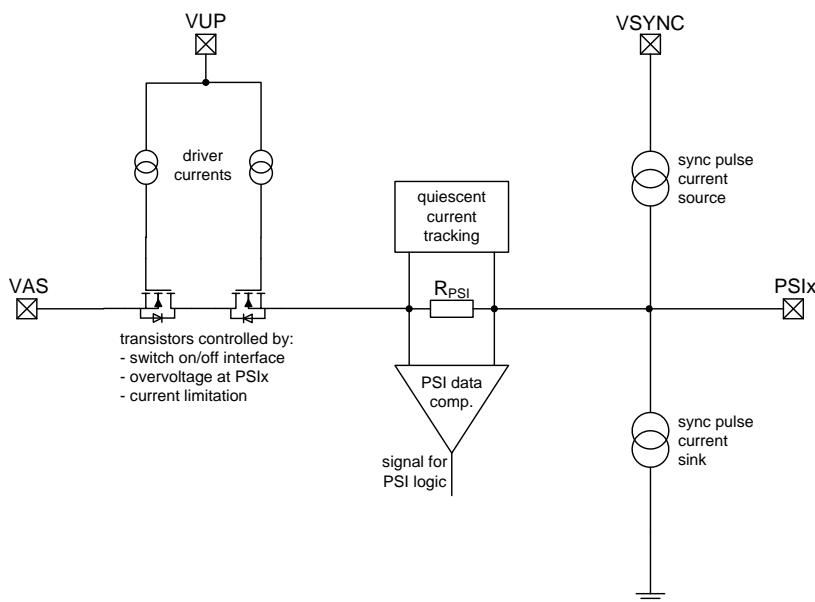
### Features:

- 6 PSI5 interfaces integrated
- Asynchronous (PSI5-A) and synchronous (PSI5) operation
- Point-to-point, bus, and daisy chain mode
- 3 different data transmission modes selectable (83.3 kbps, 125 kbps, 189 kbps)
- Operation with up to 4 sensors per interface (189 kbps data transmission)
- Operation with up to 3 sensors per interface (125 kbps data transmission)
- Operation with up to 2 sensors per interface (83.3 kbps data transmission)
- Uni- and bidirectional communication
- Two-wire interface (combined lines for supply and data transmission)
- Manchester-coded digital data transmission
- 10 bit data frame
- 3 bit CRC mode or single bit parity mode selectable
- Integrated comparator functionality for voltage monitoring of sensor channels
- Safety identifier programmable for each channel and time slot
- Integrated resistor for communication current detection
- 3 different PSI sync pulse trigger modes (pin, SPI, automatic timing)
- PSI sync pulse slew rate control
- Raised cosine sync pulse shaping for reduced electromagnetic emission
- PSI quiescent current tracking
- PSI comparator threshold control
- VAS reverse current protection
- PSI data path consistency check
- Configurable handling of data words extending across time slot limits
- Cross-coupling diagnosis
- Automatic PSI deactivation in case of short-to-ground

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## 4.2.1 PSI Functional Description

The figure listed below shows a block diagram of the interface implemented in the ASIC. Switch-on of the interface is done by driving the blocking transistors in the path between VAS and PSI (supplied by VUP). Then, the voltage VAS (voltage analog supply) supplies sensor quiescent current and sensor data current. A comparator over the resistor  $R_{PSI}$  is used to detect the data current from the sensor. The correct comparator threshold for safe detection is set by the quiescent current and data comparator threshold control circuitry.



The internal resistance between VAS pin and PSI pin can be assumed to be linear. Therefore, the drop voltage between VAS and PSI is linear to the PSI current.

For the airbag system ASIC CG904 6 PSI channels are implemented.

## 4.2.2 Safety Identifier

A programmable safety identifier (SID) is assigned to each sensor data as a safety feature for monitoring the correct data transfer via SPI to the microcontroller. The safety module (SAM) evaluates the SID to provide the dedicated sensor data thresholds for firing loop release. All bits are programmable via SPI command PROG\_PSI\_SID.

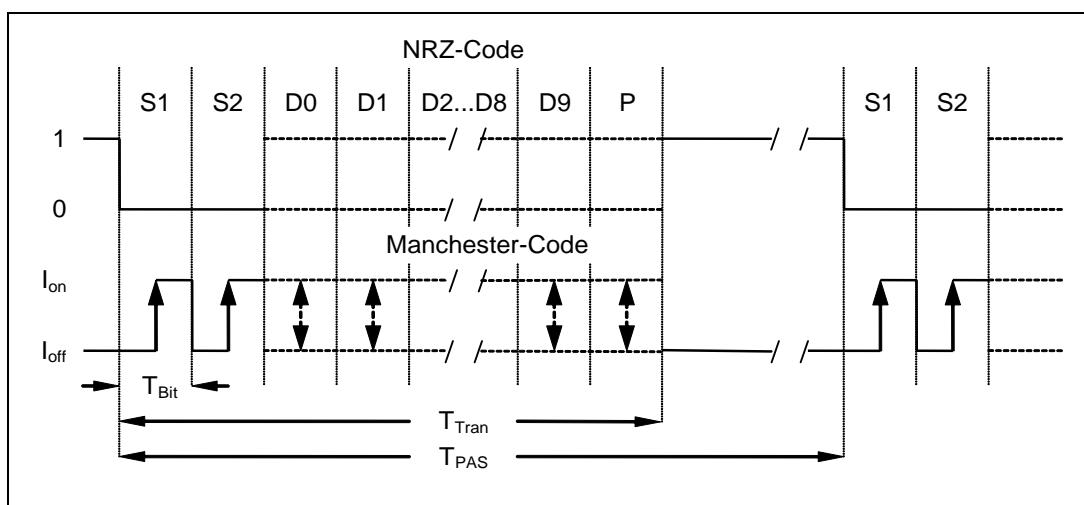
# Data sheet CG904, CG903, CG902

## 4.2.3 PSI Data Protocol

The PSI data protocol consists of:

- 2 start bits
- 10 data bits
- 1 parity bit or 3 CRC bits
- 1 stop bit (min. gap time between 2 consecutive data frames)

The typical bit width ( $T_{bit}$ ) is 8us (125kbps), the typical transmission time ( $T_{tran}$ ) is 104us (2 start bits, 10 data bits, 1 parity bit, no stop bit) and the typical cycle time ( $T_{PAS}$ ) is 228us (all times refer to a single sensor application). Data transmission mode is LSB first. The parity bit uses an even parity scheme (number of ones within data and parity bits must be even). All bits are Manchester coded. Additionally, a data protocol using a 3 bit CRC code instead of a single bit parity mode can be used.

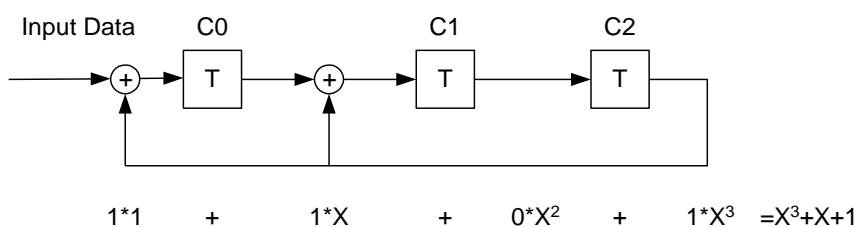


The PSI interface can be used in two different check sum modes programmable by the SPI instruction PROG\_PSI\_LINE:

- single parity mode with 10 bit data (2 start bits, 10 bit data, 1 parity bit, 1 stop bit)
- 3 bit CRC mode with 10 bit data (2 start bits, 10 bit data, 3 bit CRC, 1 stop bit)

In case the 3 bit CRC mode is used, the used generator polynomial for the CRC-recalculation is  $g(x) = x^3 + x + 1$  with a binary start value "111". Both start bits are ignored in this check. The data word is fed (LSB first) into the shift registers of the CRC check and is supplemented with three leading zeros (as MSBs). When the last data bit has been shifted into the CRC registers these registers must contain the three CRC check bits (check bits are transmitted in reverse order, MSB first).

CRC calculation scheme



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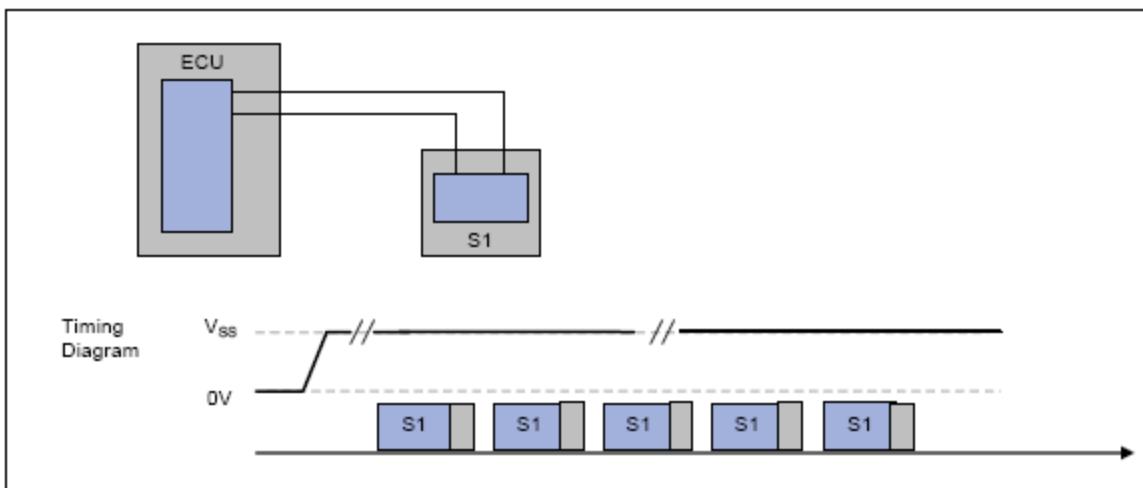
## 4.2.4 ECU Error codes in the PSI data space

<b>Data value (decimal)</b>	<b>Data value (hexadecimal)</b>	<b>Description</b>	<b>Sensor classification</b>
+511	1FF		
+510	1FE		
+509	1FD		
+508	1FC	manchester error (receiver internal)	
+507	1FB		
+506	1FA		
+505	1F9		
+504	1F8	parity or CRC error (receiver internal)	
+503	1F7		
+502	1F6		
+501	1F5		
+500	1F4		
+499	1F3		
+498	1F2		error and status messages
+497	1F1	short to ground (receiver internal)	
+496	1F0	receive buffer empty (receiver internal)	
+495	1EF		
+494	1EE		
+493	1ED		
+492	1EC		
+491	1EB		
+490	1EA		
+489	1E9		
+488	1E8		
+487	1E7		
+486	1E6		
+485	1E5		
+484	1E4		
+483	1E3		
+482	1E2		
+481	1E1		
+480	1E0	highest positive acceleration value	
...	...		
+1	001		
0	000	no acceleration	acceleration data
-1	3FF		
...	...		
-480	220	highest negative acceleration value	
-481	21F		
-482	21E		
-483	21D		
-484	21C		
-485	21B		
-486	21A		
-487	219		
-488	218		
-489	217		
-490	216		
-491	215		
-492	214		
-493	213		
-494	212		error and status messages
-495	211		
-496	210		
-497	20F		
-498	20E		
-499	20D		
-500	20C		
-501	20B		
-502	20A		
-503	209		
-504	208		
-505	207		
-506	206		
-507	205		
-508	204		
-509	203		
-510	202		
-511	201		
-512	200		

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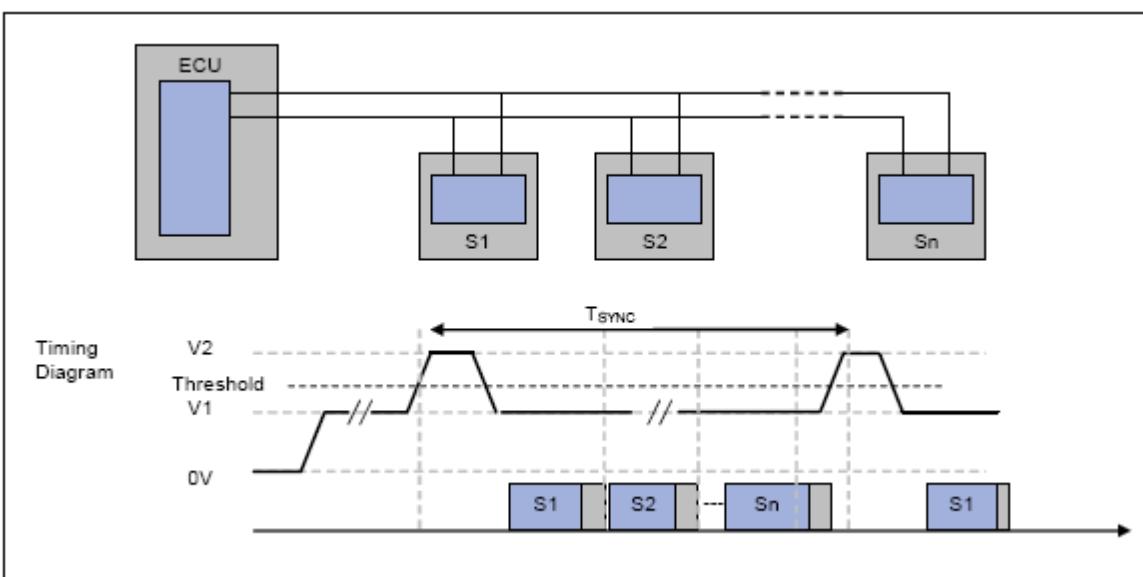
## 4.2.5 PSI Operation Modes

### Asynchronous Point-to-Point:



Each sensor is connected to the ECU by two wires. After switching on the power supply, the sensor starts transmitting data to the ECU periodically. Timing and repetition rate of the data transmission are controlled by the sensor.

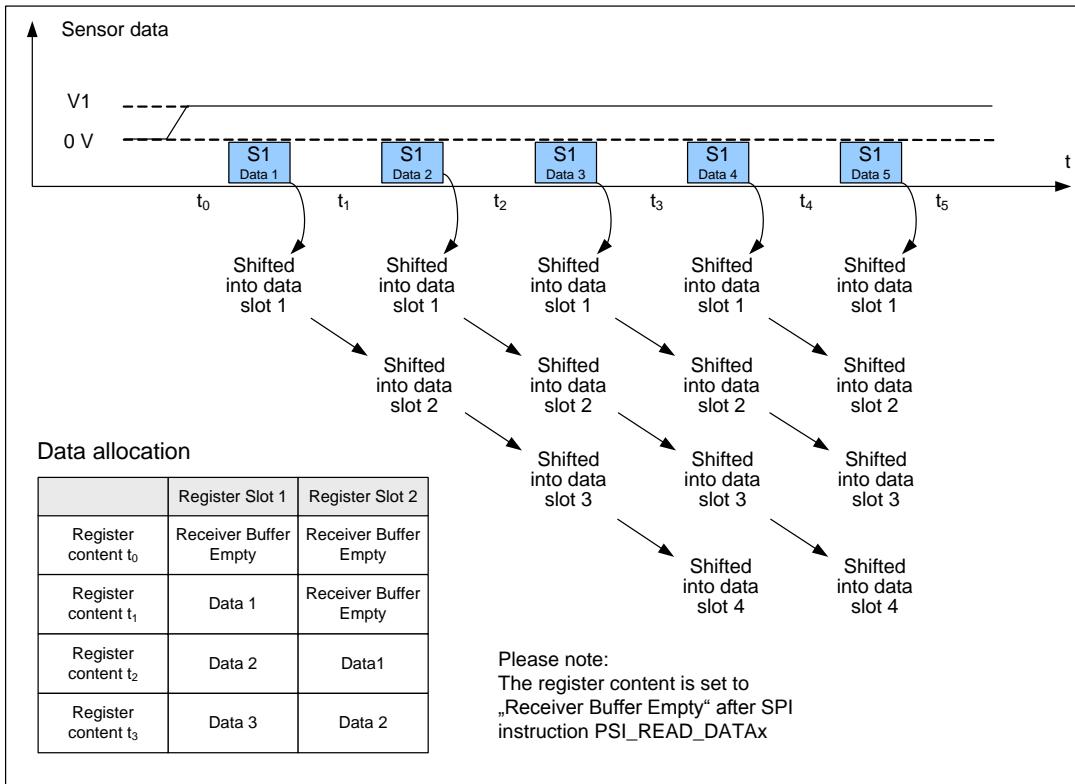
### Synchronous Parallel Bus Mode:



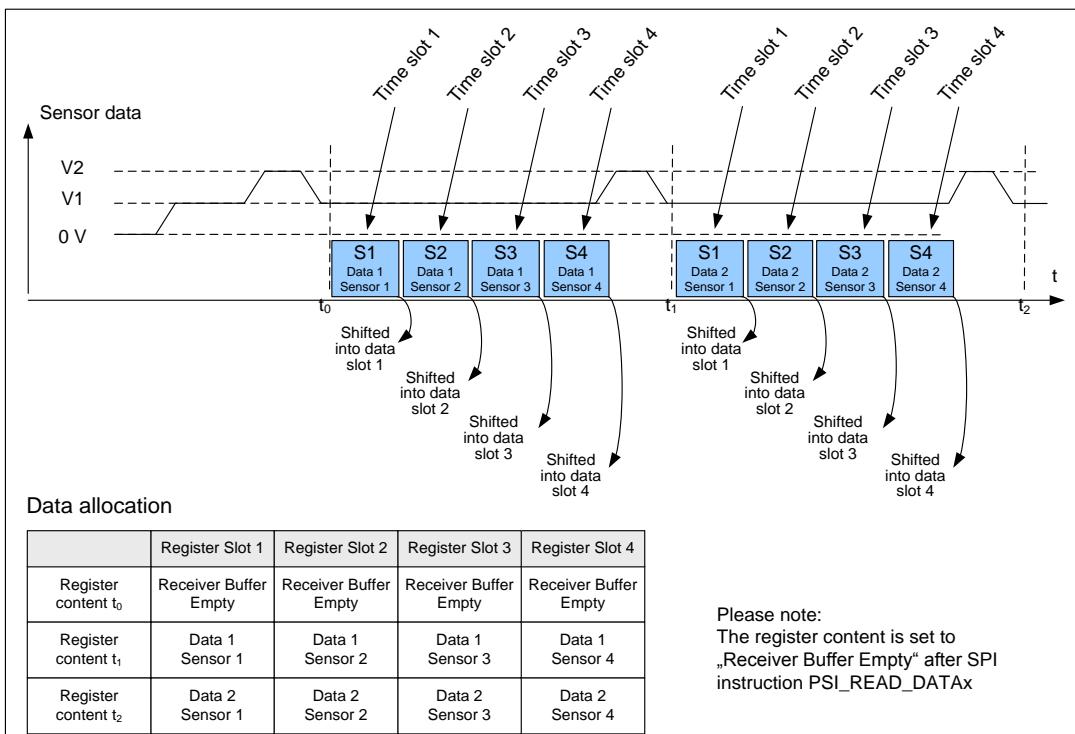
The synchronous operation modes work according to the TDMA method (Time Division Multiple Access). The sensor data transmission is synchronized by the ECU using voltage modulation. Synchronization can be optionally used for point-to-point configurations and is mandatory for bus modes. Each data transmission period is initiated by a voltage synchronization signal from the ECU to the sensors. Having received the synchronization signal, each sensor starts transmitting its data with the corresponding time shift in the assigned time slot.

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## 4.2.6 PSI Data Register Mapping (asynchronous mode)



## 4.2.7 PSI Data Register Mapping (synchronous mode)



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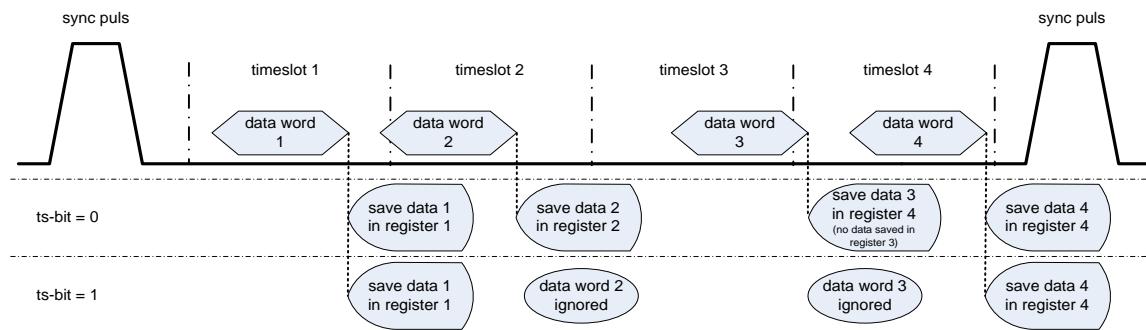
## 4.2.8 PSI time slot definition

Definition of timings:

Slot mode	Slot 1 start time	Slot 2 start time	Slot 3 start time	Slot 4 start time	
1 slot	40 µs				slot 1 end time: 492 µs
2 slots	40 µs	256 µs			slot 2 end time: 492 µs
3 slots	40 µs	181.25 µs	328.75 µs		slot 3 end time: 492 µs
4 slots	40 µs	139.50 µs	245.50 µs	362.50 µs	slot 4 end time: 492 µs

Start of timing ( $t=0$ ) is related to the PSI sync pulse voltage (sync pulse voltage = 0.5V) at PSI pin. These timings define the storage of the received PSI data into the corresponding data register. The receiving of data is possible beginning at  $t=40\text{ }\mu\text{s}$ .

The 'ts' bit in PROG\_PSI\_LINE is used to set the data handling behavior in case sensor data words extend from one time slot to the next. The next figure illustrates this behavior for the two possible configurations for 'ts'.



## 4.2.9 PSI Sync Pulse Generation

### Generation:

A sync pulse can be triggered for all PSI channels in three different ways:

- via the external pin PSI\_SYNC
- by SPI command PSI\_SYNC\_GEN
- automatically triggered internally by the ASIC by SPI command PROG\_PSI\_MODE

The sync pulse is started simultaneously for all PSI channels unless a value for a delay is set by SPI command PROG\_PSI\_MODE. The time between two consecutive sync pulses is 495µs at minimum. Any triggering in time steps smaller than 495µs is ignored independent of the trigger method.

The sync pulse can be suppressed from being generated by SPI command PSI\_SYNC\_MASK for each channel separately independent of the trigger mode.

### Sync pulse control:

The rising edge of the sync pulse is generated by a current source (push current) loading the capacitor at the PSI pin. In order to realize the falling edge of the sync pulse, an integrated current sink (pull current) decreases the potential at pin PSIx.

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The sync pulse slew rates have to fulfill the PSI5 specification independent of the number of sensors and the capacitance at the interface. Therefore, the push and pull currents are adapted to the actual quiescent current at the interface. The actual quiescent current value is obtained by the quiescent current tracking. In order to be immune against a capacitor loss on the sensor bus, a sync pulse control introduced that sets the push and pull currents depending on the load conditions.

The PSI supply voltage VSYNC is monitored. If VSYNC falls below the monitoring threshold, the 'vs' bit in SPI command PSI\_READ\_DATA is set to 1.

**Application note:**

The setup time of the sync pulse control is max. 5ms after the quiescent current tracking has completed.

## 4.2.10 PSI Quiescent Current Tracking

The quiescent current through the PSI bus can vary over a wide range. In order to detect sensor data, it is necessary to set the data detection threshold independent of this quiescent current. Therefore, a circuitry detects the quiescent current. This is further used to set up the threshold of the data comparator over the resistor  $R_{PSI}$ . The output data of the SPI instruction PSI\_IQ\_STATUS indicates whether the maximum or minimum quiescent current is detected.

The decrementing speed of the quiescent current tracking can be set by the 'qr' bit of SPI command PROG\_PSI\_LINE.

**Application note:**

The setup time of the quiescent current tracking is max. 10ms.

## 4.2.11 PSI Data Comparator Threshold Control and Data Filtering

Depending on the parameters of the PSI line (resistance, capacitance, inductance), the sensor data current signal deviates from an ideal square signal. In case of a bad signal waveform of the sensor data current, the data receiver quality can be ensured using a data comparator threshold control which sets up the optimal threshold for each slot.

The output of the data comparator is evaluated in the internal Manchester decoder. A filter is used between the output of the comparator and the Manchester decoder and set by the 'filter' bits of SPI command PROG\_PSI\_LINE.

**Application note:**

The setup time of the comparator threshold control is max. 5ms.

## 4.2.12 PSI Diagnosis & Fault Conditions

**Digital measurement of voltage at interface lines:**

A comparator compares the interface voltage to a 3.3V voltage level. This information can be read out with the SPI command PSI\_READ\_LEV.

**Data path consistency check and GS bit:**

The PSI data path is monitored continuously by the PSI consistency checker according to ISO26262. In case an internal fault is detected, the global status bit (GS bit) is set. The GS bit is also set in case an undervoltage condition at VAS or VUP is detected or in case of a parity

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mismatch of the PROG\_PSI registers. The PSI consistency check can be tested by built-in tests controlled by the SPI instruction PSI\_TEST\_CONS.

## Cross coupling check:

A cross coupling test can be started to check for external or internal shorts between PSI interface channels. The channels to be tested can be set and the test is started by SPI command PSI\_START\_CC.

If the cross coupling test is started in master mode, all 6 PSI channels are turned on sequentially, while all other PSI channels that are not turned on are checked for voltages above the internal threshold voltage of 3.3 V. Should any of the PSI channels that are not turned on, be detected with a pin voltage higher than 3.3 V, then the corresponding bit is set to 1 in PSI\_READ\_CC. A short-to-ground test is performed on the PSI channels that are turned on, and the results are stored in register PSI\_READ\_SC. The test terminates automatically after a time of 3.5 ms has passed, independent of the number of channels selected for the test.

If the cross coupling test is started in slave mode, none of 6 PSI channels are turned on, while all of them are observed for pin voltages above 3.3 V. In slave mode, the test has to be terminated manually via the stop bit 0 in PSI\_READ\_CC.

## Overvoltage at the interface pin:

Applying an external voltage to the PSI line could force a current into the interface. To protect the interface, a comparator senses an overvoltage at the interface pin and switches off the interface. This protection is active with and without ASIC supply.

## Application note:

To ensure reverse current protection in case of an external short of the PSI line to battery an external diode at pin VSYNC has to be used.

## Short and short current limitation:

In case of voltages at the PSI pin below 3.3V, an internal voltage comparator detects a short when the PSI-IF is switched on. In case the short remains for more than 128µs, but a minimum of 256µs right after turning on the PSI interface, the PSI interface is turned off automatically. The respective PSI channel has to be turned off manually and explicitly via SPI even after its automatic deactivation before it can be turned on again. The PSI channel does not turn on automatically after the short condition has disappeared. The status of the PSI lines with respect to shorts can be read by PSI\_READ\_SC. A short to ground can be detected while the PSI interface is on, and a short to supply can be detected while the PSI interface is off.

For shorts to voltages below the operating voltage, the current is limited internally immediately to values between 80 mA and 130 mA.

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## 4.2.13 PSI SPI Instructions

Switch PSI supply on/off:

### **SPI instruction PSI\_SUPPLY**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	s6	s5	s4	s3	s2	s1
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

sx : switch on PSI channel x : 1 = on, 0 = off (default 0)

PSI\_SUPPLY will be ignored in case of PSI cross coupling test is already running.

Read PSI line level:

### **SPI instruction PSI\_READ\_LEV**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	0	c6	c5	c4	c3	c2	c1

cx : comparator 3.3V on PSI channel x : 1 = level > 3.3V, 0 = level < 3.3V

All cx bits are filtered with 128us filter time.

Read PSI sensor data:

### **SPI instruction PSI\_READ\_DATA1...24**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	clr
SPI output data	0	0	0	vas	vu	vs	psi_data									

clr = 1 : clear undervoltage flags vu, vs, vas

psi\_data : read 10 bit PSI data

vu : VUP too low, 1 = VUP low (bit is latched, cleared by clr bit, filtered with 0.5/10μs)

vs : VSYNC too low, 1 = VSYNC low (bit is latched, cleared by clr bit, filtered with 0.5μs)

vas : VAS too low, 1 = VAS low (bit is latched, cleared by clr bit, filtered with 0.5/10μs)

The PSI channel address is coded within 5 bits following the first instruction bit: 3 bit channel (bit 30...28) + 2 bit time slot (bit 27...26).

Generate PSI sync pulse:

### **SPI instruction PSI\_SYNC\_GEN**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This command generates a sync pulse on all PSI channels that are turned on.

The command is ignored if the time since the last sync pulse trigger is smaller than 495μs.



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Mask PSI sync pulse:

## **SPI instruction PSI\_SYNC\_MASK**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	m6	m5	m4	m3	m2	m1
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

mx = mask PSI channel x : 1 = sync pulse enabled (PSI line has to be in synchronous mode)  
0 = PSI sync pulse masked (disabled)

Default: 1

PSI\_SYNC\_MASK affects all subsequent sync pulses until turning off the PSI channel or changing the configuration of PSI\_SYNC\_MASK via SPI.

Program PSI safety identifier:

## **SPI instruction PROG\_PSI\_SID1...24**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	psi_sid					p
SPI output data	0	0	0	0	0	0	0	0	0	0	0	psi_sid				p

psi\_sid : defines safety ID used by reading PSI data (default = 11111)

p : parity bit (odd parity), default = 0 (no parity error for an unprogrammed SID)

Please note: In asynchronous mode the SIDs of all slots used have to be programmed.

The PSI channel and timeslot are coded within the least 5 bits of the instruction.

Program PSI lines:

## **SPI instruction PROG\_PSI\_LINE1...6**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	p	0	0	1	0	0	ts	filter	qr	slot	crc	baud	as			
SPI output data	p	0	0	1	0	0	ts	filter	qr	slot	crc	baud	as			

as = 0 : PSI receiver using synchronous mode (PSI sync pulse required), default

as = 1 : PSI receiver using asynchronous mode (PSI sync pulse disabled)

baud = 00 : PSI receiver using 125kbaud mode (8us bit length), default

baud = 01 : PSI receiver using 189kbaud mode (5.3us bit length)

baud = 10 : PSI receiver using 83.3kbaud mode (12us bit length)

baud = 11 : undefined

crc = 0 : PSI receiver using single bit parity mode (default)

crc = 1 : PSI receiver using 3 bit CRC mode

slot = 00 : 1 sensor mode using single time slot (default)

slot = 01 : 2 sensor mode using two time slots

slot = 10 : 3 sensor mode using three time slots

slot = 11 : 4 sensor mode using four time slots

qr : quiescent regulation (decrementing) : 0 = 1 LSB / 8us (default), 1 = 1 LSB / 1us

filter : 00 = 2 / 3 filter (default) , 01 = no filter, 10 = 3 / 5 filter

ts : 1 = PSI data will be ignored if time slot changes during data reception (default)

p : parity bit (odd parity)

The PSI line address is coded within the least 3 bits of the instruction.

The correct parity bit has to be calculated by the SW when programming the register.

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Program PSI mode:

## **SPI instruction PROG\_PSI\_MODE**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	p2	del				p1	fil	aut	trg
SPI output data	0	0	0	0	0	0	0	p2	del				p1	fil	aut	trg

trg = 0 : PSI sync pulse generated by falling edge of pin PSI\_SYNC (default)

trg = 1 : PSI sync pulse generated by rising edge of pin PSI\_SYNC

aut = 0 : PSI sync pulse is controlled by pin PSI\_SYNC or instruction PSI\_SYNC\_GEN (default)

aut = 1 : automatic PSI sync pulse generation every 500us

del = 0 : no delay between all channels

del = 1...15 : PSI sync pulse is delayed by del \* 0,5 us incrementally per channel (default = 4)

fil : filter time for VAS- and VUP-undervoltage-monitoring, 0 = 0,5µs (default), 1 = 10µs

p1 : parity bit (bit 0...2, odd parity)

p2 : parity bit (bit 7...4, odd parity)

The correct parity bits have to be calculated by the SW when programming the register.

Start PSI cross coupling test:

## **SPI instruction PSI\_START\_CC**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	ma	e6	e5	e4	e3	e2	e1
SPI output data	0	0	0	0	0	0	0	0	0	c6	c5	c4	c3	c2	c1	

ex : enable PSI channel x for cross-coupling test (only for master mode, 1 = enable)

ma : master mode : 1 = master mode, 0 = slave mode

cx : comparator 3.3V on PSI channel x : 1 = level > 3.3V, 0 = level < 3.3V (not latched)

Cross coupling slave mode runs continuously.

ccx and rdy (from PSI\_READ\_CC) are cleared by PSI\_START\_CC.

PSI\_START\_CC will be ignored in case CC test is already running.

Read PSI cross coupling test result:

## **SPI instruction PSI\_READ\_CC**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	stp
SPI output data	0	0	0	0	0	0	0	0	rdy	run	cc6	cc5	cc4	cc3	cc2	cc1

stp : stop cross coupling test immediately

ccx : 0 = no error, 1 = cross coupling error in channel x

run : 1 = cross coupling test is running

rdy : 1 = cross coupling test finished, 0 = not started or running (only in master mode)

ccx and rdy are cleared by PSI\_START\_CC.

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Read PSI short circuit status:

## **SPI instruction PSI\_READ\_SC**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	vzl	0	0	0	sb6	sb5	sb4	sb3	sb2	sb1	sg6	sg5	sg4	sg3	sg2	sg1

sgx : 1 = short to gnd (clear by read)

sbx : 1 = short to battery (clear by read)

vzl : 1 = VZP too low, 0= VZP OK (clear by read)

Read PSI quiescent current control status:

## **SPI instruction PSI\_IQ\_STATUS**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	h6	l6	h5	l5	h4	l4	h3	l3	h2	l2	h1	l1

hx : quiescent current control of channel x at highest level (max error)

lx : quiescent current control of channel x at lowest level (min error)

Test PSI data path consistency:

## **SPI instruction PSI\_TEST\_CONS**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	pc8	pc7	pc6	pc5	pc4	pc3	pc2	pc1	pc0
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

pc0 = 1 : inverting PSI data crc bit 0

pc1 = 1 : inverting PSI data crc bit 1

pc2 = 1 : inverting PSI data crc bit 2

pc3 = 1 : inverting PSI timeslot check bit 0

pc4 = 1 : inverting PSI timeslot check bit 1

pc5 = 1 : inverting PSI channel check bit 0

pc6 = 1 : inverting PSI channel check bit 1

pc7 = 1 : inverting PSI channel check bit 2

pc8 = 1 : inverting PSI SID parity check bit

Activating the PSI consistency test with at least one bit inversion as indicated by SPI bits pc1...pc8 leads to the GS (global status) bit set to 1.

The SPI instruction PSI\_TEST\_CONS is only accepted before end of programming (EOP2) and the PSI consistency test mode has been activated by the SPI command DEMAND\_TEST. In case of end of programming (EOP2) or the PSI consistency test mode is switched off, the register of PSI\_TEST\_CONS is cleared immediately.



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## 4.2.14 PSI Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
4.2-1	PSIx	output voltage	VAS = 6.5V...6.9V, I_PSIx = 0mA			6.9	V
4.2-2	PSIx	output voltage	VAS = 6.5V...6.9V, I_PSIx = 65mA at all 6 PSI channels	5.57			V
4.2-3	PSIx	output voltage	supply switched off			100	mV
4.2-4	PSIx	voltage drop	VAS – PSIx, I_PSIx = 65mA at all 6 PSI channels			930	mV
4.2-5	PSIx	turn-on time	switching PSI supply on; time between N_CS @ 10 %, PSIx = 5.9 V, and VAS = 6.7 V			50	us
4.2-6	PSIx	current limitation	PSIx = 0V	80		130	mA
4.2-7	PSIx	threshold	short circuit detection	2.95	3.25	3.55	V
4.2-8	PSIx	reverse current	PSIx = 16.5V, PSI supply switched on			2	mA
4.2-9	PSIx	reverse current	PSIx = 16.5V, PSI supply switched off			2	mA
4.2-10	PSIx	reverse current	PSIx = 16.5V, ASIC unsupplied			1	mA
4.2-11	VSYNC	threshold	VSYNC undervoltage comparator	14.0		14.8	V
4.2-12	PSI_SYNC	pull-up current		50		100	uA
4.2-13	PSI_SYNC	filter time		250		500	ns
4.2-15	PSI_SYNC	input voltage	PSI_SYNC high	0.7*VIO			
4.2-16	PSI_SYNC	input voltage	PSI_SYNC low			0.3*VIO	
4.2-14	PSIx	I_PSIx	neg. current (without ASIC malfunction; not to be tested in series production)			-100	mA

## Application Notes:

<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / recommendation</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>	
PSIx	capacitive load	complete line capacity			107	nF	
PSIx	sensor data current		22	26	30	mA	
PSIx	bit time 83.3kbps mode			11.4	12.0	12.6	us
PSIx	bit time 125kbps mode			7.6	8.0	8.4	us
PSIx	bit time 189kbps mode		5.0	5.3	5.6	us	

For additional parameters of the system configuration please refer to "Technical Specification PSI5 V1.3"

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## 4.3 System Control

### 4.3.1 External Clock (ECLK)

The digital control of the airbag system ASIC is based on the external clock ECLK. The required frequency is 4MHz with an accuracy of 1% and a duty cycle of 50%.

### 4.3.2 System Reset (N\_SYS\_RES)

The airbag system ASIC performs a power-on reset automatically (see power-on reset description N\_POR in chapter 2.9 starting on page 44). Additionally, the airbag system ASIC can be reset by activating the system reset N\_SYS\_RES (low active).

The system reset has no influence on the power supply nor the watchdog fault counter and watchdog failure flags.

### 4.3.3 Reset Configuration (CONF\_RES)

The function of the reset configuration pin is described in the watchdog chapter 5.1.3 starting on page 149.

### 4.3.4 Analog Output (AOUT)

For test purposes during production test an analog output is available at pin AOUT.

### 4.3.5 Test Mode (TESTM)

To enter internal test mode a dedicated pin TESTM is available. This test mode is used for production test only.

#### Application Note:

The pin TESTM should be connected to ground in all applications.

### 4.3.6 System Control Electrical Characteristics

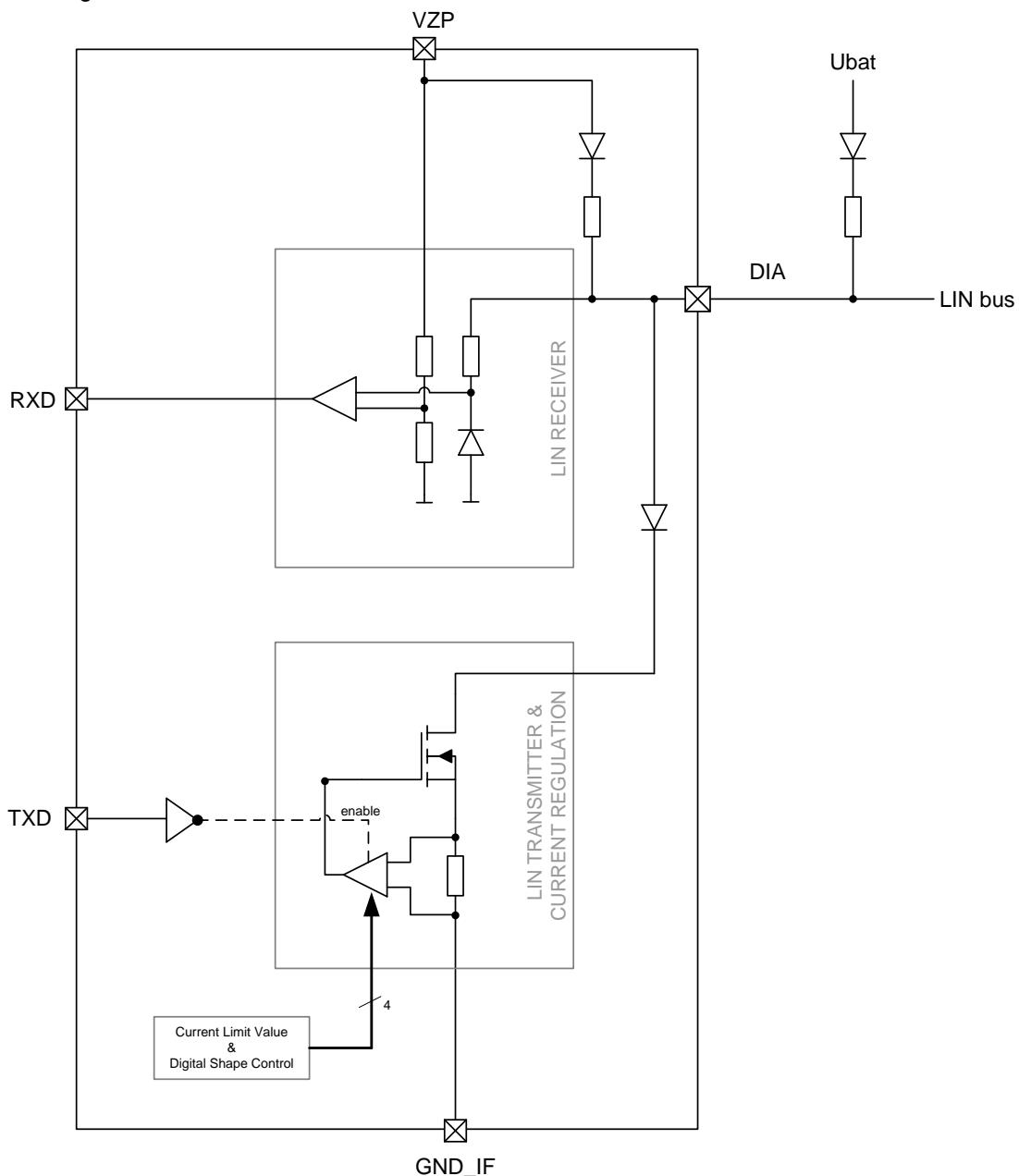
<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
4.3-1	ECLK	pull-down current		50	75	100	uA
4.3-2	ECLK, N_SYS_RES	threshold	input low voltage			0.3 * VIO	V
4.3-3	ECLK, N_SYS_RES	threshold	input high voltage	0.7 * VIO			V
4.3-4	ECLK, N_SYS_RES	hysteresis	input voltage	0.5		1.5	V
4.3-5	ECLK	frequency		-1%	4	+1%	MHz
4.3-6	ECLK	duty cycle		49	50	51	%
4.3-7	TESTM	pull-down resistor		30	50	75	kΩ
4.3-8	CONF_RES	pull up current	$V_{CONF\_RES} < 2V$ at $OTP\_READY=L$	100			uA
4.3-9	CONF_RES	pull up current	$V_{CONF\_RES} < 2V$ at $OTP\_READY=H$	20			uA

The pull-down resistor of N\_SYS\_RES is defined in chapter 2.9.1 on page 45.

## 4.4 LIN

The airbag system ASIC includes a combined interface for communication according to the LIN 2.1 standard and for general purpose.

Block diagram:



By default, the interface is in general purpose mode with the lowside transistor switched off. Activating of the lowside driver can be done by selecting the appropriate current limitation via the SPI instruction PROG\_LIN and pulling down TXD. The LIN mode can be enabled by selecting the digital shape control via the same SPI instruction. In both modes, TXD being high disables the lowside driver.

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In LIN mode the ASIC transmits data from TXD to DIA and receives data from the LIN node, DIA, at RXD. The LIN mode can be enabled by SPI instruction PROG\_LIN. The data transmission is performed including digital control of the rising and falling slopes.

In general purpose mode the interface acts as a digital programmable current sink. The current sink is controlled by the pin TXD (set TXD low for current sink activation).

## 4.4.1 LIN short detection

A comparator at the DIA port is implemented that compares the voltage at the DIA pin with an internal voltage threshold. With this comparator it is possible to detect a short circuit at the pin in the general-purpose or PWM mode. In case the PWM mode is active, the comparator checks if the level is below the threshold during the ON phase and checks if the level is above the threshold during the OFF phase, using two independent counters.

During the ON phase and in normal operation, the voltage at the DIA pin is expected to be lower than the threshold voltage of the short detection comparator. In case the voltage at the DIA pin is higher (lower) than the threshold voltage of the short detection comparator, an internal 9-bit counter is incremented by (decremented) every 12.5 us. As soon as this internal counter reaches 160, which corresponds to a time of 2 ms, a short to supply is qualified and flagged in the corresponding SPI register. Automatic deactivation of the interface occurs once the counter reaches 320, which corresponds to a time of 4 ms.

During the OFF phase and in normal operation, the voltage at the DIA pin is expected to be higher than the threshold voltage of the short detection comparator. In case the voltage at the DIA pin is lower (higher) than the threshold voltage of the short detection comparator, an internal 8-bit counter is incremented (decremented) every 12.5 us. As soon as this internal counter reaches 160, which corresponds to a time of 2 ms, a short to ground is qualified and flagged in the corresponding SPI register.

The port status can be read back by SPI command LIN\_STATUS. After the automatic turn-off, the port can only be turned again by SPI command AIO\_LIN\_EN.

## 4.4.2 PWM frequency selection

The PWM frequency can be selected via SPI command PROG\_SAFETY. The frequency can be set to 100 Hz, 200 Hz, 266 Hz, or 400 Hz with tolerances based on the ECLK tolerance.

## 4.4.3 Dominant timeout protection

In case the TXD pin is forced to a permanent low level by an external software and/or hardware failure, the dominant timeout protection prevents the bus line from being driven to a permanent dominant state and thereby prevents the network communication from being blocked.

The timer is triggered by a negative edge on pin TXD. If the duration of the low level on pin TXD exceeds the internal timer value, the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

The dominant timeout protection is independent of the external clock ECLK. Therefore, the dominant timeout protection is also functional in case the external system clock is not available to the system ASIC.

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## 4.4.4 LIN SPI Instructions

Program LIN interface current and mode:

### **SPI instruction PROG\_LIN**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	dt	lin	lin_current					
SPI output data	0	0	0	0	0	0	0	0	dt	lin	lin_current					

lin\_current = 0...62: I\_DIA = lin\_current \* 1.6mA (default = 0)

lin\_current = 63: LIN interface in PWM mode (controlled by internal PWM signal)

lin : 0 = general purpose mode (default), 1 = LIN mode

dt : dominant timeout protection : 0 = off (default), 1 = on

During LIN mode (lin=1) the value of lin\_current has no influence to the functionality of the LIN interface because the current is controlled by the LIN interface automatically.

The dominant timeout protection is only available during LIN mode (lin=1).

Set LIN PWM duty cycle and force mode (general purpose mode only):

### **SPI instruction LIN\_PWM**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	fce	pulse_width						
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

pulse\_width: (only used in PWM mode (current=111111))

0 : no PWM signal, DIA switched off

1...99: DIA signal modulated according to pulse width value

≥ 100: no PWM signal, DIA switched on (default)

During a watchdog 1 failure the pulse width is set to 100%.

fce : PWM force :

0 = a pulse width change is synchronized to the next PWM cycle (default)

1 = DIA reacts instantly to a pulse width change

Read LIN status:

### **SPI instruction LIN\_STATUS**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	vzl	0	0	0	0	0	0	0	0	0	0	to	off	on	lin_status	

lin\_status = xx1 : short between DIA pin and supply

lin\_status = x1x : short between DIA pin and ground

lin\_status = 1xx : DIA pin has been switched-off due to short to supply detection

on : 0 = DIA is/was not switched on, 1 = DIA is/was switched on (since last read)

off : 0 = DIA is/was not switched off, 1 = DIA is/was switched off (since last read)

to : timeout : 1 = dominant timeout protection is/was active

vzl : 1 = VZP too low, 0 = VZP OK (status at the moment of shortcut evaluation)

All bits are cleared by reading.



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## 4.4.5 LIN Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
4.4-1	DIA	output current	current set = 00 0001	-30%	1.89	+20%	mA
4.4-2	DIA	output current	current set = 00 0010	-15%	3.77	+15%	mA
4.4-3	DIA	output current	current set = 00 0100	-11%	7.54	+11%	mA
4.4-4	DIA	output current	current set = 00 1000	-11%	15.08	+11%	mA
4.4-5	DIA	output current	current set = 01 0000	-11%	30.16	+11%	mA
4.4-6	DIA	output current	current set = 10 0000	-11%	60.32	+11%	mA
4.4-7	DIA	output current	current set = 11 1111	-11%	118.76	+11%	mA
4.4-8	DIA	drop voltage	current set = 11 1111 (I_DIA = max)	1.0		2.0	V
4.4-9	DIA	leakage current	current source switched off, DIA = 36V, VZP = 36 V	-10		+20	uA
4.4-10	DIA	leakage current	current source switched off, DIA = 36V, VZP = 0 V	-10		+30	uA
4.4-11	DIA	leakage current	DIA = -5 V, VZP = 0 V	-300		-100	uA
4.4-12	DIA	leakage current	DIA = -10.5 V, VZP = 0 V	-1000		-100	uA
4.4-13	DIA	leakage current	DIA = -12 V, VZP = 0 V (not tested in series production)	-2000		-100	uA
4.4-14	DIA	receiver recessive state	DIA low -> high @ RXD, VZP $\geq$ 4.85V	0.6 * VZP			-
4.4-15	DIA	receiver dominant state	DIA- high -> low @ RXD, VZP $\geq$ 4.85V			0.4 * VZP	-
4.4-16	DIA	symmetry	(VDIA_rec + VDIA_dom) / 2, VZP $\geq$ 4.85V	0.475 * VZP		0.525 * VZP	-
4.4-17	DIA	hysteresis	VDIA_rec - VDIA_DOM, VZP $\geq$ 4.85V			0.175 * VZP	-
4.4-18	RXD	output voltage	RXD low, I_RXD = +1600uA			0.2 * VIO	-
4.4-19	RXD	output voltage	RXD high, I_RXD = -500uA	0.8 * VIO			-
4.4-20	TXD	input voltage	TXD high	0.7 * VIO			-
4.4-21	TXD	input voltage	TXD low			0.3 * VIO	-
4.4-22	TXD	pull-up current	TXD = 0V	50		100	uA
4.4-23	TXD	propagation delay tpTxDom	TXD high -> low @ DIA 60%, R=0.5k $\Omega$ to VZP=18V, C=10nF	0.1		15	us
4.4-24	TXD	propagation delay tpTxRec	TXD low -> high @ DIA 40%, R=0.5k $\Omega$ to VZP=18V, C=10nF	0.1		15	us
4.4-25	TXD	delay delta	tpTxDom - tpTxRec, R=0.5k $\Omega$ to VZP=18V, C=10nF	-8		8	us
4.4-26	RXD	propagation delay tpRxDom	DIA high -> low @ RXD	0.1		6	us
4.4-27	RXD	propagation delay tpRxRec	DIA low -> high @ RXD	0.1		6	us
4.4-28	RXD	delay symmetry	tpRxDom - tpRxRec, VZP $\geq$ 7V	-2		2	us
4.4-29	RXD	delay symmetry	tpRxDom - tpRxRec, LIN mode R=1.0k $\Omega$ to VZP $\geq$ 7V, C=1nF	-2		2	us
4.4-30	RXD	delay symmetry	tpRxDom - tpRxRec, LIN mode R=0.5k $\Omega$ to VZP $\geq$ 7V, C=10nF	-2		2	us
4.4-31	DIA	I_DIA_SENSE	neg. current (without ASIC malfunction, not to be tested in series production)			-100	mA
4.4-32	DIA	Slave pull-up resistor		20		60	kOhm
4.4-33	DIA	short detection	voltage threshold	2.7	3.0	3.3	V
4.4-34	DIA	short detection filter time	filter time between occurrence of short and writing LIN_STATUS data registers	2		2.2	ms
4.4-35	DIA	dominant timeout protection	time TXD stays low thereby triggering the dominant timeout protection	30	33	36	ms

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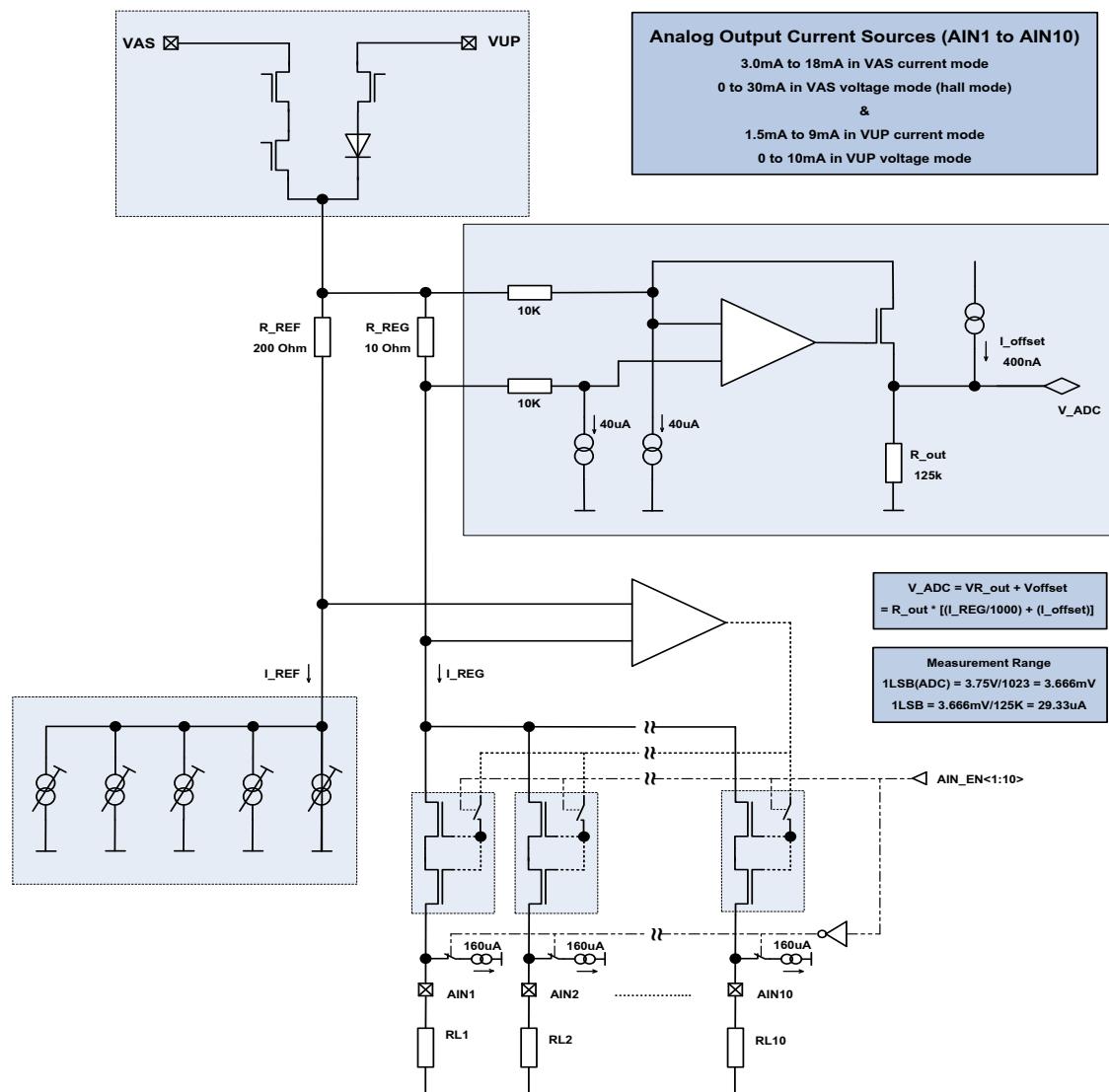
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## 4.5 Analog Input (AIN)

The AIN analog input unit consists of 5 main blocks:

- Software adjustable VAS/VUP voltage at all AIN outputs (AIN1...10)
- Software adjustable current source from 3mA up to 18mA in fixed VAS current mode and 1.5mA up to 9mA in fixed VUP current mode.
- Software adjustable voltage source with an ability to drive current of 30mA in fixed VAS voltage mode (hall mode) and 10mA in fixed VUP voltage mode.
- Reference current generation.
- Analog current measurement in fixed current and fixed voltage mode possible.

Automated build-in-test can be used to detect internal/external cross coupling or shorts to both ground and voltages > 1V. External cross coupling detection depends on the attached components on the pin.



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#### 4.5.1 VAS / VUP supply switch

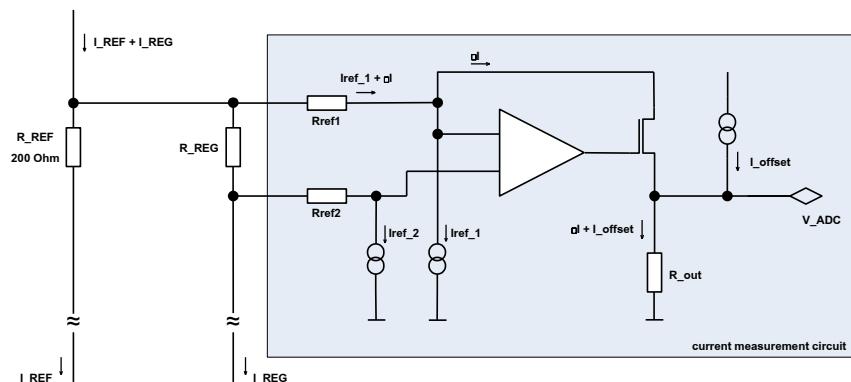
The output voltage level of the AIN driver stages can be switched between two levels. One level is the VAS voltage level, the other level is the VUP voltage level. Both voltage levels are programmable with the bit src for each AIN output separately via the SPI command PROG\_AINO\_CONF1...12 (please see chapter 4.7.13 starting on page 139).

The VAS line switch can drive loads up to 30mA in fixed voltage mode. In this mode it is possible to drive low resistive loads e.g. active seat belt circuits with hall effect sensors.

The VUP line switch can drive loads up to 10mA in fixed voltage and fixed current mode. In this mode it is possible to drive higher resistive loads e.g. passive resistor networks up to 5.5k $\Omega$ .

#### 4.5.2 Current measurement

The current measurement circuit is fully integrated and temperature compensated. Therefore, no external components are necessary.



To avoid a systematic offset of the current measurement, an offset compensation is integrated. During automatic current measurement, the offset will be compensated by doing two measurements, which are subtracted from each other. The difference will be shown in the output data of the SPI command ADC\_READ\_AINO (please see chapter 4.7.7 and 4.7.13).

In case of a manual current measurement, this offset voltage will not be compensated and the output data of the SPI will show the measured current including an offset current (please see chapter 4.7.8).

**Application Note:** The current measurement is done over the internal  $10\Omega$  resistor R\_REG. Due to internal leakage currents the output current at the pin AINx is higher than the measured current at the internal shunt. The maximum value of this offset error is specified in the electrical characteristics in chapter 4.7.14. Furthermore, the current measurement is only available with source VAS. The result of a current measurement with source VUP is undefined.

#### 4.5.3 AIN Current Regulator

The current regulator consists of three main circuits. These circuits are the programmable reference current sink, an OTA and 10 output power stages. If the current regulator is activated by a SPI command, only one power stage can drive the current to the selected AIN output at the same time.

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The current regulator will be activated over the SPI command START\_AINO\_AUTO and starts with the defined parameters which are programmed in the data register PROG\_AIN\_CONFIG1...12. If e.g. the regulator parameters are set for AIN1 in VAS fixed current mode, the chosen reference current I\_REF will be switch on and the OTA regulates the power stage as long as the I\_REG current is reached. Starting one AIN source, the reference current sink I\_REF, the regulator itself, the programmed channel and the voltage supply will be switched on. In the automatic AINO measurement the switch-on time for one selected channel is 1ms, the switch-off time is 500μs.

## 4.5.4 AIN fixed current mode

For measuring resistances, the AIN channels can be supplied with different fixed currents from a current source supplied by two selectable voltages programmable via SPI. By measuring the voltage at the AIN channel the value of the resistance can be calculated.

The voltage at AIN is limited by the voltage at VAS or VUP and the drop voltage of the current regulator of the VAS/VUP switch.

**Application Note:** Specified values for R, C and L in fixed current mode

$$\begin{aligned}0 \Omega &\leq R_{\text{meas}} \leq 5.5 \text{ k}\Omega \\0 \text{ nF} &\leq C_{\text{meas}} \leq 220 \text{ nF} \\0 \mu\text{H} &\leq L_{\text{AINx}} \leq 10 \mu\text{H}\end{aligned}$$

The permutations of external components need to be fully charged within 900μs (5 τ).

## 4.5.5 AIN fixed voltage mode (hall mode)

In the fixed voltage mode the current limitation for the AIN channels is increased to a typical value of 32mA in VAS voltage mode. In the VUP voltage mode the limitation is set to 12mA. That means as long as the current consumption of an external component (e.g. hall sensor) is below the current limitation, the voltage at AIN is equal to the voltage at VAS or VUP minus the drop voltage of the current regulator and the VAS/VUP switch.

**Application Note:** Specified values for I, C and L in fixed voltage mode

$$\begin{aligned}0 \text{ mA} &\leq I_{\text{meas}} \leq 30 \text{ mA} \\0 \text{ nF} &\leq C_{\text{meas}} \leq 220 \text{ nF} \\0 \mu\text{H} &\leq L_{\text{AINx}} \leq 10 \mu\text{H}\end{aligned}$$

The permutations of external components need to be fully charged within 700μs (5 τ).

## 4.5.6 AIN Pull-down Current

To discharge external capacitors at the AIN pins every AIN channel has a pull-down current source (typ. 160uA). In order to avoid influences on the AIN measurements the pull-down current source of a single channel is switched off as long as a measurement at this AIN channel is performed. It is also possible to measure the capacitance of the external connected capacitor by activating this pull down current source.

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## 4.5.7 AIN Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
4.5-1	AINx	saturation voltage, VAS mode	I_AINx = -20mA (VAS fixed voltage mode (Hall mode))	0.4		1.6	V
4.5-2	AINx	current limitation, VAS mode	VAS fixed voltage mode (Hall mode)	-31		-36	mA
4.5-3	AINx	output current min, VAS mode	Fixed current mode, set = 0000		3.0		mA
4.5-4	AINx	output current max, VAS mode	Fixed current mode, set = 1111		18.0		mA
4.5-5	AINx	current accuracy, VAS mode	Fixed current mode, I_AINx < 5mA	-15		+15	%
4.5-15	AINx	current accuracy, VAS mode	Fixed current mode, I_AINx = 5...9 mA	-8		+8	%
4.5-6	AINx	current accuracy, VAS mode	Fixed current mode, I_AINx > 9mA	-5		+5	%
4.5-7	AINx	saturation voltage, VUP mode	I_AINx = -9mA (VUP fixed voltage mode)	0.4		4.0	V
4.5-8	AINx	current limitation, VUP mode	VUP fixed voltage mode	-10		-13	mA
4.5-9	AINx	output current min, VUP mode	Fixed current mode, set = 0011		3.0		mA
4.5-10	AINx	output current max, VUP mode	Fixed current mode, set = 1111		9.0		mA
4.5-11	AINx	current accuracy, VUP mode	Fixed current mode, I_AINx < 5mA	-15		+15	%
4.5-12	AINx	current accuracy, VUP mode	Fixed current mode, I_AINx ≥ 5mA	-8		+8	%
4.5-13	AINx	pull down current source	1V < V_AINx < 33V	100	160	200	uA
4.5-14	AINx	I_AINx	neg. current (without ASIC malfunction, not be tested in series production)			-100	mA

The electrical ADC characteristics of the AIN module are defined in chapter 4.7

## 4.6 Analog I/O (AIO)

The two AIO ports AIO1 and AIO2 are independent current sinks. They are programmable to sink currents between 0mA and 70mA, adjustable via a software command for each port. The current sinks can be pulse width modulated between 0% and 100%. Additionally, the second AIO port can be coupled to the first AIO port so that software commands of the first port can control both ports simultaneously.

With an initial software command, PROG\_AIO1 and PROG\_AIO2, the outputs can be set under control of DIS\_ALP (warning lamp mode).

### 4.6.1 Current levels at AIOx

Each AIO port can be programmed independently to sink currents between 0mA and 70mA in steps of 4.7mA. The digital values can be calculated using the following formula:

$$I_{\text{AIO}} [\text{mA}] = I_{\text{AIO,programmed}} \times \text{accuracy} [\%] + \text{offset} [\text{mA}]$$

### 4.6.2 Voltage measurement at AIOx

The voltage at each AIO port can be measured using the internal A/D converter. Therefore, the voltage at each AIO port is divided by an internal resistor voltage divider. The absolute voltage is A/D-converted and can be read by the µC via SPI as a 10bit value. The voltage range for both AIO ports is 0V...30V. The typical resolution for the voltage measurement at AIOx ( $x = 1, 2$ ) is 34.13LSB/V. The digital values can be calculated using the following formula:

$$\text{ADC}_{\text{typ}} [\text{LSB}] = \text{resolution} [\text{LSB}/\text{V}] \times V_{\text{AIO}} [\text{V}] + \text{offset} [\text{LSB}]$$

### 4.6.3 AIO short detection

A comparator at each AIO port is implemented that compares the voltage at the AIO pin with an internal voltage threshold. With this comparator it is possible to detect a short circuit at the pin. In case the PWM mode is active, the comparator checks if the level is below the threshold during the ON phase and checks if the level is above the threshold during the OFF phase, using two independent counters.

During the ON phase and in normal operation, the voltage at the AIOx pin is expected to be lower than the threshold voltage of the short detection comparator. In case the voltage at the AIOx pin is higher (lower) than the threshold voltage of the short detection comparator, an internal 9-bit counter is incremented by (decremented) every 12.5 us. As soon as this internal counter reaches 160, which corresponds to a time of 2 ms, a short to supply is qualified and flagged in the corresponding SPI register. Automatic deactivation of the interface occurs once the counter reaches 320, which corresponds to a time of 4 ms.

During the OFF phase and in normal operation, the voltage at the AIOx pin is expected to be higher than the threshold voltage of the short detection comparator. In case the voltage at the AIOx pin is lower (higher) than the threshold voltage of the short detection comparator, an internal 8-bit counter is incremented (decremented) every 12.5 us. As soon as this internal counter reaches 160, which corresponds to a time of 2 ms, a short to ground is qualified and flagged in the corresponding SPI register.

The port status can be read back by SPI command AIOx\_STATUS. After the automatic turn-off, the port can only be turned again by SPI command AIO\_LIN\_EN. The port remains undamaged up to 18 V at the maximum current.

### 4.6.4 PWM frequency selection

The PWM frequency can be selected via SPI command PROG\_SAFETY. The frequency can be set to 100 Hz, 200 Hz, 266 Hz, or 400 Hz with tolerances based on the ECLK tolerance.

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## 4.6.5 Application notes

### Maximum Power Dissipation of AIOx

The maximum static power dissipation for one AIOx channel is 500mW. The power dissipation of both AIOx channels has to be included in the calculation of the power dissipation of the complete ASIC to ensure a maximum chip junction temperature.

### Drop-Voltage

To drive the maximum current of 70mA within the specified tolerance-band the minimum voltage at the respective AIOx port may not be lower than the maximum AIO drop voltage (please see AIO electrical characteristics for details).



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## 4.6.6 AIO SPI Instructions

Program AIO current and mode:

### SPI instruction PROG\_AIO1...2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	cp	wl_mode	aio_current				
SPI output data	0	0	0	0	0	0	0	0	0	cp	wl_mode	aio_current				

aio\_current:

0 : AIO switched off (default)

1...14:  $I_{AIO} = aio\_current * 4.7mA$

15 : AIO in PWM mode (controlled by internal PWM signal: 0mA / 70mA)

wl\_mode :

00/11 : normal mode, no DIS\_ALP influence (default 00)

01: non inverted warning lamp mode (DIS\_ALP = high => current on)

10: inverted warning lamp mode (DIS\_ALP = high => current off)

cp : AIO coupling (only within PROG\_AIO1):

0 : AIO2 is controlled individually (default)

1 : AIO2 is coupled to AIO1 (AIO1 and AIO2 connected externally)

Please note: In case AIO is controlled by DIS\_ALP but DIS\_ALP is not active (low), AIO can be switched on, nevertheless. In case the inverted warning lamp mode is used, the AIO current should be set to a value higher than zero.

Set AIO PWM duty cycle and mode:

### SPI instruction AIO1...2\_PWM

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	en	fce	pulse_width						
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

pulse\_width: (only used in PWM mode (current=1111), en=1)

0 : no PWM signal, AIO switched off

1...99: AIO signal modulated according pulse width value

≥ 100: no PWM signal, AIO switched on (default)

During a watchdog 1 failure the pulse width is set to 100%.

fce : PWM force:

0 = a pulse width change is synchronized to the next PWM cycle (default)

1 = AIO reacts instantly to a pulse width change

en: 0 = AIO switched off (default), 1 = AIO switched to programmed current

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Read AIO status:

## **SPI instruction AIO1...2\_STATUS**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	vzl	0	0	0	0	0	0	0	0	0	0	off	on	aio_status		

aio\_status = xx1 : short between AIO pin and supply

aio\_status = x1x : short between AIO pin and ground

aio\_status = 1xx : AIO pin has been switched-off due to short to supply detection

on : 0 = AIO is/was not switched on, 1 = AIO is/was switched on (since last read)

off : 0 = AIO is/was not switched off, 1 = AIO is/was switched off (since last read)

vzl : 1 = VZP too low, 0 = VZP OK (status at the moment of shortcut evaluation)

All bits are cleared by reading.

Reset short current switch-off at AIO1, AIO2 and LIN:

## **SPI instruction AIO\_LIN\_EN**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	In	a2	a1
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

a1, a2, In = 1 : re-enable AIO1, AIO2 and LIN interface after short current switch-off

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## 4.6.7 AIO Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
4.6-1	AIOx	input current	current_set = 0000		0		mA
4.6-2	AIOx	input current	current_set = 0001		4.7		mA
4.6-3	AIOx	input current	current_set = 0010		9.4		mA
4.6-4	AIOx	input current	current_set = 0100		18.8		mA
4.6-5	AIOx	input current	current_set = 1000		37.6		mA
4.6-6	AIOx	input current	current_set = 1111 (max current)		70.5		mA
4.6-7	AIOx	leakage current	AIOx $\leq$ 36V	-20		20	uA
4.6-8	AIOx	drop voltage	I_AIOx max (current_set = 1111)		0.5		V
4.6-9	AIOx	current accuracy	I $<$ 5mA	-15		+15	%
4.6-10	AIOx	current accuracy	I $\geq$ 5mA	-10		+10	%
4.6-11	AIOx	current offset	all currents	-0.3		+0.3	mA
4.6-12	AIOx	resolution	voltage measurement	-3%	34.1	+3%	LSB/V
4.6-13	AIOx	offset	voltage measurement	-5		+5	LSB
4.6-14	AIOx	I_AIOx	neg. current (without ASIC malfunction, not to be tested in series production)			-100	mA
4.6-15	AIOx	short detection	voltage threshold	2.7	3.0	3.3	V
4.6-16	AIOx	short detection filter time	filter time between occurrence of short and writing AIOx_STATUS data registers	2		2.2	ms

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## 4.7 AINO measuring unit

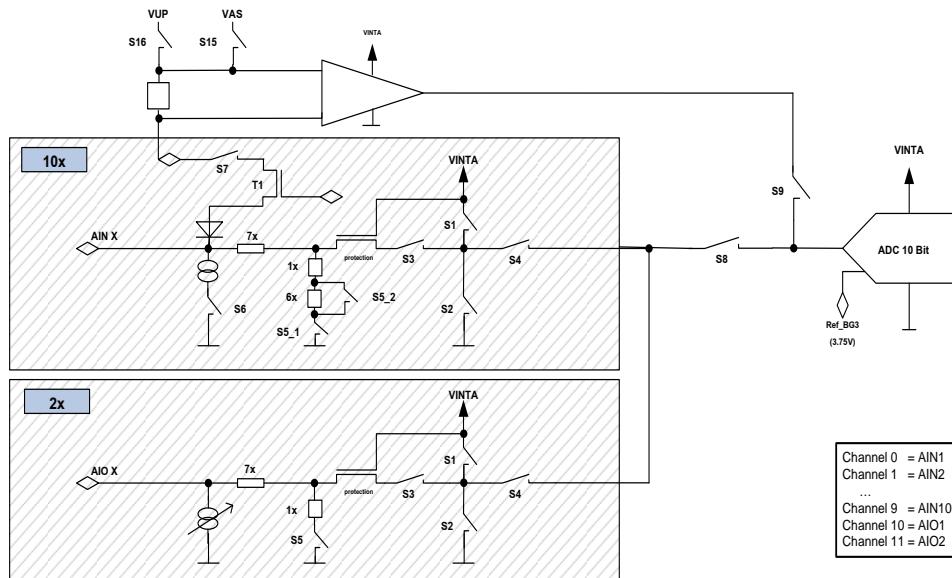
With the AINO measurement unit it is possible to measure external components on the pins **AINx** and **AIOx**. Those can be external resistors, hall sensors or fixed voltage sources. For the measurements on **AIN1-10** the measurement condition can be defined by SPI command **PROG\_AINO\_CONFIG1-10**.

The measurement itself is implemented automatically with all 12 AIN/AIO channels in a row. The procedure is described in the referring chapter. Each pin is measured within a time of approx. 1ms. In this time the programmed condition is applied on the pin and an A/D conversion is done. The result is stored in a dedicated SPI register.

### 4.7.1 AINO Block diagram

The AINO Block connects the AIN/AIO pins or the measurement shunt to the ADC. This connection is only active when an AINO measurement is done.

The current and voltage measurement is done using the same ADC, but with different paths. For current measurement the voltage drop of an internal resistor is amplified to the ADC's input range, for voltage measurement an internal voltage divider reduces to the ADC's input.



AIO has no internal AIN current source, no measurement shunt and no 160 $\mu$ A pull-down current sink (only the AIO current sink). Therefore neither supplied mode (fixed voltage or fixed current) is available. Also current measurement is not possible at AIO. The internal AIO current sink is not controlled by AINO measurement logic, but only by AIO logic.

### 4.7.2 AINO in combination with AIN current source

An internal current source is implemented which can be connected to all AINs. The current can be programmed with 4 Bits. The current source can be configured to be supplied out of VAS (approx. 6.7V) or VUP (approx. 32V). The regulation itself is done with transistor T1 and a shunt

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resistor. With this external components (e.g. resistors, hall sensors) can be supplied to measure their current or voltage. 3 supply modes are available: fixed voltage, fixed current or no source.

The measurement unit consists of 2 separate paths. One is a voltage divider which reduces two voltage ranges (0-7,5V with VAS and 0-30V with VUP) to 0-3.75V. The divider factors (1/8 and 1/2) can be selected by programming. Afterwards an active clamp ensures a save voltage range. This voltage is measured by the ADC.

The second path is used to measure the current flowing out of the pin AINx. The voltage drop over a shunt resistor is amplified by factor 12.5 to a voltage range 0-3.75V. This voltage can also be measured by the ADC.

## 4.7.3 Voltage measurement at AINx, AIoX

The voltage on the pin is put through a restrictive voltage divider and the voltage afterwards is A/D converted. This can be done using automatic measurement (using AINO\_START\_AUTO) or manual (using ADC\_START\_AINO). The result can be read via SPI as a 10bit value.

In case of AIN with “fixed voltage supplied by VAS” or “fixed current supplied by VAS” the divider 1:2 is used (input range 0 to 7.5V). In all other cases the divider 1:8 is used (input range 0 to 30V). In case of AIo only a divider 1:8 is used (input range 0 to 30V).

With divider 1:2 the internal resistance is >120k Ohm, with divider 1:8 the internal resistance is >70k Ohm. During voltage measurement the internal current sink is detached from the pin.

The typical adc\_resolution of the ADC is 3.66 mV/LSB. For voltage measurement at AINx with range 0-7,5V this is equal to 136.53 LSB/V, for AINx and AIoX range 0-30V this is equal to 34.13 LSB/V.

$$\begin{aligned} \text{ADC\_typ[LSB]} &= (\text{div\_factor}/\text{adc\_resolution}) * \text{V\_ain [V]} \\ \text{ADC\_typ[LSB]} &= 136.53 \text{ LSB/V} * \text{V\_ain [V]} && \text{with range } 0\dots7.5\text{V} \\ \text{ADC\_typ[LSB]} &= 34.13 \text{ LSB/V} * \text{V\_ain/o [V]} && \text{with range } 0\dots30\text{V} \end{aligned}$$

Tolerances for gain error and offset error are given in the referring chapter.

## 4.7.4 Current measurement at AINx

The current is wired through a shunt resistor of 10 Ohm. The voltage drop is amplified by factor 12.5 to a range of 0 – 3.75V and an offset of approx. 50mV is added. This voltage is A/D converted. This can be done using automatic measurement (using AINO\_START\_AUTO) or manual (using ADC\_START\_AINO). The result can be read via SPI as a 10bit value.

During automatic measurement the current measurement is performed by doing 2 current measurements: one with the AINx connected to the shunt and another with all AINx disconnected from the shunt. The difference of both is the offset compensated result of the current measurement. The manual measurement has no offset compensation. If needed two measurements have to be done and the results have to be subtracted in the µC.

The typical adc\_resolution of the ADC is 3.666 mV/LSB. For current measurement at AINx this is equal to 34.1 LSB/mA.

$$\begin{aligned} \text{ADC\_typ[LSB]} &= 125\text{mV/mA} * (1/\text{adc\_resolution}) * \text{I\_ain [mA]} \\ \text{ADC\_typ[LSB]} &= 34.1 \text{ LSB/mA} * \text{I\_ain [mA]} && \text{with range } 0\dots30\text{mA} \end{aligned}$$

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Tolerances for gain error and offset error are given in the referring chapter.

Current measurement is only possible with active AIN current source (fixed current or fixed voltage).

## 4.7.5 Resistance measurement at AINx

Measuring resistances connected to an AIN channel is basically a subset of the voltage measurement. When using “fixed current mode” in PROG\_AINO\_CONFIG1...10 the current source supplies the external resistor with a defined current and a voltage is generated on pin AINx. This voltage is digitalized with a normal voltage measurement as described above.

$$V_{\text{ain}} [\text{V}] = I_{\text{ain\_prog}} [\text{A}] * R_{\text{meas}} [\Omega]$$

Tolerances for gain error and offset error are given in the referring chapter. This does not include the error of the current source.

## 4.7.6 AINO measurement sequences

The AINO has automatic measurement sequences and build-in-tests (BIST) implemented. These are started by SPI and their results can be read by SPI after the measurements are finished.

## 4.7.7 AINO Measurement: Automatic sequence

An automatic measurement sequence is implemented. With this all AINx and AIox can be measured in a row.

The measurement conditions for each channel are defined by PROG\_AINO\_CONFIG1...12. Channels with mode setting “00” are not measured (default). In this case the pin settings are not changed at all (no internal change of capacity, resistance or current).

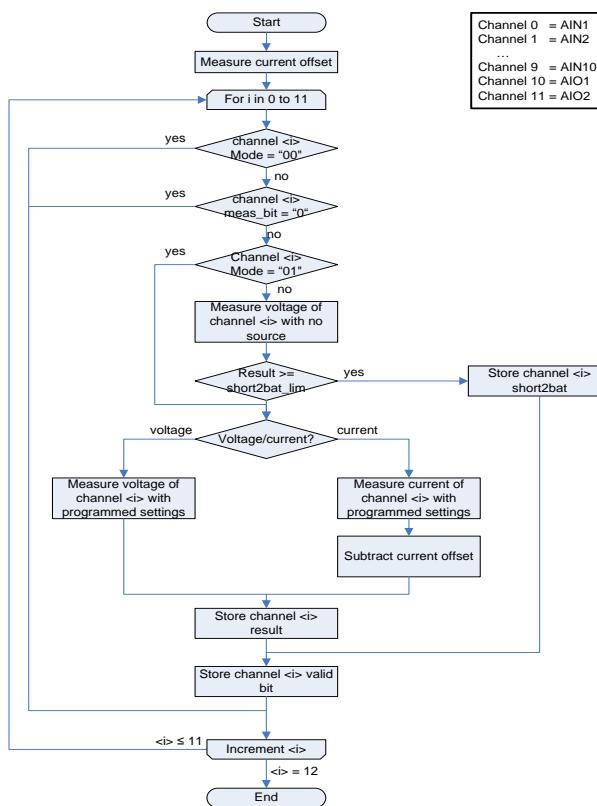
The sequence is started with AINO\_START\_AUTO. Each channel can be excluded from measurement by not setting the referring Bit. The behavior within the sequence is as if the mode setting for this pin is “00”. This might be used when a failure is detected and a channel must not be switched on (e.g. after EOP).

The sequence itself is fixed. When channels are not measured the timing frame simply stays empty without doing anything. The length of the sequence is  $0.5 + 12 * 1.5\text{ms} = 18.5\text{ms}$ . For synchronization with the ADC time frames there is a time of  $0\dots 500\mu\text{s}$  until the sequence starts, so that the sequence is finished max 19ms after the start.

The results can be read after at least 19ms after the start using AINO\_READ\_AUTO1...12. This will clear the valid bit for the referring channel. With the bit “sds” the influence on the SDIS\_S (hardware path) can be switched on/off (see referring chapter). The results will be cleared with each start of the measurement sequence.

The AINO busy flag will stay “1” for 18.5...19ms. Any starting command (START\_AINO\_AUTO, START\_AINO\_BIST and ADC\_START\_AINO) will be ignored while the busy flag is “1”.

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A current offset measurement is implemented. This is necessary to compensate any internal leakage currents. This is done using the internal current source in VAS and hall mode without connecting any pin to the source and doing a current measurement. The result is stored as offset which is subtracted from all following current measurement. If the offset measurement is >100LSB the valid bit of all following current measurements will not be set (error indicator). Negative values after the subtraction will be set to 0.

A Short2bat detection is implemented. This is only done when the measurement needs the internal current source to be activated. An external short would interfere with the programmed measurement or might even damage internal circuits. So a voltage measurement checks if the AINx are > 3V. If so the short2bat flag will be set for this pin and the following measurement on this pin will not be done.

For pure voltage measurement without internal source (mode = 01) the short2bat detection will not be done. In this configuration the voltage is set from the outside, so the short2bat test would interfere with this measurement.

The programmed measurement itself takes 1 ms. The previously configured conditions are applied at the referring pin for the whole 1 ms. The first 900 $\mu$ s are needed to charge external components. If the external components are not fully charged within this time, a sampling error will occur which adds to the tolerances of the measurement. This might happen if external R and C are too large. During the last 100 $\mu$ s the ADC conversion is made. The timing of the ADC is described in the referring chapter.

During the automatic AINO measurement two voltages from POM block are checked. The status of VZP\_L is stored at the exact time of the short2bat detection. If the short2bat detection is not done (mode = 01), the bit simply stays low. VZP\_L is stored for every channel individually. The status of VUP\_LF is stored at every time a result of an auto AINO measurement is stored.

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There is only one VUP\_LF flag for all channels. The flags will be cleared with each start of the measurement sequence.

## 4.7.8 AINO Measurement: manual sequence

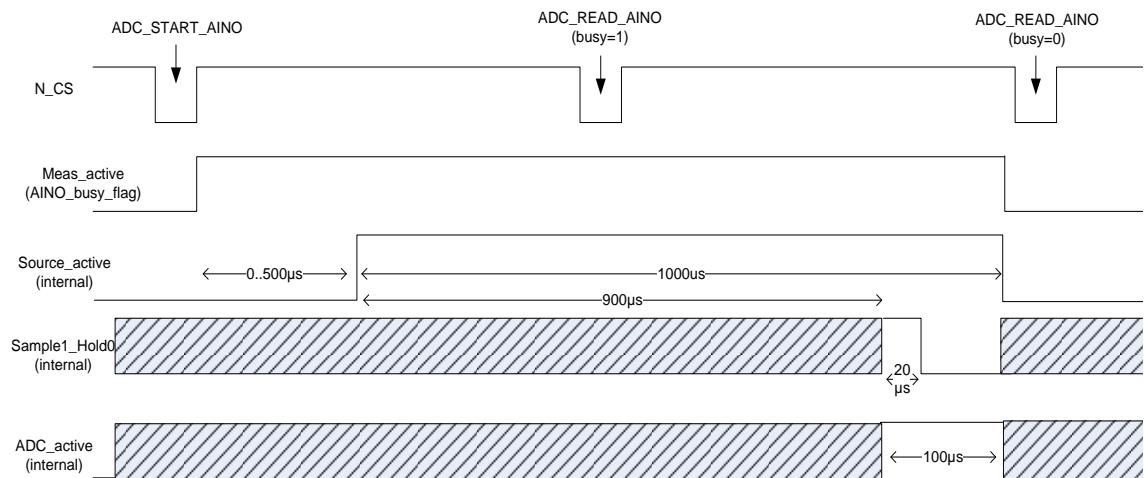
Manual AINO measurement is implemented as backup for the automatic measurement. It gives the possibility to do any single measurement of the automatic AINO sequence (started with AINO\_START\_AUTO) and most of the AINO BISTs (started with AINO\_START\_BIST).

All necessary settings for the measurement are defined within the ADC\_START\_AINO command. The only exception is the programmed current to be used when using the AIN current source. This is defined by the referring PROG\_AINO\_CONFIG1...12 of the channel to be measured.

The timing of a manual AINO measurement is always 1 ms. For synchronization with the ADC time frames there is a time of 0...500 $\mu$ s until the measurement starts. The test condition is always applied for 1 ms. During the first 900 $\mu$ s external components are charged. If the external components are not fully charged within this time, a sampling error will occur which adds to the tolerances of the measurement. This might happen if external R and C are too large.

During the last 100 $\mu$ s the ADC conversion is made. The timing of the ADC is described in the referring chapter. The status of the ADC outside this 100 $\mu$ s window is controlled by other modules.

The result of the measurement can be read 1.5ms after the start using ADC\_READ\_AINO. With the bit "sds" the influence on the SDIS\_S (hardware path) can be switched on/off (see referring chapter). The AINO busy flag will stay "1" for 1..1.5 ms. Any starting command (START\_AINO\_AUTO, START\_AINO\_BIST and ADC\_START\_AINO) will be ignored while the busy flag is "1".



During the manual AINO measurement two voltages from POM block are checked. The status of VZP\_L and VUP\_LF are stored at the same time the AINO measurement result is stored.

Known discrepancies of the manual measurement:

- Current measurements have no offset compensation
- Measurement time is always 1 ms (+ 0.5ms for synchronization). Short2bat, short2gnd and most BIST measurements are performed with 0.5 ms only.

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- Short2bat and short2gnd measurements on external BIST are made with voltage divider 1:2, with manual measurement are only with factor 1:8 possible

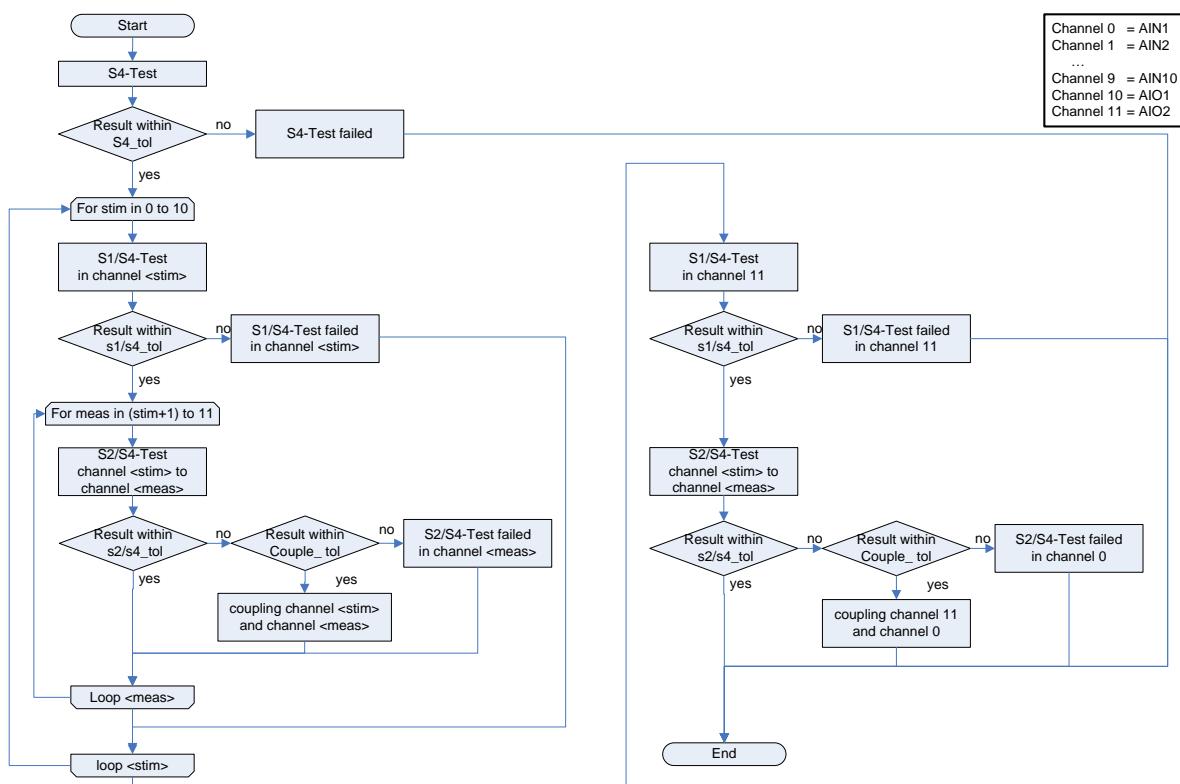
## Application Note:

The use of the automatic sequence should always be preferred.

### 4.7.9 AINO BIST: internal cross coupling test

An automated build in self test is implemented to identify any internal shortcuts or cross couplings. Therefore a complex sequence performs a number of measurements where all internal switches in the AINO multiplexer are tested. The test itself is done by applying certain voltage levels at different points within the circuit and using the ADC to measure the resulting level. If any test is outside the expected range, the referring channel(s) are identified as failed.

The internal coupling test is started with the SPI command AINO\_START\_BIST using mode = 001. All channels are tested. The bits for the channel selection have no influence in this mode. The test takes a fixed time of 40 ms plus max 0.5 ms for synchronization. The result can be read using SPI command AINO\_READ\_BIST1-3 at least 40.5ms after the start command. The first command report the S1/S4 fails, the second the S2/S4-fails and the third the channel couplings.



For the following explanations please refer to the AINO block diagram.

S3 is open during the whole internal coupling test. So external components or the internal current sink on AINx and cannot interfere with the test. These switches have to be checked by external coupling or capacitance test.

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## S4-Test:

All S4 are open, all S2 are closed. An internal voltage of  $\frac{3}{4} * V_{ref3\_test}$  (approx. 2.8V) is applied on the output of the AINO multiplexer over a resistor of approximately 70k Ohm (see chapter ADC linearity test). Any closed S4 or a low-resistive coupling of the multiplexer output to any internal voltage would influence the measurement and cause the measurement to fail S4-Test. Ideal value should be 768 LSB.

## S1-S4-Test:

All S4 are open. In one channel S1 and S4 is closed. The resulting voltage on the output of the AINO multiplexer should nominally be  $> 3.75V$ . If S1 and S4 are not closed or a low-resistive coupling to ground exists (e.g. S2 is not open), the measurement will fail S1-S4-Test. Ideal value should be 1023 LSB.

## S2-S4-Test:

All S1, S2 and S4 are open. Channel  $<i>$  S1 and channel  $<j>$  S2 and S4 are closed. The resulting voltage on the output of the AINO multiplexer should nominally be  $< 0.7 V$ . If S4 in channel  $<i>$  is not fully opened, S1 in channel  $<j>$  is not fully closed or both channels are coupled with low resistance, the output should normally be approx 1.65V (with ideal coupling voltage divider channel  $<i,j>$  S1 and channel  $<j>$  S2). Both channels will then be marked as coupled. If S4 and S2 in channel  $<j>$  are not fully closed the test will fail S2-S4-Test.

## 4.7.10 AINO BIST: external cross coupling test (master mode)

An automated build in self test is implemented to identify any external shortcuts or cross couplings on the AINx. Therefore a complex sequence performs a number of measurements where the AINx are stimulated by the internal current source and using the ADC to measure the resulting level. If any test is outside the expected range, the referring channel(s) are identified as failed.

The AIOx are not tested during this test. Due to the different application the external circuit on the AIOx is not compatible to the testing flow and will likely fail. They have to be tested with the possibilities the AIO provides.

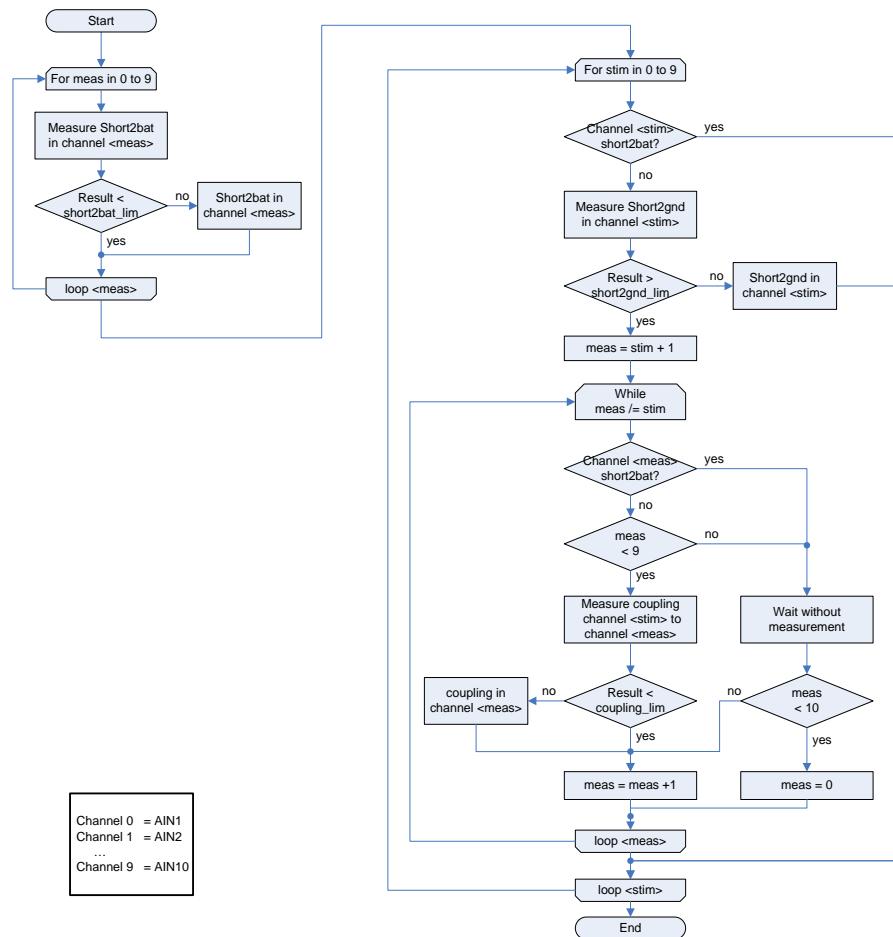
The test result depends on the external components attached. The basic idea of this test is to check if the pin voltage on the AINx can be forced below and above approx. 1V by switching the internal current source. If both are possible, then the pin is forced above 1V and all other AINx are measured whether they are influenced by this pin.

The test might fail if the external circuit contains:

- A fixed voltage  $> 1V \Rightarrow$  short2bat
- A low resistive switch to gnd  $\Rightarrow$  short2gnd
- And RC combination which is not able to be charged above 1V in 400 $\mu$ s  $\Rightarrow$  short2gnd
- Other reasons are possible

The external coupling test is started with the SPI command AINO\_START\_BIST using mode = 100. The bits for the channel selection define the ones to be tested. Each channel which is not selected is not stimulated and not measured.

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First the voltages on all AINx are measured with no source activated. When only passive components are connected at the AINx, the pin voltage should be approximately 0V. If a voltage > short2bat\_lim is detected, an external source is forcing the pin from outside and a short2bat flag is set. Any pin where a short2bat is detected will not be stimulated or measured in the following sequence.

Afterwards each pin will be activated with fixed voltage mode and source VAS for 6ms each. The voltage on the stimulating pin should rise, while the voltage on the other pins should not. During this time the voltage of all 10 AINs are measured. The voltage on the stimulating pin should be nearly VAS-level, the voltage on the other nearly 0V. If the voltage on the stimulation pin is below short2gnd\_lim, a short2gnd flag is set for this pin and will not be stimulated or measured in the following sequence. If the voltage on any other pin is above coupling\_lim, a coupling flag is set for this pin. The coupling flag for the stimulating pin will not be set.

The test takes a fixed time of 65 ms plus max 0.5 ms for synchronization. The result can be read using SPI command AINO\_READ\_BIST5-6 at least 65.5ms after the start command. The first command report the short2bat fails, the second the short2gnd and the third the channel couplings.

## 4.7.11 AINO BIST: external cross coupling test (slave mode)

An automated build in self test is implemented to identify any external shortcuts or cross couplings on the AINx in applications with multiple system ASICs. The exten cross coupling test as slave should be done while another chip is doing its external cross coupling test as master. The other chip is stimulating its AINx by using the internal current source. The slave performs only short2bat measurements to identify those AINx which might be affected by the master chip's test. The measurement is done using the ADC to measure the resulting level on the AINx. If any test is outside the expected range, the referring channel(s) are identified as failed.

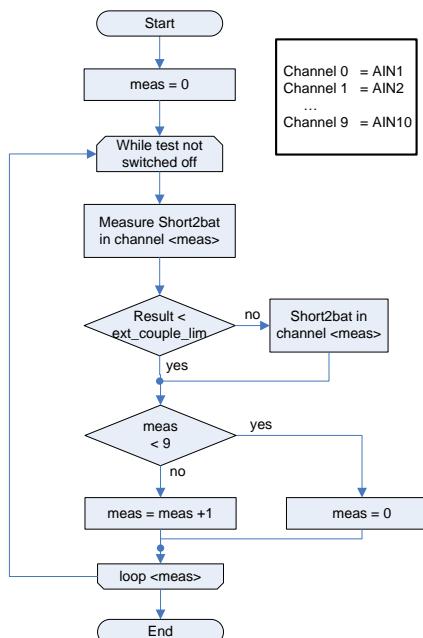
The AIOx are not tested during this test. Due to the different application the external circuit on the AIOx is not compatible to the testing flow and will likely fail. They have to be tested with the possibilities the AIO provides.

The test result depends on the external components attached. The basic idea of this test is to check if the pin voltage on the AINx stays below approx. 1V while other external lines on the ECU are forced above. So if the external components interfere with this condition the test might fail.

The test might fail if the external circuit contains:

- A fixed voltage > 1V => short2bat
- Other reasons are possible

The external coupling test is started with the SPI command AINO\_START\_BIST using mode = 101. The bits for the channel selection define the ones to be tested. Each channel which is not selected is not stimulated and not measured. The test does not end automatically. Is has to be switched off by sending AINO\_START\_BIST using mode = 000.



A test cycle takes 5 ms for all AINx, so any external line which a cross coupling should be detected to needs to be stimulated for longer than that. This includes the time needed to charge

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external components on the stimulated line. The result can be read using SPI command AINO\_READ\_BIST5 during running test or after it has been switched off.

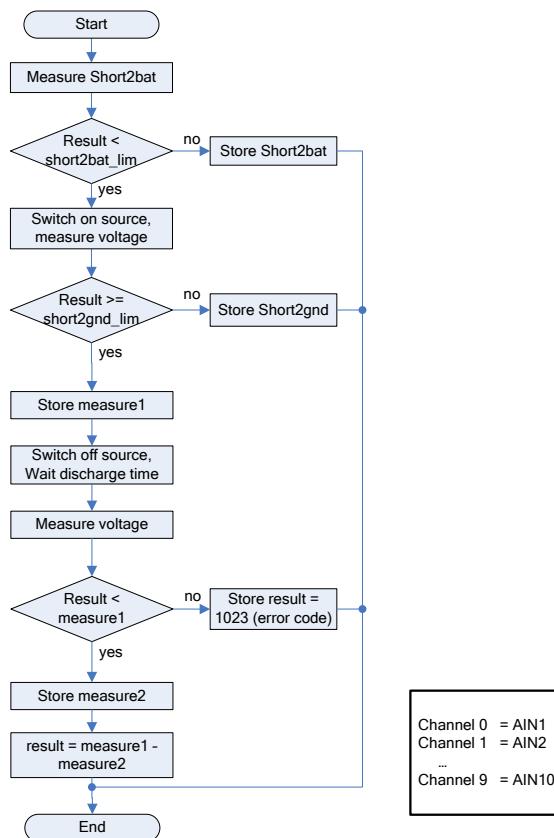
Remark: The external coupling test as master uses 6 ms for stimulating each channel. The external coupling test as slave uses 5 ms for measuring all channels.

## 4.7.12 AINO BIST: external capacitance test

An automated build in self test is implemented to verify the connection of external capacitance at AINx during ECU production test. Each time the test is started only one AINx is measured.

The external capacitance test is started with SPI command AINO\_START\_BIST using mode = 011. The pin to be measured is coded in the bits cx. If multiple channels are selected the SPI command is ignored.

The test takes a fixed time of 2 ms plus max 0.5 ms for synchronization. The result can be read using SPI command AINO\_READ\_BIST5-7 at least 2.5ms after the start command. The first command report the short2bat fails (coded in lowest bit) and the second the short2gnd (coded in lowest bit). The third is the difference of the 2 voltage measurements, one with the internal current source active and another after discharging the capacitance for a fixed amount of time.



First the voltage of the selected pin AINx is measured with no source activated. When only passive components are connected at the AINx, the pin voltage should be approximately 0V. If a voltage  $>$  short2bat\_lim is detected, an external source is forcing the pin from outside and a short2bat flag is set. If a short2bat is detected the pin will not be stimulated or measured in the following sequence.

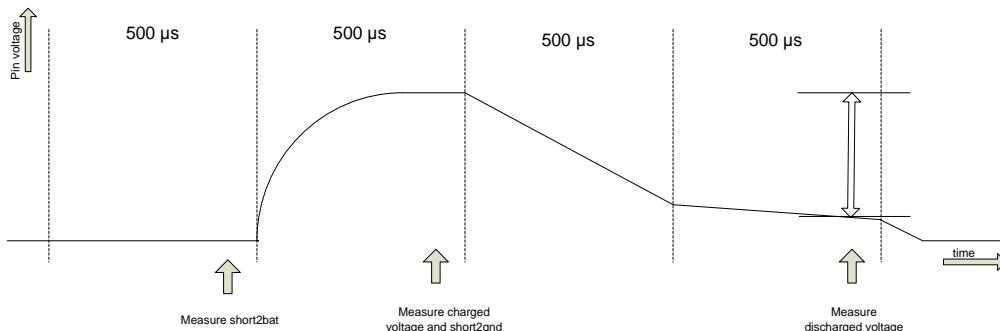
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Afterwards the current source pin will be activated with fixed voltage mode and source VAS for 500 $\mu$ s each. The external capacitance is charged and the voltage on the pin should rise. The voltage is measured within the last 100 $\mu$ s of this time and stored as measure1. If the external capacitance is not fully charged within 400  $\mu$ s, then a sampling error will occur which adds to the tolerances of the measurement. This might happen if external R and C are too large.

Now the internal current sink is switched on for 500 $\mu$ s to discharge the capacitance with nominal 150 $\mu$ A and the pin voltage will reduce. This reduced will be A/D converted. Therefore the voltage divider is connected and the internal voltage sink disconnected from AlNx for the next 500 $\mu$ s, while the A/D conversion is done in the last 100 $\mu$ s of this time. The voltage divider additional discharges the capacitance with nominal 25 $\mu$ A which has to be taken into account. The result of this measurement is stored as measure2.

The result of the capacitance test is the difference measure1 minus measure2. If measure2 is larger than measure1 the result will be set to 1023 (error code). This value cannot occur in normal function. Smaller difference indicates larger capacitance.



The accuracy of this test is limited because the saturation voltage of the current source, the internal resistance and the current sink has a huge production tolerance and do change over temperature. If the external components are not fully charged within 400  $\mu$ s, a sampling error will occur which adds to the tolerances of the measurement. This might happen if external R and C are too large.

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## 4.7.13 AINO SPI Instructions

Program AIN/AIO measurement configuration:

### **SPI instruction PROG\_AINO\_CONF1...12**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	mode	ui	src	current_level				
SPI output data	0	0	0	0	0	0	0	0	mode	ui	src	current_level				

Channel 1...10 (AIN):

current\_level : current level

src : voltage source : 0 = VAS, 1 = VUP

ui : select between voltage and current measurement : 0 = voltage, 1 = current

mode : measurement mode: 00 = no meas., 01 = no source, 10 = fix current, 11 = fix voltage

Channel 11...12 (AIO):

mode : measurement mode : 00 = no meas., 01 = no source

The channel address is coded within the least 4 bits of the instruction.

The default value of this register is zero.

Start AIN/AIO automatic measurement:

### **SPI instruction AINO\_START\_AUTO**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cx : enable channel x for automatic measurement : 0...9 = AINx, 10...11 = AI0x

The instruction is ignored in case all cx bits are zero.

Read AIN/AIO automatic measurement results:

### **SPI instruction AINO\_READ\_AUTO1...12**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	sds
SPI output data	vzl	0	0	s2b	sup	vd	adc_data									

adc\_data : adc result

vd : valid : 1 = adc data are valid, 0 = adc data are old or invalid

sup : supply error : 1 = supply for measurement was too low (VUP)

s2b : short to battery : 1 = short

sds : 0 = no influence on SDIS\_S, 1 = influence according to PROG\_SW\_MODE

vzl : 1 = VZP too low, 0 = VZP OK (status at the moment of shortcut evaluation)

The valid bit vd is set directly after the referring channel measurement is done. The valid bit vd is cleared on read.

All measurement results are cleared by the SPI instruction AINO\_START\_AUTO.

The vzl flag is a single flag for all AIN channels and cleared by the SPI instruction AINO\_START\_AUTO.

The channel address is coded within the least 4 bits of the instruction.

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Start AIN/AIO build-in self test:

## **SPI instruction AINO\_START\_BIST**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	-	-	-	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0	mode		
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cx : enable channel x for build-in self test : 0...9 = AINx

mode:

000 = stops external cross coupling test slave

001 = internal cross coupling test, cx bits will be ignored

010 = ADC BIST (5 internal reference voltages), cx bits will be ignored

011 = connector capacitor test, only one cx bit must be set, no test if all cx bits are zero

100 = external cross coupling test master, no test if all cx bits are zero

101 = external cross coupling test slave (runs continuously) , no test if all cx bits are zero

Read AIN/AIO build-in self test results:

## **SPI instruction AINO\_READ\_BIST1...7**

	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	vzl	0	0	err	channel_result											

Unless otherwise stated channel\_result bit 11...10 map to AIO 2...1, bit 9...0 map to AIN 10...1.

Bits which are not mentioned to in the referring line are set to 0.

1 : result of internal cross coupling test : S1/S4 error (channel\_result(11-0) , err = S4 failure )

2 : result of internal cross coupling test : S2/S4 error (channel\_result(11-0) , err = S4 failure)

3 : result of internal cross coupling test : cross coupling detected (channel\_result(11-0) )

4 : result of ADC bist (channel\_result(4..0) = channel 5 ..1 out of range)

5 : result of connector capacitor test : short to ubat (channel\_result(9-0) )

5 : result of external cross coupling test master : short to ubat (channel\_result(9-0) )

5 : result of external cross coupling test slave : short to ubat (channel\_result(9-0) )

6 : result of connector capacitor test : short to ground (channel\_result(9-0) )

6 : result of external cross coupling test master : short to ground (channel\_result(9-0) )

7 : result of connector capacitor test : difference of voltage measurement (channel\_result(9-0) )

In case of a negative value, channel\_result(9-0) is set to 1111111111

7 : result of external cross coupling test master : cross coupling detected (channel\_result(9-0) )

5 & 6: vzl : 1 = VZP too low, 0 = VZP OK (status at the moment of shortcut evaluation)

The content of channel\_result, err and vzl will be cleared with AINO\_START\_BIST.

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Start manual A/D conversion:

## **SPI instruction ADC\_START\_AINO**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	0	0	src	test_source				ui	-	mode			channel			
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

channel : 0...9 = AINx, 10...11 = AIox, 15 = high impedant

mode:

000 : no test active, no source switched on (normal voltage measurement)

001 : instruction will be ignored

010 : no test active, fixed current source

011 : no test active, fixed voltage source (hall mode)

100 : test active : internal multiplexer test

101 : test active, ADC reference voltages

110 : test active, fixed current source

111 : test active, fixed voltage source

ui : select between voltage and current measurement : 0 = voltage, 1 = current

test\_source : 0...9 = AINx, 10...11 = AIox, 15 = no source

src : voltage source : 0 = VAS, 1 = VUP

Between two ADC\_START instructions a time of 1 ms is required.

Read manual A/D conversion result:

## **SPI instruction ADC\_READ\_AINO**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	sds
SPI output data	vzl	0	0	0	sup	vd	adc_result									

adc\_result : adc data

sds : 0 = no influence on SDIS\_S, 1 = influence according to PROG\_SW\_MODE

vd : valid : 1 = adc data are valid, 0 = adc data are old or invalid

sup : supply error : 1 = supply for measurement was too low (VUP)

vzl : 1 = VZP too low, 0 = VZP OK (status at the moment of shortcut evaluation)

All measurement results are cleared by the SPI instruction ADC\_START\_AINO.

The valid bit vd is cleared on read.

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## 4.7.14 AINO Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
<b>§4.7.7</b>							
4.7-1	AINx	duration	Time aino busy bit stays high	18.5		19	ms
4.7-2	AINx	Resolution (voltage meas)	voltage measurement, source VAS		136.4		LSB/V
4.7-3	AINx	Resolution (voltage meas)	voltage measurement, source VUP or no source		34.1		LSB/V
4.7-4	AINx	Gain error (voltage meas)	compared to voltage on pin	-3		3	%
4.7-5	AINx	Offset error (voltage meas)	compared to voltage on pin	-5		5	LSB
4.7-6	AINx	Resolution (current meas)	current measurement		34.1		LSB/mA
4.7-7	AINx	Gain error (current meas)	compared to current flowing out of pin (source VAS)	-3		3	%
4.7-8	AINx	Offset error (current meas)	compared to current flowing out of pin (source VAS)	-5		5	LSB
4.7-9	AI0x	Resolution (voltage meas)			34.1		LSB/V
4.7-10	AI0x	Gain error (voltage meas)	compared to voltage on pin	-3		3	%
4.7-11	AI0x	Offset error (voltage meas)	compared to voltage on pin	-5		5	LSB
4.7-12	AINx	Short2bat_lim	with divider factor (1:8)		100		LSB
4.7-13	AINx	Short2bat_lim			2.93		V
4.7-14	AINx	offset_lim			100		LSB
4.7-15	AINx	offset_lim			2.93		mA
4.7-16	AINx	R_int (voltage meas, 1:2)	Internal resistance during voltage measurement using divider 1:2	120			kOhm
4.7-17	AINx, AI0x	R_int (voltage meas, 1:8)	Internal resistance during voltage measurement using divider 1:8	70			kOhm
<b>§4.7.8</b>							
4.7-18	AINx	duration	Time aino busy bit stays high	1		1.5	ms
<b>§4.7.9</b>							
4.7-19	intern	duration	Time aino busy bit stays high	40		40.5	ms
4.7-20	AINx	S4_tol		700		800	LSB
4.7-21	AINx	S1/S4_tol		900		1023	LSB
4.7-22	AINx	S2/S4_tol		0		200	LSB
4.7-23	AINx	couple_tol		300		600	LSB
<b>§4.7.10</b>							
4.7-24	intern	duration	Time aino busy bit stays high	65		65.5	ms
4.7-25	AINx	Short2bat_lim	with divider factor (1:2)		140		LSB
4.7-26	AINx	Short2bat_lim			1.03		V
4.7-27	AINx	Short2gnd_lim	with divider factor (1:2)		140		LSB
4.7-28	AINx	Short2gnd_lim			1.03		V
4.7-29	AINx	ext_couple_lim	with divider factor (1:2)		140		LSB
4.7-30	AINx	ext_couple_lim			1.03		V
<b>§4.7.11</b>							
4.7-31	AINx	ext_couple_lim			140		LSB
4.7-32	AINx	ext_couple_lim			1.03		V
<b>§4.7.12</b>							
4.7-33	intern	duration	Time aino busy bit stays high	2		2.5	ms
4.7-34	AINx	Short2bat_lim	with divider factor (1:2)		140		LSB
4.7-35	AINx	Short2bat_lim			1.03		V
4.7-36	AINx	Short2gnd_lim	with divider factor (1:2)		140		LSB
4.7-37	AINx	Short2gnd_lim			1.03		V

### Application Note:

For resistance measurement the tolerances of the output current and the tolerances of the voltage measurement have to be added.



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## 4.7.15 Application Notes AINO

### Mixed supply mode

Each AIN can be used with different supply methods (fixed voltage, fixed current, no source) and different external components. The AIO can only be used with "no source".

With the three methods of supply and the two methods for measurements at AIN, there are different applications possible:

- Measuring Voltages with no supply of the AIN-channels from the chip
- Measuring Currents with fixed-voltage supply
- Measuring Resistances by measuring the voltage at AIN with fixed-current supply.

The following combinations of supply and voltage/current measurement are possible but are not tested in series production. Therefore there are no guaranteed tolerances for these applications:

- Measuring Currents with fixed-current supply
- Measuring Voltages with fixed-voltage supply

The following combination of supply and measurement is not possible:

- Measuring Currents with no supply from the AIN-channels from the ASIC

### Manual AINO measurements

These are possible, but are not tested in series production. Therefore there are no guaranteed tolerances for this application. Automatic measurements should be preferred whenever possible.

### More switches

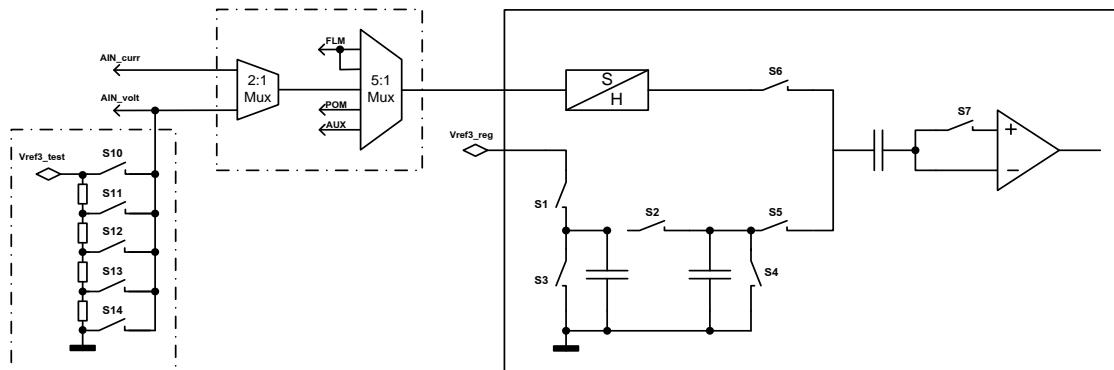
To increase the number of usable switches in the system, external hardware is required. This hardware must be built up as a multiplexer-structure. A channel is selected by the µC directly. Be aware that the testability of this multiplexer must be ensured by the additional hardware and not by the airbag system ASIC.

### External ground

Injection-Currents at the AIN pins have to be avoided. Therefore it is not allowed to connect low-ohmic switches between any AIN pin and an external ground that is not equal to the GND of the ECU.

## 4.8 ADC & Multiplexer

An analog to digital converter is implemented. Its purpose is to measure multiple voltages throughout the chip with the input range of 0...3.75V. The reference voltage is Vref3\_reg (three times bandgap voltage). The ADC is a 10 bit SAR converter with sample&hold. The total conversion time is about 88.5µs



### 4.8.1 ADC multiplexer

The ADC is equipped with a 5-to-1 input multiplexer which puts different sources onto the ADC input. These lines come from following internal modules:

- firing loop module (FLM1)
- firing loop module (FLM2)
- analog input- and output (AINO)
- power module (POM)
- auxiliary (AUX)

Each of the input lines has their own preprocessing and multiplexing structure to measure different voltage ranges and signals within their module. These structures are not controlled by the ADC and will not be described here. Please see the referring module chapters

The multiplexer uses a timeslot technique. The A/D conversion time is less than 100µs long, so all 5 input channels can be measured within 500µs cyclically. The sequence row is the same as the input lines described at the beginning of this chapter. The timeslot selection is done by a simple arbiter with static timing. There is no possibility to change one timeslot to another module.

FLM has two timeslots to be able to make two measurements as fast as possible after each other, but the lines to be measured are identical. AINO has also 3 separated sources. One used during AINO voltage measurement, the next is used during AINO current measurement and the last is used for the internal ADC (linearity) test. All 3 three are required for the AINO internal multiplexer cross coupling test to meet in one line.

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## 4.8.2 A/D converter

The ADC is a 10 bit SAR converter with a conversion time < 100 $\mu$ s. The input of 0...3.75 V is sampled with a sample&hold (S&H) circuit and which holds the value during the actual conversion. The D/A converter is implemented in switched capacity technique charged by Vreg3\_reg, referencing on Ugnd\_quiet. The switches are controlled by digital logic. For each output digit the DAC creates a voltage which is compared to the input, successively approximating the input voltage.

The handshake between modules and ADC are done by an arbiter. The module block needs to send a request to schedule the measurement in the referring timeslot of this module. If no request was sent the measurement will not be done. After the conversion time the module which triggered the conversion receives a trigger to fetch the data.

At most 5 measurements can be done within 500 $\mu$ s. To avoid influence from one measurement to the other the sample&hold is discharged between 2 measurements. If no conversion is scheduled the sample&hold is also discharged, minimizing the number of switching and power consumption.

Here some remarks to the accuracy parameter:

- INL: Is the maximal discrepancy of the result to a best fit line. The INL does not include offset and gain error of best fit line.
- DNL: Is the maximal discrepancy of the actual step size to the ideal step size. Value less than 1LSB guarantees monotonic transfer function with no missing codes.
- Offset error: Value at crossing of best fit line and U=0V.
- Full-scale error: Output discrepancy of best fit line at U=Full-scale voltage (Vref3\_reg)
- Accuracy is defined by Offset error, Full-scale error and INL.

## 4.8.3 ADC linearity test

The ADC is equipped with an internal test source Vref3\_test which is independent from the ADC's own reference Vref3\_reg and is based on a different bandgap. With a voltage divider 5 test voltages are generated which can be A/D converted.

- 1 \* Vref3\_test
- $\frac{3}{4}$  \* Vref3\_test
- $\frac{1}{2}$  \* Vref3\_test
- $\frac{1}{4}$  \* Vref3\_test
- 0 \* Vref3\_test

$\frac{3}{4}$ \* Vref3\_test is also used during AINO internal cross coupling test.

An automated test is implemented to check the ADC. Therefore all 5 internal test voltages are A/D converted and their results compared with fixed limits. The ADC linearity test is started with SPI command AINO\_START\_BIST using mode = 010. The test takes a fixed time of 2.5 ms plus max 0.5 ms for synchronization. The result can be read using SPI command AINO\_READ\_BIST4 at least 3ms after the start command and contains the fail information of the test. If the answer is all 0 the test has passed all voltages.

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## 4.8.4 ADC Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
<b>§4.8.2</b>		<b>A/D converter</b>					
4.8-1	intern	duration of A/D conversion	internal ADC busy flag is high	88.5			us
4.8-2	intern	duration sampling	time S&H is in sampling mode	21.5			us
4.8-3	intern	duration of conversion	times for successive approximation	67			us
4.8-4	intern	discharge time	time S&H is discharged between 2 A/D conversions	12.5			us
4.8-5	intern	conversion rate				10	kHz
4.8-6	intern	resolution			3.666		mV/LSB
4.8-7	intern	Vref3_ref		3.70	3.75	3.8	V
4.8-9	intern	INL	absolute value (not to be measured in series production)			4	LSB
4.8-10	intern	DNL	absolute value (not to be measured in series production)			3	LSB
4.8-11	intern	offset error	offset error best fit line @ 0V	-4		4	LSB
4.8-12	intern	full scale error	error best fit line @ 3.75V (offset + gain error at full scale point)	-14		14	LSB
<b>§4.8.3</b>		<b>ADC linearity test</b>					
4.8-13	intern	duration	time aino busy bit stays high	2.5		3	ms
4.8-14	intern	Vref3_test		3.7	3.75	3.8	V
4.8-15	intern	tolerance ( $1 * V_{ref3\_test}$ )	nom 3.750 V	993	1023	1023	LSB
4.8-16	intern	tolerance ( $\frac{3}{4} * V_{ref3\_test}$ )	nom 2.813 V	738	768	798	LSB
4.8-17	intern	tolerance ( $\frac{1}{2} * V_{ref3\_test}$ )	nom 1.875 V	482	512	542	LSB
4.8-18	intern	tolerance ( $\frac{1}{4} * V_{ref3\_test}$ )	nom 0.938 V	226	256	286	LSB
4.8-19	intern	tolerance ( $0 * V_{ref3\_test}$ )	nom 0.000 V	0	0	30	LSB

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## 5. Functional Description Safety Module (SAM)

The safety module includes the monitoring functionality of the internal clock (watchdog 1), the software tasks (watchdog 2 and 3) and the SPI traffic (monitor SPI). The monitored SPI data is evaluated within the internal safety controller and result in the release of all or dedicated firing loops providing a complete uC independent safety path to the airbag system. Within the safety controller, the timing control of all enable and disable timing, the switch evaluation and the disable lines are included. Furthermore, the safety controller is configurable in a wide range of its functionality.

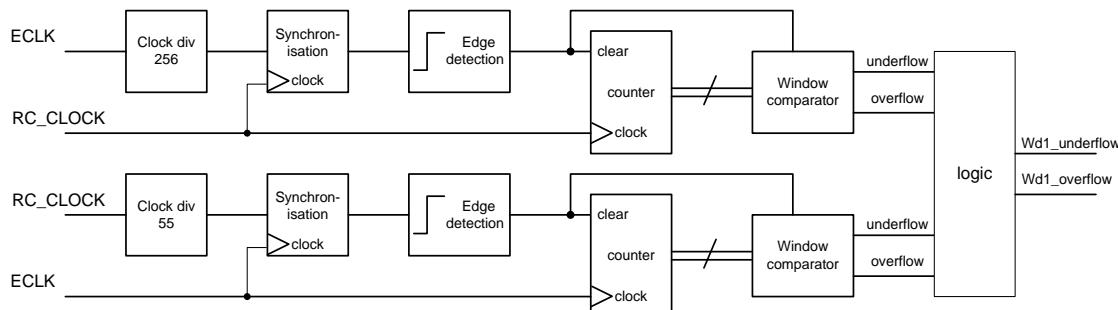
### 5.1 Watchdog

There are three watchdogs implemented. Their tasks are:

- Check ECLK timing by comparing with internal oscillator, detect tear-off
- check the correct sequence of the software (find “crazy” micros)
- check the correct behavior of the µC-kernel (prevent “crazy” micros)

#### 5.1.1 Watchdog 1 (WD1)

A watchdog is implemented to check ECLK timing using internal RC\_CLOCK as reference. The goal is to detect when ECLK frequency is out-of-tolerance or missing at all. Therefore the following structure is implemented



The watchdog1 logic contains 2 parallel paths. One is clocked by ECLK observing RC\_CLOCK, the other is clocked by RC\_CLOCK observing ECLK. The information is combined in two status bits wd1\_underflow and wd1\_overflow. These signals are stored to be read by SPI command WD\_STATUS. The stored information is cleared by reading WD\_STATUS.

A WD1 fault is present, when one of the two window comparators detects an under- or overflow. This fault stays till both window comparators detect no under- and overflow. The GS bit, the reset of Watchdog monoflop affecting DIS\_ALP/DIS\_AHP and the Watchdog reset are directly controlled by WD1 fault.

A WD1 fault disables all highside and lowside firing loops (DIS\_AHP and DIS\_ALP high) even if there was no power-on reset (N\_POR) and there is no system clock (ECLK). Therefore errors at the N\_POR line which can lead to an unstable system are recognized and all firing loops in the system are disabled.

ECLK being to slow results in wd1\_underflow, ECLK being too fast results in wd1\_overflow. The tolerances for wd1\_underflow and wd1\_overflow are pretty large. Within these tolerances the

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behavior of GS bit and WD\_STATUS might differ. GS bit indicates the actual status WD1 fault, while WD\_STATUS is the information that a WD1 fault occurred since the last readout.

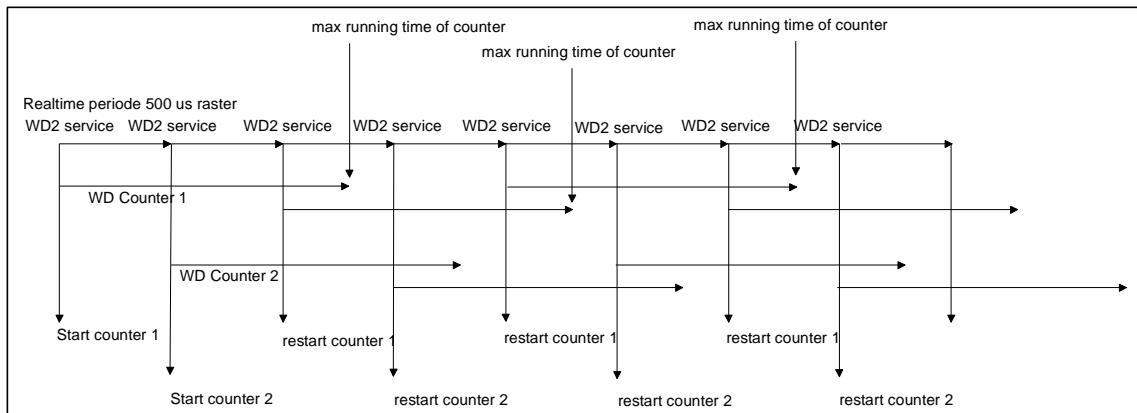
The maximum time to detect a WD1 fault is defined by the tear-off detection time. The same time is needed between fault-case and fault-free-case.

A frequency jitter is implemented for RC\_CLOCK. This jitter can be programmed in multiple configurations. The jitter affects the accuracy of RC\_CLOCK and therefore the function of WD1 detection. The WD1 function is implemented with minimal influence of the jitter on the tolerances for over- and underflow. However, if the configuration is set to active sweep jitter, the WD1 detection tolerances are increased.

## 5.1.2 Watchdog 2/3 (WD2/3)

WD2 and WD3 are both SPI watchdogs. They share the same challenge- and response procedure, but have different requirement on the SPI timing. The task of WD2 is to check the correct functionality and the correct timing frame of the real-time processes and WD3 is monitoring the correct function and the maximum time consumption of the background tasks.

Typically WD2 is served with a timing of nominal 500 $\mu$ s. During high SPI traffic within one real-time frame the time can be significantly larger which has to be compensated within the next frame. Therefore WD2 does not check every successive WD2 transmission, but uses 2 parallel paths. One checks the timing of the even transmissions, the other the timing of the odd transmissions. Both are checking for a nominal timing of 1000 $\mu$ s.



The WD2 consists of two identical upward counting timers. The first counter is used for the even transmissions, the second for the odd transmissions. The counters are set to zero with the referring even/odd WD2 transmission. If a counter exceeds approx. 1300 $\mu$ s it will stop automatically, generating a watchdog overflow. The minimum time between two even or two odd transmissions is approx. 500 $\mu$ s. If the timing is shorter than that, a watchdog underflow is generated.

WD3 checks that the background tasks are not missing. A counter is implemented which is set to zero with any WD3 transmission. If the counter exceeds approx. 96 ms it will stop automatically, generating a watchdog overflow.

The SPI data is used to check the correctness of the  $\mu$ C kernel. It's a simple question and answer game where the ASIC is giving the question and the  $\mu$ C is giving the correct response within the next WD transmission. The idea for the  $\mu$ C is not to use a look-up table to get the correct answer, but to use the basic algebraic functions within the  $\mu$ C kernel to actually calculate

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the result. This will check the internal logic of µC for correct function. If an answer does not match the expected value a WD2 or WD3 bad response flag is set.

WD2 and WD3 both used the same questions and answers, but are totally independent. A WD2 question is answered with the next WD2 transmission, WD3 question with the next WD3 transmission. The questions and corresponding answers are used cyclically using the order of the following table:

<i>n</i>	<i>checkword hex</i>	<i>response hex</i>
1	2020	E106
2	FDFD	9671
3	8A8A	4BAC
4	5757	3CDB
5	ECEC	D235
6	3131	A542
7	4646	789F
8	9B9B	0FE8

The WD2/WD3 underflow, overflow and bad response flag have direct influence on the reset of Watchdog monoflop affecting DIS\_ALP/DIS\_AHP and the Watchdog reset. They are also stored to be read by SPI command WD\_STATUS. The stored information is cleared by reading WD\_STATUS.

### 5.1.3 Further watchdog logic

There are seven different watchdog status bits depending on the functions described in the last chapters. All are stored with the occurrence of an error and cleared by reading WD\_STATUS. The storing and clearing is only possible with ECLK running. Therefore all failure flags are an or-combination of actual status and stored status.

But non-stored flags are or-combined to a single signal wd\_fault. This signal is directly resetting the watchdog monoflop which directly sets DIS\_ALP and DIS\_AHP to high level. The watchdog monoflop is a counter defining a time of 1000ms (or 360ms). Any watchdog fault will trigger the monoflop to run and therefore disable the highside and the lowside of the firing switches until this time is up.

A watchdog fault counter is implemented. This counter is used to store the information of how many watchdog faults are found since power-on-reset. This counter is only reset by power-on-reset and counts up with every wd\_fault while watchdog monoflop is not running (after min 1000ms/360ms correct serving of watchdog). The counter cannot exceed value 3. If this value is reached, it sets the flag fco (fault counter overflow). If fco is set, the watchdog monoflop is permanently reset, continuously disabling all highside and lowside of the firing switches.

A watchdog reset is implemented which is configured by CONF\_RES. This is only triggered when CONF\_RES = 0, otherwise watchdog reset is deactivated. With each counting to the watchdog failure counter this reset is triggered, resetting the µC and the ASIC. The watchdog fault counter and the WD1-3 flags are not affected by watchdog reset.

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<b>CONF_RES</b>	<b>Description</b>
1	Powerstages will be disabled for one second more than the wrong service is present. After the 3 <sup>rd</sup> change from correct to wrong watchdog service the powerstages will be kept disable for this power on cycle.
0	Reset is caused by a transient from correct serving to wrong serving. With the 3 <sup>rd</sup> transient from correct to wrong serving, the last reset is proceeded , the powerstages will be disabled and kept disabled for this power on cycle. No further Reset can be activated for this power on cycle.

3 different flags for WD1-3 failure flags are implemented. One of them is set which each upward counting of the watchdog fault counter, even when watchdog reset is triggered. If the ASIC and the µC are reset by any watchdog fault, the WD1-3 failure flags indicate which watchdog triggered the reset. The WD1-3 flags are not affected by watchdog reset, but are cleared by WD\_STATUS. The condition after power-on reset is WD\_1-3 flags = "111"

Watchdog fault counter, watchdog reset and setting WD1-3 fault flags are all possible with ECLK missing.

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## 5.1.4 Watchdog SPI Instructions

Trigger watchdog 2:

### SPI instruction WD2\_TRIGGER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	wd2_response															
SPI output data	wd2_checkword															

wd2\_response : response corresponding to the latest checkword for this task  
wd2\_checkword : new checkword for the requesting task

Trigger watchdog 3:

### SPI instruction WD3\_TRIGGER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	wd3_response															
SPI output data	wd3_checkword															

wd3\_response : response corresponding to the latest checkword for this task  
wd3\_checkword : new checkword for the requesting task

Read watchdog status:

### SPI instruction WD\_STATUS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	cr	w3	w2	w1	faultcnt	fco	r3	o3	r2	o2	u2	o1	u1	

u1 : underflow watchdog1 (default 0, please see note)

o1 : overflow watchdog1 (default 1, please see note)

u2 : underflow watchdog2 (default 0)

o2 : overflow watchdog2 (default 1)

r2 : response error watchdog2 (default 0)

o3 : overflow watchdog3 (default 1)

r3 : response error watchdog3 (default 0)

fco : fault counter overflow : 0 = fault\_counter<3, 1 = fault\_counter=3 (default 0)

faultcnt: watchdog fault counter (reset only by power-on reset) (default 00)

w1 : watchdog1 flag (no reset by N\_SYS\_RESET) (default 1)

w2 : watchdog2 flag (no reset by N\_SYS\_RESET) (default 1)

w3 : watchdog3 flag (no reset by N\_SYS\_RESET) (default 1)

cr : level of pin CONF\_RESET

All flags are read and clear except of fco and faultcnt.

Please note: The default values of u1 and o1 are only valid during reset and 40us after the reset.

Truth table for o1/u1:

"00" = ECLK within WD1 tolerance

"01" = ECLK missing or frequency too low

"10" = internal oscillator (or both clocks) missing or ECLK frequency too high

"11" = value only possible at first readout after reset (first readout after reset should be ignored)

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## 5.1.5 Watchdog Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
5.1-1	ECLK	frequency	watchdog functionality only	-1%	4.000	+1%	MHz
5.1-2	internal	frequency	RC clock	-5%	1.875	+5%	MHz
5.1-3	internal	ECLK underflow	watchdog 1 (underflow), jitter sweep off	3.40		3.96	MHz
5.1-4	internal	ECLK overflow	watchdog 1 (overflow), jitter sweep off	4.04		4.60	MHz
5.1-9	internal	ECLK underflow	watchdog 1 (underflow), jitter sweep on	3.20		3.96	MHz
5.1-10	internal	ECLK overflow	watchdog 1 (overflow), jitter sweep on	4.04		4.80	MHz
5.1-5	ECLK	Time	tear-off detection time			80	μs
5.1-6	internal	cycle time	watchdog 2 underflow	244		248	us
5.1-7	internal	cycle time	watchdog 2 overflow	652		656	us
5.1-8	internal	cycle time	watchdog 3 overflow		96	98	ms

### Application Note:

The tolerance of watchdog 1 depends on the jitter sweep being active or not. Please see SPI instruction POM\_CONVERTER in chapter 2.14 starting on page 54 for further details.

First readout of WD\_STATUS after reset might have wd1 over- and underflow. Same applies when restarting ECLK after missing-ECLK-test. In both situations is advised to wait minimum tear-off detection time and ignoring WD\_STATUS having wd1 over- and underflow.

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## 5.2 Monitor SPI

For monitoring the SPI data a second independent SPI is implemented. This monitor SPI can be used to monitor the SPI data read by the SPI master (uC). The monitored data is sent by one of the SPI slaves, e.g. an acceleration sensor, the airbag system ASIC itself, etc.

To enable the monitor SPI the monitor SPI chip select signal N\_CS\_MON has to be set low. Depending on the SPI slave monitored the chip select signal of the airbag system ASIC is activated simultaneously or kept inactive.

The monitored SPI instruction defines the action performed by the monitor SPI:

- Evaluation of sensor data
- Test sensor plausibility path
- Test monitoring functionality

All valid monitor SPI commands are defined in chapter 4.1.9 on page 97. An unknown monitor SPI instruction will be ignored.

The evaluation of sensor data and the test of the plausibility path are described in the plausibility path chapter 5.3, starting on page 155.

### 5.2.1 Monitor SPI Frame Format

The monitor SPI features 3 different frame formats: the standard 32bit frame format and extended frame formats with 16 and 17 bit frames. The selection of the mode is done automatically. The 16 and 17 bit frame format can be enabled/disabled by SPI.

The standard 32bit frame format of the monitor SPI is identical to the 32bit frame format of the normal SPI (please see chapter 4.1.1 on page 91 for details).

The monitor SPI supports extended SPI frames with a length of 16 and 17 bits:

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SI	2 bit instr.	undefined (in parity included)				IP	8 bit input data									
SO	3 check bits	3 bit safety ID				10 bit output data										

	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SI	7 bit instruction						IP	8 bit input data									
SO	8 check bits						8 bit output data										

	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SI	2 bit instr.	undefined (in parity included)				IP	8 bit input data									P <sub>SI</sub>	
SO	3 check bits	3 bit safety ID				10 bit output data											



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## 5.2.2 Monitor SPI Instructions

The monitor SPI features a built-in test to verify the monitoring functionality. Therefore, a device identifier read by the SPI command *READ\_DEV\_ID* will be stored internally if monitored by the monitor SPI. The stored identifier can be read afterwards with the instruction *READ\_MON\_ID*. After reading the monitored identifier the stored identifier will be cleared.

Read monitored identifier:

### SPI instruction *READ\_MON\_ID*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	mon_id							

mon\_id : device id monitored by Monitor SPI (default 0)

The *READ\_MON\_ID* instruction clears the mon\_id register to zero (read and clear). Reading without prior monitoring returns the value zero.

Monitoring the SPI command *DEMAND\_TEST* with at least one bit of thres\_test and pct set results in entering the FLM highside test mode. During this test mode all lowside power stages are disabled by the signal DIS\_ALP. Please see timing control chapter 5.4.3 on page 163 for additional information. The FLM highside test mode is re-triggered with every further *DEMAND\_TEST* instruction and a data byte unequal zero. Additionally, the FLM highside test mode is re-triggered with a TST bit monitored by the monitor SPI but a TST bit monitored will not enter the FLM highside test mode initially (for 16 and 17 bit frames only).

Demand for Test:

### SPI instruction *DEMAND\_TEST*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	pct	thres_test			
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

thres\_test : threshold test mode : 1111 = threshold test for 32 bit frame enabled,

1110 = threshold test for 16 bit frame enabled, others = disabled (default 0000)

pct : PSI consistency test mode : 0 = disabled (default), 1 = enabled

PSI consistency test mode is controlled by SPI instruction *PSI\_TEST\_CONS*

Both test modes can only be activated before EOP2. In case EOP2 is set both test modes are switched off immediately.

During both test modes the SPI status bit TST is set.

Please note, that all low-pass filters are cleared by *DEMAND\_TEST* (before EOP2).

For details on the thres\_test functionality please see chapter 5.3 starting on page 155.

For details on the pct functionality please see the PSI chapter 4.2 starting on page 100.

The functionality of the SPI instruction *READ\_SENSOR* is explained in chapter 5.3 starting on page 155.

## 5.3 Plausibility Path

The aim of the sensor plausibility hardware path is to disable all high-side powerstages as long as there are no significant sensor signals and to enable the powerstages if one or more sensor signals are above the programmed thresholds.

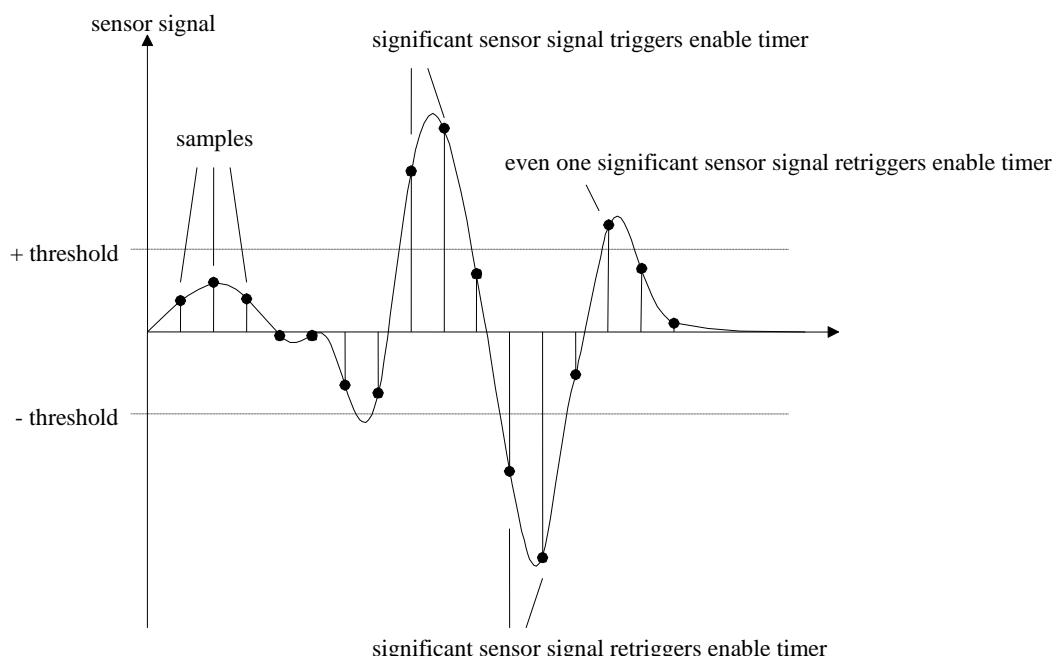
To monitor sensor signals the ASIC has an additional chip select pin N\_CS\_MON which activates the monitoring of the SPI communication during the data submission from the sensors to the microcontroller. The data monitoring is working for the ASIC internal sensor interface (PSI) as well as for external sensors communicating by SPI. The monitor SPI can monitor 16, 17 and 32 bit frames and supports multiple frames in the same system.

The ASIC is able to monitor the data transmission, but the source of data is not visible. Therefore each sensor which should lead to a power stage enable has to send the acceleration signal together with a 5 bit safety identifier (SID). Each SID is related to a safety channel with a programmable threshold.

Furthermore, each safety identifier determines the configuration used by the safety controller. The configuration defines the preprocessing of data in terms of data shift, data zeroing, data rotation and low pass filtering. The direction dependencies are stored within the configuration as well.

Within the airbag system ASIC 16 safety channels are implemented and addressed by the safety identifiers 0 to 15. Data related to the safety identifiers 16 to 31 will be ignored.

If one of the sensor signals is equal or exceeds its threshold the enable monoflop is started:



The enable flipflop releases the DIS\_AHP signal to prepare the ASIC for firing. In case of a direction dependant safety channel, the related SDIS signal is released as well (SDIS\_X, SDIS\_Y, SDIS\_W).

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## 5.3.1 Sensor plausibility path

Within the sensor plausibility path the data coming from the monitor SPI (data in) is evaluated. Sensor data are recognized by the SPI status bit S (sensor data) in 32 bit frames and by the instruction in 16 bit frames. The safety ID within these data is extracted and controls the further processing due to the selection of the safety channel and the related configuration. The configuration of each safety channel is programmed by the SPI instruction PROG\_SAF\_CH. The safety ID has a bit length of 5 bit for 32 bit frames and a length of 3 bit for 16 bit frames. In case of a 16 bit frame the safety ID is completed with two MSB bits (sid\_pre) as programmed by the SPI instruction PROG\_SAFETY.

The bit width for the internal data processing is 10 bit. Therefore, sensor data having a 16 bit width have to be compressed to 10 bit. This compression is done by a 5 bit shift operation and a subsequent clipping to the maximum data range of +511/-512. The bit width of the data is treated as programmed by the configuration of the safety channel (configuration bit shft).

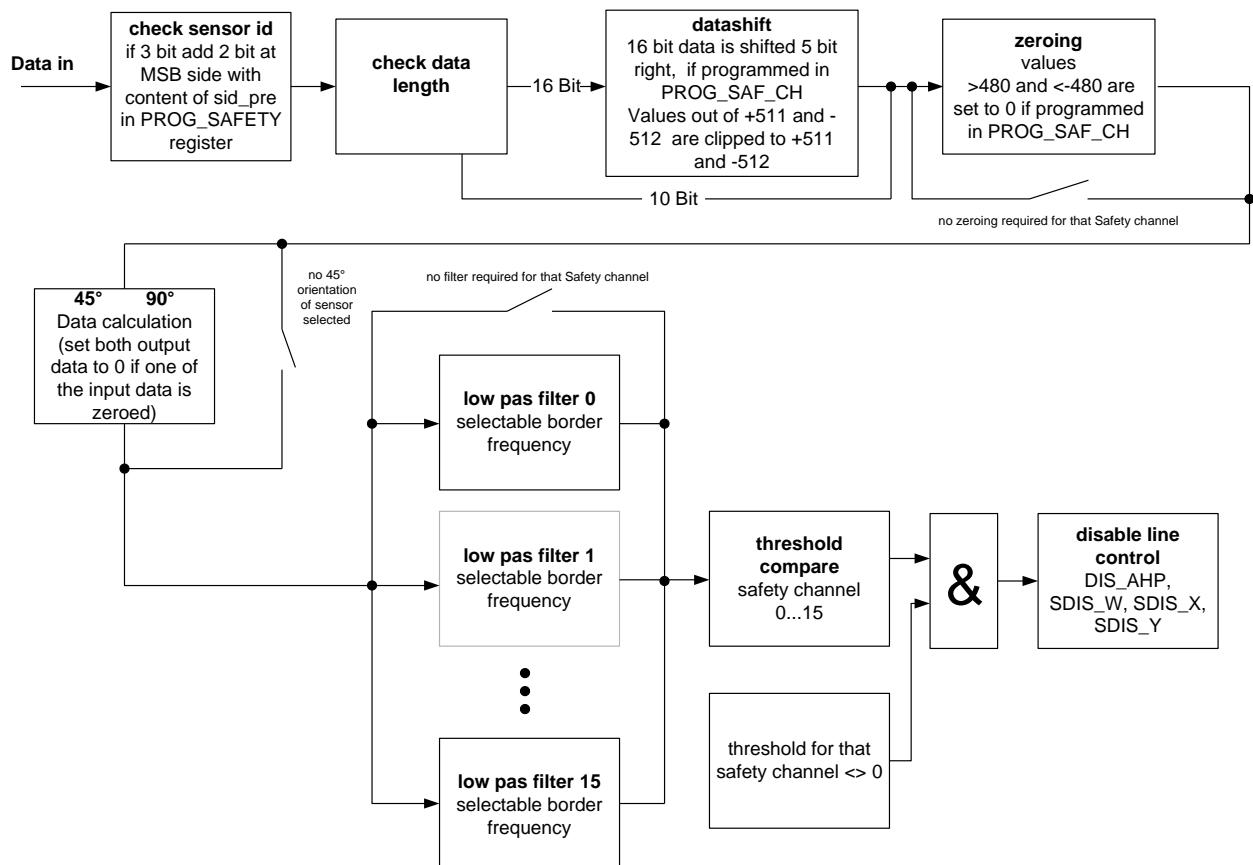
In case sensor data above +480 and below -480 LSB represent status information the ASIC can be programmed to ignore these values and set the value internally to zero (bit zero).

If the central sensor is mounted in 45° orientation, the sensor data can be transformed into data without 45° orientation (please see chapter 5.3.2 for more information).

For the safety channels 0 to 15 a low pass filter can be activated featuring 4 different corner frequencies (please see chapter 5.3.3 for more information).

The evaluated sensor data is compared with the programmed threshold of the safety channel and the disable signals are released in case of exceeding the compare threshold. A threshold with a zero value is treated as invalid.

Evaluation of sensor data block diagram:



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If sensor data should not be evaluated the monitor SPI chip select N\_CS\_MON may not be activated during reading data from this sensor.

Data recognized as invalid are set to zero but evaluated nevertheless (e.g. GS flag is set (32 bit frames), EOP bit is set (16 bit frames) or data range overflow due to zero bit).

## 5.3.2 Processing of 45° sensed data

If the central sensor is mounted in 45° orientation, the threshold monitoring has to calculate the rotation of the acceleration values to enable the DIS\_AHP as well as the related SDIS\_X, SDIS\_Y or SDIS\_W line. This special calculation procedure will be activated by programming the required rotation mode and safety identifiers in the PROG\_XY45 register.

Depending on the mounting orientations following equation is valid:

+45° mode (both acceleration directions in y-direction):

```
value1 = sensor element in 45° orientation  
value2 = sensor element in 135° orientation  
x result = value1 - value2  
y result = value1 + value2
```

-45° mode (both acceleration directions in x-direction):

```
value1 = sensor element in 315° orientation  
value2 = sensor element in 45° orientation  
x result = value1 + value2  
y result = value1 - value2
```

The rotation is calculated after the reception of value2 after value1. Value 1 is stored until value2 is received. If one of the monitored values is set to 0 (e.g. due to a range overflow), both results of the calculation are set to zero. In case of a range overflow the results are clipped to the maximum value (+511/-512). The x result is linked to the safety ID of value1 and the y result is linked to the safety ID of value2.

### Application Note:

Using the 45° mode the x and y data are not vectorized but added/subtracted only. The x and y data used internally for threshold compare are enlarged by the square root of 2. Therefore, the thresholds programmed for x and y channel should be calculated accordingly (sized by the same constant).

## 5.3.3 Low pass filter

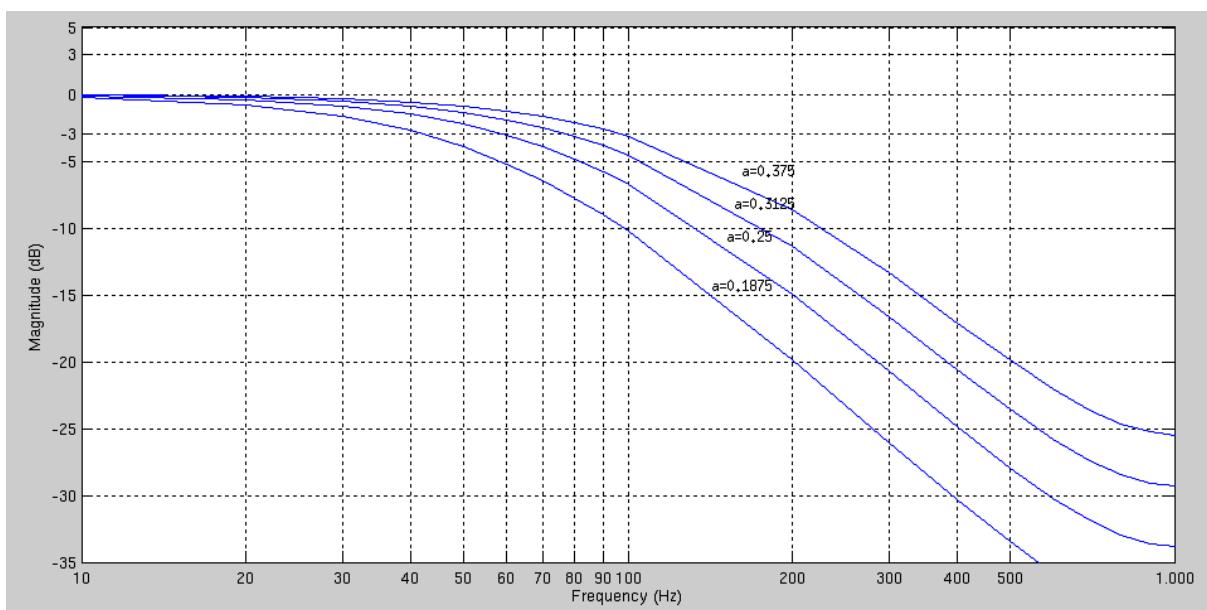
To filter the sensor data a low pass filter with 16 channels is implemented. This filter can be activated or bypassed individually for each safety channel to meet the required data evaluation. The filter is implemented for the safety channels 0 to 15 only.

The filter is a recursive system of order 2, which uses only one coefficient. Its transfer function is given by

$$H(z) = \frac{(za)^2}{(z - (1 - a))^2}$$

The filter can be configured with 4 different corner frequencies:

- 43 Hz (a=0,1875)
- 60 Hz (a=0,25)
- 78 Hz (a=0,3125)
- 98 Hz (a=0,375)



The corner frequencies depend on the data sample rate by monitoring sensor data. The corner frequencies shown here are based on a data sample rate of 500us.

The filter will be cleared by the SPI instruction DEMAND\_TEST (before EOP2), the SPI instruction END\_ENABLE (cf=1) and when the testmode monoflop time ends.

#### 5.3.4 SPI Frames with 16 Bit

For the compatibility to former airbag generations the monitor SPI supports SPI frames with a 16 bit width as well. Data read out of 16 bit frames do not feature a sensor data flag (S) neither a global status flag (GS). Therefore the recognition of sensor data is done due to the monitored instruction within the same frame. Furthermore, the status bits EOP and TST are evaluated. Sensor data are only evaluated if the TST status bit is zero 0. In case the TST status bit is set the sensor data is evaluated only if the testmode monoflop is already running. Sensor data with an invalid safety ID (111) will not be evaluated. If the EOP bit is set the sensor is out of the required function and the data is set to zero but evaluated nevertheless.

The data bit width for data out of 16 bit frames is always 10 bit. Therefore the configuration bit shft must not be set.

#### 5.3.5 Threshold Test Mode

To support the built-in sensor test a dedicated threshold test mode has been implemented. Within this threshold test mode a 16 bit data value and a 5 bit safety ID can be programmed by using the SPI instructions *THRES\_TEST\_DATA* and *THRES\_TEST\_SID*. The registers *THRES\_TEST\_DATA* and *THRESH\_TEST\_SID* may be cleared by changing the testmode from 32 bit to 16 bit and vice versa. Therefore the intended programming has to be done after changing the testmode. The threshold test mode has to be activated by the SPI instruction *DEMAND\_TEST* and can only be used before sending EOP2. The programmed data and SID can be read via the PSI interface using the SPI instruction *PSI\_READ\_DATA31* (channel=7, slot=3). By monitoring this data via the monitor SPI the sensor test can be performed testing threshold comparison and DIS\_AHP timing control.

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During the threshold test mode being active the SPI status bit TST is set and the status bit EOP is masked to zero. The SPI status bits S (sensor data) and GS (global status) can be controlled by the SPI instruction *THRES\_TEST\_SID*.

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## 5.3.6 Plausibility Path SPI Instructions

Program safety channels:

### **SPI instruction PROG\_SAF\_CH1...16**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	shft	zro	dx	dy	dw	fon	f_coeff	saf_thres								
SPI output data	shft	zro	dx	dy	dw	fon	f_coeff	saf_thres								

saf\_thres : safety threshold

f\_coeff : select filter coefficients / corner frequencies

00 = 43 Hz, 01 = 60 Hz, 10 = 78 Hz, 11 = 98 Hz

fon = 1 : filter on

dx = 1 : SDIS\_X influence on

dy = 1 : SDIS\_Y influence on

dw = 1 : SDIS\_W influence on

zro = 1: zeroing (set data to zero if data > +480 / < -480)

shft = 1: shift 16 down to 10 bits on (shift 5 bits + clipping to +511/-512)

The safety channel address is coded within the least 4 bits of the instruction.

The default value of this register is zero.

Program x/y data SID in 45° applications:

### **SPI instruction PROG\_XY45**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	mode	sid_y45						sid_x45				
SPI output data	0	0	0	0	mode	sid_y45						sid_x45				

sid\_x45 : SID of x data rotated by 45° (default 11111)

sid\_y45 : SID of y data rotated by 45° (default 11111)

mode : rotation mode

00 : sensor data expected in 90° orientation (default 00)

01 : sensor data rotated by +45° (x = value1 – value2, y = value1 + value2)

10 : sensor data rotated by -45° (x = value1 + value2, y = value1 – value2)

11 : undefined

Please note the number of safety channels is smaller than the SID range.

Program long enable time:

### **SPI instruction PROG\_PLP\_LONG**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	sid_long		en_time_long										
SPI output data	0	0	0	sid_long		en_time_long										

en\_time\_long : 0 = long enable time off (default), 1...255 = long enable time (32.768ms per bit)

sid\_long : safety ID related to long enable time (default 11111)

Before EOP2, en\_time\_long <= 10 are valid only.



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Set threshold test data:

## **SPI instruction THRES\_TEST\_DATA**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	test_data															
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

test\_data : 16 bit value used during threshold test mode (default 0)

This register can only be set during threshold test mode being active. In case the threshold test mode is switched off the test data register is cleared immediately. In 16 bit SPI frame threshold test mode the least 10 bits are used only. To use this instruction, the pe bit must be set.

Set threshold test SID:

## **SPI instruction THRES\_TEST\_SID**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	sd	gs	test_sid				
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

test\_sid : 5 bit safety ID used during threshold test mode (default 11111)

gs :

0 : sets the SPI status bit GS during threshold test mode for PSI channel 31, but does not override the influence of other events on setting the status bit GS (default)

1 : sets the status bit GS to 1

sd : 1 = SPI status bit S is set to zero (default 0: S bit normal function)

This register can only be set during threshold test mode being active. In case the threshold test mode is switched off the test SID register is cleared immediately. In 16 bit SPI frame threshold test mode the least 3 bits are used only. To use this instruction, the pe bit must be set.

Read last PLP threshold evaluated:

## **SPI instruction TEST\_PLP\_THRES**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	plp_threshold							

plp\_threshold : last threshold evaluated in plausibility path (monitoring of READ\_SENSOR)

Between READ\_SENSOR and TEST\_PLP\_THRES a minimum delay of 2 µs is needed. In 45° mode the evaluation is done after receiving the second value and only y-direction threshold can be read (because both values are evaluated directly after each other, starting with x).

Read last PLP data evaluated:

## **SPI instruction TEST\_PLP\_DATA**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	plp_data							

plp\_data : last data evaluated in plausibility path (monitoring of READ\_SENSOR)

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Between READ\_SENSOR and TEST\_PLP\_THRES a minimum delay of 2 µs is needed. In 45° mode the evaluation is done after receiving the second value and only y-direction data can be read (because both values are evaluated directly after each other, starting with x).

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## 5.4 Timing Control

The Monoflops control the timing of the disable lines DIS\_ALP, DIS\_AHP and SDIS\_X/Y/W. These pins can be forced from the outside, which will override the function of this block. The Monoflops are triggered by events and enables/disables the output for a defined time. During this time µC can react according to his observations.

- DIS\_ALP is influenced by watchdog monoflop and testmode monoflop.
- DIS\_AHP is influenced by watchdog monoflop, enable monoflop and disposal function.
- SDIS\_X/Y/W is influenced by enable monoflop, eop1 and disposal function

### 5.4.1 Behavior of Monoflops

There are 3 internal Monoflops. All of them are counters with different starting and stop values. If an event happens on the input, the counters are set to their starting value and begin counting until he reaches his stop value (monoflop = active). During active monoflop the referring Disable Lines might change their state until the counter stops, changing the Disable Line's state to the original one. If an event happens while monoflop is still counting, the counter is also set to starting value and starts again. During the whole time the Disable Line's state will stay changed, from first start till the end of counting.

The default value of the Disable lines is high during system reset (N\_SYS\_RESET) and power-on-reset (N\_POR).

### 5.4.2 Watchdog monoflop

The Watchdog monoflop is affecting DIS\_ALP and DIS\_AHP. It is triggered by system reset (N\_SYS\_RESET), power-on-reset (N\_POR), watchdog reset (WD\_FLT\_R) and watchdog fault (WDFAULT). If any of these triggers happen, the monoflop is started and DIS\_ALP and DIS\_AHP are both disabled asynchronous. This works even with missing ECLK.

The purpose of watchdog monoflop is to ensure save state if system safety is jeopardized. The indicator for a working µC and system is watchdog function. The monoflop guarantees that a failure-free system state exists for a certain time until DIS\_ALP and DIS\_AHP can be enabled.

The nominal time for watchdog monoflop is 1 second, but it can be programmed to 360ms by SPI command PROG\_SAFETY. For tolerances see timing table.

The watchdog monoflop is influencing watchdog fault counter, WD1-3 flags and watchdog reset. While the monoflop is active, watchdog reset is blocked, the watchdog fault counter cannot count up and the WD1-3 flags cannot be set. This prevents any unwanted effects during system ramp-up or system diagnosis. If watchdog fault counter is equal to 3 the watchdog monoflop is permanently triggered, continuously disabling all highside and lowside of the firing switches.

### 5.4.3 Testmode monoflop (disable monoflop)

The testmode monoflop is affecting DIS\_ALP only. It is used to disable the lowside power switches during test of the highside switches.

The testmode monoflop is triggered by SPI DEMAND\_TEST. This sets the system into testmode and the lowside switches are deactivated. Afterwards additionally SPI commands can retrigger the monoflop until it reaches the stop value. Following events cause a retrigger:

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- 32 Bit SPI DEMAND\_TEST on SPI with data/=0 before EOP2
- 16/32 Bit SPI DEMAND\_TEST on monitor SPI with data/=0
- testmode monoflop running and 16 Bit SPI on monitor SPI with flag TST = '1'
- testmode monoflop running, threshold test is running (SPI DEMAND\_TEST) and 32 Bit SPI READ\_SENSOR\_DATA on monitor SPI with sensor data flag S = '1'

The remaining time of testmode monoflop can be reduced by SPI END\_ENABLE. The counter value is set to a new value which is equal to approx. 4ms remaining time. If the actual remaining time is shorter than the 4ms, the influence of END\_ENABLE on testmode monoflop is ignored. The influence of END\_ENABLE can be switched on/off by the bit "tt". If the counter finally reaches its stop value, DIS\_ALP will return to its original value and the testmode ends. When this happens the history of PLP filter (located in plausibility path) is cleared to ensure that no sensor data sent during testmode can affect the normal function.

The testmode monoflop is also used for disposal mode. The disposal sequence can only be activated if the testmode monoflop is running.

The nominal time for testmode monoflop is 344ms. The nominal timing of END\_ENABLE is 4 ms. For tolerances see timing table.

## 5.4.4 Enable monoflop

The enable monoflop is influencing DIS\_AHP and SDIS\_X/Y/W. DIS\_AHP is generally enabling the highside of firing stages, the others can be programmed to enable certain ones. This can be used to minimize the enabled firing stages to the ones necessary.

The plausibility path is observing monitor SPI for crash relevant sensor data. The SID send together with the data can be programmed to influence no, one or two of the three axis. Additionally one SID can be assigned to a programmed enable time as multiples of 32.768ms. When sensor data is observed with this SID the enable time is set to the programmed one. The long enable time can be programmed from 1-225 (32.768ms - 8.356 seconds). Before EOP2 the value is clipped to maximum value 10 (327.68ms) to ensure that enable time never exceeds test disabling time of testmode monoflop.

The PLP block evaluates this information and generates 5 signals:

- ovfl\_any: crash relevant data detected, influence generally for all firing stages
- ovfl\_x: crash relevant data detected, influence related to SDIS\_X-Disable register
- ovfl\_y: crash relevant data detected, influence related to SDIS\_Y-Disable register
- ovfl\_w: crash relevant data detected, influence related to SDIS\_W-Disable register
- ovfl\_long: crash relevant data detected, SID = SID\_long

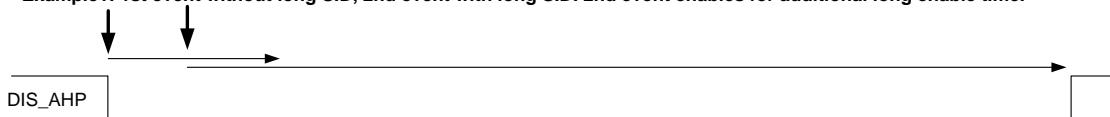
Event at ovfl\_any is generated when crash relevant data are observed. Additionally ovfl\_x/y/w might come, but not necessarily. Ovfl\_any will trigger the enable monoflop which will enable DIS\_AHP. If there is an additional event on ovfl\_x/y/w, the referring SDIS\_X/Y/W line is enabled also until the counter reaches his stop value. If a second event occurs while the enable monoflop is still running, the monoflop is retriggered, additionally enabling the related SDIS\_X/Y/W line. While the monoflop is active, DIS\_AHP and the related SDIS\_X/Y/W lines will be enabled until the end of the enabling time.

The retrigger of the enable monoflop is different from the other monoflops. Because there are two different enable times (one programmed for SID\_long and a fixed one for all others) the counter is implemented as count-down. Any retrigger will check if the actual counting value is smaller than the one to be set. If so, the counter is set to the larger value, otherwise the counter value stays the same. This will cause the remaining time to only stay or increase, but never to decrease.

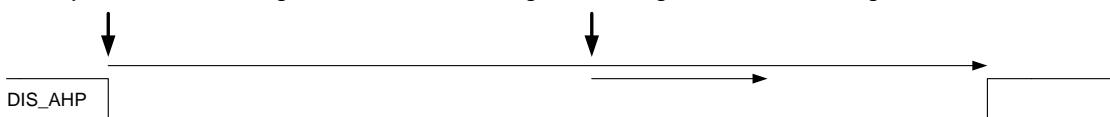
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Example1: 1st event without long SID, 2nd event with long SID. 2nd event enables for additional long enable time.



Example2: 1st event with long SID, 2nd event without long SID. Remaining time of 1st event is larger than the one of 2nd event.



Example3: 1st event with long SID, 2nd event without long SID. Remaining time of 1st event is smaller than the one of 2nd event.



The enable monoflop can be stopped by SPI END\_ENABLE. The counting will stop at once and the disable lines will return to their original value.

## Application note:

The enable time can never be decreased by additional retriggers, but it can be increased. The longer time always wins.

The retrigger affects all actually enabled disable lines plus the ones enabled by the actual retrigger. So a previously enabled SDIS\_X/Y/W for short enable time will also be affected by any event with long enable time.

Before EOP2 the long enable time is limited to maximal the time of nominal enable time to prevent DIS\_ALP and DIS\_AHP being enabled together during initial test. A larger time cannot be initially tested. To check special timing for long SID a programming should be used with shorter time (value 1-9), otherwise this SID behaves as any other SID. The value can be reprogrammed before EOP2.

### 5.4.5 Timing Control SPI Instructions

End enable time:

#### SPI instruction END\_ENABLE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	tt	cf
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

End enable time immediately (clear enable timer) in case of sensor testmode.

cf : 0 = clear all low-pass filters of all safety channels

tt : 0 = test timer reduced, 1 = test timer not affected

Please note, that the reduction of the enable times is only possible during sensor test mode.

Please note, that clearing all low-pass filters is not locked by EOP2.

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## 5.4.6 Timing Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
5.4-1	DIS_AHP, DIS_ALP	delay time	watchdog fault disable time	998		1000	ms
5.4-2	DIS_AHP, DIS_ALP	delay time	watchdog fault disable time, quick mode	359		361	ms
5.4-3	DIS_AHP, SDIS_X/Y/W	delay time	enable time	326		328	ms
5.4-4	DIS_AHP, SDIS_X/Y/W	delay time	enable time, long_SID, x = programmed time value	32.768 ms * x - 2.1 ms		32.768 ms * x + 1.1 ms	ms
5.4-5	DIS_ALP	delay time	test disable time	342.5		344.5	ms
5.4-6	DIS_AHP	delay time	end enable delay			1	us
5.4-7	DIS_ALP	delay time	end enable delay	3.0		4.2	ms

Remark:

The above mentioned timing definitions are for digital logic only (SPI DISABLE\_STATUS). The analog outputs will have additional delay of about 20µs, depending on the load of the pins.

## 5.5 Switch Evaluation

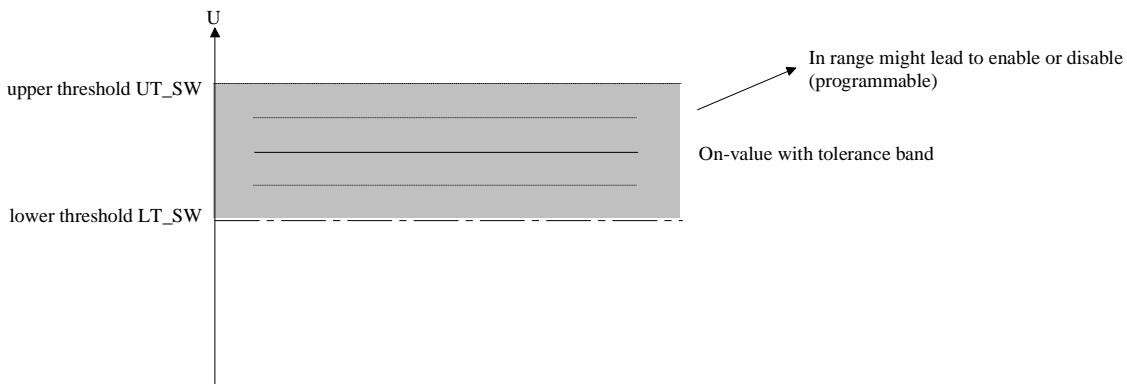
The special disable line of hardware switch (SDIS\_S) is generated by evaluating an AINO measurement. This might be used to disable certain firing loops depending on external components on AIN or AIO. Such might be a deactivation switch for passenger air bag.

Only one AIN or AIO channel is able to influence the switch evaluation. This channel is programmed with PROG\_SW\_MODE. Whenever a valid AINO measurement of this channel is read (READ\_AINO\_AUTO1-12 or ADC\_READ\_AINO) with sds-Bit = 1, the ADC result is compared to programmed limits. Because the valid bit is cleared by reading, the same ADC result cannot influence switch evaluation twice.

If sds-Bit = 0 or the measured AINO channel is not the programmed one, the SPI commands will be ignored.

The two limits can be programmed with SPI PROG\_SW\_UP\_THRES (upper tolerance UT\_SW) and PROG\_SW\_LOW\_THRES (lower tolerance LT\_SW). These limits define a tolerance band. The tolerance limits themselves belong within the band.

The band can be programmed to have enabling or disabling influence. If enable is programmed, then each ADC value within the band has enabling influence, values outside band has disabling influence. If disable is programmed it works in opposite way.



The filter is symmetric and the number of ADC results leading to disable or enable of SDIS\_S can be programmed. Each time the value changes from in-band to out-band (or the other direction), the internal counter is reset. Each new value with the same in-band or out-band evaluation will increase the counter by one. When the counter equals the programmed number and the next evaluation is the same in-band or out-band, SDIS\_S is changed accordingly.

When numbers of counts necessary is set to 0, each result will change SDIS\_S directly. The maximum is 7, meaning that 8 concurrent measurement with the same in-band or out-band behavior are necessary to change SDIS\_S.

During Reset the disable signal SDIS\_S is disabled (high), before EOP1 is sent SDIS\_S is enabled (low).

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## 5.5.1 Switch Evaluation SPI Instructions

Program switch evaluation mode:

### **SPI instruction PROG\_SW\_MODE**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	sdis_channel		count		en			
SPI output data	0	0	0	0	0	0	0	0	sdis_channel		count		en			

en : 0 = switch evaluation using enable band (default), 1 = switch evaluation using disable band

count : switch evaluation sampling count 0...7 (0=immediately, default 0)

sdis\_channel : defines channel (AIN1..10 / AIO1..2) influence to SDIS\_S (15=no channel, default 15)

Program switch evaluation upper threshold:

### **SPI instruction PROG\_SW\_UP\_THRES**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	sw_up_thres							
SPI output data	0	0	0	0	0	0	0	0	sw_up_thres							

sw\_up\_thres : switch evaluation upper threshold (default 0)

Program switch evaluation lower threshold:

### **SPI instruction PROG\_SW\_LOW\_THRES**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	sw_low_thres							
SPI output data	0	0	0	0	0	0	0	0	sw_low_thres							

sw\_low\_thres : switch evaluation lower threshold (default 0)



## 5.6 Disable Lines

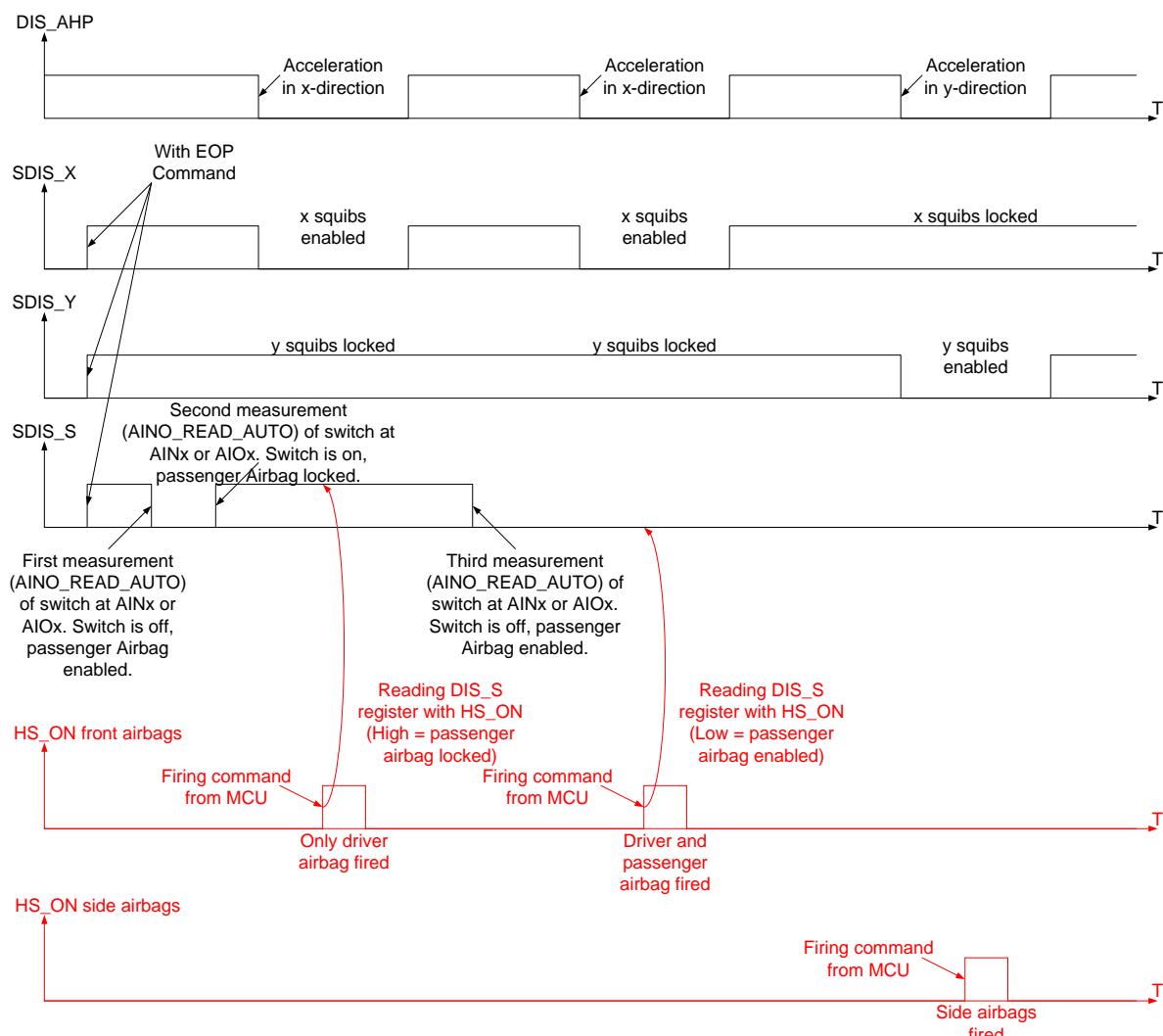
There are 7 disable lines.

- DIS\_SHP (disable dedicated highside power stages, see chapter of firing loops)
- DIS\_AHP (disable all highside power stages)
- DIS\_ALP (disable all lowside power stages)
- SDIS\_X (special disable x-channel)
- SDIS\_Y (special disable y-channel)
- SDIS\_W (special disable w-channel)
- SDIS\_S (special disable switch evaluation)

During Reset the disable signal DIS\_AHP, DIS\_ALP and SDIS\_X/Y/W/S are disabled (high), before EOP1 is sent SDIS\_X/Y/W/S are enabled (low).

SDIS\_S is not generated in timing control, but in switch evaluation. DIS\_SHP is input pin.

Example timing diagram:



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Please note: the watchdog has only influence on DIS\_AHP and DIS\_ALP as these signals are the master signals. The watchdog has no influence on SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S.

The actual status of the disable lines can be read using SPI command DISABLE\_STATUS:

Read disable line status:

## SPI instruction DISABLE\_STATUS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI output data	0	0	0	0	0	0	0	0	0	d6	d5	d4	d3	d2	d1	d0

dx : 0 = corresponding powerstages are not disabled, 1 = active disabled

d6 : DIS\_ALP

d5 : DIS\_AHP

d4 : DIS\_SHP

d3 : SDIS\_X

d2 : SDIS\_Y

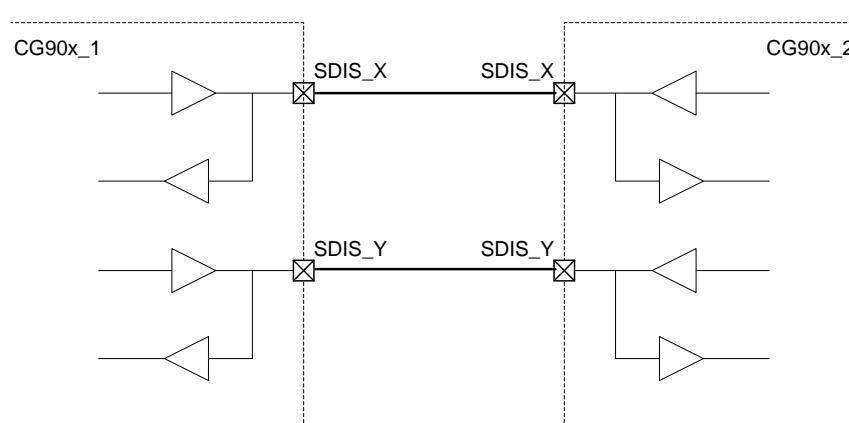
d1 : SDIS\_W

d0 : SDIS\_S

The dx bits follow the function status immediately. The bits will be cleared by reading and set with the next clock cycle. The dx bits represent the physical level of the related pin because the line level can be influenced by outside effects.

### 5.6.1 Multiple ASIC Configuration

All DIS and SDIS pins (except for DIS\_SHP) are designed to support systems with multiple ASIC configurations using more than one airbag system ASIC in the same ECU. Therefore, these pins can be connected together directly:



To avoid any short circuit conditions, these pins use a pull-up current providing a recessive high level and a lowside switch providing a dominant low level. By default, these pins have high level disabling the corresponding firing loops. During the release state, the level is forced to low by the ASIC working as output driver.

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## 5.6.2 Disable Lines Electrical Characteristics

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>parameter</i></b>	<b><i>condition / description</i></b>	<b><i>min</i></b>	<b><i>typ</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
5.6-1	DIS_AHP, DIS_ALP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	pull-up current	only active during high level additional to pull-up resistor	50	75	100	uA
5.6-2	DIS_AHP, DIS_ALP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	pull-up resistor	additional to pull-up current	20	44	66	kΩ
5.6-3	DIS_SHP	pull-up current		75	120	200	uA
5.6-4	DIS_AHP, DIS_ALP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	output voltage	low level, I = 600uA			0.2 * VIO	V
5.6-5	DIS_AHP, DIS_ALP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	output voltage	high level	0.8 * VIO			V
5.6-6	DIS_AHP, DIS_ALP, DIS_SHP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	threshold	input low voltage			0.3 * VIO	V
5.6-7	DIS_AHP, DIS_ALP, DIS_SHP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	threshold	input high voltage	0.7 * VIO			V
5.6-8	DIS_AHP, DIS_ALP, DIS_SHP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	hysteresis	input voltage	0.5		1.5	V

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## 5.7 Safety Controller Configuration

The Safety Controller within the airbag system ASIC can be configured individually. Additionally, the PWM frequency of the AIO and LIN module can be selected:

- SID prefix for 16 bit frames
- monitor SPI mode
- SO pull-up deactivation
- N\_CS\_MON behavior
- Watchdog Disable Time
- Disposal mode selection
- PWM frequency for AIO/LIN

Program safety controller:

### **SPI instruction PROG\_SAFETY**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	-	-	-	-	-	pwmfreq	dm	wd	sl	pu	mon_spi	sid_pre				
SPI output data	0	0	0	0	0	pwmfreq	dm	wd	sl	pu	mon_spi	sid_pre				

sid\_pre : SID prefix for 16/17 bit frames with 3 bit SID (default 11)

mon\_spi : monitor SPI mode : 00 = 16/17 off, 01 = 16 on, 10 = 17 on, 11 = 16/17 on (default 00)

pu : 1 = disable pull-up of SO pin, 0 = pull-up of SO pin active (default)

sl : slave mode : 0 = master mode (safety controller active, default)

1 = slave mode (N\_CS\_MON used as SDIS\_X input)

wd : watchdog disable time : 0 = 1000 ms (default), 1 = 360 ms

dm : disposal mode :

00/11 = no disposal mode active (default 00)

01 = ACL (PWM) mode enabled

10 = disposal mode 3/4 enabled

pwmfreq: 00 = 100 Hz (default), 01 = 200 Hz, 10 = 266 Hz, 11 = 400 Hz

SID prefix for 16 bit frames:

In case of monitoring a 16/17 bit frame the monitored SID has a width of 3 bits. These three bits are completed with 2 prefix bits defined by sid\_pre generating a 5 bit SID used by the safety controller. For a detailed description please see chapter 5.3 starting on page 155.

Monitor SPI mode:

The detection of 16 and 17 bit frames within the monitor SPI can be enabled and disabled independent of the 32 bit frame format which is always enabled. For a detailed description please see chapter 5.2.1 on page 153.

SO pull-up deactivation:

The pull-up current of the SO pin can be deactivated to reduce the load on the SPI bus in multiple ASIC configurations to achieve the maximum transmission speed.

N\_CS\_MON behavior:

Normally, the pin N\_CS\_MON is the chip select pin of the monitor SPI. However, the monitor SPI and the safety controller can be deactivated and the N\_CS\_MON pin can be used as a SDIS\_X input. This can be helpful in multiple ASIC configurations with system ASICs which do not have a dedicated SDIS\_X pin.

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## Watchdog Disable Time:

The watchdog disable time can be selected out of 2 different values. For a detailed description please see chapter 5.4.2 on page 163.

## Disposal mode selection:

For a description of the disposal functionality please see chapter 5.8 starting on page 174.

## PWM frequency for AIO/LIN:

The PWM frequency of the AIO and LIN module can be selected out of 4 different values. For a detailed description please see chapter 4.6 starting on page 123 for AIO and chapter 4.4 starting on page 115 for LIN.

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## 5.8 Disposal Control

The airbag system IC features the possibility for end-of-life squib firing to prevent any damage or misuse of explosive materials. This squib firing typically takes place at a scrap yard by authorized personal. To be able of squib firing without any crash relevant sensor data the safety controller has to be bypassed in a secure way, any accidentally bypassing of the safety controller has to be impossible. This squib firing is called disposal function further on in this document.

Three possibilities according to the different regional laws are available:

- Disposal function based on SPI sequence
- Disposal function based on PWM signal
- Disposal function based on pin overdrive

The digital control of the disposal functionality is given by the SPI instruction *DISPOSAL*. The disposal function based on pin overdrive does not need any digital control. The detailed function is selected by one of five valid data words DISP1 to DISP5:

Control disposal function:

### **SPI instruction DISPOSAL**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input data	disposal_code															
SPI output data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Valid disposal codes disposal\_code:

DISP1 0505hex = 0000 0101 0000 0101bin  
DISP2 0A0Ahex = 0000 1010 0000 1010bin  
DISP3 5050hex = 0101 0000 0101 0000bin  
DISP4 A0A0hex = 1010 0000 1010 0000bin  
DISP5 AAAAhex = 1010 1010 1010 1010bin

The status of the safety relevant signals can be read by SPI instruction *DISABLE\_STATUS* (see chapter 5.6 starting on page 169). The status of the disposal function can be monitored by the SPI status bits DIS1 and DIS2 (see chapter 4.1.4 on page 93).

Please note: The highest priority on the disable signals is still by the watchdog. A watchdog failure interrupts an active disposal state.

### 5.8.1 Disposal function based on SPI sequence

To enable the firing loops the disable signals DIS\_AHP, DIS\_ALP, SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S have to set to low level. The general lowside disable signal DIS\_ALP is not under the control of the disposal function. This signal is controlled by the watchdog and set to low internally if the watchdog is served correctly. The signals DIS\_AHP, SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S can be set under the control of the disposal function and will be set to low level by performing the following SPI sequence:

*DEMAND\_TEST* (triggers the testmode monoflop)  
*DISPOSAL DISP1*  
*DISPOSAL DISP2*  
*DISPOSAL DISP3*  
*DISPOSAL DISP4*

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To enter the disposal sequence (with DISP1) the watchdog monoflop has to be inactive, the testmode monoflop has to be active and the watchdog fault counter has to be zero. The same conditions occur for any other disposal instruction. Between the *DISPOSAL* commands DISP1/DISP2 and DISP3/DISP4 no further SPI commands are allowed. Otherwise the disposal sequence will be reset. SPI commands between DISP2/DISP3 stops the disposal sequence. After successful sending SPI instruction *DISPOSAL* DISP2 the SPI status flag DIS1 is set and the special disable signals SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S are deactivated (set to low level). After successful sending SPI instruction *DISPOSAL* DISP4 the SPI status flag DIS2 is set additionally and the general highside disable signal is DIS\_AHP is deactivated (set to low level).

<b><i>DIS2 flag</i></b>	<b><i>DIS1 flag</i></b>	<b><i>description</i></b>
0	0	normal operation (no disposal function active, ADC not under control of disposal function)
0	1	1 <sup>st</sup> disposal state active, all special disable signals set to low
1	1	2 <sup>nd</sup> disposal state active, DIS_AHP and all special disable signals set to low

The disposal sequence can be left by sending any additional *DISPOSAL* command.

Due to the safety relevance for releasing the DIS\_AHP signal, the disposal commands DISP3 and DISP4 are disabled by default and have to be activated by the SPI instruction *PROG\_SAFETY*. Please see chapter 5.7 on page 172 for further details.

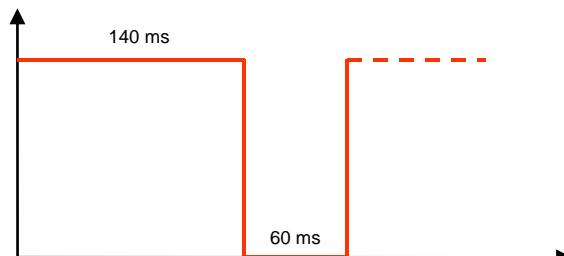
## 5.8.2 Disposal function based on PWM signal

It is possible to control the disposal function by a PWM signal at pin AIO1. Therefore, the ADC channel AINO is used. The enabling sequence needed is similar to the disposal function based on SPI sequence:

*DEMAND\_TEST* (triggers the testmode monoflop)  
*DISPOSAL* DISP1  
*DISPOSAL* DISP2  
*DISPOSAL* DISP5 (sets AIO1 and the ADC channel AINO into disposal mode)

After sending the SPI command *DISPOSAL* DISP5 the SPI status bit BSY2 is set (see chapter 4.1.4 on page 93) indicating that the ADC channel AINO is busy and cannot be accessed by any AIN/AIO SPI commands.

The required frequency of the PWM signal is 5 Hz with a duty cycle of 7 : 3 (high to low level). The voltage of the PWM signal should be 0V...3.0V at low level and 4.5V...36V at high level. The slew rate of the PWM signal should be 3V/ms or higher.



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After the system ASIC have received the DISP5 command in the correct manner, the PWM evaluation is started. The sampling of the PWM signal is fully automatic and controlled internally with a frequency of 500Hz. After successively recognition five PWM periods within the correct ranges the high side power stages will be enabled and the SPI status flag DIS2 is set.

The ADC values are evaluated in the following way: values same or below 128 LSB will lead to increment the low level counter, values above 190 LSB will lead to increment the high level counter. The first measured value in between the thresholds will be ignored, a further value will result in clearing the counters and the evaluation will start again. A PWM signal with a high level time duration between 126 ms and 154 ms and a low level time duration between 54 ms and 66 ms has to be judged as a correct signal.

To monitor the correct function of the PWM signal after the power stages are enabled a hardware failure counter is implemented which stops the disposal sequence and disables the power stages immediately if the value 75 is reached. Each failure of the PWM signal after the Power stages are enabled will increase the counter for 5, each correct PWM sequence will decrease the counter by one. If a running disposal sequence was interrupted by the failure counter it is not possible to continue the sequence. The disposal sequence has to be started with the correct procedure.

Due to the safety relevance for releasing the DIS\_AHP signal, the disposal command DISP5 is disabled by default and have to be activated by the SPI instruction PROG\_SAFETY. Please see chapter 5.7 on page 172 for further details.

### 5.8.3 Disposal function based on pin overdrive

The pins DIS\_AHP, DIS\_ALP, SDIS\_X, SDIS\_Y, SDIS\_W and SDIS\_S are designed as bidirectional input/output pins. Therefore, the disable high level can be forced externally to low without any damage of the ASIC. Contrarily, the enable low level must not be forced externally to high because it will damage the ASIC.

The disable special highside signal DIS\_SHP is an input signal and can be set externally if needed.



## 6. Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 6.1 Junction Temperature

The operating junction temperature range is -40°C to +150°C. The maximum junction temperature must not be exceeded except during firing within the firing power-stages.

### 6.2 Absolute Maximum Ratings

All external pins of the ECU are designed as high voltage pins. They are resistant against voltages up to 36V. The internal pins depend on the certain functionality.

All ground pins have to be tied to ground. The minimum voltage of all pins is -0.3V except of the pin DIA which is specified down to -12V.

<b><i>id</i></b>	<b><i>pin</i></b>	<b><i>module</i></b>	<b><i>parameter</i></b>	<b><i>min</i></b>	<b><i>max</i></b>	<b><i>unit</i></b>
6.2-1	VZP, VBAT_MONx, N_SLEEP, L1H, VUP, VUP_VAS, VER, L2H, VAS, VAS_VC, L3H, CONFx	POM	max voltage	-0.3	+36	V
6.2-2	VINT_S, VINT_A, VST50	POM	max voltage	-0.3	+5.5	V
6.2-3	VST33, VIO, VCOREx	POM	max voltage	-0.3	+3.6	V
6.2-4	VINT_D	POM	max voltage	-0.3	+2.0	V
6.2-5	N_POR, N_RST_MON	POM	max voltage	-0.3	+3.6	V
6.2-6	DIA	IM: LIN	max voltage	-12	+36	V
6.2-7	TXD, RXD	IM: LIN	max voltage	-0.3	+3.6	V
6.2-8	ECLK, N_SYS_RES	IM: SYS	max voltage	-0.3	+3.6	V
6.2-9	DIS_AHP, DIS_ALP, DIS_SHP, SDIS_X, SDIS_Y, SDIS_W, SDIS_S	IM: SAM	max voltage	-0.3	+3.6	V
6.2-10	PSI_SYNC	IM: PSI	max voltage	-0.3	+3.6	V
6.2-11	N_CS, N_CS_MON, SCK, SI, SO	IM: SPI	max voltage	-0.3	+3.6	V
6.2-12	TESTM	TEST	max voltage	-0.3	+10	V
6.2-13	IGHx, IGLx, VHx, SVR_DIAG, SQREF	FLM	max voltage	-0.3	+36	V
6.2-14	IGHx, IGLx	FLM	neg. current		-1	A
6.2-15	AINx, PSIx, AIOx, VSYNC	IM	max voltage	-0.3	+36	V
6.2-16	AINx, PSIx, AIOx	IM	neg. current		-1	A
6.2-17	AOUT	IM	max voltage	-0.3	+5.5	V
6.2-18	VZP	POM	dVZP/dt	-5	10	V/us
6.2-19	PGND1...8	FLM	max voltage	-0.3	+0.3	V
6.2-20	PGND_VUP, PGND_S	POM	max voltage	-0.3	+0.3	V

#### Application Note:

The maximum voltage of VHx during highside on (firing) depends on the firing mode!

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## 6.3 ESD Characteristics

The ASIC pins are protected against electrostatic discharge according to the human body model (HBM), according to the machine model (MM) and according to charge device model (CDM):

<b>model</b>	<b>norm/standard</b>	<b>pin</b>	<b>ESD strength</b>
HBM	IEC 61340-3-1 (1.5kΩ, 100pF)	unconnected pins ECU internal pins ECU external pins VZP VZP against GND DIA	±1kV ±2kV ±4kV ±2kV ±4kV ±6kV
MM	IEC 61340-3-2 (0Ω, 200pF)	all pins	±200V
CDM	ESD STM 5.3.1-1999	all pins all corner pins	±500V ±750V

ECU external pins are:

VBAT\_MONx, N\_SLEEP, DIA, AINx, AI0x, PSIx, IGHx, IGLx