0 Document History

Version	Chapter	Description / Changes	Name	Date
1.12		last version of datasheet before release	AE/ESI3 Jungkunst	03/12/14
1.1	8	Sensor Transfer Function is updated.	AE/ESI3 Jungkunst	28.10.14
	2.3	The self test is robust against external accelerations of at least 15g in all directions.	AE/ESI3 Jungkunst	05/11/14
	6.3	Limits of “Cross-axis sensitivity after soldering on PCB”	AE/ESI3 Jungkunst	05/11/14
	2.4, 7	Limits of Oscillator monitoring	AE/ESI3 Jungkunst	06/11/14
	6.3	The following parameters have the limits over lifetime, of 4-Sigma distribution. • Nonlinearity of sensitivity (F.S.) • Nonlinearity of sensitivity (+/-5g) • Cross-axis sensitivity of SMA	AE/ESI3 Jungkunst	13/11/14
	10	Chemical compatibility of the third coating “HumiSeal Thinner 521 EU” from HumiSeal Europe is added	AE/ESI3 Jungkunst	05/11/14
	6.3	Typical and maximal value of BITE buildup time is added	AE/ESI3 Jungkunst	13/11/14
	6.3	The condition of the maximal value of turn-on-time at VDDI is corrected	AE/ESI3 Jungkunst	13/11/14
	~~6.4~~	~~Maximal Value of Input Voltage Hysteresis~~	~~AE/ESI3 Jungkunst~~	~~13/11/14~~
	9	Description of the placement of SMA660 in tape in order to avoid handling mistakes in the further fabrication is added	AE/ESI3 Jungkunst	05/11/14
	6.3	New wording for “All parameters except for the noise exclude noise effects.”	AE/ESI3 Jungkunst	13/11/14
	9.3	SMA660 temperature profiles for storage and Life time in qualification are included	AE/ESI3 Jungkunst	05/11/14

1.12	all	"Typ." is replaced with "Nominal"	AE/ESI3 Jungkunst	13/11/14
	2.2.6	SOC Speed and its threshold are corrected	AE/ESI3 Jungkunst	13/11/14
	5.1.1, 5.1.2, 5.1.3	Application diagrams are updated-> changed to old ones	AE/ESI3 Jungkunst	20/11/14
	4.7.6 4.8.6	Conditions for timing parameters are corrected	AE/ESI3 Kathmann	24/11/14
	2.7.1, 2.7.3	Contents related "ASSD monitors external influences" are deleted	AE/ESI3 Jungkunst	03/12/14
2.0		Datasheet release	AE/ESI3 Jungkunst	03/12/14
3.0	9.7	Phrase "for max. 3 soldering cycles", "The housing is released for a soldering stencil thickness of 120µm and 150µm" and "Sensor specific tests over temperature or at a non ambient temperature (~25°C) after soldering are not necessary to achieve any performance or quality goals." added	AE/ESI3 Beckers	17/04/15
	6.1 6 6.3 / 6.5 6.4 1 9.2 12	Chapter "General information" added "Besondere Merkmale" marked by /S/C Parameter "Output capacities SO-pin in tristate" and "Output capacity SO at high impedance state" set to max value 6pF Internal customer information regarding noise added Revision ID information added Chapter "Package dimensions" added Chapter "Documents and standards" added	AE/ESI3 Beckers	20/04/15
	1 8 6.3	Revision ID table added Sensor Transfer Function updated (|±0.4g|) 150000 start-up cycles added	AE/ESI3 Beckers	28/04/15
3.1	1 1.1 11	SMA660K and SMA661K added SMA661 added Delamination free variants	AE/ESI3 Beckers	02/07/15

3.2	1 9.8 11	TA660 KO added Chapter deleted Establishment 2005.06.30 added	AE/ESI3 Beckers	07/08/15

Central Acceleration Sensor

for Automotive Airbag Applications

SMA660 / SMA660K

SMA661 / SMA661K

BOSCH internal use only

Robert Bosch GmbH, Reutlingen, Germany

Content

1 Introduction

The SMA660/SMA660K or SMA661/SMA661K (in the following SMA660)[1] sensor is a central accelerometer for an airbag control unit in the passenger compartment. It is designed for crash sensing in automotive safety applications. The SMA660 is an in-plane, dual channel (x/y axis) MEMS accelerometer. The sensor provides acceleration data for microcontroller evaluation. The digital standard serial peripheral interface (SPI) of SMA660 allows bi-directional data transmission.

Table 1 Sensor type

Sensor Type	Bosch Part N°	Nominal g-Range	Comment
SMA660	0 273 141 131	±128g	
SMA661	0 273 141 237	±128g	See Chapter 1.1
SMA660K	0 273 141 249	±128g	
SMA661K	0 273 141 256	±128g	See Chapter 1.1

The acceleration sensor SMA660 is based upon a two-chip concept – the micro-machined mechanical sensing element (CMA581M) and a separate evaluation ASIC (TA660).

Table 2 Revision ID

ASIC	Revision ID
TA660 AA	00
TA660 AB	01
TA660 BA	10
TA660 BB	11
TA660 BC	12
TA660 BD	13
TA660 KO	13

Main features of the sensors are:

- Digital output with 12-bit resolution.
- 2 different SPI protocols, selection via SPI after power up
  - RB SPI Protocol (in frame)
  - Open SPI Protocol (out of frame)
- Supply Voltage 3.3V, 5V or 6.7V.
- On-chip oscillator 18MHz with internal monitoring

[1] The data sheet is valid for all sensor types described in Table 1. In order to improve the readability of the document in the following only the name SMA660 is used.

- Overall sensitivity tolerance of 5%
- Full bipolar self-test capability of mechanical and electrical signal path, triggerable via SPI
- Fast and slow offset cancellation after power-up
- On-chip digital low-pass filter with a corner frequency of 405Hz
- non-ratiometric output (output independent of power supply voltage)
- 0g output = 0 LSB
- SOIC8n package
- Automotive Temperature Range (-40...+125°C)
- Small Number of External Components
- Transmission of individual Part Number
- Design according ISO26262

1.1 SMA661 / SMA661K

SMA661/SMA661K is a delamination free variant of SMA660/SMA660K (see Chapter 11).

The difference in the package is:

- A new mold compound: G700LS instead of G600

- A new LF type: µPPF LF instead of standard cupper LF

The difference in the OPT content:

- Extended device ID "0x61"

Note:

For any use of products outside the released applications, specified environments or installation conditions no warranty shall apply, and Bosch shall not be liable for such products or any damage caused by such products.

This product is solely intended for use in airbag ECUs where the SMA660 is soldered onto a PCB. Its use is only permitted under the specified conditions and according to the environmental and loading conditions specified in this document.

Any change in the product's operating environment from the original scope of validation, or use in applications not approved by Robert Bosch GmbH, must be communicated to and released by Robert Bosch GmbH.

2 Technical Description

2.1 Working principle of sensing element

The acceleration sensor SMA660 is based upon a two-chip concept – the micro-machined mechanical sensing element (CMA581M) and a separate evaluation ASIC(TA660) are both packaged side-by-side in a standard SOIC8 narrow package featuring inverted lead frame technology.

On the sensor chip, a silicon surface micro machined comb structure is used as a capacitive accelerometer. The structure forms a differential capacitor, consisting of a free-movable seismic mass suspended by silicon spring bars, and fixed counter electrodes. Due to acceleration in the sensing axis, the seismic mass deflects. This deflection results in a capacitance change which is evaluated by the ASIC. The micro machined structures on the surface of the sensor chip are protected and hermetically sealed by a micro machined silicon cap.

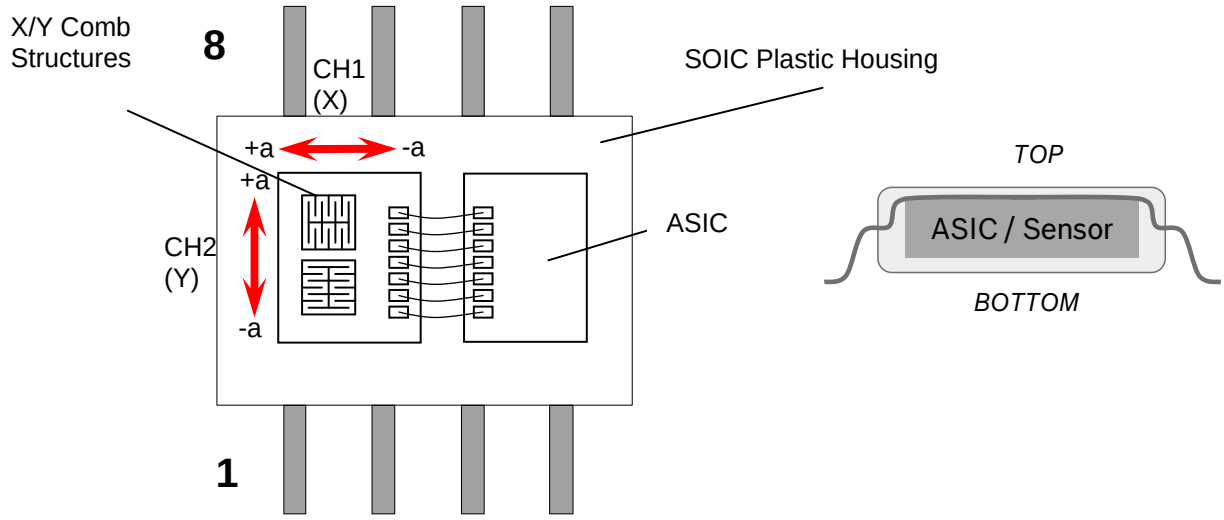


Figure 2-1 Schematic of SMA660 mechanical design and the orientation of the sensing axes

(Left: top view) (Right: side view).

The arrows in Figure 2-2 indicate the sensing directions. A positive acceleration of the sensor in +a direction leads to a positive output. A positive acceleration in –a direction correspondingly to a negative output.

The sensing direction of the SMA660 is in-plane with respect to the SOIC8 package footprint and thus in plane with the printed circuit board. An acceleration of the device in the "+a" direction results in a positive output change, a deceleration in this direction (or acceleration to the opposite side) results in a negative output signal change of the corresponding channel.

An example of a front crash situation is shown below.

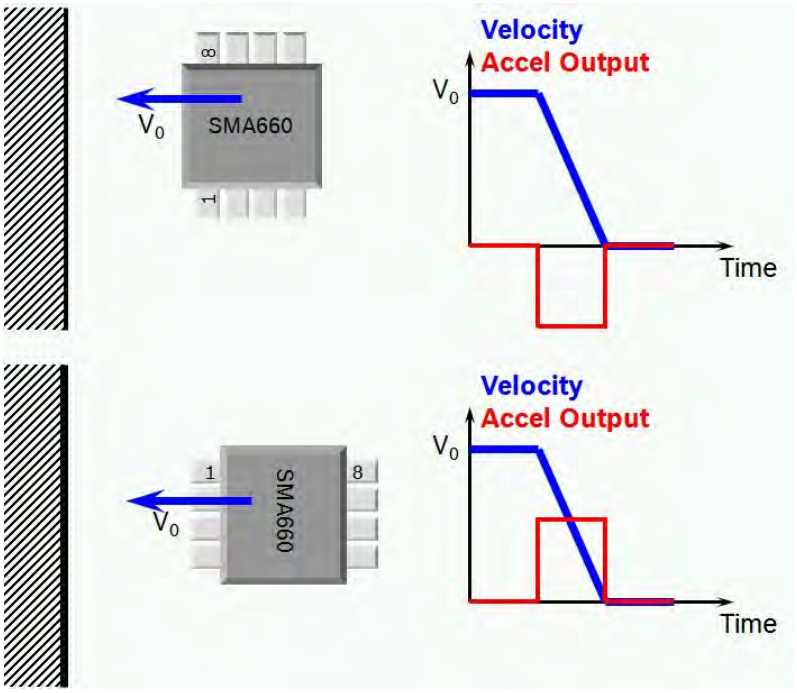


Figure 2-3 Schematic of a front crash situation (top view onto sensor) for x-axis (top) and y-axis (bottom)

2.2 Signal path

The schematic of SMA660 signal path and evaluation circuit is shown in Figure 2-4**.** An acceleration signal along the sensitive axis of the MEMS element causes a change of the capacitances of the MEMS element. This change is converted by a ΣΔ-converter into a digital serial bit stream. Then, the digital values are low-pass filtered by a decimation filter and an FIR-filter. Afterwards the gain is adjusted and the offset subtracted. To guarantee low jitter and high performance linear interpolation takes place. The 12 bits after interpolation are derived from the 16 bits by truncation of the 4 MSB (most significant bits). Each block of the signal path contributes to the overall signal delay t_{delay} as shown in Figure 2.5.

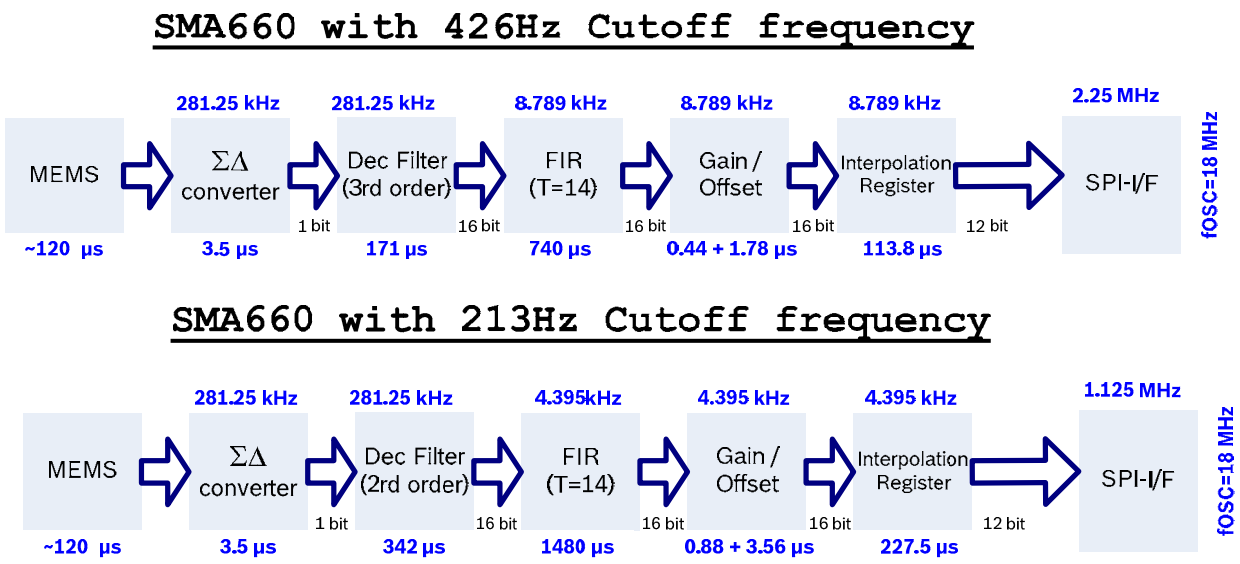


Figure 2-5 Schematic of SMA660 signal evaluation path and the delay introduced by the functional blocks

The differential capacitance change ΔC/C in the micro machined sensor element, corresponding to acceleration in the sensing axis, is converted into a digital serial bit stream by a Σ/Δ converter at a rate of $f_{OSC}/64$ (281.25 kHz in nominal case), where f_{OSC} is the frequency of the system clock (18MHz).

The acceleration signal of SMA660 is low-pass filtered by a decimation filter and a subsequent FIR filter. The overall corner frequency f_{-3dB} of both decimation and FIR filter is 426 Hz with a signal suppression better than a 3-pole Bessel filter.

Please note that the tolerance of the internal oscillator frequency directly affect the transfer function of the decimation filter and the FIR filter (e.g. the -3dB frequency). Together with the influence of CMA filter transfer function the corner freuency of SMA is shifted to 405Hz instead of 426Hz at 426Hz filter-setting and to 210.4Hz instead of 213Hz at 213Hz filter-setting. For filter-setting 106Hz and 53Hz the influence of CMA is neglectable.

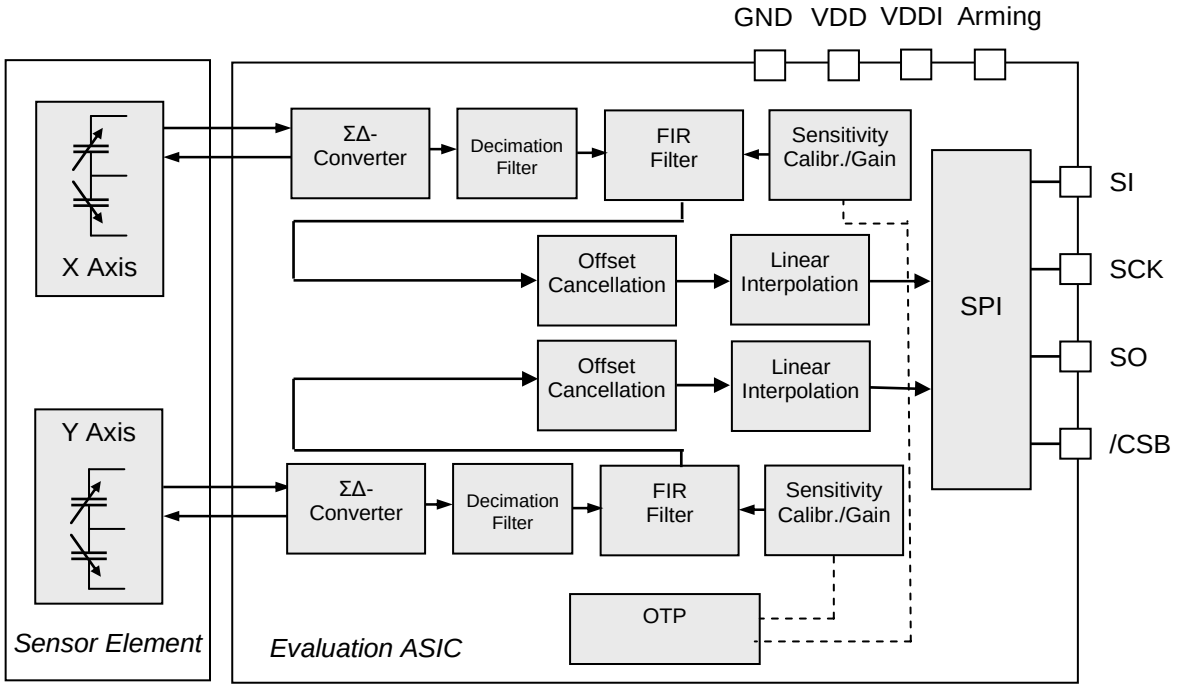


Figure 2-6 Schematic of SMA660 signal evaluation path and other functional blocks.

2.2.1 Decimation Filter

Decimation is a technique used to reduce the number of samples in a discrete-time signal. The process of decimation is used in a sigma-delta converter to eliminate redundant data at the output. In practice, this usually implies low pass filtering a signal and then down sampling to decrease its effective sampling rate. The function of the digital filter after a sigma-delta ADC is to attenuate the out of band quantization noise and signal components that are pushed out to the higher frequencies by modulator.

2.2.1.1 Filter characteristic of Decimation Filter

The decimation filter is a third order filter that down-samples the 1 bit digital signal from the Delta Sigma ADC, by a factor of 32,64,128,256 into a 19 bit wide parallel data word. The 19 bit data range is clipped in order to prevent an overflow. The transfer function is given by

$$H(z) = 1/D^{3} * \left(\frac{1 - z^{-D}}{1 - z^{-1}} \right)^{3}$$

Decimation factor D can be 32, 64, 128 or 256. The numerator represents the transfer function of a differentiator and the denominator indicates that of an integrator.

The update rate of the data word is equal to f_{OSC}/ (64*D)

f_{OSC} = oscillator frequency

D = decimation factor

2.2.2 Low pass Filter

The Characteristics of the digital Low Pass Filter consisting out of the Decimation and FIR-Filter is comparable to a 426Hz, 3rd order or 213Hz, 2nd order of Bessel filter characteristic.

Note: For SMA660, only 426Hz filter setting is released.

2.2.2.1 FIR Filter (DSP)

The second step of low-pass filtering is employed by an FIR filter with the following transfer function:

$$H(z) = \frac{\sum_{i=0}^{13} b_i \, z^{-i}}{\sum_{i=0}^{13} b_i}$$

The following coefficients are used to define the FIR filter:

$$\{b_0, \ldots, b_{13}\} = \{9, 25, 52, 87, 125, 157, 176, 176, 157, 125, 87, 52, 25, 9\}$$

These coefficients are symmetrical and yield a frequency-independent delay-time.

2.2.2.2 Filter Characteristic of Signal Path

Note: For SMA660, only 426Hz filter setting is released.

However, there are different filter-settings can be selected in register CFG_FILTER_CH1 and CFG_FILTER_CH2, such as 426Hz filter, 213Hz filter, 106Hz filter and 53Hz filter. By changing the filter settings, the group delay time is changed accordingly as the filter need different time to be settled.

PARAMETER 426Hz LP filter	MIN	NOM	MAX	UNIT
Filter cut-off frequency f-3dB (3dB bandwidth)*)		426		Hz
Group delay time of front end until output of IPOL *)		1.091		ms
Stop-band attenuation @ 1.5kHz – 3.5kHz	50			dB
Stop-band attenuation @ >=3.5kHz	60			dB

Frequency characteristics 426Hz LP filter

PARAMETER 213Hz LP filter	MIN	NOM	MAX	UNIT
Filter cut-off frequency f-3dB (3dB bandwidth)*)		213		Hz
Group delay time of front end until output of IPOL *)		2.115		ms
Stop-band attenuation @ 0.75kHz – 1.75kHz	50			dB
Stop-band attenuation @ >=1.75kHz	60			dB

Frequency characteristics 213Hz LP filter

PARAMETER 106Hz LP filter	MIN	NOM	MAX	UNIT
Filter cut-off frequency f-3dB (3dB bandwidth)*)		106		Hz
Group delay time of front end until output of IPOL *)		4.162		ms
Stop-band attenuation @ 1.5kHz – 3.5kHz	50			dB
Stop-band attenuation @ >=3.5kHz	60			dB

Frequency characteristics 106Hz LP filter

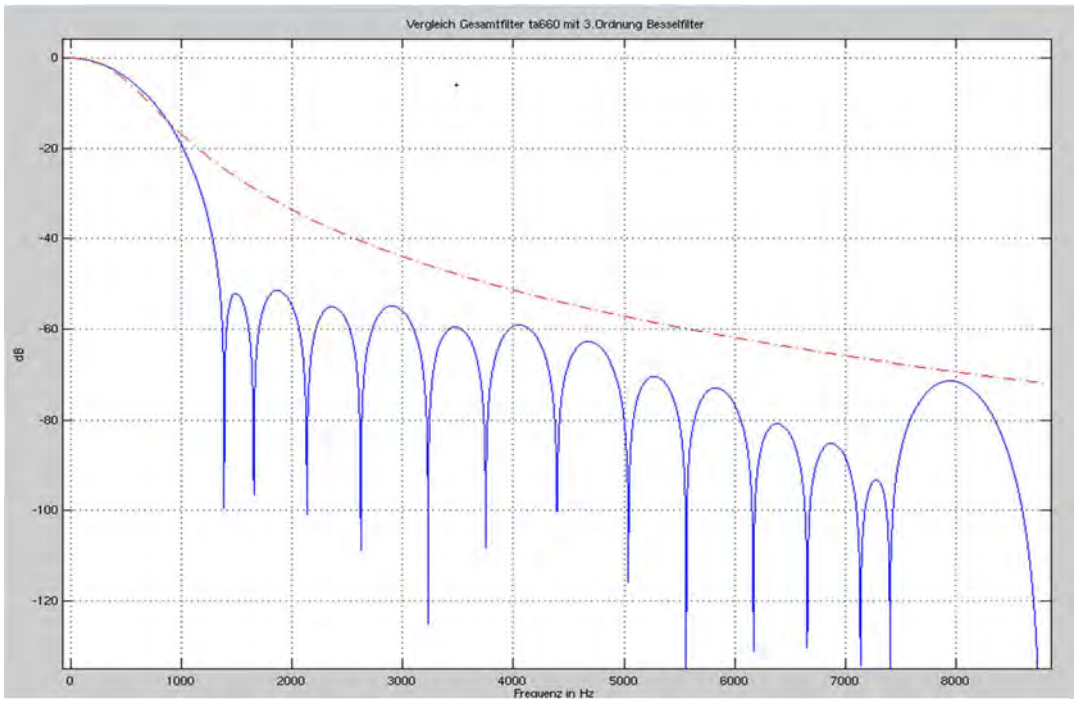
PARAMETER 53Hz LP filter	MIN	NOM	MAX	UNIT
Filter cut-off frequency f-3dB (3dB bandwidth)*)		53		Hz
Group delay time of front end until output of IPOL *)		8.258		ms
Stop-band attenuation @ 0.75kHz – 1.75kHz	50			dB
Stop-band attenuation @ >=1.75kHz	60			dB

Frequency characteristics 53Hz LP filter

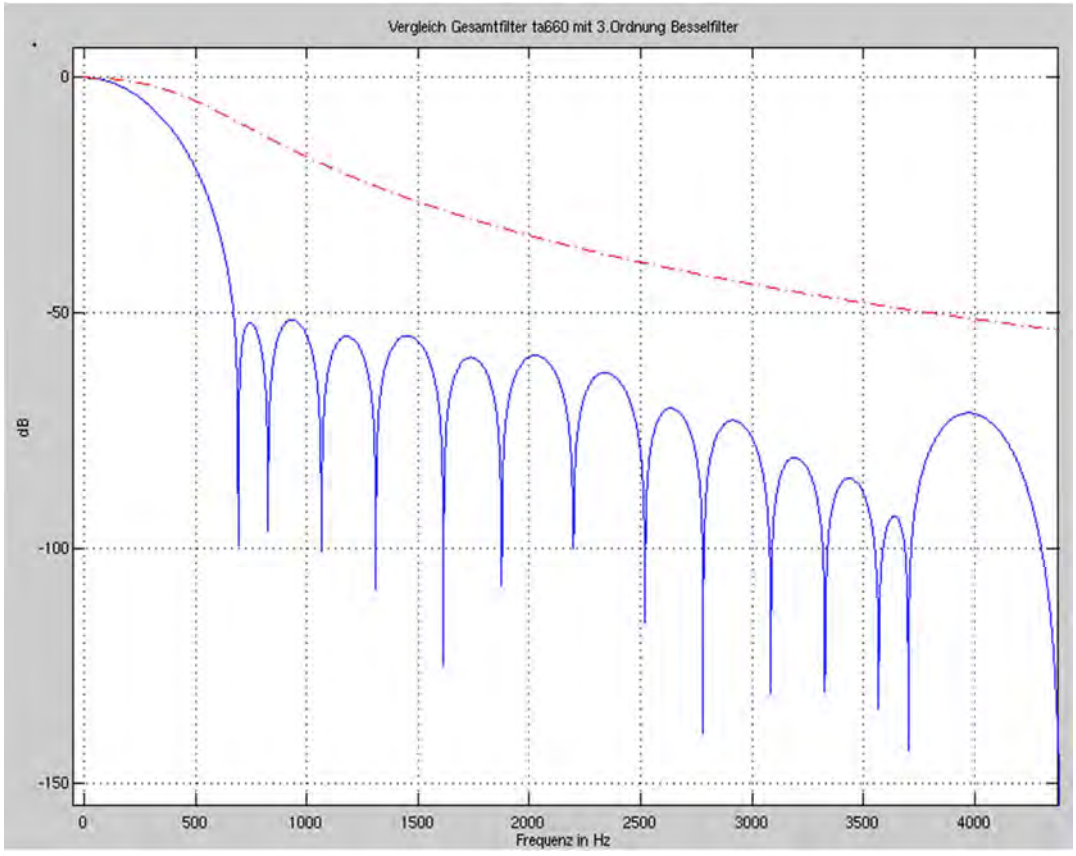
*) The nominal value is the design value of the filter. The minimal and maximal values depend on the frequency tolerance of the oscillator.

Low pass filter transfer function of TA660:

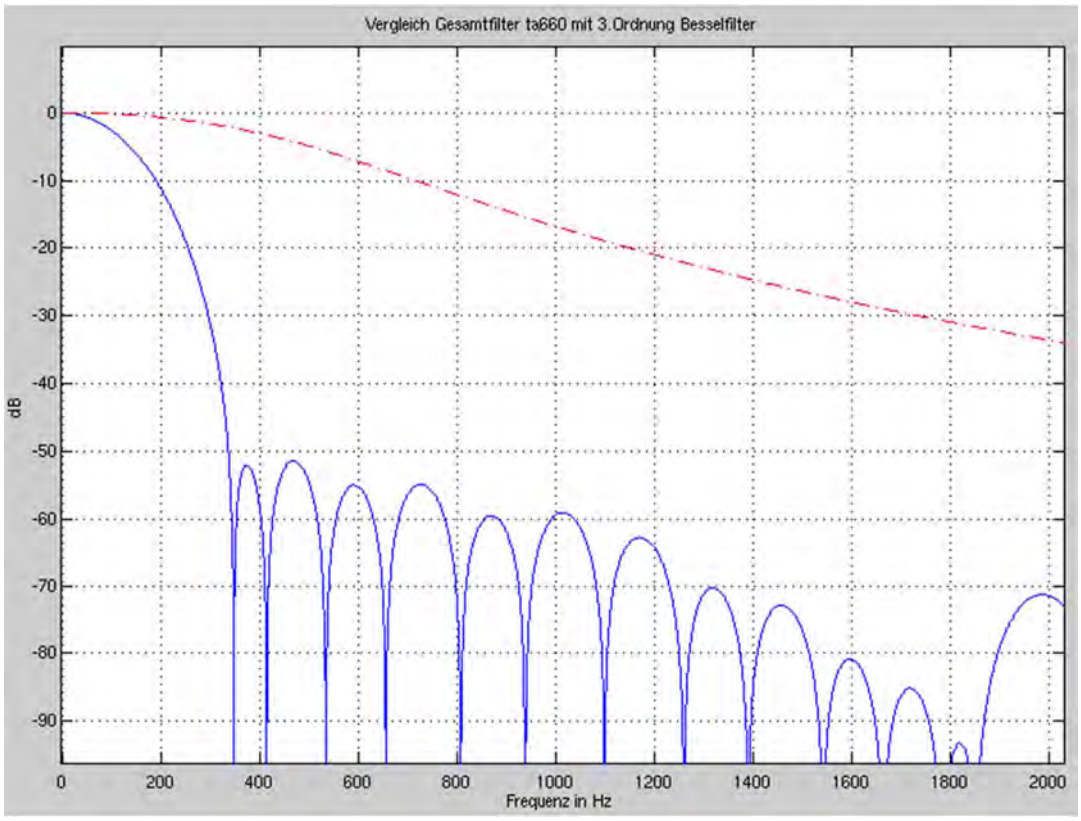
426 Hz Filter



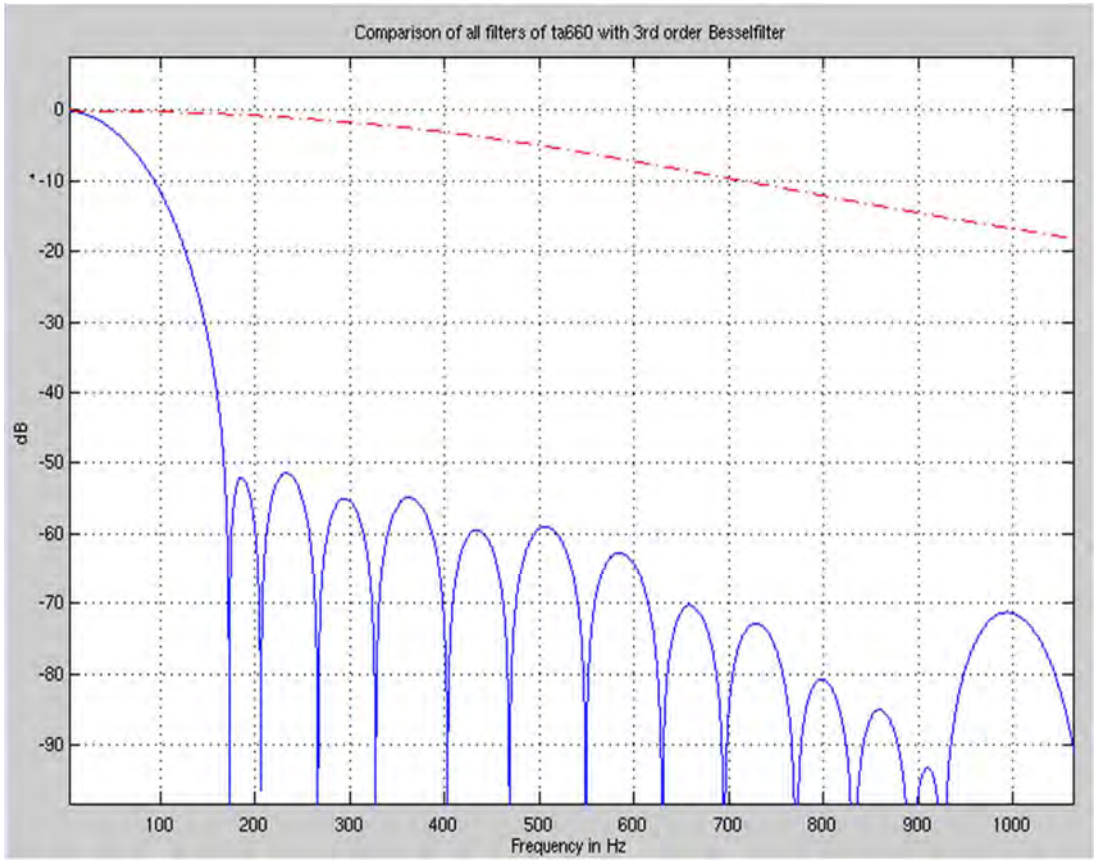
213 Hz Filter



108 Hz Filter



54 Hz Filter



2.2.3 Sensitivity and Resolution of the signal path

The sensitivity of the signal path can be adjusted to different sensors (CMA_Type) which can be connected with TA660. The TA660 with different sensors can used in different Ranges see table below.

			CMA_Type		
			120 G	480 G	800 G
OTP Content			00	01	10
SMA_Range	120g	00	Measurement Range 128g Coarse Gain = x1 Sens 16 LSB/g [12 Bit]	Measurement Range 128 G Coarse Gain = x4 Sens 16 LSB/g [12Bit]	Measurement Range 128 G Coarse Gain = x8 Sens 16 LSB/g [12Bit]
	240g	01	for characterization purpose: Coarse Gain = x2 Sens 32 LSB/g [12 Bit] no adjustment of BITE/Offset Limits	Measurement Range 256 G Coarse Gain = x2 Sens 8 LSB/g [12Bit]	Measurement Range 256 G Coarse Gain = x4 Sens 8 LSB/g [12Bit]
	480g	10	for characterization purpose: Coarse Gain = x4 Sens 64 LSB/g [12 Bit] no adjustment of BITE/Offset Limits	Measurement Range 512 G Coarse Gain = x1 Sens 4 LSB/g [12Bit]	Measurement Range 512 G Coarse Gain = x2 Sens 4 LSB/g [12Bit]
	xxx	11	for characterization purpose: Coarse Gain = x8 Sens 128 LSB/g [12 Bit] no adjustment of BITE/Offset Limits	not defined	not defined

Table 2-1 programming with different Range and CMAs

The set of SMA_Range and CMA_Type is necessary to setup the scale of the offset regulator in terms of g.

CMA-Type can be set over register MOTP_CMA_TYPE and SMA_range over register MOTP_SMA_RANGE.

As SMA660 uses CMA581M, which is a 120g sensing element, to employ a measurement range of 120g, the OTP content of both CMA_Type and SMA_range is 00.

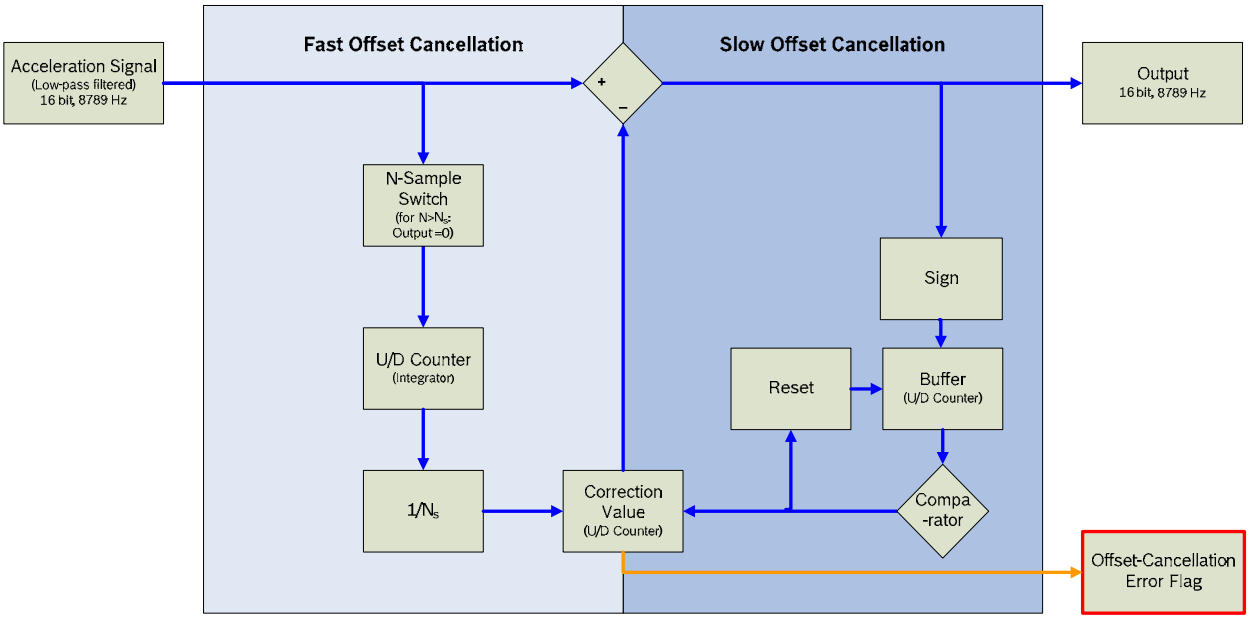
To compensate sensor element and ASIC sensitivity errors a sensitivity calibration is performed after the FIR filter. Sensitivity calibration is also called as a fine gain and can be done for each channel separately in register MOTP_SENS_CH1 and MOTP_SENS_CH2. Range of sensitivity calibration can be +/- 50% of the input signal. Accuracy of sensitivity calibration is +/- 0.3906% (derived from 100%/256LSB).

Signal Path Modul / Signal with Resolution	Bit exponent n (Bit value 2^n in LSB unit)	Gains of Module (Multiply to dC/C*2^15)
Sigma Delta: Convert dC/C to Bitstream		*1
BITSTREAM (1 BIT)	0	↓
Decimation Filter: Filter values and convert bitstream to 16 Bit word.		* 1
DEC_OUT (16 BIT)	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	↓
FIR Filter: Filter values and apply gains.		* 1,2324 * Coarse Gain * {DEC[SENS_CHx] / 512 +0,25}
FIR_OUT (16 Bit)	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	↓
Offset-Regulator: Shift 16 Bit word from FIR to the right, which reduce the 16 Bit integer value by 2.		* 0,5
OFS (16 Bit)	15 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	↓
Interpolator: Cut 16 Bits to 12 Bit		* 1
Sensor Data (12 Bit)	x x x x 12 11 10 9 8 7 6 5 4 3 2 1	

Table 2-2 Sensitivity and resolution of the complete signal path

2.2.4 Offset cancellation

The SMA660 provides on-chip offset cancellation for both channels to enable automatic offset adjustment of the 0g output level. The offset regulator will eliminate a static offset on the output of the SMA660. See chapter 2.2 for its position within the signal chain.



The offset cancellation includes two modes:

- Fast offset cancellation for offset at power-on (only possible before EOP)
- Slow offset cancellation for continuously running offset cancellation

The maximum offset correction value is ±50 g (i.e. ±800 LSB at nominal sensitivity). In case this value exceeds in either fast or slow offset cancellation mode, the OC1/OC2 flag is set, see chapter 4.8.4 .

2.2.5 Fast Offset Cancellation

After properly powering up or resetting the sensor, an initial offset may be present due to process deviations, temperatures or stress influences. The fast offset cancellation is applied during the start-up of the sensor in order to remove this initial offset.

The fast offset cancellation is realized by calculation of the mean value of N_S, minimum 64 samples. The number of samples can be selected for each channel over CFG_OC_LENGTH_CHX in SPI-Mode. During SPI-initialization the number of samples can be selected for each channel in SPI-mode, with a maximum of 1024 samples. In order to avoid unstable offset values in the beginning, there is a waiting time of 20 samples, before starting the fast offset cancellation. Afterwards each sample is divided by N_S (correction) and added (integrator) together as the estimated offset. After N_S samples have been added, the offset cancellation is finished. The mean offset reduction value is calculated from N_S samples, which equals $\frac{1}{N_S}\sum_{i=1}^{N_S} x_i$. After FOC the sensor delivers a signal without initial offset.

This value is subtracted from the initial signal including the offset. In the Open SPI protocol, the sensor data is masked while the fast offset cancellation is running; i.e., the stepwise cancellation is only visible in BOSCH SPI. In case sensor data is requested during the cancellation, the no data (ND) flag is sent for Open SPI. In BOSCH SPI the monitor flag “FOC_Busy_CH1” or “FOC_Busy_CH2” is set. The following table specifies the maximum fast offset cancellation duration for the different sample number (oscillator tolerance included):

Parameter		Max.	Unit
Maximum FOC duration	N_s =1024	126	ms
	N_s = 512	64	ms
	N_s =256	34	ms
	N_s =128	18	ms
	N_s =64	11	ms

A typical plot of the fast offset cancellation is shown below:

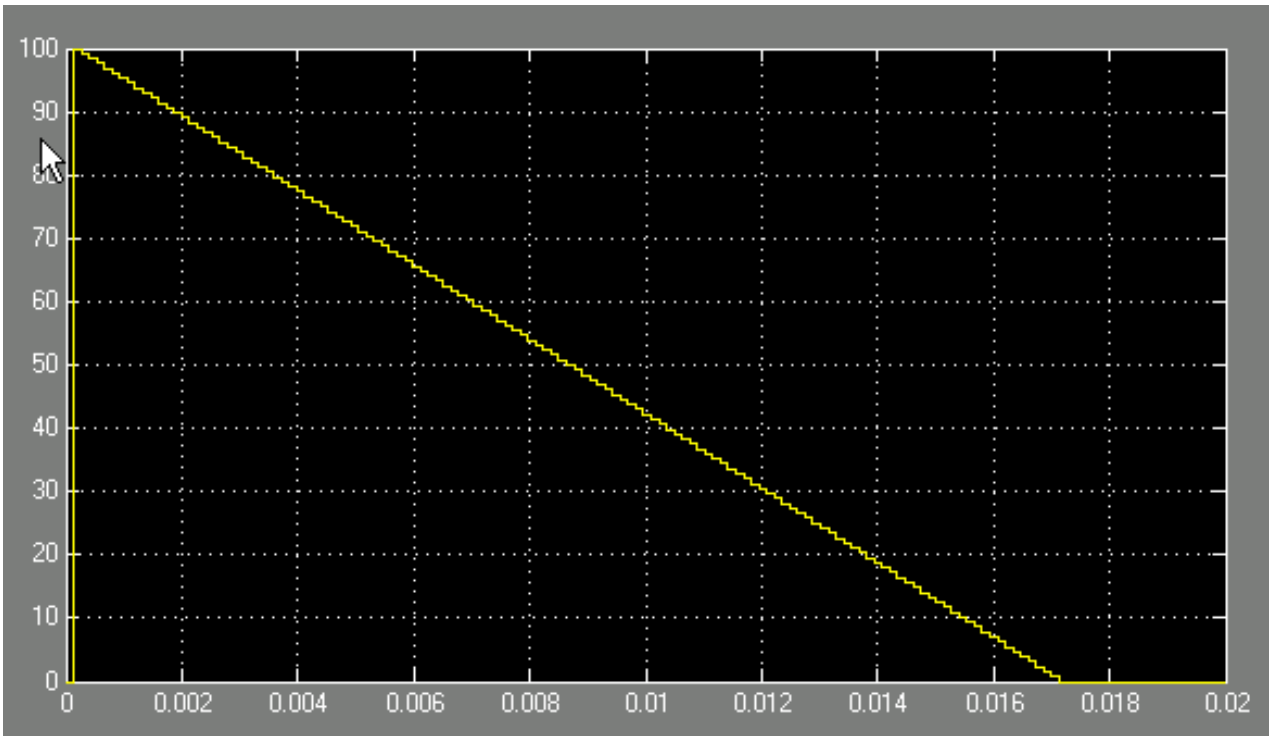


Figure 2-7 Example of Fast Offset Cancellation

2.2.6 Slow Offset Cancellation

A slow offset cancellation (SOC) is performed to compensate mainly offset drifts over temperature. Slow offset cancellation is realized by the common counter system. For each calculation cycle (update rate f_{sample}) the output signal is calculated by subtraction of the current offset compensation value from the current input value. The algorithm for determining the correction value consists of the following three steps:

(i) The sign of the offset-corrected acceleration signal is calculated and either increases or decreases the value of an up-down counter which serves as a buffer.

(ii) The counter value is compared to a fixed threshold of 4395. If this threshold is reached, two reactions follow: The first buffer counter is reset and a second up-down counter is either incremented or decremented.

(iii) The value of the second up-down counter constitutes the offset correction value which is subtracted from the low-pass filtered acceleration signal. It is incremented or decremented with steps of 0.5LSB.

The maximum correction rate is reached if the offset-corrected signal is either constantly larger or smaller than zero.

Independent of measurement range, the output is adjusted at a fixed step 0.5LSB/0.5s for 12 Bit SPI output after SOC is triggered. The residual static offset error for SOC is lesser than 0.5LSB for 12Bit.The design of the slow offset cancellation is symmetrical to zero.

It is very important that the CFG_OC_LENGTH_CHX bits have to be the same as in Fast Offset Cancellation. Otherwise there will be an offset jump.

In case of exceeding the control range (MOTP_RANG_CTRL) in slow offset compensation mode, the sensor sends an ‘OC1 / OC2’ flag.

As alternative of SOC 1, SOC 2 with a Slow Offset Cancellation Speed of 0.5LSB / 11.5s can be triggered. This functionality works identically as described above except for the speed of regulation.

2.2.7 Linear Interpolation Function

The SMA660 provides a linear interpolation of the signal. This interpolation scheme is always active. Each transmitted sensor value to the ECU is an interpolated value. It is linearly interpolated between the two most recent sensor values in the digital signal path (every 113.8µs at filter update rate of 8.79kHz) that have been generated by the filter, adding an additional latency of one filter update period to the filter path. The interpolator also transforms 16bit data to 12 bit by cutting off the 4 MSB.

The interpolation is performed in 256 equidistant steps. The output register of the interpolator is updated with 2.25 MHz for 12-Bit sensor data that gives a new calculated value every 0.44µs.

2.3 Built-in Self Test (BITE)

SMA660 features a Built-in Self Test function of the complete mechanical and electrical sensor signal chain. During the self-test procedure the seismic mass of the sensing element is physically deflected to a positive and negative direction by applying an electrostatic force between the electrodes of the seismic mass and one of the two fixed counter electrodes, respectively. The BITE voltage is equivalent to an applied acceleration.

The self-test is activated by sending the appropriate SPI command (see chapter 4.7.5.19 and 4.8.5.22). The self-test can be activated for both channels and directions (positive and negative direction). As long as a self

test is activated, each transmitted value from the sensor is marked with a dedicated flag indicating that self test data is sent. The self test response will remain as a static offset on the output until the self test is deactivated. Any acceleration applied to the sensor with the self test switched on will be seen on the output as a superposition of both acceleration and self test signal.

BITE can only be activated after the initialization phase of the sensor and before EOP command is sent in order to avoid BITE during normal operation (see chapter 4.3.3).

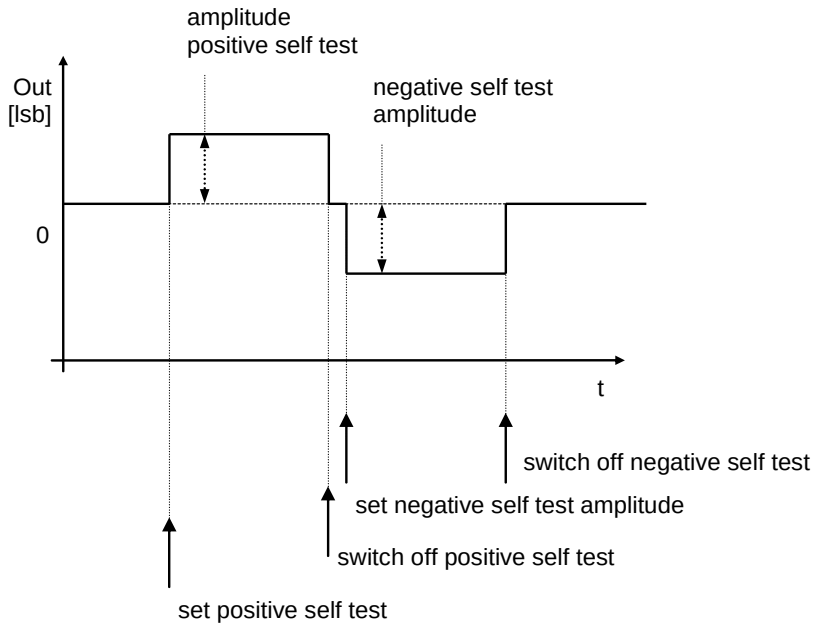


Figure 2-8 BITE response of SMA660 for one channel

Application hints:

An evaluation of the self test should include the measurement of both directions and channels. The self test response should be verified by comparison with the expected value after switching the test signal on and off. The sensor can be switched from positive to negative test signal and vice versa directly. It is mandatory to trigger self-test for both channels simultaneously (Ch1 positive & Ch2 negative, then Ch1 negative & Ch2 positive or vice versa).

If additional acceleration is present when applying BITE, it has to be smaller than 15g in all directions to ensure BITE works properly.

Before BITE activation, fast offset cancellation should be performed and finished. This will ensure exceeding measurement range and foster easy evaluation of BITE values.

For evaluation, BITE pos/neg can be compared to new part values. These values are stored internally and can be read out via SPI. New part values are stored as an 8 Bit value representing the 8 regular most significant bits (Nominal resolution of these values is 1LSB/g).

2.4 Clock counter and Oscillator monitoring

Oscillator monitoring is a mechanism to check for the correct functionality of the Oscillator. It can detect deviations of the sensor oscillator with respect to the system time reference.
The monitoring is done by the comparison of the clock counter registers value against two limits. Limits for the checking are set in two registers (clock counter min register CFG_CLK_CNT_LIMIT_MIN and clock

counter max register CFG_CLK_CNT_LIMIT_MAX). A clock counter value is incremented by one at a rate of $f_{OSCM}=f_{OSC}/8=2.25$ MHz. Its value is reset to 0 if the counter has reached its maximum value (2^{16}-1, "wrap-around counter"). A limit of +/-5% is recommended for SPI Oscillator monitoring (The tolerance of SPI Master timing is not included). The limit can be extended to +/-8%, with which the safety goal is still reachable.In case the clock counter limit is exceeded, then an internal failure counter is incremented.

Clock Counter Fault Threshold is a maximum number of failures allowed to be observed and is in configuration register CFG_CLK_CNT_FLTCNT. When the failure counter value is higher than the Clock Counter Fault Threshold then a clock failure signal is generated.

Note that any clock failure (visible by monitor flag OSC) will be suppressed by setting CFG_CLK_CNT_FLTCNT to 0xFF.

There are three different operation modes, which can be configured with the "WR_CONFIG_1" command by writing the OSCM bits (see Open SPI and Bosch SPI)

1) Mode 1 (default): OSCM bits = "00": clock counter running and readable, disable clock counter register and oscillator monitoring flag
   In the first way the evaluation is done on the system level. The clock counter value can be read out on the system level in periodic intervals (by sending "RD_CLOCK_COUNTER") and is then evaluated on system level if the value is acceptable.

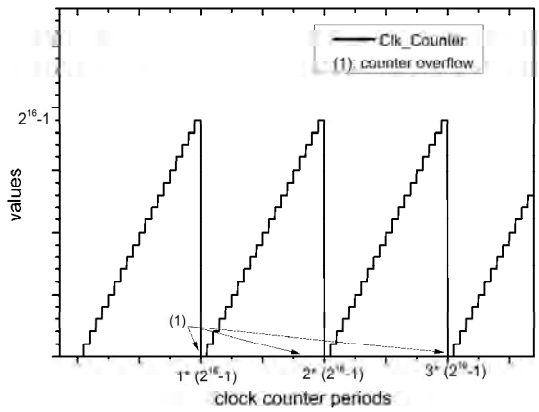


Figure 2-9 Oscillator monitor Mode1 (OSCM="00").

   The Clk_Counter is incremented with f_{OSCM} and is reset after overflow occurs (~30ms).

2) Mode 2: OSCM bits = "01": enable clock counter register, disable oscillator monitoring flag
   The current clock value is captured and reset to 0 by reading sensor data from x-channel ("READ_SENSOR_DATA_CH1"). The captured register value can then be read out on the system level (by sending "RD_CLOCK_COUNTER"). The running clock values cannot be requested in this mode, only the captured values. No monitor flag is set.

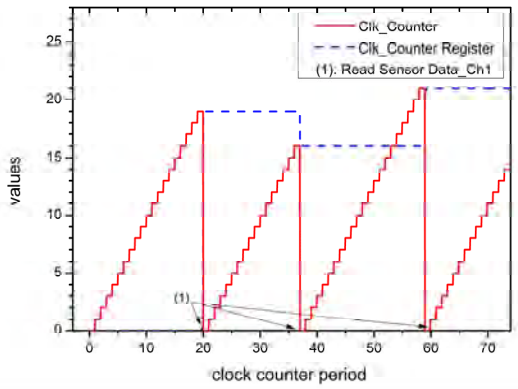


Figure 2-10 Oscillator monitor Mode2 (left) OSCM=”01”.

The Clk_Counter (red) is incremented with f_{OSCM}. After every “Read Sensor Data Ch1” request the current value is written into the Clk_Counter Register (blue) and the Clk_Counter is reset to 0.

3) Mode 3: OSCM bits = “11”: enable clock counter register and oscillator monitoring flag
The same as Mode 2 but with enabled monitor flag. This is done by continuous comparison of the captured clock counter registers value against two limits. These limits can be configured by the customer (clock counter min register and clock counter max register). In case the clock counter limit is outside this min-max interval, an internal failure counter is incremented. In case it is inside the limits, the counter is reset to 0. Clock Counter Fault Threshold is the maximum number of failures allowed in a row to be observed without setting the flag (limit can be configured with “WR_CLOCK_COUNTER_FLTCNT”; default is 3). When the failure counter value is higher than the Clock Counter Fault Threshold value then a clock failure flag is set (“OSC” flag see 4.7.4 Open SPI and 4.8.4 Bosch SPI).

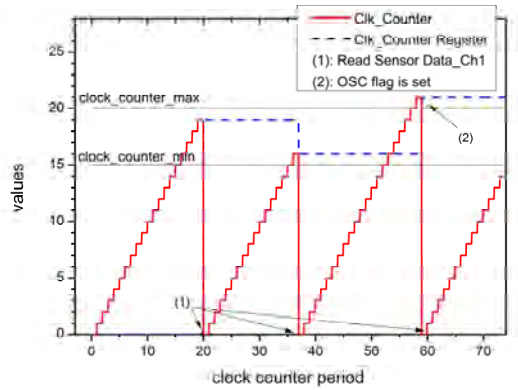


Figure 2-11 Oscillator monitor Mode2 (left) OSCM=”11”.

As Mode 2 but with activated min/max limits, fault counter and monitor flag.

4) 10 = not defined, (writing this value to the register will be ignored. Register content remains unchanged.)

Application hint:
For both ways the limits should be chosen to include not only the tolerance of the sensor oscillator frequency (+-5%) but also the tolerances of the system clock, because only relative timing jitter can be monitored.

Mode 2: The first latched counter register value (latched after the first x-channel read command) should be ignored since no correctly defined time difference exists. Only the latched values starting with the second Read Sensor Data can be used on system side to check oscillator stability.

Mode 3: If the counter values are outside the programmed limits (and Fault counter is programmed to 0), NRO will not be set already on the first x-channel read command. A second x-channel read command is needed (as in mode 2, to have a defined time difference between the commands) and if a failure has occurred, NRO will be set to 1.

2.5 Under-/Overvoltage Detection

Undervoltage Detection is used to ensure that the sensor is always in a safe state: Either working fully in specification or no communication occurs or an "Error Flag" is transmitted.
Overvoltage failures of internal voltage regulators lead to SO tri-state (VDDA, VDDD and VDDI is monitored in all modes).
If applied voltage larger than the maximum operating voltage (VDD) for 5V and 6.7V mode, it must be detected and avoided by the system.

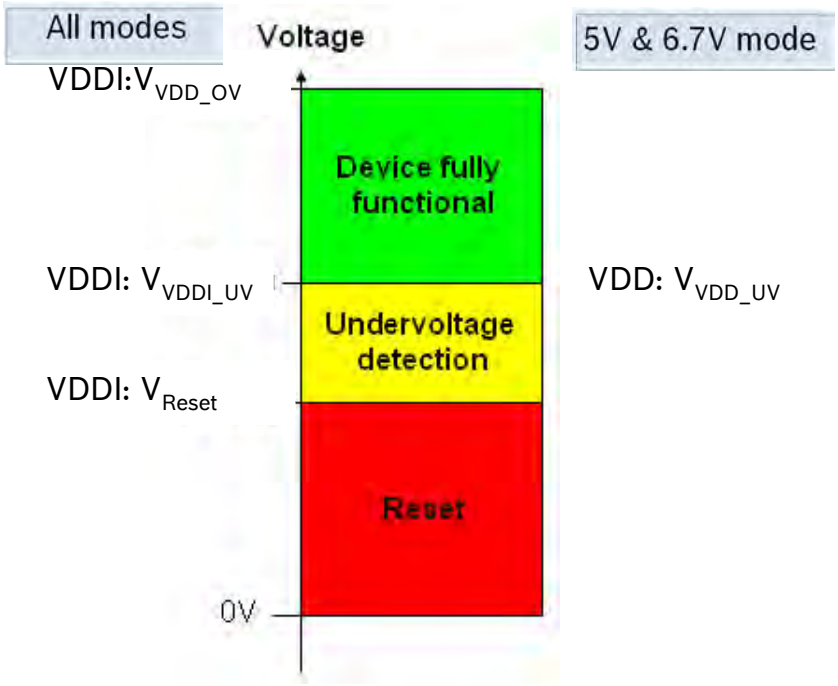


Figure 2-12 General undervoltage behaviour of VDDI/VDD voltage.

2.5.1 VDD Undervoltage Detection

This monitoring is active in 5V & 6.7V mode. In 3.3V mode the VDD Low voltage monitor will be disabled. The behaviour can be divided in three regions, dependent on the VDD voltage (see Figure 2-13). An active VDD low voltage detection leads to Undervoltage flag

Parameter @ 5V and 6.7V	Symbol	Min	Nominal	Max	Unit
Low voltage detection threshold VDD	V_{VDD_UV}	4.33	4.41	4.5	V
Hysteresis VDD	$V_{VDD\_UV,hyst}$	1		50	mV

2.5.2 VDDI low-voltage power-on-reset (POR)

After ramp-up of the external supply voltage when VDDI is above the reset threshold, the reset circuit releases the SPI communication of the sensor.
Hint: Reset is more dominant than VDDI low-voltage detection. In case of an overlap of ranges from VDDI low voltage detection and reset SMA660 is always in safe state.

Parameter	Symbol	Min	Nominal	Max	Unit
Power-on reset threshold VDDI	V_{Reset}	2.5	2.71	3.05	V
Hysteresis VDDI	$V_{VDDI,hyst}$	70	100	140	mV

2.5.3 VDDI low-voltage detection

In active VDDI low-voltage detection an undervoltage event leads to undervoltage flag (see “Error management” in Chapter 4.7.4 & 4.8.4).

Parameter	Symbol	Min	Nominal	Max	Unit
Low voltage detection threshold VDDI	$V_{VDDI\_UV,down}$	3.00	3.076	3.13	V
Hysteresis VDDI low voltage detection	$V_{VDDI\_UV,hyst}$	1		50	mV

2.5.4 VDDI high-voltage detection

For active VDDI high-voltage detection a higher voltage event leads to no communication over SPI-interface (SO in tri-state). This state can only changed through a reset or by activating testmode (analog/digital).

Parameter	symbol	Min	Nominal	Max	Unit
High voltage detection threshold VDDI	V_{VDDI_OV}	3.48		3.7	V
Hysteresis VDDI high voltage detection	$V_{VDDI\_OV,hyst}$	-1		50	mV

2.5.5 VDD high-voltage detection

For VDD, no voltage detection is implemented. This failure has to be monitored by the system.

2.6 Arming Pin

The Arming-Pin is used to indicate that the measured acceleration is above the configured threshold.

If arming function is active, a switch in ASIC will be short to GND. This switch is placed on the ARMING pin. By using an external pull up resistor, which limits the current through the switch, an arming function can be realized in an active low state.

It is recommended to use a pull up resistor of 3kOhm, 5kOhm, or 6.7kOhm for SPI Mode 3.3V, 5V and 6.7V respectively.

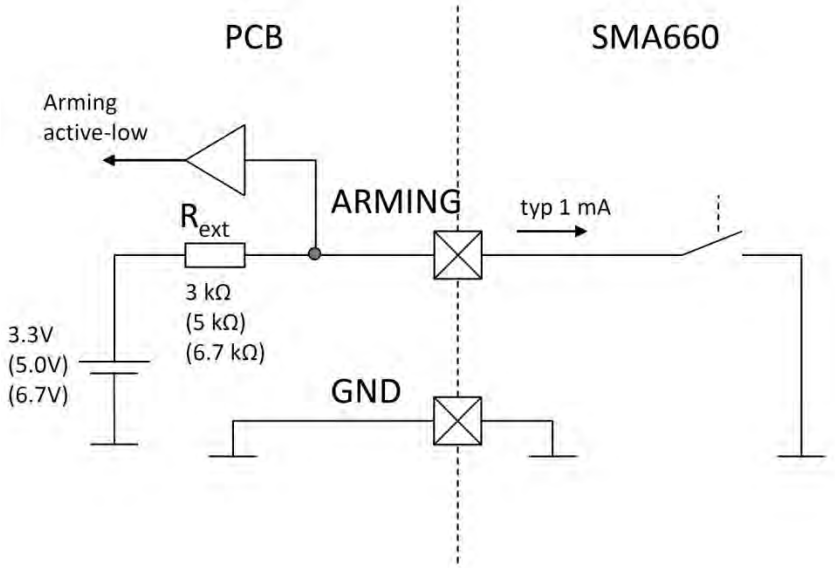


Figure 2-14 Application circuit of the arming pin.

2.6.1 Digital Control

After a request of sensor data with or without activated self test, the sensor data of the requested channel is compared to the internal arming threshold (Signal Config Arming Threshold).

For dual axis sensors, this functionality is independently performed on both channels. As soon as a consecutive number of sensor-data-samples (SAMPLE_CNT+1, defined by value in Config Arming Sample Count) is above the threshold the Arming Pin is activated. The Sample count can be 0, 1, 2, or 3. See section 2.6.2 for an example.

The activation time is dependent on the selected SPI-protocol.

- Open SPI: After the response from the previous sensor-data request and CSB is high (max 70ns after CSB high)
  - The example below: SDR = Sensor Data Request of Ch1 (above trigger threshold); R = Response. The red arrow indicates when Arming pin gets active for each Sample_CNT level.

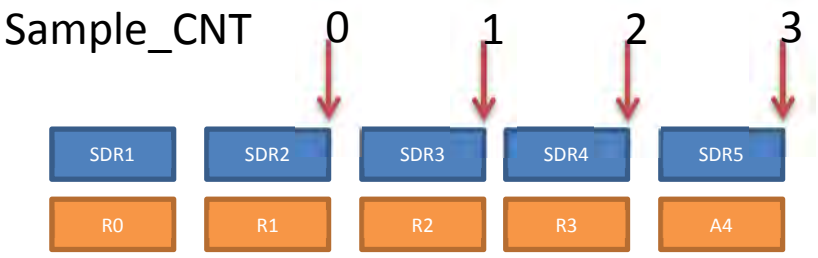


Figure 2-15 Arming pin activation scheme for Open SPI.

- BOSCH SPI: Directly after the sensor-data request frame is transmitted and CS is high after Read Sensor Data (max 70ns after CS high)
  - The example below: SDR = Sensor Data Request of Ch1 (above trigger threshold); R = Response. The red arrow indicates when Arming pin gets active for each Sample_CNT level.

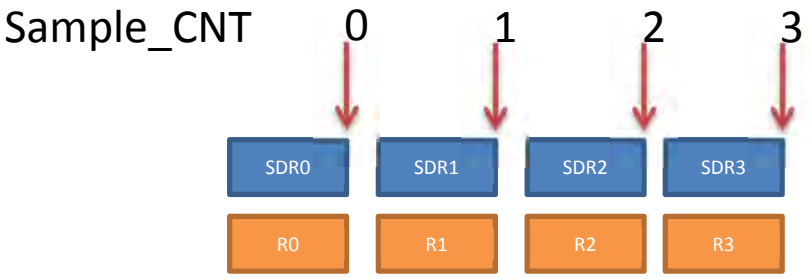


Figure 2-16 Arming pin activation scheme for Bosch SPI.

When the threshold is reached, the arming pin has digital output low during the next data frame when the sensor data of the requested channel are being transmitted:

- Open SPI: while CS low parallel with sensor response
- BOSCH SPI: while CS low before 1_{st} bit of sensor data, deactivation time after next CS low.

Otherwise, (also in case of error transmission) the arming pin stays at high.

Once the Arming Pin is active and the sensor-data drops below the arming threshold the Pulse-Stretching is activated. Pulse-Stretching extends the activation time of the Arming Pin by approx. 250 ms. If the sensor-data is still below the arming threshold after Pulse-Stretching is complete the Arming Pin will be deactivated. If the sensor-data is above the arming threshold for SAMPLE_CNT+1, the Pulse-Stretching is reset and Arming Pin kept activated.

The Arming Pin will not be activated, if one of the following conditions is true:

- fast-offset-cancellation is active
- an error condition is active:
    - Open SPI: Status-Flags, NRO, MOSI-CRC
    - BOSCH SPI: PF, TF, MOSI-CRC

The default status of the Arming Pin after reset = High

Hint:

- CFG_ARMING_TH = 4 => 16 LSB sensor data (factor 4); +-1g threshold
- Arming Pin cannot be activated before EOP (self test leads not to active arming pin)

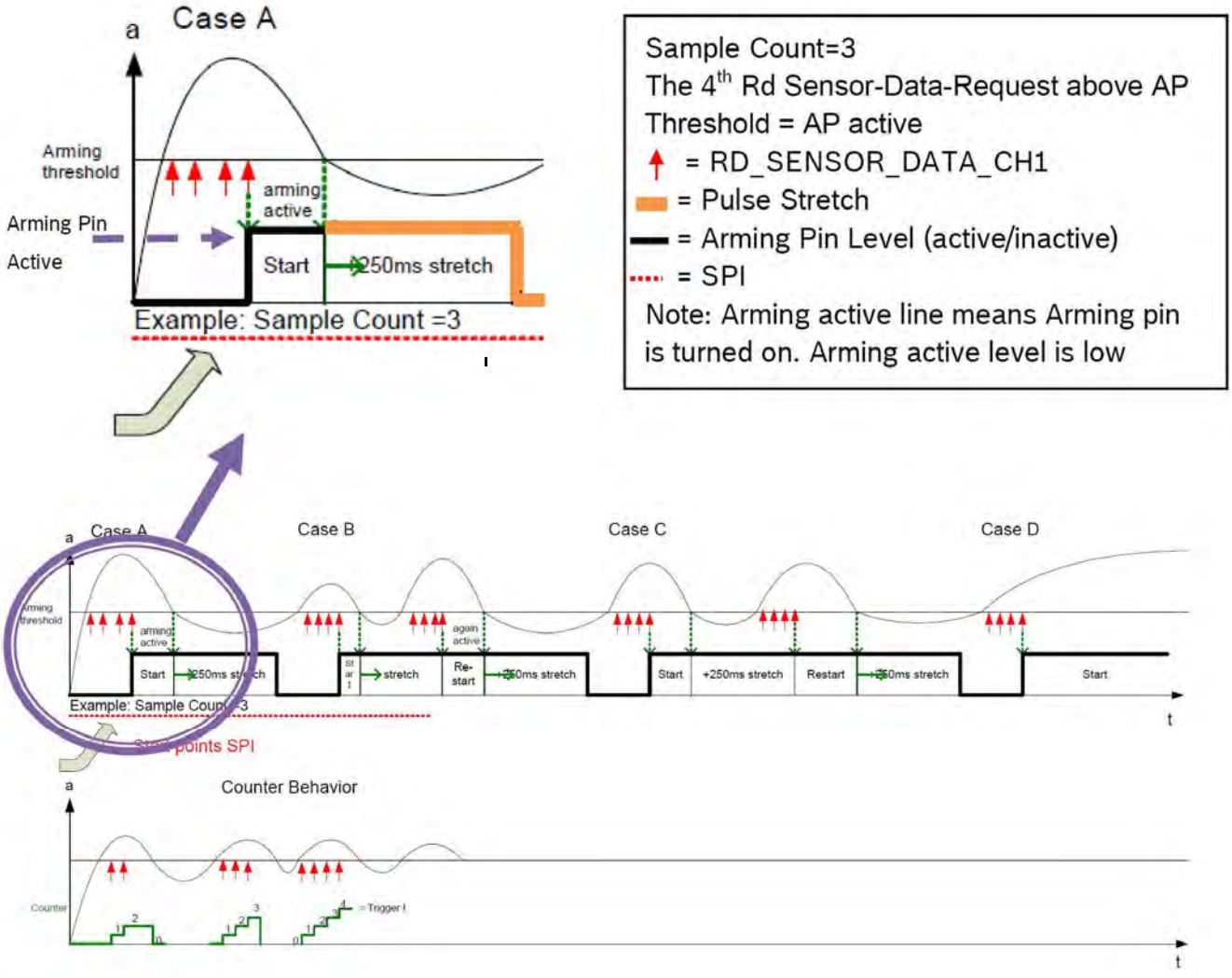
2.6.2 An Example of activating Arming Pin

This is an example of activating Arming Pin.

AP Configuration:

CFG_ARMING_SAMPLE_CNT = 3

Sample count is configured to 3. After 3 Sensor-Data-Request, and all 3 requests exceed the AP threshold, the following 4th Sensor-Data-Request activates the Arming Pin (Sample Count+1). Once the signal drops below the AP threshold, the pulse stretcher begins the countdown starting from 250ms (Case A). With every 3rd sample above the threshold, the Pulse Stretcher restarts. Once the signal drops below the threshold, the pulse stretcher finishes the countdown but does not reset.



Parameter / condition	Symbol	Min	Nom.	Max	Unit
Maximum allowed current in case of a closed arming switch	I_{ARMING}			1.5	mA
Resistance of closed arming switch	R_{ON_ARMING}	30		400	Ohm
Resistance of open arming switch	R_{OFF_ARMING}	50			kOhm
Pull Up Resistor (@3.3V Mode)*	R_{ext}		3		kOhm

Parameter / condition	Symbol	Min	Nom.	Max	Unit
Pull Up Resistor (@5.0V Mode)*	R_{ext}		5		kOhm
Pull Up Resistor (@6.7V Mode)*	R_{ext}		6.7		kOhm

Note: * Only recommended value. The value must be chosen, in order not to exceed I_{ARMING}.

2.7 Advanced Safety Sigma-Delta (ASSD)

2.7.1 Basics

The Advanced Safety Sigma Delta (ASSD) is a monitor for the Sigma Deltas which are used for acceleration channels of the TA660. The structure of the ASSD and the sigma-deltas of acceleration channels are the same, but the ASSD provides a constant reference signal. A disturbance of the signal path which leads to a wrong signal in the acceleration channels leads also to a change of the ASSD signal.

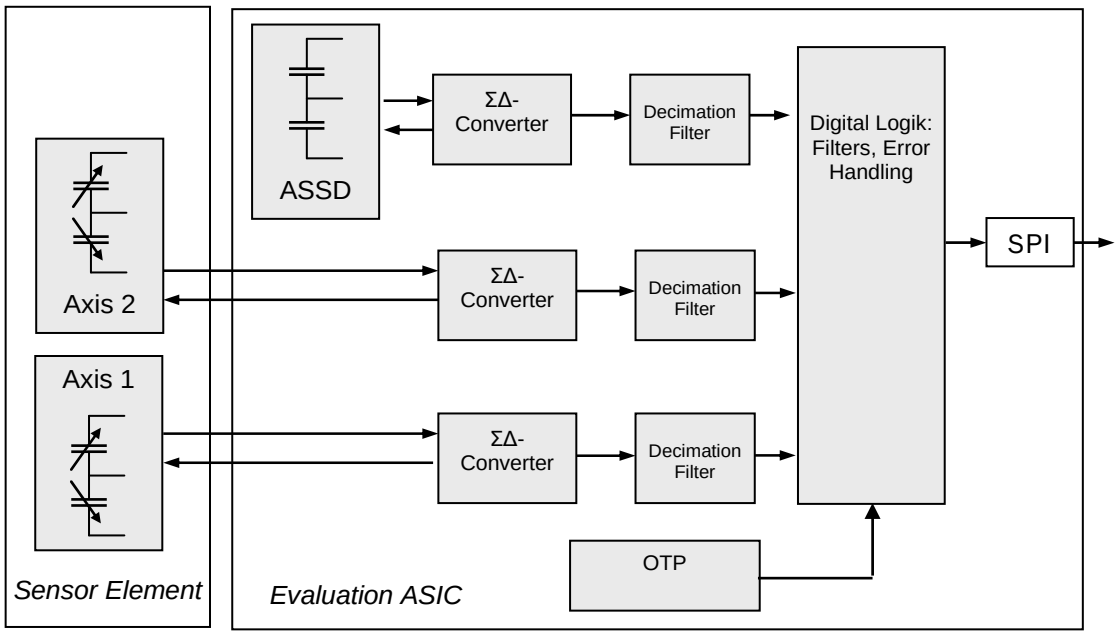


Figure 2-17 Block diagram of sensor inclusive of ASSD channel.

The Analog Front End of ASSD fulfils the following requirements:

1. Sensitivity/Gain is higher than in functional channels
2. Bandwidth equal or larger than in functional channels
3. Signal Delay is lower than in functional channels
4. Input range is the same as in functional channels
5. Linearity is the same as in functional channels
6. Resolution is the same or higher than in functional channels

The Monitored parameters through ASSD are internal references for the functional ADCs (Sigma Delta):

1. +/- V_{ref} – Voltage reference

2. I_{ref} – Current reference
3. S_{gnd} – Reference ground
4. Power Down – Power Down signal for IDDQ measurements

The ASSD is constructed like a typical acceleration channel with the following sub-blocks:

1. SD-Converter with an dummy sensor (incl. IntCaps)
2. Decimation Filter
3. Offset Regulator
4. Comparator which check programmed limits
5. Selftest-Circuit which using IntCaps (ASSD-BITE)

If the ASSD signal exceeds its limits, which are programmed for each part internally in the final test, the ASSD error counter will do an increment. If ASSD flag counter exceeds ASSD_FLAG_CNT limit, an error code arises.

The decimation filter corner frequency of ASSD is selected over MOTP_ASSD_FREQ as 580Hz.

Moreover, the Analog Front End of ASSD is designed to provide a higher sensitivity or gain, an equal or larger bandwidth, a lower signal delay and a same input range, linearity and resolution as the acceleration channels.

The ASSD is active by writing 1 to MOTP_ASSD_EN of CFG_CONFIG_1.

If the ASSD signal exceeds its limits an error code will occur (ASSD error see Monitor I flags). The ASSD monitor can be switched off via WR_CONFIG_1 command (see Open SPI commands in 4.7.5.23 and Bosch SPI 4.8.5.26 for Bosch SPI; default value=on). The ASSD monitor is an internal monitor, so that no evaluation of ASSD signal is necessary in the system.

2.7.2 Offset cancellation

A fast offset cancellation (FOC) is performed to compensate offset values of ASSD originating from the internal capacitors. Therefore, the offset cancellation averages 64 samples at a rate of 8.79 kHz.

The slow offset cancellation (SOC) compensates offset drifts over temperature. SOC of ASSD channel can be triggered with SOC speed I but not Speed II. For 16 bit resolution SOC rate of ASSD is 2LSB/s. Offset cancellation is switched on or off with DEMAND_OFFSET_CANCELLATION command (see commands in 4.7 Open SPI and 4.8 for Bosch SPI).

2.7.3 Failure monitoring

As a part of the safety concept the ASSD is developed in order to monitor the following parameters:

ASSD monitors the internal references: voltage reference (V_{ref}), current reference (I_{ref}), reference ground (SGND) and the power down signal (PD) for IDDQ measurements (PD).

2.7.4 ASSD self test (ASSD BITE)

A built in test (BITE) is also implemented for ASSD. If ASSD BITE is triggered via DEMAND_FOR_TEST in SPI mode, the internal capacitors will be switched to the ASSD front end. Positive or negative deflection can be configured similarly as for the acceleration channels. The deflection during the BITE test must be within fixed thresholds, which are +/-40% of delta C/ C at final test, to pass the test. This is done internally. A successful completion is indicated through a flag-free state (no ASSD error flag after EOP). The typical BITE activation time (Build up time) is 3.6ms. The BITE test for ASSD can be activated in parallel to the BITE Test for Ch1 and Ch2.

2.7.5 Important notes for using ASSD

TST flag should be monitored externally to determine the end of filter flush time after BITE. After TST flag is low, EOP can be activated. If TST flags are considered, ASSD BITE routine will work as planned. Otherwise, flags may indicate a failure of ASSD BITE.

TST stays high for the time equivalent of the maximum filter flush time among the three channels.

For SPI mode the typical BITE activation time is 3.6ms.

If BITE is triggered multiple times (e.g. in case of PSRR failures), the BITE_pass signal will be latched as soon as positive BITE and negative BITE is passed, irrespective of whether positive BITE and negative BITE are passed within the same cycle. (Note: One cycle is defined as one positive BITE / negative BITE sequence)

ASSD error flag starts with 1 after reset unless ASSD monitoring has been disabled or the test is passed

If the ASSD data is within the limits, the flag counter will be reset.

2.8 Extended Device ID

Extended Device ID is used to distinguish among different sensor types, which is programmed in OTP at Address 57dec.

For SMA660, 0x0060hex is implemented as the Extended Device ID, while 0x0065hex is used for SMA665. Extended Device ID is different from Device ID, which can be read out through SPI command RD_Device_ID.

The following example gives a typical sequence with Bosch SPI instructions.

Description	**Command**
1. Go to extended mode by writing the corresponding magic code to Addr. 0x72	DEMAND_EXT_MODE (0x39801EE0hex)
2. Set OTP address to be read by writing 0x38 to Addr. 0x84	WR_OTP_ADDRESS (0x4280070Chex)
3. Wait for 2 µs	Wait for 2 µs
4. Read from address set as 3. By reading Addr. 0x82 twice with a wait time of at least 2µs in between	RD_OTP_DATA (0x41000008hex) Wait 2µs RD_OTP_DATA (0x41000008hex)
5. Extended device ID is stored in Bits 15…8 of read data	

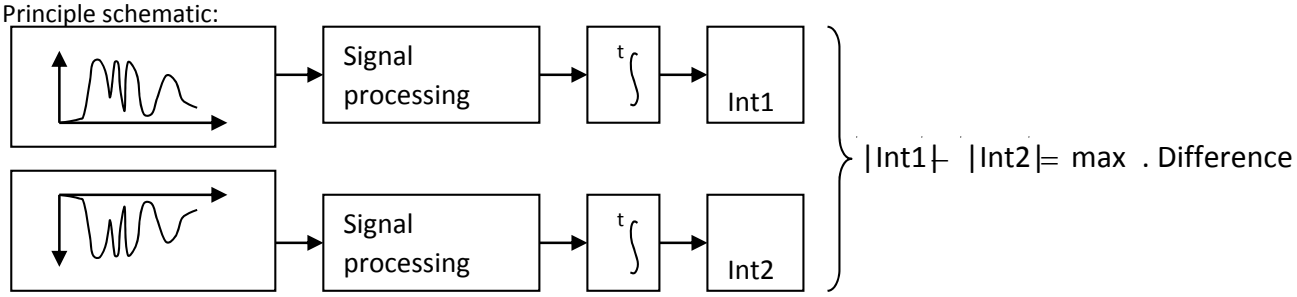
2.9 Symmetry of output signal

By applying a input value with same amplitude but different sign the signal processing of the sensor (including offset regulation, Interpolation etc.) must lead to the same but opposite output value. Integration of the positive or the negative signal must lead to a similar value. This is done by using symmetrical rounding in the complete signal path, whenever the bit width is reduced.

The maximum allowed difference for the digital evaluation path is defined in the following table:

Parameter	Readout sampling per channel [µs]	time [ms]	Type	max	Unit
Maximum difference of the integrated output value for two opposed but similar input values over a defined time with a defined readout sampling rate (Difference = Integral of positive output values + Integral of negative output values)	500	200	0	2	LSB

Principle schematic:



3 OTP

3.1.1 Basic OTP Functionality

OTP (One Time Programmable ROM) is a special type of EPROM which is electrically programmable and UV erasable. A memory cell represents Bit=0 if erased. By applying programming voltage the memory cell gets charged and then permanently represents Bit=1. Memory cells can only be erased again by UV light as long as the device is not finally packaged or packaging is transparent to UV light.

SMA660 includes a 512Bit OTP (64x 8 organizations)

The OTP is divided in 4 banks:

ASIC (0x00-0x0F)	=> wafer level testing
SMA (0x10-0x1F)	=> final testing
ENG (0x20-0x2F)	=> final testing
PAS (0x30-0x3F)	=> customer calibration

Each bank is secured by its own 8-Bit CRC and lock bit. When the lock bit is set, the CRC check over the bank will be activated after bootloading and the register content will be monitored continuously by the CRC (see also chapter OTP CRC Handling).

After power up and the release of the global reset the Bootloader is the first bus master who triggers APB bus transfers for the bootloading process (moving calibration data from OTP memory to the CONFIG_REGS slave). The other APB bus masters are disabled until the bootloading has been done. This can take up to 100us where no access over SPI is possible.

Note that the OTP memory is not directly mapped into the TA660 address space. It can be accessed via a port access scheme located in the OTP_CTRL slave. All OTP data must be transferred into the CONFIG_REGS registers (into MOTP or shadow registers) by the Bootloader before normal operation of the TA660 can start.

The registers realized in OTP_CTRL are essential for OTP memory read or programming access either directly via SPI or indirectly via Bootloader. Further all Bootloader operations and lock bit manipulations are triggered via OTP_CTRL registers.

3.1.2 OTP CRC Handling

Each OTP bank consists of 128 bits, in which 112 CRC-relevant data bits, 8 CRC-bits and 1 lock bit.

The following CRC calculation will be used.

Polynomial = 0x97 (x^8 + x^5 + x^3 + x^2 + x + 1)

Initial value = 0xFF

The Bootloader can be used to program the reference CRC values for each of the four shadow register regions (ASIC, SMA, ENG and PAS). If a Bootloader controlled OPT programming has been triggered (*BL_START_PROG* field in *BOOTLODER_CONTROL register*) by default the source for the CRC values to be programmed will be the calculated CRC values. The calculated CRC values are based on the MOTP shadow registers.

The CRC values stored in the MOTP shadow registers will be used as programming source if the bit of *BL_BYPASS_CALC_CRC field of BOOLOADER_CTRL register has* been set before OTP programming start. Note that after this procedure, the CRC values programmed and boot loaded later, the MOTP shadow register CRC checks during normal operation will always be based on a correct CRC reference. With any other procedure the proper reference CRC values must be calculated externally and stored into the MOTP registers before programming.

If incorrect CRC is calculated a flag over SPI will be sent.

The OTP CRC check procedure performs a full parallel check in each system cycle for all regions (ASIC, SMA, ENG, PAS) to a 16-bit parallel scheme handled by the Bootloader in a sequential and periodical manner. The calculation flow is as follows:

- MOTP CRC checks starts right after bootloading has been performed (boodloading_done) and are enabled if bit OTP_MASK_CRC in register OTP_CONTROL is not set.
- IF MOTP CRC checks are enabled the Bootloader starts an incremental CRC calculation every 280 kHz (trigger based on internal 280 KHz clock) for one MOTP 16-bit data register. The Bootloader will access the MOTP registers and feeds the CRC-calculation module with the value read.
- To get the final MOTP CRC for all four regions 4x8 16-bit calculations are necessary and this takes approximately 114 µsec. Note that the total calculation can be varying slightly because a SPI access can potentially postpone the Bootloader MOTP read access (to guarantee the availability of SPI read data).
- Note that the MOTP CRC checks are disabled if extended mode or extended test mode is active. Additionally MOTP CRC checks are also disabled right between first and second access to registers CFG_SOFTRESET or CFG_EXT_MODE to avoid side effects by internal Bootloader APB bus accesses.

3.1.3 OTP Lockbit Handling

The Bootloader can be used to program the lock bits for each of the four shadow register regions (ASIC, SMA, ENG and PAS). With help of lock bits the following functionality can be used:

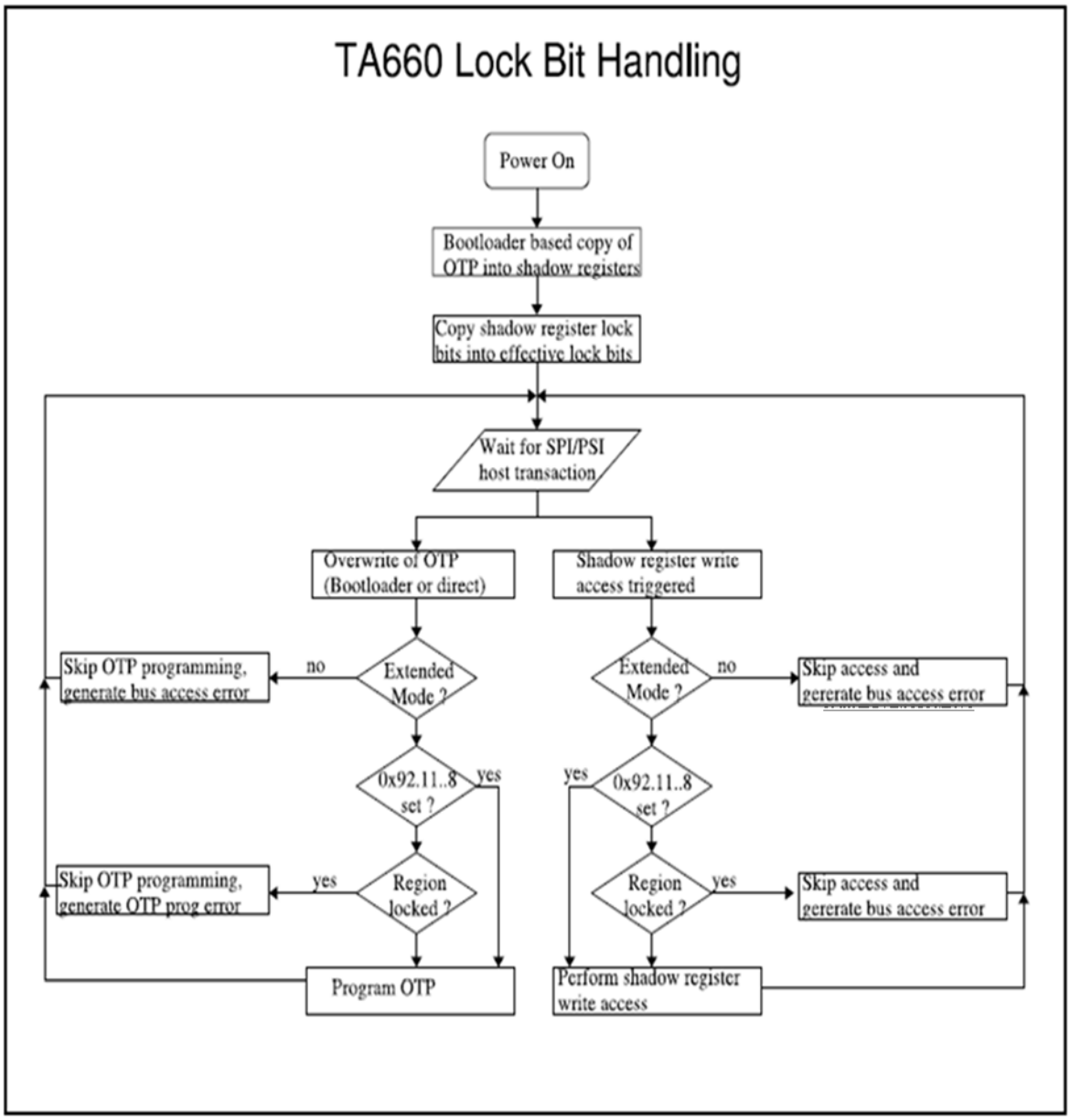
- An active MOTP lockbit will protect the associated OTP region from programming.
- An active MOTP lockbit will write protect the associated MOTP region.

A lockbit can be only activated if it was previously programmed into OTP memory (with one) and transferred by the Bootloader into the corresponding MOTP register. A write instruction directly over SPI to a MOTP lockbit will not activate the protection but can be used for a following Bootloader based OTP programming.

If a Bootloader controlled OPT programming has been triggered (using *BOOTLODER_CONTROL.BL_START_PROG bit*) the MOTP lock bits will always be the source for the lock bits to be programmed.

If the bit *BOOLOADER_CTRL.BL_IGNORE_REGIONS* has been set previously all MOTP lock bits will be reset and zeros will be programmed into OTP.

The following flow chart shows the basic lockbit handling starting with power on.



3.1.4 OTP direct access

The OTP content can be directly accessed over Bosch SPI or Open SPI. See Chapter 4.7(Open SPI) and Chapter 4.8 (Bosch SPI) chapter for details.

3.1.5 OTP Mapping

The following table shows the OTP content of SMA660.

ADDR (HEX)	ADDR (DEC)	Content 7	6	5	4	3	2	1	0	Lock-Bit Region
0	0	SN	SN	SN	SN	SN	SN	SN	SN	
	1	SN	SN	SN	SN	SN	SN	SN	SN	
2	2	SN	SN	SN	SN	SN	SN	SN	SN	
	3	SN	SN	SN	SN	SN	SN	SN	SN	
4	4	SN	SN	SN	SN	SN	SN	SN	SN	
	5	SN	SN	SN	SN	SN	SN	SN	SN	
6	6	VMON_VBG	VMON_VBG	VMON_VBG	VMON_VBG	CALIB_VBG	CALIB_VBG	CALIB_VBG	CALIB_VBG	
	7	VMON_AVDD	VMON_AVDD	VMON_AVDD	CALIB_BIAS	CALIB_BIAS	CALIB_BIAS	CALIB_BIAS	CALIB_BIAS	
8	8	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	
	9			OSC_TC	OSC_TC	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	**CALIB_OSC**	
A	10	CALIB_IPSI	CALIB_IPSI	CALIB_IPSI	CALIB_IPSI	ANAREG_CAL	ANAREG_CAL	DIGREG_CAL	DIGREG_CAL	
	11			VMON_VDD	VMON_VDD	VMON_VDD	VMON_VDDI	VMON_VDDI	VMON_VDDI	
C	12-13									
E	14	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	
	15	LOCK_BIT_ASIC = 1								ASIC
10	16				AXIS_Z = 0	CMA_TYPE = 0	CMA_TYPE = 0	OUT_PSI = 1	OUT_SPI = 0	
	17									
12	18	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	
	19	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	
14	20	RANGE_CTRL = 0	RANGE_CTRL = 0	RANGE_CTRL = 1	RANGE_CTRL = 1	RANGE_CTRL = 0	RANGE_CTRL = 0	RANGE_CTRL = 1	RANGE_CTRL = 0	
	21									
16	22	0	0	0	0	0	0	0	0	
	23	0	0	0	0	0	0	0	0	
18	24	0	0	0	0	0	0	0	0	
	25	0	0	0	0	0	0	0	0	
1A	26	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	BITE_CH1_REF_NEG	
	27	BITE_CH1_REF_POS	BITE_CH1_REF_POS	BITE_CH1_REF_POS	BITE_CH1_REF_POS	BITE_CH1_REF_POS	BITE_CH1_REF_POS	BITE_CH1_REF_POS	BITE_CH1_REF_POS	
1C	28	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	BITE_CH2_REF_NEG	
	29	BITE_CH2_REF_POS	BITE_CH2_REF_POS	BITE_CH2_REF_POS	BITE_CH2_REF_POS	BITE_CH2_REF_POS	BITE_CH2_REF_POS	BITE_CH2_REF_POS	BITE_CH2_REF_POS	
1E	30	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	
	31	LOCK_BIT_SMA = 1								SMA
20	32	UVA_DISABLE = 0	UVSI_DISABLE = 0	UVS_DISABLE = 0	OVA_DISABLE = 0	OVD_DISABLE = 0	OVSI_DISABLE = 0	C_CUT_DISABLE = 0	ASSD_EN = 1	
	33	ASSD_LIMIT	ASSD_LIMIT	ASSD_LIMIT	ASSD_LIMIT	ASSD_LIMIT	ASSD_LIMIT	ASSD_LIMIT	ASSD_LIMIT	
22	34	ASSD_BITE_THR = 0	OSC_MOD = 1	ASSD_FREQ = 1	ASSD_FREQ = 0	OSC_MOD_FREQ = 1	OSC_MOD_FREQ = 0	TM_NOERR = 0	JITTER_OFF = 0	
	35								ASSD_BITE_THR = 1	
24	36		FOC_MEAN = 0	SIGN_CH2 = 1	SIGN_CH1 = 1	BITE_SIGN_CH2 = 0	BITE_SIGN_CH1 = 0	OFS_SOC_DISABLE = 0	OFS_FOC_DISABLE = 0	
	37	GND_ERR_OV_DISABLE = 0	DC_SOFT_SO_EN = 0	ASSD_FLAG_CNT = 0	ASSD_FLAG_CNT = 0	FOC_LIMIT = 0	FOC_LIMIT = 0	FOC_LIMIT = 0	FOC_LIMIT = 0	
26	38-39	REDUNDANT TRIMMING AREA (NOT AVAILABLE FOR CUSTOMER USE)								
28-2C	40-45	REDUNDANT TRIMMING AREA (NOT AVAILABLE FOR CUSTOMER USE)								
2E	46	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	
	47	LOCK_ENG = 1								ENG
30	48	0	0	0	0	0	0	0	0	
	49					0	0	0	0	
32	50	0	0	0	0	0	0	0	0	
	51			0	0	0	0	0	0	
34	52	0	0	0	0	0	0	0	0	
	53	0	0	0	0	0	0	0	0	
36	54	0	0	0	0	0	0	0	0	
	55			0	0	0	0	0	0	
38	56	0	0	0	0	0	0	0	0	
	57	EXT_DEV_ID = 0	EXT_DEV_ID = 1	EXT_DEV_ID = 1	EXT_DEV_ID = 0	EXT_DEV_ID = 0	EXT_DEV_ID = 0	EXT_DEV_ID = 0	EXT_DEV_ID = 0	
3A	58	0	0	0	0	0	0	0	0	
	59				0	0	0	0	0	
3C	60-61									
3E	62	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	
	63	LOCK_BIT_PAS = 1								PAS

3.1.6 Address Map

OTP Mapping Registers:

The OTP content is reflected in the OTP mapping registers which reside in the addresses 0x00 to 0x3e.

Address (HEX)	Bit	Name	Description	Access
0x00		**MOTP_ASIC_SN_0**		
	15...0	MOTP_ASIC_SN_0	ASIC Serial Number 0 to 15	read-write conditional
0x02		**MOTP_ASIC_SN_1**		
	15...0	MOTP_ASIC_SN_1	ASIC Serial Number 16 to 31	read-write conditional
0x04		**MOTP_ASIC_SN_2**		
	15...0	MOTP_ASIC_SN_2	ASIC Serial Number bit 32 to 47	read-write conditional
0x06		**MOTP_CALIB_VBG_BIAS**		
	3...0	MOTP_CALIB_VBG	VBG Calibration Settings	read-write conditional
	7...4	MOTP_VMON_VBG	VBG Monitor Trimming	read-write conditional
	12...8	MOTP_CALIB_BIAS	BIAS Calibration Settings	read-write conditional
	15...13	MOTP_VMON_AVDD	AVDD Monitor Trimming	read-write conditional
0x08		**MOTP_CALIB_OSC**		
	11...0	MOTP_CALIB_OSC	Oscillator calibration settings	read-write conditional
	13...12	MOTP_OSC_TC	Oscillator Temperature Coefficient	read-write conditional
0x0A		**MOTP_CALIB_REG_IPSI**		
	1...0	MOTP_DIGREG_CAL	Calibration for Digital Regulator	read-write conditional
	3...2	MOTP_ANAREG_CAL	Calibration for Analog Regulator	read-write conditional

Address (HEX)	Bit	Name	Description	Access
	7...4	MOTP_CALIB_IPSI	PSI Current Calibration Settings	read-write conditional
	10...8	MOTP_VMON_VDDI	VDDI Monitor Trimming	read-write conditional
	13...11	MOTP_VMON_VDD	VDD Monitor Trimming	read-write conditional
0x0E		**MOTP_CRC_ASIC**		
	7...0	MOTP_CRC_ASIC	CRC for ASIC Bank	read-write conditional
	15	MOTP_LOCK_BIT_ASIC	Lock Bit of ASIC Bank Write once, unlock only in Test Mode	read-write conditional
0x10		**MOTP_CONFIG_SMA**		
	0	MOTP_OUT_SPI	SPI Disable, 0 = SPI on (default); 1 = SPI off	read-write conditional
	1	MOTP_OUT_PSI	PSI Disable, 0= PSI on (default); 1 = PSI off	read-write conditional
	3...2	MOTP_CMA_TYPE	CMA Type: 00 = 100 G; 01 =400 G; 10 = 800 G **Value** **Name** **Description** 0 CMA_100G 100G Sensor Element 1 CMA_400G 400G Sensor Element 2 CMA_800G 800G Sensor Element	read-write conditional
	4	MOTP_AXIS_Z	1 = Z AXIS available	read-write conditional
0x12		**MOTP_SENS**		
	7...0	MOTP_SENS_CH1	Sensitivity settings for Channel 1	read-write conditional

Address (HEX)	Bit	Name	Description	Access
	15...8	MOTP_SENS_CH2	Sensitivity settings for Channel 2	read-write conditional
0x14		**MOTP_RANGE_CTRL**		
	7...0	MOTP_RANGE_CTRL	Range Settings for SOC and FOC	read-write conditional
0x16		**MOTP_BITE_CH1_TOL**		
	7...0	MOTP_BITE_CH1_TOL_LOW	BITE Low-Tolerance for Channel 1	read-write conditional
	15...8	MOTP_BITE_CH1_TOL_UP	BITE Up-Tolerance for Channel 1	read-write conditional
0x18		**MOTP_BITE_CH2_TOL**		
	7...0	MOTP_BITE_CH2_TOL_LOW	BITE Low-Tolerance for Channel 2	read-write conditional
	15...8	MOTP_BITE_CH2_TOL_UP	BITE Up-Tolerance for Channel 2	read-write conditional
0x1A		**MOTP_BITE_CH1_REF**		
	7...0	MOTP_BITE_CH1_REF_NEG	NEG BITE Reference for Channel 1	read-write conditional
	15...8	MOTP_BITE_CH1_REF_POS	POS-BITE Reference for Channel 1	read-write conditional
0x1C		**MOTP_BITE_CH2_REF**		
	7...0	MOTP_BITE_CH2_REF_NEG	NEG BITE Reference for Channel 2	read-write conditional
	15...8	MOTP_BITE_CH2_REF_POS	POS-BITE Reference for Channel 2	read-write conditional
0x1E		**MOTP_CRC_SMA**		
	7...0	MOTP_CRC_SMA	CRC for SMA Bank	read-write conditional

Address (HEX)	Bit	Name	Description	Access
	15	MOTP_LOCK_BIT_SMA	Lock Bit of SMA Bank Write once, unlock only in Test Mode	read-write conditional
0x20		**MOTP_SAFETY**		
	0	MOTP_ASSD_EN	Enable Continuous Monitoring 1 = enable	read-write conditional
	1	MOTP_C_CUT_DISABLE	Disable Start-up C_CUT 1 = disable	read-write conditional
	2	MOTP_OVSI_DISABLE	Disable Over Voltage Supply VDDI 1 = disable	read-write conditional
	3	MOTP_OVD_DISABLE	Disable Over Voltage Digital Supply DVDD 1 = disable	read-write conditional
	4	MOTP_OVA_DISABLE	Disable Over Voltage Analog Supply AVDD 1 = disable	read-write conditional
	5	MOTP_UVS_DISABLE	Disable Under Voltage Detection of VDD 1 = disable	read-write conditional
	6	MOTP_UVSI_DISABLE	Disable Under Voltage Detection of VDDI 1 = disable	read-write conditional
	7	MOTP_UVA_DISABLE	Disable Under Voltage Detection of AVDD 1 = disable	read-write conditional
	15...8	MOTP_ASSD_LIMIT	Continuous Monitoring Limit	read-write conditional
0x22		**MOTP_JITTER**		

Address (HEX)	Bit	Name	Description	Access
	0	MOTP_JITTER_OFF	Jitter On/Off;1 = OFF = Jitter disabled	read-write conditional
	1	MOTP_TM_NOERR	Suppress the PSI error transmission 1 = no error transmission	read-write conditional
	3...2	MOTP_OSC_MOD_FREQ	jitter modulation frequency 00 4kHz 01 3.5kHz 10 2 kHz 11 1 kHz	read-write conditional
	5...4	MOTP_ASSD_FREQ	MOTP_ASSD_FREQ => 3dB frequency of ASSD decimation filter 00: approx. 2.1 kHz 01: approx. 1 kHz 10: approx. 580 Hz 11: approx. 280 Hz	read-write conditional
	6	MOTP_OSC_MOD	0 = +/- 0.424 oscillator frequency variation 1 = +/- 0.823 oscillator frequency variation	read-write conditional
	8...7	MOTP_ASSD_BITE_THR	00 = BITE Threshold OFF 01 = +/- 20% 10 = +/- 40% 11 = BITE Threshold OFF	read-write conditional
0x24		**MOTP_CONFIG_ENG_1**		
	0	MOTP_OFS_FOC_DISABLE	Disable Fast Offset Cancellation 1 = disable	read-write conditional
	1	MOTP_OFS_SOC_DISABLE	Disable Slow Offset Cancellation 1 = disable	read-write conditional
	2	MOTP_BITE_SIGN_CH1	BITE Sign Channel 1 1 = add negative sign to signal	read-write conditional

Address (HEX)	Bit	Name	Description	Access
	3	MOTP_BITE_SIGN_CH2	BITE Sign Channel 2 1 = add negative sign to signal	read-write conditional
	4	MOTP_SIGN_CH1	Sign for Channel 1 1 = add negative sign to signal	read-write conditional
	5	MOTP_SIGN_CH2	SIGN for Channel 2 1 = add negative sign to signal	read-write conditional
	6	MOTP_FOC_MEAN	Evaluate PAS FOC: 0 = Mean Value; 1 = 1 Sample	read-write conditional
	11...8	MOTP_FOC_LIMIT	Fast Offset Cancellation Limit	read-write conditional
	13...12	MOTP_ASSD_FLAG_CNT	ASSD FLG CNT 00 => 1 sample over the threshold leads to flag activation (default) 01 => 2 consecutive samples over the threshold lead to flag activation 10 => 3 consecutive samples over the threshold lead to flag activation 11 => 4 consecutive samples over the threshold lead to flag activation	read-write conditional
	14	MOTP_DC_SOFT_SO_EN	Daisy Chain Soft-Switch Enable 1 = enable	read-write conditional
	15	MOTP_GND_ERR_OV_DISABLE	Disable Ground Overvoltage Detection 1 = disable	read-write conditional
0x2E		**MOTP_CRC_ENG**		
	7...0	MOTP_CRC_ENG	CRC for ENG Bank	read-write conditional
	15	MOTP_LOCK_BIT_ENG	Lock Bit of ENG Bank Write once, unlock only in Test Mode	read-write conditional
0x30		**MOTP_SGB_CODE_CUSTOM**		

Address (HEX)	Bit	Name	Description	Access
	11...0	MOTP_SGB_CODE_CUSTOMER	Sensor Code Customer	read-write conditional
0x32		**MOTP_SGB_MANU_DATE**		
	13...0	MOTP_SGB_MANU_DATE	Sensor Manufacture Date	read-write conditional
0x34		**MOTP_SGB_INFO**		
	1...0	MOTP_SGB_AXIS_CH1	Sensor Axis Channel 1	read-write conditional
	3...2	MOTP_SGB_AXIS_CH2	Sensor Axis Channel 2	read-write conditional
	7...4	MOTP_PAS_GEN	PAS Generation	read-write conditional
	11...8	MOTP_SGB_LINE_NO	Sensor Line No.	read-write conditional
	15...12	MOTP_SGB_LOT_NO	Sensor Lot No.	read-write conditional
0x36		**MOTP_SGB_CODE**		
	7...0	MOTP_MANUFACT_CODE	Manufacture Code	read-write conditional
	13...8	MOTP_SGB_HOUSING_CODE	Sensor Housing Code	read-write conditional
0x38		**MOTP_OSZI_FLTCNT**		
	7...0	MOTP_OSZI_FLTCNT	Oscillator Monitor Limit	read-write conditional
0x3A		**MOTP_CONFIG_PAS**		
	1...0	MOTP_SMA_RANGE	SMA Range	read-write conditional
	7...2	MOTP_PSI_MODE	PSI Mode	read-write conditional

Address (HEX)	Bit	Name	Description	Access
	9...8	MOTP_FILTER_SETTING	Filter Settings: 00 = 426Hz (Default); 01 = 213Hz; 10 = 106Hz; 11 = 53Hz	read-write conditional
	11	MOTP_SAMPLE_TIMING	Sampling Timing: 0 = after 6µs; 1 = before Data Transmission	read-write conditional
	12	MOTP_SO_TRISTATE_EN	Enable SO Pad Tristate	read-write conditional
0x3E		**MOTP_CRC_PAS**		
	7...0	MOTP_CRC_PAS	CRC for PAS Bank	read-write conditional
	15	MOTP_LOCK_BIT_PAS	Lock Bit of PAS Bank Write once, unlock only in Test Mode	read-write conditional

Configuration Registers:

Address	Bit	Name	Description	Access	Reset
0x40		**CFG_SPI_INIT**			**0x0000**
	3...0	CFG_SPI_VOLTAGE	SPI Init Setting: Protocol/Voltage. Secured by CRC	read-write conditional	0x0
	4	CFG_SPI_PROTOCOL	Read only. Set automatically by first SPI Protocol Command after Reset. Indicating Bosch SPI ('0') or Open SPI ('1'). Secured by CRC	read-only	0x0
	15...8	CFG_CRC	CRC checksum for all the safety-related registers	read-only	0x0
0x42		**CFG_DEV_ID**			**0x0066**
	15...0	CFG_DEV_ID	Device ID	read-only	0x66
0x44		**CFG_REV_ID**			
	3...0	CFG_MSR	Metal Fix Revision	read-only	

Address	Bit	Name	Description	Access	Reset
	7...4	CFG_SWR	Full Mask Revision	read-only	
0x46		**CFG_SID**			**0x0041**
	4...0	CFG_SID1	Safety ID1	read-write conditional	0x1
	9...5	CFG_SID2	Safety ID2	read-write conditional	0x2
0x48		**CFG_DATA_ACC_CH1**			
	11...0	CFG_DATA_ACC_CH1	ACC data channel 1	read-only	
0x4A		**CFG_DATA_ACC_CH2**			
	11...0	CFG_DATA_ACC_CH2	Acc Data Channel 2	read-only	
0x4C		**CFG_DATA_ACC_CH2_CAPT**	**Channel 2 Data is captured when the channel 1 is read**		
	11...0	CFG_DATA_ACC_CH2_CAPT	Sensor Data Channel 2 Captured	read-only	
0x4E		**CFG_DATA_ASSD**			
	15...0	CFG_DATA_ASSD	ASSD Data	read-only	
0x50		**CFG_DATA_ASSD_CAPT**			
	15...0	CFG_DATA_ASSD_CAPT	ASSD Data captured	read-only	
0x52		**CFG_OFS_CH1**			
	15...0	CFG_OFS_CH1	Raw Offset channel 1	read-only	
0x54		**CFG_OFS_CH2**			
	15...0	CFG_OFS_CH2	Raw Offset Channel 2	read-only	
0x56		**CFG_OFS_ASSD**			
	15...0	CFG_OFS_ASSD	Raw Offset Channel ASSD	read-only	
0x58		**CFG_OFFSET_CONFIG**			**0x0000**
	1...0	CFG_OC_CH1	Settings for offset cancellation channel 1 0: offset cancellation channel 1 switched	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
			off (default) 1: 1LSB/s slow offset cancellation channel 1 switched on 2: 1LSB/21s slow offset cancellation channel 1 switched on 3: fast offset cancellation channel 1 switched on secured by CRC		
	4...2	CFG_OC_LENGTH_CH1	2^n offset cancellation steps 0 (000): 64 samples (Default) 1 (001): 128 samples 2 (010): 256 samples 3 (011): 512 samples 4 (100): 1024 samples 5-7 (101,110,111): 64 samples (default) (in Open SPI RE flag) secured by CRC	read-write conditional	0x0
	6...5	CFG_OC_CH2	Settings for offset cancellation channel 2 0: offset cancellation channel 2 switched off (default) 1: 1LSB/s slow offset cancellation channel 2 switched on 2: 1LSB/21s slow offset cancellation channel 2 switched on 3: fast offset cancellation channel 2 switched on secured by CRC	read-write conditional	0x0
	9...7	CFG_OC_LENGTH_CH2	2^n offset cancellation steps 0 (000): 64 samples (Default) 1 (001): 128 samples 2 (010): 256 samples 3 (011): 512 samples 4 (100): 1024 samples 5-7 (101,110,111): 64 samples (default) (in Open SPI RE flag) secured by CRC	read-write conditional	0x0
	11...10	CFG_OC_ASSD	Settings for offset cancellation channel ASSD secured by CRC	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
			Value Name Description 0 OC_OFF offset cancellation channel ASSD switched off (default) 1 OC_SLOW slow offset cancellation channel ASSD switched on 3 OC_FAST fast offset cancellation channel ASSD switched on		
0x5A		**CFG_CLK_CNT**			**0x0000**
	15...0	CFG_CLK_CNT	Clock Counter 16 bits	read-only	0x0
0x5C		**CFG_CLK_CNT_MIN**			**0x0000**
	15...0	CFG_CLK_CNT_LIMIT_MIN	Clock Counter Limit Min	read-write conditional	0x0
0x5E		**CFG_CLK_CNT_MAX**			**0xFFFF**
	15...0	CFG_CLK_CNT_LIMIT_MAX	Clock Counter Limit Max	read-write conditional	0xffff
0x60		**CFG_CLK_CNT_FLTCNT**			**0x00FF**
	7...0	CFG_CLK_CNT_FLTCNT	Clock Counter Fault Threshold	read-write conditional	0xff
0x62		**CFG_SBITE_MODE**			**0x0000**
	1...0	CFG_TMD1	BITE Test Mode Ch1 **Value Name Description** 0 CH1_OFF BITE off (default) 1 CH1_NEG neg. BITE for channel 1 2 CH1_POS pos. BITE for channel 1	read-write conditional	0x0
	3...2	CFG_TMD2	BITE Test Mode Ch2	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
			Value Name Description 0 CH2_OFF BITE off (default) 1 CH2_NEG neg. BITE for channel 2 2 CH2_POS pos. BITE for channel 2		
	5...4	CFG_TMDASSD	BITE Test Mode Channel ASSD **Value Name Description** 0 ASSD_OFF BITE off (default) 1 ASSD_NEG neg. BITE for channel ASSD 2 ASSD_POS pos. BITE for channel ASSD	read-write conditional	0x0
0x64		**CFG_MONITOR_FLAG_1**			**0x0000**
	0	CFG_F_OC1	Offset Cancellation Channel 1 out of limit	read-only	0x0
	1	CFG_F_OC2	Offset Cancellation Channel 2 out of limit	read-only	0x0
	4	CFG_F_NOCLK	clock of on-chip oscillator is absent	read-only	0x0
	5	CFG_F_OSC	oscillator frequency out of range	read-only	0x0
	6	CFG_F_OTP	OTP check error, CRC Error.	read-only	0x0
	7	CFG_F_LOCK	OTP lock bit not set (including all lock bits)	read-only	0x0
	9	CFG_F_EXTM	Ext Mode: extended mode for production relevant tests (fault grade Coverage mode).	read-only	0x0
	10	CFG_F_SOC1_INACTIVE	SOC for channel 1 not active	read-only	0x0
	11	CFG_F_SOC2_INACTIVE	SOC for channel 2 not active	read-only	0x0

Address	Bit	Name	Description	Access	Reset
	12	CFG_F_CCUT	C_Cut Function Triggered	read-only	0x0
	13	CFG_ASSD_ERR	ASSD error	read-only	0x0
	14	CFG_F_ME	Mirror Error (Memory Error in Open SPI)	read-only	0x0
0x66		**CFG_MONITOR_FLAG_2**			**0x0000**
	0	CFG_F_EOP	end of programming	read-only	0x0
	1	CFG_F_UVS	Low Voltage Detected at VDD	read-only	0x0
	2	CFG_F_UVSI	Low Voltage Detected at VDDI	read-only	0x0
	3	CFG_F_UVA	Low Voltage Detected at AVDD	read-only	0x0
	4	CFG_F_GND_ERR	GND loss detected	read-only	0x0
	5	CFG_F_OCASSD	Offset Cancellation Channel ASSD out of limit	read-only	0x0
	8	CFG_FOC_BUSY_CH1	Channel 1 Fast Offset Busy	read-only	0x0
	9	CFG_FOC_BUSY_CH2	Channel 2 Fast Offset Busy	read-only	0x0
	10	CFG_FOC_BUSY_ASSD	Offset Cancellation Channel ASSD busy	read-only	0x0
0x68		**CFG_CONFIG_1**			**0x0010**
	1...0	CFG_FILTER_CH1	Filter Settings for Ch1: 00 = 426Hz (Default) 01 = 213Hz 10 = 106Hz 11 = 53H Secured by CRC	read-write conditional	0x0
	3...2	CFG_FILTER_CH2	Filter settings for CH2. 00 = 426Hz (Default) 01 = 213Hz 10 = 106Hz 11 = 53H Secured by CRC	read-write conditional	0x0
	4	CFG_ASSD_EN	ASSD Enable Secured by CRC	read-write conditional	0x1

Address	Bit	Name	Description	Access	Reset
	5	CFG_C_CUT_TRIGGER	Triggers C_Cut_START Detection (automatically cleared)	read-write conditional	0x0
	7...6	CFG_OSCM	OSC Monitoring Mode **Value Name Description** 0 MODE1 00 = clock counter running and readable, disable clock counter register and oscillator monitoring flag (default) 1 MODE2 01 = enable clock counter register, disable oscillator monitoring flag 3 MODE3 11 = enable clock counter register and oscillator monitoring flag	read-write conditional	0x0
0x6A		**CFG_CONFIG_2**			**0x0300**
	7...0	CFG_ARMING_TH	Arming threshold Secured by CRC	read-write conditional	0x0
	9...8	CFG_ARMING_SAMPLE_CNT	counter for number of arming samples + 1	read-write conditional	0x3
0x6E		**CFG_SOFTRESET**			**0x0000**
	7...0	CFG_SOFTRESET	Soft Reset is triggered by 2xwriting this address	read-write	0x0
0x70		**CFG_EOP_EN**			**0x0000**
	0	CFG_EOP_EN	locking bit, after EOP_EN=1 only read commands allowed, also DEMAND_SOFT_RESET	read-write conditional	0x0
0x72		**CFG_EXT_MODE**			**0x0000**
	0	CFG_EXT_M	Activate Extended Mode	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
	7...1	CFG_MAGIC_CODE_7B	Magic Code 7B to enter Extended Mode	read-write conditional	0x0
	8	CFG_EXT_TM	Activate Extended Test Mode	read-write conditional	0x0
	15...9	CFG_MAGIC_CODE_5C	Magic Code 5C to enter Extended TEST Mode	read-write conditional	0x0
0x74		**CFG_TEST_CONFIG1**			**0x0000**
	0	CFG_PD_SD	combined power down for all 3 Frontend	read-write conditional	0x0
	1	CFG_PD_SGND	power down signal ground	read-write conditional	0x0
	2	CFG_PD_OSC	power down oscillator	read-write conditional	0x0
	3	CFG_PD_PSI	power down PSI-Interface	read-write conditional	0x0
	4	CFG_PD_REG_BITE	power down BITE regulator	read-write conditional	0x0
	5	CFG_PD_BG	power down Bandgap	read-write conditional	0x0
	6	CFG_PD_BG_MON	power down Monitor Bandgap	read-write conditional	0x0
	7	CFG_PD_IREF	power down current reference	read-write conditional	0x0
	8	CFG_PD_PREREG	power down pre-regulator	read-write conditional	0x0
	9	CFG_PD_AVDD	power down analog-regulator (AVDD)	read-write conditional	0x0
	10	CFG_PD_DVDD	power down digital-regulator (DVDD)	read-write conditional	0x0
	11	CFG_PD_GNDBREAK	power down ground breakdown detection	read-write conditional	0x0
	12	CFG_PD_POR18	power down POR-1.8V	read-write conditional	0x0
	13	CFG_PD_POR33	power down POR 3.3V	read-write conditional	0x0
	14	CFG_PD_VMON_3V3_VDDI	power down voltage monitor at VDDI	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
	15	CFG_PD_VMON_PREREG	power down voltage monitor at VDD	read-write conditional	0x0
0x76		**CFG_TEST_CONFIG2**			**0x0000**
	0	CFG_PD_VMON_1V8_AVDD	Power down voltage monitor at AVDD	read-write conditional	0x0
	1	CFG_PD_VMON_1V8_DVDD	power down voltage monitor at DVDD	read-write conditional	0x0
	3...2	CFG_TMSD_CH1	TMSD Channel 1	read-write conditional	0x0
	5...4	CFG_TMSD_CH2	TMSD Channel 2	read-write conditional	0x0
	11...8	CFG_TMUX_ATEST	Configure analog test Mux, 0000 = No Internal Signal multiplexed on ANATEST_EWS or SO pin	read-write conditional	0x0
	12	CFG_TMUX_ATEST_EN	Enable analog test MUXon SO pin	read-write conditional	0x0
0x78		**CFG_TEST_CONFIG3**			**0x0000**
	1	CFG_PAS2ONE	Enable PAS2ONE test	read-write conditional	0x0
	2	CFG_PAS2ZERO	Enable PAS2ZERO test	read-write conditional	0x0
	3	CFG_PSI_EN_IPOL	Enable IPOL	read-write conditional	0x0
	4	CFG_TM_CM_SW	CM Switch	read-write conditional	0x0
	5	CFG_SO_TSTOUT_EN	enable digital test-output at SO (1= MUX signal selected by CFG_TMUX_DTEST_SO to SO, 0 = normal SO function)	read-write conditional	0x0
	10...6	CFG_TMUX_DTEST_SO	configure digital test MUX	read-write conditional	0x0
	14...11	CFG_MASK_FLAGS	Mask voltage Monitor flags, POR-flags, GND-break flag. Combination b#1111 masks all flags, other combinations mask only 1 specific flag	read-write conditional	0x0
	15	CFG_EWS_START_PSI	enable start_psi	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
0x7A		**CFG_MONITOR_DATA**			**0x0000**
	15...0	CFG_MON_DATA	Signal Path Output Monitor Port controlled by register CFG_MONITOR_DATA_MUX	read-only	0x0
0x7C		**CFG_TEST_CONFIG4**			**0x0000**
	2...0	CFG_MON_DATA_MUX	Multiplexor Control for Monitor Data Register: 000 : Decimation output channel 1 001 : Decimation output channel 2 010 : Decimation output ASSD 011 : FIR output channel 1 100 : FIR output channel 2	read-write conditional	0x0
	3	OSC_CLKOFF	Switch off OSC clock generation in analog	read-write conditional	0x0
	4	OSC_TESTVREFD	Enable DAC-Output of oscillator	read-write conditional	0x0
	5	OSC_CHOPDISABLE	Disable OSC chopper	read-write conditional	0x0
	6	SCREEN_PSI	enable PSI screening	read-write conditional	0x0
	7	ICOMP_EN	MUX I_{comp} from PSI to ANATEST	read-write conditional	0x0
	8	SCREEN_PREREG	screen pre-regulator	read-write conditional	0x0
	9	TST_VBOXLO	VBOX Low Test for POR18	read-write conditional	0x0
	10	PU_DISABLE	Pull-Up disable for CSB, SCK, SI	read-write conditional	0x0
	15...11	CFG_TMUX_DTEST_EWS	TMUX for Digital Test EWS	read-write conditional	0x0
0x7E		**CFG_TEST_CONFIG5**			**0x0000**
	0	CFG_PSI_SM_EN	Activate service mode	read-write conditional	0x0
	1	CFG_PSI_SM_88KHZ_CH1	Activate service mode 8.8kHz for channel 1	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
	2	CFG_PSI_SM_88KHZ_CH2	Activate service mode 8.8kHz for channel 2	read-write conditional	0x0
	3	CFG_PSI_SM_44KHZ_CH1	Activate service mode 4.4kHz for channel 1	read-write conditional	0x0
	4	CFG_PSI_SM_44KHZ_CH2	Activate service mode 4.4kHz for channel 2	read-write conditional	0x0
	5	CFG_PSI_TRIGGER_MULTI_READ	Trigger PSI Multi-read transfer if '1' (will be automatically reset internally after multi read done)	read-write conditional	0x0
	6	CFG_PSI_SLOW_EN	activates slow service mode (only possible if service mode is still inactive)	read-write conditional	0x0

OTP-Control-Registers:

Address	Bit	Name	Description	Access	Reset
0x80		**OTP_WRITE_DATA**			**0x0000**
	15...0	OTP_WDATA	write data for OTP programming access (programming based on OTP_SADDR will be triggered with write to this register)	read-write conditional	0x0
0x82		**OTP_READ_DATA**			**0x0000**
	15...0	OTP_RDATA	OTP read data (OTP read based on OTP_SADDR will be triggered with read access to this register, OTP data will be available in a second read after OTP_BUSY_RD is zero)	read-only conditional	0x0
0x84		**OTP_ADDRESS**			**0x0000**
	5...0	OTP_SADDR	Start address for OTP read/program access	read-write conditional	0x0
0x86		**OTP_CONTROL**			**0x0007**
	0	OTP_LOW_BYTE_EN	low byte will be programmed during OTP program access if '1'	read-write conditional	0x1

Address	Bit	Name	Description	Access	Reset
	1	OTP_HIGH_BYTE_EN	high byte will be programmed during OTP program access if '1'	read-write conditional	0x1
	2	OTP_PROG_EN	OTP programming access allowed if '1'	read-write conditional	0x1
	3	OTP_MASK_CRC	mask OTP CRC failure status if '1'	read-write conditional	0x0
	4	OTP_VPROG_ENA	Explicit setting of VPROG_ENA if '1'	read-write conditional	0x0
0x88		**OTP_MARGIN_CONTROL**			**0x0000**
	0	OTP_IREF_TEST	IREF test on if '1'	read-write conditional	0x0
	1	OTP_MARGIN_PWD_B	IREF external mode enabled if '1'	read-write conditional	0x0
	4...2	OTP_MARGIN_READ_MODE	Margin read mode configuration bits (2:0)	read-write conditional	0x0
	5	OTP_ALL_WL_ON	All 'wordline on' enabled if '1'	read-write conditional	0x0
	6	OTP_ALL_WL_OFF	All 'wordline off' enabled if '1'	read-write conditional	0x0
	15...8	OTP_MARGIN_SEL	Margin module I-DAC control bits (7:0)	read-write conditional	0x0
0x8A		**OTP_STATUS**			**0x0000**
	0	OTP_BUSY_RD	Status: ongoing OTP read access if '1'	read-only	0x0
	1	OTP_BUSY_WR	Status: ongoing OTP programming access if '1'	read-only	0x0
	2	OTP_PROG_ERR	Status: OTP programming access failed if '1' (locked region or programming not allowed due to OTP_PROG_EN=0 or VPROG is not ok) This flag will be reset with a new programming trigger (write to OTP_WDATA)	read-only	0x0

Address	Bit	Name	Description	Access	Reset
	3	OTP_WRITE_ERR	Status: OTP program access triggered while OTP busy if '1'	read-only	0x0
	4	OTP_READ_ERR	Status: OTP read access triggered while OTP busy if '1'	read-only	0x0
	5	BL_BUSY	Status: ongoing Bootloader transaction if '1'	read-only	0x0
	6	BL_READ_DONE	Status: Bootloader transfer from OTP to shadow registers done, if '1'	read-only	0x0
	7	MOTP_CRC_ASIC_ERR	CRC status of ASIC region, failure if bit is set	read-only	0x0
	8	MOTP_CRC_SMA_ERR	CRC status of SMA region, failure if bit is set	read-only	0x0
	9	MOTP_CRC_ENG_ERR	CRC status of ENG region, failure if bit is set	read-only	0x0
	10	MOTP_CRC_PAS_ERR	CRC status of PAS region, failure if bit is set	read-only	0x0
0x8C		**OTP_TIMING1**			**0x0601**
	3...0	TWHC_READ	OTP_EN pulse read high time (in system cycles+1)	read-write conditional	0x1
	7...4	TWLC_READ	OTP_EN pulse read low time (in system cycles+1)	read-write conditional	0x0
	11...8	TWLC_PROG	OTP_EN pulse low time for prog (in system cycles+1)	read-write conditional	0x6
	15...12	TSU_PROG	PROG setup before OTP_EN (in system cycles+1)	read-write conditional	0x0
0x8E		**OTP_TIMING2**			**0x0708**
	15...0	TWHC_PROG	OTP_EN pulse high time for prog (in system cycles+1)	read-write conditional	0x708
0x90		**BOOTLOADER_ADDRESS**			**0x3E00**
	5...0	BL_SADDR	Start address for bootloading read/program access	read-write conditional	0x0

Address	Bit	Name	Description	Access	Reset
	13...8	BL_EADDR	End address for bootloading read/program access	read-write conditional	0x3e
0x92		**BOOTLOADER_CONTROL**			**0x0000**
	0	BL_START_PROG	Start Bootloader controlled OTP programming if '1'	read-write conditional	0x0
	1	BL_START_READ	Start Bootloader controlled OTP transfer into shadow registers if '1'	read-write conditional	0x0
	2	BL_MOTP_CALC_CRC	Recalculate MOTP CRC entries if '1' (based on shadow register contents)	read-write conditional	0x0
	11...8	BL_IGNORE_REGIONS	ignore corresponding lockbit regions during OTP program access if '1'	read-write conditional	0x0
	12	BL_BYPASS_CALC_CRC	Bypass programming of calculated CRC if '1' (use shadow register CRC)	read-write conditional	0x0

3.1.7 Access Restrictions

Normal Mode

MOTP (0x00 - 0x3e)	r (no access if EOP_EN01)
CFG (0x40 - 0x72)	r/w (r if EOP_EN=1, except 0x6e Soft Reset)
CFG (0x74 - 0x7e)	no access
OTP-CTRL (0x80 - 0x92)	no access

Extended Mode

MOTP (0x00 - 0x3e)	r/w
CFG (0x40 - 0x72)	r/w
CFG (0x74 - 0x7e)	r
OTP-CTRL (0x80 - 0x92)	r/w

3.2 Configuration Registers

3.2.1 Safety-Relevant-Configuration-Registers

The configuration registers can be configured by SPI.

To make sure the safety related data in the configuration registers are not corrupt during operation, they are secured by CRC.

The CRC-checksum is stored in 'CFG_CRC'.

The CRC will be updated if any of the safety related data is re-configured via SPI.

An error flag 'CFG_F_ME' / ME-Flag is set if the CRC check of the safety related configuration registers fails.

List of configuration data secured by CRC

CFG_SPI_VOLTAGE

CFG_SPI_PROTOCOL

CFG_OC_CH1

CFG_OC_LENGTH_CH1

CFG_OC_CH2

CFG_OC_LENGTH_CH2

CFG_OC_ASSD

CFG_FILTER_CH1

CFG_FILTER_CH2

CFG_ARMING_TH

CFG_ARMING_SAMPLE_CNT

CFG_ASSD_EN

CRC-Parameters

31 CRC-relevant data bits

8 CRC-bits

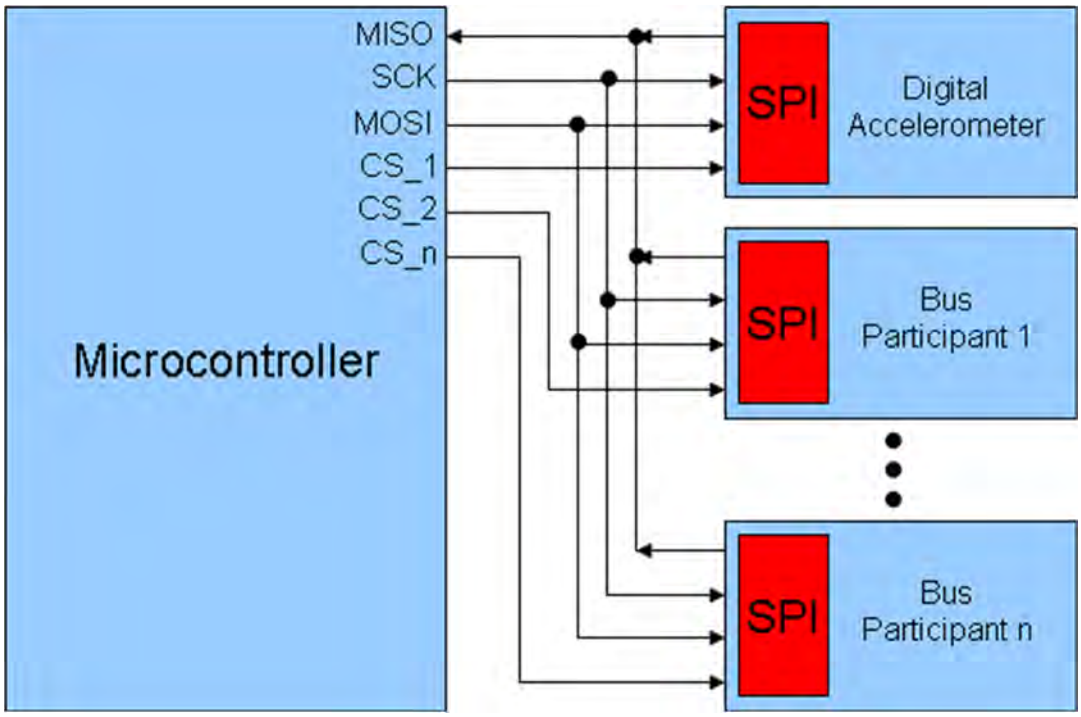
Polynomial = 0x97 (x^8 + x^5 + x^3 + x^2 + x + 1)

Initial value = 0xFF

4 Communication Interface

4.1 Hardware Layer

The SMA660 provides a bi-directional 3.3V/5V serial peripheral interface (SPI) for communication with the ECU via a 32 bit data word size. The sensor always operates in slave mode whereas the microcontroller unit (MCU) provides the master function. The interface consists of 4 ports as shown below:



Serial clock (SCK): Input for master clock signal. This clock determines the speed of data transfer and all receiving and sending is done synchronous to this clock.

Chip Select (CSB): CSB activates the SPI interface. As long as CSB is high, the IC does not accept the clock signal or data and the output SO is in high impedance. Whenever CSB is in a low logic state, data can be transferred form the microcontroller and vice versa.

Serial Input (MOSI): Data input is latched synchronized by SCK clock.

Serial Output (MISO): Data output is set synchronized by SCK clock.

4.2 SPI Protocol

It is possible to choose between two SPI protocols, the Open SPI protocol, see chapter 4.7, and the Bosch SPI protocol, see chapter 4.8.

The Bosch SPI protocol is an in-frame protocol whereas the Open SPI protocol is an off-frame protocol. The selection is carried out via a SPI command, see chapter 4.3.1.

Any “-“in MOSI corresponds to a “don’t-care-bit”, i.e. it can be arbitrary chosen without any effect on the sensor. In MISO it corresponds to high impendency SO status.

4.3 Power-on Phase to normal Operation

4.3.1 Selection of SPI

After release of the automatic power-on reset circuit, the SPI protocol (either Bosch or Open SPI) is selected by an initial SPI command sent by the master. Two SPI SI registers are listening to MO (master out): One SI register 'MOSI1' operating in Open SPI mode, the other SI register 'MOSI2' in RB SPI mode. For each protocol, the selection command is defined as described in the following.

Sensor resumes in Open SPI mode and deactivates the MOSI2 register only after receiving:

PROT_SEL: protocol selection to switch between Bosch SPI X"FF00FF00" and Open SPI X"00FF00FF"																															
SI	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Sensor resumes in RB SPI mode and deactivates the MOSI1 register only after receiving:

PROT_SEL: protocol selection to switch between Bosch SPI X"FF00FF00" and Open SPI X"00FF00FF"																															
SI	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

The sensor resumes its operation in Open SPI mode only upon receiving the Open SPI selection key in the Open SPI SI register. This ensures that by the Open SPI key cannot be interpreted as RB SPI key by the RB SPI SI register.

Immediately after SPI selection the sensor is waiting for the voltage mode selection. Every other command will be ignored (SO stays on high impedance state)

The selected protocol can only be changed after a hard reset.

4.3.2 Voltage mode selection

The SMA660 supports different voltage modes (voltages of sensor supply and SPI). Voltage mode selection command has to be sent as second command after protocol selection. SO pin stays high impedance until the voltage mode is selected.

The selected mode can only be changed after a hard reset.

Available modes are:

- 0010: Supply = 6.7V; SPI = 3.3V
- 0100: Supply = 5V; SPI = 5V
- 1000: Supply = 3.3V; SPI = 3.3V

Remark: The 6.7 V mode should not to be used in Open SPI for safety relevant application without explicit handling of GND pin loss behaviour in algorithm (monitor detection efficiency of ~5% per CSB low phase).

4.3.3 Test Phase

Offset cancellation:

- The command Demand_Offset_Cancelation is only accepted before EOP.
- The FOC has to be actively triggered by SPI Command.
- Retriggering of FOC is possible. After FOC is finished the fields OFF1 and OFF2 (DEMAND_OFFSET_CANCELLATION) must be reset to 0 explicitly before restarting FOC. There is no automatically reset implemented for OFF1 and OFF2.
- If SOC is needed it must be triggered manually before EOP.

- If SOC is triggered, the number of samples (OC length1 & 2) must be kept the same as in previous FOC command. OC length 1 & 2 shall only be changed in combination with retriggering of FOC (otherwise consequence would be an offset jump)
- FOC and SOC are not possible at the same time.
- Deactivation of SOC and triggering of FOC is possible within the same command.
- FOC cannot be deactivated manually.
- FOC cannot be triggered during active selftest

(Default = FOC/SOC deactivated; OC-length 64 steps)

Self test:

- The initial self test value is saved in the OTP at Robert Bosch end-of-line and can be read with the “RD_BITE” commands.
- It is possible to set the self test setup for both channels simultaneously
- FOC and SOC shall be deactivated before triggering self test.
- Self test cannot be activated during active SOC or FOC

(Default = self test deactivated)

4.3.4 Configuration

Automatic system clock monitoring:

- This feature can be configured by setting the OSCM-field in the config1 register with the “WR_CONFIG_1” command
  - “00” = clock counter is reset with an overflow; OSC-flag is deactivated
  - “01” = clock counter is active → Clock counter value is latched and clock counter is reset after each RD_SENSOR_DATA_CH1 request; OSC-flag is deactivated
  - “11” = clock counter is active → Clock counter value is latched and clock counter is reset after each RD_SENSOR_DATA_CH1 request; OSC-flag is activated

    (Default = “00”)
- The number of clock failures detected in row that are necessary to get a clock counter error can be set with the “WR_CLOCK_COUNTER_FLTCNT” command

  (Default = 255)
- Set the maximum and minimum value of the clock counter with the “WR_CLOCK_COUNTER_MAX” and the “WR_CLOCK_COUNTER_MIN” command → considering the maximum and minimum time between two “RD_SENSOR_DATA_CH1” requests and the tolerance of the clock counter

  (Default “WR_CLOCK_COUNTER_MAX” = max value;
  default “WR_CLOCK_COUNTER_MIN” = min value)

Initial C-loss detection:

- The initial C-loss detection can be activated with the “WR_CONFIG_1” command (default = switched off).

  In order to detect the loss of the VDDI capacitor, the discharging behaviour of the capacitor is monitored: If the capacitor is present, discharging will be slowly, whereas an absent capacitor causes a quick voltage drop. For this the VDDI regulator output is switched off and the VDDI capacitor will discharge. If a C-loss is detected the sensor goes to a reset.

Please note, that the C-loss detection only works for the 5V & 6.7V mode (not 3.3V mode).

Arming pin configuration:

- The arming pin can be activated with the “WR_CONFIG_2” command by setting a non-zero Arming threshold (default = 0 → switched off).
- The sample threshold can be set by “Sample Threshold” bits (default = 0 → one sample above threshold triggers Arming pin with next read sensor data command).

FIR Filter configuration:

The FIR filter 3-db frequency is programmed per default at 426 Hz. It can be also selected as 213Hz, 107 Hz or 53 Hz. For selection of FIR filter frequency see command “WR_CONFIG_1” in section 4.7.5.23(Open SPI) and 4.8.5.26 (Bosch SPI).

All other parameters are only guaranteed for the FIR Filter setting of 426 Hz.

4.3.5 Switch to normal operation

After the “END_OF_PROG” command has been sent to the SMA, only read access to the configuration and test registers is possible. The only allowed write access is the “DEMAND_SOFT_RESET” command.

	before protocol selection		before SPI voltage selection		before EOP		after EOP	
Command	**Read**	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**	**Write**
PROT_SEL	×	✓	×	×	×	×	×	×
PROG_MODE	×	×	×	✓	×	×	×	×
RD_MODE	×	×	×	×	✓	×	✓	×
RD_DEVICE_ID	×	×	×	×	✓	×	✓	×
RD_REVISION_ID	×	×	×	×	✓	×	✓	×
SENSOR_DATA	×	×	×	×	✓	×	✓	×
SID (only Bosch SPI)	×	×	×	×	✓	✓	✓	×
OFFSET_REG	×	×	×	×	✓	×	✓	×
OFFSET_CANCELLATION	×	×	×	×	✓	✓	✓	×
CLOCK_COUNTER	×	×	×	×	✓	×	✓	×
CLOCK_COUNTER_MIN	×	×	×	×	✓	✓	✓	×
CLOCK_COUNTER_MAX	×	×	×	×	✓	✓	✓	×
CLOCK_COUNTER_FLTCNT	×	×	×	×	✓	✓	✓	×
SELFTEST	×	×	×	×	✓	✓	✓	×
MONITOR_DATA	×	×	×	×	✓	×	✓	×
CONFIG_1	×	×	×	×	✓	✓	✓	×
CONFIG_2	×	×	×	×	✓	✓	✓	×
DEMAND_SOFT_RESET	×	×	×	×	×	✓	×	✓

END_OF_PROG	×	×	×	×	×	✓	×	×
RD_BITE	×	×	×	×	✓	×	✓/×*	×
RD_SERIAL	×	×	×	×	✓	×	✓/×*	×

*: Read not possible for Open SPI. Possible at Bosch SPI

Application hint for initialization phase:

1. SPI protocol selection
2. Voltage mode selection
3. Reading monitor register
4. Reading Device ID
5. Reading 48 bit serial number
6. Trigger fast offset cancellation (Ch1 / Ch2 / ASSD)
7. Trigger C-loss detection
8. Check oscillator frequency
9. Activate and evaluate selftest (Ch1 / Ch2 / ASSD)
10. Setup the sensor (slow offset cancellation (Ch1 / Ch2 / ASSD), Arming pin)
11. EOP
12. Normal operation (demand acceleration values)

Proper function of the sensor in the overall system must be validated by the customer.

4.4 Soft Reset

To release a Soft Reset, the “DEMAND_SOFT_RESET” command must be executed twice consecutively with no other command in between (except reading CFG_SOFTRESET itself or commands with wrong CRC or wrong bit length as there are no Bus access with such commands). If the command was sent only once or any other valid command is sent in between, no reset will be triggered and the internal counter is set to 0. After a soft reset it is recommended to perform a new initialization phase starting at number 3 (Reading monitor register).

After Soft Reset, approximately 100us should be waited before SPI communication starts working correctly (for generation of correct Status Flag).

For OPEN SPI a stabilization period of 4ms after Soft-Reset should be waited. If during the stabilization period a non-acceleration command is sent then the system responds with ‘zero’ as response with RE-flag set. For acceleration commands the ND-flag will be set.

Note: After soft reset all the registers are set to default except for the protocol selection and voltage mode selection.

4.5 Activation of Extended Mode

The Extended Mode is active after writing the specific magic code (0x7Bhex) to the field CFG_MAGIC_CODE_7B and setting CFG_EXT_M=1 in register CFG_EXT_MODE. After Extended Mode is activated, the following addresses could be accessed.

MOTP (0x00 - 0x3e)

CFG (0x40 - 0x72)

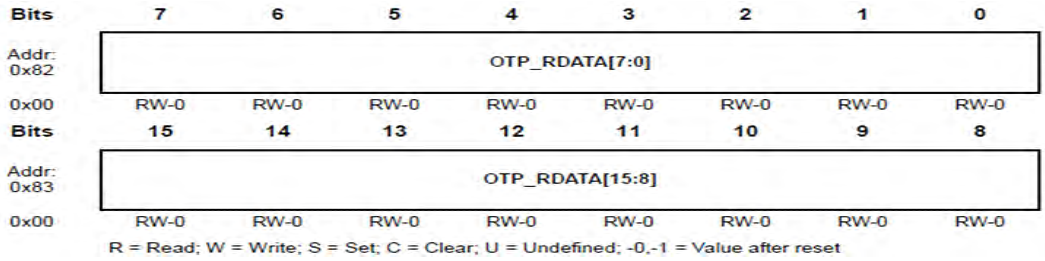
CFG (0x74 - 0x7e)

OTP-CTRL (0x80 - 0x92)

The Extended Mode can be left by resetting CFG_EXT_M to 0.

For customers only the Register OTP_READ_DATA (0X82) and the Register OTP_ADDRESS (0X84) are relevant.

4.5.1 Register OTP_READ_DATA (0x82)

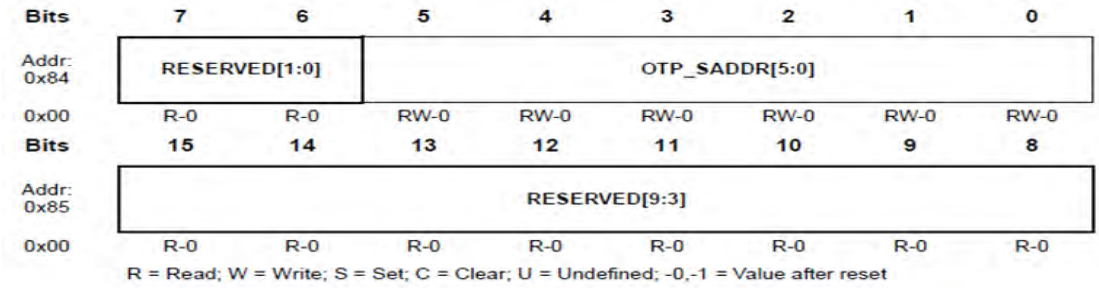


Bit 15..0 OTP_RDATA[15:0]: Data port for OTP read

An OTP read access from an OTP address specified in OTP_SADDR field of OTP_ADDRESS register will be triggered after a first read from this register. With a second read access to this register the actual OTP read data value can be accessed. An ongoing read transaction will be indicated by bit OTP_BUSY_RD in register OTP_STATUS.

Note that this register is only accessible in EXTENDED MODE.

4.5.2 Register OTP_ADDRESS (0x84)



Bit 5 to bit 0 OTP_SADDR[5:0] OTP address for OTP programming or read access

This field must be set with an OTP address before an OTP-read or programming access will be triggered via registers OTP_WRITE_DATA or OTP_READ_DATA.

Note that SADDR(0) is not significant. For an OTP read always two bytes will be returned in OTP_READ_DATA. For an OTP programming access low and high byte programming is controlled by bits 0 and 1 in register OTP_CONTROL.

Bit 9 to bit 0 RESERVED [9:0] bits not used.

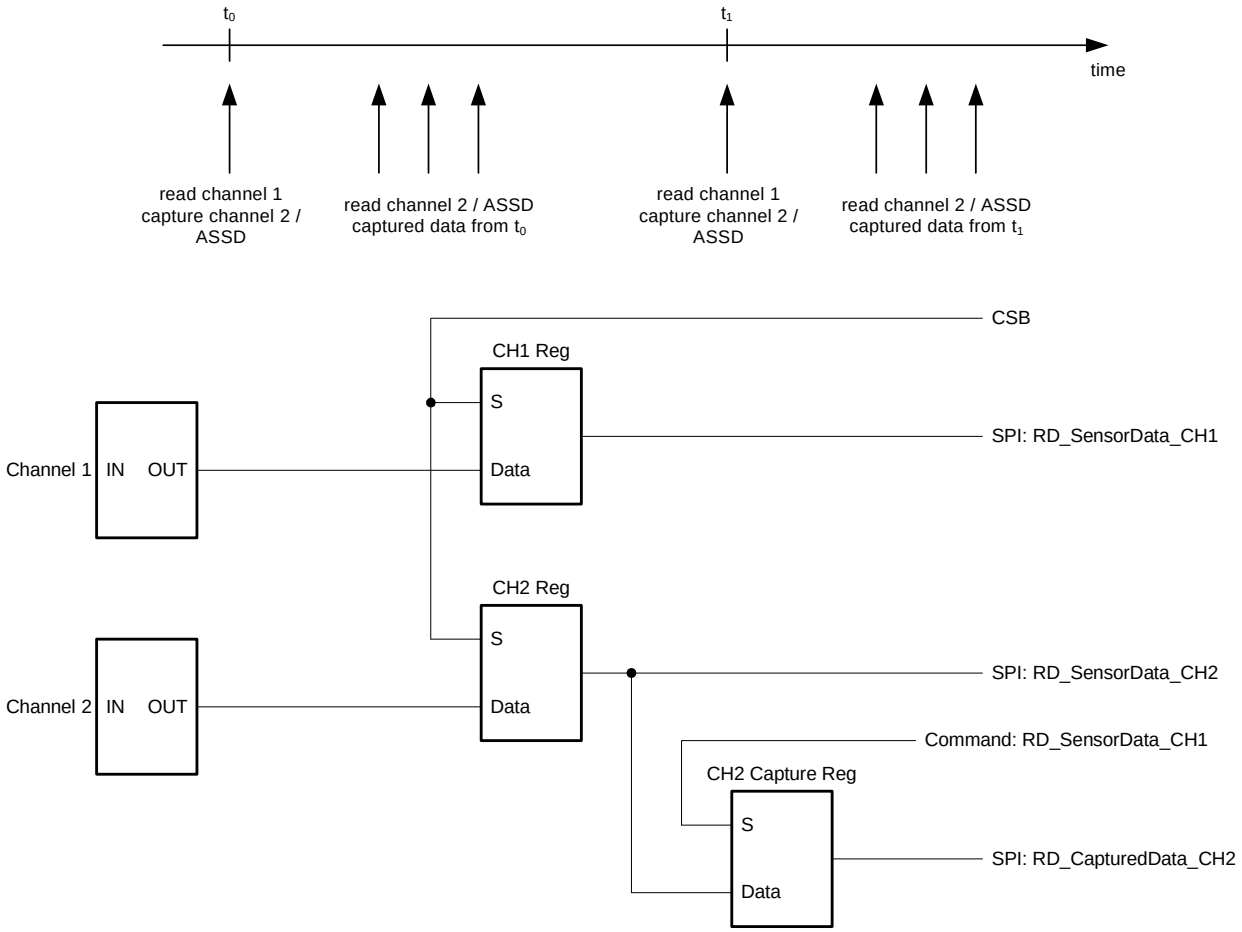
Note that this register is only accessible in EXTENDED MODE.

4.6 SPI Data Capturing

The protocol features data capturing for the second acceleration channel.

This means the sensor measurement data of channel 2 and ASSD is captured (stored in sensor internally) during every channel 1 request and read out at a later point in time.

With this concept, the sensor data of all 3 channels can be measured at the same point in time.



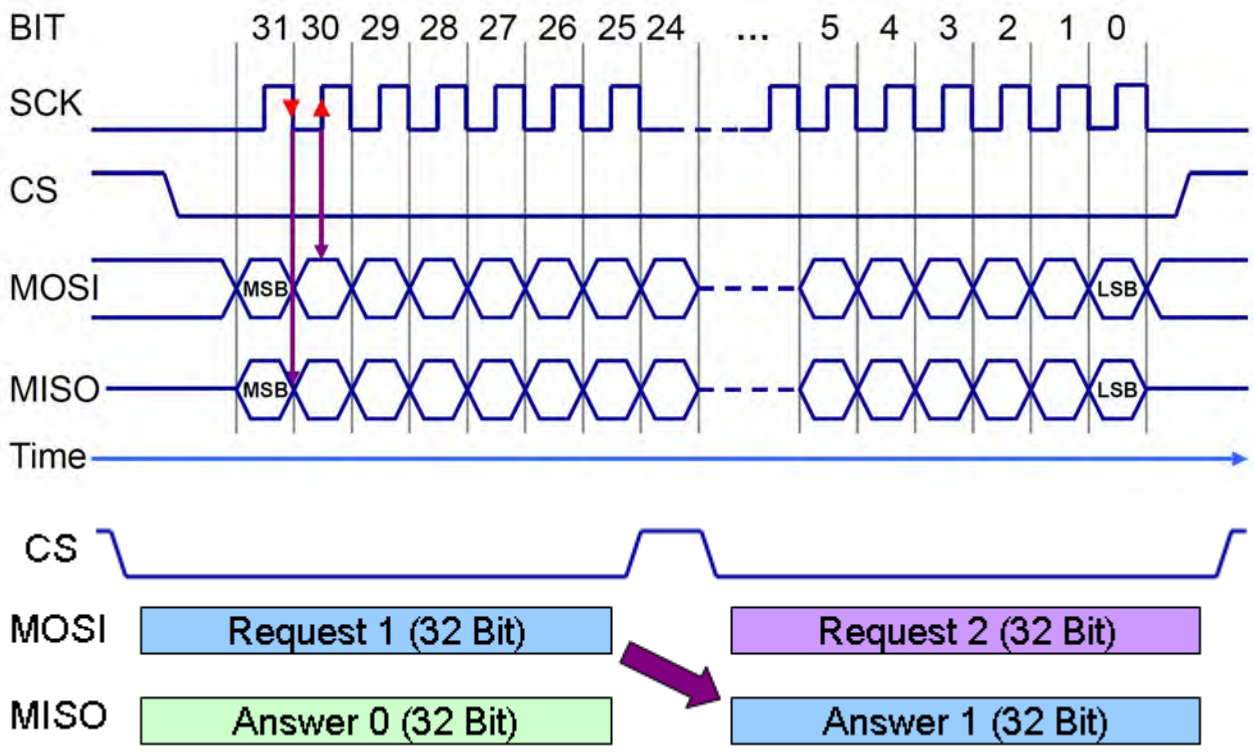
(Identical implementation for ASSD channel)

4.7 Open SPI Protocol

Communication between slave and master is realized by 32bit data word (MSB transmitted first). The maximum transmission rate is 4Mbaud for 5V mode (and 10Mbaud for other modes). A so-called off-frame protocol is used, i.e., each transfer is completed through a sequence of two phases. The answer of a given request is sent within the next frame having the same CSB active. The CSB active level is low. The SCK idle level is low.

The information at “Slave In” (SI) is taken over by the sensor with the rising edge of SCK, whereas the sensor sets the output level at “Slave out” (SO) with the falling edge of SCK.

Upon the last falling edge at SCK within each data word, the sensor sets the output SO to low. Therefore, upon CSB going active for the next transmission the level at SO is always low, i.e., the first bit of each datagram transmitted to the master is always ‘0’.



The SPI instruction set can be subdivided into two classes, acceleration and non-acceleration commands.

4.7.1 Acceleration commands (Open SPI)

These commands are used to request sensor data. The format of these commands is shown below. The 4 LSB of the 16 bit sensor data are “0”.

All MOSI Bits noted with “-” are DON’T CARE bits and have no influence (e.g. Bit0 of MOSI is a DON’T CARE bit).

Regular 32Bit acceleration data frame:

Read sensor data commands

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOSI	SEN	-	CH1	CH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2	CRC1	CRC0	-
	1	-	1/0	1/0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1/0	1/0	1/0	-
MISO	-	CH1	CH0	P0	ST1	ST0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	SF3	SF2	SF1	SF0	TST	SEN	NRC	CRC2	CRC1	CRC0
	0	1/0	1/0	1/0	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1	1/0	1/0	1/0	1/0

MOSI sensor data

Bit	Name	Description
SEN	Sensor bit	0=non sensor data request 1=Sensor data request
CH_n	Channel select	00=Channel1 01=Channel2 10=na 11=na
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit31...Bit4)

MISO sensor data

Bit	Name	Description
CH_n	Channel select	00=Channel1 01=Channel2 10=na 11=na
P0	Parity bit	P0 secures Bit31...Bit16 (odd parity)
ST_n	Signal mode	00= Non sensor data 01=Sensor data 10=Selftest data 11=Error
D_n	Data	Sensor data: 12Bit acceleration data
SF_n	Status flag	0000 = Sensor in normal operation 0001 = SPI transmission error 0010 = request error 0011 = condition not correct 0100 = no data available 0101 = end of programming not set 0110 = undervoltage error of regulator VDDA 0111 = ground loss detection 1000 = undervoltage error of supply VDDI 1001 = undervoltage error of supply VDD
TST	Selftest flag	0=Selftest not active 1=Selftest active
SEN	Sensor bit	0=non sensor data response 1=Sensor data response
NRC	Non regular operation	0= normal operation 1= No regular operation
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit30...Bit4)

For description of Status flags see Section 4.7.4.

Parity bit is even: Sum of the bits is even (including parity bit).

4.7.2 Non-acceleration commands (Open SPI)

These commands are used to write/read the sensor control and status registers.

Not used bits in the 16 bit data block of the sensor answer will be “0”.

All MOSI Bits noted with “-” are DON’T CARE bits and have no influence (e.g. Bit0 of MOSI is a DON’T CARE bit).

Remark:

In case of an invalid setting (inside the 16-bit data) the sensor ignores the whole command and responds a request error with the current register setting.

Non acceleration data frame (read access):

Non sensor data read commands

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOSI	SEN	-	OP1	OP0	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	Adr0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2	CRC1	CRC0	-
	0	-	1	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1/0	1/0	1/0	-
MISO	-	OP1	OP0	P0	ST1	ST0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SF3	SF2	SF1	SF0	TST	SEN	NRQ	CRC2	CRC1	CRC0
	0	1	1	1/0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	1/0	1/0	1/0	1/0

Non acceleration data frame (write access):

Non sensor data write commands

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOSI	SEN	-	OP1	OP0	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	Adr0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CRC2	CRC1	CRC0	-
	0	-	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	-
MISO	-	OP1	OP0	P0	ST1	ST0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SF3	SF2	SF1	SF0	TST	SEN	NRQ	CRC2	CRC1	CRC0
	0	0	1	1/0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	1/0	1/0	1/0	1/0

MOSI non sensor data

Bit	Name	Description
SEN	Sensor bit	0=non sensor data request 1=Sensor data request
OP_n	Operation Code	00=na 01=Write ASIC register 10=na 11=Read ASIC register
Adr_n	Data	Register/command adress
D_n	Data	Non sensor data write: 16Bit non acceleration data
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit31...Bit4)

MISO non sensor data		
Bit	**Name**	**Description**
OP_n	Operation Code	00=na 01=Write ASIC register 10=na 11=Read ASIC register
P0	Parity bit	P0 secures Bit31...Bit16 (odd parity)
ST_n	Signal mode	00= Non sensor data 01=Sensor data 10=Selftest data 11=Error
D_n	Data	Non sensor data: 16Bit non acceleration data
SF_n	Status flag	0000 = Sensor in normal operation 0001 = SPI transmission error 0010 = request error 0011 = condition not correct 0100 = no data available 0101 = end of programming not set 0110 = undervoltage error of regulator VDDA 0111 = ground loss detection 1000 = undervoltage error of supply VDDI 1001 = undervoltage error of supply VDD
TST	Selftest flag	0=Selftest not active 1=Selftest active
SEN	Sensor bit	0=non sensor data response 1=Sensor data response
NRO	Non regular operation	0= normal operation 1= No regular operation
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit30...Bit4)

For description of Status flags see Section 4.7.4.

4.7.3 CRC calculation

To check integrity of the sensor signals (SO) and commands (SI) to the sensor 3 bit CRC (cyclic redundancy check) is used. There are 27 CRC-relevant data bits (bit 30 to 4 for MISO) and 28 CRC-relevant data bits (bit 31 to 4 for MOSI). The CRC calculation is specified by:

Polynomial = x^3 + x + 1

Initial value = 111b

Target value = 000b

4.7.4 Open SPI Error Management

The open SPI32 Frame contains a cumulative failure flag for the monitor register (NRO) and a four-bit status flag (SF_3 – SF_0).

Status flag (SF_3 – SF_0):

Status flags stay active as long as the activation condition is present.

Status flags

Name	Name long	SF-code (SF_3 - SF_0)	Activation conditions	Failure priority	SF/NRO masks data (all bits "0") [yes=all bits "0"; no=data not masked]
SE	SPI transmission error	0001	set to '1' for request (SI) frame violation (incorrect number of SCK pulses more or less than 32 pulses). set to '1' for request (SI) CRC violation The message including SE has always the format of non-acceleration commands.	1	yes (for wrong SCK number) acceleration command: yes; other commands: no
RE	request error	0010	Set if SPI-command allowance matrix is violated set during the stabilization period after soft reset state (response to any non-acceleration command during the stabilization period of 4ms will be a RE) invalid value written for registers with enumeration fields invalid commands	2	yes
CNC	condition not correct	0011	set to '1' if sensor data for channel 3 or 4 has been requested (CH1 = 1, CH0 = 0 or CH1 = 1, CH0 = 1). set to '1' in case of single axis application and data for channel 2 has been requested (CH1 = 0, CH0 = 1).	3	yes
ND	no data available	0100	set during the stabilization period after soft reset / power on (response to any acceleration command during the stabilization period of 4ms will be a ND) set to '1' if sensor data for channel 1 or 2 has been requested while the fast offset cancelation is running => Monitor for master, showing if init and fast offset cancelation is completed or not.	4	yes
EOP	end of programming not set	0101	set as long as EOP is not set Compare to previous projects there will be no flag if BITE and FOC was not triggered before EOP	5	no
UVA	undervoltage error of regulator VDDA	0110	set if undervoltage on analog supply (internal) is detected	6	no
GND	ground loss detection	0111	set if a ground loss is detected	7	no
UVSI	undervoltage error of supply VDDI	1000	set during undervoltage situation at Vddi	8	no
UVS	undervoltage error of supply VDD	1001	set during undervoltage situation at Vdd	9	no

Remarks to undervoltage flags / SE flag:

No undervoltage flag is set: →Transmitted (sensor to ECU) acceleration data: valid

→ Transmitted (sensor to ECU) non acceleration data: valid

Any undervoltage flag is set: → Transmitted (sensor to ECU) acceleration data: invalid

→ Transmitted (sensor to ECU) non acceleration data: valid

SE flag is set → Transmitted (sensor to ECU) non acceleration data: invalid

TST (Sensor-Self-Test Flag)

This flag indicates that the Sensor-Self-Test is/was active. The flag stays active up to approx. 3.2ms after the Self-Test was deactivated.

States: 0: no Self-Test active
1: Self-Test active

No regular operation flag (NRO):

NRO flag		
Name	**Name long**	**Activation conditions**
NRO	no regular operation flag	cumulative error flag of monitor register 1 (set to '1' if at least one of the monitor flags is set and the failure condition is still present). NRO is not influenced by Inactive SOC flag before EOP is set.

Note: The NRO-flag is not set if a latched monitor flag is activated and the failure mode is not present anymore.

ST flag:

The signal mode ST flag is a summary flag: It shows 0b11 (="error data") if NRO bit is set or if status flag is not equal to 0b000 (normal operation) and SF is not equal to 0b0101 (EOP not set). This and all other combinations can be found in this table.

ST	**Condition (link: "and")**			
	SF	**TST**	**SEN**	**NRO**
00 (non-sensor data)	=0000 or =0101	don't care	=0	=0
01 (sensor data)	=0000 or =0101	=0	=1	=0
10 (self test data)	=0000 or =0101	=1	=1	=0
11 (error data)	≠0000 and ≠0101	don't care	don't care	don't care
	don't care	don't care	don't care	=1

This table explains the different conditions on the SF, TST, SEN and NRO bits for the four different states of the ST bit. The four right columns are all linked with a logical "and" condition.

Example of 3rd line "10 (self test data)":

- ST is 0b10 if: (SF=0000 OR SF=0101) AND TST=1 AND SEN=1 AND NRO=0

Monitor bits:

All monitor bits stay active as long as the failure mode is present. After the failure mode disappears, flags will be reset to “0”.

Monitor I Flags

Position	Name	Name long	Activation conditions	Relevant for acceleration data from channel1	Relevant for acceleration data from channel2	Relevant for nonacceleration data	NRO masks data (all bits "0") [yes=all bits "0"; no=data not masked] For non- and acceleration data.
0	**OC1**	offset cancellation error in channel 1	set if offset cancellation of channel 1 out of limit	yes	no	yes	no
1	**OC2**	offset cancellation error in channel 2	set if offset cancellation of channel 2 out of limit	no	yes	yes	no
2	**not used**	not used	fixed to 0	no	no	no	no
3	**not used**	not used	fixed to 0	no	no	no	no
4	**No CLK**	no clock	set if clock of on-chip oscillator is absent	yes	yes	yes	yes
5	**OSC**	oscillator out of limits	set if oscillator frequency out of range (has to be activated via SPI command)	yes	yes	yes	no
6	**OTP**	memory error of OTP data	set if the content of the MEMORY has an error. This error is detected by the cyclic redundancy check.	yes	yes	yes	no
7	**Lock**	lockbit error	set if at least one of the OTP lock bits is not set	yes	yes	yes	no
8	**not used**	not used	fixed to 0	no	no	no	no
9	**EXT_M**	extended mode	set if extended mode is active	yes	yes	yes	no
10	**SOC1**	slow offset cancellation incative	set if slow offset cancellation is inactive in channel 1 after EOP	yes	no	yes	no
11	**SOC2**	slow offset cancellation incative	set if slow offset cancellation is inactive in channel 2 after EOP	no	yes	yes	no
12	**CD**	capacity loss detection execution	set if C-loss detection (at startup or continious) is/was executed	yes	yes	yes	no
13	**ASSD**	ASSD error	error detected by ASSD	yes	yes	yes	no
14	**ME**	mirror error of device configuration data. See also chapter Safety-Relevant-Configuration-Registers	set if arming pin configuration mirror mismatch is detected set if filter configuration (channel 1 or 2) mirror mismatch is detected set if protocol selection mirror mismatch is detected set if voltage mode configuration mirror mismatch is detected	yes	yes	yes	no
15	**OC_ASSD**	offset cancellation error in ASSD	set if offset cancellation of ASSD out of limit	yes	yes	yes	no

Monitor II Flags

Position	Name	Name long	Activation conditions	Relevant for acceleration data from channel1	Relevant for acceleration data from channel2	Relevant for nonacceleration data	SF/NRO masks data (all bits "0") [yes=all bits "0"; no=data not masked]
0	FOC1	fast offset cancellation active in channel 1	set if fast offset cancellation is running in channel 1	no	no	no	no
1	FOC2	fast offset cancellation active in channel 2	set if fast offset cancellation is running in channel 2	no	no	no	no
2	FOC_ASSD	fast offset cancellation active in ASSD	set if fast offset cancellation is running in ASSD	no	no	no	no

4.7.5 Open SPI Instruction Set

Name	description	Header	16 bit Data (in case of "read" commands only for sensor response;)
PROT_SEL	protocol selection to switch between Bosch SPI and Open SPI	0x00F	Hex = 00FF00FF
PROG_MODE	voltage mode selection	0x140	0 0 0 0 0 0 0 0 0 0 0 0 voltage mode
RD_MODE	read voltage and protocol mode	0x340	Register CRC 0 0 0 PRO voltage mode
RD_DEVICE_ID	read device ID	0x342	0 0 0 0 0 0 0 0 0 1 1 0 0 1 1 0
RD_REVISION_ID	read revision ID	0x344	0 0 0 0 0 0 0 0 revision ID
RD_SENSOR_DATA_CH1	read sensor data of channel 1	0x800	S1_11 - S1_0 0 0 0 0
RD_SENSOR_DATA_CH2	read sensor data of channel 2	0x900	S2_11 - S2_0 0 0 0 0
RD_OFFSET_REG_CH1	read the register with the current offset cancellation value	0x352	16 bit offset data
RD_OFFSET_REG_CH2	read the register with the current offset cancellation value	0x354	16 bit offset data
DEMAND_OFFSET_CANCELLATION	trigger FOC/SOC	0x158	0 0 0 0 ASSD OC length2 OFF2 OC length1 OFF1
RD_OFFSET_CANCELLATION	read the status of the offset cancellation	0x358	0 0 0 0 ASSD OC length2 OFF2 OC length1 OFF1
RD_CLOCK_COUNTER	read the current value of the clock counter (captured value in case of automatic system clock monitoring)	0x35A	16 bit clock counter
WR_CLOCK_COUNTER_MIN	write the current value of the clock counter register limit min (automatic system clock monitoring)	0x15C	Automatic clock counter check lower limit
RD_CLOCK_COUNTER_MIN	read the current value of the clock counter register limit min (automatic system clock monitoring)	0x35C	Automatic clock counter check lower limit
WR_CLOCK_COUNTER_MAX	write the current value of the clock counter register limit max (automatic system clock monitoring)	0x15E	Automatic clock counter check upper limit
RD_CLOCK_COUNTER_MAX	read the current value of the clock counter register limit max (automatic system clock monitoring)	0x35E	Automatic clock counter check upper limit
WR_CLOCK_COUNTER_FLTCNT	write the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)	0x160	0 0 0 0 0 0 0 0 8 bit fault threshold
RD_CLOCK_COUNTER_FLTCNT	read the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)	0x360	0 0 0 0 0 0 0 0 8 bit fault threshold
DEMAND_FOR_TEST	trigger build in self test	0x162	0 0 0 0 0 0 0 0 0 0 TMDASSD TMD2 TMD1
RD_TEST_MODE	read the status of the build in self test	0x362	0 0 0 0 0 0 0 0 0 0 TMDASSD TMD2 TMD1
RD_MONITOR_I_DATA	read monitor 1 data	0x364	Monitor I flags
RD_MONITOR_II_DATA	read monitor 2 data	0x366	Monitor II flags
WR_CONFIG_1	write configuration for C-loss detection and oscillator monitoring	0x168	0 0 0 0 0 0 0 0 OSCM C_Loss ASSD Filter2 Filter1
RD_CONFIG_1	read configuration for C-loss detection and oscillator monitoring	0x358	0 0 0 0 0 0 0 0 OSCM C_Loss ASSD Filter2 Filter1
WR_CONFIG_2	write configuration for arming pin	0x16A	0 0 0 0 0 0 Sampl TH 8 bit arming threshold
RD_CONFIG_2	read configuration for arming pin	0x36A	0 0 0 0 0 0 Sampl TH 8 bit arming threshold
DEMAND_SOFT_RESET	reset of the component (SO only for the first transmission)	0x16E	Soft reset
END_OF_PROG	locking command, after EOP only read commands allowed, also DEMAND_SOFT_RESET	0x170	End of programming
RD_BITE_CH1	read BITE OTP value of channel 1	0x31A	positive BITE OTP channel CH1 / negative BITE OTP channel CH1
RD_BITE_CH2	read BITE OTP value of channel 2	0x31C	positive BITE OTP channel CH2 / negative BITE OTP channel CH2
RD_SERIAL1	read serial number bit15 - bit0	0x300	serial number (SN15 - SN0)
RD_SERIAL2	read serial number bit31 - bit16	0x302	serial number (SN31 - SN16)
RD_SERIAL3	read serial number bit47 - bit32	0x304	serial number (SN47 - SN32)

Note: Headers are bits 31-20 of MOSI commands.

4.7.5.1 PROT_SEL

PROT_SEL: protocol selection to switch between Bosch SPI X"FF00FF00" and Open SPI X"00FF00FF"

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

4.7.5.2 PROG_MODE

PROG_MODE: program voltage

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	voltage mode				CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	Reg CRC								0	0	0	PRO	voltage mode				SF3 - SF0				TST	SEN	MEM	CRC2 - CRC0		

Voltage Mode:
0010: Supply = 6.7V; SPI = 3.3V
0100: Supply =5V; SPI = 5V
1000: Supply = 3.3V; SPI = 3.3V
all other combinations = not allowed --> no voltage mode selected (SO stay in tristate)

PRO:
0: Bosch SPI
1: open SPI

Reg CRC:
Contains the CRC for error detection within the configuration registers

4.7.5.3 RD_MODE

RD_MODE: read voltage and protocol mode

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	Reg CRC								0	0	0	PRO	voltage mode				SF3 - SF0				TST	SEN	MEM	CRC2 - CRC0		

Voltage Mode:
0010: Supply = 6.7V; SPI = 3.3V
0100: Supply =5V; SPI = 5V
1000: Supply = 3.3V; SPI = 3.3V

PRO:
0: Bosch SPI
1: open SPI

Reg CRC:
Contains the CRC for error detection within the configuration registers

4.7.5.4 RD_DEVICE_ID

RD_DEVICE_ID: read device ID

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	SF3 - SF0				TST	SEN	MEM	CRC2 - CRC0		

value fix "0x66"

Note: The Device ID identifies the ASIC type. Any Sensor using TA660 has fixed value in Data field of 0x66hex.

4.7.5.5 RD_REVISION_ID

RD_REVISION_ID: read revision ID

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	0	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	revision ID								SF3 - SF0				TST	SEN	MEM	CRC2 - CRC0		

Note: The revision ID must not be checked against a fixed value. It can be subject to change without prior customer notification.

4.7.5.6 RD_SENSOR_DATA_CH1

RD_SENSOR_DATA_CH1: read sensor data of channel 1 (clipping to +2047, -2047)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	1	-	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	0	0	P0	ST1	ST0	S1_15 - S1_0																SF3 - SF0				TST	SEN	MEM	CRC2 - CRC0		

4.7.5.7 RD_SENSOR_DATA_CH2

RD_SENSOR_DATA_CH2: read sensor data of channel 2 (clipping to +2047, -2047)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	1	-	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	S2_15 - S2_0																SF3 - SF0				TST	SEN	MEM	CRC2 - CRC0		

4.7.5.8 RD_OFFSET_REG_CH1

RD_OFFSET_REG_CH1: read the register with the current offset cancellation value (Register will be changed by FOC & SOC)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	1	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	16 bit offset data																SF3 - SF0				TST	SEN	MRQ	CRC2 - CRC0		

16 bit offset data channel 1:
Conversion factor 0.5 for sensor output
example: "16 bit offset data channel 1"=200 LSB == 100 LSB sensor channel output correction value

4.7.5.9 RD_OFFSET_REG_CH2

RD_OFFSET_REG_CH2: read the register with the current offset cancellation value (Register will be changed by FOC & SOC)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	1	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	16 bit offset data																SF3 - SF0				TST	SEN	MRQ	CRC2 - CRC0		

16 bit offset data channel 2:
Conversion factor 0.5 for sensor output
example: "16 bit offset data channel 2"=200 LSB == 100 LSB sensor channel output correction value

4.7.5.10 DEMAND_OFFSET_CANCELLATION

DEMAND_OFFSET_CANCELLATION: start FOC or SOC

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	0	1	1	0	0	0	-	-	-	-	ASSD		OC length 2			OFF2		OC length 1			OFF1		CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	0	0	0	0	ASSD		OC length 2			OFF2		OC length 1			OFF1		SF3 - SF0				TST	SEN	MRQ	CRC2 - CRC0		

OFF1:
00: offset cancellation channel 1 switched off **-->default**
01: slow offset cancellation channel 1 switched on (1LSB/s)
10: slow offset cancellation channel 1 switched on (1LSB/21s)
11: fast offset cancellation channel 1 switched on

OFF2:
00: offset cancellation channel 2 switched off **-->default**
01: slow offset cancellation channel 2 switched on (1LSB/s)
10: slow offset cancellation channel 1 switched on (1LSB/21s)
11: fast offset cancellation channel 2 switched on

ASSD:
00: offset cancellation ASSD switched off **-->default**
01: slow offset cancellation ASSD switched on
11: fast offset cancellation ASSD switched on (64 samples)

OC length1&2:
000: 64 samples --> **default**
001: 128 samples
010: 256 samples
011: 512 samples
100: 1024 samples
all other values are not executed and lead to a RE

4.7.5.11 RD_OFFSET_CANCELLATION

RD_OFFSET_CANCELLATION: read the status of the offset cancellation

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	1	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	0	0	0	0	ASSD		OC length 2			OFF2		OC length 1			OFF1		SF3 - SF0				TST	SEN	MRQ	CRC2 - CRC0		

OFF1:
00: offset cancellation channel 1 switched off
01: slow offset cancellation channel 1 switched on
10: slow offset cancellation channel 1 switched on (1LSB/21s)
11: fast offset cancellation channel 1 switched on

OFF2:
00: offset cancellation channel 2 switched off
01: slow offset cancellation channel 2 switched on
10: slow offset cancellation channel 2 switched on (1LSB/21s)
11: fast offset cancellation channel 2 switched on

ASSD:
00: offset cancellation ASSD switched off -->default
01: slow offset cancellation ASSD switched on
11: fast offset cancellation ASSD switched on (64 samples)

4.7.5.12 RD_CLOCK_COUNTER

RD_CLOCK_COUNTER: read the current value of the clock counter register (captured value in case of automatic system clock monitoring)

SI	0	-	1	1	0	1	0	1	1	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	Automatic clock counter																SF3 - SF0				TST	SEN	MRQ	CRC2 - CRC0		

Counter frequency = 2.25MHz

4.7.5.13 WR_CLOCK_COUNTER_MIN

WR_CLOCK_COUNTER_MIN: write the current value of the clock counter register limit min (automatic system clock monitoring)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	0	1	1	1	0	0	Automatic clock counter check lower limit																CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	Automatic clock counter check lower limit																SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

Clock counter register min:
0…16383: lower failure threshold number of counted clocks (2.25MHz)
0 **-->default**

4.7.5.14 RD_CLOCK_COUNTER_MIN

RD_CLOCK_COUNTER_MIN: read the current value of the clock counter register limit min (automatic system clock monitoring)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	Automatic clock counter check lower limit																SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

4.7.5.15 WR_CLOCK_COUNTER_MAX

WR_CLOCK_COUNTER_MAX: write the current value of the clock counter register limit max (automatic system clock monitoring)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	0	1	1	1	1	0	Automatic clock counter check upper limit																CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	Automatic clock counter check upper limit																SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

Clock counter register max:
0…65535: upper failure threshold number of counted clocks (2.25MHz)
65535 **-->default**

4.7.5.16 RD_CLOCK_COUNTER_MAX

RD_CLOCK_COUNTER_MAX: read the current value of the clock counter register limit max (automatic system clock monitoring)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	0	1	1	1	1	0	Automatic clock counter check upper limit																CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	Automatic clock counter check upper limit																SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

4.7.5.17 WR_CLOCK_COUNTER_FLTCNT

WR_CLOCK_COUNTER_FLTCNT: write the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	0	0	0	0	0	0	-	-	-	-	-	-	-	-	8 bit fault threshold								CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	8 bit fault threshold								SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

Clock counter FLTCNT:
#=0…254: if ># failures are detected in a row, monitor flag will be set
255: limit is not effective (8 bit fault counter): deactivated oscillator monitor flag **-->default**

4.7.5.18 RD_CLOCK_COUNTER_FLTCNT

RD_CLOCK_COUNTER_FLTCNT: read the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	1	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	8 bit fault threshold								SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

Clock counter FLTCNT:
0…255: maximum number of failure events in row without oscillator failure flag is set

4.7.5.19 DEMAND_FOR_TEST

DEMAND_FOR_TEST: trigger build in self test

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	1	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	TMDASSD		TMD2		TMD1		CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	0	0	TMDASSD		TMD2		TMD1		SF3 - SF0				TST	SEN	NEU	CRC2 - CRC0		

TMD1 :
00: switch off self test channel 1 **-->default**
01: pos. amplitude of self test channel 1
10: neg. amplitude of self test channel 1
11 = not defined --> RE

TMD2:
00: switch off self test channel 2 **-->default**
01: pos. amplitude of self test channel 2
10: neg. amplitude of self test channel 2
11 = not defined --> RE

TMDASSD:
00: switch off self test ASSD **-->default**
01: pos. amplitude of ASSD
10: neg. amplitude of ASSD
11 = not defined --> RE

Remark:
Selfself test of channel 1, 2 and ASSD can be de/activated within one command

4.7.5.20 RD_TEST_MODE

RD_TEST_MODE:

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	1	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	0	0	TMDASSD		TMD2		TMD1		SF3 - SF0				TST	SEN	HF0	CRC2 - CRC0		

TMD1 :
00: switch off test channel 1
01: pos. amplitude of self test channel 1
10: neg. amplitude of self test channel 1

TMD2:
00: switch off test channel 2
01: pos. amplitude of self test channel 2
10: neg. amplitude of self test channel 2

TMDASSD:
00: switch off self test ASSD -->default
01: neg. amplitude of ASSD
10: pos. amplitude of ASSD
11 = not defined --> RE

4.7.5.21 RD_MONITOR_I_DATA

RD_MONITOR_I_DATA:

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	1	0	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	Monitor I flags																SF3 - SF0				TST	SEN	HF0	CRC2 - CRC0		

4.7.5.22 RD_MONITOR_II_DATA

RD_MONITOR_II_DATA:

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	1	0	0	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	0	0	0	0	0	Monitor II flags			SF3 - SF0				TST	SEN	HF0	CRC2 - CRC0		

4.7.5.23 WR_CONFIG_1

WR_CONFIG_1: write configuration for C-loss and Osc monitoring

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	1	0	1	0	0	0	-	-	-	-	-	-	-	-	OSCM		C_loss	ASSD	Filter 2		Filter 1		CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	OSCM		C_loss	ASSD	Filter 2		Filter 1		SF3 - SF0				TST	SEN	HF0	CRC2 - CRC0		

C-loss:
0 = no initial C-loss detection running -->**default**
1 = activation of initial C-loss detection (will be reset automatically after finishing)

OSCM (oscillator monitoring mode):
00 = clock counter running and readable, disable clock counter register and oscillator monitoring flag -->**default**
01 = enable clock counter register, disable oscillator monitoring flag
11 = enable clock counter register and oscillator monitoring flag
10 = not defined --> RE

ASSD:
0 = ASSD monitor off
1 = ASSD monitor on --> **default**

Filter 1 (filter frequency of channel 1):
00 = 426 Hz --> **default**
01 = 213 Hz
10 = 106 Hz
11 = 53 Hz

Filter 2 (filter frequency of channel 2):
00 = 426 Hz --> **default**
01 = 213 Hz
10 = 106 Hz
11 = 53 Hz

Note: to fulfil Safety requirements the ASSD monitor has to be set as “1”.

4.7.5.24 RD_CONFIG_1

RD_CONFIG_1: read configuration for C-loss and Osc monitoring

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	1	0	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0		-	
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	OSCM		C_loss	ASSD	Filter 2		Filter 1		SF3 - SF0				TST	SEN	MEC	CRC2 - CRC0		

C-loss:
0 = no initial C-loss detection running
1 = initial C-loss detection is currently running (will be reset automatically after finishing)

OSCM (oscillator monitoring mode):
00 = clock counter running and readable, disable clock counter register and oscillator monitoring flag
01 = enable clock counter register, disable oscillator monitoring flag
11 = enable clock counter register and oscillator monitoring flag

ASSD:
0 = ASSD monitor off
1 = ASSD monitor on

Filter 1 (filter frequency of channel 1):
00 = 426 Hz
01 = 213 Hz
10 = 106 Hz
11 = 53 Hz

Filter 2 (filter frequency of channel_2):
00 = 426 Hz
01 = 213 Hz
10 = 106 Hz
11 = 53 Hz

4.7.5.25 WR_CONFIG_2

WR_CONFIG_2: Armingpin

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	1	0	1	0	1	0	-	-	-	-	-	-	Sample TH		arming threshold								CRC2 - CRC0		-	
SO	0	0	1	P0	ST1	ST0	0	0	0	0	0	0	Sample TH		arming threshold								SF3 - SF0				TST	SEN	MEC	CRC2 - CRC0		

Arming threshold:
0: arming pin in tristate / arming pin deactivated --> **default**
1...255: Arming threshold (1 LSB of arming threshold = 4 LSB of sensor data)

Arming threshold [LSB]	*Sensor data [LSB]*
1	*4*
2	*8*
3	*12*
...	...
255	*1020*

|data CH1| <= arming threshold, then arming pin = tristate
|data CH2| <= arming threshold, then arming pin = tristate
|data CH1| > arming threshold (for more than "Sample Th" times), then arming pin = low
|data CH2| > arming threshold (for more than "Sample Th" times), then arming pin = low

Sample threshold:
00: Arming pin is activated if the arming threshold is violated one time (sensor data read access)
01: Arming pin is activated if the arming threshold is violated two times (sensor data read access)
10: Arming pin is activated if the arming threshold is violated three times (sensor data read access)
11: Arming pin is activated if the arming threshold is violated four times (sensor data read access) --> **default**

4.7.5.26 RD_CONFIG_2

RD_CONFIG_2: Armingpin

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	1	1	0	1	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0		-	
SO	0	1	1	P0	ST1	ST0	0	0	0	0	0	0	Sample TH		arming threshold								SF3 - SF0				TST	SEN	MEC	CRC2 - CRC0		

Arming threshold:
0: arming pin in tristate / arming pin deactivated
1...255: Arming threshold (1 LSB of arming threshold = 4 LSB of sensor data)

Arming threshold [LSB]	*Sensor data [LSB]*
1	*4*
2	*8*
3	*12*
...	...
255	*1020*

|data CH1| <= arming threshold, then arming pin = tristate
|data CH2| <= arming threshold, then arming pin = tristate
|data CH1| > arming threshold (for more than "Sample Th" times), then arming pin = low
|data CH2| > arming threshold (for more than "Sample Th" times), then arming pin = low

Sample threshold:
00: Arming pin is activated if the arming threshold is violated one time (sensor data read access)
01: Arming pin is activated if the arming threshold is violated two times (sensor data read access)
10: Arming pin is activated if the arming threshold is violated three times (sensor data read access)
11: Arming pin is activated if the arming threshold is violated four times (sensor data read access)

4.7.5.27 DEMAND_SOFT_RESET

DEMAND_SOFT_RESET: reset of the component (SO only for the first transmission); has to be sent 2 times --> Leads to the same state like after the voltage selection command (everything reset except SPI protocol and voltage mode)

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

4.7.5.28 END_OF_PROG

END_OF_PROG: locking command, after EOP only read commands allowed, also DEMAND_SOFT_RESET

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	0	1	0	1	1	1	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	CRC2 - CRC0			-
SO	0	0	1	P0	ST1	ST0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

4.7.5.29 RD_BITE_CH1

RD_BITE_CH1: read BITE OTP value of channel 1

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	0	0	1	1	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	positive BITE OTP channel CH1								negative BITE OTP channel CH1								SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

positive BITE OTP channel CH1 / negative BITE OTP channel CH1:
-128...+127: end-of-line saved BITE values in g (signed value; two's complement)
example: 0b10110100 (Bit10...Bit17) ==> -76g ==> -1216 LSB sensor output (for nom. sensitivity)

4.7.5.30 RD_BITE_CH2

RD_BITE_CH2: read BITE OTP value of channel 2

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	0	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	positive BITE OTP channel CH2								negative BITE OTP channel CH2								SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

positive BITE OTP channel CH2 / negative BITE OTP channel CH2:
-128...+127: end-of-line saved BITE values in g (signed value; two's complement)
example: 0b10110100 (Bit10...Bit17) ==> -76g ==> -1216 LSB sensor output (for nom. sensitivity)

4.7.5.31 RD_SERIAL1

RD_SERIAL1: serial number

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	serial number (SN15 - SN0)																SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

4.7.5.32 RD_SERIAL2

RD_SERIAL2: serial number

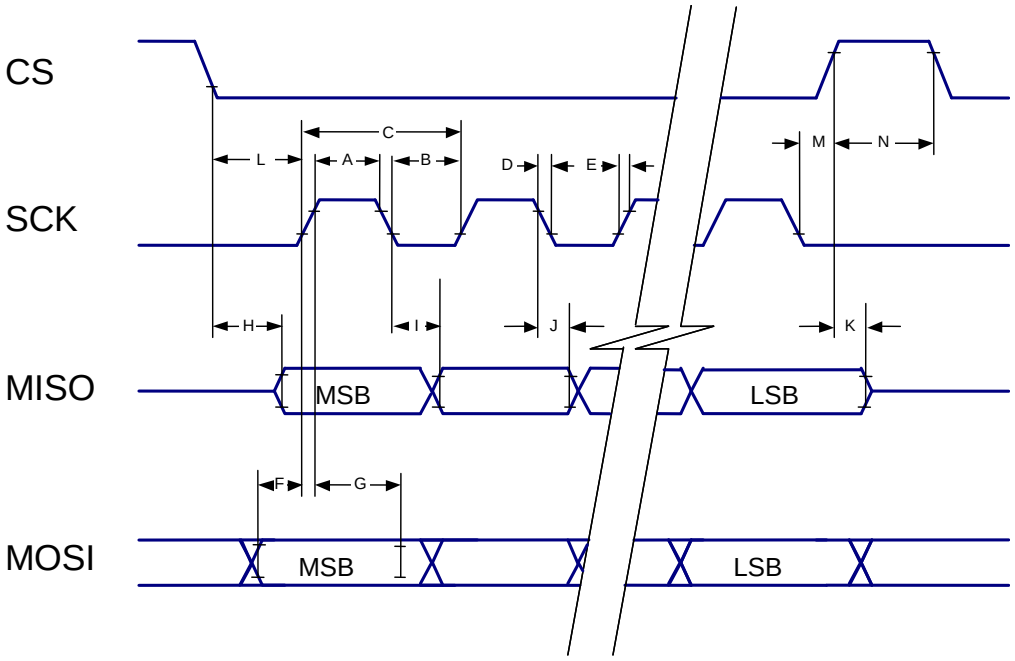
	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	0	0	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	serial number (SN31 - SN16)																SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

4.7.5.33 RD_SERIAL3

RD_SERIAL3: serial number

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	0	-	1	1	0	0	0	0	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			-
SO	0	1	1	P0	ST1	ST0	serial number (SN47 - SN32)																SF3 - SF0				TST	SEN	NRC	CRC2 - CRC0		

4.7.6 Open SPI timing



The maximum SPI clock frequency that the sensor is guaranteed to be functional is provided below. This frequency must not be exceeded.

3.3V & 6.7V Application

Num	Parameter	Symbol	Min.	Max.	Unit
-	SPI clock frequency 3.3V & 6.7V mode	f_{OP}	-	10*	MHz
A	Clock (SCK) high time	t_{WSCKIh}	½*t_{SCK}–13	-	ns
B	Clock (SCK) low time	t_{WSCKI}	½*t_{SCK}–13	-	ns
C	SCK period	t_{SCK}	100	-	ns
D	Clock (SCK) fall time	t_f	5.5	13	ns
E	Clock (SCK) rise time	t_r	5.5	13	ns
F	Data input (MOSI) setup time	t_{su}	30		ns
G	Data input (MOSI) hold time	t_{hi}	40		ns
H	Data output (SO) access time	t_a	-	40	ns
I	Data output (SO) valid after SCK	t_v	-	35	ns
J	Data output (SO) lag time	t_{lag}	0	-	ns
K	Data output (MISO) disable time	t_{dis}	-	100	ns

L	Enable (SCK) lead time	t_{lead}	½*t_{SCK}	-	ns
M	Enable (SCK) lag time	t_{lag}	½*t_{SCK}	-	ns
N	Sequential transfer delay	t_{td}	1.9	-	µs

Note: * To establish communication up to this frequency all other parameters in the table must be satisfied.

The table assumes a VDD_IO voltage of 3V, a capacitive load of 100 pF and the minimum drive frequency (PLL). Parameters may be better for other voltages, drive frequency and capacitive loads (as far as covered by operating condition specification)

5V Application

Num	Parameter	Symbol	Min.	Max.	Unit
-	SPI clock frequency 5V mode	f_{OP}	-	4*	MHz
A	Clock (SCK) high time	t_{WSCKIh}	½*t_{SCK} –13	-	ns
B	Clock (SCK) low time	t_{WSCKI}	½*t_{SCK} –13	-	ns
C	SCK period	t_{SCK}	250	-	ns
D	Clock (SCK) fall time	t_f	5.5	13	ns
E	Clock (SCK) rise time	t_r	5.5	13	ns
F	Data input (MOSI) setup time	t_{su}	30		ns
G	Data input (MOSI) hold time	t_{hi}	40		ns
H	Data output (SO) access time	t_a	-	40	ns
I	Data output (SO) valid after SCK	t_V	-	100	ns
J	Data output (SO) lag time	t_{lag}	0	-	ns
K	Data output (MISO) disable time	t_{dis}	-	100	ns
L	Enable (SCK) lead time	t_{lead}	½*t_{SCK}	-	ns
M	Enable (SCK) lag time	t_{lag}	½*t_{SCK}	-	ns
N	Sequential transfer delay	t_{td}	1.9	-	µs

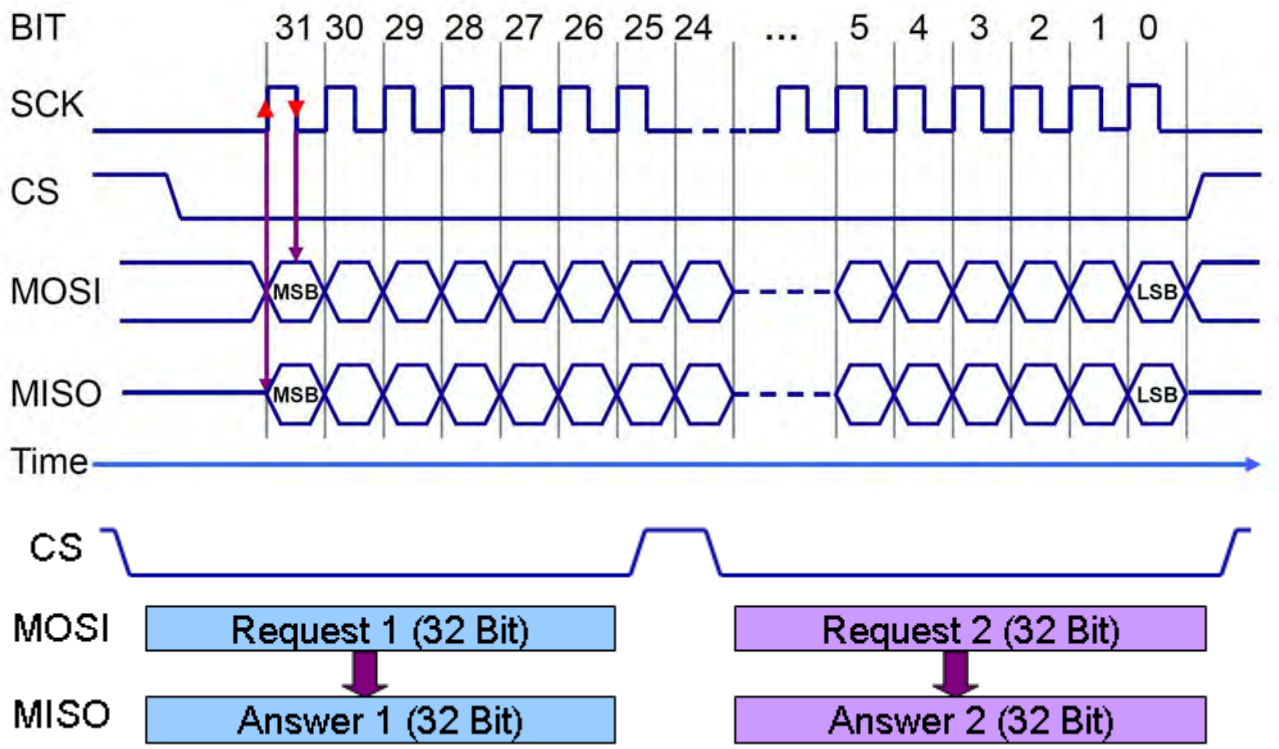
Note: * To establish communication up to this frequency all other parameters in the table must be satisfied.

The table assumes a VDD_IO voltage of 3V, a capacitive load of 100 pF and the minimum drive frequency (PLL). Parameters may be better for other voltages, drive frequency and capacitive loads (as far as covered by operating condition specification)

4.8 Bosch SPI Protocol

Communication between slave and master is realised by 32bit data word (MSB transmitted first). The maximum transmission rate is 4Mbaud for 5V mode (and 10 Mbaud for other modes). A so-called in-frame protocol is used. The answer of a given request is sent immediately. The CSB active level is low. The SCK idle level is low.

The information at “Slave In” (SI) is taken over by the sensor with the falling edge of SCK, whereas the sensor sets the output level at “Slave out” (SO) with the rising edge of SCK.



The SPI instruction set can be subdivided into two classes, acceleration and non-acceleration commands.

4.8.1 Acceleration commands (Bosch SPI)

These commands are used to request sensor data. The format of these commands is shown below.

The 4 LSB of the 16 bit sensor data are “0”.

<u>32Bit acceleration data frame:</u>

Sensor data commands

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	S	channel					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	status						S	SID					12 bit output data												0	0	0	0	gs	CRC			

MOSI sensor data

Bit	Name	Description
S	Sensor bit	0 = non sensor data request 1 = Sensor data request
CH	Channel select	00000 = Ch1 10000 = Ch2
CRC	CRC-Code	3 bit CRC-Code (covering bit 5 to bit 31)

MISO sensor data		
Bit	**Name**	**Description**
status	Status flags	Bit 31 = TFF Bit 30 = TST Bit 29 = EOP Bit 28 = 0 (not used) Bit 27 = TF (Temporary fault) Bit 26 = PF (Permanent fault)
S	Sensor bit	0 = Non sensor data request 1 = Sensor data request
SID	sensor ID	Programmable identifier for sensordata CH1/2
data	Acceleration data	12 bit Acceleration data (two's complement) in 16 bit block
gs	general status	0 = normal operation 1 = No regular operation (Monitor flag active)
CRC	CRC-Code	3 bit CRC-Code (covering bit 3 to bit 26)

Explanation of Status flags:

TFF (Transfer Failure Flag)

This flag indicates that an error occurred in the last SPI transmission.
Possible errors that lead to this are:

- SPI frame doesn't have 32 SCK pulses
- transmitted bus address is not part of the address space
- transmitted bus address is protected in the current mode

States: 0: no error detected
1: error detected

TST (Sensor-Self-Test Flag)

This flag indicates that the Sensor-Self-Test is/was active. The flag stays active up to approx. 3.2ms after the Self-Test was deactivated.

States: 0: no Self-Test active
1: Self-Test active

EOP (End-Of-Programming)

This flag indicates that the EOP-command was not sent during the power-on-cycle. After the EOP-command was sent, the ECU has only a limited access to the internal registers (see 4.3.5).

States: 0 End-Of-Programming transmitted
1 End-Of-Programming **not** transmitted

TF (Temporary Fault)

This flag indicates that a temporary fault is active. (See below for detailed description)

States: 0 no error detected
1 error detected

PF (Permanent Fault)

This flag indicates that a permanent fault is active. (See below “Monitor I & II table” for detailed description)

States: 0 no error detected
1 error detected

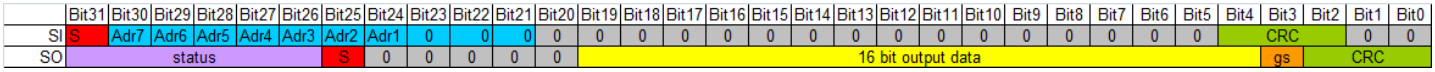
4.8.2 Non-acceleration commands (Bosch SPI)

These commands are used to write/read the sensor control and status registers.

Remark:

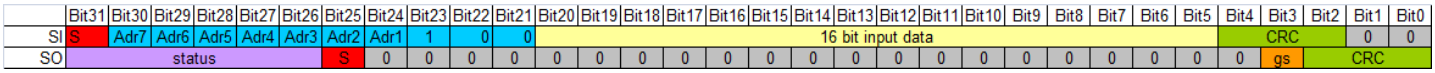
In case of an invalid setting (inside the 16bit data) the sensor writes the default value into the register.

- Non-acceleration data frame (read access):



	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	S	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	status						S	0	0	0	0	0	16 bit output data																gs	CRC			

- Non-acceleration data frame (write access):



	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	S	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	1	0	0	16 bit input data																CRC			0	0
SO	status						S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

Bit	Name	Description
S	Sensor bit	0 = non sensor data request 1 = Sensor data request
Adr_n	instruction	Adr7 to Adr1 corresponding to bit 7 to bit 1 of address; Last bit(bit0) of Address is omitted
data	Data	16 bit non acceleration data (don't care for read access)
CRC	CRC-Code	3 bit CRC-Code (covering bit 5 to bit 31)

MISO non sensor data

Bit	Name	Description
status	Status flags	Bit 31 = TFF Bit 30 = TST Bit 29 = EOP Bit 28 = 0 (not used) Bit 27 = TF (Temporary fault) Bit 26 = PF (Permanent fault)
S	Sensor bit	0 = non sensor data request 1 = Sensor data request
data	Data	16 bit non acceleration data (don't care for write access)
gs	general status	0 = normal operation 1 = Sensor defect / no regular operation (Monitor flag active)
CRC	CRC-Code	3 bit CRC-Code (covering bit 3 to bit 26)

Example: Read Monitor Flag 1

In order to read Monitor Flag1, access to CFG Register “CFG_MONITOR_FLAG_1” with address 0x64hex (= 0x1100100) has to be enabled. The Address is mapped to Adr_n in no Acceleration command (Read access). Last bit of the Register Address is omitted; therefore 0x1100100 becomes 0x110010 in Adr_n.

As no data required, therefore bit31=0.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

4.8.3 CRC calculation

To check integrity of the sensor signals (SO) and commands (SI) to the sensor 3 bit CRC (cyclic redundancy check) is used. There are 27 CRC-relevant data bits (bit 31 to 5 for MOSI and bits 26 to 3 for MISO). The CRC calculation is specified by:

Polynomial = x^3 + x + 1

Initial value = 111b

Target value = 000b

4.8.4 Bosch SPI Error Management

General status flag (GS):

GS flag

Name	Name long	Activation conditions
GS	general status flag	cumulative error flag of monitor I and II register (set to '1' if at least one of the monitor flags is set and the failure condition is still present)

Note 1: The GS-flag is not set if a latched monitor flag is active but the failure mode is not present anymore (except the delay extension, see "Remark delayed GS flag"). It is also not set if SOC1 or SOC2 is active.

Monitor bits: All monitor bits stay active as long as the failure mode is present. After the failure mode disappears, latched flags (column "Latched until readout" = "yes") will be only reset to "0" after reading the monitor register at least one time. Not latched flags (column "Latched until readout" = "no") are reset to "0", once the failure mode disappears.

Monitor I Flags

Position	Name	Name long	Activation conditions	General Status Flag (GS)	General Status Flag (GS-Flag) delayed	Temporary Fault (TF)	Permanent Fault (PF)	Latched until readout
0	OC1	offset cancellation error in channel 1	set if offset cancellation of channel 1 out of limit	yes	no	yes	no	yes
1	OC2	offset cancellation error in channel 2	set if offset cancellation of channel 2 out of limit	yes	no	yes	no	yes
2	not used	not used	not used	no	no	no	no	no
3	not used	not used	not used	no	no	no	no	no
4	No CLK	no clock	set if clock of on-chip oscillator is absent	yes	no	no	no	no
5	OSC	oscillator out of limits	set if oscillator frequency out of range (has to be activated via SPI command)	yes	yes	yes	no	yes
6	OTP	memory error of OTP data	set if the content of the MEMORY has an error. This error is detected by the cyclic redundancy check.	yes	no	no	yes	no
7	Lock	lockbit error	set if at least one of the OTP lock bits is not set	yes	no	no	yes	no
8	Not used	Not used	Not used	no	no	no	no	no
9	EXT_M	Extended mode	Set if device is in extended mode (mode for internal test purpose)	yes	no	yes	no	yes
10	SOC1	slow offset cancellation channel 1	set if slow offset cancellation of channel 1 not active	no	no	no	no	no
11	SOC2	slow offset cancellation channel 2	set if slow offset cancellation of channel 2 not active	no	no	no	no	no
12	CD	capacity loss detection error	set if C-loss detection (at startup or continious) failed	yes	yes	yes	no	yes
13	ASSD	ASSD error	error detected by ASSD	yes	yes	yes	no	yes
14	ME	mirror error of device configuration data	set if filter configuration (channel 1 or 2) mirror mismatch is detected set if protocol selection mirror mismatch is detected set if voltage mode configuration mirror mismatch is detected	yes	no	no	yes	no
15	Not used	Not used	Not used	no	no	no	no	no

Monitor II Flags

Position	Name	Name long	Activation conditions	General Status Flag (GS)	General Status Flag (GS-Flag) delayed	Temporary Fault (TF)	Permanent Fault (PF)	Latched until readout
0	EOP	end of programming	end of programming command not sent	yes	no	yes	no	no
1	UVS	undervoltage error of supply VDD	set during undervoltage situation at Vdd	yes	yes	yes	no	yes
2	UVSI	undervoltage error of supply VDDI	set during undervoltage situation at Vddi	yes	yes	yes	no	yes
3	UVA	undervoltage error of regulator VDDA	set if undervoltage on analog supply (internal) is detected	yes	yes	yes	no	yes
4	GND	GND loss detected	set if GND is detected	yes	yes	yes	no	yes
5	OC_ASSD	offset cancellation error in ASSD	set if offset cancellation of ASSD out of limit	yes	no	yes	no	yes
6	Not used	Not used	Not used	no	no	no	no	no
7	Not used	Not used	Not used	no	no	no	no	no
8	FOC_Busy_CH1	Fast offset cancellation channel 1 busy	sef if fast offset cancellation channel 1 is busy	yes	no	yes	no	yes
9	FOC_Busy_CH2	Fast offset cancellation channel 2 busy	sef if fast offset cancellation channel 2 is busy	yes	no	yes	no	yes
10	FOC_Busy_ASSD	Fast offset cancellation ASSD busy	sef if fast offset cancellation ASSD is busy	yes	no	yes	no	yes
11	Not used	Not used	Not used	no	no	no	no	no
12	Not used	Not used	Not used	no	no	no	no	no
13	Not used	Not used	Not used	no	no	no	no	no
14	Not used	Not used	Not used	no	no	no	no	no
15	Not used	Not used	Not used	no	no	no	no	no

Remark to “undervoltage” flags:

No “undervoltage” flag is set: →Transmitted (sensor to ECU) acceleration data: valid

→ Transmitted (sensor to ECU) non acceleration data: valid

Any “undervoltage” flag is set: → Transmitted (sensor to ECU) acceleration data: invalid

→ Transmitted (sensor to ECU) non acceleration data: valid

Remark delayed GS flag:

If the GS-flag is triggered by an error flag, which has an influence on the signal path, the active phase of the GS-flag will be extended (see table of monitor flags "General Status Flag delayed"). The GS-extension starts after the original error is no more there and will stay active for 2.27ms for 426 Hz filter.

4.8.5 Bosch SPI Instruction Set

The Overview of 16-bit Data in Bosch SPI data frame is listed below. For “read” access only the sensor response (MOSI) is listed. For “write” access only the commands from system (MOSI) is listed.

Name	Description	Access	16 bit Data (in case of "read" commands only for sensor response; in case of "write" commands only for request)
PROT_SEL	protocol selection to switch between Bosch SPI and Open SPI	w	Hex = FF00FF00
PROG_MODE	voltage mode selection	w	0 0 0 0 0 0 0 0 0 0 0 0 voltage mode
RD_MODE	read voltage and protocol mode	r	Register CRC 0 0 0 PRO voltage mode
RD_DEVICE_ID	read device ID	r	0 0 0 0 0 0 0 0 device ID
RD_REVISION_ID	read revision ID	r	0 0 0 0 0 0 0 0 revision ID
RD_SENSOR_DATA_CH1	read sensor data of channel 1	r	S1_11 - S1_0 0 0 0 0
RD_SENSOR_DATA_CH2	read sensor data of channel 2	r	S2_11 - S2_0 0 0 0 0
RD_CAPTURED_DATA_CH2	read captured sensor data of channel 2	r	12 bit captured data channel 2 0 0 0 0
PROG_SID	write the safety ID to the assigned channel	w	0 0 0 0 0 0 SID2 SID1
RD_SID	read the safety ID to the assigned channel	r	0 0 0 0 0 0 SID2 SID1
RD_OFFSET_REG_CH1	read the register with the current offset cancellation value	r	16 bit offset data
RD_OFFSET_REG_CH2	read the register with the current offset cancellation value	r	16 bit offset data
DEMAND_OFFSET_CANCELLATION	trigger FOC/SOC	w	0 0 0 0 ASSD OC length2 OFF2 OC length1 OFF1
RD_OFFSET_CANCELLATION	read the status of the offset cancellation	r	0 0 0 0 ASSD OC length2 OFF2 OC length1 OFF1
RD_CLOCK_COUNTER	read the current value of the clock counter (captured value in case of automatic system clock monitoring)	r	16 bit clock counter
WR_CLOCK_COUNTER_MIN	write the current value of the clock counter register limit min (automatic system clock monitoring)	w	Automatic clock counter check lower limit
RD_CLOCK_COUNTER_MIN	read the current value of the clock counter register limit min (automatic system clock monitoring)	r	Automatic clock counter check lower limit
WR_CLOCK_COUNTER_MAX	write the current value of the clock counter register limit max (automatic system clock monitoring)	w	Automatic clock counter check upper limit
RD_CLOCK_COUNTER_MAX	read the current value of the clock counter register limit max (automatic system clock monitoring)	r	Automatic clock counter check upper limit
WR_CLOCK_COUNTER_FLTCNT	write the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)	w	0 0 0 0 0 0 0 0 8 bit fault threshold
RD_CLOCK_COUNTER_FLTCNT	read the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)	r	0 0 0 0 0 0 0 0 8 bit fault threshold
DEMAND_FOR_TEST	trigger build in self test	w	0 0 0 0 0 0 0 0 0 0 TMDASSD TMD2 TMD1
RD_TEST_MODE	read the status of the build in self test	r	0 0 0 0 0 0 0 0 0 0 TMDASSD TMD2 TMD1
RD_MONITOR_I_DATA	read monitor 1 data	r	Monitor flags
RD_MONITOR_II_DATA	read monitor 2 data	r	Monitor flags
WR_CONFIG_1	write configuration for filter and C-loss detection and oscillator monitoring	w	0 0 0 0 0 0 0 0 OSCM C_loss ASSD Filter_CH2 Filter_CH1
RD_CONFIG_1	read configuration for filter and C-loss detection and oscillator monitoring	r	0 0 0 0 0 0 0 0 OSCM C_loss ASSD Filter_CH2 Filter_CH1
DEMAND_SOFT_RESET	reset of the component (SO only for the first transmission)	r	Soft reset
END_OF_PROG	locking command, after EOP only read access to the configuration and test registers is possible. The only allowed write access is the "DEMAND_SOFT_RESET" command.	w	End of programming
RD_BITE_CH1	read BITE OTP value of channel 1	r	positive BITE OTP channel CH1 / negative BITE OTP channel CH1
RD_BITE_CH2	read BITE OTP value of channel 2	r	positive BITE OTP channel CH2 / negative BITE OTP channel CH2
RD_SERIAL1	read serial number bit15 - bit0	r	serial number (SN15 - SN0)
RD_SERIAL2	read serial number bit31 - bit16	r	serial number (SN31 - SN16)
RD_SERIAL3	read serial number bit47 - bit32	r	serial number (SN47 - SN32)
DEMAND_EXT_MODE	Enable Extended Mode	w	0 0 0 0 0 0 0 0 1 1 1 1 0 1 1 1
RD_EXT_MODE	read the value in register CFG_EXT_MODE	r	0 0 0 0 0 0 0 0 1 1 1 1 0 1 1 1
WR_OTP_ADDRESS	address of OTP in OTP Control-Register OTP_ADDRESS for write access	w	0 0 0 0 0 0 0 0 OTP Adress (Bit7 to BIT0)
RD_OTP_ADDRESS	Read the value in OTP Control-Register OTP_ADDRESS	r	0 0 0 0 0 0 0 0 OTP Adress (Bit7 to BIT0)
RD_OTP_DATA	OTP read based on OTP_SADDR will be triggered with read access to this register, OTP data will be available with the second read	r	OTP Content (Bit7 to BIT0) / 0 0 0 0 0 0 0 0

4.8.5.1 PROT_SEL

PROT_SEL: protocol selection to switch between Bosch SPI X"FF00FF00" and Open SPI X"00FF00FF"

SI	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

4.8.5.2 PROG_MODE

PROG_MODE: program voltage

SI	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	voltage mode				CRC			0	0
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Voltage Mode:
0010: Supply = 6.7V; SPI = 3.3V
0100: Supply =5V; SPI = 5V
1000: Supply = 3.3V; SPI = 3.3V
all other combinations = not allowed --> no voltage mode selected (SO stay in tristate)

4.8.5.3 RD_MODE

RD_MODE: read voltage and protocol mode

SI	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	Register CRC									0	0	0	PRO	voltage mode		gs	CRC

Voltage Mode:
0010: Supply = 6.7V; SPI = 3.3V
0100: Supply =5V; SPI = 5V
1000: Supply = 3.3V; SPI = 3.3V
all other combinations = not allowed --> no voltage mode selected (SO stay in tristate)

PRO:
0: Bosch SPI
1: open SPI

Reg CRC:
Contains the CRC for error detection within the configuration registers

4.8.5.4 READ_DEVICE_ID

RD_DEVICE_ID: read device ID

SI	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	gs	CRC

value fix "0x0066"

Note: The Device ID identifies the ASIC type. Any Sensor using TA660 has fixed value in Data field of 0x66hex.

4.8.5.5 READ_REVISION_ID

RD_REVISION_ID: read revision ID

SI	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SWR				MSR			gs	CRC

Revision ID consists Metal Fix Revision(MSR) and Full Mask Revision (SWR)

Note: The revision ID must not be checked against a fixed value. It can be subject to change without prior customer notification.

4.8.5.6 RD_SENSOR_DATA_CH1

RD_SENSOR_DATA_CH1: read sensor data of channel 1 (clipping auf +2047, -2047)

SI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	1	SID1					12 bit sensor data channel 1												0	0	0	0	gs	CRC

4.8.5.7 RD_SENSOR_DATA_CH2

RD_SENSOR_DATA_CH2: read sensor data of channel 2 (clipping auf +2047, -2047)

SI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	1	SID2					12 bit sensor data channel 2												0	0	0	0	gs	CRC

4.8.5.8 RD_CAPTURED_DATA_CH2

RD_CAPTURED_DATA_CH2: read captured sensor data of channel 2

SI	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	1	SID2					12 bit captured data channel 2												0	0	0	0	gs	CRC

4.8.5.9 PROG_SID

PROG_SID: write the sensor ID to the assigned channel

SI	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	SID2				SID1				CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

SID1:
00001: sensor ID for channel 1 **-->default**
SID2:
00010: sensor ID for channel 2 **-->default**

4.8.5.10 RD_SID

RD_SID: read the sensor ID to the assigned channel

SI	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	SID2				SID1				0	gs	CRC		

4.8.5.11 RD_OFFSET_REG_CH1

RD_OFFSET_REG_CH1: read the register with the current offset cancellation value (Register will be changed by FOC & SOC)

SI	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	16 bit offset data channel 1																gs	CRC	

16 bit offset data channel 1:
Conversion factor 0.5 for sensor output
example: "16 bit offset data channel 1"=200 LSB == 100 LSB sensor channel output correction value

4.8.5.12 RD_OFFSET_REG_CH2

RD_OFFSET_REG_CH2: read the register with the current offset cancellation value (Register will be changed by FOC & SOC)

SI	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	16 bit offset data channel 2																gs	CRC	

16 bit offset data channel 2:
Conversion factor 0.5 for sensor output
example: "16 bit offset data channel 2"=200 LSB == 100 LSB sensor channel output correction value

4.8.5.13 DEMAND_OFFSET_CANCELLATION

DEMAND_OFFSET_CANCELLATION: start FOC, SOC

SI	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	ASSD		OC length2		OFF2		OC length1		OFF1			CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

OFF1:
00: offset cancellation channel 1 switched off -->**default**
01: slow offset cancellation channel 1 switched on (1LSB/s)
11: fast offset cancellation channel 1 switched on
10: slow offset cancellation channel 1 switched on (1LSB/21s)

OFF2:
00: offset cancellation channel 2 switched off -->**default**
01: slow offset cancellation channel 2 switched on (1LSB/s)
11: fast offset cancellation channel 2 switched on
10: slow offset cancellation channel 1 switched on (1LSB/21s)

OC length1&2:
000: 64 samples -->**default**
001: 128 samples
010: 256 samples
011: 512 samples
100: 1024 samples
all other values have to default

ASSD:
00: offset cancellation ASSD switched off -->**default**
01: slow offset cancellation ASSD switched on
11: fast offset cancellation ASSD switched on (64 samples)

4.8.5.14 RD_OFFSET_CANCELLATION

RD_OFFSET_CANCELLATION: read the status of the offset cancellation

SI	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	ASSD		OC length2		OFF2		OC length1		OFF1		gs	CRC			

OFF1:
00: offset cancellation channel 1 switched off
01: slow offset cancellation channel 1 switched on (1LSB/s)
11: fast offset cancellation channel 1 switched on
10: slow offset cancellation channel 1 switched on (1LSB/21s)

OFF2:
00: offset cancellation channel 2 switched off
01: slow offset cancellation channel 2 switched on (1LSB/s)
11: fast offset cancellation channel 2 switched on
10: slow offset cancellation channel 1 switched on (1LSB/21s)

OC length1&2:
000: 64 samples
001: 128 samples
010: 256 samples
011: 512 samples
100: 1024 samples

ASSD:
00: offset cancellation ASSD switched off
01: slow offset cancellation ASSD switched on
11: fast offset cancellation ASSD switched on (64 samples)

4.8.5.15 RD_CLOCK_COUNTER

RD_CLOCK_COUNTER: read the current value of the clock counter register (captured value for automatic system clock monitoring)

SI	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	16 bit clock counter																gs	CRC	

Counter frequency = 2.25MHz

4.8.5.16 WR_CLOCK_COUNTER_MIN

WR_CLOCK_COUNTER_MIN: write the current value of the clock counter register limit min (automatic system clock monitoring)

SI	0	0	1	0	1	1	1	0	1	0	0	Automatic clock counter check lower limit																	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

Clock counter register min:
0…65535: lower failure threshold number of counted clocks (2.25MHz)
0 **-->default**

4.8.5.17 RD_CLOCK_COUNTER_MIN

RD_CLOCK_COUNTER_MIN: read the current value of the clock counter register limit min (automatic system clock monitoring)

SI	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	Automatic clock counter check lower limit																gs	CRC		

4.8.5.18 WR_CLOCK_COUNTER_MAX

WR_CLOCK_COUNTER_MAX: write the current value of the clock counter register limit max (automatic system clock monitoring)

SI	0	0	1	0	1	1	1	1	0	0	Automatic clock counter check upper limit																		CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

Clock counter register min:
0…65535: upper failure threshold number of counted clocks (2.25MHz)
65535 **-->default**

4.8.5.19 RD_CLOCK_COUNTER_MAX

RD_CLOCK_COUNTER_MAX: read the current value of the clock counter register limit max (automatic system clock monitoring)

SI	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	Automatic clock counter check upper limit																gs	CRC		

4.8.5.20 WR_CLOCK_COUNTER_FLTCNT

WR_CLOCK_COUNTER_FLTCNT: write the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)

SI	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	8 bit fault threshold										CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

Clock counter FLTCNT:
#=0…254: if >#failures are detected in a row, monitor flag will be set
255: limit is not effective (8 bit fault counter): deactivated oscillator monitor flag **--> default**

4.8.5.21 RD_CLOCK_COUNTER_FLTCNT

RD_CLOCK_COUNTER_FLTCNT: read the threshold for the fault counter of the clock counter monitor (automatic system clock monitoring)

SI	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8 bit fault threshold								gs	CRC		

Clock counter FLTCNT:
0…255: maximum number of failure events in row without oscillator failure flag is set

4.8.5.22 DEMAND_FOR_TEST

DEMAND_FOR_TEST: trigger build in self test

SI	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	TMDASSD		TMD2		TMD1			CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

TMD1 :
00: switch off test channel 1 **-->default**
01: pos. amplitude of test-voltage channel 1
10: neg. amplitude of test-voltage channel 1
11: not allowed --> write default value

TMD2:
00: switch off test channel 2 **-->default**
01: pos. amplitude of test-voltage channel 2
10: neg. amplitude of test-voltage channel 2
11: not allowed --> write default value

TMDASSD:
00: switch off self test ASSD **-->default**
01: pos. amplitude of ASSD
10: neg. amplitude of ASSD
11 = not defined

4.8.5.23 RD_TEST_MODE

RD_TEST_MODE:

SI	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMDASSD		TMD2		TMD1		gs	CRC	

TMD1 :
00: switch off test channel 1
01: pos. amplitude of test-voltage channel 1
10: neg. amplitude of test-voltage channel 1

TMD2:
00: switch off test channel 2
01: pos. amplitude of test-voltage channel 2
10: neg. amplitude of test-voltage channel 2

TMDASSD:
00: switch off self test ASSD
01: pos. amplitude of ASSD
10: neg. amplitude of ASSD

4.8.5.24 RD_MONITOR_I_DATA

RD_MONITOR_I_DATA:

SI	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	Monitor flags																	gs	CRC	

Detailed information of the Monitor flags is given in 4.8.4 Bosch SPI Error Management.

4.8.5.25 RD_MONITOR_II_DATA

RD_MONITOR_II_DATA:

SI	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	Monitor flags																	gs	CRC	

Detailed information of the Monitor flags is given in 4.8.4 Bosch SPI Error Management.

4.8.5.26 WR_CONFIG_1

WR_CONFIG_1: write configuration for C-loss and Osc monitoring

SI	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	OSCM		C_loss	ASSD	Filter_CH2		Filter_CH1		CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC	

Filter_CH1:
00=426Hz -->**default; all specified parameters only for 426 Hz guaranteed**
01=213Hz
10=106Hz
11= 53Hz

Filter_CH2:
00=426Hz -->**default; all specified parameters only for 426 Hz guaranteed**
01=213Hz
10=106Hz
11= 53Hz

ASSD:
0 = ASSD-monitor is not active
1 = ASSD-monitor is active -->**default**

C-loss:
0 = no initial C-loss detection running -->**default**
1 = activation of initial C-loss detection (will be reset automatically after finishing)

OSCM (oscillator monitoring mode):
00 = clock counter running and readable, disable clock counter register and oscillator monitoring flag -->**default**
01 = enable clock counter register, disable oscillator monitoring flag
11 = enable clock counter register and oscillator monitoring flag
10 = not allowed --> write default value

Note: to fulfil Safety requirements the ASSD monitor has to be set as “1”.

4.8.5.27 RD_CONFIG_1

RD_CONFIG_1: read configuration for Filter and "Abrisserkennung"

SI	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCM		C_loss	ASSD	Filter_CH2		Filter_CH1		gs	CRC		

Filter_CH1:
00=426Hz
01=213Hz
10=106Hz
11= 53Hz

Filter_CH2:
00=426Hz
01=213Hz
10=106Hz
11= 53Hz

ASSD:
0 = ASSD-monitor is not active
1 = ASSD-monitor is active

C-loss:
0 = no initial C-loss detection running
1 = initial C-loss detection is currently running (will be reset automatically after finishing)

OSCM (oscillator monitoring mode):
00 = clock counter running and readable, disable clock counter register and oscillator monitoring flag
01 = enable clock counter register, disable oscillator monitoring flag
11 = enable clock counter register and oscillator monitoring flag

4.8.5.28 WR_CONFIG_2

WR_CONFIG_2: Armingpin

SI	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	Sample Th		arming threshold								CRC			0	0
SO	TFF	TST	EOP	OVSI	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

Arming threshold:
0: arming pin in tristate / arming pin deactivated -->**default**
1...255: Arming threshold (1 LSB of arming threshold = 4 LSB of sensor data)

Arming threshold [LSB]	Sensor data [LSB]
1	4
2	8
3	12
...	...
255	1020

|data CH1| <= arming threshold => arming pin = tristate
|data CH2| <= arming threshold => arming pin = tristate
|data CH1| > arming threshold (for more than "Sample Th" times) => arming pin = low
|data CH2| > arming threshold (for more than "Sample Th" times) => arming pin = low

Sample threshold:
00: Arming pin is activated if the arming threshold is violated one time (sensor data read access)
01: Arming pin is activated if the arming threshold is violated two times (sensor data read access)
10: Arming pin is activated if the arming threshold is violated three times (sensor data read access)
11: Arming pin is activated if the arming threshold is violated four times (sensor data read access) -->**default**

4.8.5.29 RD_CONFIG_2

RD_CONFIG_2: Armingpin

SI	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	Sample Th		arming threshold								gs	CRC		

Arming threshold:
0: arming pin in tristate / arming pin deactivated
1...255: Arming threshold (1 LSB of arming threshold = 4 LSB of sensor data)

Arming threshold [LSB]	*Sensor data [LSB]*
1	*4*
2	*8*
3	*12*
...	*...*
255	*1020*

|data CH1| <= arming threshold => arming pin = tristate
|data CH2| <= arming threshold => arming pin = tristate
|data CH1| > arming threshold (for more than "Sample Th" times) => arming pin = low
|data CH2| > arming threshold (for more than "Sample Th" times) => arming pin = low

Sample threshold:
00: Arming pin is activated if the arming threshold is violated one time (sensor data read access)
01: Arming pin is activated if the arming threshold is violated two times (sensor data read access)
10: Arming pin is activated if the arming threshold is violated three times (sensor data read access)
11: Arming pin is activated if the arming threshold is violated four times (sensor data read access)

4.8.5.30 DEMAND_SOFT_RESET

DEMAND_SOFT_RESET: Soft-reset of the component; has to be sent 2 times consecutively with no other commands in between except reading CFG_SOFTRESET itself or commands with wrong CRC or wrong bit length.

SI	0	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

4.8.5.31 END_OF_PROG

END_OF_PROG: locking command, after EOP only read commands allowed, also DEMAND_SOFT_RESET

SI	0	0	1	1	1	0	0	0	1	0	0	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

4.8.5.32 RD_BITE_CH1

RD_BITE_CH1: read BITE OTP value of channel 1

SI	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	positive BITE OTP channel CH1										negative BITE OTP channel CH1						gs	CRC	

positive BITE OTP channel CH1 / negative BITE OTP channel CH1:
-128...+127: end-of-line saved BITE values in g (signed value; two's complement)
example: 0b10110100 (Bit10...Bit17) ==> -76g ==> -1216 LSB sensor output (for nom. sensitivity)

4.8.5.33 RD_BITE_CH2

RD_BITE_CH2: read BITE OTP value of channel 2

SI	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	positive BITE OTP channel CH2										negative BITE OTP channel CH2						gs	CRC	

positive BITE OTP channel CH2 / negative BITE OTP channel CH2:
-128...+127: end-of-line saved BITE values in g (signed value; two's complement)
example: 0b10110100 (Bit10...Bit17) ==> -76g ==> -1216 LSB sensor output (for nom. sensitivity)

4.8.5.34 RD_SERIAL1

RD_SERIAL1: serial number

SI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	serial number (SN15 - SN0)																gs	CRC	

4.8.5.35 RD_SERIAL2

RD_SERIAL2: serial number

SI	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	serial number (SN31 - SN16)																gs	CRC	

4.8.5.36 RD_SERIAL3

RD_SERIAL3: serial number

SI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	serial number (SN47 - SN32)																gs	CRC	

4.8.5.37 RD_OTP_DATA

RD_SERIAL3: serial number

SI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	serial number (SN47 - SN32)																gs	CRC	

4.8.5.38 DEMAND_EXT_MODE

DEMAND_EXT_MODE

SI	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

The Extended Mode is enabled after writing the specific magic code (0x7Bhex) to the field CFG_MAGIC_CODE_7B and setting CFG_EXT_M=1 in register CFG_EXT_MODE. The Extended Mode can be left by resetting CFG_EXT_M to “0”.

4.8.5.39 RD_EXT_MODE

RD_EXT_MODE

SI	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	gs	CRC	

4.8.5.40 WR_OTP_ADDRESS

WR_OTP_ADDRESS

SI	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	OTP Address (Bit7 to BIT0)								CRC			0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

4.8.5.41 RD_OTP_ADRESS

RD_OTP_ADDRESS																													
SI	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OTP Adress (Bit7 to BIT0)						gs	CRC	

4.8.5.42 RD_OTP_DATA

RD_OTP_DATA																													
SI	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC		0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	OTP Content (Bit7 to BIT0)								0	0	0	0	0	0	0	0	gs	CRC

To read a specific OTP address

- To OTP_ADDRESS register write OTP Address that needs to be read
- wait for 2 us
- Initiate OTP read access by reading OTP_READ_DATA register (ignore the response as bus architecture takes 2 read cycles to get the content of an address)
- wait for 2 us
- Read OTP_READ_DATA register (read value is value from OTP location under address set in OTP_ADDRESS register)

4.8.6 Bosch SPI timing

The Bosch SPI timing of the SMA660 is defined as follows:

- The change at output SO is forced by the rising edge of the SCK signal.
- The input signal SI is latched on the falling edge of the SCK signal.
- The data received during a write access is written to the internal registers at the rising edge of the CSB
signal, if exactly 32 SPI clock pulses have been counted during CSB = active.

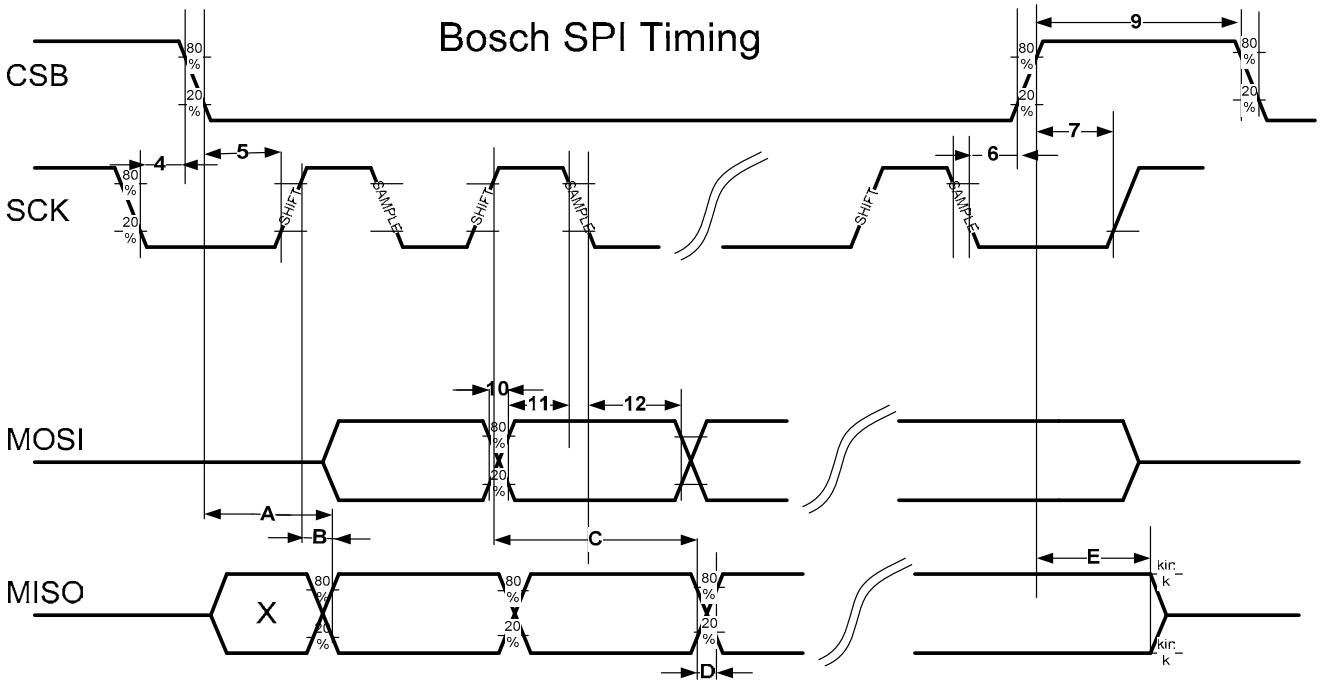


Figure 4-1 Bosch SPI Timing

The maximum SPI clock frequency that the sensor is guaranteed to be functional is provided below. This frequency must not be exceeded.

parameter / condition	Symbol	min	Nominal	max	unit	TC
SPI clock frequency (Mode2,4)	SPI_F_SCK		10	10,5	MHz	*
SPI clock frequency (Mode3)	SPI_F_SCK_5V		4	4.2	MHz	*

Slave requirements from master-point of view:

Reference in Figure 4-1	parameter / condition		symbol	min	Nominal	max	unit
A	SO data valid time (CSB) minimum drive (PLL) frequency		SPI_T_A	-		40	ns
B	SO data valid time (SCK) CL = 100 pF	Mode2 (6.7V) Mode4 (3.3V)	SPI_T_B100			32	ns
		Mode3 (5V)				80	ns
C	SO data hold time minimum drive (PLL) frequency		SPI_T_C	half clock period + switch time		-	ns
D	SO rise / fall time minimum drive (PLL) frequency		SPI_T_D	-		15	ns
E	SO data disable lag time minimum drive (PLL) frequency		SPI_T_E	-		50	ns

The table assumes a VDD_IO voltage of 3V, a capacitive load of 100 pF and the minimum drive frequency (PLL). Parameters may be better for other voltages, drive frequency and capacitive loads (as far as covered by operating condition specification)

SPI_T_A, SPI_T_B does not include the rise/fall time of CSB and SCK!

Requirements to master from slave-point of view:

Reference in Figure 4-1	parameter / condition	symbol	min	Nominal	max	unit
4	SCK disable lead time for 10 MHz mode, max load	SPI_T_4	10		-	ns
5	SCK enable lead time (CPHA = 0) for 10 MHz mode, max load	SPI_T_5_CP0	40		-	ns
5	SCK enable lead time (CPHA = 1) for 10 MHz mode, max load	SPI_T_5_CP1	95		-	ns
6	SCK enable lag time	SPI_T_6	95		-	ns

Reference **in** Figure 4-1	parameter / condition	symbol	min	Nominal	max	unit
	for 10 MHz mode, max load					
7	SCK disable lag time for 10 MHz mode, max load	SPI_T_7	10		-	ns
9	Sequential transfer delay, for read access for 10 MHz mode, max load	SPI_T_9_OS	300		-	ns
9	Sequential transfer delay, for write access for 10 MHz mode, max load	SPI_T_9_OS	450		-	ns
9	Sequential transfer delay CC32in (In case of unsuccessful write request a min. transfer delay of 310ns is required for proper generation of TFF-flag in the next frame. If this time is not observed then TFF-flag will be seen in 2nd frame) for 10 MHz mode, max load	SPI_T_9_C32	200		-	ns
10	SI rise / fall time for 10 MHz mode, max load	SPI_T_10	-		-	ns
11	SI data setup time for 10 MHz mode, max load	SPI_T_11	10		-	ns
12	SI data hold time for 10 MHz mode, max load	SPI_T_12	20		-	ns
	SCK rise / fall time	Sample / Shift	-		-	ns

Note: * To establish communication up to this frequency all other parameters in the table must be satisfied.

5 Application

5.1 Pin Out

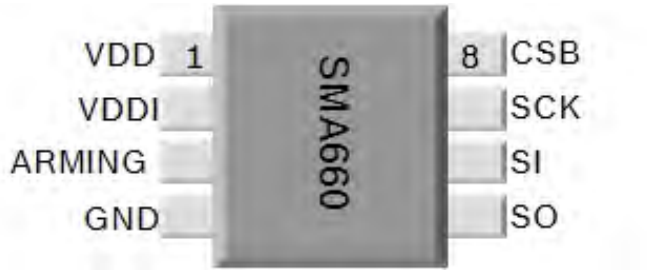


Figure 5-1 Pin-out of SMA660

Pin N°	Name	Description
1	VDD	Supply voltage (3.3V/5V/6.7V)
2	VDDI	Internal regulated voltage
3	ARMING	no Arming use: connecting to VDDI (Open SPI in 5V Mode), otherwise connecting to GND ; Arming use: connect as in **Figure** 2-14
4	GND	Ground
5	SO	Slave out
6	SI	Slave in
7	SCK	Clock signal
8	CSB	Chip select

Figure 5-2 Pin description of SMA660

5.1.1 6.7V mode

In this mode supply voltage of 6.7V (nominal) is applied and 3.3V SPI is used as a communication interface. **Figure 5-3** shows typical system setup with 6.7V supply voltage. If Arming is required Arming Pin should connect over a resistor to VDD (see **Figure** 2-14). The SO-Voltage-Level is derived from VDDI.

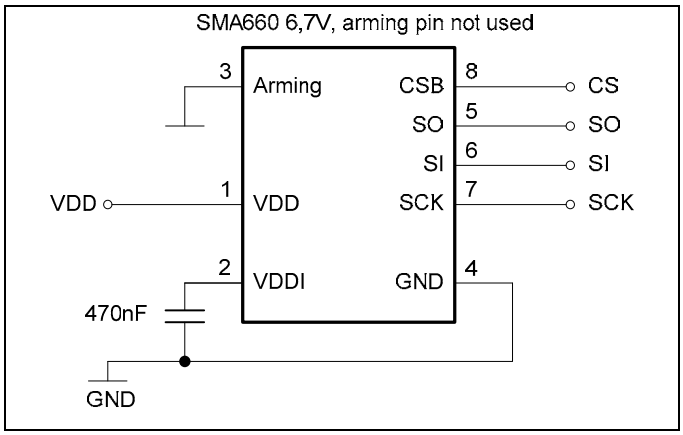


Figure 5-3 Typical system setup using SMA660 sensors with 6.7 V supply voltage.

5.1.2 5V mode

In this mode a supply voltage of 5V (nominal) is applied and 5V SPI is used as a communication interface. **Figure 5-4** and **Figure 5-5** shows typical system setup with 5V supply voltage. If Arming is required Arming Pin should be connected over a resistor to VDD (see **Figure** 2-14). The SO-Voltage-Level is derived from VDD.

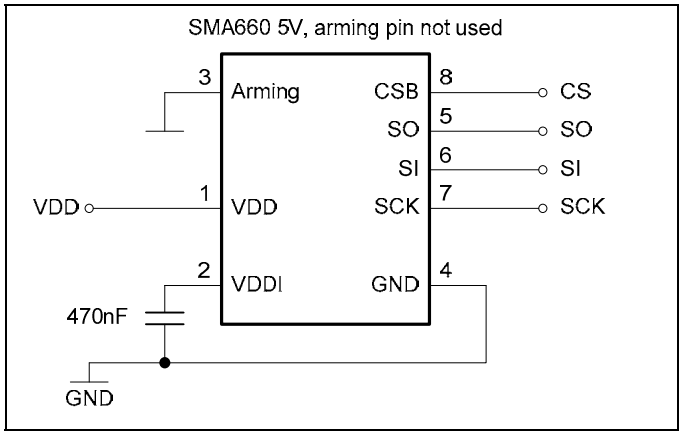


Figure 5-4 Typical system setup using SMA660 sensors with 5 V supply voltage (Bosch SPI).

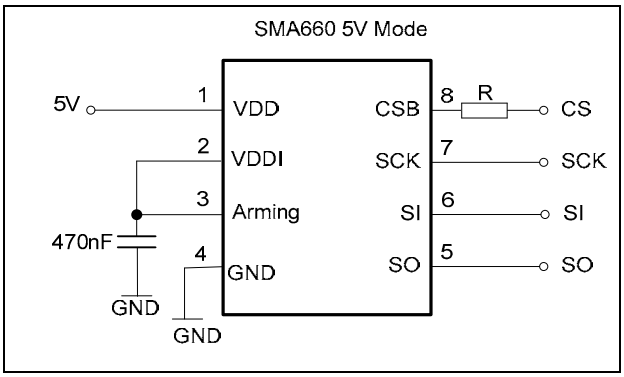


Figure 5-5 Typical system setup using SMA660 sensors with 5 V supply voltage (Open SPI)

5.1.3 3.3V mode

In this mode supply voltage of 3.3V (nominal) is applied and 3.3V SPI is used as a communication interface. Figure 5-6 shows typical system setup with 3.3V supply voltage. If Arming is required Arming Pin should connect over a resistor to VDD (see **Figure** 2-14). The SO-Voltage-Level is derived from VDDI.

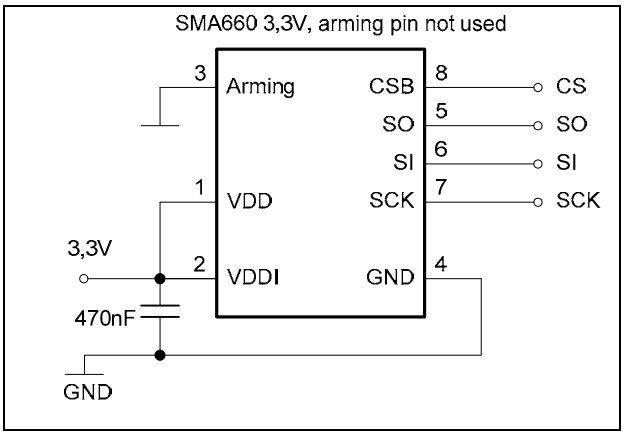


Figure 5-6 Typical system setup using SMA660 sensors with 3.3 V supply voltage

5.2 External Components

The SMA660 SOIC8 sensor module requires an external Capacitor with 470nF (min. 220 nF and max. 1300 nF) for 5V & 6.7 V mode on VDDI for EMC/ESD protection, supply filtering and for the internal supply voltage. It is not necessary to place a second capacitor parallel to C_VDDI to meet Safety-requirements for single-point-sensing. However, the system should take measures against C-loss during operation (e.g. redundancy of capacitors) to guarantee PSRR, EMV and noise performance.

For the 3.3V-application, a capacitor on VDDI is not necessarily required to fulfil the specified performance. Anyhow, the airbag-ECU has to ensure that the voltage-noise on the supply line is low enough (i.e. PSRR*, EMC**, noise**, low voltage detection and so on).

*) PSRR has been measured during characterization. The amplitude of the disturbance is regulated to a fixed value (specification in LSBpp/mV; absolute PSRR caused noise can be calculated)

**) During the EMC-measurement and characterization, the standard capacitor is 470nF

Symbol	Condition	min	Nominal	max	unit
C_VDDI	external capacitor at VDDI	220	470	1300	nF
R	CSB line (Open SPI 5V mode)	900	1000	1100	Ohm

Application Hint:

It is recommended to place the capacitors very close to the SMA660.

Proper function of the sensor in the overall system must be validated by the customer.

In any case, the electrical stability (power supply and EMC) of each system design including the SMA660 must be evaluated in advance to guarantee proper functionality during operation.

5.2.1 C-loss detection

In order to detect the loss of the VDDI capacitor, the discharging behaviour of the capacitor is monitored: if the capacitor is present, discharging will be slowly, whereas an absent capacitor causes a quick voltage drop. In the second case, the VDDI regulator is switched off and the VDDI capacitor will discharge.

If a C-loss is detected the sensor goes into a reset.

Please note that the C-loss detection does only work for 5V & 6.7V mode (not 3.3V mode).

6 Parameter Specification

6.1 General information

For SMA660, only 426Hz filter setting is released. All parameters defined here are only valid with 426Hz filter setting.

Parameters designated as Critical Characteristics or Significant Characteristics (“Besondere Merkmale”) by customers are marked with “/S/C”.

6.2 Absolute Maximum Ratings

Any values beyond the given values may seriously damage the device. The sensor must be discarded when exceeding these limits.

Parameter	Symbol	Condition	Min	Nominal	Max	Unit
Storage Temperature	T_STORAGE		- 55		+ 150	°C
Drop Height			1.5			m
Supply Voltage	VDD		-0.3		18	V
maximum voltage at VDDI relative to GND	VDDI		-0.3		3.6	V
voltage at SI, SCK, CSB and SO in tristate relative to GND	V_SPI		-0.3		5.5	V
Mechanical Shock *1)		t < 0.5ms			2000	g
ESD – Voltage (any Pin)		HBM (acc. AEC-Q100) *2)	+/-2.0			kV
		MM (acc. AEC-Q100) *3)	+/-0.2			kV
		CDM (acc. AEC-Q100)	+/-0.5			kV
ESD – Voltage (corner pins)		CDM (acc. AEC-Q100)	+/-0.75			kV
Storage Temperature Gradient*4)		ΔT/Δt			20	K/min

1) Care should be taken to avoid damage of device during handling. Drops onto hard surfaces may cause shocks larger than 4000g which is far beyond the defined absolute maximum rating of the device.
2) The test condition also complies with IEC61340-3-1.
3) The test condition also complies with IEC61340-3-2.
4) Soldering process is specified separately.

6.3 Operating Conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply Voltage	3.3V mode	VDDI	3.13	3.3	3.47	V
	5V mode	VDD	4.75	5	5.25	V
	6.7V mode	VDD	6.15	6.7	7.15	V
Internal Clock Frequency		f_{clk}	-5%	18	+5%	MHz

Parameter		Symbol	Min	Nominal	Max	Unit
Power-on slew rate (VDDI for 3.3V and VDD in 5V & 6.7V mode)			0.5*E-6		1	V/µs
Operating Temperature Range		T_A	-40		+125	°C
Operating Temperature Gradient		$T_A/\Delta t$			6	K/min
Current consumption (with internal frequency of 18MHz, and SCK inactive) (/S/C)	3.3V mode	I_{VDDI}	2.7		4.9	mA
	5V mode and 6.7V mode	I_{VDD}	3.2		4.9	mA
Inrush/Startup Current C_{VDDI}= 220nF~1300nF, $T_{startup}$ <= 1ms	3.3V mode	I_{VDDI}			60	mA
	5V mode	I_{VDD}			80	mA
	6.7V mode	I_{VDD}			92	mA
Input capacities (CSB, SI, SCK) (no external capacitive load, value without package, measured on wafer level)			1		6	pF
Output capacities SO-pin in tristate					6	pF
Operation time (powered operating hours					15 000	h
Start-up cycles					150 000	
External Capacitance @VDDI		@ 5V mode and 6.7V mode	220	470	1300	nF

The technical development/application of the product is limited to a life expectancy of 15 years and a maximum of 15000 hours of operation.

6.4 Functional Characteristics

The parameters in the following table are valid under the operation conditions defined in chapter 6.3 unless noted otherwise. They are also valid after further processing according to the given soldering process (Chapter 9.6) and milling process (Chapter **Fehler! Verweisquelle konnte nicht gefunden werden.**) in the further fabrication.

All the following parameters include voltage, temperature and lifetime effects if not noted otherwise. For the parameters as far as sensitivity, cross axis sensitivity and BITE is concerned is evaluated in mean value, i.e. the noise effect is excluded.

Parameter	Condition / Remark	Min	Nominal	Max	Unit
Full Scale Dynamic Range [1)]			+/-128		g
Sensitivity at 0Hz			16		LSB/g
Tolerance of Sensitivity (/S/C) [2) 7)]		-5		5	%
Nonlinearity of Sensitivity (F.S.) [7)]	Best fit straight line	-2		2	%
		-2.56		+2.56	g
Nonlinearity of Sensitivity (+/-5g) [7)]		-2		2	%
		-100		100	mg
Cross Axis Sensitivity of SMA [3)]		-3.5		3.5	%

Parameter	Condition / Remark	Min	Nominal	Max	Unit
Cross Axis Sensitivity of SMA after soldering on PCB (only for internal customers) [9)]		-3.6		3.6	%
Resolution of Sensor Output		-	12	-	Bit
Absolute Accuracy of Sensor Output[7)]		-	1	-	LSB
Short term Offset[7)]	Moving Average out of 10 samples on a data basis of 2k Samples while SOC is running.	-3.2	0	3.2	LSB
Offset (/S/C) (Zero acceleration Offset mean Value, incl. Drift over temperature and supply voltage) [7)]	Mean value while continuous offset cancelation running for SOC (1 LSB/s) [4)]	-0.5	0	+0.5	LSB
	Mean value while continuous offset cancelation running for XSOC (1 LSB/21s) [4a)]	-0.5	0	+0.5	LSB
Noise (Sigma) [4) 4a) 7) 10)]		0		1.06	LSB
Noise (peak to peak) [4) 4a) 7) 10)]		0		8.4	LSB
Noise Peak to Peak under PSRR (at Harmonics of ½ $f_{\Sigma\Delta converter}$; ½ $f_{\Sigma\Delta converter}$ =140 kHz) [7)]	6.7V Mode and 5V mode; Capacitor at V_{ddi}=470nF; DC=4.7V; AC=+/-170mV			0.05	LSB/ mV
	3.3V Mode; Capacitor at V_{ddi}=10nF; DC=3.3V; AC=+/-170mV			0.25	LSB/ mV
Offset under PSRR (at Harmonics of ½ $f_{\Sigma\Delta converter}$; ½ $f_{\Sigma\Delta converter}$ =140 kHz) [7)]	6.7V Mode and 5V mode			0.003	LSB/ mV
	3.3V Mode			0.025	LSB/ mV
3dB corner frequency of sensor (Both effects from sensing element and ASIC are considered) [8)]	426Hz mode (426Hz is f_{3dB} of FIR filter)	384.8 (-5%)	405	425,3 (+5%)	Hz
	213Hz mode [6)] (213Hz is f_{3dB} of FIR filter)	200,2 (-5%)	210,4	220,7 (+5%)	Hz
	107Hz mode [6)] (107Hz is f_{3dB} of FIR filter)	101,7 (-5%)	107	112,3 (+5%)	Hz
	53Hz mode [6)] (53Hz is f_{3dB} of FIR filter)	51,2 (-5%)	53,9	56,6 (+5%)	Hz
Positive BITE of channel X and Y [5) 7)]	Absolute value	732	1220	1708	LSB

Parameter	Condition / Remark	Min	Nominal	Max	Unit
(/S/C)		(-40%)	(0%)	(+40%)	
Negative BITE of channel X and Y [5) 7)] (/S/C)	Absolute value	-1610 (-40%)	-1150 (0%)	-690 (+40%)	LSB
Positive BITE of channel X and Y [5) 7)] (/S/C)	Relative to stored BITE value	(-12%)	stored value	(+12%)	LSB
Negative BITE of channel X and Y [5) 7)] (/S/C)	Relative to stored BITE value	(-12%)	stored value	(+12%)	LSB
Self test build-up/turn off time for channel X and Y (Deviation from final value < 2%)			2	3	ms
Turn-on time (time between power on and ready to run, V_{min} @ VDDI is reached)	5V mode; 6.7V mode (VDD_Slope of 5.5V/ms)			5	ms
	3.3V mode (VDDI_Slope of 2.6V/ms)			2	ms
Total signal run time (internal time). [8)]	Time delay between input and output signal (426Hz Filter)		1.15	1.21	ms

1) The full scale range is guaranteed once the offset is adjusted to 0 LSB.
2) In % of nominal sensitivity; over lifetime, defined temperature and supply Voltage range.
3) Output signal due to acceleration in any axis perpendicular to the sensing axis, limits refer to 3 sigma values
4) Test condition: 10k data samples (5 SOC-Cycles) measured with the 426 Hz filter configuration, nominal supply Voltage, SOC on. Peak to peak values of sensor are within +-4σ of data samples.

4a) Test condition: 168k data samples (4 XSOC-Cycles) measured with the 426 Hz filter configuration, nominal supply Voltage, SOC on. Peak to peak values of sensor are within +-4σ of data samples.

5) Considering process tolerances, lifetime drift, ratiometric behaviour and temperature coefficient.
6) Not released, only for internal evaluations.
7) Guaranteed with at least 4 Sigma over lifetime.
8) Guaranteed through design with at least 4 Sigma.
9) The Cross Axis Sensitivity of SMA at soldering on PCB is mainly dependent on the pick and place tolerance. The limit is defined basing on the actual data for P&P head of ASM at Bosch. It is not verified for other pick and place machine.
10) Adjustment of noise limits during final sensor test needs internal customer approval. The parameter is tested for all sensors.

6.5 Electrical Characteristics

The SPI input pin has internal pull-up resistors of nominal 100 kOhm from input to VDDI with 3.3V & 6.7V mode. The SPI input pin has internal pull-up resistors of nominal 100 kOhm from input to VDD with 5V mode.

Parameter @ 3.3V SPI	Condition / Remark	Min	Nominal	Max	Unit
Input Hi Voltage of CSB, SI, SCK (/S/C)	VDDI between min/ max values	0.7*VDDI		VDDI	V
Input Lo Voltage of CSB, SI, SCK (/S/C)	VDDI between min/ max values	0		0.3*VDDI	V
Input voltage hysteresis at CSB, SCK, SI (/S/C)	VDDI between min/ max values	0.2			V
Capacity at Input pins(CSB, SI, SCK)	no external capacitive load, value without package, measured on wafer level	1		6	pF
Output Hi Voltage of SO (/S/C)	VDDI between min/ max values ; IOUT=+/-2mA	0.8*VDDI		VDDI	V
Output Lo Voltage of SO (/S/C)	VDDI between min/ max values ; IOUT=+/-2mA	0		0.2VDDI	V
Capacity load at SO 10MHz SPI				100	pF
Output capacity SO at high impedance state				6	pF
Input low current (internal pull-up + leak current) at CSB, SI, SCK		-42		-27	µA
Input high current at CSB, SI, SCK	VDDI between min/ max values	-10		10	µA
Output current during high impedance state at SO pin	VDDI between min/ max values	-10		10	µA
Voltage range of VDDI for 6.7V Mode	(VDDI is an output) full specification for sensor evaluation	3.13		3.47	V
Voltage range of VDDI for 3.3V Mode	(VDDI is an input) full specification for sensor evaluation	3.13		3.47	V

Parameter @ 5V SPI	Condition / Remark	Min	Nominal	Max	Unit
Input Hi Voltage of CSB, SI, SCK (/S/C)	VDD between min/ max values	0.7*VDD		VDD	V
Input Lo Voltage of CSB, SI, SCK (/S/C)	VDD between min/ max values	0		0.22*VDD	V
Input voltage hysteresis at CSB, SCK, SI (/S/C)	VDD between min/ max values	0.2			V
Capacity at Input pins(CSB, SI, SCK)	no external capacitive load, value without	1		6	pF

	package, measured on wafer level				
Capacity load at SO 4MHz SPI				100	pF
Output Hi Voltage of SO (/S/C)	VDD between min/ max values ; IOUT=+/-2mA	0.8*VDD		VDD	V
Output Lo Voltage of SO (/S/C)	VDD between min/ max values ; IOUT=+/-2mA	0		0.2 * VDD	V
Output capacity SO at high impedance state				6	pF
Input low current (internal pull-up + leak current) CSB, SI, SCK		-63		-41	uA
Input high current at CSB, SI, SCK	VDD between min/ max values	-10		10	µA
Output current during high impedance state at SO pin	VDD between min/ max values	-10		10	µA
Voltage range of VDDI for 5V Mode	(VDDI is an output) full specification for sensor evaluation	3.13		3.47	V

7 Safety

SMA660 sensor is developed according to ISO26262 [4] for application in ASIL D airbag systems. According to ISO26262 a comprehensive safety concept that combines monitoring concepts with innovative, state-of-the-art technologies for SMA660 was created and implemented in SMA660. Furthermore to identify the critical paths and to verify the integrity of the safety concept a detailed failure tree analysis to support the development process was employed.

The complete safety concept is only valid when all safety relevant monitors are activated and evaluated during startup and operation, such as oscillator monitor, C-loss monitor, overvoltage monitor, undervoltage monitor, GND_loss monitor, Mirror Error monitor, OC_ASSD monitor and ASSD monitor. See details in chapter 4.7.4 und 4.8.4.

The ASSD channel is activated by default. It needs neither activation nor evaluation from the system (customer). If the signal path is disturbed, or the ASSD signal exceeds its limits, ASSD error counter is incremented. When the counter reaches its limit, an error code will be released. The acceleration signal has to be discarded. (More details regarding ASSD in section2.7).

Besides BITE tests of acceleration channels (see section 2.3) must be initiated at start up and evaluated in order to check the functionality of the sensor element and the complete signal path.

In order to ensure a correct transmission/ communication between system and sensor, the CRC Error of SPI communication at SO has to be checked all the time in the system.

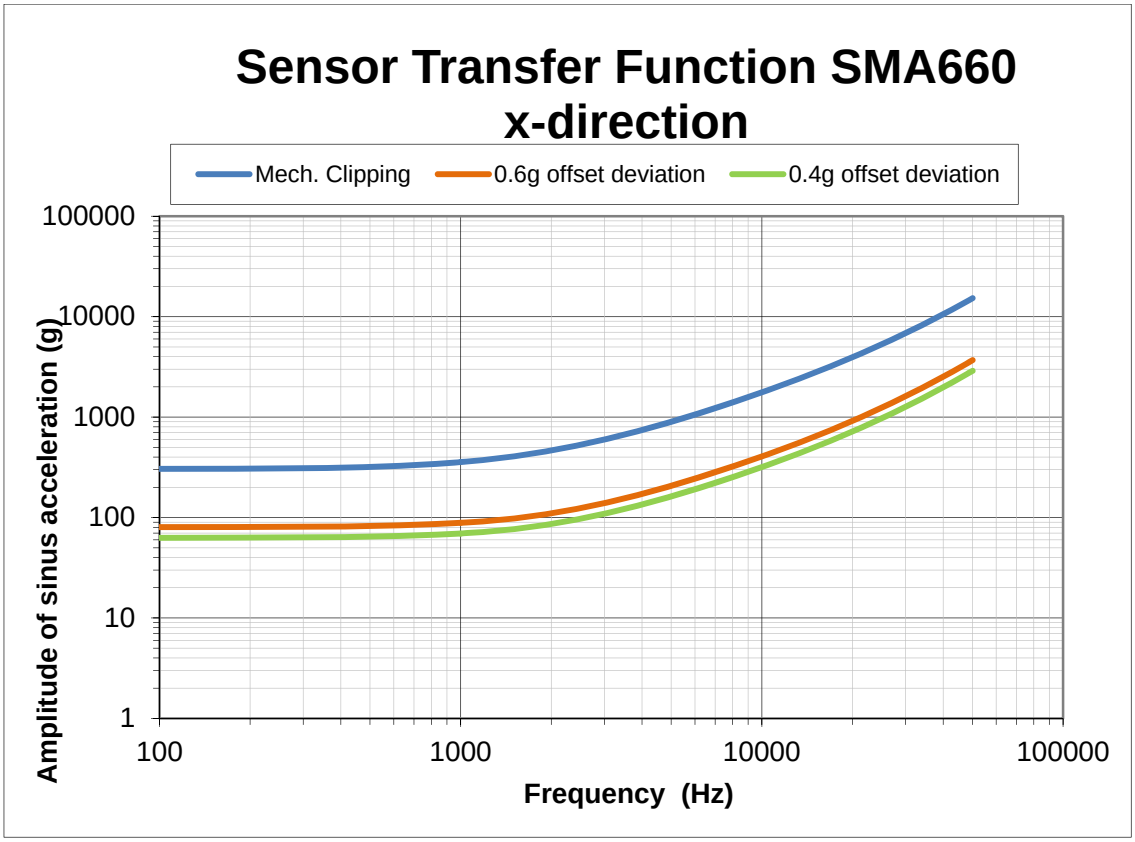
In general, a failure flag indicates that the acceleration signal is not valid. For example: GS=1 or NRO=1, or monitor I and monitor II flags.

Moreover, if a BITE-Error (BITE out of Limit) or Offset cancellation- Error (OC1 Monitor or OC2 Monitor only detected in one channel, it doesn't naturally mean that the other channel still works properly. As BITE and FOC are not activated repeatedly all the time, in this case, the sensor signal from both channels has to be discarded due to safety reasons.

8 Sensor Transfer function

Due to non-linearity of the signal path an offset deviation under some circumstances (e.g. vibration) may occur before mechanical clipping. The following diagrams show the maximum acceleration that could be applied with an offset deviation of |±0.4g| and |±0.6g| in the sensing direction (see Figure 6.5). Simulation results are verified.

The worst case curve is simulated under consideration of different CMB process deviations of 4 Sigma. As input of the simulation a sinusoidal acceleration stimuli with mean = 0 is used. If an additional static acceleration (acceleration at 0Hz) is applied the maximum acceleration will be lower than given.



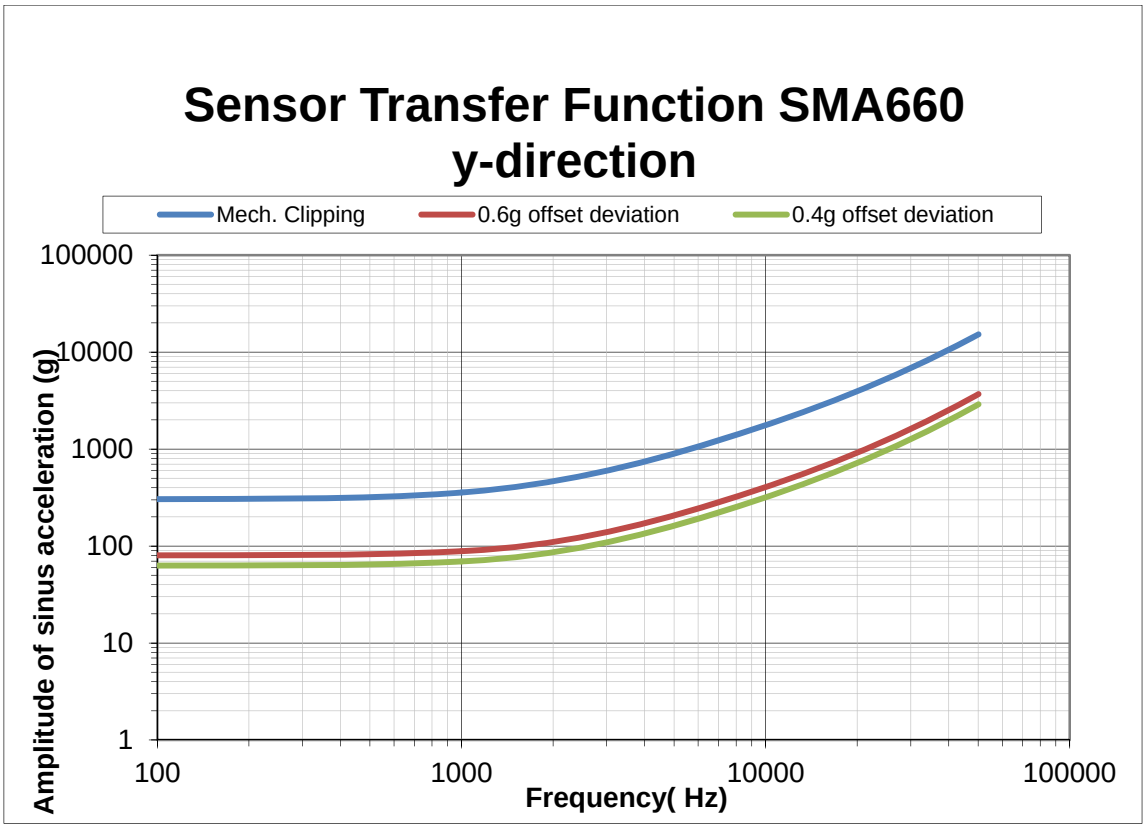


Figure 6.5 Sensor Transfer Function SMA660 for x- and y-direction (Ch1 and Ch2)

9 Handling and Storage

Micro-mechanical sensors are designed to sense acceleration with high accuracy even at low signal amplitudes and contain highly sensitive structures inside the sensor element. The sensors are protected against mechanical shock up to several thousand "g"s. However, these limits can be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping of the sensor onto hard surfaces, torque limiters, etc. Suitable ECU mounting tools must be used.

We recommend establishing a defined and qualified installation process when processing sensors to prevent g-forces in excess of 4000g during transport, handling and mounting of the sensors.

Standard ESD guidelines must be respected during handling & transport (for specified ESD values see chapter 6.2). The sensor must not be handled as bulk good.

Recommendations for the assembly in further production processes are addionally described in Application Note SMA6 [5].

9.1 Package

The SMA660 sensor is packaged in an 8-Pin narrow SOIC housing. The mechanical and electrical specifications of the housing correspond to JEDEC Publication N° MS-012F, Release August 2008. The SMA660 is a lead-free component according to RoHS “Restriction of the use of certain hazardous substances” (DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment).

9.2 Package dimensions

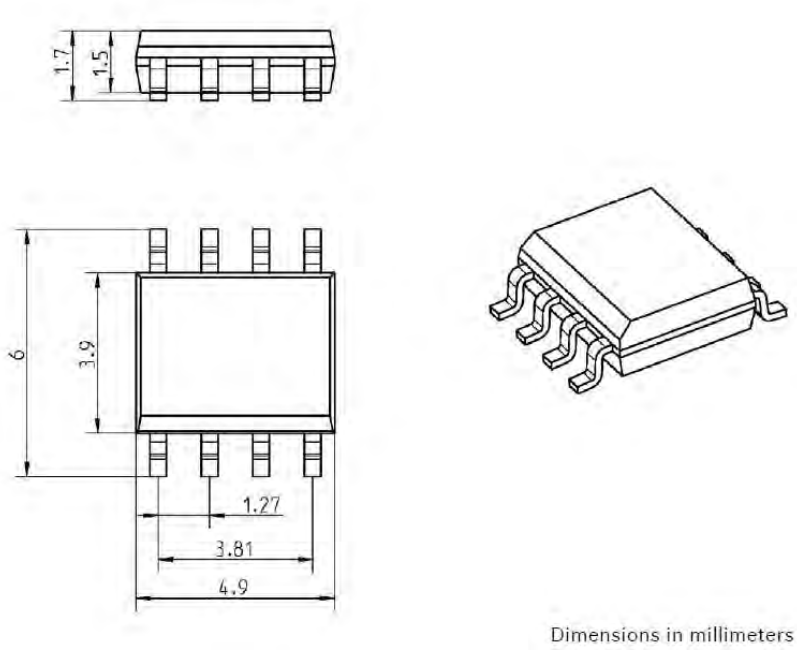


Figure 9.1 Package dimensions 8-pin narrow SOIC housing

9.3 Moisture sensitivity level

The processability of SMA660 sensors corresponds to JEDEC Level 1 (MSL 1). See also

- J-Std-020A IPC/J_STD_020 “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices” [2]

- IPC/J-033 “Standard for Handling, Packaging, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices” [3]

9.4 Storage time and Life time in Vehicles

SMA660 is qualified according to the following temperature profiles for storage and Life time.

Storage time of sensor (after production, before soldered on ECU)

Approx. 1 year

Temp.[°C]	-55 ~ 10	10 ~ 40	40 ~ 70
Duration [h]	50	8660	50
Total [h]	8760		

Storage time on ECU (after soldered on ECU, before mounted in Vehicles)

Approx. 15 years

Temp.[°C]	-55 ~ -40	-40 ~ 10	10 ~ 30	30 ~ 70
Duration [h]	50	500	130800	50
Total [h]	131400			

Operating lifetime (i.e. with supply voltage turned on in Vehicles)

Approx. 2 years

Temp.[°C]	-40	-20	25	60	80	100	125
Duration [h]	300	1500	3600	5100	3600	750	150
Total [h]	15000						

Non-operating lifetime in ECU (i.e. with supply voltage turned off in Vehicles)

Approx. 15 years

Temp.[°C]	-40 ~ 20	20 ~ 40	40 ~ 60	60 ~ 80	80 ~ 85	85 ~ 135
Duration [h]	73656	26784	20088	12053	1339	0
Total [h]	133920					

According to the temperature profiles above, SMA660 has a storage time of 16 years (Storage time of sensor + Storage time on ECU) in total. When it is mounted in vehicles, a lifetime of 17 years (Operating lifetime+ Operating lifetime) is expected.

The storage conditions have an influence on the lifetime of sensors. Different Storage Conditions will result in different maximum storage time.

Under a typical storage condition such as in Table 9-1, SMA660 has a maximum of storage time of 157,282 Hours, approximately 18 years.

Storage Conditions	Temperature	Storage Time	
Temperature	-40°C ... 10°C	<1%	100 h
	10°C ... 30°C	>99%	156632 h
	30°C ... 70°C	<1%	550 h
	Total	**100%**	**157282 h**

Table 9-1 Storage Conditions Temperature profile 1

If the storage condition is as shown in Table 9-2, SMA660 has then a maximum storage time of 131.400 Hours, approximately 15 years.

Storage Conditions	Temperature	Storage Time	
Temperature	-40°C ... 10°C	< 0,1%	100 h
	10°C ... 25°C	70%	92.000 h
	25°C ... 30°C	20%	26.300 h
	30°C ... 40°C	< 10%	12.900 h
	40°C ... 90°C	< 0,1%	98 h
	90°C ...130°C*)	< 0,0015%	2 h
	Total	**100%**	**131.400 h**

Table 9-2 Storage Conditions Temperature profile 2

*) 2h at 90°C to 130°C is the max. paint repair temperature

Deviations to the above Temperature profiles have to be evaluated again by RB-internal reliability experts.

9.5 Laser Marking

Each SMA660 is uniquely identifiable and traceable through Laser marking on package and serial number in OPT.

The laser marking of SMA660 is shown in Figure 9-2. The marking encodes the following information:

- **131:** the Last three digits of SMA660 part number
- **Y:** Date Code - Production year with modulo 36

  2010=0
  2011=1
  ...
  2020=A
  2021=B
  ...
  2045=Z
- **WW:** Date Code - Work week
- **CC:** 2 alphanumeric digits, Combined information of packing provider and lot Counter. Lot counter is package specific. Reset every work week.

There is no special marking point for Pin 1. It can be identified according to the chamfer position on the package as shown in Figure 9-3, which is defined in JEDEC Publication N° MS-012F.

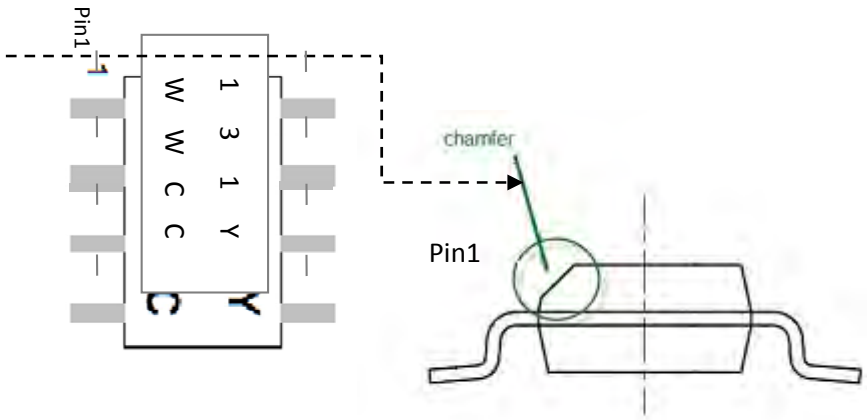


Figure 9-4 Laser Marking and Pin 1 identification

9.6 Tape and reel

Embossed tape and reel is used for presenting devices to pick-and-place machines for automatic placement onto printed circuit board. SMA660 is delieved in tape and reel in order to prevent it from physical and electro-static discharge damage during shipping and storage.

The pin orientation shall be consistent for all devices in the tape and this orientation must be valid for all tapes as shown in Figure 9-5.

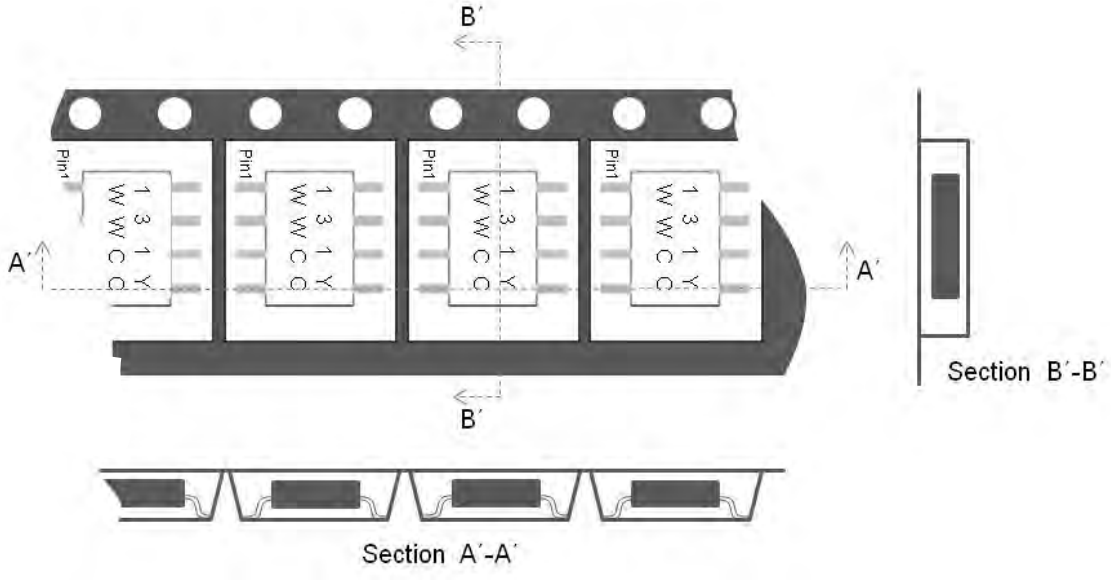


Figure 9-5 Pin Orientation in tape

9.7 Soldering Process

The housing is released for a soldering stencil thickness of 120µm and 150µm. For mounting SMA660 onto a PCB, a lead-free reflow-soldering profile has been qualified, which is released for max. 3 reflow soldering cycles. This profile is adequate both for using a lead-containing soldering process as well as for using a lead-free soldering process. The temperature profile for reflow soldering of SMA660 is given in Figure 9-6 and in the table below. Repair and manual soldering of the sensor is not permitted. Sensor specific tests over

temperature or at a non ambient temperature (~25°C) after soldering are not necessary to achieve any performance or quality goals [1].

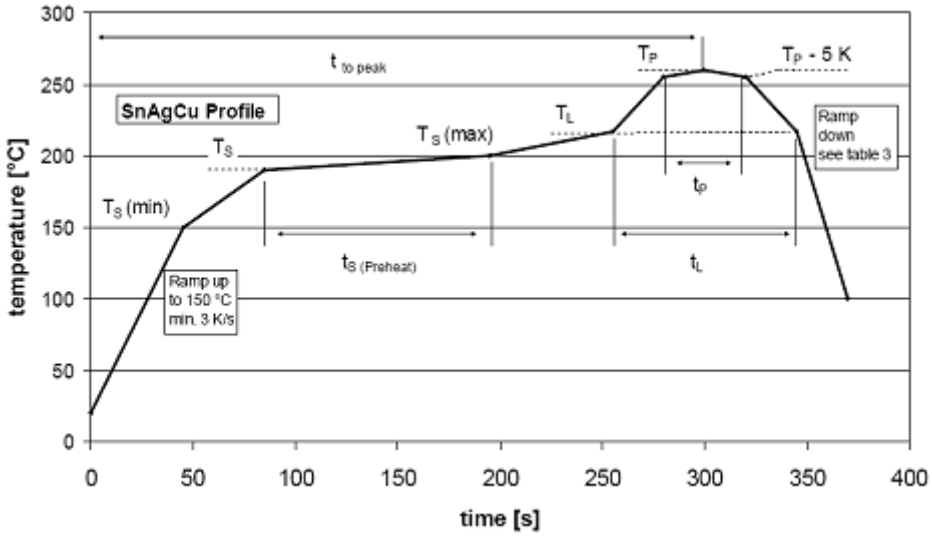


Figure 9-6 Reflow-soldering profile used for SMA660 qualification

(Both for lead-containing and lead-free soldering processes)

Reflow-Soldering Temperature Profile used for Qualification			
Profile Features	Abbreviation	Value for SOIC8	Comment
Preheat			
Ramp-up rate 20 °C to 150 °C		min. 3 K/s	***1) *2)**
Soak Temperature	T_s(min)	min. 150 °C	***2)**
Soak Temperature	T_s	190 °C	
Soak Temperature	T_s(max)	Max. 200 °C	
Soak Time (time from T_s to T_s(max))	$t_{s(preheat)}$	min. 110 s	***2)**
Time between T_s(max) and T_L		10 – 85 s	
Peak			
Ramp-up rate from 200 °C to T_{peak}		0.5 K/s to 3 K/s	***1)**
Liquidus Temperature	T_L	217 °C	
Time above T_L	t_L	min. 90 s	***2)**
Peak Temperature	T_P	260 (-0) °C	
Time within 5 K of T_P / Time above T_P – 5 K	t_P	min. 40 s	***2)**
Cooling			
Ramp-down rate from T_P		-6 K/s	***3)**
General			
Time to T_P	$t_{to\ peak}$	min. 300s	***2)**

***1)** averaged over 10 s

***2)** These values are minimum values used for qualification. Consequently, the values used in production shall be smaller than these values!

***3)** to be fulfilled over at least 10 s in the cooling zone

10 Coating over SMA660

For SMA660, the following coatings over SMA660 are evaluated regarding the chemical compatibility.

- SL1301 (PU) from Lackwerke Peters GmbH + Co KG
- SEMICOSIL 942 UV A / B (silicone) from Wacker Chemie AG
- HumiSeal 1B51NSLU/521EU PB60 from Humiseal

As far as the two types of coating are concerned, they are chemically compatible with the SO8 (molding compound + lead frame leads).

However, the mechanical stability of a coated SMA660 in any system must be evaluated in advance to ensure the proper functionality during operation. The sensor performance is not guaranteed for any kind of coating.

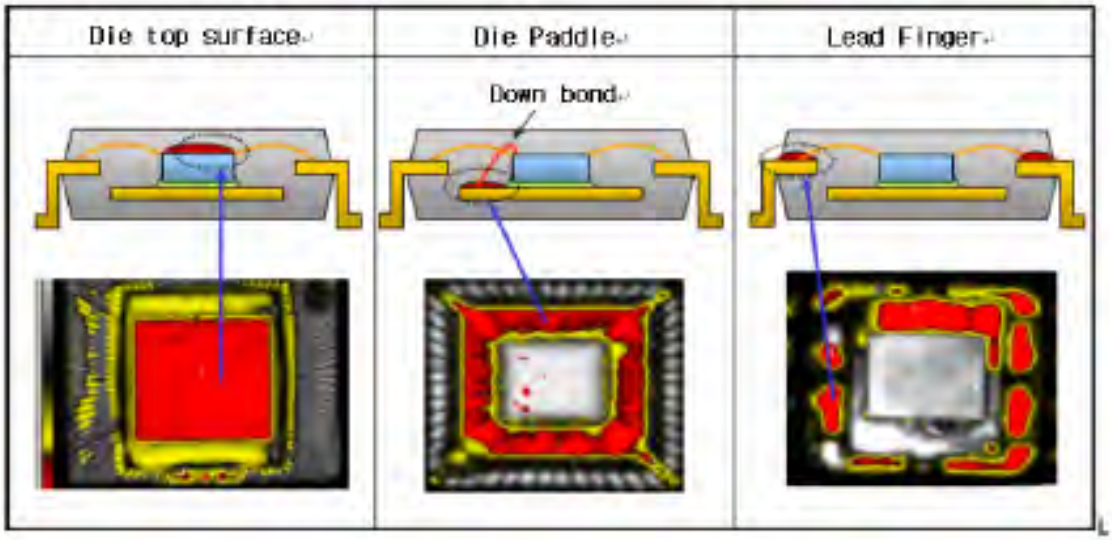
11 Delamination free variants

Delamination free variant of SMA660 is developed on request of external customer in compliance with HKMC Specification ES90000-02 (Establishment 2005.06.30).

Delamination criteria of parts (after SMD-process) according to HKMC Specification ES90000-02 is defined in the following table:

[Table 1. Delamination Criteria]

Delamination area		Criteria
Top	Die Top Surface	Reject
Lead finger	With 2nd bond	Reject
	Other area	Accept
Die paddle	With down bond	Reject
	Without down bond	Accept



12 Documents and standards

[1] Verfahrensvorschrift Fertigung 1 269 918 512 (18.11.2008)

[2] J-Std-020A IPC/J_STD_020 “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices”

[3] IPC/J-033 “Standard for Handling, Packaging, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices”

[4] ISO 26262:2011, *Road vehicles — Functional safety*

[5] Application Note SMA6