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1. Prolog

F01_7758

This document describes properties, functions and target performance of the combined angular rate and acceleration sensors SMI700 and SMI710 for the specified ambient condition defined within the SMI7-Project. It is derived from the requirement specification [01]. Each sensor is a sensitive micro-machined measuring device with high accuracy and reliability, especially designed for detection of angular rate and acceleration in automotive applications. In these applications, the sensors are usually soldered on a printed circuit board (PCB) inside an electronic control unit or similar device. The ECU is typically applied inside the passenger compartment, e.g. the transmission tunnel, underneath the passenger seat or inside the luggage compartment. For ESPi, the ECU is typically applied inside the engine compartment or hydraulic unit.

All sensor parameters are valid / guaranteed over a specified range of all relevant influence factors such as temperature, supply voltage, lifetime, humidity, vibration. Up to now temperature, supply voltage, (life-) time and humidity are known as influence factors towards the sensor performance. Especially, interactions between PCB and component have to be taken into account. To prove the functions customer orientated test devices (like DKT-shuttles made of R1566 (= FR4)) are designed as similar to target application as possible.

Interaction between up to 4 sensor module on one PCB (e.g. driving frequency modes couples into another SMI7 sensor module which leads to offset variations) is prevented by design. Self excitation are covered by design of the sensor. The sensor withstands common vibration sources as SMD elements giving vibration to the sensor by relaxing over time and temperature ("knackende Bauelemente") as far as covered by the current target vibration specification.

Description of the way key parameters are proved is described in chapter 08a "Measurement and Validation". For every parameter test cases are described to prove if development objectives for a certain parameter are fulfilled or not. Assumed boundary conditions (e.g. max. warpage of PCB, electronic circuitry ...) to reach given sensor performance are defined in this document. These conditions are recommended; deviations can lead to limited sensor performance. Development of an additional damper housing is not part of this project. Repair and manual soldering of the sensor is not permitted. The development of the devices is based on this signed document. Changes within the requirements/targets that occur during the project are handled within the project management by change requests. For this specification, 1G equals to 9.81m/s^2 .

F01_9392

Customer demands, which cannot be fulfilled according to sensor developers' estimation are given in brackets. If final characterization results show a better sensor performance than specified in the customer demands, the real performance will be noticed in datasheets.

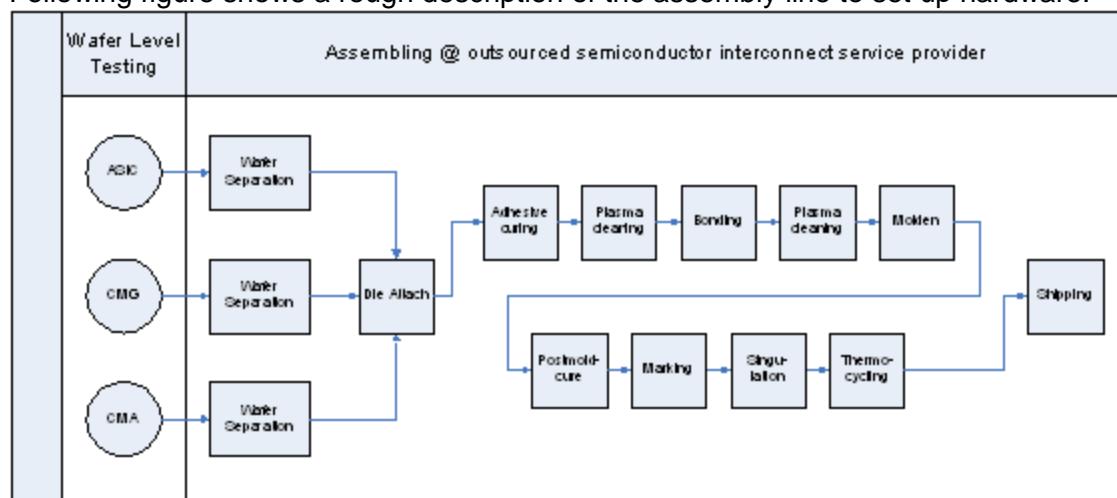
2. Miscellaneous

2.1 Production

2.1.1 Module processing during manufacturing

F02_86

Following figure shows a rough description of the assembly line to set up hardware.



2.1.2 Functional programming

F02_89

Following figure describes process flow for functional programming. Optimization of the module-calibration-flow will be proved - 3 sections are shown as an option for explanation. Please note: customer specific settings, e.g. SPI protocol, etc. are programmed in Reutlingen for sensors used in external market. For overview of customer specific settings see 1.10.5.6

F02_90

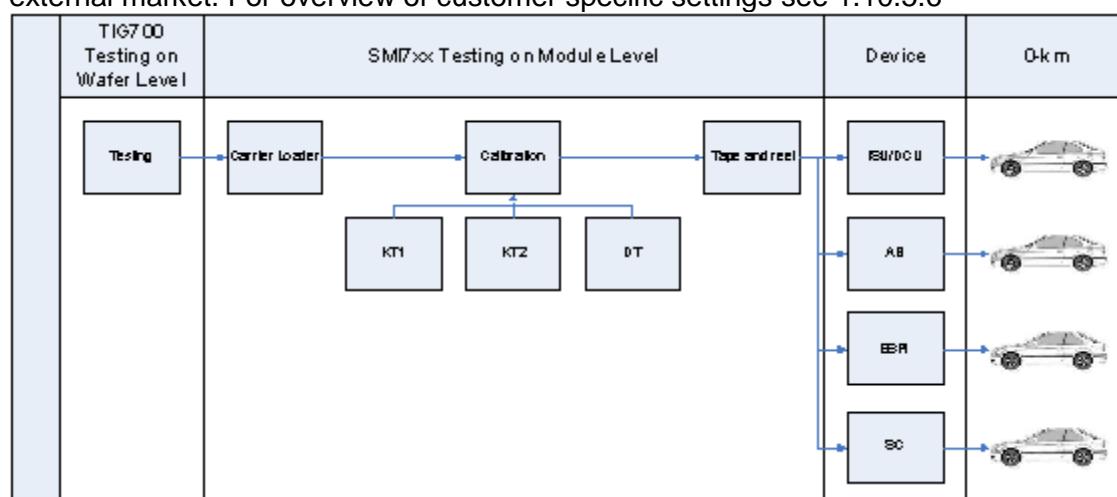


Figure 2: Process flow for functional programming

2.1.3 Serial number for traceability

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For purpose of traceability a memory area for unique serial number is implemented. The unique ID is coded in the ASIC S/N, the SMI7 type (700, 710) is coded together with (parts of) the SAP-Sample Code in the Module S/N. Therefore, the ASIC S/N and the Module S/N need to be read out by the ECU.

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The Customer S/N can be programmed and be used by the customer, but is not necessary for traceability on Module/ASIC level.

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Table 4: Unique serial numbers for traceability

Content	Responsible	Size	Unit
ASIC S/N	ASIC Wafer Level Testing	48	Bit
HW/SW-Level (ASIC Revision)	ASIC Wafer Level Testing	8	Bit
Module S/N	Module Testing	48	Bit
Customer S/N	Customer	16	Bit

F02_9394

The detailed definition of the Module S/N is given in the following Table:

Bit Sample/series	SMI7 typ	001 010 011 000	last 5 digits type part number 17 bits binary	production lot number 27 bit binary	
				sample shop lot number 17 bits binary	consecutive number 10 bits binary
Sample	0	000	0 0000 0111 0010 1010	0 0101 0101 0000 0010	10 0110 1100
Series	1	001	0 0101 0101 0100 1010	001 0101 0100 0000 1000 0000 0000	
Interpretation Sample	no standard		(0274B01)018-34	21762	620
Interpretation Series	SMI700		(1 270 1)21 834		22284288

The information in Brackets in the interpretation of the type part number are the omitted constant values of the type part number.

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The SMI7 type field identifies the sensor types as follows:

Type (3 Bit)	Sensor Desc.
000b	no standard
001b	SMI700
010b	SMI710
011b	SMI720
100b	reserved
101b	SMI740
110b	SMI750
111b	reserved

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The production lot number is coded as follows:

Item	Bits	Format
Production work week	0..5	Integer 1..53
Production year	6..10	2010 + Integer 0..31 - e.g. 2011 -> 1
Packaging Company	11..12	ASE 00, Unisem 01
Lot No	13..19	Integer 0..99
Sublot Letter	20..25	Integer as Code for Letter 1=A, 2=B, 3=C ..

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2.2 Module configuration

2.2.1 Structure of Data OTP

F02_91

For programming purpose the data OTP is virtually split in several banks (BAs): bank M0-M7 are used for storing module calibration data, bank D0-D3 are used for storing device calibration data, bank D4 is for ROM patch, bank D5 is the error memory while program OTP (P_OTP) is used to store custom program. Each bank can be programmed and secured independently.

F02_92

OTP setup and responsibility for definition of content and production-responsibility of the different BA is defined in the following table.

BA	Description	Exemplification	Size	Copied to Reg/RAM/DSP by	Written by
D0	Memory Administration BA D1 to D3	Description of setup of address space of module responsibility	8 Bytes	none	Customer
M0	Memory Administration BA M1 to M7	Description of setup of address space of module responsibility	12 Bytes	none	SMI7
M1	Wafer Level Testing	Bandgap calibration, Oscillator calibration, Chip ID, ... Checksum Bank M1	Variable	bootloader	TIG700
M2	Module Level Testing 1	Basic Module Data, ... Checksum Bank M2		bootloader	SMI7
M3	Module Level Testing 2	Calibration Acceleration Channel 1, ... Checksum Bank M3		bootloader	SMI7
M4	Module Level Testing 3	Calibration Acceleration Channel 2, ... Checksum Bank M4		bootloader	SMI7
M5	Module Level Testing 4	Calibration Acceleration and Yaw-Rate Channel over temperature, ... Checksum Bank M5		bootloader	SMI7
M6	Module Level Testing 5	Optional		bootloader	SMI7
M7	Module Reserve	Optional(e.g., for customer sample corrections)		bootloader	SMI7
D1	Device 1	Device Data Configuration, E.g DCU / ISU / Sensor Cluster fine offset calibration	Variable (364B for CAN)	bootloader	Customer
D2	Device 2	Device Data Configuration, E.g DCU / ISU / Sensor Cluster fine offset calibration		bootloader	Customer
D3	Device 3	Device Data Configuration, E.g DCU / ISU / Sensor Cluster fine offset calibration		bootloader	Customer
Production Memory 2	Device Production	Space reserved for device production purposes	16 Bytes	none	Customer
Production Memory 1	Module Production	Space reserved for module production purposes	16 Bytes	none	SMI7
RP1&RP2	ROM Patch	ROM Patch Configuration	16 Bytes	bootloader	SMI7
EM	Error Memory	Permanent storage of occurred failures, incl. activation marker	32 Bytes	none	Activation by customer

Legend:

Memory with fixed addresses

Memory with variable addresses

F02_11263

In order to keep the data storage compact, the length/start/end address of bank M1-M7 and D1-D3 are not fixed. The size of those banks can be freely configured by programming the end address of the bank accordingly.

The configuration data stored in OTP will be loaded into configuration registers, DSP RAM and µC RAM by bootloader.

F02_7760

The banks M0-M7 are written during wafer level testing and module final testing. When a SMI7 module is delivered, all M-banks are locked and thus cannot be changed on device level. The banks D1-D3 can be used for device level configuration by the customer. The size and usage of each bank D1-D3 is variable. D0 is the memory administration bank of D1-D3 (i.e. end addresses of the used banks) and is automatically written by the µC service routines used for device level programming.

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Configuration data is stored in "tuples", each containing a "target address" and a "content". The target address contains an identifier of the target memory block (i.e. hardware register, µC RAM, DSP RAM) and a short representation of the physical target memory address. Dependent on the target memory block, "target address" can be 16bit (register and µC RAM tuples) or 8bit (DSP RAM tuples). The "content" of the tuple can be up to 16 bit (register and µC RAM tuples) or 24 bit (DSP RAM tuples). Not every configuration value uses all available "content" bits. If not all bits are used the remaining bits must be set to "0".

During startup, the boot loader copies the "content" of the tuples into the memory with address "target address". The addresses which are of interest for the customer (i.e., address of the reset- vector) and the meaning of their content is shown below. The customer is able to configure the values which are listed in the "white list" shown below.

Every configuration value comes with a default value that allows for fully functional and error-free sensor operation in 5V supply mode for SPI. For 3V-VDD3-supply (with VB to be connected to GND), the VB undervoltage detection needs to be masked, see 7.7



2.2.2 Customer Configurable Sensor Parameters ("White List")

F02_10335

Configurable hardware registers:

Target address	Description	Default
0x810B	WDGI_GPIO_CFG Bit 0: WDGI_PIN_EN - Enable output driver for WDGI pin. PIN is high-resistance if not enabled. Bit 1: WDGI_PAD_CTRL_REQ - Use WDGI as general purpose output.	0x0
0x8218	MAIN_CAN_CFG Bit 1...0: CXOLVL - XTAL amplitude level. Bit 2: CX_PD - Power down on crystal oscillator. Bit 3: TX_EN - Enable TX pin; Pin is high resistant if not enabled. Bit 4: CAN_CLKS_OFF - Switch off clocks in CAN module when CAN is in power down mode. Bit 5: DSP_CLKS_ON - Switch on clocks in DSP module.	0x38
0x8423	ERROR_MASK, mask bit for error flags Bit 0: disable_can_mask - mask bit for disable can Bit 1: disable_psi_mask - mask bit for disable psi Bit 2: disable_wdgi_mask - mask bit for disable wdgi Bit 3: uc_watchdog_err_mask - mask bit for uc_watchdog_err Bit 4: uc_rom_bist_mask - mask bit for uc_rom_bist error Bit 5: uc_ram_ifa13_mask - mask bit for uc_ram_ifa13 Bit 6: uc_ram_soaf_mask - mask bit for ram_soaf Bit 7: uc_ram_dpath_mask - mask bit for ram_dpath error Bit 8: uc_otp_prog_bist_mask - mask bit for uc_otp_prog_bist error Bit 9: uc_ram_par_error_mask - mask bit for uc ram parity error Bit 10: uc_otp_data_bist_mask Bit 11: uc_otp_prog_bist_initial_mask Bit 12: uc_otp_data_bist_initial_mask Bit 13: uc_otp_data_corrupt_header_mask Bit 14: uc_otp_data_invalid_tuple_mask Bit 15: uc_stack_check_mask	0x0
0x8431	ERROR_MASK_1, mask bit for error flags Bit 0: uc_hw_timeout_mask Bit 1: can_apb_slv_mask Bit 2: uc_unrecoverable_error_mask Bit 3: uc_rom_otp_sw_incompatible_mask Bit 4: uc_can_psi_readback_mismatch_mask Bit 5: uc_tuple_readback_mismatch_mask Bit 6: v_dig_high_mask Bit 7: Ibist_err_mask Bit 8: can_ram_parity_mask Bit 9: cmg_f_check_mask Bit 10: pc_psi5_m_mask Bit 11: psi_apb_slv_mask	0x0

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0x850D	RESET_VECTOR, Reset Vector Bit 0: PONBITE_ACC - Controls automatic PowerOnBite execution off ACC1 and ACC2 channels. Bit 1: PONBITE_YRS - Controls automatic PowerOnBite execution off YRS channel. Bit 2: SPI_AUTOCALIB_EN - Automatic calibration of SPI slave parameters. Bit 3: SO_DRIVER - SO pad driver strength. Bit 4: SPI_CPOL - SPI clock polarity parameter CPOL. Bit 5: SPI_CPHA - SPI clock phase parameter CPHA. Bit 6: SPI_PROT_SELECT - SPI protocol CC32in or OpenSPI. Bit 7: BA3 - Bit three of SPI sensor address BUSADR. Bit 8: cQBITE_HI_enable - Continuous Quadrature BITE high frequent enable - DO NOT ENABLE, cQ-BITE is not to be used in SMI7 Bit 9: cQBITE_LO_enable - Continuous Quadrature BITE low frequent enable - DO NOT ENABLE, cQ-BITE is not to be used in SMI7 Bit 10: PRE_REGULATOR_DISABLE - Disable the 5V pre regulator for 3V applications. '1' is 3V and '0' is 5V application Bit 11: PSI_OFF - PSI_OFF Signal Bit 12: DCAN_OFF - DCAN_OFF Signal	0x100F
0x8516	CUSTOMER_SERIAL_NR Bit 15...0: CUSTOMER_SERIAL_NR - Serial number of customer.	0x0
0x8632	DEBUG_CONTROL Bit 14...7: ADDR_DEBUG_1 - Address for debug_1 value Bit 22...15: ADDR_DEBUG_2 - Address for debug_2 value Bit 23: ADDR_DEBUG_PARITY - Odd parity over bits 22:0 (Bits 6:0 = 0)	0x800000
0xB0C1	SID_YRS, SPI safety IDs YRS Bit 4...0: SID_RATE_LF - Safety ID yaw rate channel LF signal path. Bit 9...5: SID_RATE_HF - Safety ID yaw rate channel HF signal path.	0x3FF
0xB0C2	SID_ACC1, SPI safety IDs ACC1 Bit 4...0: SID_ACC1_LF - Safety ID Acceleration channel 1 LF signal path. Bit 9...5: SID_ACC1_HF - Safety ID Acceleration channel 1 HF signal path.	0x3FF
0xB0C3	SID_ACC2, SPI safety IDs ACC2 Bit 4...0: SID_ACC2_LF - Safety ID Acceleration channel 2 LF signal path. Bit 9...5: SID_ACC2_HF - Safety ID Acceleration channel 2 HF signal path.	0x3FF
0xB0C4	SPI address pointer #1 Bit 15...0: ADDR_P1 - Address pointer #1	0x0
0xB0C5	SPI address pointer #2 Bit 15...0: ADDR_P2 - Address pointer #2	0x0
0xB0C6	SPI address pointer #3 Bit 15...0: ADDR_P3 - Address pointer #3	0x0



F02_10336 Configurable µC RAM addresses:

Target address	Size	Description (#fract. Bits>0: right shift, <0: left shift)	Default
0xE002	8 bit	Init flush time for HF channels in ms	0xA
0xE003	8 bit	Init flush time for LF channels in ms	0x19
0xE01C	8 bit	Limit value of Error Counter 0	0x24
0xE01D	8 bit	Hold value of Error Counter 0	0x6
0xE01E	8 bit	Limit value of Error Counter 1	0x24
0xE01F	8 bit	Hold value of Error Counter 1	0x19
0xE020	8 bit	Limit value of Error Counter 2	0x24
0xE021	8 bit	Hold value of Error Counter 2	0x6
0xE022	8 bit	Limit value of Error Counter 3	0x24
0xE023	8 bit	Hold value of Error Counter 3	0x19
0xE024	8 bit	Limit value of Error Counter 4	0x24
0xE025	8 bit	Hold value of Error Counter 4	0x2
0xE026	8 bit	Limit value of Error Counter 5	0x24
0xE027	8 bit	Hold value of Error Counter 5	0x14
0xE028	8 bit	Limit value of Variable Error Counter 0	0x24
0xE029	8 bit	Hold value of Variable Error Counter 0	0x19
0xE02A	8 bit	Limit value of Variable Error Counter 1	0x24
0xE02B	8 bit	Hold value of Variable Error Counter 1	0x19
0xE02C	6 bit	Flag weights for Variable Error Counter 0	0x0
		Bit 1...0: Flag Weight of Error Flag0 linked to Variable Error Counter 0	
		Bit 3...2: Flag Weight of Error Flag 1 linked to Variable Error Counter 0	
		Bit 5...4: Flag Weight of Error Flag 2 linked to Variable Error Counter 0	
0xE02D	8 bit	Error Flag 0 linked to Variable Error Counter 0	0x0
0xE02E	8 bit	Error Flag 1 linked to Variable Error Counter 0	0x0
0xE02F	8 bit	Error Flag 2 linked to Variable Error Counter 0	0x0
0xE030	6 bit	Flag weights for Variable Error Counter 1	0x0
		Bit 1...0: Flag Weight of Error Flag0 linked to Variable Error Counter 1	
		Bit 3...2: Flag Weight of Error Flag 1 linked to Variable Error Counter 1	
		Bit 5...4: Flag Weight of Error Flag 2 linked to Variable Error Counter 1	
0xE031	8 bit	Error Flag 0 linked to Variable Error Counter 1	0x0
0xE032	8 bit	Error Flag 1 linked to Variable Error Counter 1	0x0
0xE033	8 bit	Error Flag 2 linked to Variable Error Counter 1	0x0
0xE034	6 bit	Channel Status linked to Variable Error Counter 0	0x0
		Bit 0: Channel Status Acc1_HF link to Variable Counter 0	
		Bit 1: Channel Status ACC2_LF link to Variable Counter 0	
		Bit 2: Channel Status ACC1_LF link to Variable Counter 0	
		Bit 3: Channel Status YRS_HF link to Variable Counter 0	
		Bit 4: Channel Status ACC2_HF link to Variable Counter 0	
		Bit 5: Channel Status YRS_LF link to Variable Counter 0	

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0xE035	6 bit	Channel Status linked to Variable Error Counter 1 Bit 0: Channel Status Acc1_HF link to Variable Counter 1 Bit 1: Channel Status ACC2_LF link to Variable Counter 1 Bit 2: Channel Status ACC1_LF link to Variable Counter 1 Bit 3: Channel Status YRS_HF link to Variable Counter 1 Bit 4: Channel Status ACC2_HF link to Variable Counter 1 Bit 5: Channel Status YRS_LF link to Variable Counter 1	0x0
0xE200	16 bit	Tol. of Ctm_Diff Difference Check (unsigned, 0 fract. bits)	0x3E8
0xE274	16 bit	Abs. Tol. of Yrs_Rate_V_Com Tol. Check (unsigned, 0 fract. bits)	0xF0
0xE07D	8 bit	Abs. Tol. of Yrs_Quad_I_Tol Tol. Check (unsigned, -8 fract. bits)	0x3E
0xE03E	8 bit	Abs. Tol. of Yrs_Rate_V_Cm Tol. Check (unsigned, -4 fract. bits)	0x4
0xE242	16 bit	Abs. Tol. of Yrs_Rate_V_Fb Tol. Check (unsigned, 0 fract. bits)	0x3C
0xE03F	8 bit	Rel. Tol. of Yrs_Drv_Pi_Tol Temp. Dependent Tol. Check (unsigned, 9 fract. bits)	0x80
0xE27E	16 bit	Lower Range of Ctm_Range Range Check (signed, 0 fract. bits)	0xAA10
0xE280	16 bit	Upper Range of Ctm_Range Range Check (signed, 0 fract. bits)	0x59D8
0xE044	8 bit	Abs. Tol. of Yrs_Drv_Cu_Gain Tol. Check (unsigned, -3 fract. bits)	0x1F
0xE040	8 bit	Symm. Tol. of Yrs_Quad_Hf Tol Symm. Tol. Check (unsigned, -4 fract. bits)	0xFA
0xE072	8 bit	Abs. Tol. of Yrs_Drv_AdC_Mean Tol. Check (unsigned, 0 fract. bits)	0x0
0xE073	8 bit	Abs. Tol. of Yrs_Rate_AdC_Mean Tol. Check (unsigned, 0 fract. bits)	0x0
0xE03C	8 bit	Abs. Tol. of Acc1_V_cm Tol. Check (unsigned, 0 fract. bits)	0x32
0xE03D	8 bit	Abs. Tol. of Acc2_V_cm Tol. Check (unsigned, 0 fract. bits)	0x32
0xE038	8 bit	Abs. Tol. of Yrs_PII_Tol Tol. Check (unsigned, -5 fract. bits)	0x17
0xE041	8 bit	Abs. Tol. of Yrs_Rate_V_Tn Tol. Check (unsigned, 0 fract. bits)	0x8C
0xE078	8 bit	Rel. Tol. of yrs_quad_seq_bite Pos-Zero TDTC (unsigned, 9 fract. bits)	0x4d
0xE079	8 bit	Rel. Tol. of yrs_quad_seq_bite Neg-Zero TDTC (unsigned, 9 fract. bits)	0x4d
0xE07A	8 bit	Rel. Tol. of yrs_quad_seq_bite Pos-Neg TDTC (unsigned, 9 fract. bits)	0x4d
0xE077	8 bit	Symm. Range of Yrs_Rate_Seq_Bite Symm. Tol. Check (unsigned, -4 fract. bits)	0xE1
0xE07B	8 bit	Rel. Tol. of acc1_seq_bite TDTC (unsigned, 9 fract. bits)	0x38
0xE076	8 bit	Rel. Tol. of acc2_seq_bite TDTC (unsigned, 9 fract. bits)	0x38
0x4001	-	Pointer to Block Tuple containing the CAN Configuration*	0x0
0x4003	-	Pointer to Block Tuple containing the PSI Customer Configuration*	0x0
0x4006	-	Pointer to Block Tuple in Device Bank reconfiguring error flag weights*	0x0

*Block tuple format used for CAN and PSI configuration and error flag weights: see Configuration Service 0x5 "Write Device Tuple".

F02_10705

Configurable DSP RAM addresses:

Target address	Description	Default
0x69	LF Switch	0x0
	Bit 8...7: LF_SWITCH - 0x0=LF2, 0x1=LF2, 0x2=LF3, 0x3=LF4	

2.2.3 Timing Estimation for OTP Programming

F02_1601

The programming time of data to the OTP is primarily given by two factors: first the time to transfer the data into the system, and second the time to burn the data into the nonvolatile memory.

2.2.3.1 Programming time for Data OTP

F02_8024

$$t_{\text{total}} = (4 * t_{\text{Prog}} + t_{\text{Refresh}}) * \text{size} + t_{\text{Transfer}} * \text{size}$$

- size = number of words (4Byte) to be written:

- 1 word needed per tuple for RAM, Register, DSP tuples
- 1 word needed per data block + 1 word header for block tuples

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- t_{Prog} : Programming time of one OTP cell: 100 μ s
- $t_{Refresh}$: Refresh time of charge pump after programming (to reach normal level), depends on "1"s to be written
 - typical case (50% "1"s): 7 ms
 - worst case (100% "1"s): 14 ms
 - if CP pin is supplied externally = 0ms.
- $t_{Transfer}$: time needed to transfer the data by a given interface

Example:

- Writing size=1 word (e.g. 1 register tuple) using 32bit SPI at 10 MHz clock frequency, sequential transfer delay time=200ns
- 6 SPI commands needed to program 1 word into Data OTP (3x write command on CONF_IREGx, 3x read command on CONF_OREGx) => $t_{Transfer} = 6 * (32 * 100\text{ns} + 200\text{ns}) = 20.4\mu\text{s}$
- 50% "1"s in word to be written
- => $t_{total} = (400\mu\text{s} + 7\text{ms}) * 1 + 20.4\mu\text{s} * 1 = 7.42\text{ms}$

2.2.3.2 Programming time for Program OTP

$$\text{F02_11295 } t_{total} = (t_{Prog} + t_{Refresh}) * \text{size} + t_{Transfer} * \text{size}$$

- size = number of words (4Byte) to be written:
- t_{Prog} : Programming time of one OTP cell: 100 μ s
- $t_{Refresh}$: Refresh time of charge pump after programming (to reach normal level), depends on "1"s to be written
 - typical case (50% "1"s): 7 ms
 - worst case (100% "1"s): 14 ms
 - if CP pin is supplied externally = 0ms.
- $t_{Transfer}$: time needed to transfer the data by a given interface

2.2.4 General Considerations for Device Level Configuration

- $$\text{F02_11250 }$$
- The ambient temperature during OTP programming must be below 30°C.
 - Programming is done using the Configuration Services provided by SMI7. The services are running on the integrated microcontroller (μ C) and take care of OTP memory administration automatically.
 - It is not allowed to write more than 50 tuples per bank (D1, D2, D3)
 - Writing of configuration tuples is done using configuration service 0x5 "Write Device Tuple"
 - Locking of bank (D1, D2, D3) using configuration service 0x6 "Lock Configuration Bank" is required immediately after programming to ensure data integrity.
 - Configuration service 0x6 "Lock Configuration Bank" must be called with parameter "Write Checksum2" when a fine offset calibration or a LF filter reconfiguration is done in the current bank.
 - Configuration service 0x6 "Lock Configuration Bank" must be called with parameter "Lock D0" after the last programming step to secure the device configuration header bank D0 with a CRC. After this step no more configuration data can be added to the OTP!

2.2.5 Usage of Configuration Services

2.2.5.1 General considerations for using configuration services

- $$\text{F02_11208 }$$
- The returned status of any service (CONF_OREG0) must be read back and evaluated along with an appropriate error handling
 - The next service may only be started after the previous service was finished



- The minimum delay between 2 consecutive service calls is 500µs (from finished previous service until start of next service)
- After locking a configuration bank the sensor has to be reset (so that any configuration data in the locked bank is processed by the bootloader) before the service "Read Configuration Value" returns proper values.
- The service "Send SPI Message" can lead to the flag "uc_watchdog_err" if extreme parameters are used (e.g. SPI clock frequency < 100kHz).

2.2.5.2 Overview of available Configuration Services

F02_135

ID	Service	Description
0x0	Cancel the running configuration service	Allow to terminate another previously started configuration service; if there is no currently running service, nothing will be done
0x2	N-Value function	Calculation of span, average and variance of the value at the given address
0x4	Read Config Value	Reading of the currently valid startup configuration parameter value from the last device bank or its reset value
0x5	Write Device Tuple	Device configuration by writing configuration single or block tuples into the last open device bank
0x6	Lock Configuration Bank	Module or device lock by locking M0 or D0 bank or only last open bank lock. Calculation and storage of DSP Checksum I or II
0x7	Fine Offset Calibration	Offset calibration of the acceleration and rate sensor elements
0x8	Read Memory	Reading of 32-bit data from particular address, restricted to module/device production memory
0xB	Activate Error Memory	Error storage activation
0xC	Cyclic Output of Error Counters	Sensor evaluation support on test drives
0xD	Manual BITE trigger	Dynamic or static BITE actuation, status request or switching off the current BITE

2.2.5.3 Common Interface for Configuration Services

F02_11252 The µC Configuration Service interface can be accessed via 32bit SPI protocols (on page 0) or BiDir PSI or MessCAN. "Reserved" input fields will be ignored by the config services, but shall be kept to 0 for possible future extensions. "Reserved" output fields must be ignored by the service requester, as their contents may change with possible future extensions. All values are little endian, i.e. the LSB is stored in the lowest bit in the lowest byte. A word is 32 bits long, a half-word 16 bits.

F02_9456 The configuration services interface consists of 9 registers (with 16 Bit each). A service interrupt is invoked (i.e. service execution starts) when the CONF_IREG0 register is overwritten with a new value even if the fields SERVICE_ID, ORIGIN and AR have not been changed. It must be ensured that the parameters in CONF_IREG1...CONF_IREG3 have been set properly **before** CONF_IREG0 is written. Before triggering service execution by writing CONF_IREG0 the registers CONF_IREG1...CONF_IREG3 can be written in arbitrary order and without timing constraints.
The first step after an interrupt call is copying the fields SERVICE_ID, ORIGIN and AR into the CONF_OREG0 register and setting the STATUS field to 0x3.



Type	Register	Description	Comment
Input Parameters	CONF_IREG0	uC Transfer input register 0	Configuration services request control register
	CONF_IREG1	uC Transfer input register 1	Meaning depends on CONF_IREG0
	CONF_IREG2	uC Transfer input register 2	
	CONF_IREG3	uC Transfer input register 3	
Output Parameters	CONF_OREG0	uC Transfer output register 0	Configuration services status control register (partly mirrored from CONF_IREG0)
	CONF_OREG1	uC Transfer output register 1	Meaning depends on CONF_IREG0, resp. CONF_OREG0
	CONF_OREG2	uC Transfer output register 2	
	CONF_OREG3	uC Transfer output register 3	
Control	CONF_RESERVE	uC Transfer control register	Reserved or further extensions

F02_9462 Usage of CONF_IREG0 and CONF_OREG0

CONF_IREG0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																	
	reserved								SERVICE_ID	ORIGIN		AR																					
reset value																																	
0x0																																	
																? On request acceptance the corresponding fields (same name) are copied from CONF_IREG0 to CONF_OREG0 ?																	
CONF_OREG0	ERROR_CODE				STATUS	res.	SERVICE_ID		ORIGIN		AR																						
reset value																																	
0x0																																	

Field	Values	Meaning
ORIGIN (Source of currently / last processed service)	0x0	Internal software request
	0x1	CAN
	0x2	PSI
	0x3	SPI

Field	Values	Meaning for each ORIGIN		
		CAN	PSI	SPI
AR (Active Response requested)	0x0	No Response Message is sent	Response is sent using all 3 slots (s. "Config Services on PSI")	Not relevant as Status. The output of requested service is to be read by the SPI Master (as the sensor is the SPI slave and can not initiate a transmission).
	0x1	Completion/Termination of requested service is automatically reported once in a Response Message on Standard CAN ID	Response is sent using only slot 1 (s. "Config Services on PSI")	
	0x2	Completion/Termination of requested service is automatically reported once in a Response Message on Special CAN ID	Response is sent using only slot 2 (s. "Config Services on PSI")	
	0x3	reserved	Response is sent using only slot 3 (s. "Config Services on PSI")	

F02_11272 Possible STATUS Values

Field	Values	Meaning
STATUS (Status of currently / last processed service)	0x0	Service done, resp. idle Data in CONF_OREG1-3 is valid and must be interpreted according to the SERVICE_ID.
	0x1	Service terminated with errors (e.g. due to invalid parameter values) Data in CONF_OREG1-3 is to be ignored as it's invalid.
	0x2	Service in progress Data in CONF_OREG1-3 is to be ignored as it's invalid.
	0x3	Service requested Data in CONF_OREG1-3 is to be ignored as it's invalid.



F02_9663 Valid ORIGIN/AR Combinations

		ORIGIN			
		SW	CAN	PSI	SPI
AR	0x0	dc	ok	ok	dc
	0x1	dc	ok	ok	dc
	0x2	dc	ok	ok	dc
	0x3	dc	nok	ok	dc

dc = don't care
ok = allowed
nok = not allowed

F02_11273 Possible Error Codes

Field	Values	Meaning	Cause
ERROR_CODE (ID of error reason (in case of invalid service termination))	0x00	No Error	Service successfully finished
	0x01	Service is not supported	Unknown service ID
	0x02	ORIGIN / AR combination is invalid	ORIGIN = 0x1 and AR = 0x3
	0x03	Service is protected	Service ID may not be used
	0x04	Read access error	Given address does not exist or a bus error has been detected
	0x05	Write access denied	Given address does not exist or a bus error has been detected
	0x06	Not enough Data OTP space	Not enough free words in Data OTP
	0x07	D0 is locked	Device configuration has finished and no data can be changed in the OTP
	0x08	Module config not completed yet	Cannot write into / read from device banks: M0 has not been locked yet
	0x09	Entry is not in White List	Searched tuple is not in the White List: read / write access denied
	0x0A	Device is defect and cannot be used any more	Device has been marked as defect by writing 0xFFFFFFFF into D0 CRC
	0x0B	DSP parity failure	Read DSP signal has a wrong parity
	0x0C	OTP programming failure	Error occurred during OTP programming
	0x0D	ConfigService dependent	ConfigService dependent, detailed explanation see below
	...		
	0x1F		

2.2.5.4 Configuration Services on PSI - "BiDirMode"

F02_9487 To gain access to the configuration services the sensor must be set to bi-directional communication first by a special BiDirRequestFrame with FC=0x0 (s. below).

2.2.5.4.1 Layout of BiDir RequestFrame (ECU to Sensor)

F02_9488 "x" or "ign" indicates an ignored bit field (see below).
"n" indicates a bit being 0 or 1.

order of transmission →															
PSI-Std.		Startbits		S Adr		FC		RAdr		Data		CRC		last bit	
on the bus	0	1	0	1	n	n	n	1	n	n	n	1	n	n	1
SMI7-Usage	START	ign	S	ADR	ign	FC	ign	DATA[0:15]		CRC					
	0	1	2	x	0	1	2	x	0	1	2	x	3	4	5
				LSB		MSB		LSB		1	2	x	6	7	8
Layout in	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
Receive	reserved		CRC		DATA[15:0]		REG ID		S	ADR	START				
Register	0	1	2	15	14	13	12	11	10	9	8	7	6	5	4
				LSB		MSB		MSB		LSB		MSB		LSB	

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F02_9490 Description of the contained fields:

Field	Details	Values	Meaning
START	Fix start bits	0x2	PSI standard (will not be written to the BiDir register)
S_ADR	Sensor address	0x0	reserved
		0x1	BiDirRequestFrame is accepted only if sensor address matches.
		0x2	The default sensor address is built of the sensor type bit (SMI700/710) and an external pin level (Rx). (For A-Silicon not used, for B-Silicon the same concept like SPI address should be taken.)
		0x3	
		0x4	
		0x5	
		0x6	
		0x7	Broadcast address. BiDirRequestFrame is accepted independent of own sensor address. (For AA-Silicon only broadcast address is supported)
FC	Function Code	0x0	Enter/Leave BiDir Mode
		0x1	Write DATA to CONF_IREG1
		0x2	Write DATA to CONF_IREG2
		0x3	Write DATA to CONF_IREG3
		0x4	Write DATA to CONF_IREG0
		0x5	reserved
		0x6	reserved
		0x7	reserved
DATA	Data		16 bit data as defined above
CRC	CRC		CRC over other Sadr, FC, Radr, Data in transmitted order. Message is only accepted if CRC is matching. (must be checked by software).

2.2.5.4.2 Layout of BiDirAnswerFrame (Sensor to ECU)

F02_9491

		order of transmission →																								
		S1	S2	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	C2	C1	C0
PSI-Std.		Start		Data[0:19] (20 Bit Payload)																		CRC				
on the bus		0	0	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	
SMI7-Usage		DATA[0:15]																			REG ID					
in the slot output register		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	R3	R2	R1	R0					
		B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0					

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F02_11258 Description of the contained fields:

Field	Details	Values	Meaning
START	Fix start bits	0x00	PSI standard, Generated by the ASIC HW.
REG_ID	Register ID	0x0	reserved
		0x1	DATA contains the data of CONF_IREG1
		0x2	DATA contains the data of CONF_IREG2
		0x3	DATA contains the data of CONF_IREG3
		0x4	DATA contains the data of CONF_OREG0
		0x5	DATA contains the data of CONF_OREG1
		0x6	DATA contains the data of CONF_OREG2
		0x7	DATA contains the data of CONF_OREG3
		0x8	reserved
		0x9	reserved
		0xA	reserved
		0xB	reserved
		0xC	reserved
		0xD	reserved
		0xE	reserved
		0xF	reserved
DATA	If Register FC <= 0x4		Data as defined by REG_ID value (s. above)
	If FC > 0x4 or FC == 0x0		No frame will be send
CRC	CRC over other fields		Calculated by the ASIC HW.

2.2.5.4.3 Timing and Assignment of BiDirAnswerFrames

F02_9494 In the bidirectional mode the PSI frame has 3 time slots in which the BiDirAnswer is sent. Initially (after entering the BiDir Mode) the sensor stays silent until the first configuration service is requested (by a write command to CONF_IREG1, CONF_IREG2 and CONF_IREG3) and triggered by CONF_IREG0. Each Service request is then followed by a cyclic transmission of CONF_OREG0, CONF_OREG1, CONF_OREG2, CONF_OREG3 until the next request of a config service is started with a write command to CONF_IREG1, CONF_IREG2 or CONF_IREG3.

Independently on the value given in the AR field all 3 slots are used for answer frames in 500 us period.

2.2.5.4.4 Short sample communication sequence on the PSI bus (for configuration of a single sensor on the PSI bus)

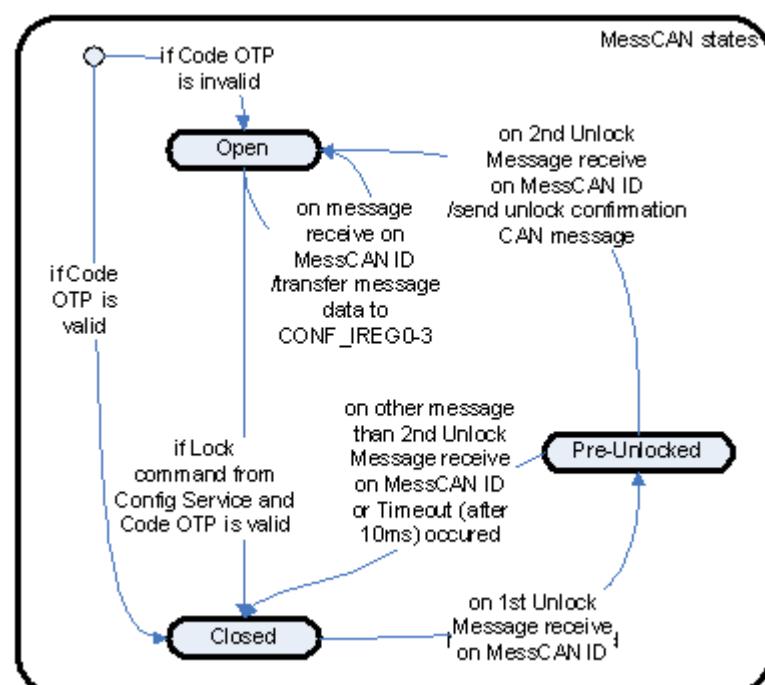
F02_9495

Configuration Step	BiDirRequestFrame				BiDirAnswerFrame(s)
	S	ADR	FC	DATA	
Enter BiDir Mode	0x7	0x0	0xA494	Enter BiDir Mode (Is only necessary, if the sensor runs with OTP program.)	
Disable Config Service Protection	0x7	0x1	0x5BAD	Write to CONF_IREG1	
	0x7	0x2	0xFEE1	Write to CONF_IREG2	
	0x7	0x3	0x0C0F	Write to CONF_IREG3	
	0x7	0x4	0x0038	Write to CONF_IREG0 – (with AR setting: answer in all 3 slots)	
	Pause with or without sync pulses to await termination of configuration service (in case of this service only a few pulses are needed as the service terminates within 500µs.)				
Call n-value function (0x40000084)	0x7	0x1	0x8021	Write to CONF_IREG1	
	0x7	0x2	0x0064	Write to CONF_IREG2	
	0x7	0x4	0xF002	Write to CONF_IREG0	
	Pause with stable sync pulses to await termination of configuration service (in case of this service call more pulses are needed as the service needs about 50ms (100 samples with 2kHz sampling rate) to terminate).				
Leave BiDir Mode	0x7	0x0	0x1111	Leave BiDir Mode (invalid password)	

2.2.5.5 Configuration Services on CAN - "MessCAN"

2.2.5.5.1 Default Unlock/Lock State

F02_11255





2.2.5.5.2 Unlock Procedure

F02_9479 To gain access to the configuration services the sensor must be unlocked first by two subsequent CAN messages within a certain time.

MessCAN Unlock Message 1 (CAN-ID: 0x742)

	7	6	5	4	3	2	1	0
Byte 0								0x34
Byte 1								0xA6
Byte 2								0xD3
Byte 3								0x4F
Byte 4								0x70
Byte 5								0x39
Byte 6								0x13
Byte 7								0xAE

In case of by mistake sent Unlock Message 1 after the MessCAN has been already opened, this message will be ignored.

The Byte 0 (0x34) is chosen in order to process this message by the Service ID 0x3.

MessCAN Unlock Message 2 (CAN-ID: 0x742) (within 10ms after 1st)

	7	6	5	4	3	2	1	0
Byte 0				0x3		0x1		AR
Byte 1								0xF8
Byte 2								0x91
Byte 3								0x39
Byte 4								0x27
Byte 5								0x71
Byte 6								0x5F
Byte 7								0x80

The AR field totally corresponds to that described in sheet CONF_IREG0-OREG0.

Unlock Message 2 causes the MessCAN Response Message described in sheet 3-EnableProtConfServices depending on the AR field.

The same procedure applies to an Unlock Message 2 which is also sent after the MessCAN has been already opened.

2.2.5.5.3 Projection of MessCAN messages to config services

F02_9481

MessCAN Request Message (CAN-ID: 0x742 or Special ID) (only accepted after successful unlock)

	7	6	5	4	3	2	1	0
Byte 0								CONF_IREG0[7:0]
Byte 1								CONF_IREG0[15:8]
Byte 2								CONF_IREG1[7:0]
Byte 3								CONF_IREG1[15:8]
Byte 4								CONF_IREG2[7:0]
Byte 5								CONF_IREG2[15:8]
Byte 6								CONF_IREG3[7:0]
Byte 7								CONF_IREG3[15:8]



MessCAN Response Message (CAN-ID: 0x743 or Special ID, sent only if requested in Request Message - field AR)

	7	6	5	4	3	2	1	0
Byte 0	CONF_OREG0[7:0]							
Byte 1	CONF_OREG0[15:8]							
Byte 2	CONF_OREG1[7:0]							
Byte 3	CONF_OREG1[15:8]							
Byte 4	CONF_OREG2[7:0]							
Byte 5	CONF_OREG2[15:8]							
Byte 6	CONF_OREG3[7:0]							
Byte 7	CONF_OREG3[15:8]							

If configuration services need less than IREG1-3 for their input parameters shorter messages with DLC < 8 CAN be used to define only the used IREG1-3 to save bandwidth.

2.2.5.5.4 Special CAN ID

F02_11257 The Special CAN IDs are used in production to address different sensors which are connected over the same CAN bus. The unique ID is calculated from the common ID as an offset plus a value from OTP production data (VMID) that is unique within a lot.

Special CAN IDs are always extended CAN IDs (29Bit). Following calculation rules apply to special CAN IDs:

Special CAN ID for reception = **VMID0 | ((VMID1 & 0xFF)<<16) | ((VMID2>>1) & 0xF)<<24**

Special CAN ID for transmission = **VMID0 | ((VMID1 & 0xFF)<<16) | ((VMID2>>1) & 0xF)<<24 | 0x10000000**

2.2.5.5.5 Handling the MessCAN Unlock / Lock Messages

F02_9482 The MessCAN Unlock Message 1 will be ignored.

If AR field in MessCAN Unlock Message 2 is equal 0x1 or 0x2 (s. sheet CONF_IREG0-OREG0), a MessCAN Response Message will be sent actively.

The MessCAN Lock Message provides locking the MessCAN.

2.2.5.6 Detailed Description of Available Configuration Services

2.2.5.6.1 Service-ID 0x0: Cancel the running configuration service

2.2.5.6.1.1 Execution

F02_9511 Only cyclic called function are affected - their next execution will be prevented. No effect to services that are precessed and finished within the interrupt. The RAM content will not be reset. Running hardware modules cannot be stopped. If no service is currently running, there will be no effect of the service ID 0x0.

2.2.5.6.1.2 Timing

F02_9512 Service is triggered and ends in the interrupt.

**2.2.5.6.1.3 Input parameters (CONF_IREG1...CONF_IREG3)**

F02_9513

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1																reserved
CONF_IREG2																reserved
CONF_IREG3																reserved

2.2.5.6.1.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9514

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1																reserved
CONF_OREG2																reserved
CONF_OREG3																reserved

2.2.5.6.1.5 Possible error codes

F02_9515

None.

2.2.5.6.2 Service-ID 0x2: N-Value Function**2.2.5.6.2.1 Execution**

F02_11271

Value at the given address is cyclicly sampled based on the sampling frequency. The 16-bit span value, 16-bit average value and 32-bit variance are calculated and stored into Config Output registers when finished.

2.2.5.6.2.2 Timing

F02_11270

Service is triggered in the interrupt and ends in the main cycle. Runtime depends on the sampling frequency and number of samples and can be calculated:

$$\text{Runtime} = 0.5 \text{ ms} + (2^{\text{LOG2_NO_OF_SAMPLES}}) * (2^{\text{LOG2_FREQ_DIVIDER}}) * 0.5 \text{ ms}.$$

2.2.5.6.2.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_11269

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMPLING ADDR																
CONF_IREG1	LOG2_FREQ_DIVIDER	res.	CHECK_MOD	SIGN	VALUE_LENGTH		LOG2_NO_OF_SAMPLES									
CONF_IREG2				reserved												VALUE_OFFSET
CONF_IREG3																
Field	Values	Meaning														
SAMPLING_ADDR	(see right)	Address of the value to be sampled														
LOG2_NO_OF_SAMPLES	0x1 to 0xB	Number of samples to be taken is calculated as ($2^{\text{LOG2_NO_OF_SAMPLES}}$)														
VALUE_LENGTH	0xF	Must be set to 0xF for signals RATE_LF, ACC1_LF, ACC2_LF, RATE_HF, ACC1_HF, ACC2_HF														
SIGN	0x1	Must be set to 0x1 for signals RATE_LF, ACC1_LF, ACC2_LF, RATE_HF, ACC1_HF, ACC2_HF														
CHECK_MOD	0x0	Do not check signal status (Cl Bit) and Parity Bit														
	0x1	Check signal status (Cl Bit) and Parity Bit (recommended)														
LOG2_FREQ_DIVIDER	0x0 to 0xF	Divider to reduce sampling frequency: base frequency of 2kHz is divided by ($2^{\text{LOG2_FREQ_DIVIDER}}$), e.g. 0 => 2kHz, 1 => 1kHz, 2 => 500Hz, 3 => 250Hz, etc.														
VALUE_OFFSET	0x0	Must be set to 0 for signals RATE_LF, ACC1_LF, ACC2_LF, RATE_HF, ACC1_HF, ACC2_HF														

Notes:

1) If CHECK_MOD is 1, the validity of the signal will be checked.

If the signal is invalid, the sampling will be continued anyway and the current invalid signal value will not be ignored. However, the output field ERROR_CODE will contain the code of the occurred error (see "Possible error codes").

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Only the first occurred error will be stored and returned in the output field ERROR_CODE after the service finishes.

2) The sensor channel to be sampled is determined by the parameter SAMPLING_ADDR:

Signal	SAMPLING_ADDR
RATE LF	0x8603
RATE HF	0x8609
ACC1 LF	0x860F
ACC1 HF	0x8615
ACC2 LF	0x861b
ACC2 HF	0x8621

2.2.5.6.2.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_11268

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1									SPAN							
CONF_OREG2					VARIANCE_EXPONENT						VARIANCE_SIGNIFICANT					
CONF_OREG3									AVERAGE							
	Field	Value	Meaning													
	SPAN	signal dependent	Max - Min of sampled values, always unsigned													
	VARIANCE_EXPONENT	signal dependent	The original variance value is calculated:													
	VARIANCE_SIGNIFICANT	signal dependent	Variance = VARIANCE_SIGNIFICANT * (2 ^ VARIANCE_EXPONENT)													
	AVERAGE	signal dependent	Average of sampled values, signed or unsigned according to SIGN parameter													

2.2.5.6.2.5 Possible error codes arranged in descending priority order

F02_11267

Code	Prio	Meaning	Causes
0x04	1	Read access error	Given address does not exist or a bus error has been detected
0x0D	2	Number of samples is out of range	2EXP_NO_OF_SAMPLES is greater than 11 or equal to zero
0x0E	3	Sampled value does not fit into a 32-bit word	(VALUE_LENGTH + VALUE_OFFSET) is greater than 31
0x0B	4	Wrong DSP signal parity	First occurred error was a wrong DSP signal parity (only can be valid if CHECK_MOD > 0x0)
0x0F	5	Temporary signal error occurred	First occurred error was a temporary signal error (only can be valid if CHECK_MOD = 0x1 or 0x2)
0x10	5	Permanent signal error occurred	First occurred error was a permanent signal error (only can be valid if CHECK_MOD = 0x1 or 0x2)
0x11	5	Signal is in INIT-phase	First occurred error was a signal INIT-phase error (only can be valid if CHECK_MOD = 0x1 or 0x2)

2.2.5.6.3 Service-ID 0x4: Read Config Value

2.2.5.6.3.1 Execution

F02_9550

The last device bank will be searched for the last written searched configuration value if the value is allowed to be read by White List. In case of no finding the value will be read from the corresponding location (Register, DSP or RAM) where it was written to by the Bootloader during startup or that read value represents the parameter reset value.

Risk: This procedure will give back false results if the requested value was modified by any other instance so that the value in the last device bank differ from its located copy.

2.2.5.6.3.2 Timing

F02_9551

Service is triggered in the interrupt and ends in the main cycle.

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2.2.5.6.3.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9552

In case of SCON Error Flags (all error flag weights are allowed to be read):

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0	0														ERROR_FLAG
CONF_IREG2																reserved
CONF_IREG3																reserved

Field	Values	Meaning
ERROR_FLAG	0x1 to 0xA0	SCON error flag number

In case of DSP Tuple (DSP Target Address has to be in White List to allowed to be read):

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1																DSP Target Address (see White List)
CONF_IREG2																reserved
CONF_IREG3																reserved

In case of Register Tuple (Register Target Address has to be in White List to allowed to be read):

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1																Register Target Address (see White List)
CONF_IREG2																reserved
CONF_IREG3																reserved

In case of RAM Tuple (RAM Target Address has to be in White List to allowed to be read):

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1																RAM Target Address (see White List)
CONF_IREG2																reserved
CONF_IREG3																reserved

In case of Block Tuple Entry (exact combination of parameters RT, LE and DESTINATION_ADDRESS has to be in White List to allowed to be read; ENTRY_NO must not exceed the maximum Block Tuple length defined in White List)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	1	1	1	1		reserved	RT	LE								ENTRY_NO
CONF_IREG2																Block Tuple Target Address
CONF_IREG3																reserved

Field	Values	Meaning
ENTRY_NO	<= maximum length	Block tuple entry number
LE (irrelevant if RT = 0)	0x0	Block tuple header address is the reference
	0x1	Block tuple last entry address is the reference
RT	0x0	Copy Block Tuple
	0x1	Reference Block Tuple
Block Tuple Target Address	(see right)	Address is given in the 16-bit form (see White List)

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2.2.5.6.3.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9553

	In case of Register, DSP and RAM Tuples as well as Reference Block Tuple Entry																															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
CONF_OREG1	FOUND_TUPLE[31:16]																															
CONF_OREG2	FOUND_TUPLE[15:0]																															
CONF_OREG3	reserved										LCN	reserved		LOCK																		
	In case of SCON Error Flags																															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
CONF_OREG1	0	0	ignored			EF_WGT		ERROR_FLAG																								
CONF_OREG2	reserved																															
CONF_OREG3	reserved										LCN	reserved		LOCK																		
	Field		Value		Meaning																											
	FOUND_TUPLE		value dependent		Found tuple																											
	ERROR_FLAG		0x1 to 0xA0		Searched SCON Error Flag number																											
	EF_WGT		0x0 to 0x3		Searched SCON Error Flag weight																											
	LOCK		0x0		D0 bank is open																											
			0x1		D0 bank is locked																											
	LCN *		0x0		Searched tuple was found in last device bank																											
			0x1		Searched tuple was not found in last device bank: FOUND_TUPLE contains its reset or bootloaded value																											
*	Entries in the last device bank have a higher priority and will be returned by the ConfigService if found (LCN = 0). If the requested entry is only found at address given in the requested tuple, this value will be returned (LCN = 1)																															
	Definition of last device bank dependent on D0 bank state:																															
	D0	Last device bank																														
	Open	New tuples can be added to Data OTP																														
	Locked	Data OTP cannot be written anymore																														

2.2.5.6.3.5 Possible error codes arranged in descending priority order

F02_9554

Code	Prio	Meaning	Causes
0x0D	1	Undefined parameter ID	None of above listed IDs has been passed to ConfigService
0x09	1	Entry is not in White List	Searched tuple is not in the White List: read access denied
0x0E	1	Requested Block Tuple entry number exceeds its size	Block Tuple size in White List is less than requested entry number
0x08	2	Module config not completed yet	Cannot read from device banks: M0 has not been locked yet
0x0F	3	Undefined SCON Error Flag number	Requested SCON Error Flag number does not exist
0x10	3	Requested Reference Block Tuple not found	Requested Reference Block Tuple has been found neither in RAM (its RAM reference address is invalid) nor in the last device bank
0x11	3	Copy Block Tuple header is not ascertainable from RAM	Copy Block Tuple header has been requested and not found in the last device bank; due to the nature of Copy Block Tuples it is impossible to get their header from RAM

2.2.5.6.4 Service-ID 0x5: Write Device Tuple

2.2.5.6.4.1 Execution

F02_9555

The configuration single or block tuple will be written in the last open device bank if the parameter is allowed to be written by White List. The device will be marked as defect by writing 0xFFFFFFFF into D0 CRC if a discrepancy between the written and the read OTP data is detected.

2.2.5.6.4.2 Timing

F02_9556

Service is triggered in the interrupt and ends in the main cycle.

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2.2.5.6.4.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9557

In case of DSP Tuple (parameter DSP_INDEX has to be in White List to allowed to be written)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CONF_IREG1						DSP Target Address (see White List)	PAR					DSP DATA[22:16]					
CONF_IREG2								DSP DATA[15:0]									
CONF_IREG3								reserved									

In case of Register Tuple (parameter ADDR has to be in White List to allowed to be written)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1								Register Target Address (see White List)								
CONF_IREG2								Data to be written in register								
CONF_IREG3								reserved								

In case of RAM Tuple (exact combination of parameters SZ and RAM_OFFSET has to be in White List to allowed to be written)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1								RAM Target Address (see White List)								
CONF_IREG2								Data to be written in RAM								
CONF_IREG3								reserved								

In case of Block Tuple there is a difference between the header of the Block Tuple and the entries (Block tuple has to be in White List to allowed to be written: The only exception is SCON Error Flag Block Tuple that is always allowed to be written)

Header (must be the first command in the sequence):

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CONF_IREG1	1	1	1	1	0	res.	RT	LE				BLOCK_SIZE_IN_WORDS					
CONF_IREG2								Block Tuple Target Address (see White List)									
CONF_IREG3								reserved									

Entries (must follow the header or previous entry after a successful feedback of the previous service call):

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	1	1	1	1	1											
CONF_IREG2								reserved								
CONF_IREG3								ENTRY[31:16]								

	Field	Values	Meaning
RT	0x0	Copy Block Tuple	
RT	0x1	Reference Block Tuple	
LE (irrelevant if RT = 0)	0x0	Block tuple header address is the reference	
LE (irrelevant if RT = 0)	0x1	Block tuple last entry address is the reference	
BLOCK_SIZE_IN_WORDS	0x1 to 0xFF	Number of entries to be written	
RAM_DATA	(see right)	Address is given in the compressed 16-bit form of 32-bit start address	
ENTRY *	(see right)	Entries will not be checked in White List	

* Independent on Block Tuple type, the numbering of the entries is always the same: the entry number one follows the header and so on

2.2.5.6.4.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9558

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1								WRITTEN DATA[31:16]								
CONF_OREG2								WRITTEN DATA[15:0]								
CONF_OREG3								reserved								

	Field	Value	Meaning
	WRITTEN DATA	(see right)	32bit data read back from the after writing

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2.2.5.6.4.5 Possible error codes arranged in descending priority order

F02_9559	Code	Prio	Meaning	Causes
	0x0F	1	Block Tuple size is zero	Size of a block tuple is not permitted to be zero
	0x0D	1	Implausible temporary parameters	Attempt to write a block tuple entry without its header before
	0x09	2	Entry is not in White List	Searched tuple is not in the White List: read access denied
	0x10	2	Undefined parameter ID	None of above listed IDs has been passed to ConfigService
	0x11	2	Requested Block Tuple entry number exceeds its size	Block Tuple size in White List is less than requested entry number
	0x12	2	Wrong size of Lower End Reference Block Tuple	Size of Lower End Reference Block Tuple must be equal to the size defined in White List
	0x0E	2	Entry number exceeds the previously declared block size	Block tuple size has been declared by writing a block tuple header. The number of entries written in a row exceeds the previously declared block tuple size
	0x06	3	Not enough free words in Data OTP	Service needs one free word in the Data OTP in case of Register, DSP or RAM tuple. A block tuple requires (1 + BLOCK SIZE IN WORDS) free words
	0x07	3	D0 is locked	Device configuration has finished and no data can be changed in the OTP
	0x08	3	Module config not completed yet	Cannot write into device banks: M0 has not been locked yet
	0x0A	4	Device is defect and cannot be used any more	Device has been marked as defect by writing 0xFFFFFFFF into D0 CRC because of a discrepancy between the written and the read OTP data
	0x0C	4	OTP programming failure	Error occurred during OTP programming

2.2.5.6.5 Service-ID 0x6: Lock Device Configuration Bank

2.2.5.6.5.1 Execution

F02_9560 The DSP checksum I or II will be calculated and written into the last open bank on demand. The last open bank will be locked. The M0 or D0 bank will be also locked on demand or when the last open bank is M7 or D3. The device will be marked as defect by writing 0xFFFFFFFF into M0 or D0 CRC if a discrepancy between written and read OTP data is detected or if a Data OTP CRC calculated in high margin read mode differs from calculated in low margin read mode.

2.2.5.6.5.2 Timing

F02_9561 Service is triggered in the interrupt and ends in the main cycle. Runtime depends on service input parameters.

2.2.5.6.5.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9562	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CONF_IREG1																CHS2	D0L
CONF_IREG2																	
CONF_IREG3																	
reserved																	
Field																	
D0L				Value													
				Meaning													
CHS2				0x0													
				Only the last open bank will be locked													
				0x1													
				Both the last open device bank and the D0 bank will be locked - no change in OTP will be possible after													
				0x0													
				DSP Checksum 2 will not be calculated and written													
				0x1													
				DSP Checksum 2 will be calculated and written into the last open bank before locking													

Notes:

1. The service always locks D0 if the last open bank is D3.
2. If the last open bank is empty and no checksum is requested to be calculated (so it remains empty), the CRC of this bank will be calculated including only a stop tuple and then the bank will be locked. Exception: if the last open bank is D3, it will not be closed (which means no D3 CRC and no D3 end address in D0 will be written. The header bank D0 will be locked instead).

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3. If D0 is requested to be locked and the last open bank is empty and no checksum is requested to be calculated (so it remains empty), only the D0 bank will be locked. The CRC of the last open bank and its end address will not be written.

9. The service searches through the last open bank for DSP tuples (DSP indexes 41 to 44 for Checksum II) and uses them for the calculation. If a tuple cannot be found in the last open bank, the appropriate value will be fetched directly from the DSP. Hence, it is important to reset the sensor after locking a bank if this bank contains a DSP tuple for the fine adjustment trim data area because the trim data will only be parsed into the DSP by bootloader after resetting.

2.2.5.6.5.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9563

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
CONF_OREG1						reserved					DOL	DXL	MOL	MXL								
CONF_OREG2						reserved																
CONF_OREG3						reserved																
	Field					Value					Meaning											
MXL (Mx locked)	0x1 to 0x6					Number of module bank that has been locked																
	0x7					When M7 is locked or M0 is locked or both (indicates that module banks cannot be written anymore)																
MOL (M0 locked)	0x0					M0 is open																
	0x1					M0 is locked																
DXL (Dx locked)	0x0 to 0x2					Number of device bank that has been locked																
	0x3					When D3 is locked or D0 is locked or both (indicates that device banks cannot be written anymore)																
DOL (D0 locked)	0x0					D0 is open																
	0x1					D0 is locked																

Note:

Since the module banks are locked when the SMI7 module is being delivered, MXL is always 0x7 and MOL is always 0x1 during device configuration

2.2.5.6.5.5 Possible error codes arranged in descending priority order

F02_9564

Code	Prio	Meaning	Causes
0x0D	1	Undefined parameter Header Lock	Both M0 and D0 are required to be locked: invalid request
0x0E	2	Undefined parameter Required CheckSum	Both CheckSum I and CheckSum II are required to be calculated: invalid request
0x07	3	D0 is locked	D0 is locked, no changes on Data OTP are possible
0x0F	4	M0 is requested to be locked but it had been locked already	M0 had been locked already
0x10	5	D0 is required to be locked but M0 is still open	M0 has to be locked before this step
0x06	6	Not enough free words in Data OTP	No free word in the last open device bank for requested DSP Checksum I or II
0x0A	7	Device is defect and cannot be used any more	Device has been marked as defect by writing 0xFFFFFFFF into M0 or D0 CRC because of a discrepancy between the written and the read OTP data or a difference between CRC in high and low margin read mode

2.2.5.6.6 Service-ID 0x7: Fine Offset Calibration

2.2.5.6.6.1 Execution

F02_9565

The DSP fine offset calibration parameter "O_fine" is set to its minimum und an average value is calculated over the given number of samples. Then O_fine is set to the maximum and an average value is calculated in the same way. Afterwards, a correcting O_fine is calculated and stored into the last open device bank. All channels are sampled in parallel. After changing O_fine a filter flush time delay is considered.

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2.2.5.6.6.2 Timing

F02_9566

Service is triggered in the interrupt and ends in the main cycle. Runtime depends on the DSP filter settings, number of samples and number of selected channels.

2.2.5.6.6.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9567

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0													
CONF_IREG1	RATE	ACC1	ACC2													LOG2_NO_OF_SAMPLES													
CONF_IREG2																NOMINAL_VALUE_ACC1													
CONF_IREG3																NOMINAL_VALUE_ACC2													
Field																													
LOG2_NO_OF_SAMPLES				Value				Meaning																					
				0x1 to 0xF				Number of samples to be taken is calculated as (2 ^ LOG2_NO_OF_SAMPLES)																					
ACC2 *				0x0 to 0x1				Flag to calibrate acceleration signal 2																					
ACC1 *				0x0 to 0x1				Flag to calibrate acceleration signal 1																					
RATE **				0x0 to 0x1				Flag to calibrate rate signal																					
NOMINAL_VALUE_ACC1				0x13EC through 0x0 to				Values as a reference for ACC1 and ACC2 (2's complement), corresponds to -5100 ... + 5100																					
NOMINAL_VALUE_ACC2				0xEC14																									
*																													
* The acceleration signal is calibrated towards the value given in the corresponding NOMINAL_VALUE_ACC_X (if flag is set). The nominal value parameter enables a calibration of a sensor mounted with its sensing direction not orthogonal to gravity.																													
** The rate signal is always calibrated to 0.																													

2.2.5.6.6.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9568

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1																reserved
CONF_OREG2																reserved
CONF_OREG3																reserved

2.2.5.6.6.5 Possible error codes arranged in descending priority order

F02_9569

Code	Prio	Meaning	Causes
0x0D	1	No channel has to be calibrated	At least one channel must be selected for calibration (RATE = ACC1 = ACC2 = 0)
0x0E	2	Number of samples is too small	Invalid number of samples (LOG2_NO_OF_SAMPLES = 0)
0x0F	3	Invalid Acc1 nominal values	NOMINAL_VALUE_ACC1 exceeds the limit
0x10	4	Invalid Acc2 nominal values	NOMINAL_VALUE_ACC2 exceeds the limit
0x08	5	Module config not completed yet	Cannot write into device banks: M0 has not been locked yet
0x07	6	D0 is locked	Device configuration has finished and no data can be changed in the OTP
0x06	7	Not enough free words in Data OTP	Service needs one free word in Data OTP for each selected channels plus one free word because one DSP tuple with Checksum II will also be needed later
0x0B	8	DSP parity failure	Read DSP signal has a wrong parity
0x0C	9	OTP programming failure	Error occurred during OTP programming
0x11	9	Signal cannot be adjusted	Output signal cannot be changed by adjusting the O_fine parameters (i.e. deviation from nominal value too large)
0x12	9	Wrong sensor position	Given nominal value cannot be achieved
0x13	9	Write verification check failed	Written DSP tuple will be overwritten with NOP tuple

2.2.5.6.7 Service-ID 0x8: Read Memory (restricted to production memory in Data OTP)

2.2.5.6.7.1 Execution

F02_9570

Read data from the given address within production memory in the Data OTP and store it into Config Output registers. Report back an error if the reading failed.

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2.2.5.6.7.2 Timing

F02_9571 Service is triggered and ends in the interrupt.

2.2.5.6.7.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9572

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1																READ_ADDRESS
CONF_IREG2																reserved
CONF_IREG3																reserved

The parameter read address is given in the compressed 16bit format. The 16 bit addresses of production memory are shown in the table below:

	Full 32bit address	READ_ADDRESS (16bit)
Dev. Prod.	0x0000E04C	0x3813
	0x0000E048	0x3812
	0x0000E044	0x3811
	0x0000E040	0x3810
Mod. Prod.	0x0000E03C	0x380F
	0x0000E038	0x380E
	0x0000E034	0x380D
	0x0000E030	0x380C

2.2.5.6.7.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9573

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1																READ_ADDRESS
CONF_OREG2																CONTENT[15:0]
CONF_OREG3																CONTENT[31:16]

2.2.5.6.7.5 Possible error codes arranged in descending priority order

F02_9574

Code	Prio	Meaning	Causes
0x03	1	Service is protected	Disable Config Service Protection must be called first
0x04	2	Read access error	Given address does not exist or a bus error has been detected

2.2.5.6.8 Service-ID 0xB: Activate Error Memory

2.2.5.6.8.1 Execution

F02_9585 Read the content of the first entry in the error memory area und write the given activation marker into this address if the given activation marker is greater than zero and the first entry in the error memory area has not been written yet. Read error memory entries on demand.

2.2.5.6.8.2 Timing

F02_9586 Service is triggered and ends in the interrupt if the activation marker has been written already or the service has only to read it. Otherwise the service ends in the main cycle; runtime depends on OTP programming.

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2.2.5.6.8.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9587

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1																ACTIVATION_MARKER[15:0]
CONF_IREG2																reserved
CONF_IREG3																reserved
	Field		Value		Meaning											
	ACTIVATION_MARKER		0x0		The error memory activation status remains unchanged. This parameter value is used for only reading the entries in the error memory area											
			all others		If error memory has not been activated already, it will be by storing the ACTIVATION_MARKER to the first entry of the error memory. Otherwise the parameter will be ignored											
	ERR_ENTRY_NO		0x0		Reading the activation marker without bits [31:16]											
			0x1 to 0x7		Number of Error Memory entry to be read (reading is only possible if the error memory has been activated already)											
*	The error memory is activated by writing a first entry to the error memory. This entry is not be treated as an error entry, but just as an activation marker. As long as the activation marker is zero, no errors are written to the error memory.															

2.2.5.6.8.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9588

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1																ERR_MEM_CONTENT[15:0]
CONF_OREG2																ERR_MEM_CONTENT[31:16]
CONF_OREG3																reserved
	Field		Value		Meaning											
	ERR_MEM_CONTENT		0x0		If AS = 0x0: Error memory is not active, access denied If AS = 0x1: Empty entry											
			all others		Content of error memory entry according to ERR_ENTRY_NO Only bits [15:0] are relevant when ERR_ENTRY_NO = 0											
	AS (Activation Status)		0x0		Error memory is not active											
			0x1		Error memory is active											

2.2.5.6.8.5 Possible error codes arranged in descending priority order

F02_9589

	Code	Prio	Meaning	Causes
	0x0C	1	OTP programming failure	Error occurred during OTP programming

2.2.5.6.9 Service-ID 0xC: Cyclic Output of Error Counters

2.2.5.6.9.1 Execution

F02_9590

The error counter values are sent regularly on CAN with the interval given. The error counter transmission is stopped (again) by calling the same service with the interval equal to zero.

2.2.5.6.9.2 Timing

F02_9591

Service is triggered and ends in the interrupt. The function called by service runs until sensor reset or its cancellation by the service with the parameter INTERVAL = 0.

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2.2.5.6.9.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9592

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CONF_IREG1	reserved								KQC	SEF	INTERVAL						
CONF_IREG2	reserved																
CONF_IREG3	reserved																
	Field								Value								Meaning
KQC (KEEP QUIET CUSTOMER)								0x0	Reactivate CAN communication on customer CAN protocol								
SEF (SPECIAL ERROR FLAGS)								0x0	Error counters are send out without SPECIAL_ERROR_FLAGS information								
INTERVAL								0x1	Output of SPECIAL_ERROR_FLAGS is activated								
INTERVAL								0x0 to 0x7F	An Error Counter Message is generated every INTERVAL ms.								

2.2.5.6.9.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9593

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	reserved															
CONF_OREG2	reserved															
CONF_OREG3	reserved															

2.2.5.6.9.5 Possible error codes arranged in descending priority order

F02_9594

None.

2.2.5.6.10 Service-ID 0xD: Manual BITE trigger

2.2.5.6.10.1 Execution

F02_9595

Check whether the command combination is valid and then proceed according to the request. In case of running dynamic BITE it is not allowed to start a new BITE.

2.2.5.6.10.2 Timing

F02_9596

Function is triggered in the interrupt and ends in the main cycle.

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2.2.5.6.10.3 Input parameters (CONF_IREG1...CONF_IREG3)

F02_9597

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	reserved							BITE_TYPE	reserved	ACC_BITE	reserved	RATE_BITE				
CONF_IREG2	reserved															
CONF_IREG3	reserved															
Field	Values							Meaning								
BITE_TYPE *	0x0							Trigger a static BITE								
	0x1							Trigger a dynamic BITE sequence								
	0x2 to 0x3							Request BITE status without change								

* All BITE trigger requests (BITE_TYPE = 0x0 or 0x1) will be rejected while a dynamic BITE is running.
Status requests (BITE_TYPE = 0x2 or 0x3) are always allowed.

Parameters for a static BITE (BITE_TYPE = 0x0)

Field	Values	Meaning
ACC_BITE	0x0 to 0x1	Switch off Static ACC BITE
	0x2	Start negative phase of static ACC BITE
	0x3	Start positive phase of static ACC BITE
RATE_BITE	0x0	Switch off static YRS BITE
	0x1	Start zero phase of static YRS BITE
	0x2	Start positive phase of static YRS BITE
	0x3	Start negative phase of static YRS BITE

Parameters for a dynamic BITE (BITE_TYPE = 0x1)

Field	Values	Meaning
ACC_BITE	0x0 to 0x2	Do not start dynamic ACC BITE
	0x3	Start dynamic ACC BITE
RATE_BITE	0x0 to 0x2	Do not start dynamic YRS BITE
	0x3	Start dynamic YRS BITE

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2.2.5.6.10.4 Output parameters (CONF_OREG1...CONF_OREG3)

F02_9598

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1							reserved	BITE_TYPE	reserved	ACC_BITE	reserved	reserved	RATE_BITE			
CONF_OREG2									reserved							
CONF_OREG3									reserved							
Field	Value														Meaning	
BITE_TYPE	0x0														Static BITE active (or all BITEs are off, in case that ACC_BITE = 00 and YRS_BITE = 00)	
	0x1														Dynamic BITE sequence is running	
Parameters of a Static BITE (BITE_TYPE = 0x0)																
Field	Values														Meaning	
ACC_BITE	0x0														Static ACC BITE is off	
	0x2														Negative phase of static ACC BITE	
	0x3														Positive phase of static ACC BITE	
RATE_BITE	0x0														Static YRS BITE is off	
	0x1														Zero phase of static YRS BITE	
	0x2														Positive phase of static YRS BITE	
	0x3														Negative phase of static YRS BITE	
Parameters of a Dynamic BITE (BITE_TYPE = 0x1)																
Field	Values														Meaning	
ACC_BITE	0x0														Dynamic ACC BITE is off	
	0x2														Negative phase of dynamic ACC BITE	
	0x3														Positive phase of dynamic ACC BITE	
RATE_BITE	0x0														Dynamic YRS BITE is off	
	0x1														Zero phase of dynamic YRS BITE	
	0x2														Positive phase of dynamic YRS BITE	
	0x3														Negative phase of dynamic YRS BITE	

2.2.5.6.10.5 Possible error codes arranged in descending priority order

F02_9599

Code	Prio	Meaning	Causes
0xD	1	Attempt to start a dynamic BITE with wrong parameters	If a dynamic BITE is requested, either one or both parameters ACC_BITE and RATE_BITE have to be set to 0x3 (Start dynamic BITE)
0xE	2	Dynamic BITE is running	All BITE trigger requests are rejected while a dynamic BITE is running

2.2.6 Programming examples

F02_136

The programming examples assume OTP programming using config services via SPI. Programming via BiDir PSI or MessCAN is similar with appropriate settings for the parameters Origin and AR in CONF_IREG0.

2.2.6.1 Example 1: Register Tuple Programming (Reset Vector)

F02_11277

- Reset Vector target address (16 bit): 0x850D
- Assumption for new Reset Vector value: 0x100F (DCAN_off bit="1", other bits in default configuration)

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2.2.6.1.1 Input Registers to be written, writing CONF_IREG0 triggers service

F02_11280

	Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value
CONF_IREG3	Reserved																0x0	
CONF_IREG2	0x0																0x0	
CONF_IREG1	Data to be written																0x100F	
CONF_IREG0	0x100F																0x850D	
CONF_IREG0	Register Target Address								0x850D								0x850D	
CONF_IREG0	Reserved								Service ID		Origin		AR		0x0		0x5C	
CONF_IREG0	0x0								0x5		0x3		0x0		0x0		0x5C	

2.2.6.1.2 Output registers to be checked against expected value when service is done

F02_11281

Service is done when status field in CONF_OREG0 = 0x0.

	Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value			
CONF_OREG3	Reserved																0x0				
CONF_OREG2	0x0																0x0				
CONF_OREG1	WRITTEN_DATA[31:16]																0x100F				
CONF_OREG1	0x100F																0x850D				
CONF_OREG0	WRITTEN_DATA[15:0]																0x850D				
CONF_OREG0	0x850D								Error Code		Status		res		Service ID		Origin		AR		0x5C
CONF_OREG0	0x0								0x0		0		0x5		0x3		0x0		0x0		0x5C

2.2.6.2 Example 2: DSP Tuple Programming (LF filter)

F02_11276

- LF_mode target address (8 bit): 0x69
- Assumption for new LF_mode_LF_switch: 0x180 (LF4 filter selected, i.e. LF_switch=LF_mode_LF_switch[8:7]=0x3)
- Odd Parity bit for DSP value 0x180 is "1"

2.2.6.2.1 Input Registers to be written, writing CONF_IREG0 triggers service

F02_11283

	Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value	
CONF_IREG3	Reserved																0x0		
CONF_IREG2	0x0																0x0		
CONF_IREG1	DSP DATA[15:0]																0x180		
CONF_IREG1	0x180																0x6980		
CONF_IREG0	DSP Target Address								Par		DSP DATA[22:16]								0x6980
CONF_IREG0	0x69								1		0x0								0x6980
CONF_IREG0	Reserved								Service ID		Origin		AR		0x0		0x5C		
CONF_IREG0	0x0								0x5		0x3		0x0		0x0		0x5C		

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2.2.6.2.2 Output registers to be checked against expected value when service is done

F02_11282 Service is done when status field in CONF_OREG0 = 0x0.

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value				
CONF_OREG3																	Reserved 0x0				
CONF_OREG2																	WRITTEN_DATA[31:16] 0x180				
CONF_OREG1																	WRITTEN_DATA[15:0] 0x690D				
CONF_OREG0																	Error Code 0x0				
																Status 0x0	res 0	Service ID 0x5	Origin 0x3	AR 0x0	0x5C

2.2.6.3 Example 3: RAM Tuple Programming (LF filter flush time)

F02_11275 - InitFlushTimeForLfChannels target address (16 bit): 0xE003

- Assumption for new LF flush time (in ms): 30=0x1E

2.2.6.3.1 Input Registers to be written, writing CONF_IREG0 triggers service

F02_11285

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value		
CONF_IREG3																	Reserved 0x0		
CONF_IREG2																	RAM Data 0x1E		
CONF_IREG1																	RAM Target Address 0xE003		
CONF_IREG0																	Reserved 0x0		
																Service ID 0x5	Origin 0x3	AR 0x0	0x5C

2.2.6.3.2 Output registers to be checked against expected value when service is done

F02_11284

Service is done when status field in CONF_OREG0 = 0x0.

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value				
CONF_OREG3																	Reserved 0x0				
CONF_OREG2																	WRITTEN_DATA[31:16] 0x1E				
CONF_OREG1																	WRITTEN_DATA[15:0] 0xE003				
CONF_OREG0																	Error Code 0x0				
																Status 0x0	res 0	Service ID 0x5	Origin 0x3	AR 0x0	0x5C

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2.2.6.4 Example 4: Error Flag Weight Reconfiguration

F02_11274 Error flag weight configuration is done using a block tuple with:

- Block Tuple target address = 0x4006
- RT = 0x1
- LE = 0x0
- BLOCK_SIZE_IN_WORDS = #flags to be reconfigured / 3, rounded up, i.e.: 1...3 flags: 1 block; 4...6 flags: 2 blocks, ...

2.2.6.4.1 Layout of 32bit data blocks for error flag reconfiguration

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Meaning	Flag No. 3				Flag No. 2				Flag No. 1				res.	Wt. 3	Wt. 2	Wt. 1																

Flag No. 1...3: Number of SCON error flag to be reconfigured (0: no flag to be reconfigured)

Wt. 1...3: New flag weights for Flags No. 1...3

2.2.6.4.2 Input registers to be written, block tuple header

F02_11287 Assumption: reconfiguration of flag v_prereg_low (flag number 0xC) to the new weight 0x3 (i.e. flag is masked) → 1 block required.

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 <th>Overall value</th>	Overall value						
CONF_IREG3	Reserved																0x0						
	0x0																						
CONF_IREG2	Block tuple target address																0x4006						
	0x4006																						
CONF_IREG1	Block tuple ID	0	res	RT	LE	BLOCK_SIZE_IN_WORDS										0xF201							
	0xF	0	0	1	0	1																	
CONF_IREG0	Reserved				Service ID		Origin	AR									0x5C						
	0x0				0x5		0x3	0x0															

2.2.6.4.3 Input registers to be written, 1. data block

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 <th>Overall value</th>	Overall value
CONF_IREG3	Entry[15:0]																0xC03
CONF_IREG2	Entry[31:16]																
CONF_IREG1	Block tuple ID	1	reserved														0xF800
CONF_IREG0		0xF	1	0x0													



2.2.6.5 Example 5: Device Configuration Bank Locking

F02_11278

Assumptions:

- DSP Checksum2 is to be calculated, i.e. fine offset calibration executed or filter setting changed in current open bank,
- current open bank to be locked is D2,
- D0 is not to be locked, i.e. further programming steps are possible after having locked current bank.

2.2.6.5.1 Input Registers to be written, writing CONF_IREG0 triggers service

F02_11292

	Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value
CONF_IREG3		Reserved															0x0	
		0x0															0x0	
CONF_IREG2		Reserved															0x0	
		0x0															0x0	
CONF_IREG1		Reserved															0x2	
		0x0															0x2	
CONF_IREG0		Reserved				Service ID			Origin		AR		0x0				0x6C	
		0x0				0x6			0x3		0x0		0x0				0x6C	

2.2.6.5.2 Output registers to be checked against expected value when service is done

F02_11291

Service is done when status field in CONF_OREG0 = 0x0.

	Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Overall value		
CONF_OREG3		Reserved															0x0			
		0x0															0x0			
CONF_OREG2		Reserved															0x0			
		0x0															0x0			
CONF_OREG1						DOL		DXL		MOL		MXL				0x2F				
						0		0x2		1		0x7				0x2F				
CONF_OREG0		Error Code		Status		res		Service ID			Origin		AR		0x0					
		0x0		0x0		0		0x6			0x3		0x0		0x0					

2.3 Module processing for device building

F02_8025

The modules will be double sided solderable with common reflow lead containing and lead free solder processes. Modules withstand up to 3 reflow lead free solder cycles.

The lead free solder process is specified in attached document [13]. Processing on AE manufacturing lines will be possible. ~~If necessary the package will be released on AE manufacturing lines.~~ Typical vibration and shocks for electronic device manufacturing will be survived without any special measures. The maximal vibration allowed during processing (press in, soldering, milling ...) will be derived during product development.

Parts will be packaged in a suitable transport package (roll, tray ...) which offers suitable lifetime, ESD and vibration protection. Fall tests at module level will be passed in the transport package. Transport package will be usable in any AE manufacturing plant.

The module can be processed according to MSL 3 (JEDEC-standard, including storage and soldering) within a Pb-free soldering process. Product-classification according MSL1 will be proved during product

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development. Dip and spray coating must be avoided due to negative performance effects, e.g. stress, shifting of modes or BLR. Sensor performance can not be guaranteed with coating or usage of under-fill.

Unintended splashes/spots of PCB lacquer/coating do not impair sensor performance when less than 20% of the SMI7 surface is affected (lacquer thickness ~50µm). It must be ensured, that no lacquer connections/bridges between sensor and PCB occur, otherwise loss of contact might occur upon aging (temperature cycles). It must be ensured, that wet lacquer slashes do not act as getter for larger particles or metallic particles as they could impair sensor performance. Legibility of the sensor labeling can be deteriorated by lacquer spots.

Component will be recyclable. No sensor specific test over temperature or at a non ambient temperature (~25°C) after soldering will be necessary to achieve any performance or quality goals.
calibration. Address to read out correction values will be defined within A-Samples.

During ramp-up of the ECU the following sensor parameters should be tested:

F02_8048

¹ Hint: Sensitivity-effects in combination with permanent acceleration (e.g. 1g application) could be wrongly interpreted as offset (e.g. 1g with 1% sensitivity error equals 10mg).

F02_144

Table 5: Sensor parameters

Komponente	Messgröße	Position	Temperaturen
ACC1, ACC2	Offset ACC1,2	beliebig aber stabil und fest	Temperaturrampen
DRS	Offset , Rauschen und Quadl DRS	beliebig aber stabil und fest	Temperaturrampen

F02_8047

The measured values should be clearly allocated to the individual sensor. The recommended number of parts tested for the ramp-up evaluation is about 10.000 sensors for the first platform (corresponding to the AE ramp-up procedure). For following platforms number of sensors depending on variation and experience of predecessor.

Test or adjustments (locking, reset-vector ...) at ECU level using SPI-protocol will not take longer than 5s. Fine offset calibration takes a certain time depending on the used parameters and filters.
No additional measurements after ramp-up (ECU, ...) are necessary to fulfill the quality targets of the module.

Usage of different CAN-Protocols or optional SW can take longer depending on the interface or data volume. E.g. the PSI sync. pulse may be used for bidirectional communication. Timing estimations can be found here: section 1.3.3

A pad geometry for the solder pads will be provided. This pad geometry is suitable for X-ray inspection (AE QSV) and will be optimized or optimized orientation after soldering (Einschwimmverhalten). Layout for A-samples and dimensions can be found in chapter 2.4.1.

F02_149

The strain in the plane of the SMI7 sensor elements due to bending of the PCB has to be less than 500µm/m to achieve described sensor performance. A strain of 1100µm/m can be applied during production process without sensor damaging.

Other stress effects within the PCB (geometry effects; humidity-changes; ...) are not known and specified today. Therefore such effects can not be covered within the described performance. If necessary they have to be handled by change requests.

F02_9391

Module will survive 1.2m free fall on concrete without damage or occurred damage will be indicated by the sensor electrical or mechanical.

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2.4 Sensor description and dimension

2.4.1 Sensor dimensions

F02_8049 Package type: BGA

Module dimensions: 7 x 7 x 1.5mm³.

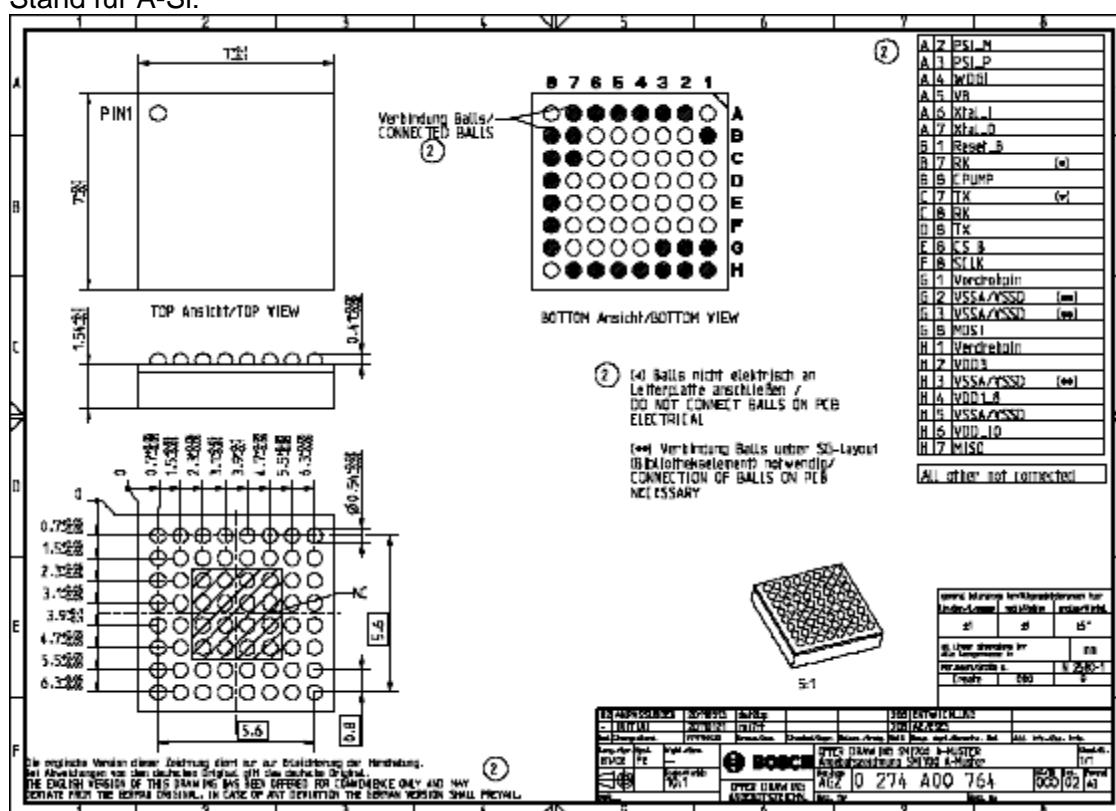
Weight w/o balls approx.: 0.164 g +/- 0.020 g

Weight w/- balls approx.: 0.195 g +/- 0.030 g

Following picture shws the dimensions and pinning for A-samples (Design for B-Samples can change till 02/2011):

F02_155

Stand für A-Si:





BOSCH

Reutlingen

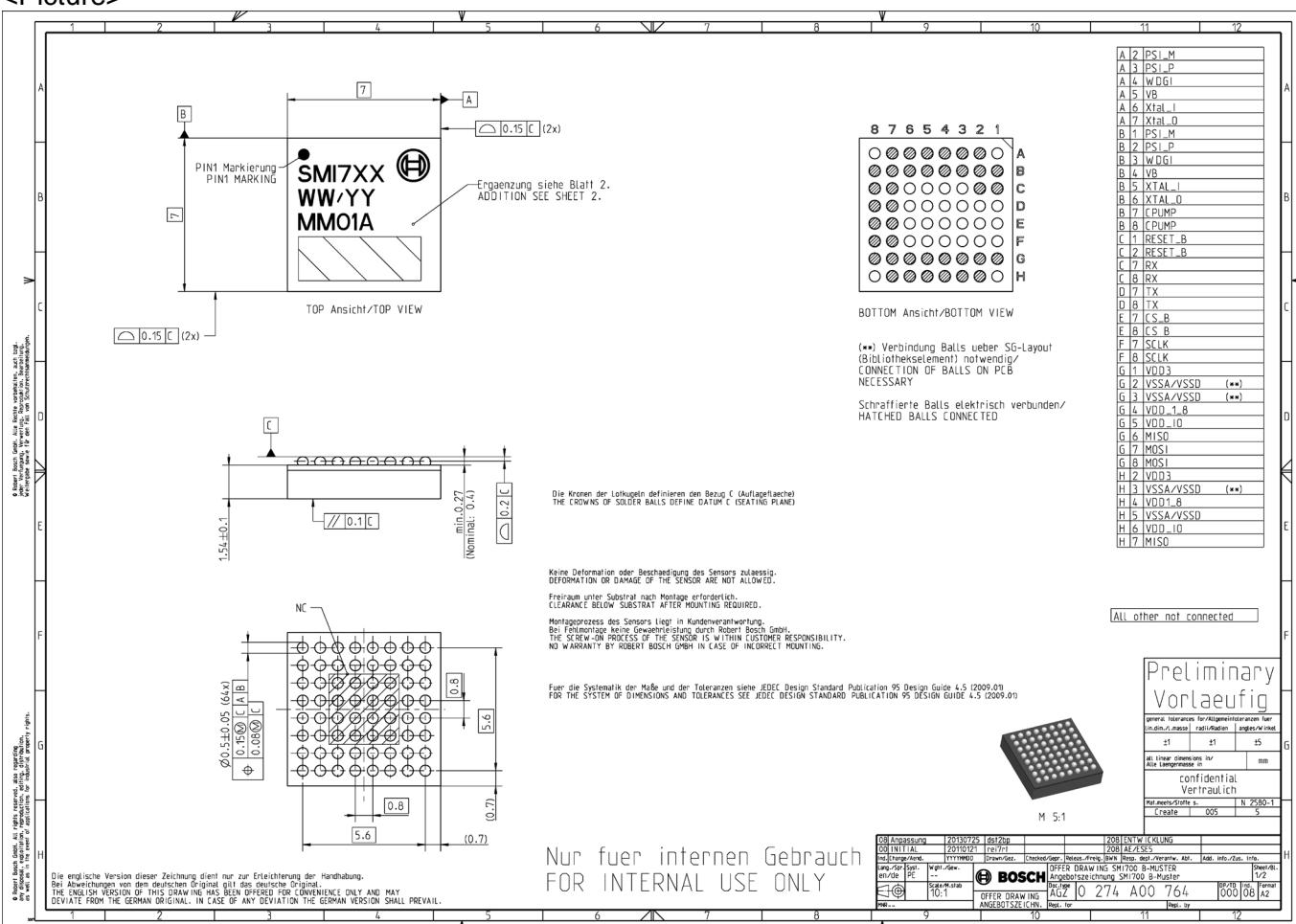
Data Sheet

SMI7

version 5.0
page - 44 / 301 -

F02_11093 Ab B-Si und Serienstand:

F02_11296 <Picture>



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BOSCH

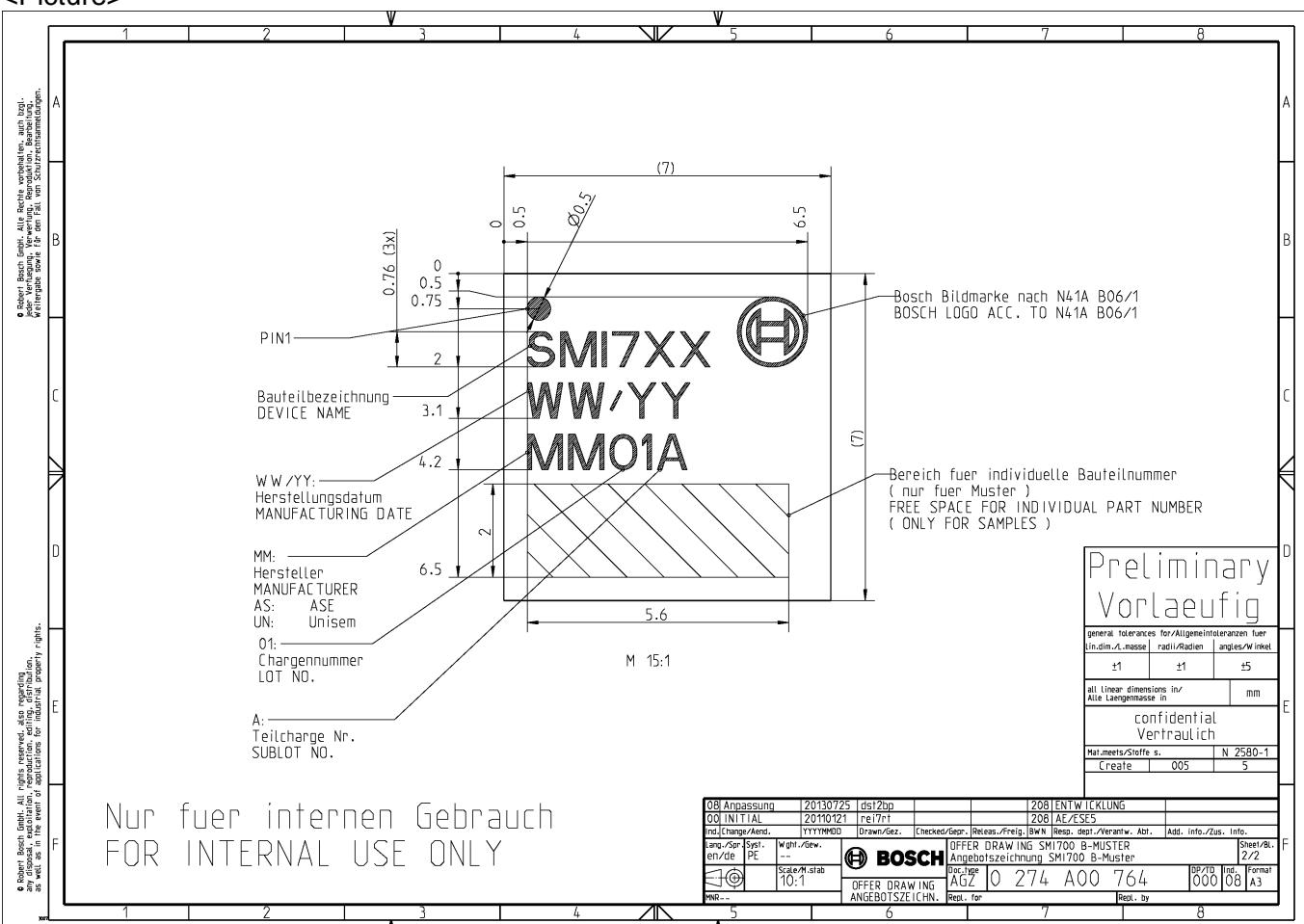
Reutlingen

Data Sheet

SMI7

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F02_11297 <Picture>



F02_11092 All pins not described in the table above are not connected and should be connected to GND.

F02_156 Orientation of the module can be verified electrically by an internal bridge between two pads or optical by pin 1 marking.

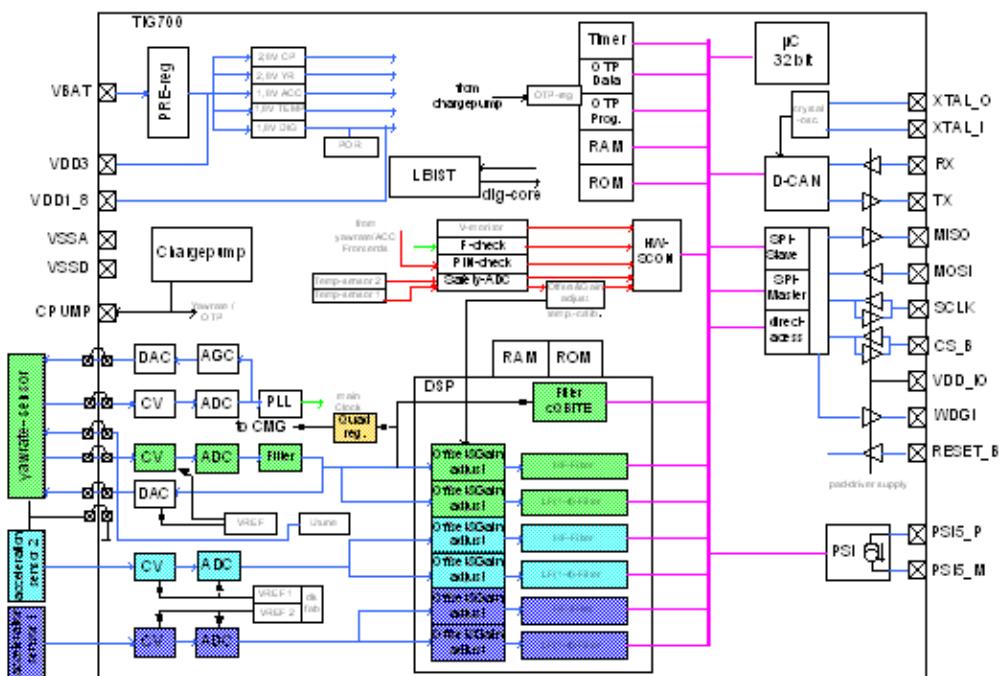
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2.5 Sensor types

2.5.1 Structural module overview

F02_159 Picture of simplified internal architecture:

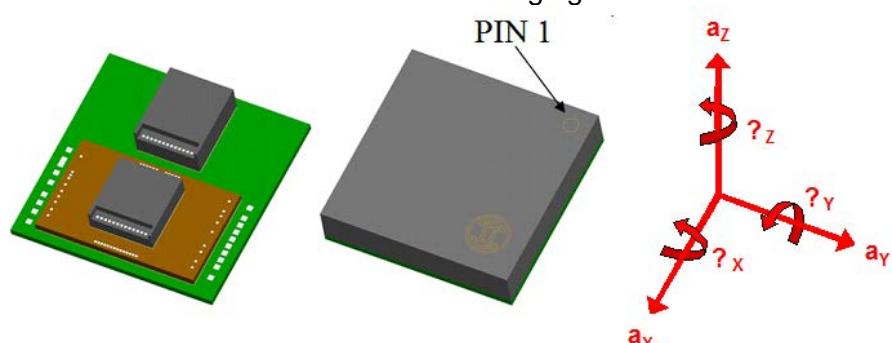


2.5.2 SMI700 & SMI710 Sensing Directions

F02_162 SMI700-Module is based on TIG700 (ASIC), CMG210M (z-sensorelement) and CMA621M (Axy-sensorelement).

SMI710-Module is based on TIG700 (ASIC), CMG240M (x-sensorelement) and CMA625M (Ayz-sensorelement).

Sensitive axes are shown in the following figure:



F02_9413 Hint: Following table shows the drive and sense direction of the yaw-rate elements:

Module	SMI700	SMI710
Drive Direction	ax ACC2	ay ACC1
Sense Direction	ay ACC1	az ACC2
Sense Axis	az (Ω_z)	ax (Ω_x)

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F02_11202

SMI700

Orientation in earth's gravity field				
ACC 1	+5000 LSB	0 LSB	-5000 LSB	0 LSB
ACC 2	0 LSB	+5000 LSB	0 LSB	-5000 LSB

SMI710

Orientation in earth's gravity field				
ACC 1	+5000 LSB	0 LSB	-5000 LSB	0 LSB
ACC 2	0 LSB	+5000 LSB	0 LSB	-5000 LSB

F02_11203 Values of the acceleration channels for different orientations of the sensor module relative to the earth's surface

2.6 Components

2.6.1 CMG240M (Ω_x -sensorelement)

F02_171 First datasheet will be provided with A-samples and can be found in [04].

2.6.2 CMG210M (Ω_z -sensorelement)

F02_173 First datasheet will be provided with A-samples and can be found in [05]

2.6.3 CMA621M (Axy-sensorelement)

F02_175 First datasheet will be provided with A-samples and can be found in [06]

2.6.4 CMA625M (Ayz-sensorelement)

F02_177 First datasheet will be provided with A-samples and can be found in [07]

2.6.5 TIG700 (ASIC)

F02_8050 Fabrication number: TIG700

Fabrication process option: LBC8_A_30V_4ML_no_no_PB_HA_DW_BA_no_ND_NL_PL_CT

Number of masks: 33

Damascene copper used.

Critical dimensions: 180 nm

Design authorchip: AE/EIS

Bosch Type number: 1279.993.865

Packaging: only as chip on wafer available

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Description of the ASIC-architecture is shown in the following figure:

F02_188

26.3.2012

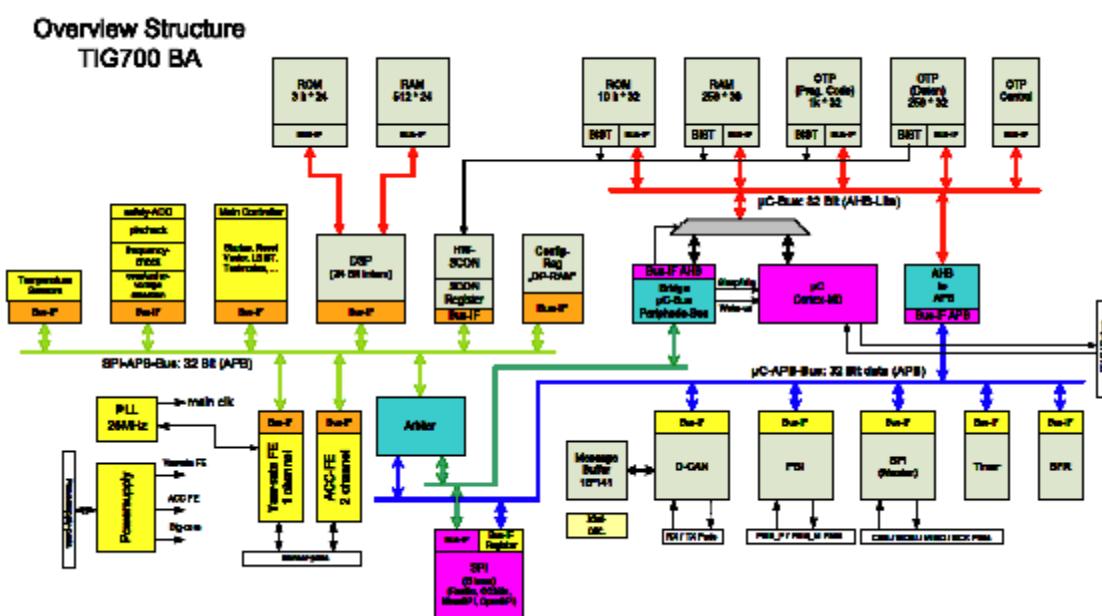


Figure 8: Bus structure TIG700

F02_11294

Available μC ressources for device specific customer software:

Memory ressources:

- RAM: 200B
- Code OTP: 4kB
- ROM: 6kB (only usable by metal fix)

Runtime:

- 1500 instructions per 500μs main cycle
- 700 instructions per 30μs in interrupt, every 500μs (only for SW running from ROM, metal fix required).

2.7 Sensor module overview

F02_192

The sensors, to be developed, SMI740 and SMI750 are capable of supplying all axis of freedom in combination. Functions will be fully proven with according methods (characterization, qualification ...) within the project. Sensor axes are also described in chapter 4.2 and 4.3. Additionally the system concept allows to be downscaled by e.g. bonding variants or turning off channels to the following options:

F02_193

Table 6: Bonding variants

Group	Variant	Description
1	SMI700 and SMI710	$\Omega zAxy, \Omega xAyz$
2	Single yaw-rate channel	$\Omega z, \Omega x$
3	Single yaw-rate channel + single acceleration channel	$\Omega zAx, \Omega zAy, \Omega zAz, \Omega xAx, \Omega xAy, \Omega xAz$
4	Different combination of sensor elements	$\Omega zAyz, \Omega xAxy$

F02_195

Function of group 2 & 3 will be proven by simple tests like bonding or programming variants.

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Function of group 4 will be proven by theoretical considerations. For group 2, 3 & 4 no characterization or qualification will be done. Cost and timing for development or release of such modules has to be negotiated, separately. The concept allows not realizing modules like shown in the following list:

F02_196

Table 7: Not realizing modules

Group	Variant	Description
5	Modules with more than one yaw-rate	e.g. $\Omega z \Omega x$
6	Modules with acceleration channels only	e.g. Axy
7	Modules that need new sensor elements	e.g. $\Omega x \Omega z$

2.8 Alphabetical list of acronym

F02_11087

apb - amber peripheral bus

ctm - chip temperature monitor

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3. Electrical interface

F03_199

Current direction into the module is counted positive.

3.1 Pinning

F03_201

Table 8: Pinning (see also 3.8.1)

#	Name	Function	I/O	Remarks
6	VB	Power supply	Power in; in for synch.- pulse detection	
10	VDD3	Power supply 3.3V; can provide additional 6mA for external IC	Power in/out	Must be connected to a blocking capacitance (see 3.8.1)
15	VDD1_8	Connection for external blocking cap	Out	Must be connected to a blocking capacitance (see 3.8.1)
16	VDD_IO	External power supply pin for CAN, SPI interface	Power in	WDGI and RESET also supplied by VDD_IO
1	PSI5_P	PSI5 data connection	Out for current sink	
2	PSI5_M	PSI5 ground	Power in	
11	VSSA/D = GND = VSSIO	Analog / digital ground	Power in	VSSA and VSSD and VSSIO are connected together internally to the BGA package, resulting in only one external GND pin (VSSA/D)
9	CPUMP	Connection for external capacitance	Out	Used for internal charge pump, must be connected to a capacitance (see 3.8.1)
3	XTAL_I	Connection for external crystal	In	20 MHz crystal
4	XTAL_O	Connection for external crystal	Out	20 MHz crystal
7	TX	Transfer CAN data	Out, high Z	Voltage level depends on VDD_IO
8	RX	Receive CAN-data	In, pull-up with at least 100kOhm	Voltage level depends on VDD_IO additionally used for SPI-ID identification
18	CS_B	Chip select for SPI	Slave: in pull-up with at least 100kOhm Master: Out, high Z	For SPI slave configuration this is input; for SPI master configuration it works as output driver. Pull-up is disconnected during master functionality. Voltage level depends on VDD_IO.
17	SCLK	SPI clock	Slave: in pull-up with at least 100kOhm Master: Out, high Z	For SPI slave configuration this is input, for SPI master configuration it works as output driver. pull-up is disconnected during master

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				functionality. Voltage level depends on VDD_IO.
12	MISO	SPI data output	Out, high Z	Regardless of slave or master configuration this is always the data output pin
14	MOSI	SPI data input	In, pull-up	Regardless of slave or master configuration this is always the data input pin
5	RESET	Reset-input, low active, same function as power-on reset	In, pull-down with at least 200kOhm	In PSI modes, reset has to be switched externally to VDD3. In case of PSI5 configuration VDD_IO must be put to VDD3. In this case RESET must be inactive and only internal power-on reset applies.
13	WDGI	Watchdog data	Out, high Z	If not used during PSI5 or CAN configuration, output is high Z; WDGI usage is only foreseen in combination with CA510

F03_1602 A Pin-FMEA (short to GND (VSSA/D), short to supply and short to any neighbor PIN or open behavior) will be provided. External components will be included in estimations; parameter drifts not.

3.2 Maximum ratings

F03_204 Values inside the specified maximum conditions must not damage the SMI7. No specification point is met at these ratings. SMI7 will be full functional after stimulation.

Table 9: Maximum ratings

Parameter / Condition	Min	Max	Unit
Maximum voltage at VB and PSI5_P relative to VSSA,VSSD	-0,3	20	V
Maximum voltage at VB and PSI5_P relative to VSSA,VSSD for reverse Voltage if current is limited to 140mA	-20	-0,3	V
Maximum voltage at VDD3 relative to VSSD	-0,3	3,6	V
Maximum voltage at VDD1_8 relative to VSSD	-0,3	2,0	V
Maximum voltage at VDD_IO relative to VSSD	-0,3	5,5	V
Maximum voltage at RX,TX, MOSI,MISO, SCLK,CS_B, WDGI and RESET relative to VSSD	-0,3	VDD_IO + 0,35 but max. 5,5	V
Maximum voltage at XTAL_I, XTAL_O relative to VSSD	-0,3	VDD1_8 + 0,3 but max. 2,0	V
Maximum junction temperature with applied supply voltage		175	°C
Maximum junction temperature without voltage applied (for example during soldering process)		260	°C
Maximum current at every pin without latchup except PSI5_P and PSI5_M	-100	100	mA
Maximum current at PSI5_P (together with VBAT) and PSI5_M (together with GND) without latchup	-140	140	mA

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3.3 Operating conditions

F03_207 Under the following conditions all specified values of acceleration sensor evaluation, yaw rate sensor evaluation and interface specifications (including pin specifications) are guaranteed.

Table 10: Operating conditions

	Parameter/Condition	Symbol	Max	Unit
Start-up timing 1	Early communication may happen and may not lead to illegal conditions or misleading. However SMI7 with applied MEMS-sensor may not respond or respond in a defined error state.	Ts1	50	ms
Start-up timing 2	SMI7 with applied MEMS sensor is full functional, including all initial self tests (with 15Hz filter)	Ts2	See section 5.4	ms

F03_210 After start-up timing 1 supply voltage will be monitored. Operating the sensor outside its specified voltage conditions leads to an observable error condition (flag). Sensor will be fully functional until over/undervoltage-detection-flag is set; see following figure:

F03_211

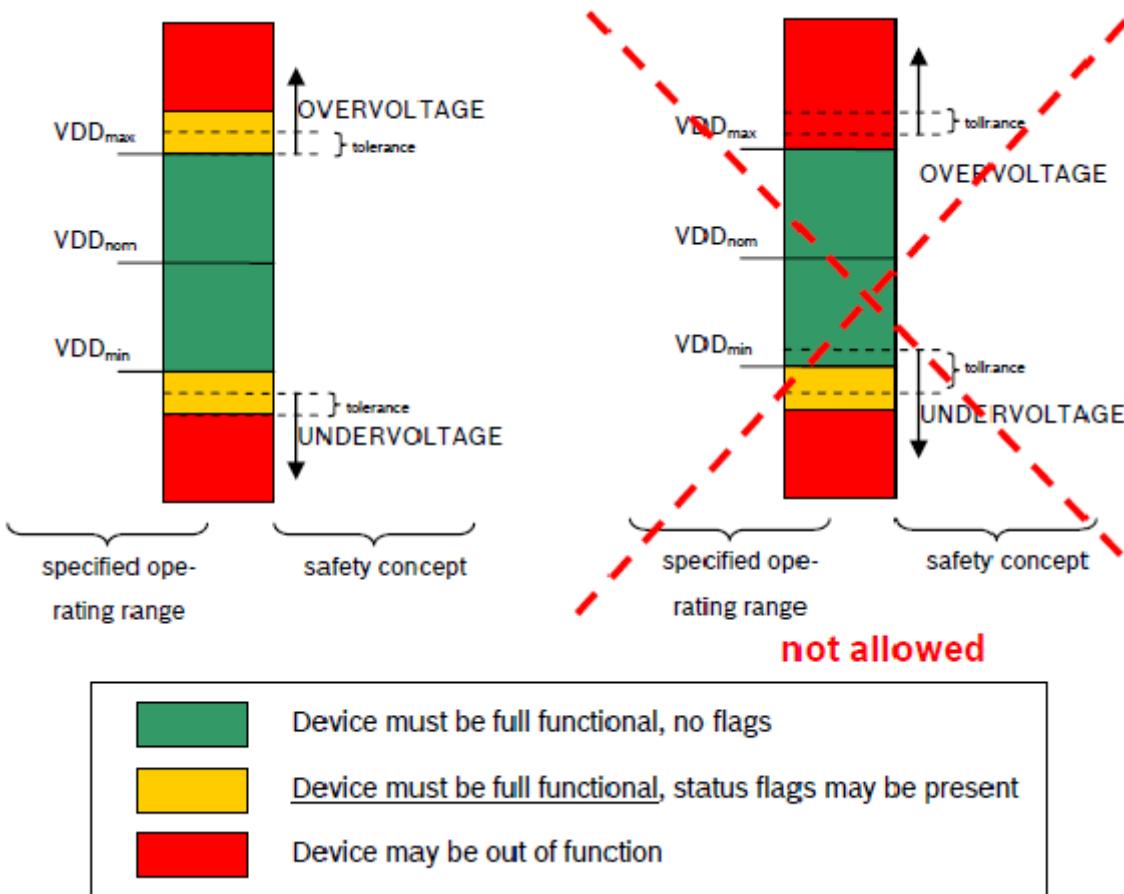


Figure 9: Over/undervoltage-detection

F03_16162 There is also a monitoring for the operating temperature inside the chip. Since

- 1) it must be guaranteed that no flag is set within the range of the specified operation conditions of the sensor and

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- 2) the calibration of the temperature inside the chip is not possible better than to an accuracy of several degrees,

the temperature flag cannot be taken as an indicator for the temperature range in which the full sensor performance is guaranteed (details see 7.4.6).

3.4 Pin specification

F03_213

All voltages described for VDD3 and VDD1_8 for output are specified after boot sequence has finished. This is due to the calibration of the on-chip voltage regulators. That is also valid for all monitoring values for over/undervoltage. Measurements are valid only after end of boot sequence, because they are also calibrated during wafer level test.

3.4.1 Electrical specification for VB

F03_8312

VB is the main power supply connection for PSI5 operation mode and 5V operation mode. The functionality of the synchronization pulse for PSI5 is also realized at the VB pin.

F03_222

Table 12: Electrical specification for VB

Parameter / Condition	Symbol	Min	Type	Max	Unit
Voltage range (incl. Sync. Pulse) (full specification for sensor evaluation)	VB	4,3		16,5	V
Voltage range (flagging, specification not fulfilled)	VB			4,3	V
Voltage range (reset occurs)	VB			3,8	V
Current consumption SPI/PSI mode ¹ (PLL frequency max., VB max., CAN deactivated, no secondary device, only modes 1...5)	Ivb			29	mA
Current consumption CAN mode (PLL frequency max., VB max., crystal oscillator at 20MHz, no secondary device, only modes 1...5)	Ivb_CAN			31	mA
Current consumption during active reset (PLL frequency max., VB max., crystal oscillator at 20MHz, no secondary device, only modes 1...5)	Ivb_reset	3		20	mA
Current consumption SPI/PSI mode with externally attached device ¹ (PLL frequency max., VB max., CAN deactivated, secondary device attached, only mode 6, secondary device must not exceed 6mA current consumption)	Ivb6			35	mA
Voltage monitoring range, low level ² (full specification for sensor evaluation guaranteed)	VB_ML	see {REF:F07_98 98}		see {REF:F07 _9898}	V
Voltage monitoring range, high level 1 (full specification for sensor evaluation guaranteed)	VB_MH1				V
Voltage monitoring range, high level 2 (full specification for sensor evaluation guaranteed)	VB_MH2	see {REF:F07_98 97}		see {REF:F07 _9897}	V
Voltage ripple at VB without setting any failure	F_RIP_V			340	mVpp

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flags. (Frequency range for ripple: DC to 1MHz) Measurement method as defined in <u>PH_SMI7xx_Measurement_And_Validation_work.doc#psrr</u> <u><PH_SMI7xx_Measurement_And_Validation_work.doc></u>	B				
Slope of power supply at VB	DVSUP	0,2			V/s
Slope of power supply at VB	DVSUP		200	V/ μ s	
Settling time for quiescent current	tSET		25.0	ms	

F03_8939

¹ Analog/digital CAN circuitry on ASIC must be deactivated by reset vector (Config:RESET_VECTOR:DCAN_OFF).

² For mode 2 (VB at 3,3V) the low level monitor of VBAT is disabled.

³ High level monitor only monitors levels above min.

F03_9301

Protection circuits limit the maximum current consumption due to slope of power supply as shown in the following figure:

F03_224

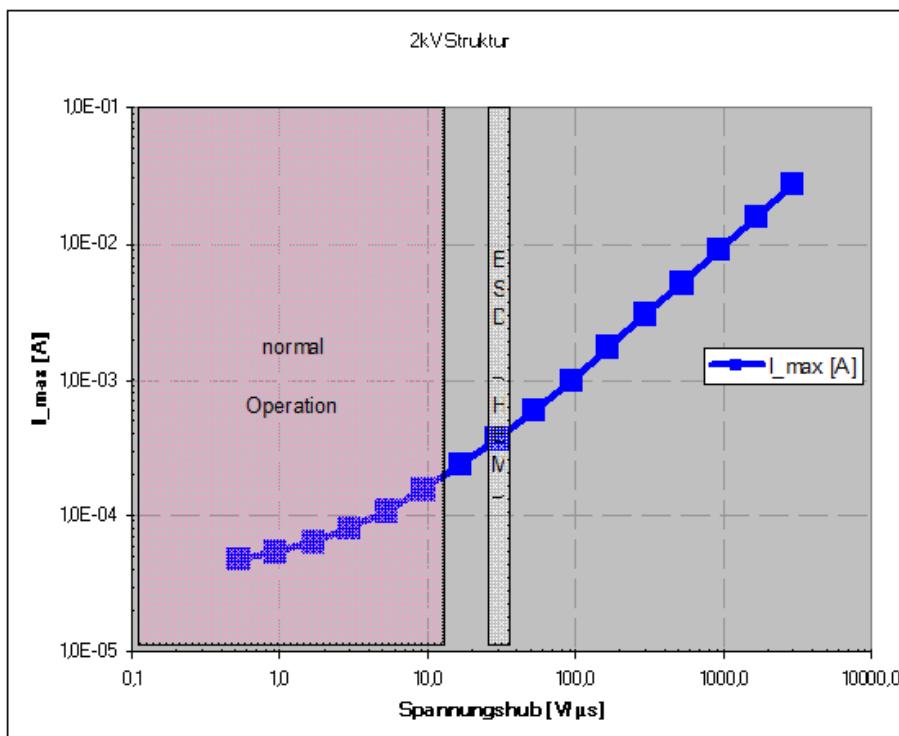


Figure 10: Max. current due to slope of power supply

F03_226

According to section 3 (Figure 9) it will be guaranteed by the sensor that if the supply voltage is out of the specified range the sensor will deliver the specified performance or it is signalized by an defined safety mechanism (e.g. flags). Any "Graubereich" with bad sensor performance due to wrong voltage supply without detection will be avoided.

F03_9400

Please notice:

The pins "PSI5_P" together with pin "VBAT" and pin "PSI5_M" can be applied in reverse polarity to the PSI5 interface. The current must be limited to 140 mA.

3.4.1.1 Electrical specification of synchronization pulse

F03_228 The PSI5 interface is triggered by the first (rising) slope of the sync pulse. The slope is to be maintained in the PSI5 bus with all sensors attached, considering parasitic capacitances of wires and blocking capacitors and EMC-capacitors of the sensor system. Picture of synchronization waveform:

F03_229

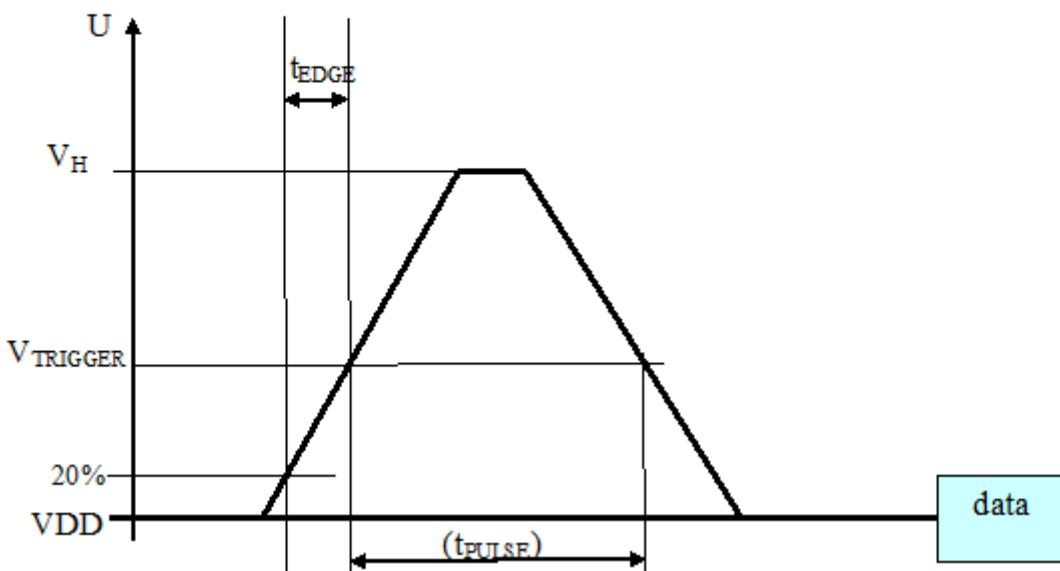


Figure 11: Synchronization waveform

F03_230

Table 13: Synchronization

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Sync. threshold voltage	V_TRIGGER	VB + 1,4		VB + 2,6	V
Slew rate of sync. pulse at t_EDGE	VSYNC_SLR	0,43	0,75	1,5	V/µs
Time above threshold to accept sync. pulse (1/256*Fmain, Fmain = 25,6MHz)	TSYNC_H	10			µs
Sync. pulse duration (t_PULSE (time between puls voltage is beyond and below V_TRIGGER))	TSYNC_DUR			20	µs
Maximum time from rising syncpuls to triggerededge (= t_edge)	T_edge	0		10	µs

3.4.2 Electrical specification for VDD3

F03_233

VDD3 can be used as voltage output (Mode 1,3,4,5,6) and input (Mode 2). In every case an external capacitor (minimum 150nF) must be applied to VDD3. The voltage is monitored for a range above and below the normal operating mode. When the voltage at VDD3 reaches a range specified by VDD3_ML or VDD3_MH, the TIG700 is still full functional and performs in the specified range, but the failure flags for over/undervoltage protection are set.

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F03_234

Table 14: Electrical specification for VDD3

Parameter / Condition	Symbol	Min	Max	Unit
Voltage range for output mode (full specification for sensor evaluation)	VDD3	3,13	3,47	V
Output current for output mode connecting second devices (mode 6)	IVDD3_out	0	6	mA
Voltage range for input mode (full specification for sensor evaluation)	VDD3_in	3,13	3,47	V
Voltage monitoring range, low level (full specification for sensor evaluation guaranteed)	VDD3_ML	see {REF:F07_9900}	see {REF:F07_9900}	V
Voltage monitoring range, high level (full specification for sensor evaluation guaranteed)	VDD3_MH	see {REF:F07_9899}	see {REF:F07_9899}	V
Slope of power supply at VDD3 / no additional current through clamping of esd protection circuit	DVSUP	0,2*1e-6	1	V/µs
Fast slope of power supply at VDD3 / with additional current through clamping of esd protection circuit typical 2mA	DVSUP_MAX		200	V/µs

F03_236

For Mode 6 the maximum additional current for another part (eg. SMA660) may not exceed 6 mA. That means, that the SPI interface should not used the maximum capacitive loads and should also reduce the transmission speed from maximum 10MHz down to max 4 MHz.

F03_13430

Formula for calculation can be found at F03_2189.

F03_237

Table 15: Electrical specification for VDD3

Parameter / Condition	Symbol	Min	Max	Unit
Voltage ripple at VDD3 without setting any failure flags and output-signal within specified limits (+/-1%/s; +/-20mG). For the frequency range 687kHz+/-10% and 812.5kHz +/-10% the acceleration limit is +/-30mg. Frequency range for ripple: DC to 1MHz			50	mVpp
Measurement method as defined in PH_SMI7xx_Measurement_And_Validation_work.doc#psrr <PH_SMI7xx_Measurement_And_Validation_work.doc>				
Slope of power supply at VDD3		0.2		V/s
Slope of power supply at VDD3			200	V/µs

F03_239

According to section 3 (**Figure 9: Over/undervoltage-detection**) it will be guaranteed by the sensor that if the supply voltage is out of the specified range the sensor will deliver the specified performance or it is signalized by an defined safety mechanism (e.g. flags). Any "Graubereich" with bad sensor performance due to wrong voltage supply without detection will be avoided.

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3.4.3 Electrical specification for VDD1_8

F03_241 VDD1_8 can not be used as voltage supply output. The pin is only used for connecting a blocking capacitance.

F03_242 **Table 16:** Electrical specification for VDD1_8

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Voltage range (full specification for sensor evaluation; voltage after end of boot sequence)	VDD1_8	1,65		2,0	V
Voltage monitoring range, low level due power on reset.	VDD_POR	1,65		1,8	V
Voltage monitoring range, high level (full specification for sensor evaluation, voltage after end of boot sequence)	VDD1_8_MH	1,9		2,0	V
EWS Voltage monitoring, high level	VDD1_8_MH	2,0		2,04	V
A capacitor at VDD1_8 for all applications must be connected directly between VDD1_8 and VSS (all application modes). The capacitance must be in the following range for all temperatures and guaranteed over lifetime:	C_VDD1_8	10		50	nF

3.4.4 Electrical specification for VDD_IO

F03_244 VDD_IO must be externally supplied. It powers the interface pins: RX,TX, CS_B, SCLK, MISO, MOSI, RESET_B and WDGI. If these interfaces are not used, VDD_IO must be set to VDD3.

If application mode 1, 2 or 4 is used, then the blocking capacitance at VDD_IO must be 1nF at least.

If the application mode 5 or 6 are used (self supplied VDD_IO), then the blocking capacitance at VDD_IO must be 15nF at least.

F03_245 **Table 17:** Electrical specification for VDD_IO

Parameter / Condition	Symbol	Min	Max	Unit
Voltage range (full specification for sensor evaluation)	VDD_IO	3,13	5,5	V
Mean current consumption during interface pins are active. (RX,TX and/or CS_B,SCLK,MISO and MOSI) (PLL frequency at max, load at TX and MISO max)	IVDD_IO		8	mA
Mean current consumption during interface pins are active. (RX,TX and/or CS_B,SCLK,MISO and MOSI; SCLK at 4MHz, 35pF load)	IVDDIO_4M		? (1)	mA
Peak current at VDD_IO (limited due to internal resistor) (load at 100pF, 10ns rise/fall time)	IVDD_IO_P		30	mA

F03_247 No explicit voltage monitoring of VDD_IO implemented. Deviation of nominal voltage within specified limits does not influence any parameter to exceed specified limits or is registered by other parts of the sensor (e.g. SPI protocol CRC). Missfunction is signaled before deviation of sensor parameters occur or communication is stopped.

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3.4.5 Electrical specification for PSI5_P

F03_8958 PSI5_P is the data pin for the PSI5 interface. It provides the current sink for data transmission. The control of rise and fall time of PSI communication current pulse is realized by a digital control of the current sinks which generate the current signal. 8 bits digital vector is used to control 8 separate current sinks. Current sinks 1, 2, 7 and 8, each contribute 2.6mA; Current Sinks 3, 4, 5 and 6 contribute each 3.9mA to the total sending current of 26mA. The current sinks with different amplitude are activated subsequently with a 9MHz - clock. After 8 cycles the current will achieve the nominal level of 26mA.

F03_251 The following Picture shows the slope generation.

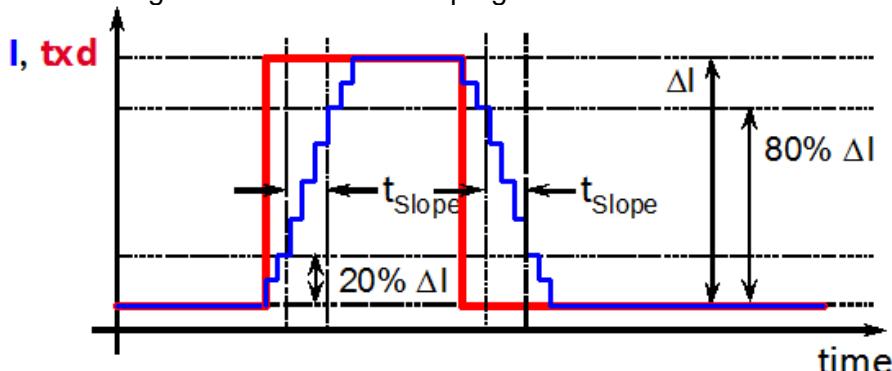


Figure 12: Slope generation

F03_252 Table 18: Electrical specification for PSI5_P

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Maximum current in case of reversed connection	PSI5_P_IR			140	mA
Maximum reverse Voltage (PSI Application relevant only)				20	V
Sink current delta I (delta_I = I_high - I_low)	I_SINK	22	26	30	mA
Sink current edge duration tslope (20% to 80% of delta_I)	I_slope_20_80	350	500	600	ns
Sink current edge duration tslope (80% to 20% of delta_I)	I_slope_80_20	350	500	600	ns

F03_9401 Please notice:

The pins "PSI5_P" together with pin "VB" and pin "PSI5_M" and all other pins connected to GND can be applied in reverse polarity to the PSI5 interface. The current must be limited to 140 mA.

3.4.6 Electrical specification for VSSA/D

F03_254 VSSA and VSSD are bonded to the same pin. The voltage level between VSSA and VSSD must not exceed at any circumstances 0,3 V in any direction.



3.4.7 Electrical specification for PSI5_M

F03_256 Table 19: Electrical specification for PSI5_M

Parameter / Condition	Symbol	Min	Max	Unit
Maximum voltage difference between PSI5_M and VSSA or VSSD (PSI5_P active)	PSI5_M_DV	-0,3	0,3	V
Maximum current flow through PSI5_M (PSI5_P active)	PSI5_M_I		-30	mA

F03_9402 Please notice:

The pins "PSI5_P" together with pin "VBAT" and pin "PSI5_M" can be applied in reverse polarity to the PSI5 interface. The current must be limited to 140 mA.

3.4.8 Electrical specification for CPUMP

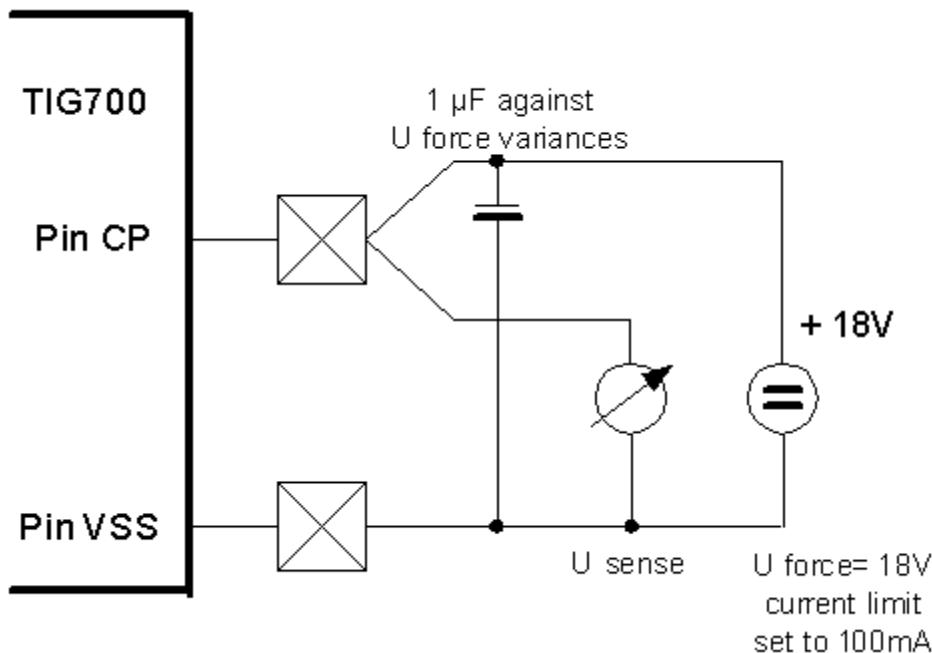
F03_258 CPUMP must be connected with a blocking capacitor to VSSA/D (see 3.8.1).

F03_259 Table 20: Electrical specification for CPUMP

Parameter / Condition	Symbol	Min	Max	Unit
Output voltage range with / without internal load (PLL frequency at maximum; minimum voltage with 100µA load)	VCP	18,5	27	V

F03_261 During programming the OTP the following circuit can be optionally connected to CP and VSS (VSSD and VSSA) to program faster:

F03_262



F03_8972 The user should ensure, that the programming voltage of 18V is stable in the range down to 16V.

The total range of Uforce must be between 16V and 20V. The internal programming regulator depends on this voltage range.



3.4.9 Electrical specification for XTAL_I and XTAL_O

F03_266 XTAL_I and XTAL_O are the external connections to an 20MHz crystal. Only one additional capacitor from XTAL_I to VSS and XTAL_O to VSS should be applied. The crystal oscillator is only necessary, if the CAN-interface option is used. Otherwise the pin XTAL_I should be connected to VSSA/D.

F03_267 Table 21: Electrical specification for XTAL_I and XTAL_O

Parameter / Condition	Symbol	Min	Max	Unit
Capacitor at XTAL_I ⁴	C_XTALI	0	50	pF
Capacitor at XTAL_O ⁵	C_XTALO	0	50	pF

3.4.10 Electrical specification for TX and RX

F03_8974 TX and RX are the logical data pins for the connection to an interface chip, which realize the physical CAN interface. RX receives the data, TX transmits the data to the physical interface. The RX pin has a pull up resistor of nominal 100 kOhm from input to VDD_IO. The TX pin can be put into high ohmic state, if the CAN functionality is not used.

During start-up the RX pin is compared to VDD_IO/2 for recognizing the ID of the SPI interface. This is only possible if VDD_IO is supplied.

F03_271 Table 22: Electrical specification for TX and RX

Parameter / Condition	Symbol	Min	Max	Unit
Input low voltage of RX pin (VDD_IO between min/max values)	V_IL_RX	0	0,3* VDD_IO	V
Input low current of RX pin including pull-up resistor and leakage current (VDD_IO at 5V)	I_IL_RX	41	63	µA
Input high voltage of RX pin (VDD_IO between min/max values)	V_IH_RX	0,7*VDD_IO	VDD_IO	V
Input high current of RX pin (VDD_IO between min/max values, input level at VDD_IO)	I_IH_RX	-10	10	µA
Input capacitance at RX pin (VDD_IO between min/max values)	C_I_RX	1	6	pF
Input voltage hysteresis (VDD_IO between min/max values)	V_HY_RX	0,1		V
Capacitive load at TX (1MBaud for CAN-Communication)	C_L_TX		35	pF
Output high voltage of TX pin (VDD_IO betw. min/max values, output current @ +/- 2mA)	V_OH_TX_2m	VDD_IO - 0,4	VDD_IO	V
Output low voltage of TX pin (VDD_IO betw. min/max values, output current @ +/- 2mA)	V_OL_TX_2m	0	0,4	V
Maximum rise time from maximum output low voltage to minimum output high voltage at TX (max. capacitive load)	T_R_TX		50	ns
Maximum fall time from minimum output high voltage to maximum output low voltage at TX (max. capacitive load)	T_F_TX		50	ns

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Output capacitance at TX without load (no external capacitive load, value without package, measured at wafer level)	C_O_TX		6	pF
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3.4.11 Electrical specification for CS_B

F03_273

The CS_B pin has a pull up resistor of nominal 100 kOhm from input to VDD_IO. If the SPI interface is configured as slave, then CS_B is an input. If the SPI interface is configured as master, the CS_B is an output and the internal pull-up resistor is switched off. During input mode the driver of CS_B is set to high impedance state.

F03_274

Table 23: Electrical specification of CS_B

Parameter / Condition	Symbol	Min	Max	Unit
Input low voltage of CS_B pin (VDD_IO between min/max values)	V_IL_CSB	0	0,3*VDD_IO	V
Input low current of CS_B pin including pull-up resistor and leakage current (VDD_IO at 5V, input level at VSSA/D)	I_IL_CSB	41	63	µA
Input high voltage of CS_B pin (VDD_IO between min/max values)	V_IH_CSB	0,7*VDD_IO	VDD_IO	V
Input high current of CS_B pin (VDD_IO between min/max values)	I_IH_CSB	-10	10	µA
Input voltage hysteresis at CSB_B (VDD_IO between min/max values)	V_HY_CSB	0,2		V
capacitance at CS_B (no external capacitive load, value without package, measured on wafer level)	C_L_CSB	1	6	pF
Maximum rise time from maximum output low voltage to minimum output high voltage at CSB, if SPI is in master mode (maximum capacitive load)	T_R_CSB		25	ns
Maximum fall time from minimum output high voltage to maximum output low voltage at CSB, if SPI is in master mode (maximum capacitive load)	T_F_CSB		25	ns
Capacitive load at CS_B, if SPI is in master mode (maximum external capacitive load)	C_L_CSB		35	pF
Output high voltage of CS_B pin, if SPI is in master mode (VDD_IO between min/max values, output current @ +/-2mA)	V_OH_CSB_2m	VDD_IO - 0,4	VDD_IO	V
Output low voltage of CS_B pin, if SPI is in master mode (VDD_IO between min/max values, output current @ +/-2mA)	V_OL_CSB_2m	0	0,4	V

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3.4.12 Electrical specification for SCLK

F03_276 The SCLK has a pull-up resistor of nominal 100 kOhm from input to VDD_IO. If the SPI interface is configured as slave, then SCLK is an input. If the SPI interface is configured as master, the SCLK is an output and the internal pull-up resistor is switched off. During input mode the driver of SCLK is set to high impedance state.

F03_277 Table 24: Electrical specification of SCLK

Parameter / Condition	Symbol	Min	Max	Unit
Input low voltage of SCLK pin (VDD_IO between min/max values)	V_IL_SCLK	0	0,3*VDD_IO	V
Input low current of SCLK pin including pull-up resistor and leakage current (VDD_IO at 5V)	I_IL_SCLK	41	63	µA
Input high voltage of SCLK pin (VDD_IO between min/max values)	V_IH_SCLK	0,7*VDD_IO	VDD_IO	V
Input high current of SCLK pin (VDD_IO between min/max values)	I_IH_SCLK	-10	10	µA
Input voltage hysteresis at SCLK (VDD_IO between min/max values)	V_HY_SCLK	0,2		V
Input capacitance at SCLK (no external capacitive load, value without package, measured on wafer level)	C_I_SCLK	1	6	pF
Maximum rise time from maximum output low voltage to minimum output high voltage at SCLK, if SPI is in master mode (maximum capacitive load)	T_R_SCLK		25	ns
Maximum fall time from minimum output high voltage to maximum output low voltage at SCLK, if SPI is in master mode (maximum capacitive load)	T_F_SCLK		25	ns
Capacitive load at SCLK, if SPI is in master mode (maximum external capacitive load)	C_L_SCLK		35	pF
Output high voltage of SCLK pin, if SPI is in master mode (VDD_IO between min/max values, output current @ +/-2mA)	V_OH_SCLK_2m	VDD_IO - 0,4	VDD_IO	V
Output low voltage of SCLK pin, if SPI is in master mode (VDD_IO between min/max values, output current @ +/-2mA)	V_OL_SCLK_2m	0	0,4	V

3.4.13 Electrical specification for MISO

F03_279 Regardless, whether the SPI is in master or slave mode, MISO functions only as output. For master mode the MISO pin takes over the meaning of MOSI. This is only done by cross wiring the MISO and MOSI pins outside of TIG700. When CS_B during slave mode is inactive high, then MISO goes into the high impedance state.

F03_280 Table 25: Electrical specification of MISO

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Parameter / Condition	Symbol	Min	Max	Unit
Output high voltage of MISO pin (VDD_IO betw. min/max values, output current @ +/-4mA)	V_OH_MISO	0,8*VDD_IO	VDD_IO	V
Output low voltage of MISO pin (VDD_IO betw. min/max values, output current @ +/-4mA)	V_OL_MISO	0	0,16 * VDD_IO	V
Maximum rise time from maximum output low voltage to minimum output high voltage at MISO (maximum capacitive load)	T_R_MISO		15	ns
Maximum fall time from minimum output high voltage to maximum output low voltage at MISO (maximum capacitive load)	T_F_MISO		15	ns
Capacitive load at MISO (10MHz SPI, strong driver mode)	C_L_MISO		100	pF
Capacitive load at MISO if TIG700 is used in self-supplied mode. (VDD_IO connected to VDD3) (4MHz SPI, weak driver mode)	C_L_MISO_S		35	pF
Output capacitance at MISO during tristate and active operation (no external capacitive load, value without package, measured on wafer level)	C_MISO	1	6	pF
Output current during high impedance state at MISO pin (VDD_IO between min/max values)	I_OUTZ_MISO	-10	10	µA

3.4.14 Electrical specification for MOSI

F03_282

Regardless, whether the SPI is in master or slave mode, MOSI functions only as input. For master mode the MOSI pin takes over the meaning of MISO. This is only done by cross wiring the MOSI and MISO pins outside of TIG700. MOSI has a pull-up resistor of nominal 100 kOhm from input to VDD_IO.

F03_283

Table 26: Electrical specification of MOSI

Parameter / Condition	Symbol	Min	Max	Unit
Input low voltage of MOSI pin (VDD_IO between min/max values)	V_IL_MOSI	0	0,3*VDD_IO	V
Input low current of MOSI pin including pull-up resistor and leakage current (VDD_IO at 5V)	I_IL_MOSI	41	63	µA
Input high voltage of MOSI pin (VDD_IO between min/max values)	V_IH_MOSI	0,7*VDD_IO	VDD_IO	V
Input high current of MOSI pin (VDD_IO between min/max values)	I_IH_MOSI	-10	10	µA
Input voltage hysteresis at MOSI (VDD_IO between min/max values)	V_HY_MOSI	0,2		V
Input capacitance at MOSI pin (no external capacitive load, value without package, measured on wafer level)	C_I_MOSI	1	6	pF

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3.4.15 Electrical specification for RESET

F03_285 The RESET has a pull down resistor of nominal 200 kOhm from input to VSSD. The pin is low active.

F03_286 **Table 27:** Electrical specification of RESET

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Input low voltage of RESET pin (VDD_IO between min/max values)	V_IL_RESET	0		0,3*VDD_IO	V
Input low current of RESET pin (VDD_IO between min/max values)	I_IL_RESET	-10		10	µA
Input high voltage of RESET pin (VDD_IO between min/max values)	V_IH_RESET	0,7* VDD_IO		VDD_IO	V
Input high current of RESET pin including pull-down resistor and leakage current (VDD_IO at 5V)	I_IH_RESET	21		31	µA
Input voltage hysteresis at RESET (VDD_IO between min/max values)	V_HY_RESET	0,1			V
Input capacitance at RESET pin (no external capacitive load, value without package, measured on wafer level)	C_I_RESET	1		6	pF
Reset delay time (input above V_IH_RESET)	T_D_RESET	80	95	110	µs

F03_1671 Any low voltage pulse at RESET, which lasts less than T_D_RESET, will not be detected (Glitch filter function).

3.4.16 Electrical specification for WDGI

F03_290 **Table 28:** Electrical specification for WDGI

Parameter / Condition	Symbol	Min	Max	Unit
Maximum rise time from maximum output low voltage to minimum output high voltage at WDGI (maximum capacitive load)	T_R_WDGI		50	ns
Maximum fall time from minimum output high voltage to maximum output low voltage at WDGI (maximum capacitive load)	T_F_WDGI		50	ns
Capacitive load at WDGI (maximum external capacitive load)	C_L_WDGI		35	pF
Output high voltage of WDGI pin (VDD_IO betw. min/max values, output current @ +/-2mA)	V_OH_WDGI_2m	VDD_IO - 0,4	VDD_IO	V
Output low voltage of WDGI pin (VDD_IO betw. min/max values, output current @ +/-2mA)	V_OL_WDGI_2m	0	0,4	V
Output current during tristate (VDD_IO between min/max values)	I_IL_WDGI	-10	10	µA
Output capacitance during tristate and active	C_WDGI	1	6	pF

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operation
(no external capacitive load, value without
package, measured on wafer level)

3.4.17 Electrical specification for acceleration sensor pins

F03_291

All pins named MA, MB, MC and MD are the sensitive charge connections to the acceleration micro mechanical sensor. They should show low leakage, low capacitive behavior and any simulation with the acceleration front end should contain the actual layout extracted view.

F03_292

Table 29: Electrical specification for acceleration sensor pins

Parameter / Condition	Symbol	Min	Max	Unit
Input leakage current at MA, MB, MC and MD (maximum VDD3)	IL_MABCD	-1	1	nA
Input capacitance at MA, MB, MC and MD (maximum VDD3)	CIN_MABCD		0,5	pF
Maximum voltage at all acceleration sensor pins (maximum VDD3)	V_ACC		2,15	V

3.4.18 Electrical specification for yaw-rate sensor pins

F03_294

All pins named CN, CP, DL and DR are the sensitive charge connections to the yaw rate micro mechanical sensor. They should show low leakage, low capacitive behavior and any simulation with the yaw rate front end should contain the actual layout extracted view.

F03_295

Table 30: Electrical specification for yaw-rate sensor pins

Parameter / Condition	Symbol	Min	Max	Unit
Input leakage current at CN,CP,DL and DR (maximum VDD3)	IL_MABCD	-1	1	nA
Input capacitance at CN,CP,DL and DR (maximum VDD3)	CIN_MABCD		1	pF
Maximum voltage at CN,CP,DL and DR (maximum VDD3)	V_CNPDLR		2,9	V
Maximum voltage at AL,AR,TN,TP,QP and QN (maximum VDD3)	V_ATQ		18	V
Maximum voltage at SUBH (maximum VDD3)	V_CNPDLR		2,9	V

3.4.19 Microcut specification

F03_298

Microcut means, that the connection from the external power supply is cut off. It does not mean, that there is a short from power supply to ground. Microcut definition is only valid for VB supply (Normally PSI5 mode operation) - normal reset behavior for all other modes.

In Mode2 (3.3V supply) a blocking Capacitor is supporting the Supply Voltage. With a 150nF Capacitor an allowed voltage drop of $3.3V - 3.15V = .15V$ with a current consumption of 29mA max. a microcut of $t=CU/I = 0.75\mu s$ can be tolerated.

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**Stopping of Communication due to Microcut**

By default SMI7 module is configured such that if a low voltage is detected at VB the PSI communication is inhibited, i.e. no current pulses are sent. The configuration of the microcut behaviour is not configurable by the customer on device level.

F03_299

Table 31: Microcut specification

Parameter / Condition	Symbol	Min	Max	Unit
Maximum microcut time at VB with attached external capacitor ($\geq 150\text{nF}$) at VDD3 (VB disconnected from external powersupply without setting any failure flag. VDD3 at external capacitor $\geq 150\text{nF}$)	T_MICRO		0,5	μs
Voltage range at VB before microcut rejection time	V_MICRO	4,5	16,5	V
Minimum time between 2 microcuts without setting any failure flags (VDD3 at external capacitor $\geq 150\text{nF}$)	T_MICRO_D	10		μs



3.5 Startup behavior

3.5.1 Overview startup sequence

F03_308

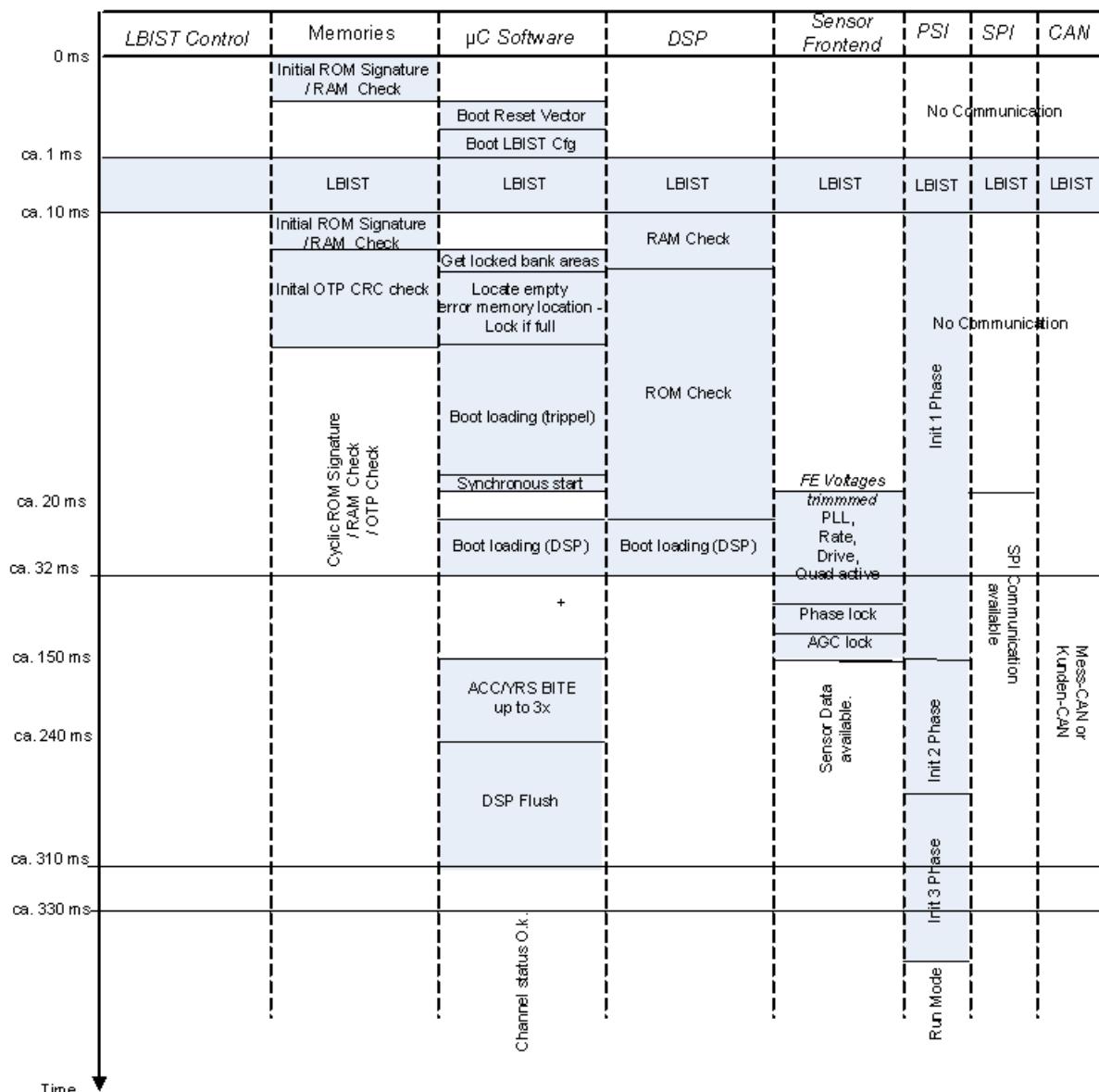


Figure 14: Startup Sequence with 15Hz filter (all timesteps are rough estimations, not guaranteed)

F03_9134

Overall timing depends strongly on number of BITE-cycles and flush-time. Estimated flush times are given here and depending on error control config:



F03_312 Table 32: Flushtime for different filter settings

BITE Flush Times:

Flush times after bite* **wc aus YRS/ACC1/ACC2**LF1 ms 90,0
LF1 ms 90,0LF2 ms 25,0
LF2 ms 25,0LF3 ms 155,0
LF3 ms 155,0LF4 ms 60,0
LF4 ms 60,0HF ms 10,0
HF ms 10,0

*) Variation: f_system: +/-10%; f_cmb;DL_cmb min/max 4s

Bitehöhe ACCxyz 20g;

Rest-Fehler LF=20mg

Rest-Fehler HF 500mg

Bitehöhe YRS 300°/s

Rest-Fehler LF=3°/s

Rest-Fehler HF 3°/s

3ms have to be added to all BITE flush times since the flags dsp_acc1/2_if_out are yet masked.

Hold Times for Failure Counters:

Flush times after shock*		YRS	CMAx/y	CMAz
LF1	ms	80,0	90,0	90,0
LF1	ms	80,0	90,0	90,0
LF2	ms	20,0	25,0	25,0
LF2	ms	20,0	25,0	25,0
LF3	ms	140,0	155,0	155,0
LF3	ms	140,0	155,0	155,0
LF4	ms	50,0	60,0	60,0
LF4	ms	50,0	60,0	60,0
HF	ms	2,00	6,0	10,0
HF	ms	2,00	6,0	10,0

*) Variation: f_system: +/-10%; f_cmb;DL_cmb min/max 4s

Bitehöhe ACCxy 80g;ACCz 40g

Rest-Fehler LF=20mg

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Rest-Fehler HF 500mg
 Bithöhe YRS 1000°/s
 Rest-Fehler LF=3°/s
 Rest-Fehler HF 3°/s

3.5.1.1 SPI activation after startup

F03_16314 SPI communication possible on reset after following delay (dependent on number of configuration tuples and free-running DCO frequency):

typical	max.
22 ms	28 ms

F03_1863 Estimated duration after that a sensor signal can be provided (assuming PON-BITE 3 times and the following filter/protocol settings) after power on:

F03_314 **Table 33:** Specification for availability of a sensor signal in ms (max) after power-on

	SPI	CAN	PSI
LF1	297	297	N/A
LF2	232	232	N/A
LF3	362	362	N/A
LF4	267	267	N/A
	217	217	N/A

F03_1944 (Uncertain HF channel corner frequency-possible reduction to 200Hz for acceleration channel could increase duration)

3.5.2 Power Consumption during Startup

F03_16130 Current consumption during Startup is specified for Application Modes using VB as Supply (Mode 1,3,4,5) with max. C as recommended in F03_16182.

Voltage ramp has to be monotonous, high current consumption starts when VB>4.3V, this means the timings specified in this chapter refer to the time difference to VB>4.3V

Max. current consumption during start-up:

Time	Maximum Current	Comment
0ms ... 1ms	70mA	Minimum current consumption 35mA
1ms ... 21ms	35mA	excl. additional supplied part
>21ms	29mA (SPI/PSI) / 31mA (CAN)	excl. additional supplied part

3.6 Power supply concept

3.6.1 Schematic of power-supply concept

F03_320

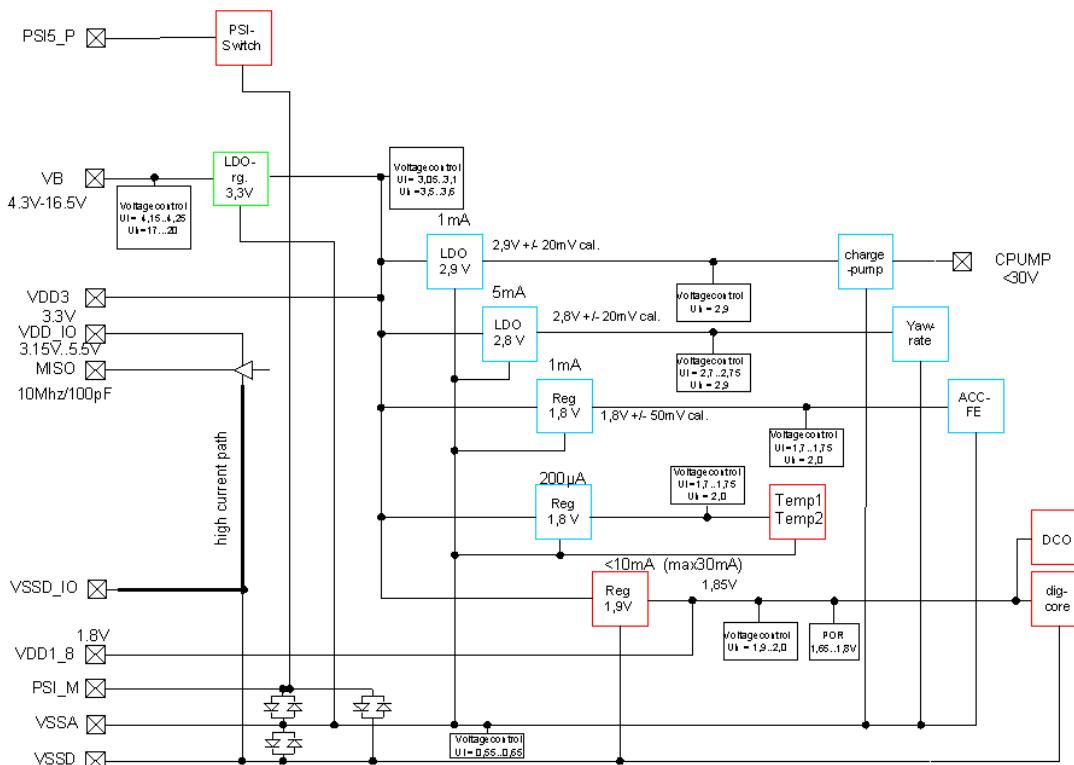


Figure 15: schematic representation of supply structure

3.6.2 Overview of power consumption depending on application

F03_323

The given scenarios show extreme supply conditions for evaluating the maximum supply current and possible package requirements for cooling.

F03_16291

Scenario 1: PSI5 active, VDD_IO self biased, reduced SPI driver:

Modul	main current [mA]	voltage drop in worst case [Volt]	Aktiv high (duty cycle)	Aktiv low (duty cycle)	total current [mA]	total power consumption [W]
TIG700 intern	30	11.5	1	0	30	0.35
VDD IO	0.07	5.5	1	0	0.07	0.000
PSI5	30	11.5	0.396	0.604	11.88	0.14
VDD3 extern	0	8.4	1	0	0	0
				Sum	0.48	W
				RTH package	45	K/W
				Tambient	135	C
				Tjunction	156.69	C



F03_16292 Scenario 2: PSI5 active, VDD_IO self biased, reduced SPI driver, external IC supply support

Modul	main current [mA]	voltage drop in worst case [Volt]	Aktiv high (duty cycle)	Aktiv low (duty cycle)	total current [mA]	total power consumption [W]
TIG700 intern + IO	30.07	11.5	1	0	30.07	0.35
VDD IO	0.07	3.3	1	0	0.07	0.000231
PSI5	30	11.5	0.396	0.604	11.88	0.14
VDD3 extern	6	8.4	1	0	6	0.05
					Summe	0.53 W
					RTH package	45 K/W
					Tambient	135 C
					Tjunction	158.99 C

F03_16293 Scenario 3: PSI5 inactive, VDD_IO external supplied:

Modul	main current [mA]	voltage drop in worst case [Volt]	Aktiv high (duty cycle)	Aktiv low (duty cycle)	total current [mA]	total power consumption [W]
TIG700 intern	30	11.5	1	0	30	0.35
VDD IO	0.17	3.3	1	0	0.17	0.00
PSI5	0	11.5	0.396	0.604	0	0
VDD3 extern	0	8.4	1	0	0	0
					Summe	0.35 W
					RTH package	45 K/W
					Tambient	135 C
					Tjunction	150.55 C

3.6.3 Application hint for VDD_IO

F03_2189 To calculated the expected current due load mainly at MISO pin use following formula:

$$I@VDD_IO = Fsclk * VDD_IO * (Cload * 500 + 4,8e-9) \text{ [mA].}$$

Use Fsclk = clock frequency[Hz] of SCLK, Cload = capacitive load [F] at pin MISO ; add 6e-12F; VDD_IO = voltage at VDD_IO [V].

Example: VDD_IO = 3V, Cload = 100pF, SCLK = 4MHz; I@VDD_IO = 0.69mA.

3.7 Default wiring and configuration

F03_340 Default configuration (identical with Configuration until BootLoading / Software is finished):

Supply: - Pre-Regulator active

- Over/Undervoltagedetection VB active
- Flag V_Preg_low will be used in failure handling
- Flag V_Preg_11_high will be used in failure handling (flag at ~17V)
- Flag VDD3_high will be used in failure handling
- Flag VDD3_low will be used in failure handling

SPI: - Slave configuration

PSI: - sensitive to BiDir, but no active transmission

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F03_342 CAN: - XTAL is expected, no WDGI transmission
For some applications, the sensor may need to be reconfigured (see next chapter).

3.8 Wiring and configuration for different applications

F03_345 All pictures show only the wiring of the power supply pins, whereas the tables describe the wiring, purpose and configuration of all pins.

All given values for external capacitors and resistors are absolute min/max values including all tolerances.

The pins VSSA and VSSD are connected together via 2 separate bonds to one common package pin, internally. Details for the connection of a crystal see section 9.



3.8.1 Pinning: function, connections and configurations for different applications

3.8.1.1 Supply Pins

F03_16182

	Supply: 3.3V @ VDD3	Supply: 4.5V-16.5V @ VB	Supply: 4.5V-16.5V @ VB and 2nd IC supplied by VDD3
VB	Function: None	Function: Power Supply of SMI7 For PSI5 application: In for sync-pulse detection	Function: Power Supply of SMI7 For PSI5 application: In for sync-pulse detection
	Pin connected to: GND	Pin connected to: 4.5V-16.5V For PSI applications: PI-Filter (characterization done with 2.2nF/18Ohm/15nF). For SPI&CAN applications, a decoupling capacitor to VSS is recommended. A typical value for that capacitor is 100nF.	Pin connected to: 4.5V-16.5V For PSI applications: PI-Filter (characterization done with 2.2nF/10Ohm/ 33nF) For SPI&CAN applications, a decoupling capacitor to VSS is recommended. A typical value for that capacitor is 100nF.
	Configuration deviant from Default: - Pre-Regulator needs to be deactivated via Reset Vector (otherwise leakage current of some μ A) - Flag V_Preg_low needs to be masked	Configuration deviant from Default: -none	Configuration deviant from Default: -none
VDD3	Function: Power Supply of SMI7 Pin connected to: 3.3V. No external capacitor is required but may be connected as long as the input requirements of VDD3 are fulfilled. If the external regulator causes ripples in the frequency range from 600kHz to 1MHz a RC lowpass filter direct connected to VDD3 is necessary. A typical value for the RC lowpass filter is 2Ohm and 940nF. The application has to guarantee the given voltage limits in that case.	Function: Stabilization of internal 3.3V Pin connected to: via ext. blocking capacitance (160nF..730nF, nom 300nF) to GND. If more than 1 C is used, the minimum capacitance per capacitor must be > 160nF incl all tolerances.	Function: Stabilization of internal 3.3V and 3.3V-supply of 2nd IC (6mA max) Pin connected to: via ext. blocking capacitance (160nF..730nF, nom 300nF) to GND, and to supply pin of 2nd IC. If more than 1 C is used, the minimum capacitance per capacitor must be > 160nF incl all tolerances.
VDD1_8	Function: Output stabilization of internal 1.8V Pin connected to: Must be connected to a blocking capacitance of 10...50nF (nom. 15nF) Configuration deviant from Default: None	<- same	<- same
VSSA/D = GND	Function: Power in GND (Analog and digital ground, connected on BGA level) Pin connected to: GND Configuration deviant from Default: None	<- same	<- same



	<p>Function: Power Supply for CAN and SPI. VDD_IO defines the voltage levels for SPI, CAN, WDGI and RESET.</p> <p>Pin connected to: to be supplied with 3.3V or 5V. For PSI application, VDD_IO must be connected to VDD3 without additional blocking cap. For all other applications, this pin must be supplied externally with blocking cap 1nF...1uF (nom. 100nF, characterization with 2x100nF)</p> <p>Configuration deviant from Default: None</p>
--	---

<- same

<- same

3.8.1.2 SPI Pins

F03_16181

Name	no SPI mode	SPI slave mode	SPI master mode
CS_B	<p>Function: None. Pull-Up with at least 100kOhm</p> <p>Pin connected to: In order to prevent leakage currents, this pin should be connected to VDD_IO (directly or via 5.6kOhm* +-10%) if no SPI is used at all.</p> <p>Configuration deviant from Default: None.</p>	<p>Function: Input, Chip select for SPI. Pull-Up with at least 100kOhm</p> <p>Pin connected to: CS_B-pin of SPI-Master-IC</p>	<p>Function: Output (high Z), Chip select for SPI. Pull-up is disconnected. Default voltage level = VDD_IO</p> <p>Pin connected to: CS_B-pin of SPI-Slave-IC</p>
		<p>Configuration deviant from Default: None</p>	<p>Configuration deviant from Default: Configure CS_B as output for SPI-Master</p>
SCLK	<p>Function: None. Pull-Up with at least 100kOhm</p> <p>Pin connected to: In order to prevent leakage currents, this pin should be connected to VDD_IO (directly or via 5.6kOhm* +-10%) if no SPI is used at all</p> <p>Configuration deviant from Default: None.</p>	<p>Function: Input, SPI Clock Pull-Up with at least 100kOhm</p> <p>Pin connected to: SLCK-pin of SPI-Master-IC</p>	<p>Function: Output (high Z), SPI Clock. Pull-up is disconnected. Default voltage level = VDD_IO</p> <p>Pin connected to: SCLK-pin of SPI-Slave-IC</p>
		<p>Configuration deviant from Default: None</p>	<p>Configuration deviant from Default: Configure SLCK as output for SPI-Master</p>
MISO	<p>Function: None (high Z)</p> <p>Pin connected to: VSSD (external to VSS) directly or via 5.6kOhm* +-10%</p> <p>Configuration deviant from Default: No configuration necessary, this pin is always output. Default is Tristate.</p>	<p>Function: SPI data output as Slave (MISO), (high Z)</p> <p>Pin connected to: MISO-Pin of SPI-Master-IC</p>	<p>Function: SPI data output as Master (MOSI) (high Z)</p> <p>Pin connected to: MOSI-pin of SPI-Slave-IC</p>
		<p>Configuration deviant from Default: No configuration necessary, this pin is always output. Default is Tristate.</p>	<p>Configuration deviant from Default: No configuration necessary, this pin is always output. Default is Tristate.</p>
MOSI	<p>Function: None (pull-up)</p> <p>Pin connected to: VDD_IO (directly or via 5.6kOhm* +-10%)</p> <p>Configuration deviant from Default: No configuration necessary, this pin is always input.</p>	<p>Function: SPI data input as Slave (MOSI), (pull-up)</p> <p>Pin connected to: MOSI-Pin of SPI-Master-IC</p>	<p>Function: SPI data input as Master (MISO) (pull-up)</p> <p>Pin connected to: MISO-pin of SPI-Slave-IC</p>
		<p>Configuration deviant from Default: No configuration necessary, this pin is always input</p>	<p>Configuration deviant from Default: No configuration necessary, this pin is always input</p>

*for programming purposes on MM7 device level.
not being characterized on SMI7 level



3.8.1.3 PSI Pins

F03_16183

Name	PSI5 inactive	PSI5 active
PSI5_P	Function: None Pin connected to: VSS Configuration deviant from Default: None (Sensor does not start PSI5 by itself, but is sensitive to BiDir commands)	Function: Current sink output for PSI5 communication Pin connected to: external PSI + Configuration deviant from Default: None (Sensor does not start PSI5 by itself, but is sensitive to BiDir commands)
PSI5_M	Function: None Pin connected to: GND (low resistance-connection to VSS) Configuration deviant from Default: None	Function: Supply In (GND) for PSI5 Pin connected to: GND (low resistance-connection to VSS) Configuration deviant from Default: None

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3.8.1.4 CAN Pins

F03_16184

Name	CAN inactive	CAN active
XTAL_I	<p>Function: None</p> <p>Pin connected to: GND</p> <p>Configuration deviant from Default: no configuration needed. Default is that Quartz is expected. If no quartz is present => no clock => no CAN communication, but no side effects</p>	<p>Function: Input, connection for external crystal</p> <p>Pin connected to: 20MHz Quartz</p> <p>Configuration deviant from Default: no configuration needed. Default is that Quartz is expected. If no quartz is present => no clock => no CAN communication, but no side effects</p>
XTAL_O	<p>Function: None</p> <p>Pin connected to: GND</p> <p>Configuration deviant from Default: should be switched off if no XTAL is used, otherwise max. output of 100µA.</p>	<p>Function: Output, connection for external crystal</p> <p>Pin connected to: 20MHz Quartz</p> <p>Configuration deviant from Default: no configuration needed. Default is that Quartz is expected. If no quartz is present => no clock => no CAN communication, but no side effects.</p>
TX	<p>Function: None</p> <p>Pin connected to: VDDIO</p> <p>Configuration deviant from Default: No configuration needed (VDDIO will be driven)</p>	<p>Function: Output, Transfer CAN data. Voltage level depends on VDDIO</p> <p>Pin connected to: CAN transceiver (e.g. CA510)</p> <p>Configuration deviant from Default: None (TX is active per Default)</p>
RX	<p>Function for CAN: None (In, pull-up with at least 100kOhm)</p> <p>Pin connected to: VDDIO or GND</p> <p>Configuration deviant from Default: for CAN: No configuration necessary.</p>	<p>Function: Receive CAN-data (In, pull-up with at least 100kOhm)</p> <p>Pin connected to: CAN transceiver (e.g. CA510)</p> <p>Configuration deviant from Default: No configuration necessary</p>
WDGI	<p>Function: None, HighZ</p> <p>Pin connected to: GND</p> <p>Configuration deviant from Default: None (Default: no pulse is sent)</p>	<p>Function: Output of WDGI</p> <p>Pin connected to: WDGI-Input of CAN Receiver</p> <p>Configuration deviant from Default: Activation of WDGI via Bootloading necessary, this is early enough for CA510 which expects pulses from ~150ms on. WDGI usage is only foreseen in combination with CA510.</p> <p>Remark: during the first startup of the sensor, when WDGI is activated yet, CA510 does not trigger the reset which would usually be triggered when the WDGI pulse is missing. Hence, the activation of the WDGI needs to be programmed during the first startup</p>

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**additional for RX:**

SPI Slave application.:

Function for SPI: Autodetect SPI-ID**Pin connected to:** for SPI: VDDIO or GND (depending on desired SPI-ID), Information sampled @ End Of Bootloading process**Configuration deviant from Default:** for SPI: None.**3.8.1.5 CPUMP, RESET_B**

F03_16185

Name	All Configurations
CPUMP	<p>Function: Output, used for internal charge pump</p> <p>Pin connected to: must be connected to a capacitance of 39...167nF (nominal 100nF, characterized with 68nF) and 40V range; External voltage may be applied in order to speed up programming</p>
	<p>Configuration deviant from Default: None (External voltage applied to speed up programming will be used automatically)</p>
RESET_B	<p>Function: Reset Input, low-active, pull-down with at least 200kOhm</p> <p>Pin connected to: must be connected to VDD_IO-level, otherwise Reset</p>
	<p>Configuration deviant from Default: None</p>

The pin RESET must be connected to VDD_IO, if it is not controlled externally. Due its pulldown resistor a floating RESET pin will be pulled to active low and TIG700 will enter the reset state. (No communication, no sensor measuring, all values internally set to initial state.)

3.8.2 SPI and CAN only modes (Mode 1)

F03_2190

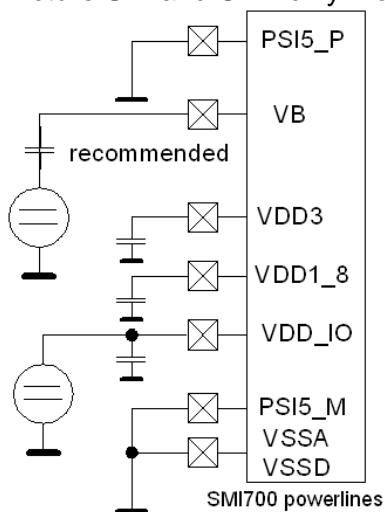
- Only SPI and/or CAN interface can be used
- In case, that only the SPI and/or CAN interface is used, the connections to PSI5_P and PSI5_M must be connected to the same ground level as the VSSA and VSSD pads.
- VDD_IO must be externally supplied with 3,3V or 5V nominally.
- VB must be supplied with 4.5V -16.5V. VDD_IO, VDD3 and VDD1_8 have to be connected to external blocking capacitors.
- See electrical specification (tables in 3.8.1) for the exact value of these capacitors.

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F03_352 Picture SPI and CAN only modes (Mode 1)



F03_11528 Mode1: CAN + SPI Master, 4.5...16.5V@VB

F03_11695 Mode1A: SPI Slave Only, 4.5...16.5V@VB

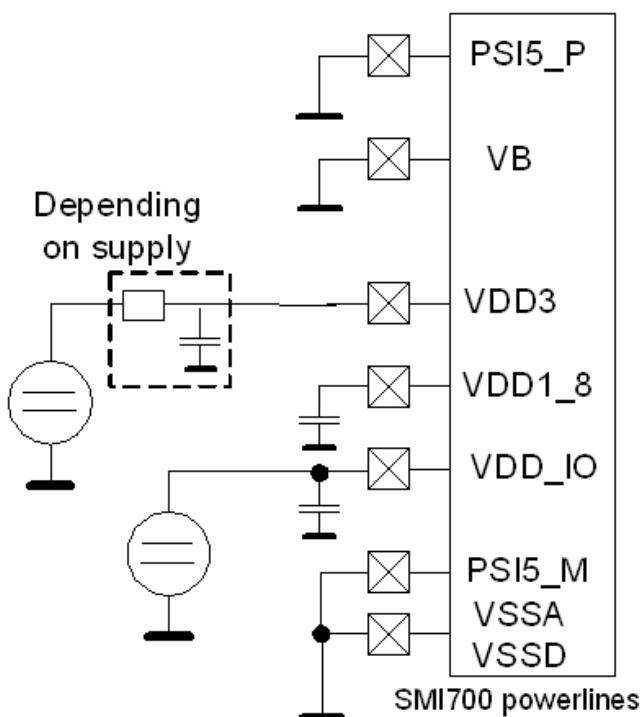
F03_11862 Mode1B: CAN Only, 4.5...16.5V@VB

3.8.3 SPI and CAN only modes (Mode 2A, 2B, 2C)

F03_2191

- Only the SPI and / or CAN interface are being used.
- The connections to PSI5_P and PSI5_M must be connected to the same ground level as the VSSA and VSSD pads.
- VB has to be connected to ground (VSS), VDD3 has to be connected to a 3.3V supply
- VDD_IO must be externally supplied with 3.3V or 5V nominally.
- VDD_IO and VDD1_8 have to be connected to external blocking capacitors.
- VDD3: No external capacitor is required but may be connected as long as the input requirements of VDD3 are fulfilled. If the external regulator causes ripples in the frequency range from 600kHz to 1MHz a RC lowpass filter direct connected to VDD3 is necessary.
- See electrical specification (tables in 3.8.1) for the exact value of these capacitors.

F03_360 Picture SPI and CAN only modes (Mode 2A, 2B, 2C)



[F03_12029](#) Mode2A: CAN + SPI Master, 3.3V@VDD3

[F03_12196](#) Mode2B: SPI Slave Only, 3.3V@VDD3

[F03_12363](#) Mode2C: CAN Only, 3.3V@VDD3

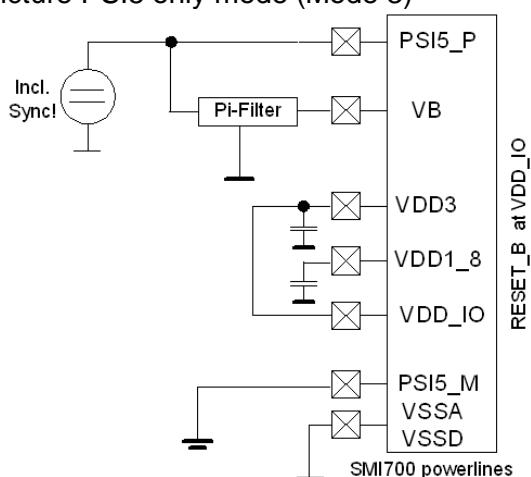
3.8.4 PSI5 only mode (Mode 3)

[F03_2192](#)

- If only PSI5 is available for power supply, then VDD_IO has to be connected to VDD3. The I/O pins TX, CS_B, SLCK and MOSI should be connected to VDD_IO (in order to prevent leakage currents), whereas MISO should be connected to ground and RX should be connected to VDD_IO or ground.
- All interface outputs are switched to high ohmic state.
- VDD3 and VDD1_8 have to be connected to external blocking capacitors.
- See electrical specification (tables in 3.8.1) for the exact value of these capacitors.

[F03_367](#)

Picture PSI5 only mode (Mode 3)





F03_13421 Ohmic resistance between GND and PSI5_M has to be smaller than 0.1 Ohm.

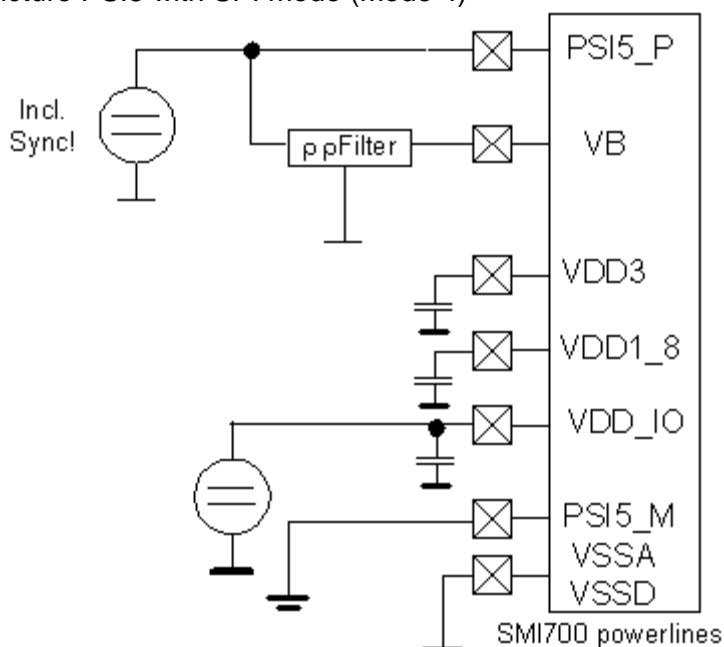
3.8.5 PSI5 with SPI mode (Mode 4)

F03_2193

- PSI5 is used for main power supply and VDD_IO is supplied with 3.3 or 5V nominally.
- The I/O pins (CS_B, SCLK, MISO, MOSI) can be used for SPI.
- VDD3 and VDD1_8 have to be connected to external blocking capacitors.
- See electrical specification (tables in 3.8.1) for the exact value of these capacitors.

F03_374

Picture PSI5 with SPI mode (Mode 4)



F03_2194 Note: If the PSI5 functionality is used, you must not power the TIG700 via VDD3, because only VB has the functionality for recognizing the synchron-puls from the PSI5 interface definition.

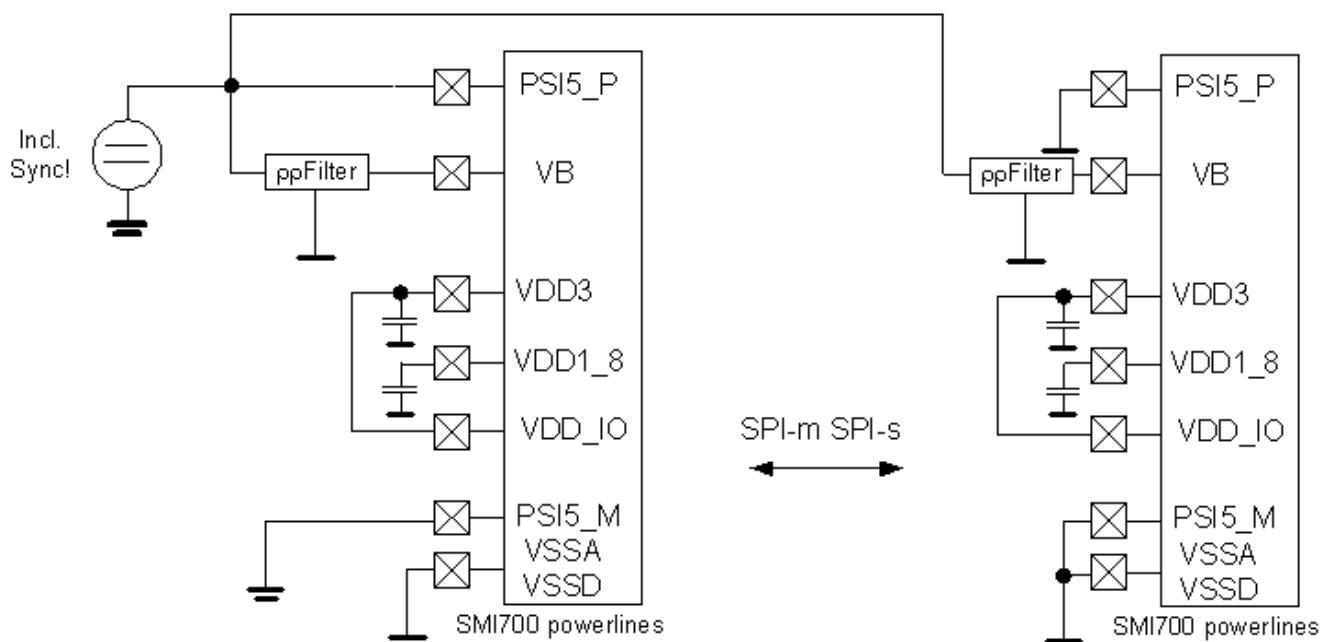
3.8.6 PSI5 with self supplied VDD_IO for SPI (Mode 5)

F03_2195

- PSI5 is used for main power supply and VDD_IO is self supplied from the VDD3 connection.
- The I/O pins (CS_B, SCLK, MISO, MOSI) can be used for SPI.
- VDD3 and VDD1_8 have to be connected to external blocking capacitors.
- See electrical specification (tables in 3.8.1) for the exact value of these capacitors.
- In this mode it is possible to connect 2 SMI7 via either SPI-Master or SPI-Slave interface together.
- The second device (right device on below picture) has no connection to the PSI interface, but transfers all data via SPI interface to the device with the PSI5 connection.

F03_384

Picture PSI5 with self supplied VDD_IO for SPI and CAN (Mode 5)



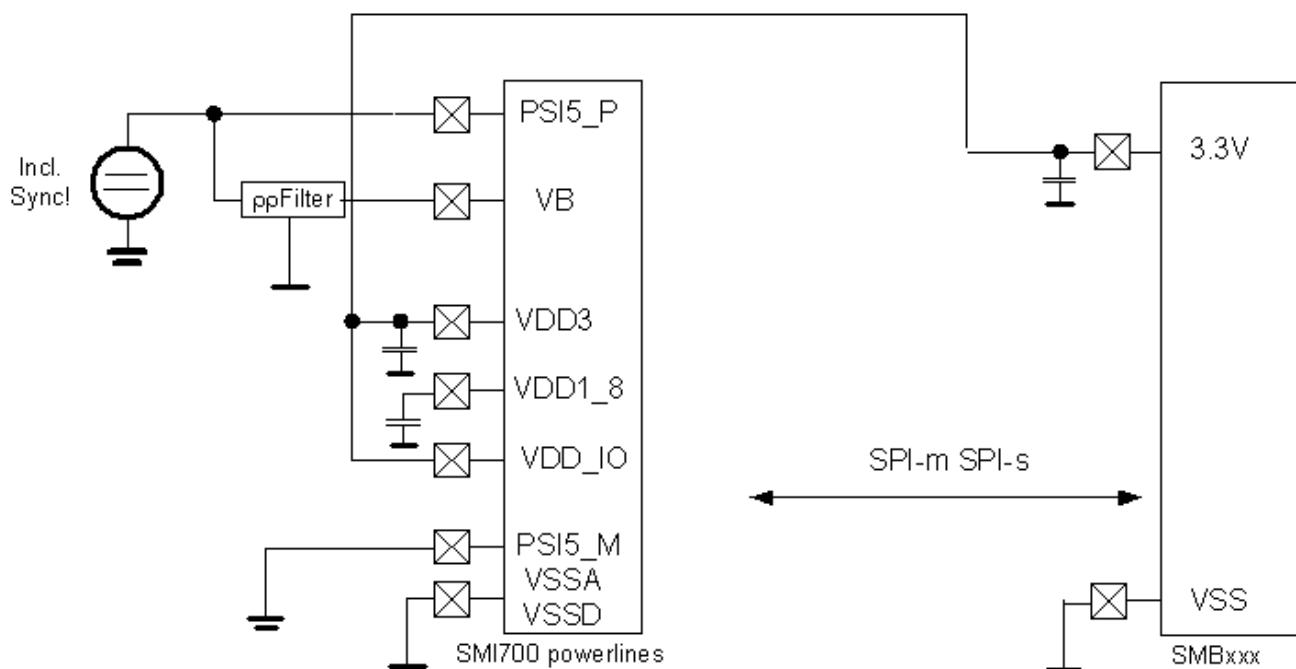
F03_12864 Mode5: PSI with SPI Slave, self-biased VDDIO

3.8.7 PSI5 with self supplied VDD_IO and secondary IC supply (Mode 6)

F03_2196

- It is also possible to connect another IC instead of a second TIG700. This mode is intended for using TIG700 with an additional acceleration device. The current consumption of the second device is strictly limited to the specified current listed under the paragraph electrical specification.
- VDD3 and VDD1_8 have to be connected to external blocking capacitors.
- See electrical specification (tables in 3.8.1) for the exact value of these capacitors.
- Only the VDD3 output can be used for supplying external ICs. Connection to VDD1_8 is strictly forbidden.

F03_391 Picture PSI5 with self supplied VDD_IO and secondary IC supply (Mode 6)



3.8.8 How to reconfigure the sensor for different applications

F03_9398 In order to change the default configuration, the following procedures have to be carried out:

Switch off XTAL_O if no CAN communication is used:

Set CX_PD = 1 in register MAIN_CAN_CFG (see {REF:F02_10335}).

Switch to SPI Master mode:

- configure desired polarity, phase, frequency, frame length, parity, drive strength and request master mode with SPI_PAD_CTRL_REQ = 1 in register MSPI_CTRL.
- disconnect pull-up resistors for CSB and SCLK by setting CSB_R_PU_DISABLE = 1, SCLK_R_PU_DISABLE = 1 in register MAIN_PULL_UP_CFG
- to send a message, fill TX_BUFFER, then set CSB_CTRL to 0 for the length of the message to be transmitted

Activate WDGI:

- Configure pulse width and period based on programmed clock ratio in registers WDGI_PULSE_WIDTH and WDGI_PULSE_PERIOD
(to be done by tuple programming at device level (for CAN devices))
- Enable WDGI pads by setting WDGI_PIN_EN = 1 in register WDGI_GPIO_CFG

3.9 Crystal oscillator (XTAL)

3.9.1 Functionality

F03_394

A crystal oscillator is used to create an electrical periodic signal with a very precise frequency. A quartz crystal can be modelled as a lumped elements circuit with low series impedance and a high anti-resonant impedance spaced closely together.

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3.9.2 Electrical / XTAL parameter

F03_419

Table 37: Electrical / XTAL parameters

Parameter	Condition	Symbol	Min	Typ	Max	Unit
XTAL frequency		f _{osc}		20		MHz
Settling Time of oscillation amplitude @ XTALO	90% of nominal amplitude @ XTALO	T _s			1.5	Ms
Jitter	1MBaud	T _{jit}			20	Ns
Equivalent series resistance		ESR			80	Ohm
Motional resistance		R ₁			80	Ohm
Motional inductance		L ₁		17.5		mH
Motional capacitance		C ₁	typ. - 30%	3.6	typ. +30%	fF
Shunt capacitance		C ₀	1.6	1.8	2.0	pF
XTAL Pin capacitance	C ₂ = C ₃	C _{2,C3}		8		pF
Optimal Load capacitance	$C_L = \frac{C_2 \cdot C_3}{C_2 + C_3} = \frac{1}{2} C_2$	C _L		4		pF
Mode of operation	Fundamental @ series resonant frequency					

F03_421

Crystal-circuit described - matching will be confirmed by CC/ECS4 with external crystal-supplier.
Improvements from previous projects for improved robustness will be implemented.

3.10 Communication interface

F03_2296

Generally the physical layer and the data link layer are realized in hardware. The protocol layer and the application layer will be realized in software for CAN, PSI and SPI Master Operation, while it will be fully implemented in HW for all SPI slave protocols.

Hint: Config Services are realized in SW even if called by SPI.

3.10.1 General purpose I/O pins

F03_2297

The pins MISO, TX and WDGI are always outputs, the pins RX and MOSI are always inputs. The pins CS_B and SCLK can be configured as input or output by the internal microcontroller. MISO, MOSI, CS_B, SCLK, TX, RX, WDGI can be used as general purpose pins (GPIO, GPI or GPO). By configuring a group (all SPI pins, all CAN pins) it loses its original purpose and can be directly accessed (read or write) by the internal microcontroller. All input pins are configurable to give an interrupt on change.

Configuration is possible by configuration set during startup that triggers a configuration register, which is set during startup. This configuration register can also be overwritten during operation by programming. Detailed description will be defined with A-Samples. Pins will be disabled by internal connection to VSS (Data set to 0). It is recommended to connect the pins externally also to GND for EMC purpose.

Additional Information:

Master SPI (2 possibilities):

CS_B can be used as output in master SPI mode with SCLK, MISO and MOSI controlled by hardware.

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CS_B, SCLK, MISO and MOSI controlled by µC.

CAN Pins:

TX, RX, WDGI together controlled by µC.

3.10.2 SPI interface

3.10.2.1 General

F03_447

This specification covers the SPI interface requirement for SMI7xy sensors. The standard interface consists of 4 ports as shown in Figure 27.

F03_448

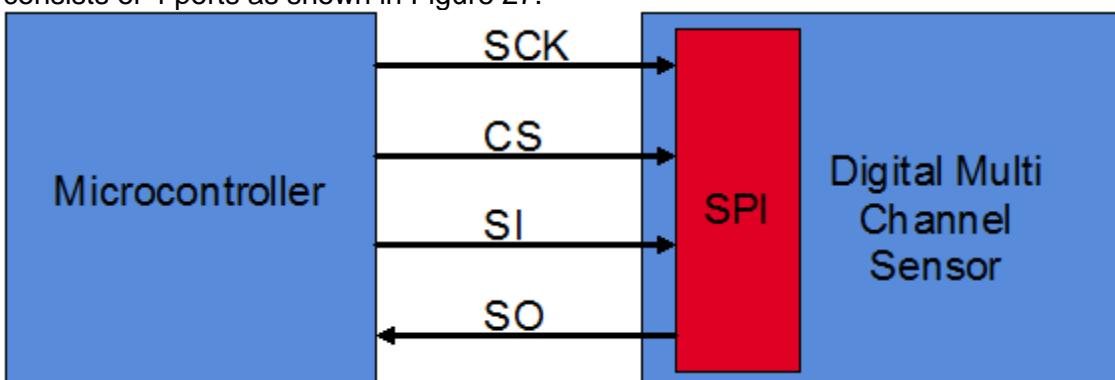


Figure 27: SPI- interface

F03_449

The **Serial clock (SCLK)** input represents the master clock signal. This clock determines the speed of data transfer and all receiving and sending is done synchronously to this clock. **Chip Select (CS_B)** activates the SPI interface. As long as CS_B is high, the sensor will not accept the clock signal or data input. The output MISO is in high impedance. Whenever CS_B is in a low physical state, data can be transferred from the micro controller and vice versa. Commands are transmitted through the **Serial Input (MOSI)** pin to the sensor and the sensor returns its response through the **Serial Output (MISO)** pin.

The same pins are used for the Master SPI with different directions.

F03_9306

The advanced SPI protocol features several sensors on one chip select line. Sensors can be logically addressed and only sensors which are asked will respond. Figure 2 shows an example configuration with several sensor modules. Each module may contain several sensor channels. Several modules may be connected on one chip select line.

F03_450

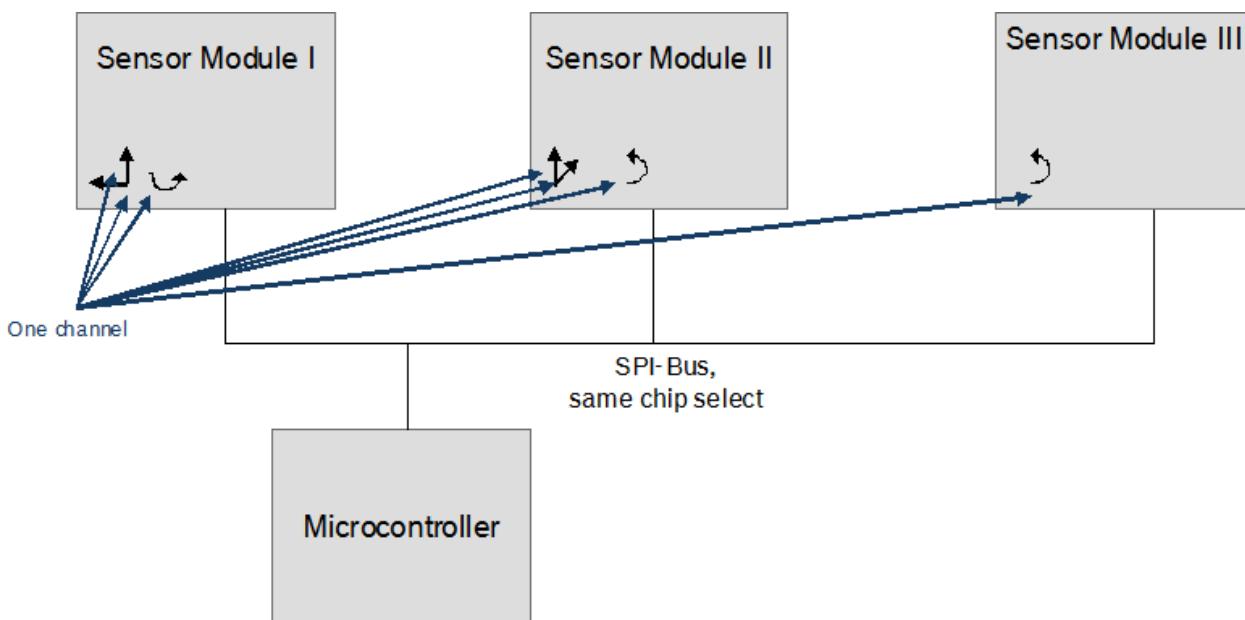


Figure 28: Sensor configuration and difference between sensor modules and sensor channel

3.10.2.2 Levels and timing for SPI slave

F03_2298 SPI clock phase and polarity are sensor individually configurable.

Requirements to slave from master-point of view (SMI is slave, parameters guaranteed by SMI):

F03_454

Table 38: Master-point of view

Identifier	Name	condition	min	max	Unit
	SPI clock frequency (Duty cycle 50/50) SPI_F_CLK			10,5	MHz
A	MISO data valid time (CSB)	VDD_IO = 3 V, capacitive load = 100 pF	-	40	ns
B	MISO data valid time (SCK)	VDD_IO = min, capacitive load = 100 pF	-	40	ns
		VDD_IO = min CL = 90 pF	-	32	ns
		VDD_IO = min CL = 80 pF	-	30	ns
		VDD_IO = min CL = 70 pF	-	29	ns
		VDD_IO = min CL = 60 pF	-	28	ns
		VDD_IO = min CL = 50 pF	-	27	ns
C	MISO data hold time*			-	ns
D	MISO rise/fall time	VDD_IO = min, capacitive load = 100 pF	-	15	ns
E	MISO data disable lag time		-	50	ns



F03_2336 * MISO data is guaranteed to be stable until the next SCK shift edge

F03_2337 The table assumes a VDD_IO voltage of 3V, a capacitive load of 100 pF and the strong MISO pad driver mode and the minimum drive frequency (PLL).

Parameters may be better for other voltages, drive frequency and capacitive loads (as far as covered by operating condition specification) and will be worse for the weak MISO pad driver mode.

Parameter A, B do not include the rise/fall time of CS_B and SCLK.

Requirements to master from slave-point of view (SMI is slave, parameters to be guaranteed by external SPI master):

F03_460

Table 39: Slave-point of view

Identifier	Name	Condition	min	max	Unit
4	SCK disable lead time	for 10 MHz mode, max load	10	-	ns
5	SCK enable lead time (CPHA = 0)	for 10 MHz mode, max load	40	-	ns
	SCK enable lead time (CPHA = 1)	for 10 MHz mode, max load	10	-	ns
6	SCK enable lag time	for 10 MHz mode, max load	10	-	ns
7	SCK disable lag time	for 10 MHz mode, max load	10	-	ns
9	Sequential transfer delay OpenSPI	for 10 MHz mode, max load	450	-	ns
	Sequential transfer delay CC32in	for 10 MHz mode, max load	200	-	ns
10	MOSI rise / fall time	for 10 MHz mode, max load	-	-	ns
11	MOSI data setup time	for 10 MHz mode, max load	10	-	ns
12	MOSI data hold time	for 10 MHz mode, max load	20	-	ns

F03_2405 The table assumes 10 MHz mode, max load.

F03_462

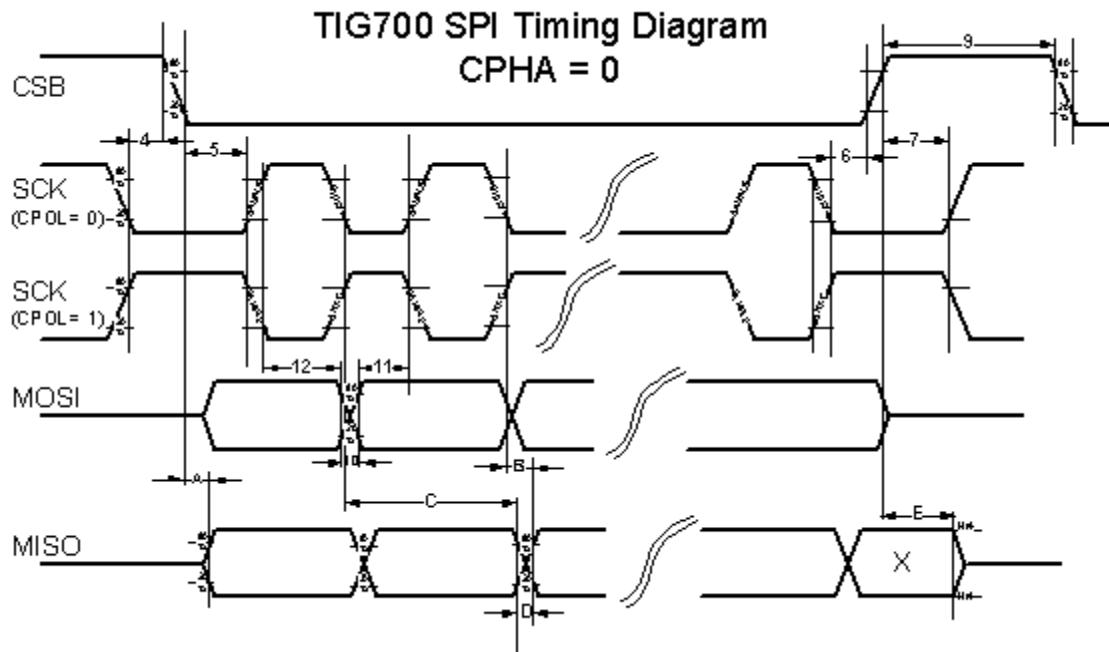
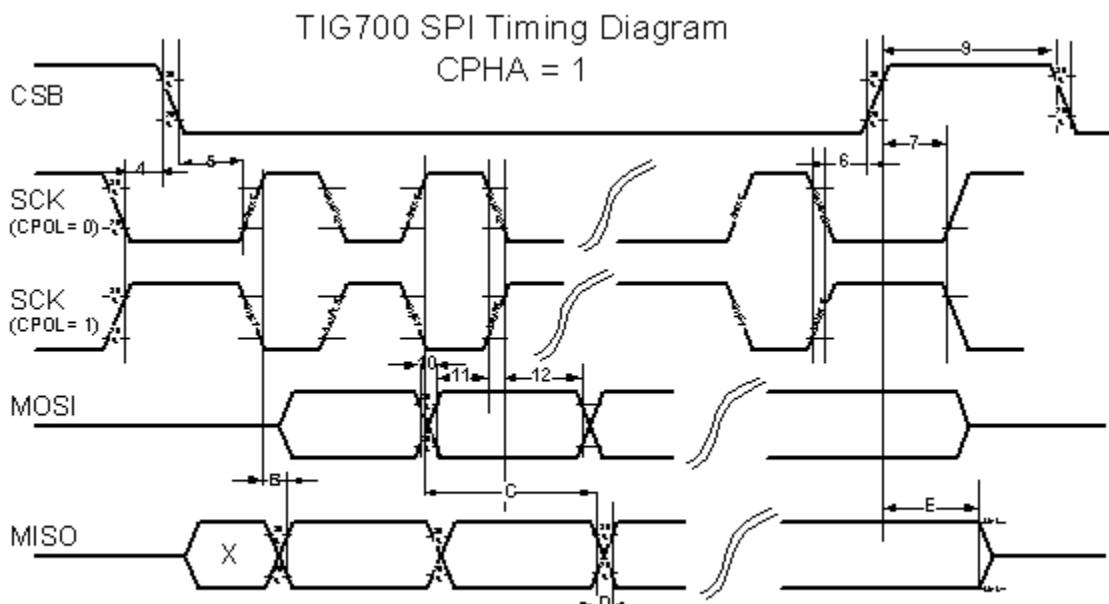


Figure 29: Timing diagram of info. on 1st edge of SCK

F03_464



Note: Parameter A is not applicable for CPHA=1

Figure 30: Timing diagram-sampling of information on 2nd edge of SCK

3.10.2.3 Data link layer

F03_467 In general terms there are two types of protocols - in-frame and out-of-frame. The in-frame protocol interleaves request and response in one message. The second protocol separates request and response in two messages sent consecutively.

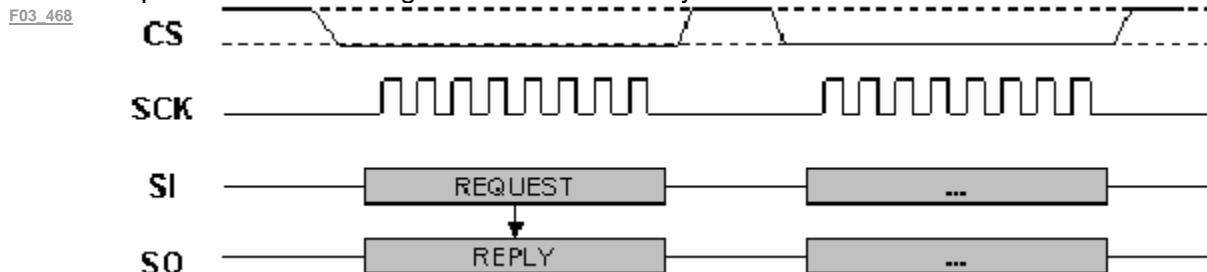


Figure 31: In-frame communication

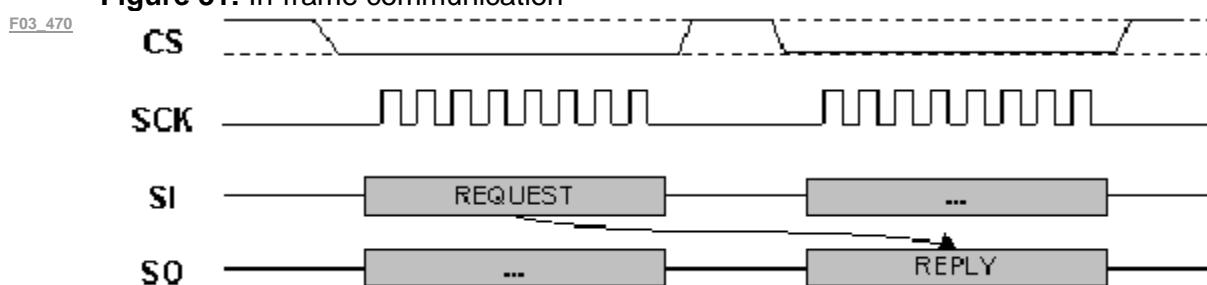


Figure : Out-of-frame communication

3.10.2.4 SPI slave activation

F03_2406 The SPI slave interface is locked after power on until the interface has been configured by the internal bootloader. While the interface is locked all requests are ignored and no response will be generated (MISO will stay at high impedance).

The RX pin logic level will be sampled once when the bootloader end is signaled.

F03_13516 Definition of start time for waiting on sampling the RX state in case of supplying at VB.
Time starts at voltage level at VB = 4,5V (min)

F03_13517 Definition of start time for waiting on sampling the RX state in case of supplying at VDD3.
Time starts at voltage level at VDD3 = 3,1V (min)

F03_13521 Sample time of RX pin logical level (main clock between min and max) = 1ms

F03_13522 Sample time starts after the following conditions have been fulfilled:

If Pin VB is used for powersupply, then VB must reach a voltage level RX_VB.

If Pin VDD3 is used for powersupply, then VDD3 must reach a voltage level of RX_VDD3.

If Pin RESET_B is used for external reset control, then RESET_B must have reached high level.

3.10.2.5 Common features of both 32bit SPI protocols (in-frame and out-of-frame)

3.10.2.5.1 Sensor addressing

F03_2407 The sensor will be applied on a SPI bus with several sensors on one chip select line. By using a specific addressing scheme different sensors can be addressed logically. Each sensor module has a specific bus address to communicate with. Each channel of a sensor module (i.e. rate, two accelerations, and for each channel normal output and monitor output) has also its own bus address. This means each TIG700



has 1 module-address and 6 channel-addresses. If measurement data of a sensor is requested, one of the channel addresses is used.

The module addresses must be configured for each individual system in the OTP (BUSADR(4:3)).

Two same sensors on the same CS line are configurable at ECU level with two different addresses via the potential applied to the RX Pin (= ID Pin). The potential is sampled after spi configuration due to bootloader, meaning that the potential is sampled >1 ms after startup.

This information needs to be transferred into the Reset Vector bit "BA3" on Device level (see {REF:F02_105}). Once the SPI_AUTOCALIB_EN in the Reset Vector bit is set to '0', the RX potential will be ignored and BUSADR(3) will be taken from bit "BA3" of the Reset Vector.

BUSADR(4): Denotes the module type (SMI700/SMI710) and is provided during bootloading from the OTP (written during module calibration at RtP1):

0=SMI700, 1=SMI710

BUSADR(3): Denotes the discriminator of two instances of the same module type on one SPI chip select line (written into the Reset Vector on Device level). Until end of line calibration the bit is sampled at startup from the RX Pin (= ID Pin). High potential (VDDIO) at RX pins equals '1', GND equals '0').

Broadcast Address: Using the broadcast address BUSADR(2:0)= 000b the upper bits of the busaddress BUSADR(4:3) are ignored and a module always reacts regardless of its actual module address as if a module command had been sent. This Address can be used in a single sensor configuration or during manufacturing when the module address is not known.

Module Address: Using the module address BUSADR(2:0)= 001b the upper bits of the busaddress BUSADR(4:3) are evaluated and only the module configured with the corresponding settings will recognise the module command. Other sensors possibly connected on the same chip select line will not react.

Valid Addresses are:

F03_487

Table 40: Valid address bits configured in the OTP

BUSADR(4)	BUSADR(3)	BUSADR(2)	BUSADR(1)	BUSADR(0)	Meaning
700/710	A/B	0	0	0	Module-broadcast
700/710	A/B	0	0	1	Module-address
700/710	A/B	0	1	0	Rate low-frequency
700/710	A/B	0	1	1	Rate high-frequency
700/710	A/B	1	0	0	Acc-1 low-frequency
700/710	A/B	1	0	1	Acc-1 high-frequency
700/710	A/B	1	1	0	Acc-2 low-frequency
700/710	A/B	1	1	1	Acc-2 high-frequency

3.10.2.5.2 Data capturing

F03_498

The protocol features data capturing. This means sensor measurement data and channel status of all channels (LF and HF) on one chip select line can be captured (stored sensor internally) at one point in time and read out at a later point in time. With this mechanism sensor data at one point of time of

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several sensors can be read subsequently. With this concept, the data and status of all channels can be measured at the same point in time.

F03_499

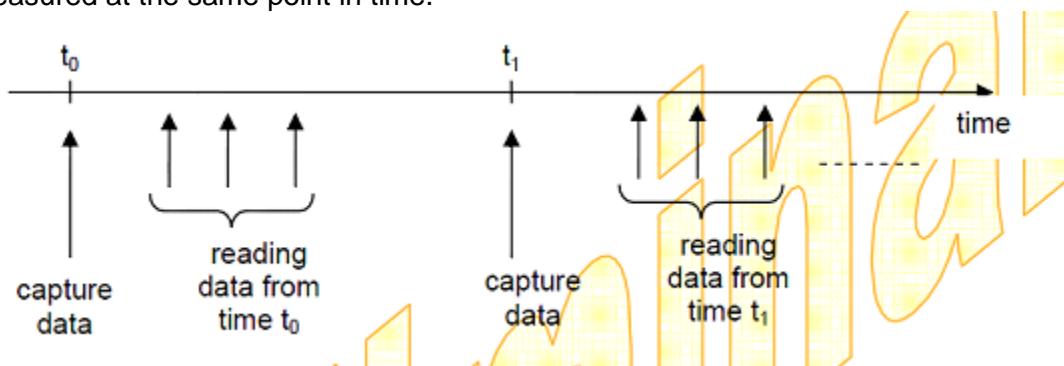


Figure 32: Data capturing timing

3.10.2.5.3 Address pages for 32 bit SPI protocols

F03_535

Register map page 0 (=default page after startup or reset):

Page	Adr	Description	Access
0	0x0	CONF_IREG0 Bit 15...0: CONF_IREG0 - uC Transfer input register 0, write on register issues interrupt to uC	read-write
0	0x1	CONF_IREG1 Bit 15...0: CONF_IREG1 - uC Transfer input register 1	read-write
0	0x1	CONF_IREG1 Bit 15...0: CONF_IREG1 - uC Transfer input register 1	read-write
0	0x2	CONF_IREG2 Bit 15...0: CONF_IREG2 - uC Transfer input register 2	read-write
0	0x3	CONF_IREG3 Bit 15...0: CONF_IREG3 - uC Transfer input register 3	read-write
0	0x4	CONF_OREG0 Bit 15...0: CONF_OREG0 - uC Transfer output register 0	read-only
0	0x5	CONF_OREG1 Bit 15...0: CONF_OREG1 - uC Transfer output register 1	read-only
0	0x6	CONF_OREG2 Bit 15...0: CONF_OREG2 - uC Transfer output register 2	read-only
0	0x7	CONF_OREG3 Bit 15...0: CONF_OREG3 - uC Transfer output register 3	read-only
0	0x8	CONF_RESV Bit 15...0: CONF_RESV - uC Transfer reserved register	read-only
0	0x9	password 1 for offset addressing	read-write



0	0xA	password 2 for offset addressing	read-write
0	0xB	password 1 for 64-bit SPI	read-write
0	0xC	password 2 for 64-bit SPI	read-write
0	0xD	RESET_VECTOR Reset Vector presets. Bit 0: PONBITE_ACC - Controls automatic PowerOnBite execution off ACC1 and ACC2 channels. Bit 1: PONBITE_YRS - Controls automatic PowerOnBite execution off YRS channel. Bit 2: SPI_AUTOCALIB_EN - Automatic calibration of SPI slave parameters. Bit 3: SO_DRIVER - SO pad driver strength. Bit 4: SPI_CPOL - SPI clock polarity parameter CPOL. Bit 5: SPI_CPHA - SPI clock phase parameter CPHA. Bit 6: SPI_PROT_SELECT - SPI protocol CC32in or OpenSPI. Bit 7: BA3 - Bit three of SPI sensor address BUSADR. Bit 8: cQBITE_HI_enable - Continuous Quadrature BITE high frequent enable Bit 9: cQBITE_LO_enable - Continuous Quadrature BITE low frequent enable Bit 10: PRE_REGULATOR_DISABLE - Disable the 5V pre regulator for 3V applications. '1' is 3V and '0' is 5V application Bit 11: PSI_OFF - PSI_OFF Signal Bit 12: DCAN_OFF - DCAN_OFF Signal	read-only
0	0xE	indirect adr ADDR_P1	read-write
0	0xF	upper 16 bit of last internal read access	read-only

F03_536

Register map page 1:

Page	Adr	Description	Access
1	0x0	PLL frequency	read-only
1	0x1	PLL_ICO_OUT Bit 8...0: PLL_ICO_OUT - Output to Oscillator DAC	read-only
1	0x1	PLL_ICO_OUT Bit 8...0: PLL_ICO_OUT - Output to Oscillator DAC	read-only
1	0x2	RATE_FEEDBACK Bit 3...0: RATE_FEEDBACK - Output of the quantizer to the feedback path	read-only
1	0x3	CQ_HIGH Bit 22...0: CQ_HIGH_VALUE - value of CQ_HIGH Bit 23: CQ_HIGH_VALUE_PARITY - Odd parity bit for bit 0-22	read-only
1	0x4	CQ_LOW Bit 22...0: CQ_LOW_VALUE - value of CQ_LOW Bit 23: CQ_LOW_VALUE_PARITY - Odd parity bit for bit 0-22	read-only



1	0x5	QUAD_I	
		Bit 22...0: QUAD_I_VALUE - value of QUAD_I	
		Bit 23: QUAD_I_VALUE_PARITY - Odd parity bit for bit 0-22	read-only
1	0x6	FASTSO2	
		Bit 7...0: DRV_DAC_OUT - Output to Drive DAC	
		Bit 15: DRV_SW_OUT - Output to Drive Switch	
		Bit 9...8: FE_GAIN - Value of front end gain	
		Bit 14...12: PLL_STATE - Output of the current PLL state	
		Bit 11...10: ZCD_STATE - Output of the state of the zero cross detection	read-only
1	0x7	QUAD_HF_LIMITED	
		Bit 15...0: QUAD_HF_LIMITED - quadrature high-frequency limited	read-only
1	0x8	channel_status_hw_scon	
		channel status generated by hw_scon	
		Bit 1...0: ACC1_HF_STATUS_HW_SCON - channel status of ACC1 HF generated by hw_scon	
		Bit 3...2: ACC1_LF_STATUS_HW_SCON - channel status of ACC1 LF generated by hw_scon	
		Bit 5...4: ACC2_HF_STATUS_HW_SCON - channel status of ACC2 HF generated by hw_scon	
		Bit 7...6: ACC2_LF_STATUS_HW_SCON - channel status of ACC2 LF generated by hw_scon	
		Bit 9...8: Yaw_Rate_HF_STATUS_HW_SCON - channel status of Yaw Rate HF generated by hw_scon	
		Bit 11...10: Yaw_Rate_LF_STATUS_HW_SCON - channel status of Yaw Rate LF generated by hw_scon	read-only
1	0x9	TEMP2	
		Bit 22...0: TEMP_SENSOR_2_VALUE - Value of temperature sensor 2	
		Bit 23: TEMP_SENSOR_2_VALUE_PARITY - Odd parity bit for bit 0-22	read-only
1	0xA	MAIN_SOFT_RST	
		Bit 15...0: SOFT_RESET - Soft reset, activated by SPI or software if password value 0xB26C is written	read-write
1	0xB	unused	
1	0xC	unused	
1	0xD	unused	
1	0xE	indirect adr ADDR_P2	read-write
1	0xF	indirect adr ADDR_P3	read-write



F03_15089 Register map page 2:

Page	Adr	Description	Access
2	0x0	TEMP1 Bit 22...0: TEMP_SENSOR_1_VALUE - value of temperature sensor 1 Bit 23: TEMP_SENSOR_1_VALUE_PARITY - Odd parity bit for bit 0-22	read-only
2	0x1	error_flag_16_bank0 bank 0 of error flags (16bit) Bit 0: dsp_rate_HF_adjust Bit 1: dsp_rate_LF_adjust Bit 2: dsp_HF_out Bit 3: dsp_LF_out Bit 4: dsp_acc1_HF_in Bit 5: dsp_acc1_LF_in Bit 6: dsp_acc1_HF_adjust Bit 7: dsp_acc1_LF_adjust Bit 8: dsp_adjust_data_err Bit 9: dsp_fine_err Bit 10: dsp_pe_flag_err Bit 11: dsp_pe_sign_err Bit 12: dsp_pe_irq_err Bit 13: dsp_sqrt_lim_flag Bit 14: dsp_gp_status Bit 15: dsp_pe_dsp_status_0_err	read-only
2	0x1	error_flag_16_bank0 bank 0 of error flags (16bit) Bit 0: dsp_rate_HF_adjust Bit 1: dsp_rate_LF_adjust Bit 2: dsp_HF_out Bit 3: dsp_LF_out Bit 4: dsp_acc1_HF_in Bit 5: dsp_acc1_LF_in Bit 6: dsp_acc1_HF_adjust Bit 7: dsp_acc1_LF_adjust Bit 8: dsp_adjust_data_err Bit 9: dsp_fine_err Bit 10: dsp_pe_flag_err Bit 11: dsp_pe_sign_err Bit 12: dsp_pe_irq_err Bit 13: dsp_sqrt_lim_flag Bit 14: dsp_gp_status Bit 15: dsp_pe_dsp_status_0_err	read-only
2	0x2	error_flag_16_bank1 bank 1 of error flags (16bit) Bit 0: dsp_acc1_HF_out Bit 1: dsp_acc1_LF_out Bit 2: dsp_acc2_HF_in Bit 3: dsp_acc2_LF_in	

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Bit 4: dsp_acc2_HF_adjust
Bit 5: dsp_acc2_LF_adjust
Bit 6: dsp_acc2_HF_out
Bit 7: dsp_acc2_LF_out
Bit 8: dsp_pe_ram_err
Bit 9: dsp_pe_sqrt_err
Bit 10: dsp_pe_dsp_status_1_err
Bit 11: dsp_pe_dsp_status_2_err
Bit 12: dsp_neg_flag_sqrt
Bit 13: dsp_ram_ifa13_err
Bit 14: dsp_ram_soaf_err
Bit 15: dsp_rom_crc_error read-only

2 0x3 error_flag_16_bank2
bank 2 of error flags (16bit)
Bit 0: dsp_cq_high_lim
Bit 1: dsp_cq_low_lim
Bit 2: dsp_quad_adjust
Bit 3: dsp_quad_QI_lim
Bit 4: dsp_ctm1_adjust
Bit 5: dsp_ctm2_adjust
Bit 6: dspmem_debugaccess_on
Bit 7: dsp_online_test
Bit 8: can_ram_parity
Bit 9: dsp_pe_quad_i_sqrt_udf_err
Bit 10: uc_otp_prog_bist_inital
Bit 11: uc_otp_data_bist_inital
Bit 12: uc_otp_data_corrupt_header
Bit 13: uc_otp_data_invalid_tuple
Bit 14: uc_tuple_readback_mismatch
Bit 15: uc_hw_timeout read-only

2 0x4 error_flag_16_bank3
bank 3 of error flags (16bit)
Bit 0: uc_rom_bist
Bit 1: uc_ram_ifa13
Bit 2: uc_ram_soaf
Bit 3: uc_ram_par_error
Bit 4: uc_watchdog_err
Bit 5: uc_otp_data_bist
Bit 6: uc_otp_prog_bist
Bit 7: uc_stack_check
Bit 8: uc_psi_async_timing
Bit 9: uc_unrecoverable_error
Bit 10: uc_rom_otp_sw_incompatible
Bit 11: uc_can_psi_readback_mismatch
Bit 12: uc_otp_data_open_bank
Bit 13: uc_generic_error_flag_2
Bit 14: uc_generic_error_flag_3
Bit 15: uc_generic_error_flag_4 read-only



- 2 0x5 error_flag_16_bank4
bank 4 of error flags (16bit)
Bit 0: yrs_drv_bp_lim
Bit 1: yrs_rate_pt2_lim
Bit 2: yrs_agc_irregular
Bit 3: yrs_pll_unlock
Bit 4: yrs_pll_lim
Bit 5: yrs_drv_adc
Bit 6: yrs_rate_adc
Bit 7: yrs_rate_quantizer
Bit 8: yrs_rate_adc_mean
Bit 9: yrs_drv_pi_tol
Bit 10: yrs_pll_tol
Bit 11: yrs_drv_adc_mean
Bit 12: yrs_drv_cu_gain
Bit 13: yrs_rate_seq_bite
Bit 14: yrs_quad_seq_bite
Bit 15: yrs_quad_cq_bite read-only
- 2 0x6 error_flag_16_bank5
bank 5 of error flags (16bit)
Bit 0: yrs_quad_cqhigh_bite
Bit 1: yrs_quad_cqlow_bite
Bit 2: yrs_quad_hf_tol
Bit 3: yrs_quad_i_tol
Bit 4: yrs_rate_v_tn
Bit 5: yrs_rate_v_com
Bit 6: yrs_rate_v_cm
Bit 7: yrs_rate_v_fb
Bit 8: acc1_seq_bite
Bit 9: acc2_seq_bite
Bit 10: acc2_overload_det
Bit 11: acc1_overload_det
Bit 12: acc1_v_cm
Bit 13: acc2_v_cm
Bit 14: acc1_ds_lim
Bit 15: acc2_ds_lim read-only
- 2 0x7 error_flag_16_bank6
bank 6 of error flags (16bit)
Bit 0: ctm_range
Bit 1: ctm_diff
Bit 2: acc_clk_ovlp
Bit 3: v_cp_high
Bit 4: v_cp_low
Bit 5: v_yrs_high
Bit 6: v_yrs_low
Bit 7: v_acc_high
Bit 8: v_acc_low
Bit 9: v_dig_high
Bit 10: v_ctm_high
Bit 12: v_prereg_low



		Bit 13: v_prereg_11_high Bit 14: vdd3_high Bit 15: vdd3_low read-only
2	0x8	error_flag_16_bank7 bank 7 of error flags (16bit) Bit 0: v_ctm_low Bit 1: cmg_f_check Bit 2: lbist_err Bit 3: pc_shd Bit 4: pc_cs1 Bit 5: pc_cp Bit 6: pc_vdd3_vdd1_8 Bit 8: pc_vssa Bit 9: pc_vssd Bit 10: pc_psi5_m Bit 11: acc1_clk_cnt Bit 12: acc2_clk_cnt Bit 14: uc_ram_dpath Bit 15: dsp_ram_dpath read-only
2	0x9	error_flag_16_bank8 bank 8 of error flags (16bit) Bit 0: misc_apb_slv Bit 1: main_ctrl_apb_slv Bit 2: dsp_apb_slv Bit 3: conf_apb_slv Bit 4: can_apb_slv Bit 5: frontend_apb_slv Bit 6: uc_sub_apb_slv Bit 7: hw_scon_apb_slv Bit 8: psi_apb_slv Bit 9: spi_apb_slv Bit 10: spi_mst_apb_slv Bit 11: gpt_apb_slv Bit 12: ahb_hang_up Bit 13: ctm_apb_slv Bit 14: sfr_apb_slv Bit 15: dsp_rom_apb_slv read-only
2	0xa	error_flag_16_bank9 bank 9 of error flags (16bit) Bit 0: dsp_ram_apb_slv Bit 1: acc1_pe_flag_8k_err Bit 2: acc1_pe_flag_1k_err Bit 3: acc2_pe_flag_8k_err Bit 4: acc2_pe_flag_1k_err Bit 5: pe_flag_cic4_err Bit 6: pe_flag_quad_2k_err Bit 7: pe_flag_quad_8k_err Bit 8: pe_flag_rate_8k_err Bit 9: pe_flag_rate_1k_err



		Bit 10: dsp_ram_toggle_missing Bit 11: dsp_rom_toggle_missing Bit 12: uc_ram_toggle_missing Bit 13: uc_rom_toggle_missing Bit 14: otp_data_toggle_missing Bit 15: otp_prog_toggle_missing read-only
2	0xB	err_cnt_comb_0 Combined Error Counter 0 (error_cnt_1 / error_cnt_0) Bit 15...0: err_cnt_comb_0 - Combined Error Counter 0 (error_cnt_1 / error_cnt_0) read-only
2	0xC	err_cnt_comb_1 Combined Error Counter 1 (error_cnt_3 / error_cnt_2) Bit 15...0: err_cnt_comb_1 - Combined Error Counter 1 (error_cnt_3 / error_cnt_2)read-only
2	0xD	err_cnt_comb_2 Combined Error Counter 2 (error_cnt_5 / error_cnt_4) Bit 15...0: err_cnt_comb_2 - Combined Error Counter 2 (error_cnt_5 / error_cnt_4) read-only
2	0xE	err_cnt_comb_3 Combined Error Counter 3 (error_cnt_7 / error_cnt_6) Bit 15...0: err_cnt_comb_3 - Combined Error Counter 3 (error_cnt_7 / error_cnt_6) read-only
2	0xf	error_group_out = 16 Bit Flag Cluster Meaning of Bits: see Functional Safety chapter read-only

F03_15088 Register map page 3:

Page	Adr	Description	Access
3	0x0	scon_adc_ucm_yaw result of scon adc for ucm_yaw Bit 11...0: scon_adc_ucm_yaw - result of scon adc for ucm_yaw	read-only
3	0x1	scon_adc_ucm_acc1 result of scon adc for ucm_acc1 Bit 11...0: scon_adc_ucm_acc1 - result of scon adc for ucm_acc1	read-only
3	0x1	scon_adc_ucm_acc1 result of scon adc for ucm_acc1 Bit 11...0: scon_adc_ucm_acc1 - result of scon adc for ucm_acc1	read-only
3	0x2	scon_adc_ucm_acc2 result of scon adc for ucm_acc2 Bit 11...0: scon_adc_ucm_acc2 - result of scon adc for ucm_acc1	read-only
3	0x3	scon_adc_temp1 result of scon adc for temp1	



		Bit 11...0: scon_adc_temp1 - result of scon adc for temp1	read-only
3	0x4	scon_adc_temp2 result of scon adc for temp2 Bit 11...0: scon_adc_temp2 - result of scon adc for temp2	read-only
3	0x5	scon_adc_det_cncp result of scon adc for det_cncp Bit 11...0: scon_adc_det_cncp - result of scon adc for det_cncp	read-only
3	0x6	scon_adc_fb_mux result of scon adc for fb_mux Bit 11...0: scon_adc_fb_mux - result of scon adc for fb_mux	read-only
3	0x7	scon_adc_udf_det result of scon adc for udf_det Bit 11...0: scon_adc_udf_det - result of scon adc for udf_det	read-only
3	0x8	unused	
3	0x9	unused	
3	0xA	unused	
3	0xB	unused	
3	0xC	unused	
3	0xD	unused	
3	0xE	unused	
3	0xF	unused	

F03_15090 Register map page 4:

Page	Adr	Description	Access
4	0x0	ASIC_SERIAL_NR_0 Serial number programmed at electrical wafer sort part 0 Bit 15...0: ASIC_SERIAL_NR_0 - Serial number Bit 15 - 0	read-only
4	0x1	ASIC_SERIAL_NR_1 Serial number programmed at electrical wafer sort part 1 Bit 15...0: ASIC_SERIAL_NR_1 - Serial number Bit 31 - 16	read-only
4	0x1	ASIC_SERIAL_NR_1 Serial number programmed at electrical wafer sort part 1 Bit 15...0: ASIC_SERIAL_NR_1 - Serial number Bit 31 - 16	read-only
4	0x2	ASIC_SERIAL_NR_2	



		Serial number programmed at electrical wafer sort part 2 Bit 15...0: ASIC_SERIAL_NR_2 - Serial number Bit 47 - 32	read-only
4	0x3	ASIC_NAME Name of ASIC (TIG700) Bit 15...0: ASIC_NAME - Name of Chip (TIG700)	read-only
4	0x4	ASIC_REVISION Revision of ASIC (e.g. AA) Bit 7...0: REVISION_ID - 2 digit revision in BCD.	read-only
4	0x5	SMI_SERIAL_NR_0 Serial number of SMI part 0 Bit 15...0: SMI_SERIAL_NR_0 - Serial number of SMI bit 15 - 0.	read-only
4	0x6	SMI_SERIAL_NR_1 Serial number of SMI part 1 Bit 15...0: SMI_SERIAL_NR_1 - Serial number of SMI bit 31 - 16.	read-only
4	0x7	SMI_SERIAL_NR_2 Serial number of SMI part 2 Bit 15...0: SMI_SERIAL_NR_2 - Serial number of SMI bit 47 - 32.	read-only
4	0x8	CUSTOMER_SERIAL_NR Serial number of customer. Bit 15...0: CUSTOMER_SERIAL_NR - Serial number of customer.	read-only
4	0x9	sampled logic-level of RX-pin	read-only
4	0xA	Safety IDs for HF channels: Bit 14...10: SID Rate HF Bit 9...5: SID ACC2 HF Bit 4...0: SID ACC1 HF	read-only
4	0xB	Safety IDs for LF channels: Bit 14...10: SID Rate LF Bit 9...5: SID ACC2 LF Bit 4...0: SID ACC1 LF	read-only
4	0xC	ACC1_DIST_CNT Bit 11...0: ACC1_DIST_CNT - Number of errors detected by disturbance_det in ACC1 within last detection period.	read-only
4	0xD	ACC2_DIST_CNT Bit 11...0: ACC2_DIST_CNT - Number of errors detected by disturbance_det in ACC2 within last detection period.	read-only
4	0xE	unused	
4	0xF	unused	

F03_15091 Register map page 5:

Page	Adr	Description	Access
5	0x0	LAST_BITE_ACC1_POS Bit 15...0: LAST_BITE_ACC1_POS - Result of last internal BITE sequence.	read-only
5	0x1	LAST_BITE_ACC1_NEG Bit 15...0: LAST_BITE_ACC1_NEG - Result of last internal BITE sequence.	read-only
5	0x1	LAST_BITE_ACC1_NEG Bit 15...0: LAST_BITE_ACC1_NEG - Result of last internal BITE sequence.	read-only
5	0x2	LAST_BITE_ACC2_POS Bit 15...0: LAST_BITE_ACC2_POS - Result of last internal BITE sequence.	read-only
5	0x3	LAST_BITE_ACC2_NEG Bit 15...0: LAST_BITE_ACC2_NEG - Result of last internal BITE sequence.	read-only
5	0x4	LAST_BITE_QUAD_YR_POS Bit 15...0: LAST_BITE_QUAD_YR_POS - Result of last internal BITE sequence.	read-only
5	0x5	LAST_BITE_QUAD_YR_NEG Bit 15...0: LAST_BITE_QUAD_YR_NEG - Result of last internal BITE sequence.	read-only
5	0x6	LAST_BITE_QUAD_YR_ZERO Bit 15...0: LAST_BITE_QUAD_YR_ZERO - Result of last internal BITE sequence.	read-only
5	0x7	LAST_BITE_RATE_YR_POS Bit 15...0: LAST_BITE_RATE_YR_POS - Result of last internal BITE sequence.	read-only
5	0x8	LAST_BITE_RATE_YR_NEG Bit 15...0: LAST_BITE_RATE_YR_NEG - Result of last internal BITE sequence.	read-only
5	0x9	LAST_BITE_RATE_YR_ZERO Bit 15...0: LAST_BITE_RATE_YR_ZERO - Result of last internal BITE sequence.	read-only
5	0xa	DEBUG_CONTROL Bit 14...7: ADDR_DEBUG_1 - Address for debug_1 value Bit 22...15: ADDR_DEBUG_2 - Address for debug_2 value Bit 23: ADDR_DEBUG_PARITY - Address for debug_2 value	read-only

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5	0xb	DEBUG_OUT_1
		Bit 22...0: DEBUG_OUT_1_VALUE - Debug_1 value of DSP
		Bit 23: DEBUG_OUT_1_VALUE_PARITY - Odd parity bit for bit 0-22
		Bit 31...24: DEBUG_COUNTER_1 - Debug counter value of DSP (7:0) read-only
5	0xc	DEBUG_OUT_2
		Bit 22...0: DEBUG_OUT_2_VALUE - Debug_2 value of DSP
		Bit 23: DEBUG_OUT_2_VALUE_PARITY - Odd parity bit for bit 0-22
		Bit 31...24: DEBUG_COUNTER_2 - Debug counter value of DSP (7:0) read-only
5	0xd	DEBUG_OUT_1_2_CAPTURED
		Bit 22...0: DEBUG_OUT_1_2_CAPTURED - Captured debug_2 value at the time when DEBUG_OUT_1 has been read, or captured debug_1 value at the time when DEBUG_OUT_2 has been read.
		Bit 23: DEBUG_OUT_1_2_CAPTURED_PARITY - Odd parity bit for bit 0-22
		Bit 31...24: DEBUG_COUNTER_CAPTURED_3 - 8bit (7:0) Captured debug counter value of DSP read-only
5	0xe	DEBUG_COUNTER_CAPTURED
		Bit 22...7: DEBUG_COUNTER_CAPTURED_4 - 16bit Captured Debug counter value of DSP (15:0)
		Bit 23: PARITY_DEBUG_COUNTER_CAPTURED_4 - parity of Captured Debug counter value of DSP read-only
5	0xf	unused

F03_15092 Register map page 6:

Unused

F03_15093 Register map page 7:

unused

3.10.2.6 SPI CC32in

F03_477 The CC32in-protocol is an in-frame SPI protocol. The protocol offers access to all sensor data channels using "sensor data commands" and to additional module information using "sensor module commands".

3.10.2.6.1 Polarity, phase and protocol selection / command calibration

F03_2472 SPI clock polarity (CPOL), clock phase (CPHA) and protocol (CC32in or OpenSPI) can be programmed at end of line ECU calibration for each sensor module individually with the settings in the reset-vector. If the programmed settings shall be used by the sensor, the bit SPI_AUTOCALIB_EN in the Reset Vector must be "0".

When the module is being delivered, the bit SPI_AUTOCALIB_EN in the reset-vector is "1" (see {REF:F02_105}). In this case, CPOL, CPHA and the SPI protocol can be changed after startup of the sensor.

F03_13404 For CPOL, CPHA and protocol selection a special Calibration-Command is used. This Calibration-Command is only accepted, if it is the first SPI-Command after the reset and if the bit SPI_AUTOCALIB_EN reset-vector is set. Calibration-Commands will have a high impedance SO as response. Regular SPI commands are not accepted nor executed as first command after reset if SPI_AUTOCALIB_EN=1!

F03_13405 The Calibration Command for CC32in and CPHA = 0 is 0x10000004 (bits 31:0).



The Calibration Command for CC32in and CPHA = 1 is 0x1003FFF4 (bits 31:0).

The Polarity is automatically detected from the request frame.

For OpenSPI calibration commands see section 10.5.2.

F03_13406 The answer to the first command will be generally high-impedance, as long as SPI_AUTOCALIB_EN=1. All sensors on the same CS line with SPI_AUTOCALIB_EN=1 will accept the calibration command. Regular SPI commands are not accepted nor executed as first command after reset if SPI_AUTOCALIB_EN=1!

As soon as SPI_AUTOCALIB_EN=0, the settings of the reset-vector will be used (see {REF:F02_105}). Then, the sensor will answer on the first command as specified (instead of high impedance when SPI_AUTOCALIB_EN=1). If a calibration SPI command is received even though SPI_AUTOCALIB_EN=0, the sensor will try to interpret it as regular SPI command resulting in a recognized CRC error (TF bit set) for modules with BUSADR(4:3)=b00 or tristate answer on MISO for modules with BUSADR(4:3) other than b00.

3.10.2.6.2 Detailed SPI protocol structure

F03_501 The frame is an in-frame protocol with 32 clock cycles. In-frame means that the logical response to a request is in the same frame. All commands have a basic structure which will be valid for all commands. The base structure is described in the following table.

F03_502 **Table 41:** Communication frameset

1.row=Bit#, 2.row=MOSI, 3.row=MISO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	...	6	5	4	3	2	1	0
BUSADR(4:0)																CRC	*						
TRI	OE	SD															CRC/TF						

F03_2473 **Table 42:** Frameset description

BUSADR	To address different modules or different data channels.
CRC	3bit CRC over bits 31 to 5 polynom: x^3+x+1 , start value: 111b, target value 000b.
TRI	Sensor output is tri-state (high impedance, high resistance)
SD	Sensor channel data or module data - 0: module data - 1: sensor data
OE	Offrame-Error (OE will be transmitted in next frame, only visible in next frame) 1: sclk-cycles not equal 32 (16 for 16 bit airbag mode) 0: else
CRC/TF	3bit CRC over bits 26 to 3. Polynom: x^3+x+1 , start value: 111b, target value 000b. If CRC of request (MOSI) was wrong or command is unknown or a read access on the APB bus failed a transfer failure will be signaled by destroying the CRC of the response (MISO). The last bit (TF) of the calculated CRC will be inverted.
*	These bits are ignored by the sensor and can be either 0 or 1.

3.10.2.6.3 Sensor data commands

F03_505 If the bus-address is not a sensor module address (XX000b or XX001b) the sensor interprets the command as sensor channel command. The addressed channel (channel-address is identical to channel-address, see section 10.4.1) will respond to the command. Capture bits are interpreted from all modules on a chip select line.

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**Table 43:** Communication frameset for sensor data commands

F03_507

1.row=Bit#, 2.row=MOSI, 3.row=MISO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	...	6	5	4	3	2	1	0
BUSADR(4:0)	CAP(2:0)	*	16BITADR (4:0)		*												CRC		*				
TRI	OE	SD	SID(4:0)		R-DATA(15:0)												CN	CRC/TF					

F03_2498

Table 44: Frameset description

BUSADR	Bus Address: is configurable at end of line ECU calibration in OTP (see 4.10.4.1) all addresses not equal to XX000b or XX001b are valid channel-addresses
CAP	<p>bits to define if captured or current data should be read and if data should be captured</p> <p>011b: read current data and channel-status (do not alter captured data)</p> <p>010b: read captured data and channel status (do not capture or alter captured data)</p> <p>101b: sensor channels of any module on the bus must capture data and channel status of all channels. Only channel with valid BUSADR: read capture data of selected channel afterwards</p> <p>else: reserved (illegal command)</p> <p>Remarks:</p> <ul style="list-style-type: none"> - Sensor will capture data before being able to check CRC bits. Therefore, the CAP command is defined as 3 bit value with higher hamming distance (redundancy) since write access is not CRC protected. - When reading captured date the CN bit in the MISO frame for is a combination (logical OR) of the CN bit at the reading time and the sampling time.
SID(4:0)	Safety ID. Each sensor channel (rate, twice acceleration, HF or LF output channel) must be configurable at end of line ECU calibration to its specific SID.
CN	<p>Channel Not Valid (also different for monitor and normal output)</p> <p>0: channel sensor data fully valid</p> <p>1: channel sensor data not valid (sensor error, initialization, or self test) if captured data is read, then the CN-bit is the captured CN OR the actual CN</p>
R-DATA(15:0)	Two's complement sensor data of selected channel
16BITADR(4:0)	<p>Only used for passive safety systems. Should be set to 00000b for all other systems.</p> <p>If the 16BITADR is identical to a programmed channel-address, the sensor will respond off-frame with a special 16-bit frame. See chapter "Airbag Backward Compatibility: Special 16 bit Mode" for details.</p>
OE	Offrame-Error (OE will be transmitted in next frame, only visible in next frame)
	1: sclk-cycles not equal 32
	0: else
SD	Sensor channel data or module data: 1 for sensor channel data commands.
*	These bits are ignored by the sensor and can be either 0 or 1.

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3.10.2.6.4 Module Commands

F03_9308 With Module Commands all data provided on the SPI pages 0...7 can be accessed.

By unlocking the password mechanism all inframe-capable addresses can be accessed. This mechanism is not needed in field operation and is therefore not described in this document.

F03_510 **Table 45:** Communication frameset for module commands

F03_511 1.row=Bit#, 2.row=MOSI, 3.row=MISO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BUSADR(4:0)				ADR(3:0)				W	W-DATA(15:0)				CRC				*							
TRI				OE	SD	MID		PAGE				R-DATA(15:0)				CRC/TF								

F03_2518 **Table 46:** Frameset description

BUSADR(4:0)	Module Address: BUSADR(4:3): is configurable at calibration in OTP XX001b valid module-address, one module will react XX000b broadcast-address: all modules will react
ADR(3:0)	Address within current page of data to be read or to be written
W	Write data. (Writing to a read only register gives a transfer failure) 0: read data (WDATA is being interpreted for Offset Address handling, see section 10.4.7) 1: write W-DATA to sensor
W-DATA(15:0)	Data written to the sensor
MID	Module ID to identify which module responded MID(2:1) = BUSADR(4:3) MID(0) = BUSADR(0) 1: reaction on individual module command 0: reaction on broadcast command (broadcast commands are often used during final measurement in order to simplify the communication)
OE	Offrame-Error (OE will be transmitted in next frame, only visible in next frame) 1: Last write bus access on APB bus not successful or sclk-cycles not equal 32 (16 for 16bit airbag mode) 0: ok Note: If the next frame after a write is sensor-command the information of the write status will be lost. It will only be visible in an immediately following non-sensor command.
PAGE	Identifies page number (Offset) from which data is read or written to 0 = page 0 (0x0000) 1 = page 1 (0x0001) 2 = page 2 (0x0002) 3 = page 3 (0x0003) 4 = page 4 (0x0004) 5 = page 5 (0x0005) 6 = page 6 (0x0006) 7 = page 7 (0x0007 or higher)
R-DATA(15:0)	Data read from sensor
SD	Sensor channel data or module data: 0 for module commands.
*	These bits are ignored by the sensor and can be either 0 or 1.



3.10.2.6.4.1 Paging Mechanism

F03_2545 Since only 16 Registers can be accessed with the 4 bit address field ADR(3:0), a paging mechanism is implemented.

The current page is returned in the MISO response of the sensor. When using module commands it is recommended to check the returned page information in the MISO response to ensure that read/write operations are performed on the correct page.

After sensor startup the default page is 0.

The page can be switched using read-commands with the (in read-commands otherwise unused) W-DATA field.

F03_2546 **Module command for page switching:**

1.row=Bit#, 2.row=MOSI, 3.row=MISO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	...	9	8	7	6	5	4	3	2	1	0
BUSADR(4:0)					ADR(3:0)	0	0	1				0		New Page	CRC	*								
TRI	OE	SD		MID		PAGE			R-DATA(15:0)						CRC/TF									

Description:

Bit 22: R/W command bit, "0" for module read command

Bit 20: W-DATA(15), "1" as identifier for page switching command (otherwise normale read command is executed)

Bits 19...8: W-DATA(13...3), must be "0". Otherwise a Transfer Failure will be signaled without PW for offset addressing being provided.

Bits 7...5: New Page - Number of new page to be set.

The new page will be valid from the subsequent frame to the switching command. Therefore the PAGE field in the MISO repsonse of the switching command will still return the current (old) page.

Since a page switching command is also a valid "read" module command it is possible to read an address from the current page and switch to a new page within one command.

3.10.2.6.4.1.1 Indirect register access mechanism

F03_2548 During boot loading three addresses, that have been programmed into the OTP at final testing in Rt, will be copied into three SPI-internal registers (*SPI_CONF.ADDR_P1*, *SPI_CONF.ADDR_P2*, *SPI_CONF.ADDR_P3*). When accessing these registers, the decoder will deliver these programmed addresses, which will then be used by the SPI for the internal bus access.

The three 16 bit register holds the lower 16 bit of the internal 32bit APB address, which will be automatically extended with 16 upper bits (0x4000) that constitute the internal 32 bit address. Therefore the implicit extension limits the indirect addressable content to the range 0x40000000 - 0x400018FF, because all other regions are not inframe capable by default.

3.10.2.6.5 Password mechanism

F03_2549 The passwords to access registers not available on SPI pages 0...7 and for switching to 64bit SPI protocol are not required for field operation and will not be documented in this document.
Passwords exclude each other and can not be used parallel.

3.10.2.6.6 Airbag backward compatibility: special 16bit mode

F03_2550 If the 16 BITADR in previous 32-bit frame is identical to the bus address, the sensor will respond with a special 16 bit frame. The data on MOSI will be ignored by all sensors on the bus.



DATA*(15:6) upper 10bit of channel current data clipped to +/-480LSB (referred to 10bit).

No captured data will be readable in backward compatibility mode.

The 16-bit frame has the following format:

F03_548

Table 48: 16bit frame format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
0	0	S	SID(2:0)		R-DATA(15:6)										

F03_2551

* These bits are ignored by the sensor and can be either 0 or 1.

S status of channel (as status of channel for normal channel commands)

SID(2:0) lowest 3 bits from 5-bit Safety ID (SID) (2:0)

R-DATA(15:6) upper 10bit of channel current data clipped to +/-480LSB (referred to 10bit).

3.10.2.6.6.1 Error Handling

Error	Description	Reaction
cpol_err	The polarity of SCK-Pin is sampled at each falling-edge of CSB. If the sampled value is not equal to the setting of CPOL, the MISO will stay high-impedant.	no answer (tristate)
sckcnt_err	Number of clock cycles does not match the valid frame length (16, 32)	Bit26 in next frame is set (OE-bit)
crc_err	CRC of the received SPI message is not valid	CRC last bit inverted
invalid_instr_err	Received SPI command not recognized as valid instruction	CRC last bit inverted
ba_finish_err	Internal ABP Bus access not accomplished during 2 pll-clock-cycles	CRC last bit inverted
cpha_error	SPI is currently not working in the phase that was defined during startup	Phase errors cannot be detected; the sensor will not understand the message, resulting in a CRC error.

F03_16125 If the interframe delay is smaller than an internal clock cycle the rising edge and falling edge of CSB will not be sampled and the frame will be extended with additional bits. It will be the same behaviour as if the frame has too many clock cycles.

If the CSB is sampled correct a valid frame will be generated for any read command; for write commands the WS (write status) may be incorrect.

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3.10.2.7 SPI dialect SMI7-32OUT (B-samples)

3.10.2.7.1 Detailed SPI protocol structure SMI7-32OUT

F03_555 The frame is an 'out- of- frame' protocol with 32 clock cycles. Out- of- frame means that the logical response to a request is in the next frame. All commands have a basic structure which will be valid for all commands.

3.10.2.7.2 Polarity, phase and protocol selection / calibration command

F03_2620 Polarity, phase and protocol (i.e. SPI 32IN or SPI 32OUT) will be selectable at end of line ECU calibration for each sensor module individually with the settings in the reset-vector. When the module is being delivered, the reset-vector is not activated, therefore the default settings for polarity, phase and protocol will be used (see {REF:F02_105}). Without the reset-vector being activated, the sensor accepts a calib.-SPI command as first command.

To set sensor to out of frame SPI (if sensor is in in frame mode, Module A) the following calibration commands are used for A samples:

CPHA=1: 0xEF9FFE0 for phase set to be 1
CPHA=0: 0xEF800014 for phase set to be 0

To set sensor to in frame SPI (if sensor is in out of frame mode, Module A) the following calibration commands are used for A samples:

CPHA=0: 0x10000004 for phase set to be 0
CPHA=1: 0x1003FFF4 for phase set to be 1

(calib.-SPI commands for CC32in see also CC32 in section 10.4.2).

The polarity will be determined by the polarity of the Calibration Command.

The following table shows the possible combinations of polarity (CPOL) and phase (CPHA) for an example of 8bit.

F03_586

Combinations of CPOL and CPHA

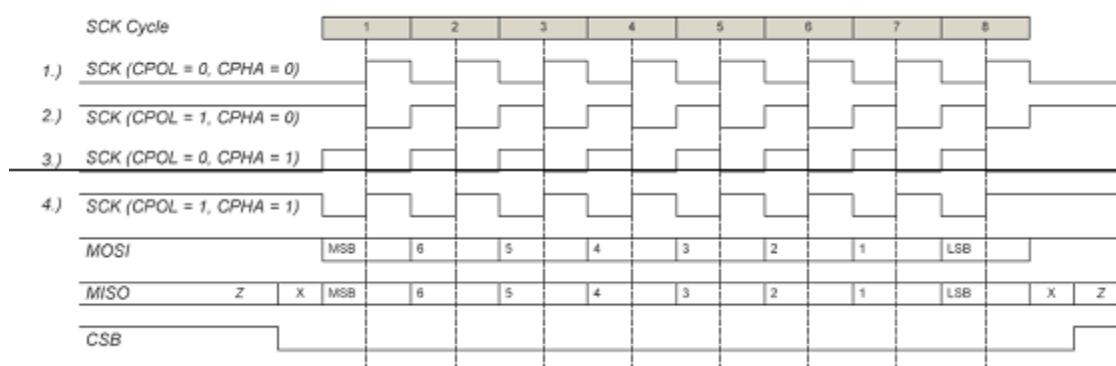


Figure 41: Combinations of CPOL and CPHA



3.10.2.7.3 General instruction format

F03_591 The used SPI instructions can be subdivided into two classes, sensor data and non-sensor/module data commands.

MOSI bits '*' are ignored and MISO bits '*' are undefined (can be '0' or '1').

3.10.2.7.3.1 Sensor Commands

F03_16089 If the bus-address is not a sensor module address (XX000b or XX001b) the sensor interprets the command as sensor channel command. The addressed channel will respond to the command. Capture bits are interpreted from all modules on a chip select line.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6
MOSI						CAP(2:0)		0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
MISO						BADR(4:0)	TE	SD=1	CS	BE	INIT	*	*													DATA(15:0)

Figure 43a: instruction format for sensor commands

F03_594 **Table 50:** Frameset description

CAP(2:0)	Bits to define if captured or current data should be read and if data should be captured 011b: read current data and channel-status (do not alter captured data) 010b: read captured data and channel status (do not capture or alter captured data) 101b: sensor channels of any module on the bus must capture data and channel status of all channels. Only channel which is addressed within BADR feedbacks captured data of selected channel as response to capture command else: reserved (illegal command)
SID=BADR	SID will be set equal for BADR in EOL programming at RB
CS	Channel-Status of requested channel. b'0': channel sensor-data fully valid b'1': channel sensor-data not valid (sensor-error, initialization or self test) if captured data is read, then the CS-bit is the captured CS OR the actual CS
INIT	Initialization Status b'0': Self-Test inactive b'1': Self-Test active
TE	Time-error : APB-bus-acces not finished between 2 SPI-frames 0: no error 1: error
BE	Bus-error : internal Bus error (e.g. read access on the internal failed, parity error on internal bus) 0: no error 1: error
SD	Sensor channel data or module data - 0: module data - 1: sensor data
DATA	Sensor data: 2nd complement sensor data of selected channel
CRCA/R	3 bit CRC; Polynom: x^3+x+1 , start value: 111b, target value 000b. RX-CRC : CRC over bits 31 to 5. TX_CRC : CRC over bits 31 to 3.



3.10.2.7.3.2 Instruction Format Safety Sensor Command

F03_16086

For SMI7-32OUT SPI the sensor features a special response frame for sensor commands.

This frame is activated by setting bit 23 in an sensor request to '1'.

The response frame format is described in the following

MOSI	BADR4 1/0	BADR3 1/0	BADR2 1/0	BADR1 1/0	BADR0 1/0	CAP2 1/0	CAP1 1/0	CAP0 1/0	MOD 1	-	-	-	-	-	-	-
Modul adress data																
MISO	-	-	-	-	-	ST 1	ST 1	D15 1/0	D14 1/0	D13 1/0	D12 1/0	D11 1/0	D10 1/0	D9 1/0	D8 1/0	
	0	0	0	0	-	Status		Channel data								

MOD Selects Safety Sensor command if Bit is set to '1'

ST Status

01b: channel sensor-data fully valid

10b: channel sensor-data not valid (init or selftest)

11b: channel sensor-data not valid (bus-error, wrong command etc.)

3.10.2.7.3.3 Non Sensor/module Commands

F03_16072

Instruction Format Non Sensor Command

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6
MOSI	BADR(4:0)				ADR(3:0)				W	*	WDATA(15:0)															
MISO	BADR(4:0)				TE	SD=0	*	BE	*	PAGE(2:0)		R-DATA(15:0)														

MOSI bits “**” are ignored and MISO bits “**” are undefined (can be “0” or “1”).

F03_596

Table 51: Description of Non Sensor command format bits

ADD	Register-Address : Address of data to be read (relative address within one page)
W	Write data. (Writing to a read only register gives a transfer failure) 0: read data (W-DATA is being interpreted for Offset Address handling) 1: write W-DATA to sensor
WDATA	Data to be written to the sensor. Ignored if W=0 and Bit 20=0
PAGE	Identifies page number (Offset) from which data is read or written to Identifies page number (Offset) from which data is read or written to OFFS = 0x000 corresponds to Page0 OFFS = 0x001 corresponds to Page1 OFFS = 0x002 corresponds to Page2 ... OFFS = 0x007 or higher corresponds to Page7
R-DATA	Data read from sensor. In case of response to a write request the data which should be written is returned.
TE	Time-error : APB-bus-acces not finished between 2 SPI-frames 0: no error 1: error
BE	Bus-error : internal Bus error (e.g. read access on the internal failed, parity error on internal bus) 0: no error 1: error
CRC	3 bit CRC; Polynom: x^3+x+1 , start value: 111b, target value 000b. CRCR: CRC over bits 31 to 5. CRCA: CRC over bits 31 to 3.

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3.10.2.7.4 Addressing Scheme

F03_607

Since only 16 Registers can be accessed with ADR(3:0), a paging mechanism is implemented.

Each page addresses a fixed set of 16 Registers. The pages can be changed by a Read-Command:

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6
MOSI	BADR(4:0)				ADR(3:0)				W=0	*	1	*	*	*	*	*	*	*	*					OFFSET(9:0)		
MISO	BADR(4:0)				TE	SD=0	*	BE	*	PAGE(2:0)				DATA(15:0)												

For Offset values 0...7 the following pages are defined:

For page description see CC32in protocol

Please note: Reading within page, changing to next page/Change to next page: Bit 22 must! be set to '0'. Bit 20 must! be set to '0' for reading within page and set to '1' otherwise. Bits7 to 5 are the offset, e.g. changing to page 1 means bit7 to 5 are: 001. Bits 13:8 must be 0.

3.10.2.7.5 Error handling

F03_609

a) MISO is high impedance for:

- CRC of request (MOSI) was wrong
- SCK-Counter-error : SCK-clocks not equal to 32
- CPOL-error : actual sampled SCK-level not equal to CPOL

Please note: CPHA errors are not detected.

b) unkown command with correct CRC

Case 1): wrong 'CAP' entry → BE bit is set

Case2): wrong BUSADR → high impedance

c) for answers to module command 'WRITE' the 'R-DATA'-field contains the written data

F03_16126

If the interframe delay is smaller than an internal clock cycle the rising edge and falling edge of CSB will not be sampled and the frame will be extended with additional bits. It will be the same behaviour as if the frame has too many clock cycles.

If the CSB is sampled correct but a internal bus transfer is ongoing, that prevents the transfer of valid data, the error bit TE will be set in this frame.

3.10.2.7.6 Programming

F03_2797

The sensor can be programmed within an application to define the application specific behaviour, including

- A) Reset Vector
- B) error counter settings (limit/hold)
- C) Filter flush Zeit
- D) Filter selection LF/HF channels
- E) ACC1/2/rate/quad BITE tolerances
- F) SID settings
- G) Serial number of customer
- H) Activating/deactivating error memory
- I) CRC Checksumme fo all programmed memory sections

3.10.2.8 Master SPI

F03_619

A master SPI function will be implemented, where all protocol functions must be overtaken by the on-chip µC.

3.10.2.8.1 General description

F03_2798

During master SPI operation, the pin "SCLK" is defined as output, the pin "CS_B" is defined as output, the pin "MISO" is used as master output not slave output and the pin "MOSI" is used as master input not output (the pin names "MOSI" and "MISO" refer to SPI slave operation of the SMI).

At all output pins, which performs as input in the slave SPI configuration, the pull resistors are switched off. The pins "CS_B" and "SCLK" are controlled as outputs from the master SPI hardware controller.

This controller generates the transfer from the 32 bit bus register to the shift register, the shifting synchronous to the SCLK, the controlling of SCLK and the control of CS_B.

The phase and polarity of the data can be configured. The shift frequency may be configured to 5 different frequencies. The driver strength of the outputs can also configured to either the 10 MHz strength or 4 MHz strength.

F03_623

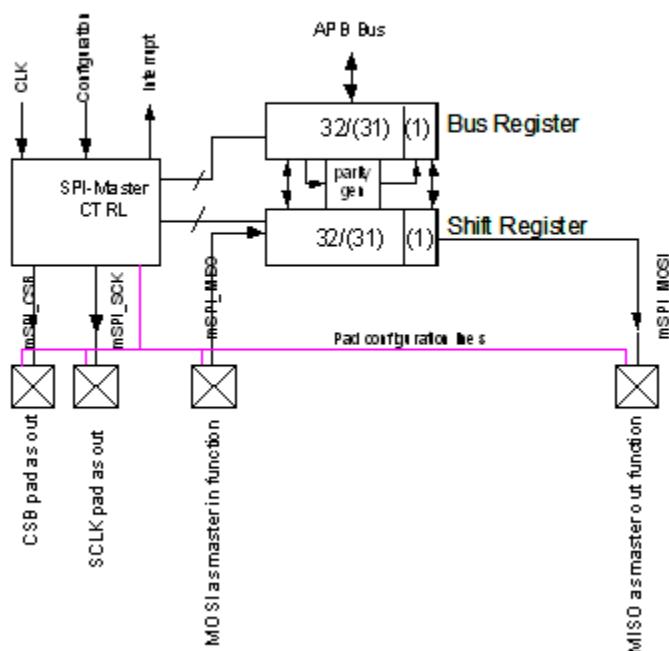


Figure 44: Master-SPI



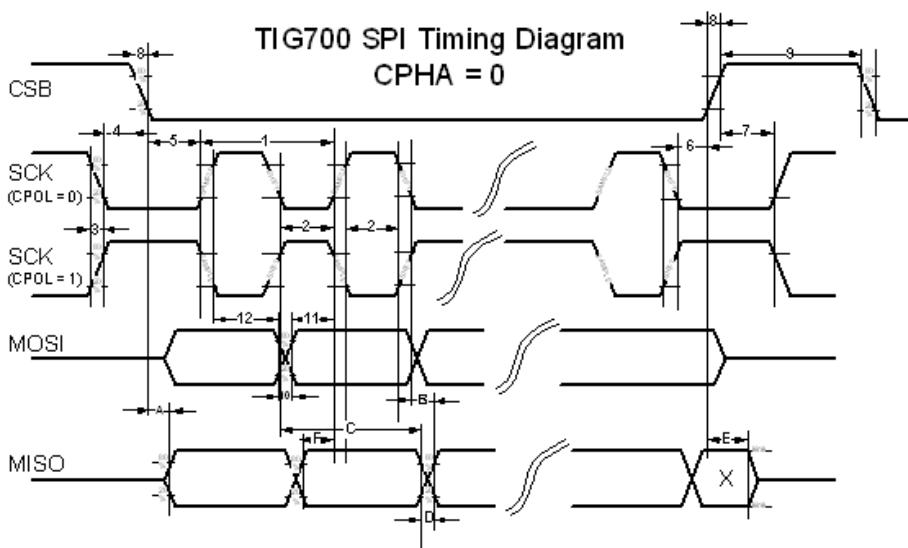
3.10.2.8.2 Timing of master SPI

F03_626

Table 54: Timing of master-SPI

ID	parameter/condition	symbol	min	typ	max	unit	TC
M20_199	SCLK cycle time (1) min. Freq-10%, max. Freq +10%	MSPI_1	142		1038	nsec	
M20_200	SCLK high / low time (2) min. freq-10%, max. Freq +10%	MSPI_2	70		550	nsec	
M20_201	SCLK rise / fall time (3) max. load 35pF	MSPI_3			25	nsec	
M20_202	SCLK enable lead time (5) Max. frequency	MSPI_5	33			nsec	
M20_203	SCLK enable lag time (6) max. frequency	MSPI_6	33			nsec	
M20_204	CSB rise / fall time (8) max. load 35 pF	MSPI_8			25	nsec	
M20_205	MOSI (physically at MISO) rise/fall time (10) max. load 35pF	MSPI_10			25	nsec	
M20_206	MOSI (physically at MISO) data setup time (11) max. frequency	MSPI_11	33		50	nsec	
M20_207	MOSI (physically at MISO) data hold time (12) max. frequency	MSPI_12	33		50	nsec	
M20_209	MISO (physically at MOSI) set up time (F) (shown for rising SCLK, same for falling SCLK) max. frequency	MSPI_F			25	nsec	
M20_210	MISO (physically at MOSI) hold time (G) (shown for rising SCLK, same for falling SCLK) max. frequency	MSPI_G			25	nsec	

F03_628



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3.10.2.8.3 Physical layer

F03_630 The driver capabilities of the pins are described in the chapter "electrical specification" at the appropriate pins. The transfer clock selection will generate the SCLK frequency with a tolerance of +/- 10 % due to limitation of CMG-frequency-tolerances.

F03_631 **Table 55:** SCLK frequencies

Divider	SPI CLK	Unit
4	6.4	MHz
6	4.27	MHz
8	3.2	MHz
12	2.13	MHz
24	1.07	MHz

3.10.2.8.4 Data link layer

F03_634 The length of transferred frame can be selected to 16 / 17 or 32 bits. A hardware parity generator may be used to insert a 17th bit in the 17 bit frame transfer. The transfer is triggered by the µC and the transfer is controlled by the SPI-master control block. After sending the last SCLK phase, the CS_B is going inactive and a interrupt to the µC is generated to indicate the end of transfer. At the beginning of the transfer all 16 /17 or 32 bits according to the configuration are transferred from the bus register to the shift register. At the end of the transfer all 16 /17 or 32 bits according to the configuration are transferred from the shift register to the bus register. No interpretation of the transferred data takes place.

3.10.2.8.5 Bus interface / registers

3.10.3 CAN

F03_637 The CAN interface is used for interconnecting sensor modules with external ECUs. The SMI7xx provides the logical data CAN_TX and CAN_RX. The physical CAN signals CAN_H and CAN_L has to be realized by an external transceiver module.

F03_638

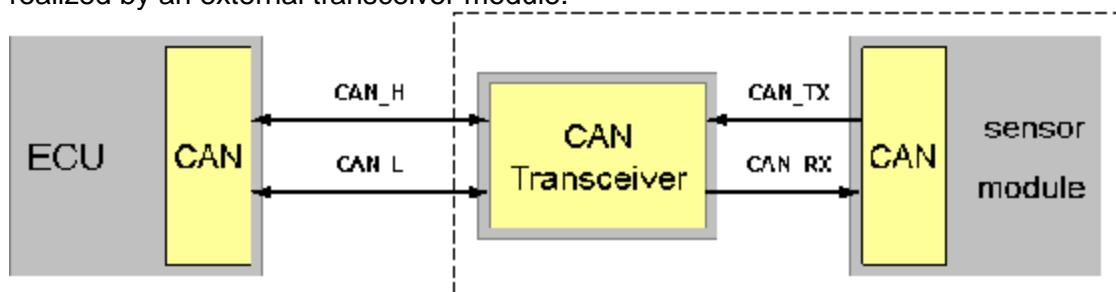


Figure 45: Typical connection between external ECU and sensor modul via. CAN transceiver

F03_2933

The CAN-core used is conforming to ISO16845. A detailed description of this IP module can be found here: [14]

Additional CAN related requirements:

CAN Baud rate configurable up to 1MBaud

32 Message Buffers (if available with self check mechanisms)

Interrupt capability on reception, transmission, error towards µC if available with IR trigger specifically on No Acknowledge occurrence

CAN clock stability < 1/1000

read/write access time of µC to message buffers is < 10 µs / 8 Bytes



Additionally the SMI includes a configurable timer/(down)counter based on CAN clock with following characteristics:

Interrupt capability on timer run off towards µC.

Auto-reload on run-off (to have a stable cyclic trigger for the CAN application protocol logic).

Timer is dynamically configurable (in reload register) by µC with a range of 1 to 2^{14} -1 cycles and a step size of 1 cycle (resulting in a maximum period of ~2s for a 8 MHz CAN clock).

Current Timer value can be read out by µC, e.g. to enable a frequency check of the CAN against the µC clock.

The sensor operates with standard quartz as resonator. It is possible (will be confirmed) to use the resonators specified in:

c_NX5032GA-STD-CSU-2_e.pdf

cx5032ga_at_e.pdf

15073v1.pdf

3.10.3.1 General / D-CAN

F03_2934

The D_CAN is a CAN IP module that can be integrated as stand-alone device or as part of an SoC or ASIC. It is described in VHDL on RTL level, prepared for synthesis. It consists of the components (see figure 1) Mux, CAN_Core, Message RAM interface, Message handler, registers and message Object (MO) access, module interface. The D_CAN performs CAN protocol communication according to ISO 11898-1 (identical to Bosch CAN protocol specification 2.0 A, B). The bit rate can be programmed to values up to 1 MBit/s depending on the used technology. Additional transceiver hardware is required for the connection to the physical layer (the CAN bus line). For communication on a CAN network, individual message objects are configured. The message objects and identifier masks are stored in the message RAM.

All functions concerning the handling of messages are implemented in the message handler. Those functions are acceptance filtering, transfer of messages between the CAN_Core and the message RAM, and the handle of transmission requests as well as the generation of the module interrupts.

The register set of the D_CAN can be accessed directly by an external CPU via the module host interface. These registers are used to control/configure the CAN_Core and the message handler and to access the message RAM via the IF1 and IF2 register sets.

Features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- Dual clock source, enabling FM-PLL designs
- 16, 32, 64 or 128 message objects (configurable during synthesis)
- Each message object has its own identifier mask
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Parity check mechanism for all RAM modules (optional)
- 2 Interrupt lines
- DMA support with automatic message object increment
- Power-down support
- RAM initialization

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Block diagram of D-CAN:

F03_675

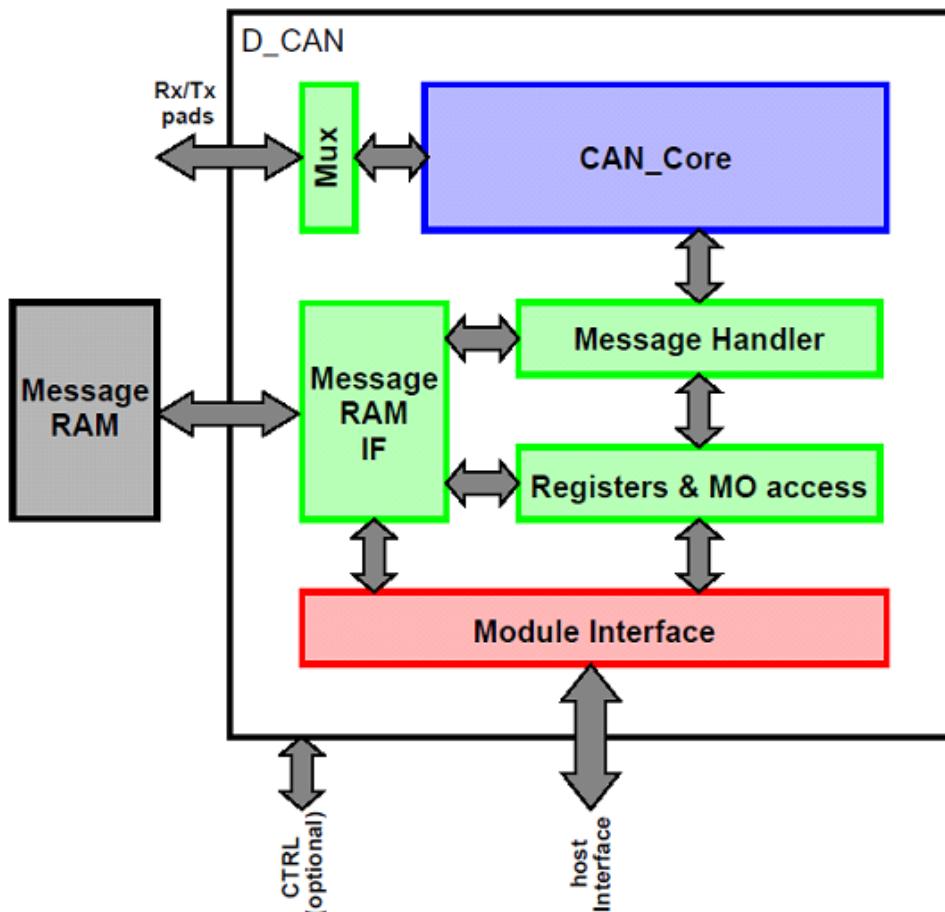


Figure 46: D-CAN block Diagram

F03_676

CAN protocol controller and Rx/Tx shift register, handles all ISO 11898-1 protocol functions.

3.10.3.2 Bus interface / registers

F03_2935

MUX:

This multiplexer controls the functionality of the two CAN ports, that is:

- transmit & receive lines for normal CAN communication
- configurable self test features, when test mode is enabled

F03_2936

Message handler:

State machine that controls the data transfer between the single ported message RAM and the CAN Core's Rx/Tx shift register. It also handles acceptance filtering and the interrupt setting as programmed in the control and configuration registers.

F03_2937

Register and MO access:

Status and configuration registers for module setup and indirect message object (MO) access to ensure data consistency; all CPU accesses to the message RAM are relayed through CPU IFC registers that have the same word-length as the message RAM.

F03_2938

Module Interface:

The D_CAN module is equipped with a generic 32-bit interface. The customer specific interface is a wrapper one hierarchy level higher, implementing a "generic interface" to "host interface" bridge.

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The D_CAN module allocates an address space of 512 Bytes for the D_CAN registers. Data is accessible by host interface using a data width of 8 bit (byte access), 16 bit (halfword access) and 32 bit (word access). The two sets of interface registers (IF1 and IF2) providing an indirect read-and write-access for the host CPU to the message RAM. They buffer the data to be transferred to and from the RAM, avoiding conflicts between CPU accesses and CAN frame reception/ transmission.

F03_690

Table 56: Register table I

Address	Symbol	Name	Page	Reset	Acc
CAN Status and Configuration Registers					
0x000	CCTRL	CAN Control Register	17	0000 0001	r/w
0x004	CSTS	CAN Status Register	19	0000 0007	r
0x008	CERC	CAN Error Counter Register	21	0000 0000	r
0x00C	CBT	CAN Bit Timing Register	22	0000 2301	r/w
0x010	CIR	CAN Interrupt Register	43	0000 0000	r
0x014	CTR	CAN TEst Register	23	0000 0080 ¹	r/w
0x0018	CFR	CAN Function Register	24	0000 0000	r/w
0x01C	PEC	CAN Parity Error Counter Register	26	0000 UUUU ²	r
0x020	CRR	CAN Core Relase Register	27	100S SSS ³	r
0x024	HWS	CAN Hardware Configuration Status	28	0000 000S	r
0x028 - 0x080		reserved for future use		0000 0000	r
CAN Message Object Status Registers					
0x084	MOTRX	MO Transmission Request X Register	38	0000 0000	r
0x088	MOTRA	MO Transmission Request A Register	37	0000 0000	r
0x08C	MOTRB	MO Transmission Request B Register	37	0000 0000	r
0x090	MOTRC	MO Transmission Request C Register	37	0000 0000	r
0x094	MOTRD	MO Transmission Request D Register	39	0000 0000	r
0x098	MONDX	MO New Data X Register	39	0000 0000	r
0x09C	MONDA	MO New Data A Register	38	0000 0000	r
0x0A0	MONDB	MO New Data B Register	38	0000 0000	r
0x0A4	MONDC	MO New Data C Register	38	0000 0000	r
0x0A8	MONDD	MO New Data D Register	38	0000 0000	r
0x0AC	MOIPX	MO Interrupt Pending X Register	41	0000 0000	r
0x0B0	MOIPA	MO Interrupt Pending A Register	40	0000 0000	r
0x0B4	MOIPB	MO Interrupt Pending B Register	40	0000 0000	r
0x0B8	MOIPC	MO Interrupt Pending C Register	40	0000 0000	r
0x0BC	MOIPD	MO Interrupt Pending D Register	40	0000 0000	r
0x0C0	MOVALX	MO Message Valid X Register	42	0000 0000	r
0x0C4	MOVALA	MO Message Valid A Register	41	0000 0000	r
0x0C8	MOVALB	MO Message Valid B Register	41	0000 0000	r

F03_2940

Table 57: Register table II

Adress	Symbol	Name	Page	Reset	Acc
0x0CC	MOVALC	MO Message Valid C Register	41	0000 0000	r
0x0D0	MOVALD	MO Message Valid D Register	41	0000 0000	r
0x0D4 - 0x0FC		reserved for future use		0000 0000	r
CAN application Interface Registers					
0x100	IF1CMR	IF1 Command Register	30	0000 0001	r/w

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0x104	IF1MSK	IF1 Mask Register	34	FFFF FFFF	r/w
0x108	IF1ARB	IF1 Arbitration Register	34	0000 0000	r/w
0x10C	IFMCTR	IF1 Message Control Register	35	0000 0000	r/w
0x110	IF1DA	IF1 Data A Register	36	0000 0000	r/w
0x114	IF1DB	IF1 Data B Register	36	0000 0000	r/w
0x118 - 0x11C		reserved for future use		0000 0000	r
0x120	IF2CMR	IF2 Command Register	30	0000 0001	r/w
0x124	IF2MSK	IF2 Mask Register	34	FFFF FFFF	r/w
0x128	IF2ARB	IF2 Arbitration Register	34	0000 0000	r/w
0x12C	IF2MCTR	IF2 Message Control Register	35	0000 0000	r/w
0x130	IF2DA	IF2 Data A Register	36	0000 0000	r/w
0x134	IF2DB	IF2 Data B Register	36	0000 0000	r/w
0x138 - 0x1FC		reserved for future use		0000 0000	r

F03_2941

Interrupt handling:

The D_CAN provides three groups of interrupt sources, these are:

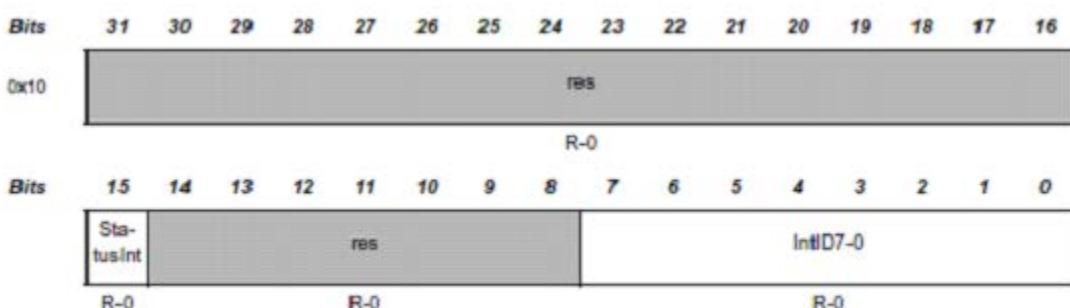
Error iuninterrupts are generated by bits PER, BOff and EWarn monitored in status register, see chapter {in F02 chapter 1.2.2 -> does not exist}. This error interrupt group will be enabled by setting bit EIE which is located in CAN control register.

RxOk, TxOk and LEC belong to the status interrupt group and can be enabled by SIE bit which is located in CAN Control Register.

The message object interrupts, which are generated by events concerning the message object itself controlled by flags IntPND, TxIE and RxIE.

Error and status interrupts can only be routed to interrupt port CAN_INT_STATUS which has to be enabled by setting CCTRL.ILE. The message object interrupts can be routed to interrupt port CAN_INT_STATUS or CAN_INT_MO controlled by CCTRL.MIL. Setting CCTRL.MIL to one, a message object interrupt will set the port CAN_INT_MO to one.

F03_698



R = Read, W = Write, U = Undefined; -r = Value after reset

Figure 47: Interruptregister

F03_2942

Message RAM:

Single ported RAM, word-length = [CAN message & acceptance filter mask & control bits & status bits] 136 bits + 5 bits parity (optional).Message RAM will be 32x141 Bits.

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3.10.4 PSI5 interface

F03_702 The PSI interface is used for interconnecting sensor modules with external ECUs. This 2-wire interface supplies the sensor module with electrical power and carries the information sent by the sensor module. The information is transmitted by a current modulation using manchester coding.

F03_16186 Sensorinterface according PSI5 V2.1 except Base Specification chapter 6.2 Sensor Power-on Characteristics (settling time > 10ms; in discussion) and Substandard Airbag chapter 6.4 Data Transmission Parameters (Sensor clock deviation during data frame 1%; accepted).

F03_703

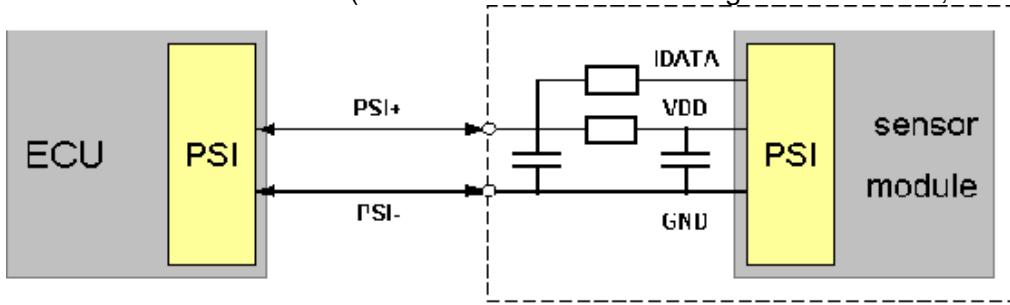


Figure 48: Typical connection between external ECU and one sensor module

F03_705 There is an asynchronous as well as a synchronous mode. In the asynchronous mode the sensor module continuously sends its information. The synchronous mode is characterized by a sync pulse sent by the ECU in order to start one communication sequence called sync period. This sync pulse is represented by a voltage pulse.

F03_706

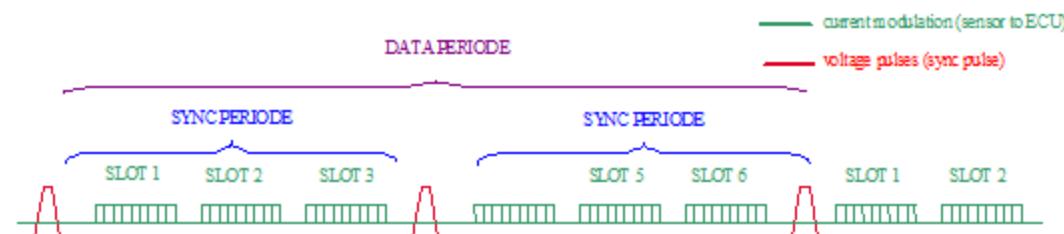


Figure 49: PSI-communication with sync.-pulse

3.10.4.1 Physical layer

F03_708 The following table shows parameters of sync.-pulse, current pulses and message telegrams.

Table 58: Parameters of sync.-pulse, current pulses, message telegrams

Parameter	Condition/Remark	Min	Nominal	Max	Unit
Supply voltage	V_{SS}	5.0		11.0	V
Supply voltage (standard voltage)	V_{CE}	5.5		11.0	V
Supply voltage (increased voltage)	V_{CE}	6.5		11.0	V
Interface quiescent current (standard current)	I_{LOW}	4.0		19.0	mA
Interface quiescent current (extended current)	I_{LOW}	4.0		35.0	mA
Drift of quiescent current		-4.0		4.0	mA
Quiescent current, drift rate				1.0	mA/s
ECU current limitation (standard current)	I_{LIMIT} $I_{LIMIT, dynamic}$	50.0 65.0		105	mA mA
ECU current limitation (extended current)	I_{LIMIT} $I_{LIMIT, dynamic}$	65.0 80.0		130	mA mA

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3.10.4.2 Data link layer

F03_3012

The SMI7xy will support asynchronous and synchronous communication. For the normal application only unidirectional communication is required. For configuration and failure analysis a bidirectional communication as described in the PSI5 specification will be provided.

The timing of the PSI interface is derived from the mechanical resonance frequency of the yaw-rate sensor. A PLL transposes this drive frequency up to 1024 times the drive frequency. The absolute value is measured during production test and an appropriate calibration value is programmed into the non volatile part of the on-chip memory (OTP).

If any disturbances (mechanical shocks) force the PLL of the clock generation to unlock, the frequency shift of the PLL is limited to narrow range - see 4.2.

The SMI7 allows the following features in hardware:

High speed (189kHz) and low speed (125kHz) PSI5 communication.

Frame width can be selected from 10 to 26 bits (excluding start bits and/or parity/CRC) in 1 bit steps configurable for each single slot individually.

All frames are configurable to parity or CRC checksums as defined by PSI5; calculations done in HW. The HW CRC/parity mechanisms can be disabled. In this case CRC/parity needs to be included within the data register of the specific slot.

Sync.-periods will have a nominal timing of 500 µs or 1000 µs. Different sync.-periods possible.

Each sync.-period may have 0 to 6 transmission slots.

Each slot is configurable to nominal start timing between 0 and 1000 µs with a 0.5 µs nominal resolution.

All timings of the PSI5 communication (bit width, slot starts ...) have an absolute precision of 1% if and only if the correction value is used.

Configurable half bit time with a resolution of one system clock cycle and a maximum of 127 cycles (range includes high speed (189kHz) and low speed (125kHz) PSI5 communication)

Configurable time windows for bidir sync.-pulse detection, allowing to reduce the standard 500us periode and enable faster communication from ECU to ASIC.

Special requirement to the SMI7xy µC system to implement the PSI5 protocol and application layer in SW that are fulfilled:

An interrupt is set on reception of a sync.-pulse. If a sync.-pulse is detected, all sync.-pulse timers will restart.

An interrupt is set on reception of a valid Bidir XLong Frame (Stuffing bits checked in hardware). This interrupt can occur at any time, not only during Init Phase II as described in the PSI5 specification.

An interrupt is set on reception sync.-pulse if the minimum (configurable) time gap with respect to the previous sync.-pulse is violated. The sync.-cycle duration is configurable between 0 µs and 1100 µs with a resolution of 0.5 µs. Setting the duration time to 0 µs this feature is turned off so that all sync.-pulses are detected.



An interrupt is set if the maximum (configurable) time gap with respect to the previous sync.-pulse is violated. The duration is configurable between 0 µs and 1100 µs with a resolution of 0.5 µs. Setting the duration time to 0 µs this feature is turned off.

An interrupt is set if an arbitrary, configurable time span is reached (e.g. used as presync.- warning). The duration is configurable between 0 µs and 1100 µs with a resolution of 0.5 µs. Setting the duration time to 0 µs this feature is turned off.

The interrupt PSI_async_periode_end is issued for one clock cycle once the time counter value equals the register PSI_async_cycle. The interrupt is disabled, if synchronous communication is selected or if the PSI.PSI_async_cycle is set to zero.

6 output registers are provided to be filled by the µC.

These output registers are automatically shifted out by HW as data slots depending on configuration of timing, bit width and checksum.

Timer functionality with a range from 0 to 1000 µs and a resolution of at least 0.5 µs is provided to realize an asynchronous and synchronous protocol.

A minimum sync cycle duration between 0 µs and 1100 µs is configurable with a resolution of 0.5 µs. If a sync pulse would be detected within this minimum sync cycle, it is ignored, but signaled to the µC. Setting the duration time to 0 µs this feature is turned off so that all sync.-pulses are detected.

Two bytes are available to read out the CAN/PSI5 SW version by SPI.

The internal time counter that records the elapsed clock cycles since the last valid sync.-pulse can be read out by a register.

3.10.4.2.1.1 Description of Interrupts

F03_16206 This is a compilation of the SW documentation, where also diagrams can be found [23].

All data that will be transmitted through psi lines have to be written to the psi output registers during interrupts. For synchronous mode the Psi_SyncRcvd_Handler is used, for asynchronous mode the Psi_AsyncPrdEnd_Handler is used. Therefore the PSI Application can be called interrupt-driven.

During initialisation the interrupts regarding of the psi application needs will be activated or deactivated.

All Interrupts can be redirected to otp routines.

PreSync Warning

A special timer value triggers an interrupt which shows that the sync pulse is going to appear soon (realized through a compare register). This feature can be used to catch the signal data earlier because of timing needs. It is recommended to use this interrupt for OTP application SW.

Sync too late

The register PSI_timer_sync_late holds a compare value more than usually a sync periode duration takes. If the PSI timer reaches this compare value this triggers a sync to late interrupt. If this interrupt is activated, during init the compare value must be written to the PSI_timer_sync_late register.



The PSI module hardware does not react on this interrupt. The application react in the case that an error is detected and the active flags are set to zero and the data valid bit is cleared.

Sync too early

This interrupt shows that the last sync pulse has appeared too early, means inside of a sync period (realized through a compare register). The PSI module hardware reports this through its interrupt to the application but does not react in any case. Also the sync interrupt is triggered. The application can use this interrupt for error monitoring. For instance in case a sync pulse appeared then first the sync too early interrupt is triggered because of an higher priority of the sync too early interrupt. The sync too early handler routine acts in the kind that the sync interrupt is disabled and the sync too early interrupt too for the rest of the main cycle. With the next main cycle both interrupts are enabled again.

For A- and B- Silicon this interrupt has not been used in psi application.

For CA-Silicon this interrupt will be used together with the sync interrupt to prepare an interrupt overload prevention mechanism. Therefore the interrupt is enabled in every synchronous CUSTOMER mode and in the SLOW and FAST BIDIR mode. The default value in ROM for the timer register is 450 us.

Synchronous Interrupt

In synchronous PSI communication mode with every sync pulse from the ECU a sync interrupt will be generated. The whole PSI application in synchronous mode runs in this ISR. Also in asynchronous PSI mode it is possible to get a sync interrupt when the interrupt is not deactivated. This interrupt is maskable.

Asynchronous Interrupt (Timer Interrupt)

During asynchronous data transmission with every new transmit period a timer interrupt is generated. This means the PSI timer will be set back to zero and starts counting again. For the asynchronous mode this is the trigger to get new signal data and prepare the slots with the values.

In case of asynchronous psi mode this interrupt will be called with every expired async period.

BiDir

The BiDir interrupt shows that a new complete, syntactically correct bidir frame has been received. The start field and the stuffing bits are checked in the hw module and then skipped.

The Psi_task polls the interrupt pending flag every main cycle. In case a pending flag is present, the value is taken from the PSI_BiDir_frame register which holds this XLONG frame (without stuff bits and start bits but with CRC). Then the pending flag is cleared by SW.



3.10.4.3 Bus interface / registers

F03_739

Table 59: Bus interface register

according to /TIG700/PH/20_Interface_description/M20_192

register name	bit width	meaning	read/write
PSI_tx_counter	16	Timer for TX communication	r
PSI_half_bit_time	8	no of clks for half bit time	w/r
PSI_tx_data_1	29	data to send	w/r
PSI_tx_data_2	29	data to send	w/r
PSI_tx_data_3	29	data to send	w/r
PSI_tx_data_4	29	data to send	w/r
PSI_tx_data_5	29	data to send	w/r
PSI_tx_data_6	29	data to send	w/r
PSI_data_length_1	5	data length for slot 1	w/r
PSI_data_length_2	5	data length for slot 2	w/r
PSI_data_length_3	5	data length for slot 3	w/r
PSI_data_length_4	5	data length for slot 4	w/r
PSI_data_length_5	5	data length for slot 5	w/r
PSI_data_length_6	5	data length for slot 6	w/r
PSI_slot_active	6	activates slot	w/r
PSI_crcParity	2	bit1 for crc or parity, bit0 if to compute	w/r
PSI_timer_slot_1	16	frame start time 1	w/r
PSI_timer_slot_2	16	frame start time 2	w/r
PSI_timer_slot_3	16	frame start time 3	w/r
PSI_timer_slot_4	16	frame start time 4	w/r
PSI_timer_slot_5	16	frame start time 5	w/r
PSI_timer_slot_6	16	frame start time 6	w/r
PSI_timer_sync_early	16	interrupt if sync-pulse and counter not reached	w/r
PSI_timer_sync_late	16	interrupt if no sync-pulse	w/r
PSI_timer_pre_sync	16	interrupt if timer value has been reached	w/r
PSI_sync_window_min_1	18	window for 1st sync-pulse	w/r
PSI_sync_window_max_1	18	window for 1st sync-pulse	w/r
PSI_sync_window_min_2	18	window for 2nd sync-pulse	w/r
PSI_sync_window_max_2	18	window for 2nd sync-pulse	w/r
PSI_sync_window_min_3	18	window for 3rd sync-pulse	w/r
PSI_sync_window_max_3	18	window for 3rd sync-pulse	w/r
PSI_sync_window_min_4	18	window for 4th sync-pulse	w/r
PSI_sync_window_max_4	18	window for 4th sync-pulse	w/r
PSI_BiDir_frame_including_CR	25	received PSI-BiDir-Frame	r
PSI_async_cycle	16	cycle time for one asynchronous periode	w/r
PSI_mode	1	Synchronous/asynchronous PSI mode	w/r
PSI_timer_enable	1	Enable/disable psi timer	w/r
PSI_rx_counter	16	Timer for RX communication (BiDir)	r

F03_3184

⁶ Counter frequency is 1024 times the drive frequency.

The start bits and the stuffing bit of the ECU to sensor protocol are checked and removed by hardware. If a valid XLong Frame has been received, an interrupt PSI_irq_bidir_rcvd is issued for one clock cycle.

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F03_3185 PSI_tx_counter is the timer value of the tx (sensor to ECU) communication, used for asynchronous and synchronous communication.

The timer is a free running counter that is clocked with the fastest internal system clock. It is reset by different conditions in synchronous and asynchronous mode, eg. a change between asynchronous and synchronous mode. If the asynchronous mode is selected and the PSI_counter equals the value of PSI_async_cycle, the PSI_counter will be reset and will start again at zero.

If the defined reset condition is not reached the timer stops at its maximum value.

If the timer is not enabled, it has a constant value of zero in asynchronous mode. In synchronous mode, the timer has a constant value of 0xFFFF when it is not enabled.

PSI_rx_counter is the timer value of the rx (ECU to sensor) communication, used for bidirectional mode. This timer is reset by a valid sync pulse and indicates how many clock cycles elapsed since the last bit that was part of a bidirectional message and had a value of '1'. Timer is always active and cannot be stop manually.

If the sensor has lost synchronization with the ECU, the counter is set to its maximum value.

PSI_timer_enable:

Bit 0: '1' = The PSI timer for synchronous and asynchronous communication is enable. Timer is set and reset internally.

Bit 0: '0' = The PSI timer for synchronous and asynchronous communication is disable. The Timer is reset and held to zero if no slot is in process of being send or as soon as an ongoing slot has been finished.

Active flag has to be set before a specific slot can be send. After a slot has been completely send the corresponding bit in the register PSI_slot_active will be cleared (set to '0') by the PSI module.

During sending a frame will always be sent completely due to triggering of the send start only due to timer.

3.10.4.4 PSI5 timing

F03_747 Overall start-up timing is as follows:

F03_748 **Table 60:** Overall start-up timing

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Start-up time - Communication full functional SPI and CAN communication is available earlier	PSI_T_START			200	ms
Sensor full functional after start-up time, including all BIST PSI_T_START + PSI_T_READY	PSI_T_READY			450	ms

F03_3208 Note, early communication may happen and may not lead to illegal conditions or misleading. However the sensor may not respond or respond in a defined error state. This corresponds to the PSI5 initialization phases 1 to 3:

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F03_750

Table 61: PSI initialization phases

Parameter / Condition	Symbol	Min	Typ	Max	Unit
PSI Init phase 1 duration (Phase 1: No Communication)	PSI_PH1	150		200	ms
PSI phase 2 transmittal of mandatory and optional static information, duration depends on application, given values are for example applications	PSI_PH2	60	64 - 116	120	ms
Phase 3 - end of init phase, either data with status invalid are sent (default) or a dedicated sensor status is sent	PSI_PH3		2		ms

F03_3238

The most critical time specification due to the constant of the main clock is defined by the mode of 189kps, 20 Bit per frame data, 3 CRC bits and 3 frames per sync.-period. With these timing constraints the following bit time, gap time and time per frames can be realized:

3.10.4.4.1.1.1 Duration of PSI phase 2

F03_16221 Sync Mode PSI5-P20CRC-500 with 4 repetitions

typ. 64 ms

Async Mode PSI5-A20CRC-300/1L with 3 signals and 4 repetitions

typ. 116 ms

F03_752 **Table 62:** Bit time, gap time and time per frames which can be realized

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Bit time (189 kbps mode)	PSI_T_BIT	5,246		5,355	µs
Time per frame	PSI_T_FRAME	131,149		133,879	µs
Gap time (189 kbps mode)	PSI_T_GAP	5,6			µs
Sensor clock deviation during data frame				0,1	%
Maximum clock drift rate				1	%/s
Mark/Space ratio (as defined in PSI5 specification)		47		53	%
Start of first sensor data word	PSI_T_SLOT1	44			µs

F03_3261

These times are theoretically calculated worst case timings.

3.10.4.5 Init Phase

F03_13534 *ID : SMI7_RS_PSI5_206*

There are 3 init phases defined in the PSI5 specification.

ID : SMI7_RS_PSI5_207

During the first init phase no PSI frames should be send.

ID : SMI7_RS_PSI5_208

During the second init phase one page with 16 nibble and additional data in the request and response message should be send.

ID : SMI7_RS_PSI5_209

The repeat time of every data pair should be 4.

ID : SMI7_RS_PSI5_210

During the third init phase at least two messages with signal data marked with status flag invalid should be send .

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ID : SMI7_RS_PSI5_211

After the SMI has finished the initialization and power on safety checks at the end of init phase 3 the signal values switch to valid.

ID : SMI7_RS_PSI5_212

If an error was detected inside of the SMI during initialization the status flag inside of the message stays to invalid or the sensor will switch off the psi communication regarding to the error.

ID : SMI7_RS_PSI5_437

Every slot has it's own init phase.

3.10.4.5.1.1 *Init Phase 1*

F03_16211 During this phase the sensor transmits no data to the ECU and ignores BIDIR frames. The sensor element needs 150 ms (with 1 % Tclock tolerance) to lock the PLL for the accurate timing inside of the PSI5 module, so the Initialization Phase I takes 150 ms.

A SW timer is configured to count 150 ms down. A routine which configures the timer is named Rom_Psi_Configure_Timer_for_Initphase. The timer value is hard coded and so not configurable. But because of the routine is called during the Rom_Psi_Config_v routine, the time for the bootloading and all other previous init routines has to be added to calculate the final psi init phase I time. The bootloading time depends on the number of tuples which will be loaded.

When the sw timer for init phase I reached 0, the pll state will be checked. Only in case of the timer is expired **and** the init_ready flag is set, the psi state machine switches to Psi_Init_2 phase.

If the init_ready flag is not identical to 1, the psi state machine sticks in psi init phase I.

3.10.4.5.1.2 *Init Phase 2*

F03_16213 **Data sent in Initialisation Phase 2**

Following table gives the initialisation phase. Slots Data which are marked with otp have to be customer configurable via configuration services. OTP space reserved for PSI5/CAN applications can be used therefore (300Bytes).

The data transmitted during psi init phase II can vary depending on the psi application and sensor application. Until 4 slots can be configured. The default rom configuration is described below.

The init table contains 16 blocks of 4 bits. This data should be read from the data OTP and put to the PSI send slots. Every slot has it's individual initialization. The first slot holds the ID1 for the first signal; the second slot holds the ID1 for the second signal; the third slot holds the ID1 for the third signal. In the next sync period slot 1 holds data for ID 1, slot 2 holds data for ID1 of the second signal and slot 3 holds data for ID1 for the third signal. This will be repeated the number of iteration times taken from the Data OTP configuration area as well.

Single part number can be found in the OTP and is programmed during module or part production.

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Field	Status Data	ID	Description	Value Data Nibble (D13 .. D10)	Binary Data Nibble (D13 .. D10)	Value Additional Init as Serial Number	Additional Init Range (D9 .. D4)
Page 1							
Mandatory data	F1	Data1	0x200	Protocol revision	Psi5 2.0 (Data Range Initialization) - fixed -	0110	ID: Single part number High Nibble (Byte 0) DATA: Single part Low Nibble (Byte 0)
		Data2	0x201	Number of data blocks (bit 7 – 4)	16blocks - fixed -	0000	ID: Single part number High Nibble (Byte 1) DATA: Single part Low Nibble (Byte 1)
	F2	Data3	0x202	Number of data blocks (bit 3 – 0)		0010	ID: Single part number High Nibble (Byte 2) DATA: Single part Low Nibble (Byte 2)
		Data4	0x203	Vendor ID (bit 7 – 4)	Bosch - fixed -	0100	ID: Single part number High Nibble (Byte 3) DATA: Single part Low Nibble (Byte 3)
	F3	Data5	0x204	Vendor ID (bit 3 – 0)		0010	ID: Single part number High Nibble (Byte 4) DATA: Single part Low Nibble (Byte 4)
		Data6	0x205	Sensor type (bit 7 – 4)	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 5) DATA: Single part Low Nibble (Byte 5)
	F4	Data7	0x206	Sensor type (3 - 0)	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 6) DATA: Single part Low Nibble (Byte 6)
		Data8	0x207	Sensor parameter (axis)	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 7) DATA: Single part Low Nibble (Byte 7)
	F5	Data9	0x208	Sensor parameter (range)	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 8) DATA: Single part Low Nibble (Byte 8)
		Data10	0x209	Customer configurable, i.e. Specific sensor code manufacturer	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 9) DATA: Single part Low Nibble (Byte 9)
Optional product ID	F6	Data11	0x20A	Customer configurable, i.e. Specific sensor code manufacturer	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 10) DATA: Single part Low Nibble (Byte 10)
		Data12	0x20B	Customer configurable, i.e. Sensor code customer	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 11) DATA: Single part Low Nibble (Byte 11)
	F7	Data13	0x20C	Customer configurable, i.e. Sensor code customer	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 12) DATA: Single part Low Nibble (Byte 12)
		Data14	0x20D	Customer configurable, i.e. Sensor code customer	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 13) DATA: Single part Low Nibble (Byte 13)
	F8	Data15	0x20E	Customer configurable, i.e. PSI5 SW implementation number	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	ID: Single part number High Nibble (Byte 14) DATA: Single part Low Nibble (Byte 14)
		Data16	0x20F	Customer configurable, i.e. PSI5 SW implementation number	Slot 1: otp Slot 2: otp Slot 3: otp	xxxx xxxx xxxx xxxx	Reserved (Zeros will be send.)

[Every slot should be configured through otp or the default rom values will be send.
 Single part number must be a unique number compared to MM7 part number.
 Additional Data Range Is zero for the default rom variant
 Default value for xxxx is zero.

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Table 1 - Data Content in Init Phase 2

3.10.4.5.1.3 Default Configuration of Init Phase 2

F03_16217

ID	Description	Value	Binary
Page 1			
Data1	0x200 Protocol revision	Version 2.0	0110
Data2	0x201 Number of data blocks (bit 7 – 4)	16 blocks	0001
Data3	0x202 Number of data blocks (bit 3 – 0)		0000
Data4	0x203 Vendor ID (bit 7 – 4)	Bosch	0100
Data5	0x204 Vendor ID (bit 3 – 0)		0010
Data6	0x205 Sensor type (bit 7 – 4)	See def. below	xxxx
Data7	0x206 Sensor type (bit 3 – 0)	See def. below	xxxx
Data8	0x207 Sensor parameter (axis)	See def. below	xxxx
Data9	0x208 Sensor parameter (range)	See def. below	xxxx
Data10	0x209 Specific sensor code manufacturer (bit 7 – 4) MM7 sensor '7X'		0111
Data11	0x20A Specific sensor code manufacturer (bit 3 – 0)		xxxx
Data12	0x20B Sensor code customer (bit 11 – 8)	ROM SW Revision ID	xxxx
Data13	0x20C Sensor code customer (bit 7 – 4)	Config.ID for Data OTP	xxxx
Data14	0x20D Sensor code customer (bit 3 – 0)	Config. ID for Data OTP	xxxx
Data15	0x20E reserved	reserved	0000
Data16	0x20F reserved		0000

Legend

Fix

Slot individual

Sensor individual

ROM SW Version specific

OTP configuration specific

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Signal Information

Status Data	Slot 1	Slot 2	Slot 3
Data6	0x1 (timeslot 1)	0x2 (timeslot 2)	0x3 (timeslot 3)
Data7	0xA (omega z)	0x2 (low g: ax)	0x3 (low g: ay)
Data8	0x4 (z-axis)	0x0 (x-axis)	0x2 (y-axis)
Data9	0x5 (100°/s)	0x3 (4.6g)	0x3 (4.6g)

SC type

- One SMI module = MM7.8 = 0111 0001
- Two SMI modules = MM7.11 = 0111 0010
- One SMI module and one SMA module = MM7.30 = 0111 0011

Configuration specific data

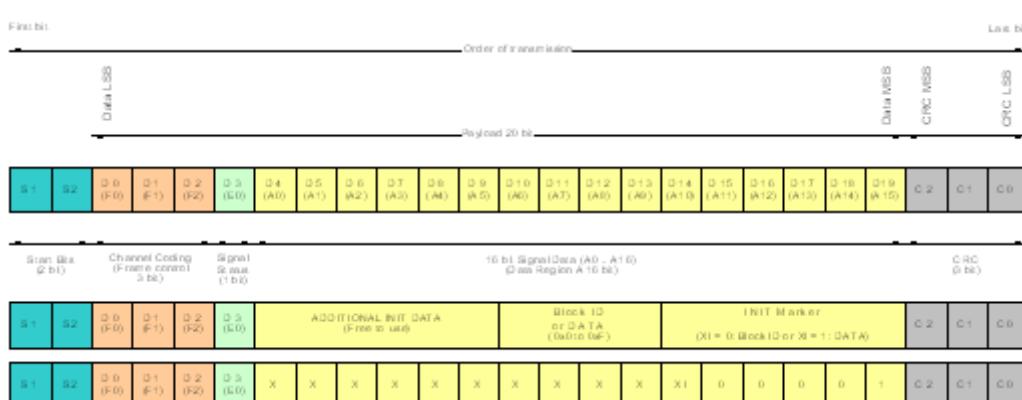
- ROM SW Version 0xAA = 0
- ROM SW Version 0xAB = 1
- ROM SW Version 0xBB = 2
- ROM SW Version 0xCA = 3

For every data OTP configuration an individual number will be assigned

- ROM default (no Data OTP configuration) = 0x00
- Data OTP default MM7.8 configuration = 0x01

Repetition rate : typically 4 (in ROM), maximal 15 -> 4 bit for repetition rate necessary

Frame definition during init phase 2 is shown in the picture below:



F03_13539 Single Part Number Mapping

The PSI5 serial number equals the SMI7 120bit unique part serial number as given in SMI7 Datasheet 3.0, 2.1.3.2, Table 4. The mapping has to be as followed:



Byte 14		Byte 13		Byte 12	
High Nibble	Low Nibble	High Nibble	Low Nibble	High Nibble	Low Nibble
ASIC S/N					
Byte 11		Byte 10		Byte 9	
High Nibble	Low Nibble	High Nibble	Low Nibble	High Nibble	Low Nibble
ASIC S/N					
Byte 8		Byte 7		Byte 6	
High Nibble	Low Nibble	High Nibble	Low Nibble	High Nibble	Low Nibble
HW/SW Level					
Byte 5		Byte 4		Byte 3	
High Nibble	Low Nibble	High Nibble	Low Nibble	High Nibble	Low Nibble
Module S/N					
Byte 2		Byte 1		Byte 0	
High Nibble	Low Nibble	High Nibble	Low Nibble	High Nibble	Low Nibble
Customer S/N					

Table 2 - Layout for Single Part Number

3.10.4.5.1.4 Init Phase 3

F03_16214 After init phase II is finished the sensor transmits sensor signals with status invalid until the internal safety checks are done. If the status of the signals inside of the dsp switches to valid the overall initialization phase is over.

The time for the init phase 3 is configurable. Default is 2 ms and at least two periods of data with status invalid.

It is also possible to configure the message during this phase to a data range status/error value, for instance 'Sensor Busy'. This only is planned for 10 bit applications.

3.10.4.6 Data Range Description

F03_16209 The PSI data range is divided into three separate ranges:

- Status and error message range,
- Signal range and
- Initialization range.

The data range depends on the data length for every slot and on the bit definition in detail.

The following table shows a detailed description of the data ranges and the channel coding bits for the 20 bit variant .

binary	decimal	hex	Signifivation	Range
MSB <- transmit order LSB				
d19 d18 d17 d18 d15 d14 d13 d12 d11 d10 d9 d8 d7 d8 d6 d4 d3 d2 d1 d0				
b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0				
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	524287	7FFF	Reserved	
0 1 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0	512000	7D000	Sensor Detect	Status and Error Message
0 1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1	495711	79FFF	Sensor Ready	
0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	491655	78000	Highest positive Sensor Signal	Signal Range
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	Highest Negative Sensor Signal	
1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	557055	87FFF	Status Data	
1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	540671	83FFF	ID16	Initialization Range
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	524288	80000	ID17	

Figure - Data Range in Synchronous and Asynchronous Mode



Error Range

Beside the signal range also a status and error messages range is defined in the psi specifacaton [1]. The signal status bit is invalid; the channel coding bits depend on the send slot. The bits D4 to D19 are defined as follow:

Bidirectional Communication: RC "o.K."	0x7840
Bidirectional Communication: RC "Error"	0x7880
"Sensor Busy"	0x7A00
"Sensor Ready"	0x79FF
"Sensor Defect"	0x7D00

This error signals are not implemented and not planned to send out in ROM-SW. It is possible to use this error signals in OTP - SW versions.

3.10.4.7 Bidirectional communication

F03_3262

One purpose of the bidirectional communication is the end-of-line programming or configuration. The other purpose is the diagnosis of the sensor unit, e.g. returned parts from the field. In normal operation mode, the sensor transmits sensor output data in data range 1 (as example ref. to PSI5 specification). A special "extended communication mode" is foreseen for testing and failure analysis. In the extended communication mode, the sensor may send other than the specified sensor output data in data range 1. For entering communication mode see [23] chapter Config Services on PSI - "BiDirMode".

According to the PSI5 Specification the ECU to sensor communication uses the "sync.-pulse" as the physical layer. A logical "1" is represented by the presence of a sync pulse, a logical "0" by the absence of a sync pulse at the expected time window of the sync signal period (tooth-gap method). The voltage for a logical "0" must remain below the 0.5 V limit specified as the sync signal t0 start condition. Entering the extended communication mode using the "XLong" data frame the expected sync.-period will have the nominal timing of the standard communication. The option to change the sync.-period after recognition of the extended communication is foreseen by separate registers that define the time windows. These sync.-periods may not be confused with sync periods of the standard communication. For the data link layer the definitions of the PSI5 specification regarding bit coding, data framing and frames, function codes and error return codes apply.

To allow synchronising before the start field of the BiDir command a SyncPulse has to be sent.

The uC transfer registers are accessible by the PSI Bidir interface and all functions of the chapter uC transfer commands apply (e.g. programming of OTP).

Further information see [23].

3.10.4.8 Example applications

F03_3263

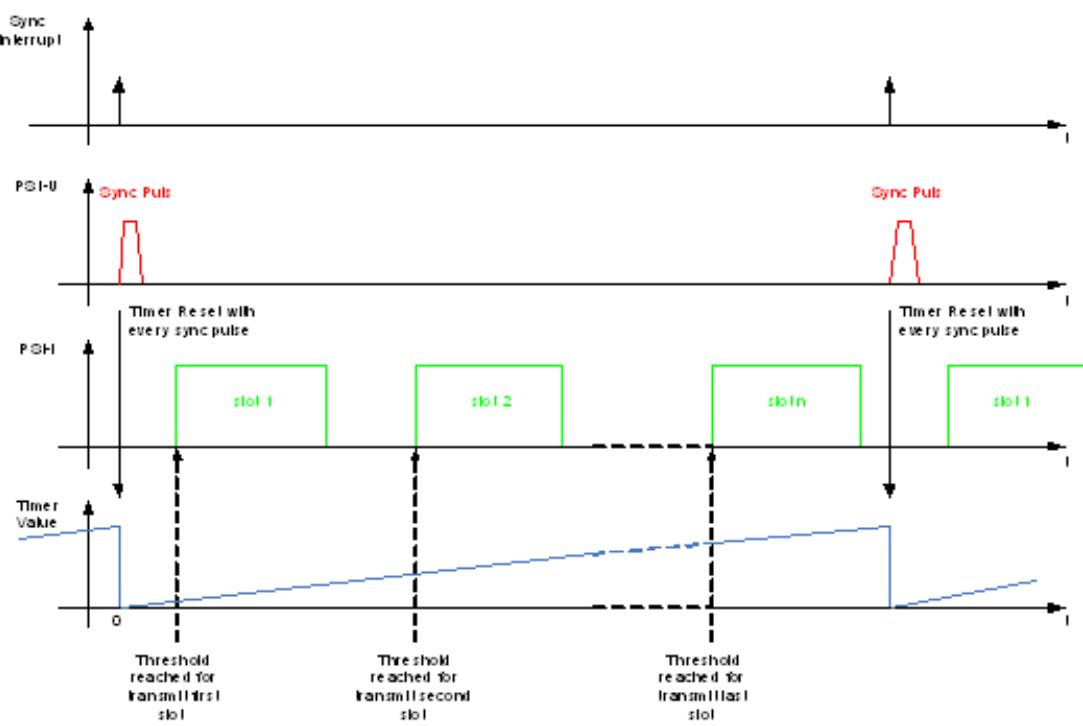
The section 4 in "SMI7xy Requirement Specification PSI5" describes two example applications which must be implemented as example in SMI7xy:

- PSI5-P20CRC-500/3H synchronous, high speed, 3 values in a 500 µs slot
- PSI5-A20CRC-300/L asynchronous, low speed, a new slot each 250 µs

The asynchronous protocol may be implemented in a form according to PSI5-A20CRC-900/3L.

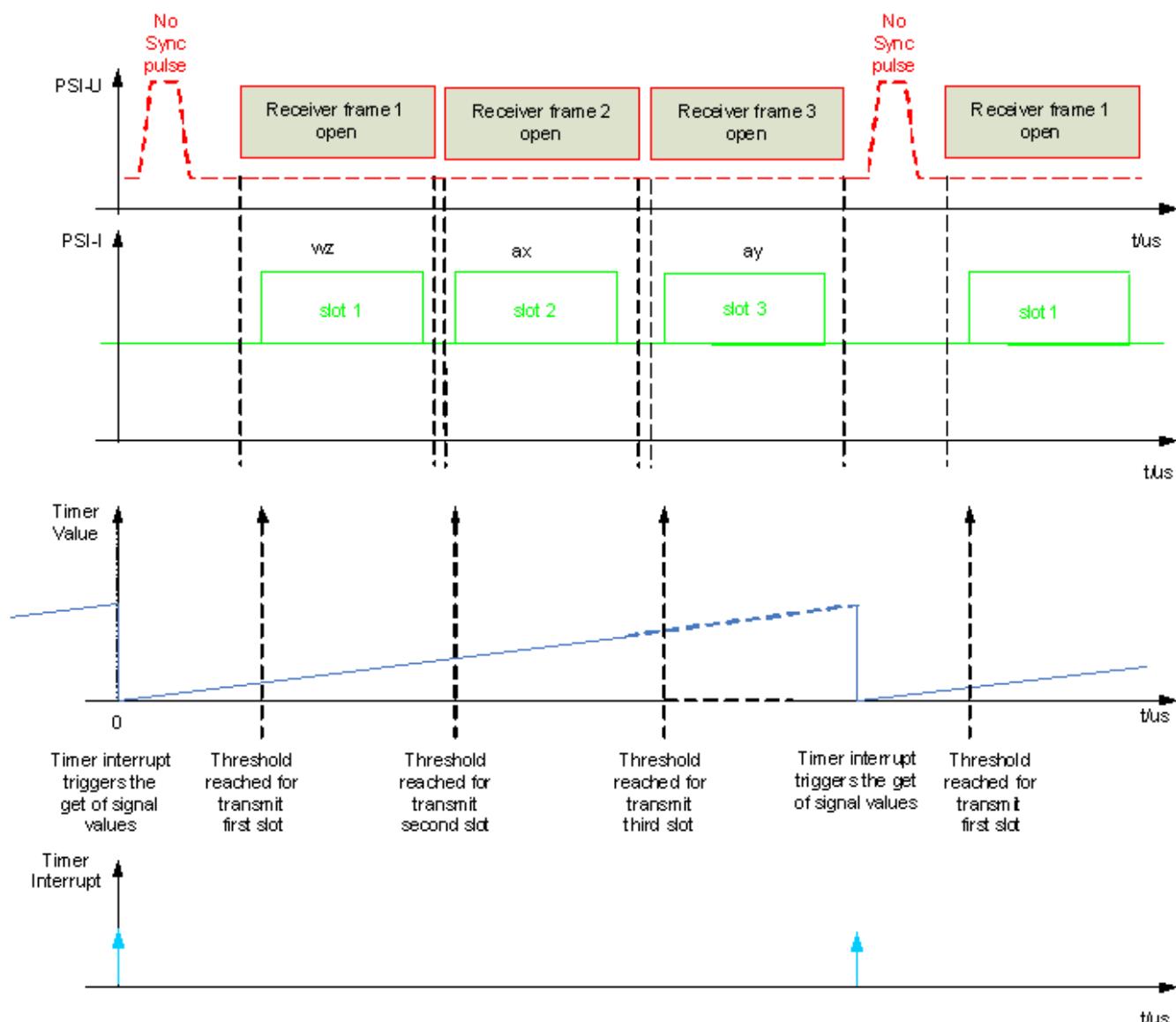
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Example application Synchronous Mode

For every slot the signal values is configurable with ID. No multiplexing during sync periods is possible.



Example application Asynchronous Mode

For every slot the signal values are configurable:

- with ID
- with address where the signal is read from
- sign correction
- signal limitation

Only 3 slots with 20 bit or 4 slots with 10 bits can be configured. It is not possible to multiplex between asynchronous periods.

A typical application sends the data in the order Ω / a1 / a2 (rate / acceleration /acceleration).



3.10.4.8.1 PSI Error Counter Application

3.10.4.8.1.1 General Description

F03_16277 For special investigations information about the start of counting of the error counters should come to know to the outside world. Usually only the reaching of the limit runs into a set of status flags or switching off the communication interface. Sometimes also the time before reaching the limits should be visible to evaluate the criticality of a situation or driving maneuver.

For the following measurements the Error Counter Application can be used:

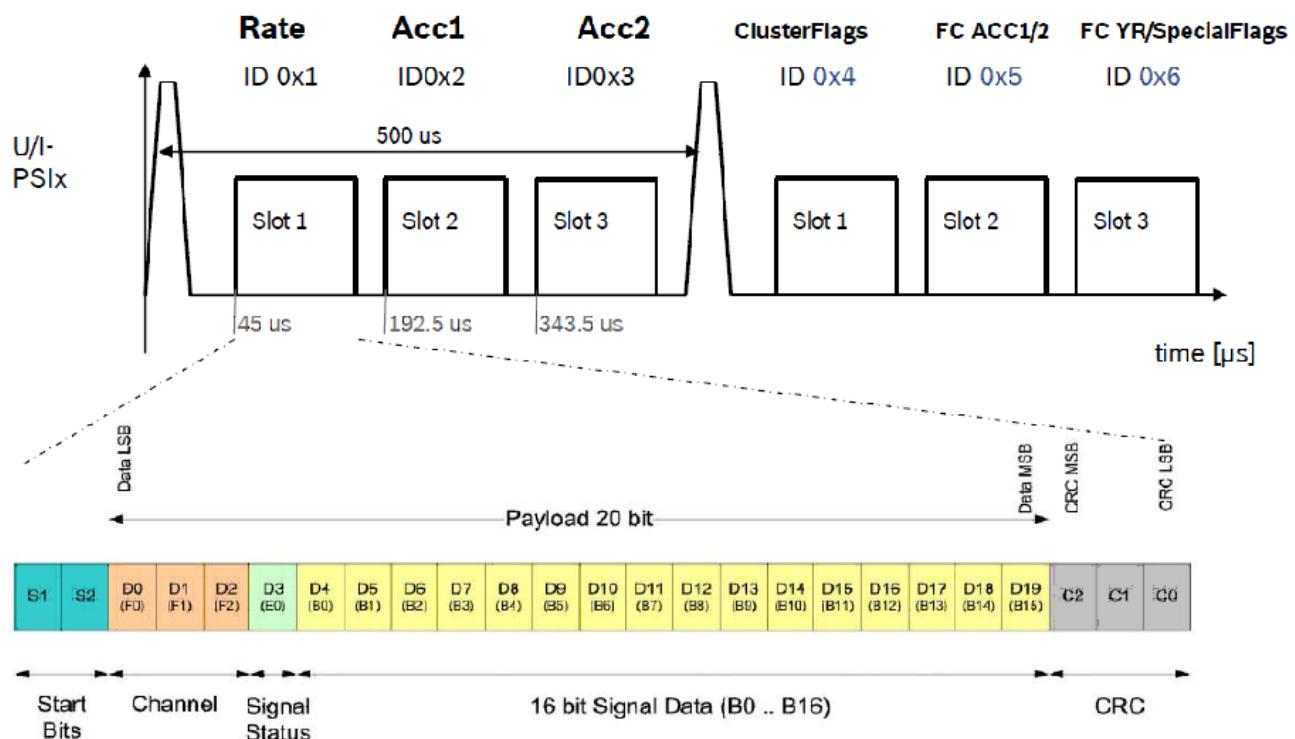
- Buildin car investigation (Einbauuntersuchungen)
- EMC investigation
- Electrostatic discharge measurement
- Turn and tilt table (Dreh- und Kipptisch) measurement
- Shaker investigation

There are some boundary conditions (Randbedingungen):

- only 20 bit slots
- with 189 kbaud synchronous mode or 125 kbaud asynchronous mode
- only relevant for the standard variant called MM7.z, not implemented for redundant SW variants
- SCON must be functional
- in every second sync period the error counter will be transmitted in a special layout format
- only LF error counter will be transmitted
- only the 8 LSBs of the LF error counter will be transmitted
- during the PSI Init phase no error counter values will be transmitted

3.10.4.8.1.2 Layout on the PSI5 Bus

F03_16276



Error Counter Layout:

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- 16 Bit Cluster Flags -> Slot1.b15 ..b0
- FC ACC1_LF (8bit LSB) -> Slot2.b15 .. b8
- FC ACC2_LF (8bit LSB) -> Slot2.b7..b0
- FC_YR_LF (8bit LSB) -> Slot3.b15..b8
- Special Flags (8bit LSB) -> Slot3.b7.. b0

The following PSI5 Channel ID's will be used:

- Signal Slot1 -> Rate ->ID 0x1 -> Slot1.d2 .. d0
- Signal Slot2 -> Acc1 ->ID 0x2 -> Slot2.d2 .. d0
- Signal Slot3 -> Acc2 ->ID 0x3 -> Slot3.d2 .. d0
- FZ Slot1 -> ID0x4 -> Slot1.d2 .. d0
- FZ Slot2 -> ID0x5 -> Slot1.d2 .. d0
- FZ Slot3 -> ID0x6 -> Slot1.d2 .. d0
- (Sync pulse periodes are alternating)

For status bits the following agreement takes place:

- Status bit d3 for all error counter slots are 1, which mean invalid.

Status bit d3 for all signal slots are DSP_Signalstatus [1] OR DSP_Signalstatus [0].

3.10.4.8.1.3 Layout for the CAN2PSI Interface (SesKion Box)

3.10.4.8.1.4 SW implementation hints

F03_16274 There are some **boundary conditions** for the SW implementation (Randbedingungen):

- PreSync Interrupt und Sync Interrupt has to be activated and implemented.
- Error counter values and flags has to be catched and prepared into the PreSync Interrupt. (This was for OTP-SW mandatory, for ROM-SW it could maybe done in the sync interrupt, depending from the run time of the sync interrupt routine.)
- Sync interrupt handler writes the data to the PSI DATA_TX register for transmission during sync period.
- In the sync period signal data and error counter data are alternately.
- The error counter are 10 bit wide, but only the 8 bit LSB of the error counter register will be transmitted over PSI.

The table depict the **register of the error counter**, only the bold marked error counter will be transmitted.



0x4000103c		error_cnt_0	error counter Nr. 0			0x00000000
	9...0	error_cnt_0	FC ACC1_HF	read-write	false	0x0
0x40001040		error_cnt_1	error counter Nr. 1			0x00000000
	9...0	error_cnt_1	FC ACC1_LF	read-write	false	0x0
0x40001044		error_cnt_2	error counter Nr. 2			0x00000000
	9...0	error_cnt_2	FC ACC2_HF	read-write	false	0x0
0x40001048		error_cnt_3	error counter Nr. 3			0x00000000
	9...0	error_cnt_3	FC ACC2_LF	read-write	false	0x0
0x4000104c		error_cnt_4	error counter Nr. 4			0x00000000
	9...0	error_cnt_4	FC YR_HF	read-write	false	0x0
0x40001050		error_cnt_5	error counter Nr. 5			0x00000000
	9...0	error_cnt_5	FC YR_LF	read-write	false	0x0
0x40001054		error_cnt_6	error counter Nr. 6			0x00000000
	9...0	error_cnt_6	FC Variable 1	read-write	false	0x0
0x40001058		error_cnt_7	error counter Nr. 7			0x00000000
	9...0	error_cnt_7	FC Variable 2	read-write	false	0x0

This table depicts the **cluster flag register**:

Bit Number	Fehler #	SMI7 Fehlerflagnamen	Fehlerbild
Slot3.b0	1	acc1_overload_det	Übersteuerung Signal Frontend, ACC1
Slot3.b1	2	acc2_overload_det	Übersteuerung Signal Frontend, ACC2
Slot3.b2	3	yrs_rate_quantizer	Erkennung Sättigung Detektionskreis
Slot3.b3	4	yrs_quad_I_tol	Übersteuerung Quadratur
Slot3.b4	5	yrs_agc_irregular	Erkennung Antriebsanschlägen (z.B. Klipping)
Slot3.b5	6	yrs_pll_unlock	Erkennung Antriebsanschlägen (Frequenzverlust, ggf. neues Anschwingen)
Slot3.b6	7	yrs_rate_adc	Sättigung AD - Wandler
Slot3.b7	8	yrs_drv_bp_lim	Sättigung Antrieb AD Wandler

Inside of the SCON Task the special flags for the EC application are collected and memorized in a RAM cell. Then the EC application does not read from the error flag registers directly, instead of this it reads from the RAM cell. After reading from the RAM cell the content of the RAM cell has to be set to zero to support a clear on read mechanism.

3.10.5 Sensor interfaces in different applications

F03_764

This chapter summarizes the different interfaces and defines which interfaces might be used at the same time during normal operation. Modes which are possibly needed during manufacturing are not covered by this specification. The following table lists the possibly interfaces used by SMI7xy sensors at the same time. "Si" denotes the sensors which are using the interfaces. Sensors which are using more than one interface are listed twice in a row.

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F03_765

Table 63: Possibly interfaces used by SMI7xy sensors at the same time

System	SPI (physical)	CAN (logical)	PSI (physical)	SPI-Mast. (physical)
Generic ECU with n sensors	X(S1...Sn)			
AB+ with n sensors	X(S1...Sn)			
ESPi with n sensors	X(S1...Sn)			
Current DCU with n sensors	X(S1...Sn)			
Future DCU with n sensors	X(S1...Sn)		X(S1...Sn)	
Sensor cluster with n sensors and PSI			X(S1...Sn)	
Sensor cluster with CAN		X(S1)		
Sensor cluster additional µC	X(S1...Sn)			
Sensor Cluster with CAN with n sensors	X(S2...Sn)	X(S1)		X(S1)
Sensor Cluster with PSI5 and different sensors	X(S2...Sn) (e.g. SMA560)			

F03_3331

Application hint: Limitations like the maximal number of sensors linked to the communication bus are unaccounted in the table above. The electrical limitations are described in the according chapters and have to be considered in application.

3.10.6 Watchdog interface

F03_768

The pin WDGI is used as an watchdog output pin. It generates a fixed puls train during normal operation. If any failure that affects CAN communication (see table in 7.4.4, column "WDGI_DISABLE") occurs, the WDGI output is turned off (constant at off, low level voltage). The pin is used as pure watchdog and is not used to do a frequency check.

F03_769

Table 64: Watchdog interface

Parameter / Condition	Symbol	Min	Typ	Max	Unit
Frequency range of the WDGI puls	F_WDGI	108,9	110	111,1	Hz
			Config.		
Duty cycle of puls train, on value	CY_ON_WDGI		2,5		%
Duty cycle of puls train, off value	CY_OFF_WDGI		97,5		%

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4. Parameter specifications

F04_9676 All parameter specifications are valid for the new part and after soldering with the soldering profile given in chapter 2.

4.1 Maximal conditions

F04_773 Values inside the specified maximum conditions must not damage the SMI7xy. No specification point is met at these ratings. SMI7xx will be full functional after stimulation.

4.1.1 General

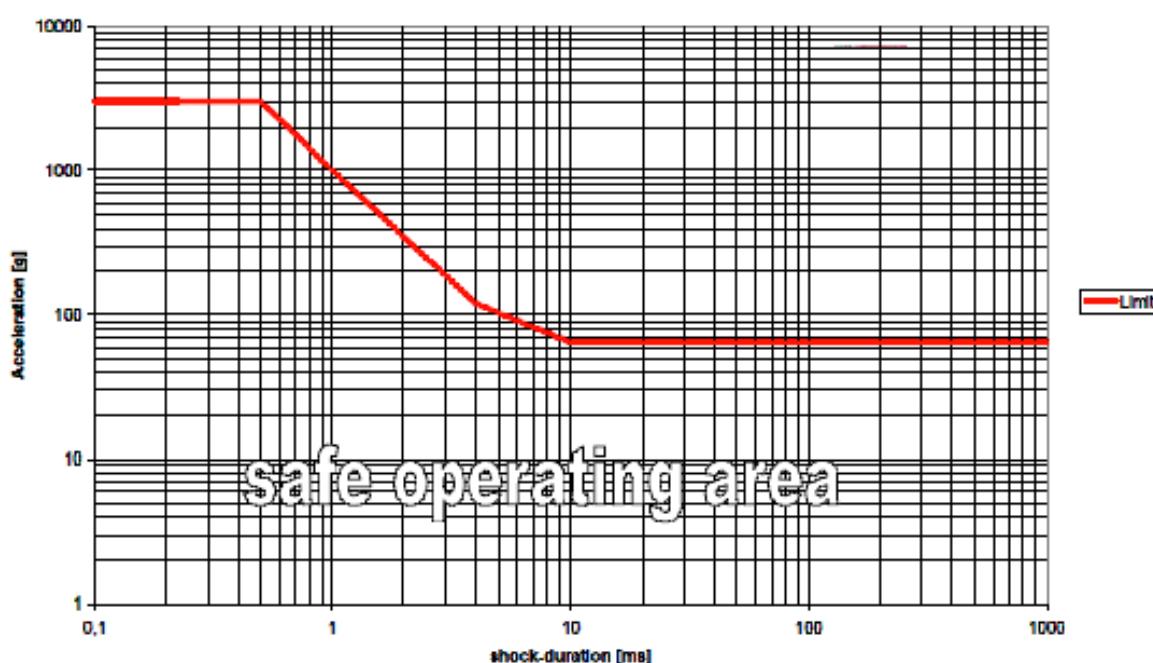
Parameter	Condition	Min. Value	Max. Value	Unit
Supply	See 3.4	-	-	V
Mechanical shock resistance	see {REF:F04_9631}	-	-	G
Temperature	Min./max. temperature while storing without damage of component	-55	140	°C
	Min./max. temperature while operating without damage of component	-50 ¹¹	140	°C
	Max. programming Temp.		70	°C
	Maximum gradient without damage of component	-20	20	K/min

F04_3411 ¹¹ No special failure concept for the temperature region -50°C to -40°C foreseen

F04_9630 Mechanical shock resistance is given for passive shocks in x, y and z direction for shock durations and accelerations given in the following plot.

F04_9631

Specification for acceleration during mounting





4.2 Operating conditions

F04_3409 No failure flags may be present inside valid operation condition unless the sensor itself has any faults or setting of failure flags is explicit required.

F04_3410 Table 65: Operating conditions

Parameter	Condition	Min. Value	Max. Value	Unit
Supply	See 3.4	-	-	-
Reset Glitch Timing	See section 3.4.15	-	-	-
Temperature (ambient)	Static	-40	125	°C
	Static, ESPi (no usage of PSI communication or supply of another component)	-40	140	°C
	Variation over time	-6	+6	K/min
	Variation over time, ESPi	-11	11	K/min
Lifetime	See section 5.1	-	-	-
Start-up timing	See 3.5.1, {REF:F03_314}	-	-	-
Measurement range	Angular rate, no clipping at real input, no flags	-300	300	°/s
	Acceleration, no clipping at real input, no flags low frequency (LF) acceleration channel	-5	5	G
	Acceleration, no clipping at real input, no flags high frequency (HF) acceleration channel	-35 for Axy; -15 for Az	35 for Axy; 15 for Az	G
	Temperature, output with no clipping at real input, no flags	-40	140	°C

F04_9667 On/off cycles: 300.000 including 12410 cold starts (2/day) with 54k temperature change (for ESPi: 66K)and 49640 warm starts (8/day) with 30k temperature change

4.3 Functional parameter requirements

F04_3497 All following parameters will be fulfilled with 4sigma probability / 90% confidence as proved on defined test equipment. Mentioned probability is based on the mathematical definition and not on the SIX-SIGMA-QUALITY PROZESS.

For parameters that are not normally distributed, the according number of parts failing the specific criteria will be set as goal (in % / ppm / ppb):

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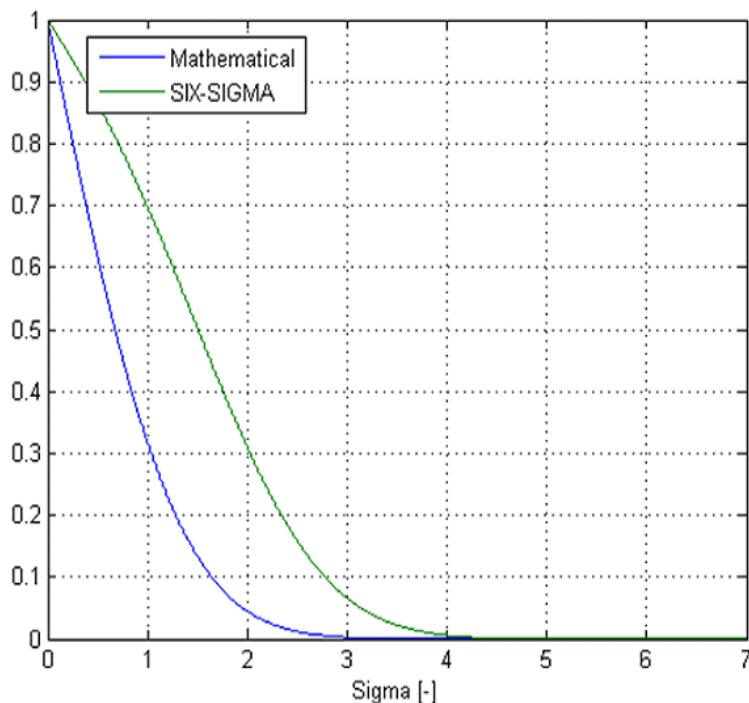


Figure above compares the mathematical sigma-function and SIX-SIGMA function that can be found in industrial literature.

Sigma	Mathematical	SIX-SIGMA
1	31,73%	69,77%
2	4,55%	30,88%
3	0,27%	6,68%
4	63,34ppm	6209ppm
5	0,57ppm	232,63ppm
6	1,97ppb	3397,67ppb
4,645	3,40ppm	830,43ppm

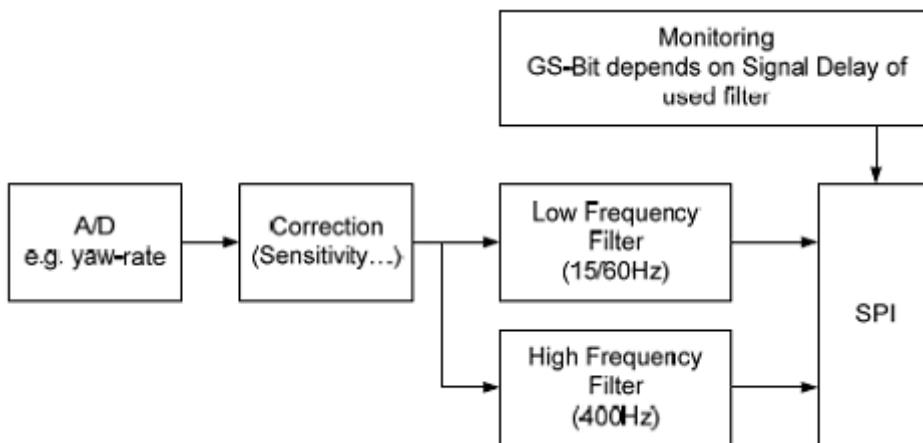
F04_3498 Values will be achieved after the specified start-up time.

4.3.1 Different output channels

F04_3499 The values are valid for all output channels and axis if not noted otherwise. This means, the low frequency channels **LF** (e.g. 7Hz, 15Hz, 57Hz) and the high frequency channel **HF** (400Hz) are compensated. The signal delay of the used channels will be considered by the monitoring function (GS-Bit (channel status bit) is set because of an internal failure, after the failure disappears the GS status must remain for the filter specific signal delay time).

See following figure:

F04_787

**Figure 50:** Different output channels

F04_788

No additional channels (ports) will be foreseen.

4.3.2 Yaw-rate channels

F04_790

Customer demands in brackets if not fulfilled. If qualification results of sensor parameters are better than the required targets, the better values will be provided with the final datasheet (for RB internal use only):

F04_791

Table 67: Yaw-rate channels

Parameter	Condition	Ω_x	Ω_z	Unit
Bit width	LF and HF channel before output	16	16	Bit
Output range	LF and HF channel before output	-2^{15} $\dots 2^{15}-1$	-2^{15} $\dots 2^{15}-1$	LSB
Sensitivity ¹³	Rate LF and HF nominal output	100	100	LSB/ [°] /s
	Quad HF nominal output	25	25	LSB/ [°] /s
	cQ-BITE High nominal output	337.5	337.5	LSB/ [°] /s
	cQ-BITE Low nominal output	225	225	LSB/ [°] /s
Sensitivity error	Variation to nominal (full measurement range)	< 3 (2)	< 3 (2)	%
	Variation to nominal (<100/ [°] /s) (evaluation with A-samples)	< 3	< 3	%
	Variation to nominal (<10/ [°] /s) (evaluation with A-samples)	< 3	< 3	%
Resolution	Smallest measurable variation	< 0.05	< 0.05	/ [°] /s
Nonlinearity	Up to 10/ [°] /s (Least square fit [-10/ [°] /s...10/ [°] /s])	< 0.3	< 0.3	/ [°] /s
	Up to 150/ [°] /s (Least square fit [-150/ [°] /s...150/ [°] /s])	< 0.5	< 0.5	/ [°] /s
	Up to 300/ [°] /s (Least square fit [-300/ [°] /s...300/ [°] /s])	< 1	< 1	/ [°] /s
Differential Nonlinearity ¹⁴	Up to 150/ [°] /s (5/ [°] /s steps)	< 4	< 4	%
	Up to 300/ [°] /s (5/ [°] /s steps)	< 10	< 10	%
Offset	Offset overall (offset calibration in mounting position at 25°C with +/- 0.1/ [°] /s accuracy conducted by the customer is obligatory to fulfill offset)	< 3 (1)	< 3 (1)	/ [°] /s

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	specification)			
Offset short term drift	Short term drift span at constant temp. ^{26,27} Short term drift span including full temperature range ^{26,28} Short term drift span overall ^{26,29}	< tbd (1) < tbd (2) < tbd (3)	< tbd (1) < tbd (2) < tbd (3)	°/s
Absolute Offset	Absolute Offset Reference point is the absolute zero point, i.e. 0mg ³⁰	< tbd (<+/- 1)	< tbd (<+/- 1)	°/s
	Offset Over all w/o calibration after soldering for information (evaluation with A-samples)	< tbd.	< tbd.	°/s
	Offset @ 25°C after soldering for information (evaluation with A-samples)	< tbd.	< tbd.	°/s
	Absolute drift at start-up, t=500ms... 3min @ const. temp.	< 0.5	< 0.5	°/s
	Absolute drift at start-up, t=3min... 10min @ const. temp.	< 0.2	< 0.2	°/s
	Drift over time (with 3K/min), no binding commitment to RB-external customers until proven, value in bracket can be committed.	< 0.1 [<0.2]	< 0.1 [<0.2]	°/s/min
	Drift over time (with 6K/min)	< 0.2 (0.1)	< 0.2 (0.1)	°/s/min
	Drift over time (with 11K/min) ¹⁵	< 0.2 (0.1)	< 0.2 (0.1)	°/s/min
	Drift over temperature (with 6K/min) ¹⁶	< 0.1	< 0.1	°/s/K
	Drift over temperature (with 11K/min) ^{15,16}	< 0.1	< 0.1	°/s/K
Sensitivity hysteresis	Over yaw-rate @ const. temp.	< 0.3	< 0.3	°/s
Noise	Depends on filter setting, see chapter {REF:F04_847}.	-	-	°/s _{RMS}
Cross-axis sensitivity	Variation from input of off-axis (Rotation estimated 1.5° / Tilt 1°)	< 2.3 (1.74)	< 1.74	%
Overload ¹⁷	DC Yawrate stimulus in any axis for longer than 50ms with output signal at clipping level but no failure flags and signal path not in saturation	< 1000	< 1000	°/s
	DC Acceleration stimulus in any axis for longer than 50ms with output signal at clipping level but no failure flags and signal path not in saturation	< 500	< 500	G
	Recovery time after overload LF1 filter channel (15Hz/50dB)	< 120	< 120	ms
	Recovery time after overload LF2 filter channel (60Hz/40dB)	< 50	< 50	ms
	Recovery time after overload LF3 filter channel (7Hz/50dB)	< 200	< 200	ms
	Recovery time after overload LF4 filter	< 90	< 90	ms

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	channel (15Hz/40dB)			
	Recovery time after overload HF filter channel	< 35	< 35	ms
Earth gravity ¹⁸	Sensitivity dependence on earth gravity if mounted in different positions	< 0.1	< 0.1	%/G
	Offset dependence on earth gravity if mounted in different positions	< 0.1	< 0.1	%/G
Vibration robustness	See chapter 4.6.	-	-	-
PSRR	See chapter 3.4.1 and 3.4.2	-	-	-
EMC	See chapter 5.2	-	-	-
Ratiometry 5.0V Case ¹⁹ (For information only, no requirement)	d Offset / d Supply: The angular rate output shall be insensitive over the specified DC- supply voltage range, 3.3V and 5V operation	< 0.2 (0.05)	< 0.2 (0.05)	°/s/V
Ratiometry 3.3V Case ²⁰ (For information only, no requirement)	d Offset / d Supply: The angular rate output shall be insensitive over the specified DC- supply voltage range, 3.3V and 5V operation	< 0.2 (0.05)	< 0.2 (0.05)	°/s/V

F04_3645

¹³ Sensitivity defined @ 0Hz (DC-stimulus). Sensitivity is declining at higher frequencies depending on damping of sensor element and filter settings

¹⁴ Differential nonlinearity is linked to the step size, not the measurement range.

¹⁵ Can not be guaranteed and has to be estimated with A-samples (according to SMI650)

¹⁶ Derived from „Drift over time“-parameter: 0.2°/s/min with 6K/min = 0.03°/s/K; 0.2°/s/min with 11K/min = 0.02°/s/K

¹⁷ Recovery time is the time the sensor output signal returns to its real value (within specified limits) after exceeding the specified DC stimulus finishes. Proof by simulations and experiments as far as possible. No failure flags for overload below specified limit with shorter duration than 50ms. When signal is at clipping level a dsp_limiter flag is set, but masked to have no effect on the channel status

¹⁸ Errors due to earth gravity are included in offset and sensitivity parameters. Parameters guaranteed by design.

¹⁹ Errors due to ratiometry are included in offset over all parameter. The given value is no hard limit, has informational character and will be measured during development.

²⁰ Errors due to ratiometry are included in offset over all parameter. The given value is no hard limit, has informational character and will be measured during development.

4.3.3 Acceleration channels

F04_795

Customer demands in brackets if not fulfilled. If qualification results of sensor parameters are better than the required targets, the better values will be provided with the final datasheet (for RB internal use only):

F04_796

Table 68: Acceleration channels

		SMI700		SMI710		
Parameter	Conditions	Ax (=ACC2)	Ay (=ACC1)	Ay (=ACC1)	Az (=ACC2)	Unit
Bit width	LF and HF channel before output	16	16	16	16	Bit
Output range	LF and HF channel before	-2 ¹⁵ ... 2 ¹⁵ -1	LSB			

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	output					
Sensitivity ²¹	LF nominal output	5000	5000	5000		LSB/G
	HF nominal output	500	500	500		LSB/G
Sensitivity Error	Variation to nominal, LF channel ²²	< 3 (2)	< 3 (2)	< 3 (2)	< 3 (2)	%
	Variation to nominal, HF channel with $ accil < 4.9G^{22}$	< 3 (2)	< 3 (2)	< 3 (2)	< 3 (2)	%
	Variation to nominal, HF channel with $ accil < 35G$	< 6 (5)	< 6 (5)	< 6 (5)	< 5 ²³	%
Resolution	Smallest measurable change, LF channel	< 2.2	< 2.2	< 2.2	< 2.2	mG
	Smallest measurable change, HF channel	< 5	< 5	< 5	< 5	mG
Offset	Offset over all after calibration @ 25°C with +/- 1mG accuracy ^{24,25}	< 50	< 50	< 50	< 70; (50) < 50: -10°C ... 140°C (50)	mG
	Offset Over all w/o calibration after soldering for information / evaluation with A-sample	tbd	tbd	tbd	tbd	mG
	Offset @ 25°C after soldering for information only / evaluation with A-samples	tbd	tbd	tbd	tbd	mG
Offset short term drift	Short term drift span at constant temp. ^{26,27}	< tbd (10)	< tbd (10)	< tbd (10)	< tbd (10)	mG
	Short term drift span including full temperature range ^{26,28}	< 20	< 20	< 20	< 35	mG
	Short term drift span overall ^{26,29}	< tbd (20)	< tbd (20)	< tbd (20)	< tbd (35)	mG

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Absolute Offset	Absolute Offset Reference point is the absolute zero point, i.e. 0mg^{30}	tbd	tbd	tbd	tbd	mG
Offset	Drift over time, full temperature range and maximum gradient	< 5	< 5	< 5	< 5 ³¹	mG/min
	Drift over temperature, full range and maximum gradient ³²	< 5	< 5	< 5	< 5	mG/K
	Absolute drift over time at a constant temperature (Bias stability 24h)	< 10	< 10	< 10	< 10	mG
Hysteresis	Over acceleration @ const. temp.	< 5.4	< 5.4	< 5.4	< 5.4	mG
Nonlinearity	LF channel accil < 1.7G	< 15	< 15	< 15	< 15	mG
	LF channel accil < 3G	< 20	< 20	< 20	< 20	mG
	LF channel accil < 4.9G	< 50	< 50	< 50	< 50	mG
	HF channel accil < 4.9G	< 50	< 50	< 50	< 50	mG
	HF channel accil < 35G	< 1150 (700)	< 1150 (700)	< 1150 (700)	< 700 ³³	mG
Differential nonlinearity	-	-	-	-	-	-
Noise	Depends on filter setting, see chapter {REF:F04_850}.	-	-	-	-	mG _{RMS}
Cross-axis sensitivity	Variation from input of off-axis (Rotation estimated 1.5° / Tilt 1°)	< 2.3 (1.74)	< 2.3 (1.74)	< 2.3 (1.74)	< 1.74	%
Overload ³⁴	DC Acceleration stimulus in any axis for longer than 50ms with output signal at clipping level but no failure flags	< 500	< 500	< 500	< 500	G

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	and signal path not in saturation					
	DC Yawrate stimulus in any axis for longer than 50ms with output signal at clipping level but no failure flags and signal path not in saturation	< 1000	< 1000	< 1000	< 1000	°/s
	Recovery time after overload LF1 filter channel (15Hz/50dB)	< 120	< 120	< 120	< 120	ms
	Recovery time after overload LF2 filter channel (60Hz/40dB)	< 50	< 50	< 50	< 50	ms
	Recovery time after overload LF3 filter channel (7Hz/50dB)	< 200	< 200	< 200	< 200	ms
	Recovery time after overload LF4 filter channel (15Hz/40dB)	< 90	< 90	< 90	< 90	ms
	Recovery time after overload HF filter channel	< 35	< 35	< 35	< 35	ms
Earth gravity ³⁵	Sensitivity dependence on earth gravity if mounted in different positions	<0.1	<0.1	<0.1	<0.1	%/G
	Offset dependence on earth gravity if mounted in different positions	<2	<2	<2	<2	mG/G
Vibration robustness	See chapter Fehler! Verweisquelle konnte nicht gefunden werden.	-	-	-	-	-
PSRR	See chapter 3.4.1 and 3.4.2	-	-	-	-	-
EMC	See chapter 5.2	-	-	-	-	-
Ratiometry 5.0V Case ³⁶ (For	d offset / d supply: The	< 5	< 5	< 5	< 5	mG/V

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information only, no requirement)	angular rate output shall be insensitive over the specified DC- supply voltage range, 3.3V and 5V operation					
Ratiometry 3.3V case ³⁶ (For information only, no requirement)	d offset / d supply: The angular rate output shall be insensitive over the specified DC- supply voltage range, 3.3V and 5V operation	< 5	< 5	< 5	< 5	mG/V

F04_3962 Hint: Signal will be valid available a certain time after PLL Unlock - See section 7.

²¹ Sensitivity defined @ 0Hz (DC-stimulus). Sensitivity is declining at higher frequencies depending on damping of sensor element and filter settings.

²² Adjustment over temperature is technical foreseen within ASIC. No set up of measurement equipment for temperature adjustment planned. Decisions to realize fix temperature adjustment with A-Samples evaluation to achieve 2% (CC+AE) - fixed value.

²³ Measurement range 15G

²⁴ An offset calibration in mounting position at ambient temperature conducted by the customer is obligatory to fulfill offset specification (offset-measurement without error due to sensitivity is only possible without stimulus due to earth gravity).

²⁵ Offset specification only valid for max. ambient temperature of 125°C

²⁶ The "short term drift span" is defined by the delta between the maximum and minimum offset value (|max. value - min. value|) under variation of the respective parameters (time, if applicable temperature, ratiometry, humidity, etc). The specified values for the short term drift have to be fulfilled after soldering and at any time during lifetime.

²⁷ Short term drift span at constant temperature including drift during one full PON cycle (i.e. including drift at start-up "Einlaufdrift"), drift during POFF for up to 1 day, drift during 100 subsequent short PON/POFF cycles

->Protokoll zum CR 111 (06.02.13): Einschätzung auf Basis A-Muster: 20mg wären erreichbar, 10mg vmtl. grenzwertig, möglicherweise nicht erreichbar. Werte werden nach B-Si Charakterisierung definiert.

²⁸ Short term drift span including drift over temperature (-40°C - 140°C), drift during one full PON cycle (i.e. including drift at start-up "Einlaufdrift"), drift during POFF for up to 1 month (temperature conditions at POFF can be opposite extreme corner temperature as compared to PON). Humidity and ratiometric effects are not included.

²⁹ Short term drift span including drift over temperature (-40°C - 140°C), drift during one full PON cycle (i.e. including drift at start-up "Einlaufdrift"), drift during POFF for up to 1 month (temperature conditions at POFF can be opposite extreme corner temperature as compared to PON), humidity 90% r.h. at 45°C / 80% r.h. at 55°C (worst-case conditions derived from worldwide humidity/temperature distribution), ratiometric effects including each of the following variations of supply voltage at V_b: SPI/CAN: 3.0-3.6V, 4.6-5.5V, 6.4-7.1V; PSI: 4.3-12V (DC-effect of sync puls in considered in 12V)

->Protokoll zum CR 111 (06.02.13): 20mg für SPI und CAN grenzwertig bzw. nicht ganz erreichbar, 30mg erreichbar (Basis: A-Muster-Charakterisierung), PSI-Variante etwas schlechter als CAN und SPI

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aufgrund der zu erwartenden größeren Spannungsschwankungen, aber besser als 30mg. Werte werden nach B-Si Charakterisierung definiert.

³⁰ Reference point is the absolute zero point 0mg, i.e. lifetime effects are included. The measurement has to include the following effects: No calibration after soldering (i.e. soldering effects are included); Drift during one full PON cycle, i.e. including drift at start-up ("Einlaufdrift"); Drift during Power off (up to 1 month, temperature conditions at switching off are not the same as at switching on, opposite extreme corner temperatures have to be considered); full temperature range (-40°C – 140°C)

->Protokoll zum CR 111 (06.05.13): Werte werden auf Basis B-Muster Charakterisierung / A-Mu Erprobung ermittelt und geliefert

³¹ <12mg/min for power-on-drift, otherwise 5mg/min

³² Derived from „Drift over time“-Parameter: 5mG/min with 11K/min = 0.45mG /K is estimated by AE and therefore the 5mG/K can be achieved.

³³ Measurement range 15G

³⁴ Recovery time is the time the sensor output signal returns to its real value (within specified limits) after exceeding the specified DC stimulus finishes. Proof by simulations and experiments as far as possible. No failure flags for overload below specified limit with shorter duration than 50ms. When signal is at clipping level a dsp_limiter flag is set, but masked to have no effect on the channel status.

³⁵ Errors due to earth gravity are included in offset and sensitivity parameters.

³⁶ Errors due to ratiometry are included in offset parameters. The given value is no hard limit, has informational character and will be measured during development.

4.4 Temperature signal

F04_799

Table 69: Temperature signal

Paramter	Conditions	min	typ	max	unit
Sensitivity	Nominal		200		LSB/K
	Variation to nominal ³⁷	-5		5	%
Nonlinearity		-2		2	K
Offset	Temperature at 0 LSB		50		°C
Offset error		-5		5	K
Noise				1	K _{RMS}
Update Rate		10			Hz
Bandwidth	-3dB Cut Off Frequency	1			Hz

F04_4020

Two temperature sensors are implemented in the module.

³⁷ +/-5% w/- calibration; w/o calibration +/-6% achievable

F04_9390

Temperature signal can be read at TEMP1 (0x400018a4, Page1 ID0) and TEMP2 (0x400018a8, Page1 ID9).

4.5 Signal filtering and update specification

F04_802

The following filter specification is valid for the complete sensor including mechanical, analog and digital filter elements. The different filter elements are designed to achieve the specified characteristic for the complete sensor. The following figure shows the definition of the following specifications.

F04_803

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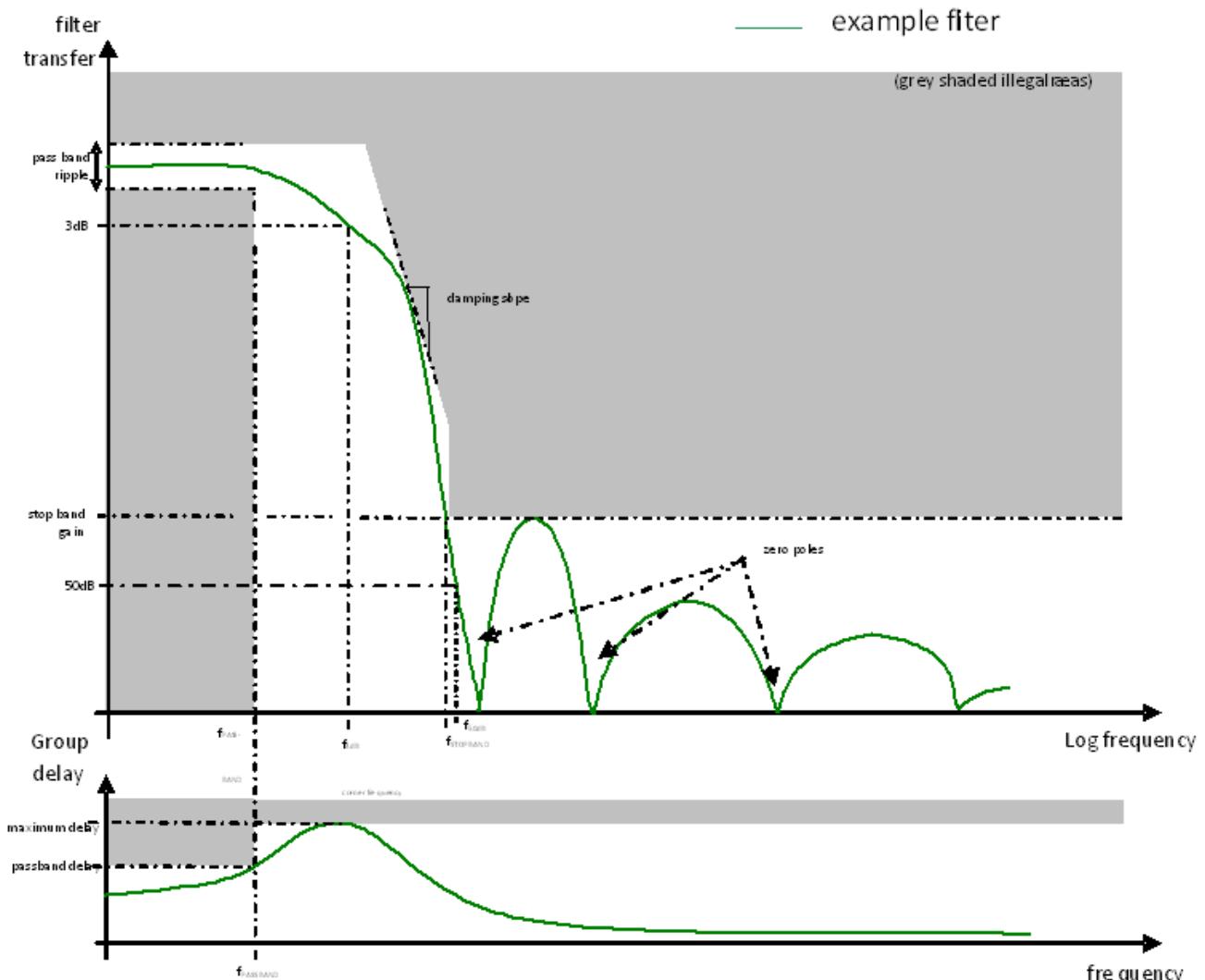


Figure 51: Filter Specification

4.5.1 General Filter Specifications

E04_805

The damping in pass-band is monotonically decreasing for all filter configurations. The filters characteristic between different channels of one module (all acceleration and rate channels) are.



Parameter	Conditions	Min	Typ	Max	Unit
difference in	LF1 (15Hz)	-0.83	-1.13	-1.42	ms
	LF2 (60Hz)	-0.40	-0.64	-0.87	ms
	LF3 (7Hz)	-1.27	-1.62	-1.97	ms
	LF4 (t.b.d.)	-0.71	-0.98	-1.26	ms
	HF (400Hz)	-0.30	-0.52	-0.75	ms
3dB difference	LF1 (15Hz)	0.45	0.55	0.65	Hz
Between wxz –axy	LF2 (60Hz)	2.40	5.41	8.43	Hz
	LF3 (7Hz)	0.24	0.27	0.31	Hz
	LF4 (t.b.d.)	0.39	0.49	0.58	Hz
	HF (400Hz)	94.01	181.87	269.72	Hz

Parameter	Conditions	Min	Typ	Max	Unit
difference in	LF1 (15Hz)	-1.08	-1.80	-2.51	ms
	LF2 (60Hz)	-0.65	-1.26	-1.88	ms
	LF3 (7Hz)	-1.52	-2.29	-3.07	ms
	LF4 (t.b.d.)	-0.96	-1.65	-2.35	ms
	HF (400Hz)	-0.54	-1.19	-1.85	ms
3dB difference	LF1 (15Hz)	0.47	0.82	1.17	Hz
Between wxz –az	LF2 (60Hz)	3.76	14.71	25.66	Hz
	LF3 (7Hz)	0.24	0.32	0.40	Hz
	LF4 (t.b.d.)	0.42	0.76	1.11	Hz
	HF (400Hz)	157.23	261.61	365.98	Hz

Parameter	Conditions	Min	Typ	Max	Unit
difference in	LF1 (15Hz)	-0.25	-0.67	-1.09	ms
	LF2 (60Hz)	-0.24	-0.63	-1.02	ms
	LF3 (7Hz)	-0.25	-0.67	-1.10	ms
	LF4 (t.b.d.)	-0.25	-0.67	-1.09	ms
	HF (400Hz)	-0.25	-0.67	-1.10	ms
3dB difference	LF1 (15Hz)	0.02	0.27	0.52	Hz
Between axy –axy	LF2 (60Hz)	1.36	9.30	17.23	Hz
	LF3 (7Hz)	0.00	0.05	0.09	Hz
	LF4 (t.b.d.)	0.02	0.28	0.53	Hz
	HF (400Hz)	63.22	82.60	101.98	Hz

4.5.2 Specific Filter Specifications

F04_425Z

4 different LF filter characteristics are foreseen. LF-Filter: LF1($f_{3dB} \sim 20Hz$), LF2($f_{3dB} \sim 75Hz$), LF3($f_{3dB} \sim 10Hz$) and LF4($f_{3dB} \sim 20Hz$, minimal group delay) are specified in the following. Only one of the LF-filters will be used at the same time. The configuration is at the end of line.

An additional HF-filter ($f_{3dB}: W_{x,z} \sim 400Hz$, $a_{x,y} \sim 250Hz$, $a_z \sim 150Hz$) characteristic is foreseen an output signal with this characteristic is in parallel to one of the other LF-filter characteristics.

F04_811

Table 70: Signal update rate

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Parameter	Conditions	Min	Typ	Max	Unit
Signal update rate	New signal value available, angular rate and acceleration output after LF-filter	1850	2100	2300	Hz
	New signal value available, angular rate and acceleration output after HF-filter	7500	8300	9200	Hz

4.5.2.1 YRS-xz Bandwidth LF1

F04_813

Table 71: YRS-xz Bandwidth LF1

YRS_xz	Min	Typ	Max	Unit
f _{PASSBAND}		5.0		Hz
f _{STOPBAND}		50		Hz
corner frequency	18.6	20.6	22.7	Hz
pass band ripple	-0.05	-0.04	0.00	dB
stop band gain	-53.0	-52.8	-52.4	dB
f _{-50dB}	40.3	44.8	49.3	Hz
f _{-40dB}	39.0	43.3	47.6	Hz
min. damping slope	-22.6	-22.0	-21.3	dB/dec
max. damping slope	-1001.5	-1001.0	-1000.5	dB/dec
Group delay pass band	27.1	29.7	32.3	ms
Group delay between pass- and stopband	36.9	40.4	44.0	ms

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4.5.2.2 ACC-xy Bandwidth LF1

F04_815

Table 72: ACC-xy Bandwidth LF1

ACC, xy	Min	Typ	Max	Unit
f_{PASSBAND}		5.0		Hz
f_{STOPBAND}		50		Hz
corner frequency	18.1	20.1	22.1	Hz
pass band ripple	-0.05	-0.04	0.00	dB
stop band gain	-53.3	-53.0	-52.4	dB
$f_{-50\text{dB}}$	39.3	43.7	48.1	Hz
$f_{-40\text{dB}}$	38.0	42.3	46.5	Hz
min. damping slope	-22.6	-22.5	-22.5	dB/dec
max. damping slope	-998.3	-990.9	-983.5	dB/dec
Group delay pass band				
	27.9	30.8	33.7	ms
Group delay between pass- and stopband				
	37.9	41.8	45.6	ms

4.5.2.3 ACC-z Bandwidth LF1

F04_817

Table 73: ACC-z Bandwidth LF1

ACC, z	Min	Typ	Max	Unit
f_{PASSBAND}		5.0		Hz
f_{STOPBAND}		50		Hz
corner frequency	17.8	19.9	22.1	Hz
pass band ripple	-0.07	-0.05	0.00	dB
stop band gain	-54.6	-53.5	-52.5	dB
$f_{-50\text{dB}}$	39.3	43.7	48.1	Hz
$f_{-40\text{dB}}$	37.9	42.2	46.5	Hz
min. damping slope	-22.6	-22.2	-21.8	dB/dec
max. damping slope	-994.1	-956.0	-918.0	dB/dec
Group delay pass band				
	28.2	31.5	34.8	ms
Group delay between pass- and stopband				
	38.2	42.3	46.4	ms

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4.5.2.4 YRS-xz Bandwidth LF2

F04_819

Table 74: YRS-xz Bandwidth LF2

YRS_xz	Min	Typ	Max	Unit
f_{PASSBAND}		20.0		Hz
f_{STOPBAND}		170		Hz
corner frequency	69.8	77.5	85.3	Hz
pass band ripple	-0.15	-0.12	0.00	dB
stop band gain	-41.5	-41.3	-25.1	dB
$f_{-50\text{dB}}$	n.a.	n.a.	n.a.	Hz
$f_{-40\text{dB}}$	152.4	189.3	186.2	Hz
min. damping slope	-18.9	-18.4	-17.8	dB/dec
max. damping slope	-688.1	-687.5	-686.9	dB/dec
Group delay pass band	5.9	6.4	7.0	ms
Group delay between pass- and stopband	7.7	8.5	9.3	ms

4.5.2.5 ACC-xy Bandwidth LF2

F04_821

Table 75: ACC-xy Bandwidth LF2

ACC_xy	Min	Typ	Max	Unit
f_{PASSBAND}		20.0		Hz
f_{STOPBAND}		170		Hz
corner frequency	64.5	73.2	81.9	Hz
pass band ripple	-0.20	-0.15	0.00	dB
stop band gain	-44.1	-43.0	-28.3	dB
$f_{-50\text{dB}}$	n.a.	n.a.	n.a.	Hz
$f_{-40\text{dB}}$	147.8	164.6	181.5	Hz
min. damping slope	-18.7	-18.1	-17.5	dB/dec
max. damping slope	-665.1	-617.7	-570.3	dB/dec
Group delay pass band	6.3	7.1	7.9	ms
Group delay between pass- and stopband	8.1	9.0	9.9	ms

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4.5.2.6 ACC-z Bandwidth LF2

F04_823

Table 76: ACC-z Bandwidth LF2

ACC_z	Min	Typ	Max	Unit
f _{PASSBAND}		20.0		Hz
f _{STOPBAND}		170		Hz
corner frequency	53.2	66.4	79.5	Hz
pass band ripple	-0.39	-0.26	0.00	dB
stop band gain	-49.1	-45.9	-29.2	dB
f _{50dB}	n.a.	n.a.	n.a.	Hz
f _{40dB}	145.1	162.9	180.8	Hz
min. damping slope	-18.4	-16.1	-13.9	dB/dec
max. damping slope	-631.6	-521.7	-411.8	dB/dec
Group delay pass band	6.5	7.7	8.9	ms
Group delay between pass- and stopband	8.2	9.1	9.9	ms

4.5.2.7 YRS-xz Bandwidth LF3

F04_825

Table 77: YRS-xz Bandwidth LF3

YRS_xz	Min	Typ	Max	Unit
f _{PASSBAND}		2.5		Hz
f _{STOPBAND}		25		Hz
corner frequency	10.1	11.2	12.3	Hz
pass band ripple	-0.06	-0.05	0.00	dB
stop band gain	-53.0	-45.2	-30.6	dB
f _{50dB}	22.4	24.9	27.4	Hz
f _{40dB}	21.7	24.1	26.5	Hz
min. damping slope	-21.4	-20.8	-20.3	dB/dec
max. damping slope	-994.2	-993.7	-993.3	dB/dec
Group delay pass band	50.8	55.5	60.1	ms
Group delay between pass- and stopband	69.7	76.3	82.8	ms

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4.5.2.8 ACC-xy Bandwidth LF3

F04_827

Table 78: ACC-xy Bandwidth LF3

ACC_xy	Min	Typ	Max	Unit
f_{PASSBAND}		2.5		Hz
f_{STOPBAND}		25		Hz
corner frequency	9.8	10.9	12.0	Hz
pass band ripple	-0.07	-0.05	0.00	dB
stop band gain	-53.1	-46.4	-33.9	dB
$f_{-50\text{dB}}$	21.9	24.3	26.7	Hz
$f_{-40\text{dB}}$	21.1	23.5	25.8	Hz
min. damping slope	-21.4	-21.4	-21.4	dB/dec
max. damping slope	-992.5	-990.0	-987.6	dB/dec
Group delay pass band	52.1	57.1	62.1	ms
Group delay between pass- and stopband	71.4	78.3	85.2	ms

4.5.2.9 ACC-z Bandwidth LF3

F04_829

Table 79: ACC-z Bandwidth LF3

ACC_z	Min	Typ	Max	Unit
f_{PASSBAND}		2.5		Hz
f_{STOPBAND}		25		Hz
corner frequency	9.8	10.9	12.0	Hz
pass band ripple	-0.07	-0.05	0.00	dB
stop band gain	-53.5	-46.6	-34.0	dB
$f_{-50\text{dB}}$	21.9	24.3	26.7	Hz
$f_{-40\text{dB}}$	21.1	23.5	25.8	Hz
min. damping slope	-21.4	-21.3	-21.2	dB/dec
max. damping slope	-991.1	-977.4	-963.6	dB/dec
Group delay pass band	52.3	57.7	63.2	ms
Group delay between pass- and stopband	71.6	78.9	86.1	ms

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4.5.2.10 YRS-xz Bandwidth LF4

F04_831

Table 80: YRS-xz Bandwidth LF4

YRS_xz	Min	Typ	Max	Unit
f_{PASSBAND}		5.0		Hz
f_{STOPBAND}		50		Hz
corner frequency	16.2	18.0	19.8	Hz
pass band ripple	-0.28	-0.23	0.00	dB
stop band gain	-41.5	-41.3	-27.2	dB
$f_{-50\text{dB}}$	n.a.	n.a.	n.a.	Hz
$f_{-40\text{dB}}$	44.8	49.7	54.7	Hz
min. damping slope	-14.4	-13.9	-13.4	dB/dec
max. damping slope	-550.4	-549.9	-549.4	dB/dec
Group delay pass band	23.2	25.2	27.2	ms
Group delay between pass- and stopband	24.3	26.4	28.6	ms

4.5.2.11 ACC-xy Bandwidth LF4

F04_833

Table 81: ACC-xy Bandwidth LF4

ACC_xy	Min	Typ	Max	Unit
f_{PASSBAND}		5.0		Hz
f_{STOPBAND}		50		Hz
corner frequency	15.7	17.5	19.3	Hz
pass band ripple	-0.29	-0.24	0.00	dB
stop band gain	-41.8	-41.7	-29.7	dB
$f_{-50\text{dB}}$	n.a.	n.a.	n.a.	Hz
$f_{-40\text{dB}}$	43.7	48.6	53.4	Hz
min. damping slope	-14.4	-14.4	-14.4	dB/dec
max. damping slope	-547.8	-542.7	-537.7	dB/dec
Group delay pass band	23.9	26.1	28.4	ms
Group delay between pass- and stopband	25.0	27.4	29.8	ms

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4.5.2.12 ACC-z Bandwidth LF4

F04_835

Table 82: ACC-z Bandwidth LF4

ACC_z	Min	Typ	Max	Unit
f _{PASSBAND}		5.0		Hz
f _{STOPBAND}		50		Hz
corner frequency	15.4	17.3	19.2	Hz
pass band ripple	-0.30	-0.25	0.00	dB
stop band gain	-43.1	-42.3	-29.7	dB
f _{50dB}	n.a.	n.a.	n.a.	Hz
f _{40dB}	43.5	48.5	53.4	Hz
min. damping slope	-14.4	-14.4	-14.3	dB/dec
max. damping slope	-545.0	-519.7	-494.4	dB/dec
Group delay pass band				
	24.1	26.8	29.5	ms
Group delay between pass- and stopband				
	25.3	27.9	30.6	ms

4.5.2.13 YRS-xz Bandwidth HF

F04_837

Table 83: YRS-xz Bandwidth HF

YRS_xz	Min	Typ	Max	Unit
f _{PASSBAND}		140.0		Hz
f _{STOPBAND}		1150		Hz
corner frequency	364.8	406.5	448.1	Hz
pass band ripple	-0.43	-0.36	0.00	dB
stop band gain	-40.6	-40.4	-26.9	dB
f _{50dB}	n.a.	n.a.	n.a.	Hz
f _{40dB}	1032.6	1148.0	1263.4	Hz
min. damping slope	-14.3	-13.9	-13.5	dB/dec
max. damping slope	-557.5	-551.2	-545.0	dB/dec
Group delay pass band				
	0.88	0.96	1.05	ms
Group delay between pass- and stopband				
	0.90	0.99	1.07	ms

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4.5.2.14 ACC-xy Bandwidth HF

F04_839

Table 84: ACC-xy Bandwidth HF

ACC_xy	Min	Typ	Max	Unit
f _{PASSBAND}		140.0		Hz
f _{STOPBAND}		1150		Hz
corner frequency	170.0	237.0	304.1	Hz
pass band ripple	-2.16	-1.42	0.00	dB
stop band gain	-57.6	-54.1	-38.4	dB
f _{-50dB}	n.a.	n.a.	n.a.	Hz
f _{-40dB}	910.4	1038.1	1165.8	Hz
min. damping slope	-13.2	-12.1	-11.1	dB/dec
max. damping slope	-318.6	-258.5	-198.3	dB/dec
Group delay pass band	1.17	1.48	1.80	ms
Group delay between pass- and stopband	1.14	1.34	1.54	ms

4.5.2.15 ACC-z Bandwidth HF

F04_841

Table 85: ACC-z Bandwidth HF

ACC_z	Min	Typ	Max	Unit
f _{PASSBAND}		140.0		Hz
f _{STOPBAND}		1150		Hz
corner frequency	81.2	152.0	222.7	Hz
pass band ripple	-6.20	-3.76	0.00	dB
stop band gain	-65.1	-60.1	-42.6	dB
f _{-50dB}	n.a.	n.a.	n.a.	Hz
f _{-40dB}	826.6	974.3	1122.0	Hz
min. damping slope	-12.1	-11.1	-10.2	dB/dec
max. damping slope	-249.6	-191.2	-132.7	dB/dec
Group delay pass band	1.4	2.2	2.9	ms
Group delay between pass- and stopband	1.3	1.4	1.6	ms

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4.5.2.16 Additional information

F04_844 Exact filter-frequency depends on the eigenfrequency of each yaw-rate sensor element. Comparing two parts the maximal difference can be the maximum minus the minimum eigenfrequency and filterparameter.

4.5.3 Noise

F04_846 The following table shows the yaw-rate (customer demands in brackets if not fulfilled).

Table 86: Yaw-rate

Parameter	Conditions	Ω_x	Ω_z	Unit
Noise	7Hz-Filter (LF3)	0.08 (?)	0.04 (?)	$^{\circ}/s_{RMS}$
Noise	15Hz-Filter (LF1, 4)	0.1 (0.03)	0.05 (0.03)	$^{\circ}/s_{RMS}$
Noise	60Hz-Filter (LF2)	0.15 (0.1)	0.1	$^{\circ}/s_{RMS}$
Noise	400Hz-Filter (HF)	0.75 (0.17)	0.75 (0.17)	$^{\circ}/s_{RMS}$

F04_849 The following table shows the acceleration (customer demands in brackets if not fulfilled).

Table 87: Acceleration

		SMI700	CMA	SMI710	CMA	
Parameter	Conditions	Ax	Ay	Ay	Az	Unit
Noise	7Hz-Filter (LF3)	2.5 (?)	2.5 (?)	2.5 (?)	2.75 (?)	mG_{RMS}
Noise	15Hz-Filter (LF1, 4)	3 (2)	3 (2)	3 (2)	3.3 (2)	mG_{RMS}
Noise	60Hz-Filter (LF2)	6 (5)	6 (5)	6 (5)	6.6 (5)	mG_{RMS}
Noise	400Hz-Filter (HF)	16 (13)	16 (13)	16 (13)	16 (13)	mG_{RMS}

4.6 Vibration robustness

F04_852 See document [03].

4.7 PLL

F04_5742 The PLL operates in 3 different main states:

1. Start-up:

First state is directly after the reset at start up, where the PLL tries to find the resonance frequency of the drive part of the yaw rate sensor. In this state the phase detector of the PLL detects the existing difference of frequency and phase between the frequency of the digital controlled oscillator of the PLL and the frequency of the drive frequency of the mechanical sensor. The DCO is controlled with this difference filtered by the PLL-loop filter.

This control value is limited only by the total possible frequency range of the drive frequency of the yaw rate sensor. Every individual yaw rate sensor has a fixed frequency, but it lies in a tolerance band of +/- 10 %. (The limits for the DCO frequency control values are calibrated during production test). This frequency range may vary +/- 10 % of the nominal drive frequency value. During this time the frequency change is not suitable for PSI communication; that is the reason, why the communication in this phase is not allowed via PSI-Interface.

The loop filter is set to a higher frequency to fasten the time until the PLL is in the locked state.

2. Locked-state:

After detecting the right frequency and phase the PLL is in the so called locked-state.

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The loop filter is set to lower frequency to ensure noise performance and stability.

During locked-state, the frequency constant is far below 1 % (~0,33%).

The frequency depends on the stability of the mechanical properties of the yaw rate sensor.

As the mechanical oscillator of the yaw-rate sensor has typically a quality of several thousands, this frequency is very stable over time and temperature.

The control value of the DCO is tracked by the PLL control logic.

3. Unlock-state:

If during normal operation of the PLL (State 2) a mechanical disturbance occurs, which leads to an unlocking of the PLL, the phase detector detects this unlocking and the PLL control logic limits the DCO control value around the last DCO value when it was locked.

This limit guarantees that the DCO will not shift more than 0,7 % from the frequency of the frequency of state 2. (Together with the 0,3% of the sensor it gives us the necessary 1% stability).

After the unlocking of the PLL two possibilities can occur:

a. Sensor is not damaged and the PLL will be able to go to lock state. Then State 2 is again reached. Communication over PSI is available during this time.

b. Sensor is damaged and PLL will not be able to reach lock state again. Yaw-rate signal will be not available. The DCO may drift over temperature. To guarantee the frequency stability of 1 %, the DCO holds only for max. of 0,5 sec with the specified temperature drift the necessary frequency stability. During this time PSI communication is still possible. After 0,5 sec in the unlocked state of the PLL, communication must be shut down, as frequency stability cannot be longer guaranteed.

4.7.1 Calculations for PLL reference frequency

F04_861 The following table shows a table of calculation with respect to PSI5 specification:

F04_862 **Table 88:** Calculations of PLL limits

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FA min.	20	MHz		20	MHz	
Relative temperature change	195	Kelvin		195	Kelvin	
Frequency change over temperature of CMG worst case	0,328	% +/-		0,328	% +/-	
DCO Limiter absolut	8	LSB +/-		7	LSB +/-	
DCO frequency shift/LSB	1,75E+04	Hz/LSB		1,75E+04	Hz/LSB	
DCO frequency shift/sec over temperature	995	Hz/sec		995	Hz/sec	
Max. hold time after PLL lock out (ROSE ACC operating time after PLL-lockout)	0,5	sec		0,5	sec	
	min	nom	max	min	nom	max
Frequency limits with above assumptions [MHz]	19,794	20,000	20,206	19,811	20,000	20,189
Deviation in %	1,030	0,000	1,030	0,943	0,000	0,943

F04_5824 Sensor will be configurated with DCO-Limiter 7 or less to fulfill 1% accuracy.

The following table gives the summary of the PIS5 tolerance calculation to achieve the required 1% absolute precision (0.1%).

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F04_864

Table 89: PSI Timing Estimations

Parameter/Conditions	Symbol	Min	Typ	Max	Unit
Sensor resonance frequency over all parts	F_cmg	22,5 -10	25 0	27,5 +10	kHz %
Single part variation sensor frequency over temperature and lifetime ³⁸		-0,328		+0,328	%
Absolute discretisation tollerance of PSI5 timer (see 3.10.9.3) = +/- 1 / (1024*f_CMG) ³⁹		-0,044		0,044	us
Total variation of PSI5 frequency with stable oscilation ³⁸		-0,328	0	+0,328	%
DCO stability after distortion or defect of rate element within 500ms ³⁹		-0,662		+0,662	%
Total variation of PSI5 frequency with unstable oscilation for 500ms ³⁹		-1		+1	%

F04_5911 ³⁸ Informative values. Balancing of tolerance chain possible during sample stages³⁹ +/-5% w/- calibration; w/o calibration +/-6% achievable

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5. Qualification requirements

5.1 Temperature profile

F05_868

Estimations for lifetime environmental validation plan:

F05_869

Storage time sensor

1 year (after delivery by AE-plant) plus storage time within AE-plant

temp. [°C]	-55 - 10	10 - 40	40 - 70
duration [h]	50	8660	50
total [h]	8760		

Storage time in ECU

15 years

temp. [°C]	-55 - -40	-40 - 10	10 - 30	30 - 70
duration [h]	50	500	130800	50
total [h]	131400			

Operating lifetime (i.e. with supply voltage turned on)*Non-ESPi applications (self-heating included)*

temp. [°C]	-40	-20	25	60	80	100	125/135
duration [h]	300	1500	3600	5100	3600	750	150
total [h]	15000						

ESPi (self-heating included)

temp. [°C]	-40 - -15	-10 - -5	0 - 40	45 - 75	80 - 90	100	120-140
duration [h]	250	1250	3000	4250	3000	625	125
total [h]	12500						

Non-operating lifetime in ECU (i.e. with supply voltage turned off)*Non-ESPi applications*

temp. [°C]	-40 - 20	20 - 40	40 - 60	60 - 80	80	80 - 135
duration [h]	73656	26784	20088	12053	1339	0
total [h]	133920					

ESPi

temp. [°C]	-40 - -30	-30 - -20	-20 - 25	25 - 30	30 - 60	60 - 80	80-100	100-120	125-140
duration [h]	2390	11890	31033	70686	1440	1011	215	235	0
total [h]	118900								

External customers

temp. [°C]	-55 - -25	-25 - 50	50 - 85	85 - 135
duration [h]	20298	78804	20283	0
total [h]	119385			

Figure 53: Lifetime requirements ³²F05_5913 ³² Non-ESPi applications: 17years lifetime (148920h) including 15.000h operating time

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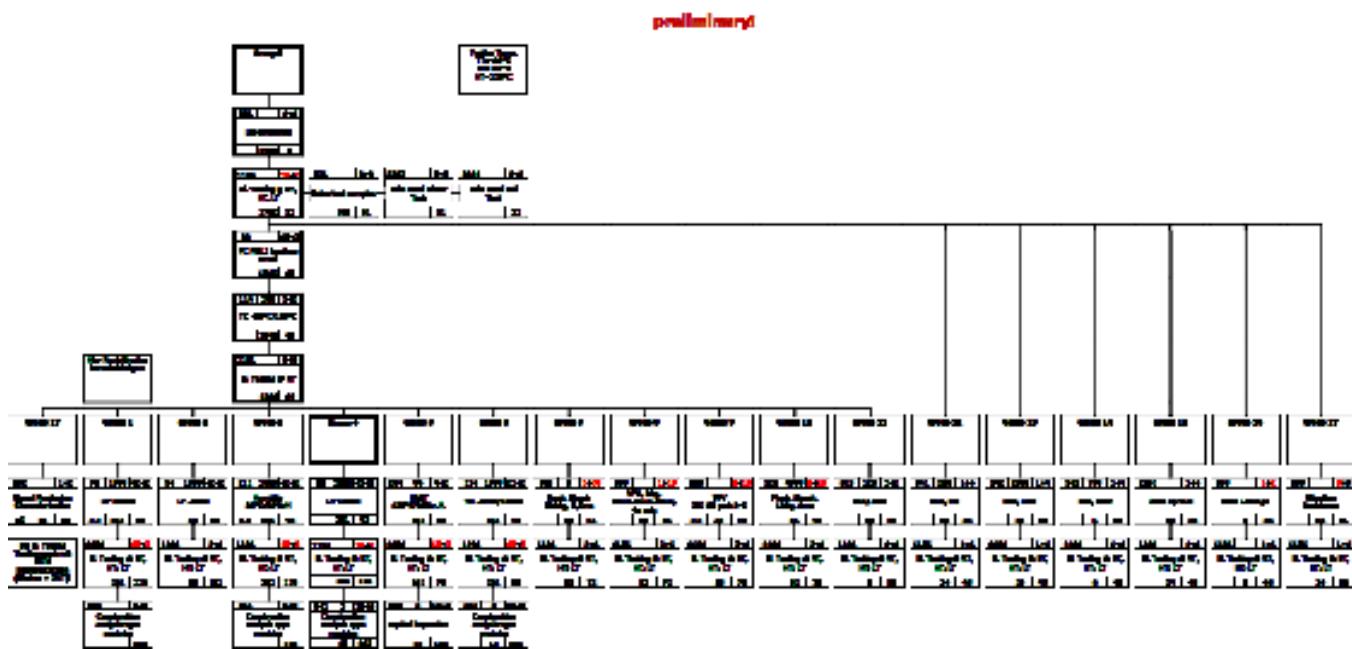
ESPi: 15years lifetime (131400h) including 12.500h operating time

For lifetime testing, the worst-case temperature of the respective temperature range is to be used (e.g. 100°C-120°C -> 120°C)

F05_9393 AEC-Q100 Rev. G Validation Plan for C-Samples

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5.2 EMC / ESD

F05_5914 Test plan development based on BISS (V 1.2 / 15. November 2007)

Failure criteria:

- Rate offset-change > 1°/s (300°/s full scale)
- Acceleration offset-change > 50mg (5g full scale)
- Upcoming status-flags
- function class A filter setting LF 60Hz (LF1) & HF 400Hz for rate and acceleration

Complete test plan can be found here: [16]

5.2.1 Testplan - direct power injection

F05_886 Specification/Release criteria:

0,15MHz - 1 GHz

Modulation:

CW and AM (60Hz) < 800MHz

GSM(217Hz 12.5%) > 800Mhz

Measurements from 1GHz to 3.2GHz for evaluation and Data collection on Immunity for High frequency EMC

Step size:

Frequency Range	Frequency Step
100kHz - 1MHz	10kHz
1MHz - 10MHz	100kHz
10MHz - 100MHz	1MHz
100MHz - 1GHz	5MHz

F05_9413 Details see test plan [16].

5.2.2 Test plan conducted emission

F05_888 VBAT (150 Ohm/1Ohm) 0,03MHz - 1GHz

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Measurement of other pins will be performed but not evaluated for release
Details see test plan in [16]

5.2.3 Test plan μTEM

F05_890 μTEM Method (immunity), 2 orientations
0.1MHz-2GHz, 800V/m
μTEM Method (emission), 2 orientations
0.003MHz-1GHz, 12dB μ V
Details see test plan in [16]

5.2.4 ESD

F05_892 Sensor without external circuitry (BGA - pure module, 1st level package):
HBM 4kV for all PSI5 Pins incl. VB (1.5k, 100pF)
HBM 2kV for all other Pins (1.5k, 100pF)
MM 200V and Charakterization of 250V
CDM 500V (750V corner pins if available)
F05_9389 Sensor with proposed external circuitry (as defined by specification, 2nd level package - MM7)
HBM 8kV PSI5 Pins (330Ohm, 150pF), measurement on test board
HBM 15kV PSI5 Pins (Air - ESD Gun Test) - not reasonable on test board level - to be tested with ECU

5.3 Qualification and environmental test requirements

5.3.1 Nissan requirement

F05_5915 SMI7xx will fulfill nissan reliability qualification guideline [19] for semiconductor device for **class I (Temperature Cycles according coffin manson)**.
SMI7xx acceleration channels will fulfill Nissan guideline [20] for acceleration sensors.
Validation tests for group G1, G2, G3, G4 and G5 will be done for acceleration channels. Interpretations of the tests will be done for yaw-rate. All results will be documented.
Alternative tests for better testing can be used as substitute if they are agreed with CC. Sensor characteristics will be proved by BIST during power-on phase.
F05_9391 TC-Nissan-Requirement (500 Zyklen -55°C bis 150°C) uses 5°C lower temperature than AEC-Q100 (1000 Zyklen -50°C bis 150°C). From technical point of view, AEC-Q100 demands exceed Nissan demands. Therefore no additional Nissan-Qualification necessary.

5.3.2 Additional temperature change test

F05_5916 To check if the sensor does not have sporadic faults the following tests will be fulfilled (number of parts >= 24):

- -40°C/125°C; 2.5K/min; 800cycles Temperature Cycles with **active** monitoring of error status flags, acceleration and rate
- Storage at 135°C with **active** monitoring of error status flags, acceleration and rate
- Storage at -40°C with **active** monitoring of error status flags, acceleration and rate

For all tests acceleration and rate will be evaluated against special limits to react on external sources of disturbance from the measurement equipment.
Necessary cycles/hours, limits and flag-limits will be estimated within an testrun before A-Sample-Validation.



6. Customer Models

F06_908 The following table shows customer-models that will be provided during development.

F06_909 Table 90: Customer models that will be provided during development

	Digital Model (EDIF)	System Simulation Model (fast DLL)	System Simulation Model (complex DLL)
A-Sample	Yes, A-Si net list	Yes	No
B-Sample	Yes, B-Si net list	Yes, with adaptations if necessary	Yes
C-Sample	Yes, C-Si net list	Yes, with adaptations if necessary	Yes
Remarks	<ul style="list-style-type: none"> * New net lists for each new SPI-Implementation needed * net lists needed at tape-out 	<ul style="list-style-type: none"> * Focus on fast calculation 	<ul style="list-style-type: none"> * Focus on detailed modeling

F06_9389 The sensor models will be developed and verified according to the NE4-EHB (Entwicklungshandbuch), CMMI-L3.

The model release includes a peer review with experts as well as the verification of the model against measurements with samples. Every model is delivered including documentation concerning model content, verification and restrictions of use.

6.1 EDIF net lists (comment only; no legal agreement)

F06_5950 Use: For sensor emulation in system integration tests like HIL (HW in the loop) or SW-releases.

Spec: EDIF-description to be assessed in cooperation with system test engineer during ASIC development. (complexity and expenditure comparable to TIG580 EDIF net list).

All (field-) relevant SPI commands have to be implemented, especially

- Part and device numbering
- Error flags and counters
- ...

Responses have to be identical to all possible sensor configurations

All output channels have to be implemented (i.e. HF, LF, temperature ...)

Details must be agreed as soon as complete SMI7xx SPI instruction set is available.

6.2 Customer system simulation model (fast)

F06_5951 Use: For sensor emulation in airbag algorithm development.

Spec:

- Interface with VDA-AK interface
- File format: *.dll (OEM use possible)
- Additional file format: simulink (internal use only)
- **Calculation speed: simulation time will be 5 times faster than signal duration (e.g. 20ms calculation time for 20ms input data) / improvement factor 50 not possible.**
- No timeout limitation for very long input data streams (**up to 1 minute**)
- Model verification with experiments; set of experiments to be assessed with system engineering
- Model comparison to detailed system simulation model
- **(comparison between fast and complex implementation of the customer model at B- and C-sample status; not at A-sample status)**



- Description of validity range of the model, description of sensor performance out of this validity range (**verbal description in customer model documentation**)
- Customer documentation to be provided
- **Main low pass filter should be implemented not exactly as in real world (e.g. filter order will be implemented correctly; rounding errors not)**
- Total signal delay should be modeled to a precision of at least 5%

The model (which is in responsibility of AE/EST4) includes models of the ASIC, which to be contributed by and in responsibility of AE/EIS2.

6.3 Customer system simulation model (detailed)

F06_5952 Use: For reference calculations / for comparison with fast system simulation model.

Spec:

- Interface with VDA-AK interface
- File format: *.dll (OEM use possible)
- Additional file format: simulink (internal use only)
- Calculation speed: no requirement
- No timeout limitation for very long input data streams (**up to 25 sec**)
- Model details according to VDA-AK
- Model verification with experiments; set of experiments to be assessed with system engineering
- Description of validity range of the model, description of sensor performance out of this validity range (**verbal description in customer model documentation**)
- Customer documentation to be provided
- Sensor parameters must be adjustable with given min/nom/max (**analog VDA-AK**) values for all parameters

The model (which is in responsibility of AE/EST4) includes models of the ASIC, which to be contributed by and in responsibility of AE/EIS2.

Vibration sensitivity (mechanical (micro machined sensor, sensor housing) and electrical; clipping and saturation effects) will not be modeled because it is not possible to be covered on the level of customer simulation models.



7. Safety concept

7.1 Introduction

F07_975 In section 2 the safety goals and functional safety requirements as defined by CC/PJ-SMI7 in the concept phase are documented [100503_SMI7xy_Safety_Concept_v1_0.pdf and CR007]. Any future changes in these requirements will be dealt with using the change request procedure used for all SMI700 change requests. Section 2 also contains some definitions. Section 3 describes the chosen safety architecture concept. In section 4 the technical details of the safety concept are described (monitor functions and flags, error counters and error memory). Section 5 refers to the metrics forecast and section 6 specifies the criteria for safety validation of SMI700. Section 7 describes the flexibility and the validity of the safety concept.

7.2 Definition of functional safety requirements for safety goals

7.2.1 Definition of safe state

F07_5954 The safe state is the state a sensor may go to, if any safety criterion is violated. There are four states possible:

- a) status flag set for corresponding channel
- b) wrong checksum for response
- c) no response
- d) for CAN application using the WDGI output, a missing WDGI is considered a safe state, as well as a wrong CAN clock.

Wherever possible, a) will be used.

7.2.2 Definition of errors

F07_5955 Errors are defined by the customer as follows:

In general an error is present if the sensor does not comply with its specification concerning Top Events. Errors are indicated within the fault tolerant time interval if any of the given Top Events (column "error (E)") has occurred. The critical error modes are offset jumps, freezes and drifts, sensitivity, signal delay and noise errors. The following table specifies the error modes more precisely. The table should be read as follows:

The allowed residual failure rate which leads to an error E may not be higher than R. The single point failure metric to detect a fault within the time T must be higher than SPFM. Systematic faults must be avoided according to an ASIL X.

F07_987

Table 91: Definition of errors

signal/function	error (E) / Top Event	time (T)	failure rate (R)	single point failure metric (SPFM)	Latend point failure metric (LPFM)	ASIL (X) ⁽⁴⁾
rate (wx,wy,wz) ⁽²⁾	Any of the faults below	as below	1e-8/h	90%	60%	-
	offset jump >3°/s	18ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾
	Offset freezed	18ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾
	Offset drift >2.8°/s / s	18ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾

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	sensitivity error >+7% or <-5%	18ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾
	Signal has wrong sign	18ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾
	Phase delay up to $f_{3dB} > 120\text{ms}$	18ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾
	Noise (Peak to Peak) > 12°/s	100ms	1e-8/h	90%	60%	ASIL D* ⁽⁵⁾
acceleration (ax,ay,az) ⁽²⁾	Any of the faults below	as below	1e-8/h	90%	60%	-
	Offset jump >2m/s ² (~0,2g)	18ms	1e-8/h	90%	60%	ASIL B (D)
	Offset freezed	18ms	1e-8/h	90%	60%	ASIL B (D)
	Offset drift >0.1m/s ² / min	18ms	1e-8/h	90%	60%	ASIL B (D)
	sensitivity error >+12% or <-20%	18ms	1e-8/h	90%	60%	ASIL B (D)
	Signal has wrong sign	50ms	1e-8/h	90%	60%	ASIL B (D)
	Phase delay up to $f_{3dB} > 420\text{ms}$	18ms	1e-8/h	90%	60%	ASIL B (D)
	Noise (Peak to Peak) > 600mg	50ms	1e-8/h	90%	60%	ASIL B (D)
acceleration and rate ⁽³⁾	Any acceleration faults and any rate fault	as above	5e-10/h	99%	90%	ASIL D* ⁽⁵⁾

F07_5958

(2 Requirement valid for all axes since sensors may be mounted in all axes (ESPi, CSC, others)

(3 A fault of a rate channel and any of both acceleration channels should be considered

(4 This means, systematic faults must be avoided according to this ASIL level

(5 ASIL D*: "Entwicklung in Anlehnung an ASIL D" (CR 087)

F07_5956

In addition, the customer specified HW metrics for the transfer of data from the SPI-Master to the CAN or PSI interface as follows:

In SPI master operation, the sensor reads as SPI master data of another device, possible transforms the data and outputs it on another interface. For safety critical signals, the reading, processing and transmitting of the data must not be corrupted. There is currently no defined application, so the following definition is out of the context and gives the best guess of future safety targets.

Error: any bit flip or error in internal calculation

Fault tolerant time span: 1ms

Safe state: internal uC (software) notification that a fault has occurred

ASIL: ASIL D* (see comment in {REF:F07_5958})

Failure rate: 1e-9/h

SPFM: 99%

LPFM: 90%

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7.2.3 Definition of fault tolerant time interval

F07_1001 The target fault tolerant time interval (error detection time) is measured from the time, when the error criteria is superseded until the sensor is brought into any of its save states. The timing is depicted in the following figure.

F07_1002

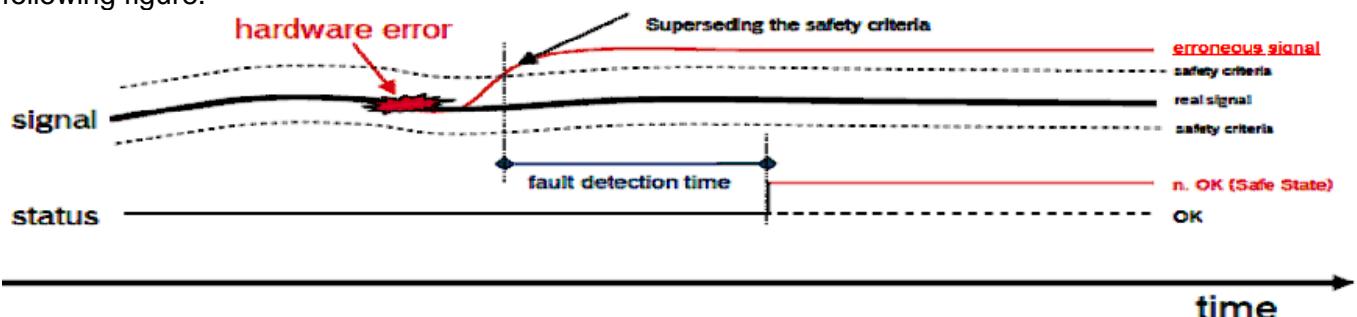


Figure 54: fault tolerant time interval

7.3 Safety architecture concept

F07_9994 This chapter will give a comprehensive architectural view on the SMI7xy scope. It does not focus on the functional design of and functional interactions between the different building blocks, but focuses on their relation to safety topics.

Capital descriptors are the unique identifiers of the SMI7xy scope which will be used in the safety analysis and metric calculation.

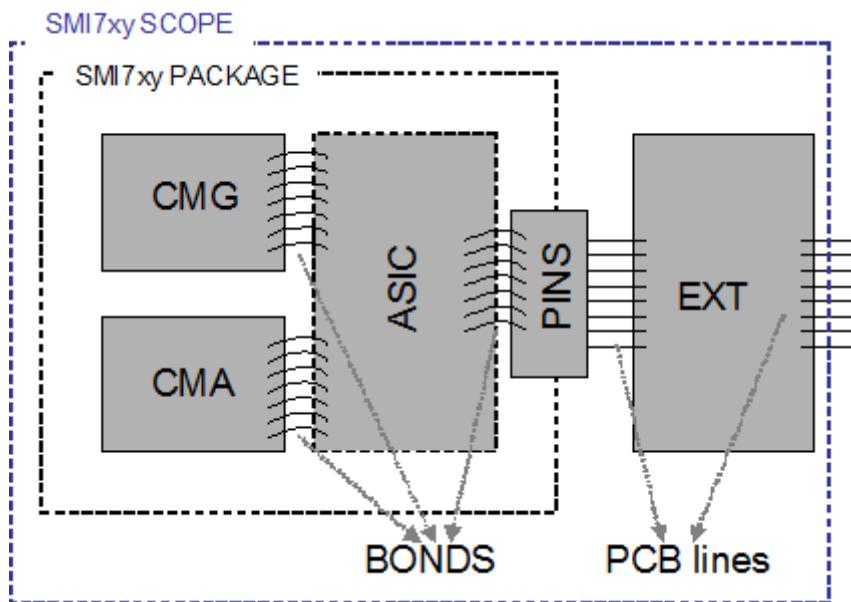
Atomic building blocks are visualized with a solid border line whereas building blocks consisting of sub blocks are marked with a dashed border line. For each atomic building block the failure modes used in the hardware metric calculations are described.

The function of transmitting data between different blocks is assigned directly to the different blocks themselves. The interfaces between blocks do not exist as own distinct blocks. Some interfaces are shown for the main signal path interfaces but not all interactions from blocks to blocks can be shown in this architectural overview.

F07_10161 In the following, the architecture will be described in detail. The failure mechanisms considered in the metrics calculation and their effect on the Top Events in {REF:F07_987} is described, as well as the assumed monitoring mechanisms which are described in detail in {REF:F07_142}.

7.3.1 System architecture overview

F07_9996 The following figures give an overview of the SMI7xy safety scope:



F07_6121 The SMI700 consists of the following signal paths:

- Angular Rate (W_x , W_y or W_z depending upon module configuration and orientation)
- Acceleration 1 (x, y, or z low g depending upon configuration and orientation)
- Acceleration 2 (x, y, or z low g depending upon configuration and orientation)

Each channel is evaluated with low-frequency filters (selectable) and a high frequency filter (see {REF:F04_4255}) intended for high-g applications.

Each signal path originates in its own micromechanical sensor structure, the acceleration sensor elements are both on the same chip (CMA); the angular rate sensor element is a separate chip (CMG). All micromechanical sensor elements are connected to one and the same ASIC using wire bonds (BONDS).

F07_9997 The SMI7xy scope consists of the SMI7xy package and the external circuitry as defined in the application descriptions. The Printed Circuit Board (PCB) lines are assumed to be non destructable and are not considered within the safety scope of the SMI7xy.

The external circuitry (EXT) stands for all external components as resistors, capacitances and the quartz as given in the application descriptions. The SMI7 package consists of the pins (PINS) connecting the package to the PCB, the integrated circuit (ASIC) and the micromechanical elements (CMA, CMG). All components are connected together with BOND connections.

The package itself is not considered explicitly in the following but its influence on the different elements is taken into account.

F07_9492 Safety-related Software will be developed according to ASIL D* (CR087).



7.3.1.1 CMG

F07_9998 The CMG block is the micromechanical element to measure rate. A moving core is placed inside a hermetically sealed package. There are three failure modes:

F07_10011 CMG_PARTICLE:

This failure mode describes a particle which is inside the cavity, might touch or stuck the moving parts, which may lead to signal deviations.

F07_10012 CMG_SPRING:

This failure mode describes that a spring of the core is broken or damaged. A damaged spring might lead to signal deviations.

F07_9999 CMG_LEAK:

This failure mode describes a leakage within the cavity. The leakage leads to an variation of the inside pressure and damping characteristics which may lead to a signal deviation.

F07_10013 All three failure modes may have impact on the yaw rate offset, sensitivity and noise.

F07_10014 Monitoring is mainly done via monitoring

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_drv_pi_tol, yrs_pll_unlock, yrs_pll_lim, yrs_drv_adc_mean),
- the voltage the common mode voltage (yrs_rate_V_com)
- the operation point of the Quadrature controller (yrs_quad_I_tol).

F07_10015 The monitoring of the CMG is possible since the yaw rate detection circuit is a closed circuit with feedback to the CMG, such that failures somewhere in the loop will be detected by several monitors. Therefore, a good diagnostic coverage can be guaranteed for the CMG.

7.3.1.2 CMA

F07_10017 The CMA block is the micromechanical element to measure acceleration in two directions. Two cores are packed within one package. It has the following five failure modes:

F07_10018 CMA_LEAK:

This failure mode describes a leakage within the cavity. The leakage leads to an variation of the inside pressure and damping characteristics which may lead to offsets or sensitivity deviations of the acceleration. Since both cores are packed within the same cavity, this failure mode affects both cores.

F07_10019 CMA_CORE1PARTICLE, CMA_CORE2PARTICLE:

This failure mode describes a particle which is inside the cavity, might touch or stuck the moving parts and may influence acceleration offset and sensitivity.

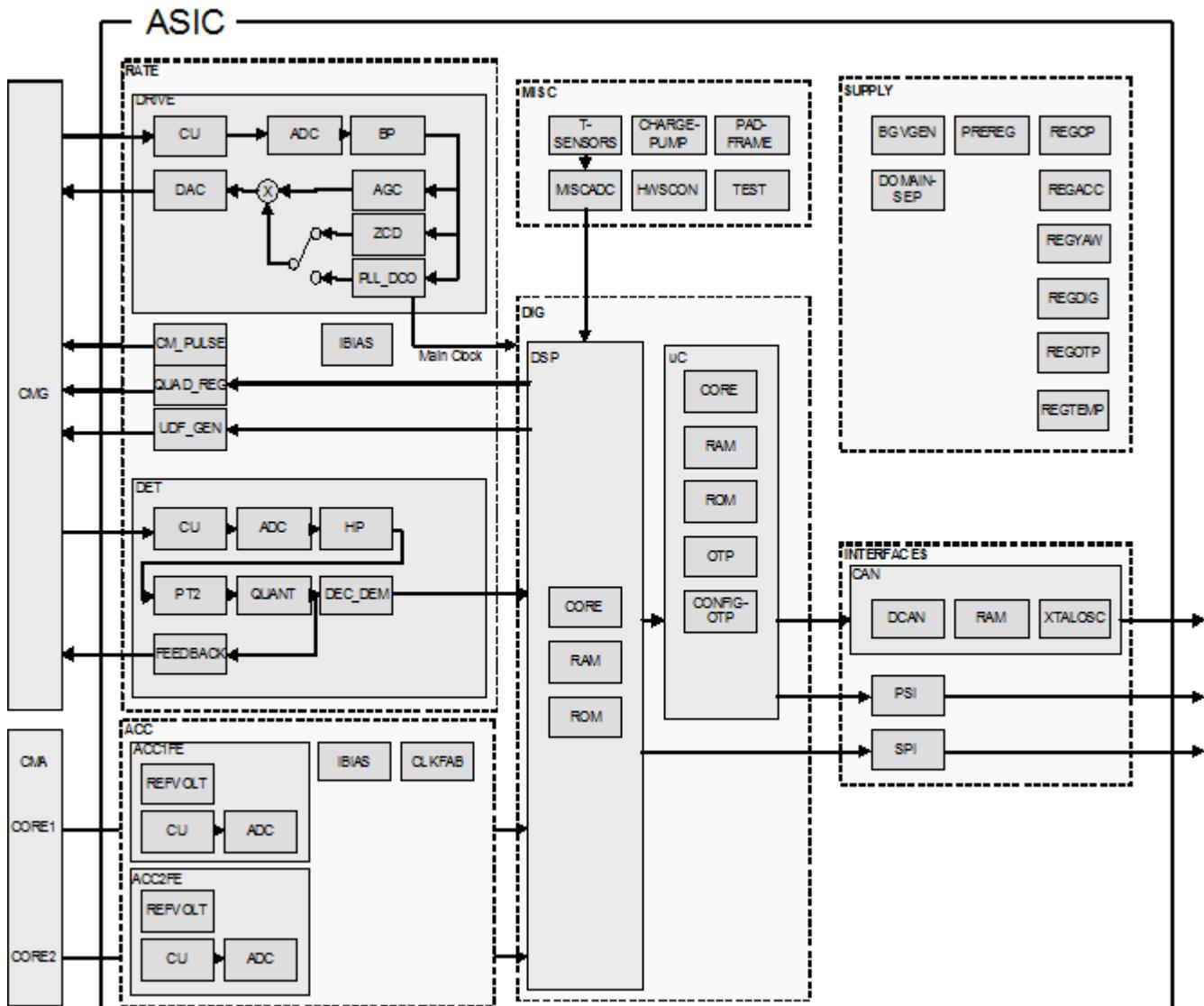
F07_10020 CMA_CORE1BROKENMECH, CMA_CORE2BROKENMECH:

This failure mode describes that a spring of the core or the CMA itself is broken or damaged. A damaged spring may influence acceleration offset and sensitivity, similar to a broken CMA because of changed ohmic resistances of the connection lines within the CMA.

F07_10021 Due to the extremely high requirements concerning vibration robustness of the sensor, the sensor is strongly damped. This prevents the implementation of a continuously running self test including mechanical excitation of the sensor at frequencies outside the required band width. Without such kind of test, it is not possible to distinguish between an external acceleration and a failure within the sensor. Some severe CMA failures can be detected via DSP limiters (dsp_acc1/2_HF/LF/in); any further monitoring needs to be done externally by plausibilization versus the external conditions (e.g., a second acceleration sensor).

7.3.1.3 ASIC

F07_10022 The following figure gives an overview of the modules within the ASIC:



F07_10023 The ASIC consists of the main signal path for rate and acceleration. The micromechanics is controlled by the analog frontends for the angular rate (RATE) and the acceleration (ACC) sensor element which are converting the signal to a digital signal.

The digital part (DIG) consists of the main signal processing capabilities and is responsible for the whole control of the sensor and parts of the interfaces.

The interfaces (INTERFACES) transmit the sensor data as master or slave to the outside.

The supply power of the ASIC modules is regulated and controlled by different voltage regulators (SUPPLY).

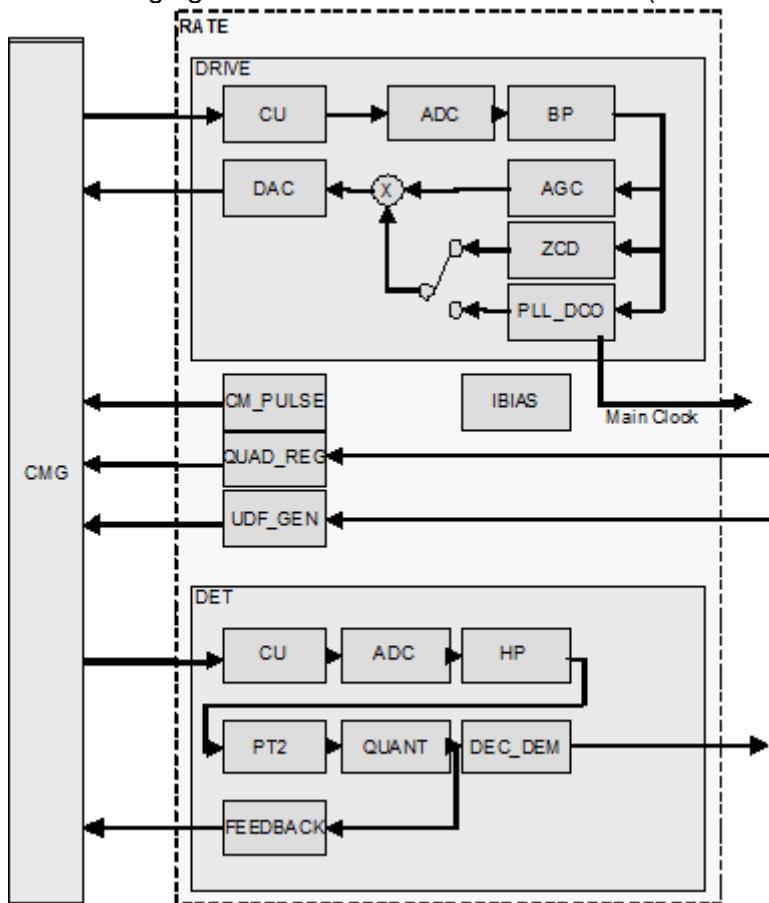
A remaining part of the ASIC (MISC) consists of additional control and test logic, safety functions, the charge pump and the temperature sensors.

The modules are complex integrated circuitry. Failures could exist in connections, gate oxides or resistors and capacitances. No distinct failure modes are distinguished for these atomic blocks, but the effects of malfunctioning of each block is considered.

All modules will be described in detail below, including the effects of failures in these blocks.

7.3.1.3.1 ASIC_RATE

F07_10040 The following figure shows the rate frontend block (and the CMG):



F07_10041 The Rate frontend consists of an amplitude control loop (AGC), a phase-locked loop (PLL) for clock recovery of the ASIC's main clock from the micromechanical oscillator (CMG), and an electromechanical delta-sigma loop to measure the Coriolis force using force feedback to the sensor element.

Amplitude control is realized by measuring the capacitance change at the drive electrodes, i.e. the displacement of the mechanical oscillation, using C/V conversion (CU) and adjacent A/D conversion (ADC). Any offset of the time discrete, quantized signal is cancelled by a band-pass filter (BP) without introducing phase delay in the signal band around 25kHz. In the AGC block, the amplitude of the sinusoidal drive signal is extracted and the amplitude offset with respect to the reference value is compensated by a PI controller. The controller value is finally modulated again with the drive frequency (from PLL) and applied to the sensor element by multiplication of a DC voltage offset to an AC rectangular voltage (DAC) driving the mechanical oscillator in terms of an electrostatic force.

Clock recovery during start-up and normal operation is done by the PLL. Phase/frequency offsets are calculated by sinusoidal multiplication and adjacent low-pass filtering of the drive signal with a reference signal from the digitally controlled oscillator (DCO). The phase error is compensated by a PI controller driving the DCO.



The zero-crossing-detection unit (ZCD) is a backup solution for start-up clock recovery inherited from former yaw rate sensor generations. In such a backup configuration, during start-up, clock recovery is done by a hit-and-count algorithm. The oscillation period of the sinusoidal drive signal is obtained by counting the high-frequency clocks at 400kHz between two rising zero crossings of the signal. During this phase the DCO on the ASIC is kept at a fixed frequency. At certain amplitude of the drive signal, clock recovery is then switched to the PLL. The ZCD unit is disabled by default and does not influence the safety concept.

The delta-sigma loop of the detection unit captures the capacitance change, i.e. the displacement, of the Coriolis structure of the mechanical sensor element (CU). It is quantized by an A/D converter (ADC) and filtered to the desired transfer function by high-pass (HP) and band-pass filters (PT2). The feedback signal is reduced in quantization by a 4 Bit quantizer (QUANT), whereas this quantization is spread over time using pulse-width modulation in the feedback D/A converter (FEEDBACK). This results in a linear electrostatic force at the sensor element.

Additional components cover measurement pulse generation as the input voltage of C/V conversion (CM_PULS), force generation to compensate the quadrature error (QUAD_REG) – the crosstalk from drive to Coriolis displacement by non-ideal springs, and force generation used for electrostatic spring-softening in the Coriolis structure (UDF_GEN) to match the frequency of the Coriolis oscillator to the drive oscillator, which results in optimal suppression of quantization noise in the delta-sigma loop.

The failure effects of these blocks are:

F07_10042 All RATE_DRIVE blocks:

Malfunction may affect offset, sensitivity and noise of the yaw rate.

F07_10043 All RATE_DET blocks:

Malfunction may affect offset, sensitivity and noise of the yaw rate.

F07_10044 RATE_IBIAS:

Malfunction may affect offset, sensitivity and noise of the yaw rate.

F07_10045 RATE_CM_PULSE:

Malfunction may affect offset, sensitivity and noise of the yaw rate.

F07_10046 RATE_QUAD_REG:

Malfunction may affect offset, sensitivity and noise of the yaw rate.

F07_10047 RATE_UDF_GEN:

Malfunction may affect offset, sensitivity and noise of the yaw rate.

F07_10048 Monitoring of the DRIVE path is mainly done via monitoring

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_drv_pi_tol, yrs_pll_unlock, yrs_pll_lim, yrs_drv_adc_mean),
- the special CU and ADC gain test (overlaid pulse with 1/32 of the sensor frequency, flag yrs_drv_cu_gain),
- the undervoltage detection of the charge pump (see flag v_cp_low)
- the quadrature controller (see flag dsp_quad_QI_lim),
- a possible overload of the drive ADC (see flag yrs_drv_adc).

F07_10050 Monitoring of the DET path is mainly done via monitoring

- the limiter of the PT2 filter (see flag yrs_rate_pt2_lim),
- a possible overload of the quantizer (see flag yrs_rate_quantizer),
- the mean rate (DC level, operating point) of CU and ADC stage (see flag yrs_rate_adc_mean),
- the voltage at the TN electrode (see flag yrs_rate_V_TN),
- the feedback force (see flag yrs_rate_V_fb),
- a possible overload of the rate detection ADC (see flag yrs_rate_adc)
- the common mode (CN_CP) voltage (see flag yrs_rate_V_com).

F07_10051 Monitoring of the CM_PULSE module is mainly done via monitoring

- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_pll_unlock),
- the undervoltage detection of the charge pump (see flag v_cp_low),
- the quadrature controller (see flag dsp_quad_QI_lim),



- the UCM-voltage, measuring the pulse on CM (see flag yrs_rate_V_CM).

F07_10052 Monitoring of the QUAD_REG module is mainly done via monitoring

- the operation point of the Quadrature controller (see flag yrs_quad_I_tol),
- the undervoltage detection of the charge pump (see flag v_cp_low).

F07_10053 Monitoring of the module UDF_GEN is mainly done via monitoring

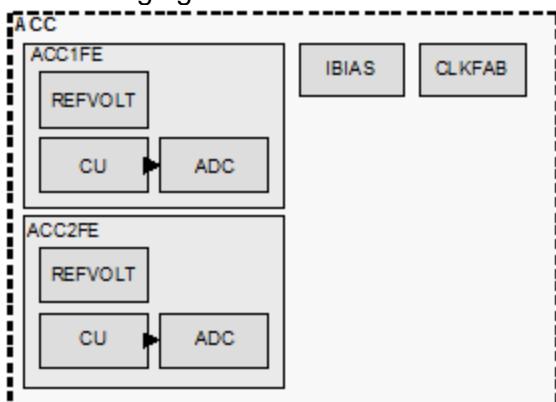
- the voltage at the TN electrode (see flag yrs_rate_V_TN).

F07_10054 Monitoring of the IBIAS module is mainly done via monitoring

- the drive force necessary to obtain the goal oscillation amplitude (see flag yrs_drv_pi_tol),
- the CU and ADC gain test (see flag yrs_drv_cu_gain),
- the drive phase and amplitude (see flag yrs_pll_unlock),
- the operation point of the Quadrature controller (see flag yrs_quad_I_tol),
- the deviation from required quadrature (0°/s) (see flag yrs_quad_HF_tol),
- the voltage at the TN electrode (see flag yrs_rate_V_TN),
- the feedback force (see flag yrs_rate_V_fb),
- the UCM-voltage, measuring the pulse on CM (see flag yrs_rate_V_CM).

7.3.1.3.2 ASIC_ACC

F07_10028 The following figure shows the acceleration frontend block.



F07_10032 The acceleration frontend contains a bias current generation (IBIAS) and a separate block (CLKFAB) which derives the ACC frontend clock from the yaw rate clock (generated by the DCO, see below). There are two signal processing parts (ACC1FE, ACC2FE) which transform the micromechanic deflection into a digital value.

First, the capacitance in the ACC core (which depends on the acceleration-induced deflection) is converted to a voltage signal (CU) before being converted into a digital signal by a sigma/delta convertor (ADC). Two individual reference voltages (REFVOLT) are being used to guarantee a good functioning of the transformation of the capacitance into a digital value.

The ACC FE functions within spec in the frequency range of 133,3kHz +/- 15%. Therefore, short-time frequency changes (including an unlocking of the Yaw rate PLL) do not influence the ACC FE, hence, these flags are not related to ACC functionality (see {REF:F04_5742}).

The failure effects of these blocks are:

F07_10033 IBIAS:

Malfunction may affect offset, sensitivity and noise of both acceleration channels.

F07_10034 CLKFAB:

Malfunction may affect offset, sensitivity, sign and noise of both acceleration channels.

F07_10035 ACC1FE_CU, ACC2FE_CU:

Malfunction of ACC{1,2}FE CU may affect offset, sensitivity and noise of acceleration channel {1,2}.

F07_10036 ACC1FE_ADC, ACC2FE_ADC:



Malfunction of ACC{1,2}FE_ADC may affect offset, sensitivity, sign and noise of acceleration channel {1,2}.

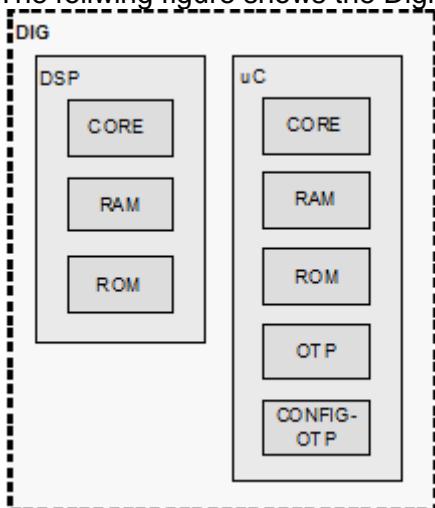
F07_10037 ACC1FE_REFVOLT, ACC2FE_REFVOLT:

Malfunction of ACC{1,2}FE_REFVOLT may affect offset and noise of acceleration channel {1,2}.

F07_10038 Monitoring of the reference voltage and the bias is done via the monitoring of the voltage used to evaluate the capacitive changes of the CMA (acc1_V_cm, acc2_V_cm). The ADC is monitored by a bit train monitor detecting an implausible sequence of zeros or ones (acc1_ds_lim, acc2_ds_lim). In addition, large signal peaks (which may be real, but may also be an indicator for an ADC malfunctioning) can be detected with an "energy flag" (acc1_overload_det, acc2_overload_det) which integrates the signal for a given time. These flags are no failure flags but indicator flags only.

7.3.1.3.3 ASIC_DIG

F07_10056 The following figure shows the Digital block:



F07_10057 The digital block consists of the Digital Signal Processor (DSP) and the Microcontroller unit (uC).

In the DSP module, the yaw rate and acceleration signals as well as the temperature signals are being calibrated and filtered. This is done by the DSP CORE using the filter code in the ROM and calibration and configuration data stored in the RAM (set by the boot loading process).

In addition, the temperature signal is calibrated.

Acceleration1, Acceleration2 and the Yaw Rate are filtered in two ways:

- with a ~400Hz ("high frequency") low pass filter
- with a configurable low pass filter (7 to 60Hz, "low frequency"), resulting in two signals each (..._HF, ..._LF).

In addition, the quadrature controller of the yaw rate path is located in the DSP.

The uC module consists of the uC Core and several memory blocks:

- ROM (software code and default settings)
- RAM (used as temporary memory during execution of the software routines)
- OTP including the CONFIG-OTP block (used for additional software code and calibration/configuration data).

In the uC module, several software routines are implemented:

- some services only being used during manufacturing (help functions) which are password-protected and which are not safety relevant
- the Boot Loader service which transfers OTP configuration and calibration data into the front ends, the DSP, the interfaces and the uC RAM
- the SW-SCON including



- the generation of several flags
- the debouncing of the flags and setting of the general status flag, including the writing of the failure
- PSI and CAN software.

The tasks are dealt by a scheduler with a timing raster of 500µs.

For SPI slave applications, the acceleration and yaw rate signals are not modified by the uC, but are directly transferred to the SPI module.

For CAN and PSI applications, the signals are passed via the uC to the PSI and CAN modules.

The failure effects of the DSP and uC modules are:

F07_10058

DSP_CORE, DSP_RAM, DSP_ROM:

Malfunction may affect offset, sensitivity, sign, phase and noise of both acceleration channels and the yaw rate channels.

F07_10059

uC_CORE, uC_RAM, uC_ROM, uC OTP, uC_CONFIG-OTP:

Malfunction may affect offset, sensitivity, sign, phase and noise of both acceleration channels and the yaw rate channels in case of PSI and CAN applications (not in SPI slave only applications)

F07_10060

Monitoring of the DSP_CORE module is mainly done via monitoring

- the DSP online test (answering of test requests triggered by the µC software, see flag `dsp_online_test`),
- the program flow via checking the signature of program code (see flag `dsp_pe_sign_err`)
- the validity of the registers internal to the DSP via parity check of all registers (see flag `dsp_pe_flag_err`)
- the interrupt module within the DSP (see flag `dsp_pe_irq_err`)
- diverse limiters in the signal pathes of ACC1_LF, ACC1_HF, ACC2_LF, ACC2_HF, RATE_LF, RATE_HF, Quadrature, Temperature
(see `dsp_..._in-flags` at the input of the DSP,
see `dsp_..._adjust-flags` after calibration,
see `dsp_..._out-flags` at the output of the DSP)

F07_10061

Monitoring of the DSP_RAM module is mainly done via monitoring

- the parity within each RAM cell (see flag `dsp_pe_ram`)
- the RAM address decoder (see flag `dsp_ram_soaf_err`)
- structural tests of the RAM cells (see flag `dsp_ram_ifa13_err`)
- the additional checksum test of the RAM cells containing configuration or calibration data (see flags `dsp_adjust_data_err`, `dsp_fine_err`)

F07_10062

Monitoring of the DSP_ROM module is mainly done via monitoring

- the CRC check of the ROM (see flag `dsp_rom_crc`)

and most flags that are used for the DSP_CORE.

F07_10063

Monitoring of the uC_CORE module is mainly done via monitoring

- the uC online test (answering of test requests triggered by the HW SCON module, see flag `uc_watchdog_err`)

In addition, a malfunctioning of the uC_CORE will be visible in a malfunction of the CAN or the PSI communication (in CAN resp. PSI applications) with a certain probability, and by flags being set misleadingly by the non-correct working SW-SCON flag setting unit (in all applications).

F07_10064

Monitoring of the uC_RAM module is mainly done via monitoring

- the parity within each RAM cell (see flag `uc_ram_parity`)
- the RAM address decoder (see flag `uc_ram_soaf`)
- structural tests of the RAM cells (see flag `uc_ram_ifa13`)

In addition, a malfunctioning of the uC_RAM will be visible in a malfunction of the CAN or the PSI communication (in CAN resp. PSI applications) with a certain probability, and by flags being set misleadingly by the non-correct working SW-SCON flag setting unit (in all applications).

F07_10065

Monitoring of the uC_ROM module is mainly done via monitoring

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- the CRC check of the ROM (see flag uc_rom_bist)

In addition, a malfunctioning of the uC_ROM will be visible in a malfunction of the CAN or the PSI communication (in CAN resp. PSI applications) with a certain probability, and by flags being set misleadingly by the non-correct working SW-SCON flag setting unit (in all applications).

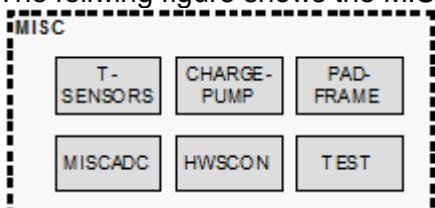
F07_10066 Monitoring of the uC OTP and the uC_CONFIGOTP modules is mainly done via monitoring

- the CRC check of the OTP (data and code OTP, see flags uc_otp_data_bist and uc_otp_prog_bist)

In addition, a malfunctioning of the uC OTP will be visible in a malfunction of the CAN or the PSI communication (in CAN resp. PSI applications) with a certain probability, and by flags being set misleadingly by the non-correct working SW-SCON flag setting unit (in all applications).

7.3.1.3.4 ASIC_MISC

F07_10068 The following figure shows the MISC (miscellaneous) block:



F07_10069 The MISC block contains the CHARGE PUMP which provides high voltages (18-20V) for the yaw rate frontend and also for the programming of the OTP.

The MISCADC is a Analog-Digital-Converter which is used to digitize 6 analog monitoring signals for the SW-SCON (resulting in flags yrs_rate_V_TN, yrs_rate_V_com, yrs_rate_V_fb, yrs_rate_V_CM, acc1_V_cm, acc2_V_cm) and is also being used to convert the analog voltages of the two temperature sensors (TSENSORS) into a digital signal.

The HWSCON (Hardware Safety Controller) triggers the uC-online-Test (question-response) and includes the memory checks of the uC, the checks of the bus system, the pinchecks, the over- and undervoltage checks, the frequency control and the Power-On-Reset. In addition, the area needed for filtering of the MISCADC is taken into account in the HWSCON area.

Additional test logic which is only being used during wafer-level testing (and which is, therefore, not safety relevant) such as a screening aid for the regulators and a test multiplexer is summarized in the module TEST.

The PADFRAME corresponds to the area of the pads and the corresponding wiring.

The failure effects of the MISC modules are:

F07_10070

TSENSORS:

The temperature sensors are being used to correct the sensitivity and offset of acceleration and yaw rate sensors over temperature. Therefore, offset and sensitivity as well as noise of yaw rate and acceleration may be affected when the temperature sensors fail.

They are also being used to correct some monitors over temperature, but this does not have effects on the top events.

F07_10071

MISCADC:

Since the MISCADC is used to digitize the temperature signals, the effects are the same as for failed TSENSORS.

F07_10072

CHARGE PUMP:

In normal operation, the charge pump is only being used for the yaw rate. A failed charge pump may therefore affect yaw rate offset, sensitivity and noise.

F07_10073

PADFRAME:

Failures of the pads are not considered explicitly, but are taken into account via the bond failures (shortages and ruptures).

F07_10074

HWSCON:



Since currently, the MISCADC filtering is considered in the HWSCON area, the effects are the same as for the MSICADC. Beside that, failures in the HWSCON do not directly affect any of the top events.

F07_10075 TEST:

The functions summarized in TEST do not have impact on the top events.

F07_10076 Monitoring of the TSENSORS is mainly done via redundancy check of both temperature sensors versus each other (see flag ctm_diff). If a failure in a temperature sensor yields a signal that is out of the measurement range, this would be found via the flag ctm_range. In addition, a failure of the temperature sensor would indirectly be found via all temperature-dependent monitors such as yrs_drv_pi_tol or acc1/2_V_cm.

F07_10077 Monitoring of the MISCADC is done indirectly via all monitors (including the temperature checks) that are digitized by the MISCADC (see flags yrs_rate_V_TN, yrs_rate_V_com, yrs_rate_V_fb, yrs_rate_V_CM, acc1_V_cm, acc2_V_cm, ctm_range, ctm_diff). Since the monitored voltage signals relate to different band gaps (acc band gap for acc1_V_cm, acc2_V_cm, main band gap for all others and the ADC itself), the monitoring is considered to be good.

F07_10078 Monitoring of the CHARGEUPUMP is mainly done via monitoring

- the voltage at the TN electrode (see flag yrs_rate_V_TN),
- the quadrature controller which will first try to compensate, but then saturate (see flag dsp_quad_QI_lim),
- the phase and amplitude of the drive path (see flag yrs_agc_irregular).

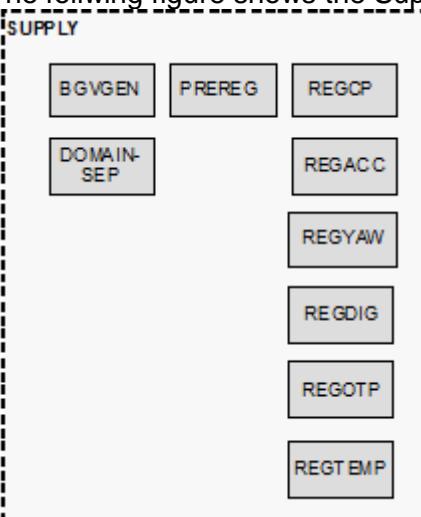
F07_10079 Continuous monitoring of the HWSCON is not necessary since there are no effects on the top events (except for the adc filtering whose monitoring is the same as for the TSENSORS and the MISCADC); nevertheless, the HWSCON is indirectly monitored by all flags that are handled by this module. In addition, it is scanned by the LBIST during startup to detect latent faults.

F07_10080 Since the failure modes of the PADFRAME are taken into account via the bonds, no explicit monitoring is necessary.

F07_10081 Since the TEST functions do not have impact on the top events, no monitoring is necessary.

7.3.1.3.5 ASIC_SUPPLY

F07_10085 The following figure shows the Supply block:



F07_10086 In the SUPPLY block (see also {REF:F03_320}, all supplies are summarized.

With the pre-regulator (PREREG), the >4.3V-Range is regulated down to the 3.3V range.

This voltage is further reduced

- by the charge pump regulator (REGCP) to ~2.9V, supplying the charge pump (ASIC_MISC_CHARGEUPUMP),
- by the acceleration regulator (REGACC) to ~1.8V, supplying both acceleration frontends (ASIC_ACC),



- by the yaw rate regulator (REGYAW) to ~2.8V, supplying the rate frontend (ASIC_RATE except DCO),
- by the temperature regulator (REGTEMP) to ~1.8V, supplying the temperature sensors (ASIC_MISC_TSENSORS),
- by the digital regulator (REGDIG) to ~1.85V, supplying the digital part (ASIC_DIG and ASIC_RATE_DRIVE_PLL_DCO) and
- by the otp regulator (REGOTP) to ~8V, being used for OTP programming.

The BGVGEN is the main band gap, used as reference voltage for all regulators except for the ACC regulator (REGACC) which has his own bandgap.

The module DOMAINSEP represents approx. 400 domain separators in which the data transfer between 1.8V and 3.3V is done. All data transferred between analog and digital part passes these domain separators.

The failure effects of the SUPPLY modules are:

[F07_10087](#)

BGVGEN:

A failure of the main band gap will result in a complete malfunction of the frontends and also of the digital part.

[F07_10088](#)

DOMAINSEP:

Failures in the transfer between digital and analog part may induce malfunction of the sensor and hence may affect each acceleration and yaw rate top event.

[F07_10089](#)

PREREG:

Failures in the pre-regulator may lead to a malfunction of the whole sensor in all applications in which the pre-regulator is being used.

[F07_10090](#)

REGCP:

Failures of the charge pump regulator will induce a malfunction of the yaw rate measurement.

[F07_10091](#)

REGACC:

Failures of the acceleration frontend regulator will induce a malfunction of the acceleration measurement.

[F07_10092](#)

REGYAW:

Failures of the yaw rate regulator will induce a malfunction of the yaw rate measurement and also of the MISCADC (and hence, possibly also on the temperature correction of the acceleration signals).

[F07_10093](#)

REGDIG:

Failures of the regulator of the digital part may affect the DSP, the uC, the main clock (via the DCO) and the interfaces and hence have impact on all top events.

[F07_10094](#)

REGOTP:

This regulator is only being used for the OTP programming and has hence no effects on the top events (since the only programming that may take place during use is the storage of a failure event in the failure memory, which is not safety relevant).

[F07_10095](#)

REGTEMP:

Failures in this regulator may affect the temperature measurement and hence offset and sensitivity as well as noise of yaw rate and acceleration.

[F07_10096](#)

Monitoring of the BGVGEN is mainly done via

- the monitoring of the voltage used to evaluate the capacitive changes of the CMA (see flags acc1_V_cm, acc2_V_cm); this monitoring references to a different band gap situated in the ACC frontend,
- the power-on-reset (POR).

[F07_10097](#)

Monitoring of the DOMAINSEP is mainly done indirectly via all flags of the frontends which all need to pass these separators.

[F07_10098](#)

Monitoring of the PREREG is done via

- over- and undervoltage detection (see flags VDD3_high, VDD3_low at the output of this regulator)
- indirectly via all other voltage monitoring flags (see below)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply

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F07_10099 Monitoring of the REGCP is done via

- over- and undervoltage detection (see flags V_CP_high, V_CP_low)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply in the yaw rate frontend.

F07_10100 Monitoring of the REGACC is done via

- over- and undervoltage detection (see flags V_ACC_high, V_ACC_low)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply in the acceleration frontend.

F07_10101 Monitoring of the REGDIG is done via

- overvoltage detection (see flag V_DIG_high) and the undervoltage detection (Power-On Reset, POR)
- indirectly via all other flags that indicate a malfunction of the sensor due to bad supply in the DSP, the main clock (via the DCO) and the interfaces.

F07_10102 Monitoring of the REGOTP is not necessary since it has no effects on the top events (see {REF:F07_10094}).

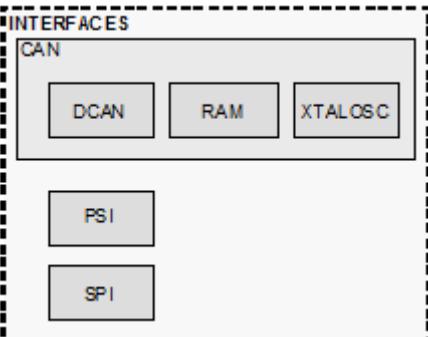
F07_10103 Monitoring of the REGTEMP is done via

- over- and undervoltage detection (see flags V_CTM_high, V_CTM_low)

In addition, a failure of the temperature sensor would indirectly be found via all temperature-dependent monitors such as yrs_drv_pi_tol or acc1/2_V_cm.

7.3.1.3.6 ASIC_INTERFACES

F07_10105 The following figure shows the interface block:



F07_10106 The ASIC contains three interfaces:

- a SPI interface (usually SPI slave, but alternatively useable as SPI master interface in some applications)
- a PSI interface
- a CAN interface which includes the core (DCAN), special Memory registers (originally RAM, now registers) and also an internal oscillator unit (XTALOSC) to which an external Xtal can be attached in order to get the frequency normal for the CAN module.

The failure modes are:

F07_10107 SPI:

A failure of the SPI module may induce wrong sensor signals and therefore affect all yaw rate and acceleration top events in SPI slave applications and the data transfer top event in SPI master applications.

F07_10108 PSI:

A failure of the PSI module may induce wrong sensor signals and therefore affect all top events in PSI applications.

F07_10109 CAN (incl. DCAN, RAM and XTALOSC):

A failure of the CAN module may induce wrong sensor signals and therefore affect all top events in CAN applications.

F07_10110 Monitoring of the SPI interface is done via



- a working communication (including check of polarity, phase, number of clock cycles, validity of contained addresses)

- check of the CRC included in the SPI message

F07_10112 Monitoring of the PSI interface is done via

- a working communication

- check of the CRC/parity included in the PSI message

F07_10113 Monitoring of the CAN interface (incl. DCAN, RAM and XTALOSC) is done via

- a working communication (see 1.4.12)

- check of the CRC/parity included in the CAN message

- check of the CRC within the "RAM" Memory (see flag can_ram_parity (Flag name not changed even though RAM w/ parity was replaced by Registers w/ CRC))

7.3.1.4 BONDS

F07_10117 As shown in figure {REF:F07_9996} there are three different parts which are connected by chip to chip or chip to substrate bonds. Chip to Chip bonds are the bonds from the ASIC to the acceleration element (BONDS_CMA) and the angular rate element (BONDS_CMG). The bonds from the ASIC to the substrate pins (BONDS_PINS) are chip to substrate bonds.

In the following each single bond is denoted by the placeholder "*". For each bond connection, there are two different failure modes.

BONDS_CMA_*_OPEN, BONDS_CMG_*_OPEN, BONDS_PINS_*_OPEN:

This failure mode describes that the bond is open.

BONDS_CMA_*_SC_*, BONDS_CMG_*_SC_*, BONDS_PINS_*_SC_*:

This failure mode describes that two bonds are shorted to each other.

These are the potential effects of bond failures:

F07_10118 BONDS_CMA1_*_OPEN, BONDS_CMA1_*_SC_*:

may affect acceleration1 offset, sensitivity and noise.

F07_10119 BONDS_CMA2_*_OPEN, BONDS_CMA2_*_SC_*:

may affect acceleration2 offset, sensitivity and noise.

F07_10120 BONDS_CMG_*_OPEN, BONDS_CMG_*_SC_*:

may affect yaw rate offset, sensitivity and noise.

F07_10121 BONDS_PINS_*_OPEN, BONDS_PINS_*_SC_*:

may affect almost all top events via different mechanisms, except

BONDS_PINS_WDGI_OPEN (no effect on top events, only safety indicator) and

BONDS_PINS_VSSA_SC_VSSD (no effect since VSSA and VSSD are shortened anyway within the package).

The effects are strongly application-specific,

i.e., a bond rupture of the XTALO bond (connecting the external XTAL to the XTAL oscillator) does not influence anything in a pure SPI application, hence is not safety-relevant in this application.

For details, pls refer to the FTA/metrics calculation.

F07_10122 Monitoring of acceleration bond ruptures and shortcuts (BONDS_CMA_*_OPEN,

BONDS_CMA_*_SC_*) are mainly monitored by:

- the pin check module to detect ruptures of the substrate pins (see flag pc_cs1)

- the monitoring of the voltage used to evaluate the capacitive changes of the CMA (see flags acc1_V_cm, acc2_V_cm) in case of bond shortages.

F07_10123 Monitoring of yaw rate bond ruptures and shortcuts (BONDS_CMG_*_OPEN, BONDS_CMG_*_SC_*) are mainly monitored by:

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- the pin check module to detect ruptures of the substrate pins (see flag pc_shd),
- the voltage at the TN electrode (yrs_rate_V_TN) and the common mode voltage (yrs_rate_V_com)
- the drive phase and amplitude (see flags yrs_agc_irregular, yrs_drv_pi_tol, yrs_pll_unlock, yrs_pll_lim, yrs_drv_adc_mean),
- the operation point of the Quadrature controller (see flag yrs_quad_I_tol),
- a possible overload of the rate detection ADC (see flag yrs_rate_adc),
- the voltage at the TN electrode (yrs_rate_V_TN) and the common mode voltage (yrs_rate_V_com),
- the quadrature controller (see flag dsp_quad_QI_lim).

F07_10124 Monitoring of pin bond ruptures and shortcuts (BONDS_PINS_*_OPEN, BONDS_PINS_*_SC_*) are mainly monitored by:

- the pin check module to detect voltage level differences between VSSA, VSSD and PSI5m (see flags pc_vssa, pc_vssd, pc_psi5_m) that may indicate ruptures or shortages,
- the pin check module to detect voltage ripples on CPUMP (charge pump) pin that may indicate ruptures of the CP (loss of external blocking cap), (see flag pc_cp),
- the monitors which base on voltages that are digitized by the MISC_ADC detect a rupture of VDD3 pin and/or loss of VDD3 blocking caps (in case of VB supply), since the MISC_ADC is sensitive to ripple on VDD3
- a functioning of the digital part (whose monitors detect whether a rupture of a VDD1_8 pin or a loss of the VDD1_8 blocking cap has lead to a malfunction of the digital part)
- a power-on reset (POR) in case of a shortcut in the supply pins or a rupture of the RESET_B pin,
- a running WDGI (checking ruptures or shortcuts of the WDGI bond) in case of CAN applications,
- the functioning of the communication via the interfaces.

The latter monitors are obviously application-dependent; for details, pls refer to the FTA/metrics calculation.

7.3.1.5 EXT

F07_10127 SMI7 needs, for proper functionality, several external electrical parts such as capacitors and resistors or an XTAL (see {REF:F03_344}).

Some are application-specific (like the PI-filter for PSI-applications or the XTAL for CAN applications), others are always necessary (as the blocking caps for VDD3, VDD1_8 and CPUMP).

The components are:

- EXT_C_CP: blocking cap at the charge pump
- EXT_C_VDD18: blocking cap at VDD1_8
- EXT_C_VDD3: blocking cap at VDD3
- EXT_PI_CIN, EXT_PI_RV, EXT_PI_CV: C's and R's for the PI filter
- EXT_QUARZ: external quartz for high-stable frequency for CAN

The effects of OPENs and SHORTs are:

F07_10128 EXT_C_VDD18_OPEN, EXT_C_VDD3_OPEN:

Loss or malfunction of the blocking caps at VDD3 and VDD1_8 may affect offset, sensitivity and noise of acceleration and yaw rate and also disturb the communication SPI-Master -> CAN/PSI.

F07_10129 EXT_C_VDD18_SHORT, EXT_C_VDD3_SHORT, EXT_PI_CIN_SHORT, EXT_PI_CV_SHORT:

Shortage of these capacitors means a short-circuit of the supply, therefore the whole chip will stop operation. All top events are affected.

F07_10130 EXT_C_CP_SHORT:

Shortage of the charge pump may affect offset and sensitivity of the yaw rate.

F07_10131 EXT_PI_RV_OPEN:

If the resistor of the PI filter is open, the supply voltage is disconnected, therefore the whole chip will stop operation. All top events are affected.

F07_10139 EXT_PI_RV_SHORT:



If the resistor of the PI filter is shortened, the PI filter will not work properly, with potential effects on offset and noise of acceleration and yaw rate, as well as the transfer SPI-MASTER -> PSI/CAN

F07_10132 EXT_PI_CIN_OPEN, EXT_PI_CV_OPEN:

Open capacitors in the PI filter may affect the offset and the noise of acceleration and yaw rate (ripple not suppressed), as well as the transfer SPI-MASTER -> PSI/CAN

F07_10133 EXT_QUARZ_OPEN:

With an open quartz, the crystal oscillator will not work, therefore all top events are affected in CAN applications since the CAN communication will not work any more.

F07_10134 Monitoring of an open or shortened charge pump capacitor (EXT_C_CP_OPEN, EXT_C_CP_SHORT) is mainly done via

- the pin check module to detect voltage ripples on CPUMP pin that may indicate loss of external blocking cap (see flag pc_cp),
- monitoring the phase and the amplitude of the yaw rate (see flag yrs_agc_irregular)
- the voltage at the TN electrode (see flag yrs_rate_V_TN)
- no communication any more (due to undervoltage)

F07_10135 Monitoring an open blocking cap for VDD1_8 (EXT_C_VDD18_OPEN) is mainly done via

- the potential malfunction of the digital part, especially the memoris (see flags uc_ram_*, uc_rom_*, uc_otp_*) and the uc watchdog (see flag uc_watchdog_err).

F07_10136 Monitoring an open blocking cap for VDD3 (EXT_C_VDD3_OPEN) is mainly done via

- the monitors which base on voltages that are digitized by the MISC_ADC detect a rupture of VDD3 pin and/or loss of VDD3 blocking caps (in case of VB supply), since the MISC_ADC is sensitive to ripple on VDD3

F07_10137 Monitoring an open quartz (EXT_QUARZ_OPEN) is done via a non-functional CAN communication.

F07_10138 Monitoring an open resistance in the PI filter (EXT_PI_RV_OPEN) is automatically detected due to the rupture of the power supply (POR) -> no communication any more.

F07_10140 Monitoring of open capacitors in the PI filter (EXT_PI_CIN_OPEN, EXT_PI_CV_OPEN) as well as a shortened resistance in the PI filter (EXT_PI_RV_SHORT) cannot be detected.

7.3.1.6 PINS

F07_10115 There are 81 pins at the package of the SMI7xy. Out of these 81 pins only 21 pins are functionally used. For this BGA package, each pin consists of the solder joint between the substrate printed circuit board of the SMI7xy and the printed circuit board of the top level hardware. All pins are described in section {REF:F03_200} of the datasheet. In the following each single pin is denoted by the placeholder "/*". There are two failure modes known for the PINs.

PINS_*/open:

This failure mode assumes that the connection is totally open between SMI7xy and the external printed circuit board.

PINS_*/SC_*/:

This failure mode describes the error that a pin has a shortcut to another pin

The PINS are not yet considered in the Metrics calculation (tbd).

The effects of open pins are the same as in {REF:F07_10117}.

7.4 Outline of the monitoring concept

F07_6122 The SCON continuously monitors each functional block, detecting HW failures which could result in incorrect signals being transmitted over CAN/SPI/PSI and marking these signals with error flags. In order to detect these failures the SCON has dedicated HW (AD-Converter, registers); the evaluation of

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errors and running of algorithms is however software based. Thus it is not possible to separate the HW associated with the different channels and the functional safety requirements must be applied for all functional blocks related to the different Top Events (see {REF:F07_987}).

Using a metric calculation (based on FTA/FMEDA methods) in the concept phase it has been determined whether such failures exist and the corresponding failure rates and SPF will be evaluated (see section 1.5). The SCON monitors are based on the MM3/MM5 architecture, with additions. Thus the SMI700 safety concept is designed to provide equal or better diagnostic coverage than current designs.

The µC will be checked continuously by the HW-SCON with a watchdog algorithm (challenge-response-dialog, see flag uc_watchdog_err).

In a similar way, the SCON-SW checks the DSP continuously (see flag dsp_online_test).

The temperature range is checked via two redundant temperature sensors (see flag ctm_range, ctm_diff).

In the case of an error being detected, the SMI700 communicates this to the next system level (normally the ECU of the affected system: Airbag/ESP/...) using the options detailed in 1.2.1. If possible (i.e. if the technical fault allows) the sensor will continue to communicate, marking the affected signals as incorrect (Channel Information = CI). This emergency operation mode allows the System ECU to assess the fault, and if compatible with the system safety goals the remaining signals may continue to be used.

The SMI700 does not switch itself off automatically (except for too low voltage in the digital core which will lead to a power-on reset); it is the task of the system ECU to decide on the basis of the SMI700 error flags which signal information to use. For this reason no assumptions have been made with respect to system or driver actions. Signals marked with an error channel status (e.g. internal flag CI<>0, SPI flag CN<>0) are to be considered incorrect, and not to be used for safety relevant systems.

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- A = Amplitude check
- V = Voltage supervision
- I = current supervision
- B = Bonding supervision
- L = Limit check
- M = Mean check
- C = CRC or Parity check
- D = Digital scan check
- T = number of Ticks
- R = Response / question
- S = Startup check
- P = plausibility check, digital

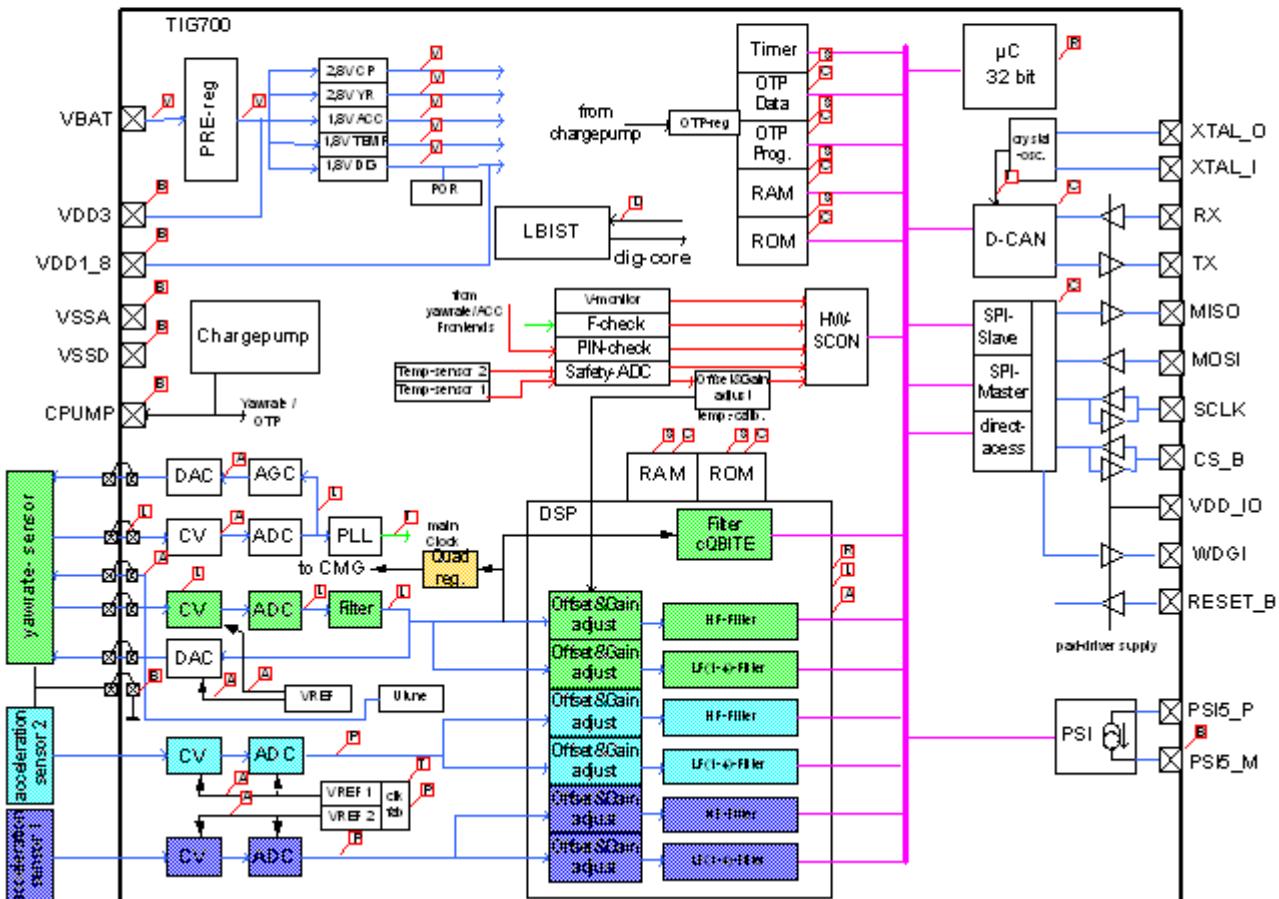


Figure 56: Monitor overview in the TIG700

7.4.1 Startup monitoring

7.4.1.1 Memory tests

F07_6123 During startup, the memories will be tested first. The RAMs will get a structural test at startup (SOAF, IFA13).

The ROMs and OTP (data OTP and code OTP) will be checked initially with a one shot CRC to detect bad programming of OTP cells (see flags uc_otp_prog_bist_initial, uc_otp_data_bist_initial).

In addition, it is being checked whether the OTP Code and the ROM code are compatible, otherwise the flag uc_rom_otp_sw_incompatible is set.

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Once the initial ROM/RAM memory check is finished, the µC gets reset. It starts with bootloading process.

The bootloader parses all the locked OTP banks and the next open bank (if it exists; this may happen during manufacturing. This bank will be interpreted, but in parallel, the flag uc_otp_data_open_bank will be set since in final operation state, all banks need to be closed).

If any bank is skipped, an error flag must be set ('uc_otp_data_corrupt_header'). It initializes the CRC-check of each locked banks by sending command to HW-CRC engine. If the locked bank passes the CRC check, the bootload copies all the configuration tuples for registers to destination registers.

If any tuple cannot be interpreted, the flag uc_otp_data_invalid_tuple is set.

All information distributed by the boot loader to the registers is being read back and checked for consistency. Any failure in the consistency check results in the flag uc_tuple_readback_mismatch.

The DSP configuration tuples will be first skipped since DSP is still in memory checking mode. This part of bootloading process is called configuration bootloading.

Once LBIST is configured, the system starts LBIST. The whole µC core and the rest digital circuit is scanned. After LBIST, the system generates again a reset so that the µC restarts with the configuration bootloading. The system has to know that the LBIST has been started once and disables the LBIST this time. When all the configuration tuples are parsed, µC waits in loop for DSP to finish its memory check.

A query to the DSP and sensor frontend is sent regularly by uC. Once the DSP initial memory check is finished, uC starts to download the DSP tuples. When DSP configuration data are loaded to the DSP registers, bootloader saves the bootloading status flags and returns to the main routine.

After initial memory tests, the continuous memory tests are being started, e.g. continuous SOAF and IFA13 and parity checks for the RAMs. For details, refer to 1.4.8.

Cyclic OTP checks are used to detect modifications of code OTP during operation, it always uses CRC-Checksum generated by one-shot CRC check (see flags uc_otp_data_bist, uc_otp_prog_bist).

7.4.1.2 LBIST

F07 10160 At each startup, a structural digital scan test is carried out, called LBIST. It checks the whole digital part except the Test Mode Controller (i.e., Clock Multiplexer and Scan Mode configuration), since this part is necessary to control the LBIST itself, and some digital gates in the ACC Frontends (i.e. the ACC clock fab). Variable pattern sequences can be generated.

The test will be carried before startup of the sensor frontends and the boot loading of the system. The configuration of the LBIST will be performed by the uC in the bootloader routine by config tuples of type 16bit. At the end of the LBIST configuration the last tuple will initiate the LBIST procedure by writing LBIST_START. When the LBIST is completed, the Test Controller will issue a reset to the system, which will reboot the uC. The uC will again configure the LBIST and try to start it, but the LBIST will ignore the request and thus the program execution and start of the system will continue.

Compared to the externally controlled LBIST used during wafer-level testing, this integrated LBIST is less powerful. The integrated LBIST checks for stuck-at faults with an estimated fault coverage of ~70%. Since it is being carried out only once at startup, it is only being used for latent faults.

7.4.1.3 Startup of continuous monitoring

F07_7029 Concerning startup behaviour, the flags can be split into the following categories: S

Frontend and DSP flags:

Right from the start, the Frontends and the DSP will start generating flags (interrupted by the LBIST) which will be handled "transparent" (which means that there is no sample-hold mechanism) by the HW-SCON.

After Bootloading, the Software releases the Frontends ("FE release", ~ 25ms), leading to the initiation process in the Frontend (frequency finding etc.).

In this phase, the SW starts monitoring signals and setting internal flags. This phase ends with a locked PLL (yrs_pll_unlock = 0) and regulated AGC (yrs_agc_irregular = 0) ("FE locked")

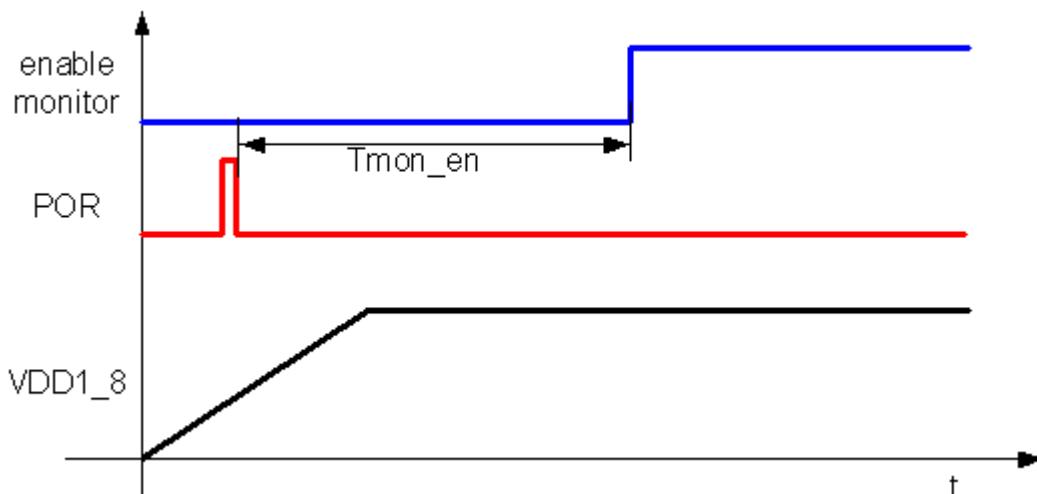
At this time, the HW SCON starts accumulating the flags (= removes transparency from all flags that were transparent before).

When, in addition, the Quadrature regulator is ok (yrs_quad_l_tol = 0, set by the SW), ("FE ready", ~150ms), the SW starts evaluating the flag's effect on the failure counters and hence, on the Channel Information flags (2bit-Status).

Supply flags:

The supply monitoring flags will not be set prior to "FE release" (Bootloading accomplished). They will remain transparent until "FE ready", similar to the Frontend and DSP flags.

The over/under voltage monitors will be active at least 50 msec (Tmon_en) after power on reset has created the reset pulse.



Only the low voltage monitor of the digital core (on the 1,8V line behind regulator), leading to a Power-On-Reset, is active from the start on and can not be disabled.

DSP online test (carried out by SW) starts with "FE release" and is not transparent.

The **memory tests** are active from the start on (interrupted by the LBIST), except uc_otp_data_bist and uc_otp_prog_bist, which will not start earlier than parallel to the boot loading process.

The **Pinchecks** are dependent on the clock and do therefore not start earlier than "FE release".

The **μC watchdog** (carried out by the HW-SCON) starts after "FE locked".



The **Bite** flags can only be set during Bite phase (after "FE ready" if PON_BYTEx = 1).

The SW-generated flags "**uc_...**" are generated depending on when the corresponding modules are running and will act immediately via HW on all Channel Information flags.

During startup, some flags may occur that may still be visible in the "Interface flag list" (see next chapter, {REF:F07_F031}), since they are hold until read. As long as they did not lead to an invalid signal (status CI>0 / CN>0), these flags can be ignored. It is recommended to read them out once prior to using sensor acceleration or yaw rate data (in order to make sure that flags occurring normal operation are not being mixed with residual flags from startup phase).

7.4.2 SCON error handling

7.4.2.1 SCON incoming flags

F07_7031

From the SCON point of view, there are basically four sources of error flags (for better understanding, refer to figure in {REF:F07_7036}).

- 1) the µC status and SW-flags (set by SW)
- 2) the flags resulting from SW-based checks of selected signals (set by SW)
- 3) the flags deriving directly from the Frontends or the DSP (set by HW)
- 4) the flags which are generated by the SCON-HW itself (set by HW).

All units are responsible to set and remove the flags according to their correct status.

The flags will be collected with ~25MHz into the following clear-on-read registers:

- 1) the "Interface flag list" (error_flag_16_bankXX) which can be read out by all interfaces in order to get an detailed information on which flags were active.
 - 2) the 2 MSBs of the "16bit Info cluster" which can be read out by all interfaces in order to get an overview which classes of failures were active (definition of the classes see table) (the 14 LSBs of that cluster are updated by the SW with ~2kHz)
 - 3) the flag list that will be used by the SCON-SW (error_flag_32_bankXX) in order to act on the failure counters (and hence the Channel Information (CI) bits); these flag list is also being used for updating the 14 LSBs of the "16bit Info cluster".
- 1) and 2) are cleared as soon as the read request has been received by the sensor. If any succeeding error in the communication occurs, e.g. CRC error in the SPI response frame due to disturbances, the information is lost and can not be recovered.
- 3) is cleared on read (read by the µC)

In addition, some flags (especially the flags indicating that the µC itself and hence the SCON-SW is not working correctly any more) induce special actions such as

- 1) Overwrite the CI status calculated by the SCON-SW to "10"
- 2) Disable the CAN and/or PSI interface right at the pads
- 3) Invoke a non-maskable Interrupt (IR) in the µC leading to a final error memory entry followed by an idle loop.

Details see 1.4.4.

7.4.2.2 Error counters and channel status flags

F07_7032

Every flag may act as an input for all failure counters. These error counters work like low pass filters, so that errors flags at the interfaces do not toggle.

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The flag list for the µC SCON SW will be read out and evaluated by the SCON-SW with 2kHz ("absolutley timed"). It is predefined in ROM which flag can act on which failure counter (see table ...). Each flag may have the following weights (in RAM-table, initialized by OTP):

- 11 the flag is masked and does not act on failure-counters 0-5
- 01 the flag acts with weight 1 on the assigned failure counters 0-5
- 10 the flag acts with weight 2 on the assigned failure counters 0-5
- 00 the flag acts immediately and permanently on the failure counters 0-5

Both, weight 1 and weight 2 are set to 1.

The failure counters will be increased with the maximum weight of the assigned and active flags (see below); if several flags act on a failure counter simultaneousley, they are counted as one.

Once a flag with weight "00" acts on a failure counter, the counter will be set to a value above the limit and will not be decreased again, resulting in a permanent CI flag until the next reset. Flags that are masked (weight "00") will not contribute to the SW-Part of the 16bit-Infocluster.

8 failure counters are foreseen. The error counters are configurable so that the error latency timing defined at the beginning of this chapter is not exceeded, and an error is transmitted as long as corrupted data is still present in the filter chain (filter flush time). For that purpose, the limit and the hold time need to be configurable individually via the boot loading process.

As soon as the limit of a counter is exceeded, the corresponding channel status flags are set to 01 (temporary) or 10 (permanent). When passing the limit or in occurance of an additional active SCON flag when being above the limit, the counter is increased such that the automatic decrease of the counter passes the limit after the "Hold time".

The channel information (CI) bits can have the following values:

- 00 signal ok
- 10 permanent flags present
- 01 temporary flags present (FC > Limit)
- 11 BITE or Init ongoing

F07_1109

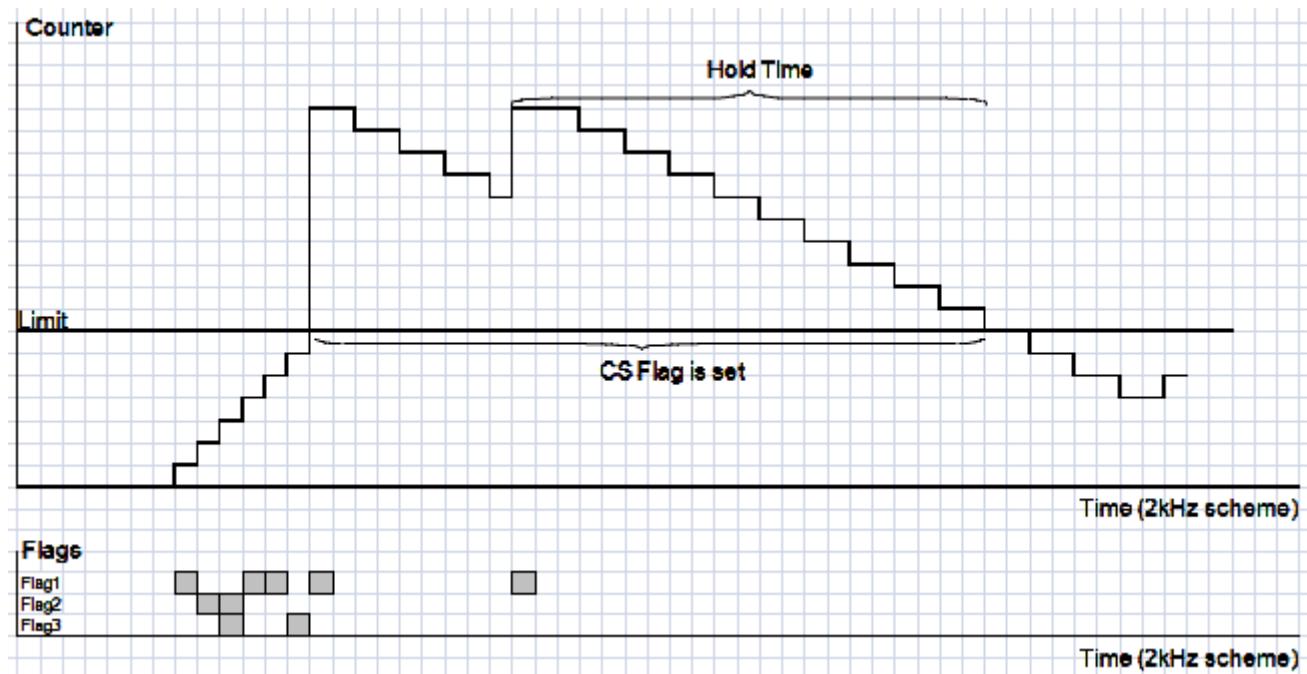


Figure 57: Schematic flow of the failure counters

F07_7033

The failure counters are:

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Nr.0	ACC1_HF	sets CI flag of ACC1-HF-channel (400Hz-channel)
Nr.1	ACC1_LF	sets CI flag of ACC1-Channel (LF-channel)
Nr.2	ACC2_HF	sets CI flag of ACC2-HF-channel (400Hz-channel)
Nr.3	ACC2_LF	sets CI flag of ACC2-Channel (LF-channel)
Nr.4	YR_HF	sets CI flag of YR-HF-channel (400Hz-channel)
Nr.5	YR_LF	sets CI flag of YR-Channel (LF-channel)
Nr.6	VARIABLE1	sets 0-6 CI flags (configurable soft/OTP)
Nr.7	VARIABLE2	sets 0-6 CI flags (configurable soft/OTP)

When an error counter has reached its limit and signals an error on the interface, only the affected signals are marked invalid (CI flag in SPI/PSI/CAN message; in CC32in-SPI, the 2 bits of the CI flag are "ORed" resulting in the CN flag).

The assignment of the flags to the failure counters is done by design, except for the Variable Counters to which up to 3 flags each can be assigned by OTP/soft (with weights independent from the weights used for the other error counters). It is thus possible to reroute a flag completely. The result of the variable failure counters can be assigned to 0-6 CI flags, also by OTP/RAM.

The configuration of variable counter is stored in RAM (see {REF:F02_10336}). They can be configured by RAM-Tuples stored in OTP.

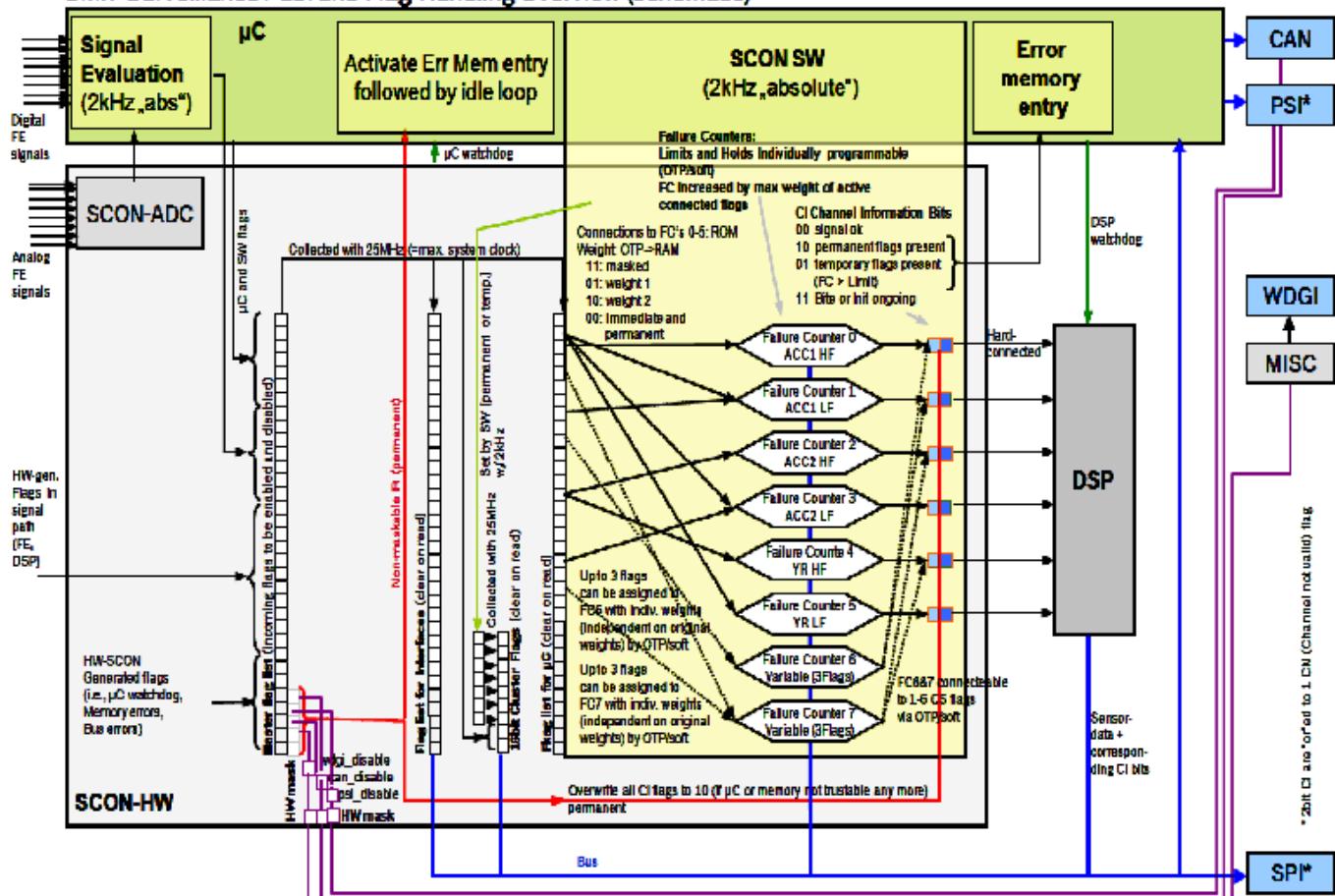
For configuration of flag weights and variable error counters each flag is referenced by its unique flag number (see {REF:F07_9510}).

The counter status of all failure counters is readable via the interfaces (also CC32in inframe).

The 2bit-CI-status is hard-connected to the DSP. Whenever sensor data of a specific channel is requested via the bus by any interface, the 16bit-data is delivered together with the corresponding 2bit-CI-status. This way, it is assured that the CI status always corresponds to the data.

7.4.2.3 Overview of the SCON error flag handling

F07_7036 The following graph gives an overview of the error flag handling in the TIG700:
SMI7 Surveillance Path and Flag Handling Overview (schematic)



F07_1129 "25MHz" corresponds to the system clock, therefore no flags will be lost.

Only for A-Silicon, the "Activate-Err-Mem entry followed by idle loop" will be replaced temporarily by a jump into a debug diagnostic mode allowing to communicate via the interfaces ("Mess-CAN", "BiDir-PSI", SPI), except for the failure uc_stack_check which will lead to the endless loop.

7.4.2.4 Error memory

F07_1159 32 Bytes error memory locates in data OTP. It is used to store error entry permanently. Error Memory must be first activated for error storing. The lowest address word of error memory is used to store the error memory activation code. If the error memory is activated (see {REF:F07_9501}), an error entry will be generated when a channel_info is set to invalid due to an error counter reaching its limit (not just due to sensor initialisation). Maximal one error entry is stored per each power on cycle.

7.4.2.4.1 Format of Error Entries

F07_9497 Each Error Entry consists of 4 Bytes, each holding the index of an error flag correlated to the occurred error situation. The error flag index is from 1 to 160 (see {REF:F07_9510}).



7.4.2.4.2 Error Storage Concept

F07_9499

Error Flag Priorisation regarding Information Relevance for Error Analysis:

Goal:

Store the most relevant information for error analysis. Most important is data about the root cause, i.e. where in the signal paths did the original error occur (as other errors might be detected only in consequence of the root cause).

In every SCON-SW cycle, the readout contents of the error flag registers are temporarily kept (as a copy) in the µC RAM for one SCON cycle.

When (later in the SCON-SW cycle) one or more of the error counter reach their limit (and in succession one or more channel_info change to invalid) the SCON SW parses the error flag register copy for set flags linked to the "overflowed" error counter(s).

From these set and linked flags the four flags with the highest priority build the later error entry: for each of these flags its number (see {REF:F07_9510}) is stored in one of the 4 bytes of the new error entry.

The flag priority is defined by their register and bit address: a lower address means a higher priority (the register address is more significant than the bit address). The flag to register assignment and therefore the flag addresses are defined in the ASIC design.

Rules:

- Flags of monitors closer to the frontend shall get a higher priority than those checking subsequently in the signal path.
- The belonging to different signal paths is no criteria for prioritization of flags.

In order to store more information in error memory, not every error entry will be stored in error memory. If the new error entry is identical to the last error entry in error memory, the new error entry will not be saved in error memory.

All errors, that include the risk, that the SCON-SW may be defect (Bus-Error, µC-Errors, Code Memory Errors) must be handled by the SCON-HW in a way that it forces the affected channel_info to invalid.

7.4.2.4.3 Activation of error storing

F07_9501

As long as the first error memory entry (i.e. error memory activation marker) is empty, no error entries are stored.

The activation of the error memory is to be done using the configuration service "Activate Error Memory".

7.4.3 List of all monitors

F07_1021

In sum, approximately 130 internal monitorings are running continuously, with corresponding failure flags.

F07_6124

The flags are being handled (and partly generated) by the SCON. The following table lists all planned monitor flags including a description of their purpose, their source and their handling (HW/SW partitioning). A second table lists the effects on failure counters, the CI (Channel Information) flags and the 16bit summarizing cluster, see 1.4.4.

F07_10155 If flags are handled by the SCON-SW, the following evaluation types are being used:

1. Range Check: $f_{min} \leq f(t) \leq f_{max}$
2. Tolerance Check: $|f(t) - f_{ref}| < f_{tol}$
3. Symmetric Range Check: $|f(t)| < f_{max}$
4. Difference Check: $|f_{1(t)} - f_{2(t)}| < f_{diff}$



5. Temperature dependent Tolerance Check(TDTC): $|f(t) - f_{ref_Tref} * (1 + f_{tc} * (T(t) - Tref))| < |f_{tol}*f_{ref_Tref}|$ (**Tref is a fixed raw temperature value = 32LSB, which is the norminal value of 55°C**); f_{ref_Tref} is the reference value at temperature $Tref$)

If the incoming signal exceeds the limit, an error flag will be generated by SCON.

6. DSP online BIST

7.4.3.1 Yaw rate drive monitors

7.4.3.1.1 yrs_agc_irregular

F07_9864

S

Flag Name:	yrs_agc_irregular
Goal:	Oscillation amplitude of CMG out of limits (goal: 8µm, goal tolerance: ~1%), measured at input of PI
Test:	<p>Test (HW): The AGC_irregular-Flag is set to zero in case - the AGC is enabled (done by the startup process) and CMG has reached its target amplitude (see below) AND - the PLL is locked (yrs_pll_unlock = 0). Otherwise, the flag is set to 1.</p> <p>If the nominal amplitude is reached will be tested as below: $HW_av.64(DRV_ERR) < DRV_AGC_LIM$ DRV_ERR = difference of current amplitude DRV_AMP and the nominal amplitude DRV_AMPL_REF</p>
Programmable by Customer:	-
Frequency:	Average of 64 ~25kHz oscillations -> ~400Hz
Source of flag:	YRS Frontend HW

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.1.2 yrs_drv_pi_tol

F07_9865

S

Flag Name:	yrs_drv_pi_tol
Goal:	Drive force which is necessary to obtain the goal oscillation amplitude of the CMG is out of limits, measured at output of PI.
Test:	Test (SW): Temperature dependent Tolerance Check (TDTC) of register YRS_DRV_PI_TOL_REG (11..0) (HW-averaged 16x) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Relative tolerance f_tol
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	YRS Frontend via SW

7.4.3.1.3 yrs_drv_bp_lim

F07_9867

S

Flag Name:	yrs_drv_bp_lim
Goal:	Overload flag of the band pass limiter in the drive path.
Test:	Flag is set by HW if Min/Max of filter range is reached or exceeded.
Programmable by Customer:	-
Frequency:	~400kHz
Source of flag:	YRS Frontend HW

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.1.4 yrs_drv_adc_mean

F07_9868

S

Flag Name:	yrs_drv_adc_mean
Goal:	Check offset+gain of drive CU and ADC stage by controlling the mean drive value.
Test:	Test (SW): Tolerance Check of register YRS_DRV_ADC_MEAN_REG (14...0) (HW-averaged 512x) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~400kHz/512 = ~0.8kHz
Source of flag:	YRS Frontend via SW

7.4.3.1.5 yrs_drv_cu_gain

F07_9869

S

Flag Name:	yrs_drv_cu_gain
Goal:	Test (only) the gain of drive CU and ADC stage by applying an additional pulse with 1/32 of the sensor frequency (~780Hz) prior to the CU and demodulation/average after ADC.
Test:	Test (SW): Tolerance Check of register YRS_DRV CU_GAIN_REG (14...0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~25kHz/32 = ~0.8kHz
Source of flag:	YRS Frontend via SW

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7.4.3.1.6 yrs_pll_lim

F07_9870

S

Flag Name:	yrs_pll_lim
Goal:	Detect PLL Frequency is at regulator limit
Test:	Flag is set by HW if PLL regulator value (limited to 9bit = 0...511) is reached
Programmable by Customer:	-
Frequency:	~ 400kHz
Source of flag:	YRS Frontend HW

7.4.3.1.7 yrs_pll_tol

F07_9871

S

Flag Name:	yrs_pll_tol
Goal:	Compare PLL regulator value to new part value
Test:	Test (SW): Tolerance Check of register (phase) YRS_PLL_TOL_REG (12...0) (HW-averaged 16x) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~25kHz/16 = ~1.6kHz
Source of flag:	YRS Frontend via SW

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7.4.3.1.8 yrs_pll_unlock

E07_9872

S

Flag Name:	yrs_pll_unlock
Goal:	PLL is unlocked, which means: Phase error (output of phase detector is above limit; goal: ~1°) OR Frequency error (Digitally controlled Oscillator DCO has reached lower or upper limit; goal: ~ +0.7%)
Test:	Test (HW): Phase error: $ HW\text{-Average64}(PLL_PD_ERR) < PLL_PFD_LockLim$ (Average of 64 ~25kHz-Oscillations -> ~400Hz) $PLL_PD_ERR = \text{aktual phase} - PLL_PHASE_REF$ DCO output: Limiter Flags (Hi/Lo) (~25kHz)
Programmable by Customer:	-
Frequency:	400kHz if Oszillator control value reaches upper or lower limit; for phase errors: Average of 64 oscillations with 400kHz/16 = ~25kHz -> ~400Hz
Source of flag:	YRS Frontend HW

7.4.3.1.9 yrs_drv_adc

E07_9873

S

Flag Name:	yrs_drv_adc
Goal:	Overload flag of the ADC in the drive path.
Test:	Drive-ADC overload w/ HW-precounter; The A/D converter samples every drive/rate period with 16 samples, i.e. at $16 \times 25\text{kHz} = 400\text{kHz}$. The precounter is configured such that an permanent overload will trigger the flag after 16 sensor cycles.
Programmable by Customer:	-
Frequency:	$\sim 25\text{kHz}/16 = \sim 1.6\text{kHz}$
Source of flag:	YRS Frontend HW

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Dept.: AE/NE4



7.4.3.2 Yaw rate detection monitors

7.4.3.2.1 yrs_quad_I_tol

F07_9874

S

Flag Name:	yrs_quad_I_tol
Goal:	Compare Quadrature regulator to new part value.
Test:	Test (SW): Tolerance Check of register QUAD_I_VALUE(15...0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~25 kHz/16 = ~1.6 kHz
Source of flag:	DSP via SW

7.4.3.2.2 yrs_quad_HF_tol

F07_9875

S

Flag Name:	yrs_quad_HF_tol
Goal:	Deviation from required quadrature (0°/s) at input of controller. Value is sensitive to external vibration.
Test:	Test (SW): Symmetric Range Check of register QUAD_HF_LIMITED(15...0) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_max
Frequency:	~25 kHz/16 = ~1.6 kHz
Source of flag:	DSP via SW

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7.4.3.2.3 yrs_rate_pt2_lim

F07_9876

S

Flag Name:	yrs_rate_pt2_lim
Goal:	Overload flag of the Controller in the Rate path
Test:	After the additional gain at the controller output the clipping will be detected (flag will be set by HW).
Programmable by Customer:	-
Frequency:	~400kHz
Source of flag:	YRS Frontend HW

7.4.3.2.4 yrs_rate_quantizer

F07_9877

S

Flag Name:	yrs_rate_quantizer
Goal:	Overload flag of the quantizer (the quantizer reduces the resolution of the PT2 output to a 4bit signal).
Test:	Quantizer overload w/ HW-precounter; The Quantizer samples every drive/rate period with 16 samples, i.e. at $16 \times 25\text{kHz} = 400\text{kHz}$. The precounter is configured such that an permanent overload will trigger the flag after 16 sensor cycles.
Programmable by Customer:	-
Frequency:	$\sim 25\text{kHz}/16 = \sim 1.6\text{kHz}$
Source of flag:	YRS Frontend HW

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7.4.3.2.5 yrs_rate_adc_mean

F07_9878

S

Flag Name:	yrs_rate_adc_mean
Goal:	<p>Check DC level (operating point) of rate CU and ADC stage by controlling the mean rate value (ADC out).</p> <p>The mean value of the 6Bit output of the ADC is supposed to be monitored. Since the dither might be activated leading to different offsets for 16 sensor cycles the mean value must be calculated over this time: 16 sensor cycles * 16 samples = 256. Thus 256-400kHz-cycles are taken for an average.</p> <p>Due to Sine/Cosine demodulation at 100 kHz, no 2f-portion (f from CMG) is expected.</p>
Test:	<p>Test (SW): Tolerance Check of register YRS_RATE_ADC_MEAN_REG (13...0) (HW-averaged 256x).</p> <p>Flag is set as soon as limits are reached or exceeded.</p>
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~400kHz/256 = ~1.6kHz
Source of flag:	YRS Frontend via SW

7.4.3.2.6 yrs_rate_adc

F07_9879

S

Flag Name:	yrs_rate_adc
Goal:	Overload flag of the rate ADC
Test:	Rate-ADC overload w/ HW-precounter; The A/D converter samples every drive/rate period with 16 samples, i.e. at $16 \times 25\text{kHz} = 400\text{kHz}$. The precounter is configured such that an permanent overload will trigger the flag after 16 sensor cycles.
Programmable by Customer:	-
Frequency:	~25 kHz/16 = ~1.6 kHz
Source of flag:	YRS Frontend HW

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7.4.3.2.7 yrs_rate_V_TN

F07_9880

S

Flag Name:	yrs_rate_V_TN
Goal:	UDF-Voltage at TN-electrode
Test:	Test (SW): Tolerance Check of register SCON_ADC_UDF_DET(11..0) (1/16-buffered) (~4,57mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~0.5kHz
Source of flag:	MISC via SCON-ADC and SW

7.4.3.2.8 yrs_rate_V_com

F07_9881

S

Flag Name:	yrs_rate_V_com
Goal:	Common Mode voltage monitor for rate CU (Cn-Cp-check; goal: check vs ~1% deviation)
Test:	Test (SW): Tolerance Check of register SCON_ADC_DET_CNCP(11..0) (~0,43 mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~0,1kHz (sampled at 10KHz, filtered 1st order at cut off frequency of 100Hz to reject possible vibration issues at 1KHz)
Source of flag:	MISC via SCON-ADC and SW

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7.4.3.2.9 yrs_rate_V_fb

F07_9882

S

Flag Name:	yrs_rate_V_fb
Goal:	Sensor feedback force monitor (check vs new-part values)
Test:	Test (SW): Tolerance Check of register SCON_ADC_FFB_MUX(11..0) (~0,71mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~0,5kHz
Source of flag:	MISC via SCON-ADC and SW

7.4.3.2.10 yrs_rate_V_CM

F07_9883

S

Flag Name:	yrs_rate_V_CM
Goal:	UCM-voltage (measures pulse on CM of YR-FE)
Test:	Test (SW): Tolerance Check of register SCON_ADC_UCM_YAW(11..0) (~0,71mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	~100Hz due to low-pass filtering
Source of flag:	MISC via SCON-ADC and SW

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7.4.3.2.11 pe_flag_rate_8k_err

F07_10179	Flag Name: pe_flag_rate_8k_err	S
	Goal: Parity prediction of YR HF decimation filter	
	Test: see goal	
	Programmable by Customer: -	
	Frequency: ~8kHz	
	Source of flag: YRS Frontend HW	

7.4.3.2.12 pe_flag_rate_1k_err

F07_10180	Flag Name: pe_flag_rate_1k_err	S
	Goal: Parity prediction of YR LF decimation filter	
	Test: see goal	
	Programmable by Customer: -	
	Frequency: ~1kHz	
	Source of flag: YRS Frontend HW	

7.4.3.2.13 pe_flag_quad_8k_err

F07_10181	Flag Name: pe_flag_quad_8k_err	S
	Goal: Parity prediction of Quad HF decimation filter	
	Test: see goal	
	Programmable by Customer: -	
	Frequency: ~8kHz	
	Source of flag: YRS Frontend HW	

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7.4.3.2.14 pe_flag_quad_2k_err

F07_10182	Flag Name: pe_flag_quad_2k_err	S
	Goal: Parity prediction of Quad LF decimation filter	
	Test: see goal	
	Programmable by Customer: -	
	Frequency: ~2kHz	
	Source of flag: YRS Frontend HW	

7.4.3.2.15 pe_flag_cic4_err

F07_10183	Flag Name: pe_flag_cic4_err	S
	Goal: Parity prediction of CIC (Cascaded Integrator Comb) filter (which is a form of a FIR decimation filter) in the Rate Detection path	
	Test: see goal	
	Programmable by Customer: -	
	Frequency: ~4kHz	
	Source of flag: YRS Frontend HW	

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7.4.3.3 Acceleration frontend monitors

7.4.3.3.1 acc1_clk_cnt

F07_9884

S

Flag Name:	acc1_clk_cnt
Goal:	Check ACC clock frequency 130kHz
Test:	HW counts 25MHz-pulses within n ACC-130kHz-pulses. Resulting number is checked by HW vs goal (fixed Value and fixed tolerance)
Programmable by Customer:	-
Frequency:	~130kHz
Source of flag:	ACC Frontend

7.4.3.3.2 acc2_clk_cnt

F07_9885

S

Flag Name:	acc2_clk_cnt
Goal:	Check ACC clock frequency 130kHz
Test:	HW counts 25MHz-pulses within n ACC-130kHz-pulses. Resulting number is checked by HW vs goal (fixed Value and fixed tolerance)
Programmable by Customer:	-
Frequency:	~130kHz
Source of flag:	ACC Frontend

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7.4.3.3.3 acc_clk_ovlp

F07_9886

S

Flag Name:	acc_clk_ovlp
Goal:	The ACC frontend works with Switched capacitor technique. The frontend implementation comprises of two 180°-Phase shifted clocks, PHI1 and PHI2. To make sure error free transfer of the charge from one capacitor of the other, PHI1 and PHI2 clocks must not be set high simultaneously.
Test:	This is checked via AND-Gate (HW), which set a high signal when both the clocks are high i.e. overlapping. A R/S FF (flag acc_clk_ovlp) is set to indicate an invalid state of the clock fab.
Programmable by Customer:	-
Frequency:	on occurrence (~130kHz)
Source of flag:	ACC Frontend

7.4.3.3.4 acc1_V_cm

F07_9887

S

Flag Name:	acc1_V_cm
Goal:	Check FE voltage Ucm of ACC1 in order to check bonds
Test:	Test (SW): Temperature dependent Tolerance Check (TDTC) of register SCON_ADC_UCM_ACC1(11..0) (~0,43mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Relative tolerance f_tol
Frequency:	~0,5kHz
Source of flag:	SCON(HW) via SCON-ADC and SW

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7.4.3.3.5 acc2_V_cm

F07_9888

S

Flag Name:	acc2_V_cm
Goal:	Check F E voltage Ucm of ACC2 in order to check bonds
Test:	Test (SW): Temperature dependent Tolerance Check (TDTC) of register SCON_ADC_UCM_ACC2(11..0) (~0,43mV/LSB) Flag is set as soon as limits are reached or exceeded.
Programmable by Customer:	Relative tolerance f_tol
Frequency:	~0,5kHz
Source of flag:	SCON(HW) via SCON-ADC and SW

7.4.3.3.6 acc1_ds_lim

F07_9889

S

Flag Name:	acc1_ds_lim
Goal:	Overload detection of ACC1 ADC
Test:	In order to detect an overload state of the sigma-delta converter, a consecutive train of digital ones or zeroes is observed and accumulated. If an overload condition is detected, the flag acc1_ds_lim is raised.
Programmable by Customer:	-
Frequency:	~130kHz/16
Source of flag:	ACC Frontend

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7.4.3.3.7 acc2_ds_lim

F07_9890

S

Flag Name:	acc2_ds_lim
Goal:	Overload detection of ACC2 ADC
Test:	In order to detect an overload state of the sigma-delta converter, a consecutive train of digital ones or zeroes is observed and accumulated. If an overload condition is detected, the flag acc2_ds_lim is raised.
Programmable by Customer:	-
Frequency:	~130kHz/16
Source of flag:	ACC Frontend

7.4.3.3.8 acc1_overload_det

F07_9891

S

Flag Name:	acc1_overload_det
Goal:	Disturbance detection of ACC1 signal
Test:	In order to detect disturbances in the ACC1 signal ("high energy peaks"), a weighted counter is used to sum up consecutive bittrains of same polarity. A second counter sums up the upper 8 bit values of the first counter and compares it every milli-second with a limit, before resetting the counter to zero. If the limit is exceeded, the flag will be set. This flag is not a failure flag, but an vibration indication flag.
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	ACC Frontend

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7.4.3.3.9 acc2_overload_det

F07_9892

S

Flag Name:	acc2_overload_det
Goal:	Disturbance detection of ACC2 signal
Test:	In order to detect disturbances in the ACC2 signal ("high energy peaks"), a weighted counter is used to sum up consecutive bittrains of same polarity. A second counter sums up the upper 8 bit values of the first counter and compares it every milli-second with a limit, before resetting the counter to zero. If the limit is exceeded, the flag will be set. This flag is not a failure flag, but an vibration indication flag.
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	ACC Frontend

7.4.3.3.10 acc1_pe_flag_1k_err

F07_10184

S

Flag Name:	acc1_pe_flag_1k_err
Goal:	Parity prediction of ACC1 LF decimation filter
Test:	see goal
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	ACC Frontend

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7.4.3.3.11 acc1_pe_flag_8k_err

F07_10185	Flag Name: acc1_pe_flag_8k_err	S
Goal:	Parity prediction of ACC1 HF decimation filter	
Test:	see goal	
Programmable by Customer:	-	
Frequency:	~8kHz	
Source of flag:	ACC Frontend	

7.4.3.3.12 acc2_pe_flag_1k_err

F07_10186	Flag Name: acc2_pe_flag_1k_err	S
Goal:	Parity prediction of ACC2LF decimation filter	
Test:	see goal	
Programmable by Customer:	-	
Frequency:	~1kHz	
Source of flag:	ACC Frontend	

7.4.3.3.13 acc2_pe_flag_8k_err

F07_10187	Flag Name: acc2_pe_flag_8k_err	S
Goal:	Parity prediction of ACC2 HF decimation filter	
Test:	see goal	
Programmable by Customer:	-	
Frequency:	~8kHz	
Source of flag:	ACC Frontend	

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.4 Voltage levels and regulators

7.4.3.4.1 V_Prereg_11_high

F07_9897

Flag Name:	V_Prereg_11_high
Goal:	Check upper voltage limit at VB-Pin
Test:	flag if VB > 17...20V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	Analog Regulator

7.4.3.4.2 V_Prereg_low

F07_9898

Flag Name:	V_Prereg_low
Goal:	Check lower voltage limit at VB-Pin
Test:	flag if VB < 4.17...4.25V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	Analog Regulator

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.4.3 VDD3_high

F07_9899

Flag Name:	VDD3_high
Goal:	Check upper voltage limit at VDD3-Pin
Test:	flag if VDD3 > 3.5 ... 3.6V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	Analog Regulator

7.4.3.4.4 VDD3_low

F07_9900

Flag Name:	VDD3_low
Goal:	Check lower voltage limit at VDD3-Pin
Test:	flag if VDD3 < 3.05 ... 3.1V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	Analog Regulator

7.4.3.4.5 V_CTM_high

F07_9901

Flag Name:	V_CTM_high
Goal:	Check upper voltage limit behind regulator for T-Sensors
Test:	flag if V_CTM > 1.9 ... 2V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

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7.4.3.4.6 V_CTM_low

F07_9902

Flag Name:	V_CTM_low
Goal:	Check lower voltage limit behind regulator for T-Sensors
Test:	flag if $V_{CTM} < 1.65 \dots 1.75V$
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.4.7 V_CP_high

F07_9903

Flag Name:	V_CP_high
Goal:	Check upper voltage limit behind regulator for ChargePump
Test:	flag if $V_{CP} > 3.0 \dots 3.1V$
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.4.8 V_CP_low

F07_10328

Flag Name:	V_CP_low
Goal:	Check if charge pump voltage is $> 16V$.
Test:	Inversebit to "cp_ok" = charge pump ok
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

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7.4.3.4.9 V_YRS_high

F07_9905

Flag Name:	V_YRS_high
Goal:	Check upper voltage limit behind regulator for YR FE
Test:	flag if V_YRS > 3.5...3.6V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.4.10 V_YRS_low

F07_9906

Flag Name:	V_YRS_low
Goal:	Check lower voltage limit behind regulator for YR FE
Test:	flag if V_YRS < 2.78...2.83V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.4.11 V_ACC_high

F07_9907

Flag Name:	V_ACC_high
Goal:	Check upper voltage limit behind regulator for ACC FE
Test:	flag if V_ACC > 2.2...2.4V
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

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7.4.3.4.12 V_ACC_low

F07_9908

Flag Name:	V_ACC_low
Goal:	Check lower voltage limit behind regulator for ACC FE
Test:	flag if $V_{ACC} < 1.8 \dots 1.84V$
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.4.13 V_DIG_high

F07_9909

Flag Name:	V_DIG_high
Goal:	Check upper voltage limit behind regulator for digital core
Test:	flag if $V_{DIG} > 1.9 \dots 2.0V$
Programmable by Customer:	-
Frequency:	continuously collected and interpreted by SW-SCON w/ 2kHz
Source of flag:	SCON(HW)

7.4.3.4.14 V_DIG_low = POR (no flag)

F07_9910

Flag Name:	V_DIG_low = POR (no flag)
Goal:	Check lower voltage limit behind regulator for digital core
Test:	POR if $V_{DIG} < 1.65 \dots 1.8V$
Programmable by Customer:	-
Frequency:	none (on occurrence)
Source of flag:	analog -> POR

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.5 Temperature Checks

7.4.3.5.1 ctm_range

F07_9894

Flag Name:	ctm_range
Goal:	Temperature is checked vs absolute operation condition limits
Test:	Test (SW): Range Check of register TEMP_SENSOR_1_VALUE (15...0) (~200LSB/K) Flag is set if lower or upper limit is reached or exceeded (details see {REF:F07_9495}).
Programmable by Customer:	Absolute limits f_min, f_max
Frequency:	~60 Hz, signal bandwidth 4LSB/sec
Source of flag:	SCON-ADC via SW

7.4.3.5.2 ctm_diff

F07_9895

Flag Name:	ctm_diff
Goal:	Plausibilisation check of the temperature by checking the difference to a 2nd temperature sensor
Test:	Test (SW): Difference Check of registers TEMP_SENSOR_1_VALUE (15...0), TEMP_SENSOR_2_VALUE (15...0) (~200K/LSB) Flag is set if the amount of the temperature difference equals or exceeds the tolerance.
Programmable by Customer:	Absolute tolerance f_diff
Frequency:	~60 Hz, signal bandwidth 4LSB/sec
Source of flag:	SCON-ADC via SW

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.6 DSP flags

7.4.3.6.1 dsp_adjust_data_err

F07_9911

Flag Name:	dsp_adjust_data_err
Goal:	Check integrity of DSP gain adjust data
Test:	Main Adjust Data not corresponding to Checksum Value
Programmable by Customer:	-
Frequency:	~800Hz
Source of flag:	DSP

7.4.3.6.2 dsp_fine_err

F07_9912

Flag Name:	dsp_fine_err
Goal:	Check integrity of DSP fine gain adjust data
Test:	Fine Adjust Data not corresponding to Checksum Value
Programmable by Customer:	Checksum of fine adjust data (in cl. filter selection)
Frequency:	~800Hz
Source of flag:	DSP

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.6.3 dsp_pe_flag_err

F07_9913

Flag Name:	dsp_pe_flag_err
Goal:	Check validity of internal DSP registers
Test:	HW: sDSP parity check of internal Registers
Programmable by Customer:	-
Frequency:	~20 kHz
Source of flag:	DSP

7.4.3.6.4 dsp_pe_sign_err

F07_9914

Flag Name:	dsp_pe_sign_err
Goal:	Monitoring the program flow
Test:	HW: sDSP signature check
Programmable by Customer:	-
Frequency:	~800 Hz
Source of flag:	DSP

7.4.3.6.5 dsp_pe_irq_err

F07_9915

Flag Name:	dsp_pe_irq_err
Goal:	Monitoring of the interrupt module
Test:	HW: sDSP irq-module check
Programmable by Customer:	-
Frequency:	~800 Hz
Source of flag:	DSP

Date: 07/10/2013

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7.4.3.6.6 dsp_ram_ifa13_err

F07_9916

Flag Name:	dsp_ram_ifa13_err
Goal:	Check DSP RAM
Test:	ram_ifa13_err: HW-RAMCHECK of the RAM cells
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

7.4.3.6.7 dsp_ram_soaf_err

F07_9917

Flag Name:	dsp_ram_soaf_err
Goal:	Check DSP address decoder
Test:	ram_soaf_err: HW-RAMCHECK of the address decoder
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

7.4.3.6.8 dsp_ram_dpath

F07_10408

Flag Name:	dsp_ram_dpath
Goal:	Check internal bus structures in the data path of the RAM.
Test:	This test performs simple write and read operations on a single, fixed address.
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

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7.4.3.6.9 dsp_pe_ram_err

F07_9918

Flag Name:	dsp_pe_ram_err
Goal:	Check parity of DSP RAM
Test:	HW: sDSP ram parity_check (parity monitoring of the RAM cells)
Programmable by Customer:	-
Frequency:	~20 kHz
Source of flag:	DSP

7.4.3.6.10 dsp_pe_sqrt_err

F07_10188

Flag Name:	dsp_pe_sqrt_err
Goal:	Check parity in DSP SQRT Module
Test:	HW: sDSP parity check of SQRT Module
Programmable by Customer:	-
Frequency:	~80 0Hz
Source of flag:	DSP

7.4.3.6.11 dsp_neg_flag_sqrt

F07_10189

Flag Name:	dsp_neg_flag_sqrt
Goal:	Negative Input at SQRT Module
Test:	HW: sDSP checks if input of SQRT Module is negative
Programmable by Customer:	-
Frequency:	~80 0Hz
Source of flag:	DSP

Date: 07/10/2013

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7.4.3.6.12 dsp_rom_crc_error

F07_9919

Flag Name:	dsp_rom_crc_error
Goal:	DSP ROM check
Test:	<p>rom_crc_error: ROMCHECK</p> <p>To check the ROM a special hardware is implemented into the design. The ROM is checked by a CRC algorithm. The hardware contains a shift register and a calculation of a CRC polynomial. The hardware can be triggered by a special assembler command. Each time the command is set one value is read out of the ROM and stored into a hardware register. Because of the DSP independent hardware the DSP can run while the hardware will calculate the polynomial. In this way the usage of assembler code and the usage of cycles to calculate the CRC is as few as possible.</p>
Programmable by Customer:	-
Frequency:	~3.2Hz
Source of flag:	DSP

7.4.3.6.13 dsp_ram_toggle_missing

F07_10191

Flag Name:	dsp_ram_toggle_missing
Goal:	DSP RAM toggle is missing
Test:	HW-SCON checks whether DSP RAM Toggle bit is missing
Programmable by Customer:	-
Frequency:	~6.4Hz
Source of flag:	DSP

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.6.14 dsp_rom_toggle_missing

F07_10192

Flag Name:	dsp_rom_toggle_missing
Goal:	DSP ROM toggle is missing
Test:	HW-SCON checks whether DSP ROM Toggle bit is missing
Programmable by Customer:	-
Frequency:	~3.2Hz
Source of flag:	DSP

7.4.3.6.15 dsp_pe_dsp_status_0_err

F07_10193

Flag Name:	dsp_pe_dsp_status_0_err
Goal:	DSP parity check of status register 0
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

7.4.3.6.16 dsp_pe_dsp_status_1_err

F07_10194

Flag Name:	dsp_pe_dsp_status_1_err
Goal:	DSP parity check of status register 1
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

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7.4.3.6.17 dsp_pe_dsp_status_2_err

F07_10195

Flag Name:	dsp_pe_dsp_status_2_err
Goal:	DSP parity check of status register 2
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

7.4.3.6.18 dsp_pe_quad_i_sqrt_udf_err

F07_10196

Flag Name:	dsp_pe_quad_i_sqrt_udf_err
Goal:	DSP parity check of DSP-out-registers QUAD_I and SQRT_UDF
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

7.4.3.6.19 dsp_gp_status

F07_10404

Flag Name:	dsp_gp_status
Goal:	HW-Limiter flag of all primary-Input Limiters of the DSP (YR, Quad and ACC)
Test:	see goal
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

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7.4.3.6.20 dsp_sqrt_lim_flag

F07_10406

Flag Name:	dsp_sqrt_lim_flag
Goal:	Limiter of Output Value of SQRT calculation
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

7.4.3.6.21 dspmém_debugaccess_on

F07_10197

Flag Name:	dspmém_debugaccess_on
Goal:	DSP info flag: DSP is in Debug Mode
Test:	see goal
Programmable by Customer:	-
Frequency:	on demand
Source of flag:	DSP

7.4.3.6.22 dsp_online_test

F07_9920

Flag Name:	dsp_online_test
Goal:	Control the continuing signal processing in the DSP.
Test:	A Built In Self Test (BIST) is implemented in the DSP to control the continuing signal processing in the DSP, consisting in answering 16 control questions asked by the µC. Processing and evaluation of each question takes 2ms.
Programmable by Customer:	-
Frequency:	~32Hz
Source of flag:	µC

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7.4.3.6.23 dsp_acc1_HF_adjust

F07_9921

Flag Name:	dsp_acc1_HF_adjust
Goal:	ACC1: Combined Flag from Limiter of Offset and Gain in HF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

7.4.3.6.24 dsp_acc1_LF_adjust

F07_9922

Flag Name:	dsp_acc1_LF_adjust
Goal:	ACC1: Combined Flag from Limiter of Offset and Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.25 dsp_acc2_HF_adjust

F07_9923

Flag Name:	dsp_acc2_HF_adjust
Goal:	ACC2: Combined Flag from Limiter of Offset and Gain in HF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

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7.4.3.6.26 dsp_acc2_LF_adjust

F07_9924

Flag Name:	dsp_acc2_LF_adjust
Goal:	ACC2: Combined Flag from Limiter of Offset and Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.27 dsp_rate_HF_adjust

F07_9925

Flag Name:	dsp_rate_HF_adjust
Goal:	RATE: Combined Flag from Limiter of Offset and Gain in HF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

7.4.3.6.28 dsp_rate_LF_adjust

F07_9926

Flag Name:	dsp_rate_LF_adjust
Goal:	RATE: Combined Flag from Limiter of Offset and Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

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7.4.3.6.29 dsp_quad_adjust

F07_9927

Flag Name:	dsp_quad_adjust
Goal:	QUAD: Limiter Flag of Gain-Adjust-Block
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

7.4.3.6.30 dsp_ctm1_adjust

F07_9928

Flag Name:	dsp_ctm1_adjust
Goal:	Temperature 1: OR-Binding of Input-Limiter in HF and Input-Limiter of LF Chanel (2 Flags)
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

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7.4.3.6.31 dsp_ctm2_adjust

F07_9929

Flag Name:	dsp_ctm2_adjust
Goal:	Temperature 2: OR-Binding of Input-Limiter in HF and Input-Limiter of LF Chanel (2 Flags)
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.32 dsp_acc1_HF_out

F07_9930

Flag Name:	dsp_acc1_HF_out
Goal:	ACC1: Flag from Limiter before Output-Gain in HF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

7.4.3.6.33 dsp_acc1_LF_out

F07_9931

Flag Name:	dsp_acc1_LF_out
Goal:	ACC1: Flag from Limiter before Output-Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

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7.4.3.6.34 dsp_acc2_HF_out

F07_9932

Flag Name:	dsp_acc2_HF_out
Goal:	ACC2: Flag from Limiter before Output-Gain in HF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

7.4.3.6.35 dsp_acc2_LF_out

F07_9933

Flag Name:	dsp_acc2_LF_out
Goal:	ACC2: Flag from Limiter before Output-Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.36 dsp_HF_out

F07_9934

Flag Name:	dsp_HF_out
Goal:	RATE: Flag from Limiter before Output-Gain in HF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

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7.4.3.6.37 dsp_LF_out

F07_9935

Flag Name:	dsp_LF_out
Goal:	RATE: Flag from Limiter before Output-Gain in LF-Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.38 dsp_acc1_HF_in

F07_9936

Flag Name:	dsp_acc1_HF_in
Goal:	ACC1: Flag from Input Limiter in HF-Path
Test:	Check vs and clip the signal to asymmetrically adjustable limits (in order to prevent asymmetrical clipping). This limit should be the "bottleneck"; no subsequent limiters should be activated prior to this limiter.
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

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**7.4.3.6.39 dsp_acc1_LF_in**

F07_9937

Flag Name:	dsp_acc1_LF_in
Goal:	ACC1: Flag from Input Limiter in LF-Path
Test:	Check vs and clip the signal to asymmetrically adjustable limits (in order to prevent asymmetrical clipping). This limit should be the "bottleneck"; no subsequent limiters should be activated prior to this limiter.
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.40 dsp_acc2_HF_in

F07_9938

Flag Name:	dsp_acc2_HF_in
Goal:	ACC2: Flag from Input Limiter in HF-Path
Test:	Check vs and clip the signal to asymmetrically adjustable limits (in order to prevent asymmetrical clipping). This limit should be the "bottleneck"; no subsequent limiters should be activated prior to this limiter.
Programmable by Customer:	-
Frequency:	~8kHz
Source of flag:	DSP

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7.4.3.6.41 dsp_acc2_LF_in

F07_9939

Flag Name:	dsp_acc2_LF_in
Goal:	ACC2: Flag from Input Limiter in LF-Path
Test:	Check vs and clip the signal to asymmetrically adjustable limits (in order to prevent asymmetrical clipping). This limit should be the "bottleneck"; no subsequent limiters should be activated prior to this limiter.
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

7.4.3.6.42 dsp_quad_QI_lim

F07_9940

Flag Name:	dsp_quad_QI_lim
Goal:	QUAD: Limiter of I-Control
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~2kHz
Source of flag:	DSP

7.4.3.6.43 dsp_cq_high_lim

F07_9941

Flag Name:	dsp_cq_high_lim
Goal:	QUAD: Limiter Flag of CQ Demodulation Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~1kHz
Source of flag:	DSP

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7.4.3.6.44 dsp_cq_low_lim

F07_9942

Flag Name:	dsp_cq_low_lim
Goal:	QUAD: Limiter Flag of CQ Demodulation Path
Test:	see "goal"
Programmable by Customer:	-
Frequency:	~69.5Hz
Source of flag:	DSP

7.4.3.7 Bus error flags

7.4.3.7.1 ctm_apb_slv

F07_9943

Flag Name:	ctm_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within CTM module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	CTM



7.4.3.7.2 misc_apb_slv

F07_9944

Flag Name:	misc_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within MISC module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	MISC

7.4.3.7.3 main_ctrl_apb_slv

F07_9945

Flag Name:	main_ctrl_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within Main Control module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Main_Ctrl

7.4.3.7.4 dsp_apb_slv

F07_9946

Flag Name:	dsp_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within DSP address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

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7.4.3.7.5 dsp_ram_apb_slv

F07_9947

Flag Name:	dsp_ram_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within DSP address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

7.4.3.7.6 dsp_rom_apb_slv

F07_9948

Flag Name:	dsp_rom_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within DSP address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	DSP

7.4.3.7.7 hw_scon_apb_slv

F07_9949

Flag Name:	hw_scon_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within SCON-HW module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	HW_SCON

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7.4.3.7.8 conf_apb_slv

F07_9950

Flag Name:	conf_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within CONFIG module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Config_reg

7.4.3.7.9 can_apb_slv

F07_9951

Flag Name:	can_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within CAN module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	CAN

7.4.3.7.10 frontend_apb_slv

F07_9952

Flag Name:	frontend_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within frontend address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Frontend

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7.4.3.7.11 psi_apb_slv

F07_9953

Flag Name:	psi_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within PSI module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	PSI

7.4.3.7.12 spi_apb_slv

F07_9954

Flag Name:	spi_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within SPI module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	SPI

7.4.3.7.13 spi_mst_apb_slv

F07_9955

Flag Name:	spi_mst_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within SPI Master module address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	SPI_Master

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7.4.3.7.14 gpt_apb_slv

F07_9956

Flag Name:	gpt_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within General Purpose Timer address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	GPT

7.4.3.7.15 uc_sub_apb_slv

F07_9957

Flag Name:	uc_sub_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within µC subsystem address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	uC_system

7.4.3.7.16 sfr_apb_slv

F07_9958

Flag Name:	sfr_apb_slv
Goal:	Detect illegal bus transfer to internal module
Test:	Illegal Read/Write access on APB Bus within µC subsystem address range
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	Special Function Register

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7.4.3.7.17 ahb_hang_up

F07_9959

Flag Name:	ahb_hang_up
Goal:	Detect dead lock on AHB bus
Test:	Non-terminated Read/Write access on AHB bus
Programmable by Customer:	-
Frequency:	for each bus transfer
Source of flag:	uC_system

7.4.3.8 LBIST

7.4.3.8.1 lbist_err

F07_9961

Flag Name:	lbist_err
Goal:	LBIST/Scan during Power on
Test:	see LBIST description {REF:F07_10159}
Programmable by Customer:	-
Frequency:	at startup only
Source of flag:	Main_Ctrl

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.9 Memory error flags

7.4.3.9.1 can_ram_parity

F07_9962

Flag Name:	can_ram_parity
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	~20 kHz
Source of flag:	CAN

7.4.3.9.2 uc_ram_par_error

F07_9963

Flag Name:	uc_ram_par_error
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	~20 kHz
Source of flag:	uC_system

7.4.3.9.3 uc_ram_dpath

F07_9964

Flag Name:	uc_ram_dpath
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	~110Hz
Source of flag:	uC_system



7.4.3.9.4 uc_ram_ifa13

F07_9965

Flag Name:	uc_ram_ifa13
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	~110Hz
Source of flag:	uC_system

7.4.3.9.5 uc_ram_soaf

F07_9966

Flag Name:	uc_ram_soaf
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	~110Hz
Source of flag:	uC_system

7.4.3.9.6 uc_rom_bist

F07_9967

Flag Name:	uc_rom_bist
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	> 50Hz (depending on uC OTP activity)
Source of flag:	uC_system

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7.4.3.9.7 uc_otp_data_bist

F07_9968

Flag Name:	uc_otp_data_bist
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	> 50Hz (depending on uC OTP activity)
Source of flag:	uC_system

7.4.3.9.8 uc_otp_prog_bist

F07_9969

Flag Name:	uc_otp_prog_bist
Goal:	see chapter "Safety control of memory element" {REF:F07_1130}
Test:	dito
Programmable by Customer:	-
Frequency:	~180Hz
Source of flag:	uC_system

7.4.3.9.9 uc_ram_toggle_missing

F07_10198

Flag Name:	uc_ram_toggle_missing
Goal:	uC RAM toggle is missing
Test:	uC System checks whether uC-Ram toggle bit is missing
Programmable by Customer:	-
Frequency:	~50Hz
Source of flag:	uC_system

Date: 07/10/2013

Dept.: AE/NE4



7.4.3.9.10 uc_rom_toggle_missing

F07_10199

Flag Name:	uc_rom_toggle_missing
Goal:	uC ROM toggle is missing
Test:	uC System checks wether uC-Rom toggle bit is missing
Programmable by Customer:	-
Frequency:	~50 Hz
Source of flag:	uC_system

7.4.3.9.11 otp_data_toggle_missing

F07_10200

Flag Name:	otp_data_toggle_missing
Goal:	Data OTP memory check toggle bit is missing
Test:	uC System checks wether Data-OTP toggle bit is missing
Programmable by Customer:	-
Frequency:	~50 Hz
Source of flag:	uC_system

7.4.3.9.12 otp_prog_toggle_missing

F07_10201

Flag Name:	otp_prog_toggle_missing
Goal:	Program OTP memory check toggle bit is missing
Test:	uC System checks wether PROG-OTP toggle bit is missing
Programmable by Customer:	-
Frequency:	~50 Hz
Source of flag:	uC_system

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7.4.3.10 Pin Checks

7.4.3.10.1 pc_vssa

F07_9970

Flag Name:	pc_vssa
Goal:	Voltage difference between VSSA,VSSD and PSI5_M to each other (due to bond ruptures).
Test:	HW-Check: Difference > 300mV
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 μ sec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.10.2 pc_vssd

F07_9971

Flag Name:	pc_vssd
Goal:	Voltage difference between VSSA,VSSD and PSI5_M to each other (due to bond ruptures).
Test:	HW-Check: Difference > 300mV
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 μ sec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

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7.4.3.10.3 pc_psi5_m

F07_9972

Flag Name:	pc_psi5_m
Goal:	Voltage difference between VSSA,VSSD and PSI5_M to each other (due to bond ruptures).
Test:	HW-Check: Difference > 300mV
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.10.4 pc_shd

F07_9973

Flag Name:	pc_shd
Goal:	To check SHD,SUBSTR CMG bond connection, a small test current is injected into SHD. If SHD or SUBSTR bond is open, then a voltage rise at the injection point is recognized and the appropriate fault flag is set.
Test:	Injection current for CS1 and SHD pins: 1-3µA
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.10.5 pc_cs1

F07_9974

Flag Name:	pc_cs1
Goal:	To check CS1,CS2 bond connection, a small test current is injected into CS1. If CS1 or CS2 bond is open, then a voltage rise at the injection point is recognized and the appropriate fault flag is set.
Test:	Injection current for CS1 and SHD pins: 1-3µA
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 µsec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

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7.4.3.10.6 pc_cp

F07_9976

Flag Name:	pc_cp
Goal:	Voltage ripple for detection connection rupture of outside blocking capacitor at CP The flag pc_cp is raised in case of a detected bond rupture. In case of applying an external AC-voltage with an amplitude above 100 mV (for example EMC disturbances) and a frequency above 100 KHz CP, the flag pc_cp may also be activated.
Test:	HW-Check: Ripple > 100mVpp (high-pass filtered with ~100kHz)
Programmable by Customer:	-
Frequency:	All checking is done serially. Every bond-rupture will be detected after 12 μ sec. (slowest PLL frequency) -> 83kHz
Source of flag:	SCON(HW)

7.4.3.11 μ C watchdog

7.4.3.11.1 uc_watchdog_err

F07_7025

Flag Name:	uc_watchdog_err
Goal:	HW-SCON asks questions to μ C, answers are compared to predefined results.
Test:	Flag is set if μ C answer does not equal the expected value. For detailed description, see text {REF:F07_10166}
Programmable by Customer:	-
Frequency:	~55 Hz (18ms)
Source of flag:	SCON(HW)

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7.4.3.12 Electromechanical self tests (BITEs)

7.4.3.12.1 yrs_rate_seq_bite

F07_997Z

Flag Name:	yrs_rate_seq_bite
Goal:	Bite sequence "Rate" failed in rate test
Test:	<p>Test (SW): Symmetric Range Check of register RATE_BITE_POS_NEG (15...0). Flag is set as soon as limits are reached or exceeded.</p> <p>The register RATE_BITE_POS_NEG will be set by the SW itself by calculating the rate difference between "positive BITE excitation" and "negative BITE excitation":</p> $\text{RATE_BITE_POS_NEG} = \text{RATE_HF_LIMITED} (\text{t} = \text{end of positive BITE}) (15...0) - \text{RATE_HF_LIMITED} (\text{t} = \text{end of negative BITE}) (15...0)$ <p>For further details, see {REF:F07_7046}.</p>
Programmable by Customer:	Absolute tolerance f_tol
Frequency:	on request
Source of flag:	SW

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7.4.3.12.2 yrs_quad_seq_bite

F07_9978

Flag Name:	yrs_quad_seq_bite
Goal:	Bite sequence "Rate" failed in quad test
Test:	<p>Test (SW): This flag evaluates the Quadrature signal during the yaw rate BITE sequence.</p> <p>The flag is set if one of the following three conditions (sub-flags) is set:</p> <p>yrs_quad_bite_pos_zero yrs_quad_bite_neg_zero yrs_quad_bite_pos_neg</p> <p>yrs_quad_bite_pos_zero is the result of a Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Zero_BITE_QUAD (15...0) = QUAD_HF_LIMITED (t = end of positive BITE) (15...0) - QUAD_HF_LIMITED (t = end of zero BITE) (15...0)</p> <p>yrs_quad_bite_neg_zero is the result of a Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Zero_BITE_QUAD (15...0) = QUAD_HF_LIMITED (t = end of negative BITE) (15...0) - QUAD_HF_LIMITED (t = end of zero BITE) (15...0)</p> <p>yrs_quad_bite_pos_neg is the result of a Temperature dependent Tolerance Check (TDTC) of the internal value Pos_Zero_BITE_QUAD (15...0) = QUAD_HF_LIMITED (t = end of positive BITE) (15...0) - QUAD_HF_LIMITED (t = end of negative BITE) (15...0)</p> <p>For further details, see {REF:F07_7046}.</p>
Programmable by Customer:	Relative tolerances f_tol (pos-zero) f_tol (neg-zero) f_tol (pos-neg)
Frequency:	on request
Source of flag:	SW

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7.4.3.12.3 acc1_seq_bite

F07_9979

Flag Name:	acc1_seq_bite
Goal:	Bite sequence ACC1 failed
Test:	<p>Test (SW): Temperature dependent Tolerance Check (TDTC) of the internal value</p> <p>Pos_Neg_BITE_ACC1 (15...0)</p> <p>The value Pos_Neg_BITE_ACC1 will be set by the SW itself by calculating the rate difference between "positive BITE excitation" and "negative BITE excitation":</p> <p>Pos_Neg_BITE_ACC1 =</p> <p>ACC1_HF_LIMITED (t = end of positive BITE) (15...0) -</p> <p>ACC1_HF_LIMITED (t = end of negative BITE) (15...0)</p> <p>For further details, see {REF:F07_7046}</p>
Programmable by Customer:	Relative tolerance f_tol
Frequency:	on request
Source of flag:	SW

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7.4.3.12.4 acc2_seq_bite

F07_9980

Flag Name:	acc2_seq_bite
Goal:	Bite sequence AC C2 failed
Test:	<p>Test (SW): Temperature dependent Tolerance Check (TDTC) of the internal value</p> <p>Pos_Neg_BITE_ACC2 (15...0)</p> <p>The value Pos_Neg_BITE_ACC2 will be set by the SW itself by calculating the rate difference between "positive BITE excitation" and "negative BITE excitation":</p> <p>Pos_Neg_BITE_ACC2 = ACC2_HF_LIMITED (t = end of positive BITE) (15...0) - ACC2_HF_LIMITED (t = end of negative BITE) (15...0)</p> <p>For further details, see {REF:F07_7046}</p>
Programmable by Customer:	Relative tolerance f_tol
Frequency:	on request
Source of flag:	SW

7.4.3.13 µC and SW errors

7.4.3.13.1 uc_otp_prog_bist_inital

F07_9982

Flag Name:	uc_otp_prog_bist_inital
Goal:	Code OTP is secured against corruption by CRC-Check. The SW-Function 'void OtpCodeCheck()' located in the ROM-SW initiates a one-Shot CRC over the entire code OTP, before any code from the Code OTP is executed. One shot CRC check is used to detect bad programming of OTP cells. If the one-shot CRC check fails, the mC error flag 'uc_otp_prog_bist_inital' will be generated.
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

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7.4.3.13.2 uc_otp_data_bist_initial

F07_9983

Flag Name:	uc_otp_data_bist_initial
Goal:	CRC error during initial check of Data OTP (CRC of a bank in OTP does not match)
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

7.4.3.13.3 uc_otp_data_corrupt_header

F07_9984

Flag Name:	uc_otp_data_corrupt_header
Goal:	Module or Device Header contain inconsistent data.
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

7.4.3.13.4 uc_otp_data_invalid_tuple

F07_9985

Flag Name:	uc_otp_data_invalid_tuple
Goal:	Bootloader found an invalid tuple (with unknown type or an invalid destination address)
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

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7.4.3.13.5 uc_tuple_readback_mismatch

F07_9986

Flag Name:	uc_tuple_readback_mismatch
Goal:	A value read back by the bootloader from a register or µC RAM did not match the value just written to it.
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

7.4.3.13.6 uc_stack_check

F07_9987

Flag Name:	uc_stack_check
Goal:	At the start of each main cycle the stack is checked for over- or underrun during the last main cycle. The overrun check is done by checking if a specific marker which is placed just below (the stack grows from top of the RAM downwards) the last allowed entry for any change (caused by the stack overwriting it). The underrun check is done by checking if the stack is empty (again) at the start of the main cycle (indicated by the stack pointer returning to its initial value). This Flag is set when the µC software detects any stack size deviation.
Test:	see goal
Programmable by Customer:	-
Frequency:	2kHz
Source of flag:	SW

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7.4.3.13.7 uc_hw_timeout

F07_9988

Flag Name:	uc_hw_timeout
Goal:	Flag is not linked to any monitor. (It was foreseen resp. planned to be set when the µC SW runs into a timeout while waiting for a hw response, but actually there is no meaningful purpose for it)
Test:	see goal
Programmable by Customer:	-
Frequency:	2kHz
Source of flag:	SW

7.4.3.13.8 uc_psi_async_timing

F07_9989

Flag Name:	uc_psi_async_timing
Goal:	This was a place holder and is not being used. PSI-Async-Timing problems are being handled in the PSI SW.
Test:	-
Programmable by Customer:	-
Frequency:	-
Source of flag:	SW

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**7.4.3.13.9 uc_unrecoverable_error**

F07_9990

Flag Name:	uc_unrecoverable_error
Goal:	A state variable contains an invalid (not used) value. The further execution of the related state machine would be undefined.
Test:	see goal
Programmable by Customer:	-
Frequency:	on occurrence
Source of flag:	SW

7.4.3.13.10**uc_rom_otp_sw_incompatible**

F07_9991

Flag Name:	uc_rom_otp_sw_incompatible
Goal:	OTP SW version does not match to ROM SW version
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

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**7.4.3.13.11****uc_can_psi_readback_mismatch**

F07_9992

Flag Name:	uc_can_psi_readback_mismatch
Goal:	To avoid errors on the transfer of data from µC RAM to the CAN or PSI modules message buffers, the data written to the message buffer is read back. If a mismatch is detected on the read back data, the µC sets this flag.
Test:	see goal
Programmable by Customer:	-
Frequency:	once per can/psi-write
Source of flag:	SW

7.4.3.13.12**uc_otp_data_open_bank**

F07_9993

Flag Name:	uc_otp_data_open_bank
Goal:	A bank in the data OTP is programmed with tuples but its end_of_bank address is not written in header bank
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW



7.4.3.13.13

uc_generic_error_flag_2

F07_10398

Flag Name:	uc_generic_error_flag_2
Goal:	= uc_DSP_parity_err: Any parity error was detected when the uC sampled data from the DSP. The Parity will be handled application-specific (e.g. status-flag in PSI/CAN-message).
Test:	see goal
Programmable by Customer:	-
Frequency:	on occurrence
Source of flag:	SW

7.4.3.13.14

uc_generic_error_flag_3

F07_10400

Flag Name:	uc_generic_error_flag_3
Goal:	= uc_registercheck_err: An error occurred during the CRC check of critical configuration registers (test carried out by the uC). Since this flag is handled within the tasks of the uc_watchdog_err, the frequency is the same.
Test:	see goal
Programmable by Customer:	-
Frequency:	~55 Hz (18ms)
Source of flag:	SW



7.4.3.13.15

uc_generic_error_flag_4

F07_10402

Flag Name:	uc_generic_error_flag_4
Goal:	= uc_yrs_drive_restart: Indicator flag (no error) that is risen in case the yaw rate drive path can not be locked successfully in the first trial and needs to be restarted with a slightly different starting parameters.
Test:	see goal
Programmable by Customer:	-
Frequency:	startup
Source of flag:	SW

7.4.3.14 Flag numbering

F07_9510

For configuration of flag weights and variable error counters each flag is referenced by its unique flag number. This number is also being used for error memory entries (see 1.4.2.4).

1	lbist_err	81	dsp_acc2_HF_out
2	v_cp_high	82	dsp_acc2_LF_out
3	v_cp_low	83	dsp_cq_high_lim
4	v_yrs_high	84	dsp_cq_low_lim
5	v_yrs_low	85	dsp_quad_QI_lim
6	v_acc_high	86	dsp_pe_flag_err
7	v_acc_low	87	dsp_pe_sign_err
8	v_dig_high	88	dsp_pe_irq_err
9	v_ctm_high	89	dsp_pe_ram_err
10	v_ctm_low	90	dsp_pe_sqrt_err
11		91	dsp_neg_flag_sqrt
12	v_prereg_low	92	yrs_quad_hf_tol
13	v_prereg_11_high	93	yrs_quad_i_tol
14	vdd3_high	94	dsp_online_test

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15	vdd3_low	95	yrs_rate_seq_bite
16		96	yrs_quad_seq_bite
17		97	
18	pc_vssa	98	
19	pc_vssd	99	
20	pc_psi5_m	100	acc1_seq_bite
21	pc_shd	101	acc2_seq_bite
22	pc_cs1	102	dsp_ram_ifa13_err
23	pc_cp	103	dsp_ram_soaf_err
24	yrs_rate_v_tn	104	dsp_rom_crc_error
25	yrs_rate_v_com	105	dspmem_debugaccess_on
26	yrs_rate_v_cm	106	can_ram_parity
27	yrs_rate_v_fb	107	ahb_hang_up
28	yrs_drv_adc	108	uc_rom_bist
29	yrs_rate_adc	109	uc_ram_ifa13
30	yrs_drv_cu_gain	110	uc_ram_soaf
31	yrs_rate_quantizer	111	
32	yrs_drv_bp_lim	112	uc_ram_dpath
33	yrs_rate_adc_mean	113	uc_otp_data_bist
34	yrs_drv_adc_mean	114	uc_otp_prog_bist
35	yrs_pll_lim	115	uc_ram_par_error
36	yrs_pll_tol	116	uc_watchdog_err
37	yrs_pll_unlock	117	uc_otp_prog_bist_inital
38	yrs_rate_pt2_lim	118	uc_otp_data_bist_inital
39	yrs_drv_pi_tol	119	uc_otp_data_corrupt_header
40	yrs_agc_irregular	120	uc_otp_data_invalid_tuple



41	pe_flag_cic4_err	121	uc_tuple_readback_mismatch
42	pe_flag_quad_2k_err	122	uc_stack_check
43	pe_flag_quad_8k_err	123	uc_hw_timeout
44	pe_flag_rate_8k_err	124	uc_psi_async_timing
45	pe_flag_rate_1k_err	125	uc_unrecoverable_error
46	acc1_v_cm	126	uc_rom_otp_sw_incompatible
47	acc2_v_cm	127	uc_can_psi_readback_mismatch
48	acc_clk_ovlp	128	uc_otp_data_open_bank
49	acc1_clk_cnt	129	uc_generic_error_flag_2
50	acc2_clk_cnt	130	uc_generic_error_flag_3
51	acc2_overload_det	131	uc_generic_error_flag_4
52	acc1_overload_det	132	ctm_apb_slv
53	acc1_ds_lim	133	misc_apb_slv
54	acc2_ds_lim	134	main_ctrl_apb_slv
55	acc1_pe_flag_8k_err	135	dsp_apb_slv
56	acc1_pe_flag_1k_err	136	conf_apb_slv
57	acc2_pe_flag_8k_err	137	can_apb_slv
58	acc2_pe_flag_1k_err	138	frontend_apb_slv
59	dsp_acc1_HF_in	139	psi_apb_slv
60	dsp_acc1_LF_in	140	spi_apb_slv
61	dsp_acc2_HF_in	141	spi_mst_apb_slv
62	dsp_acc2_LF_in	142	gpt_apb_slv
63	ctm_range	143	uc_sub_apb_slv
64	ctm_diff	144	hw_scon_apb_slv
65		145	sfr_apb_slv
66	dsp_adjust_data_err	146	dsp_rom_apb_slv

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67	dsp_fine_err	147	dsp_ram_apb_slv
68	dsp_rate_HF_adjust	148	dsp_ram_toggle_missing
69	dsp_rate_LF_adjust	149	dsp_rom_toggle_missing
70	dsp_acc1_HF_adjust	150	uc_ram_toggle_missing
71	dsp_acc1_LF_adjust	151	uc_rom_toggle_missing
72	dsp_acc2_HF_adjust	152	otp_data_toggle_missing
73	dsp_acc2_LF_adjust	153	otp_prog_toggle_missing
74	dsp_quad_adjust	154	dsp_sqrt_lim_flag
75	dsp_ctm1_adjust	155	dsp_gp_status
76	dsp_ctm2_adjust	156	dsp_pe_dsp_status_0_err
77	dsp_HF_out	157	dsp_pe_dsp_status_1_err
78	dsp_LF_out	158	dsp_pe_dsp_status_2_err
79	dsp_acc1_HF_out	159	dsp_pe_quad_i_sqrt_udf_err
80	dsp_acc1_LF_out	160	dsp_ram_dpath

7.4.4 Overview of flag effects

[F07_7030](#)

In the following table, the flags and their effects are summarized. The first column "Weight on FC's" describes the SMI7 standard configuration for the individual flag weights (see [{REF:F07_7032}](#)). The next 6 columns describe the effects on the failure counters (see 1.4.2), followed by the marking if the individual flag is empowered to overwrite the channel information bits evaluated by the Software (hard overwriting of channel information is always permanent for the current power-on cycle, see [{REF:F07_7034}](#)) or to disable the CAN or PSI interface, or if a POR (Power-On Reset) of the sensor is triggered. There is no mechanism for disabling the running SPI interface. The SPI interface will only be released if initial CRC checks of the program and data otp are successful.

In the 16 columns on the right-hand side, it is described on which bit of the 16bit-Summary-Cluster the flag is acting.

The categories F16_MEMORY and F16_UC_WD are set by the SCON-HW, all other categories are set by the SW.

F16_ST_RUNNING and F16_INIT are informative status flags (informative means: the signal is invalid because of "INIT phase" or "BITE phase" running, not because of failures).

The categories describe the potential source of the flag (e.g., external influences like EMC and/or PSRR, vibration, supply etc.) besides hardware errors.

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Reutlingen

Data Sheet

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Flag Name	Weight on FC's	Effect on Failure Counter (FC's)						16bit Cluster Flags																			
		acts on failure counter...																									
		FC_YR_LF	FC_YR_HF	FC_ACC2_LF	FC_ACC2_HF	FC_ACCL_LF	FC_ACCL_HF	Hw-Overwrite Ci-Flags on all channels to Ci-Status 10 and µC-Interrupt	CAN_DISABLE = wDG1_DISABLE	PSL_DISABLE	POR	F16_MEMORY	F16_UC_WD	F16_MECH_OVERLOAD_ACC2	F16_F_CHECK	F16_MEMORY_DATA_AND_DSP	F16_SW	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMCP_SRR	F16_SUPPLY	F16_TEMP	F16_CQBIT	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC1	F16_INIT	F16_ST_RUN
YR Drive												15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
yrs_ago_irregular	01	x	x																1	1							
yrs_drv_pi_tol	01	x	x																1	1							
yrs_drv_bp_lim	01	x	x																1	1							
yrs_drv_adc_mean	01	x	x																1	1							
yrs_drv_cu_gain	01	x	x																1	1							
yrs_pll_lim	01	x	x																1	1							
yrs_pll_tol	01	x	x																1	1							
yrs_pll_unlock	01	x	x																1	1							
yrs_drv_adc	01	x	x																1	1							
YR Detection																			1	1							
yrs_quad_l_tol	01	x	x																1	1							
yrs_quad_HF_tol	01	x	x																1	1							
yrs_rate_pt2_lim	01	x	x																1	1							
yrs_rate_quantizer	01	x	x																1	1							
yrs_rate_adc_mean	01	x	x																1	1							
yrs_rate_adc	01	x	x																1	1							
yrs_rate_V_TN	01	x	x																1								
yrs_rate_V_com	01	x	x																1								
yrs_rate_V_fb	01	x	x																1								
yrs_rate_V_CM	01	x	x																1								
pe_flag_rate_8k_err	00		x																1								
pe_flag_rate_1k_err	00	x																	1								
pe_flag_quad_8k_err	00	x	x																1								
pe_flag_quad_2k_err	00	x	x																1								
pe_flag_cio4_err	00	x	x																1								

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Flag Name	Weight on FC's	Effect on Failure Counter (FC's)						Hw-Overwrite Ci-Flags on all channels to Ci-Status 10 and μC-Interrupt	16bit Cluster Flags						Hw-Overwrite Ci-Flags on all channels to Ci-Status 10 and μC-Interrupt	16bit Cluster Flags	Hw-Overwrite Ci-Flags on all channels to Ci-Status 10 and μC-Interrupt	16bit Cluster Flags	Hw-Overwrite Ci-Flags on all channels to Ci-Status 10 and μC-Interrupt	16bit Cluster Flags		
		acts on failure counter...																				
		FC_YRLF	FC_YRH.F	FC_ACC2_LF	FC_ACC2_HF	FC_ACCL_F	FC_ACCL_HF		PSL_DISABLE	POR	F16_MEMORY	F16_UC_WD	F16_MECH_OVERLOAD_ACC2	F16_F_CHECK	F16_MEMORY_DATA_AND_DSP	F16_SW'	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMIC_PSRR	F16_CGBITE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC1
ACC																						
acc1_clk_cnt	00																					
acc2_clk_cnt	00			X	X																	
acc_olk_ovlp	00		X	X	X	X	X															
acc1_V_cm	01																					
acc2_V_cm	01		X	X	X	X	X															
acc1_ds_lim	01																					
acc2_ds_lim	01		X	X	X	X	X															
acc1_overload_det	01					X	X															
acc2_overload_det	01		X	X	X	X	X															
acc1_pe_flag_1k_err	00							X														
acc2_pe_flag_1k_err	00			X																		
acc2_pe_flag_8k_err	00				X																	
Voltage Regulators																						
V_Prereg_11_high	01	X	X	X	X	X	X															
V_Prereg_low	01	X	X	X	X	X	X															
VDD3_high	01	X	X	X	X	X	X															
VDD3_low	01	X	X	X	X	X	X															
V_CTM_high	01	X	X	X	X	X	X															
V_CTM_low	01	X	X	X	X	X	X															
V_CP_high	01	X	X																			
V_CP_low	01	X	X																			
V_YRS_high	01	X	X																			
V_YRS_low	01	X	X																			
V_ACC_high	01		X	X	X	X	X															
V_ACC_low	01		X	X	X	X	X															
V_DIG_high	00	X	X	X	X	X	X								1	1						
V_DIG_low = POR (no flag)	-															1						
Temperature Check																						
ctm_range	01	X	X	X	X	X	X															1
ctm_diff	01	X	X	X	X	X	X															1

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Data Sheet

SMI7

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Flag Name	Effect on Failure Counter (FC's)						16 bit Cluster Flags										16 bit Cluster Flags												
	acts on failure counter...						16 bit Cluster Flags										16 bit Cluster Flags												
	FC_YR_LF	FC_YR_HF	FC_ACC2_LF	FC_ACC2_HF	FC_ACC1_LF	FC_ACC1_HF	HW-Overwrite Configuration on all channels to CI-State or IO and µC-Interrupt			CAN_DISABLE = WDG1_DISABLE	PSEL_DISABLE	POR	F16_MEMORY	F16_UC_WD	F16_MECH_OVERLOAD_ACQ2	F16_F_CHECK	F16_MEMORY_DATA_AND_DSP	F16_SW	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMC_PSR	F16_SUPPLY	F16_TEMP	F16_OBITE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACQ1	F16_INIT	F16_ST_RUN	
DSP incl. DSP-Mem																													
dsp_adjust_data_err	00	X	X	X	X	X	X	X	X								1												
dsp_fine_err	00	X	X	X	X	X	X	X	X								1												
dsp_pc_flag_err	00	X	X	X	X	X	X	X	X																				
dsp_pc_sign_err	00	X	X	X	X	X	X	X	X																				
dsp_pc_irq_err	00	X	X	X	X	X	X	X	X																				
dsp_rom_ifail3_err	00	X	X	X	X	X	X	X	X																				
dsp_rom_soaf_err	00	X	X	X	X	X	X	X	X																				
dsp_rom_dpath	00	X	X	X	X	X	X	X	X																				
dsp_pc_ram_err	00	X	X	X	X	X	X	X	X																				
dsp_pc_sqrit_err	00	X	X																										
dsp_neg_flag_sqrit	00	X	X																										
dsp_rom_crc_error	00	X	X	X	X	X	X	X	X																				
dsp_rom_toggle_missing	00	X	X	X	X	X	X	X	X																				
dsp_rom_toggle_missing	00	X	X	X	X	X	X	X	X																				
dsp_pc_dsp_status_0_err	00	X	X	X	X	X	X	X	X																				
dsp_pc_dsp_status_1_err	00	X	X	X	X	X	X	X	X																				
dsp_pc_dsp_status_2_err	00	X	X	X	X	X	X	X	X																				
dsp_pc_quad_L_sqrit_wdf_err	00	X	X																										
dsp_gp_status	00	X	X	X	X	X	X	X	X																				
dsp_sqrit_lim_flag	00	X	X																										
dspmem_debugaccess_on	00	X	X	X	X	X	X	X	X																				
dsp_online_test	00	X	X	X	X	X	X	X	X																				
dsp_accel_HF_adjust	00																												
dsp_accel_LF_adjust	00																												
dsp_accel2_HF_adjust	00																												
dsp_accel2_LF_adjust	00																												
dsp_rate_HF_adjust	00																												
dsp_rate_LF_adjust	00																												
dsp_quad_adjust	00																												
dsp_ctm1_L_adjust	00	X	X	X	X	X	X	X	X																				
dsp_ctm2_adjust	00	X	X	X	X	X	X	X	X																				
dsp_accel_HF_out	01																												1
dsp_accel_LF_out	01																												1
dsp_accel2_HF_out	01																												
dsp_accel2_LF_out	01																												
dsp_ctm1_HF_out	01																												
dsp_ctm2_HF_out	01																												
dsp_ctm1_LF_out	01																												
dsp_ctm2_LF_out	01																												
dsp_accel_HF_in	01																												
dsp_accel2_HF_in	01																												
dsp_accel_LF_in	01																												
dsp_accel2_LF_in	01																												
dsp_quad_GL_lim	01	X	X																										
dsp_cq_high_lim	01	X	X																										1
dsp_cq_low_lim	01	X	X																										1

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Data Sheet

SMI7

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Flag Name	Effect on Failure Counter (FC's)						16bit Cluster Flags																		
	acts on failure counter...																								
	Weight on FC's	FC_YR_LF	FC_YR_HF	FC_ACC2_LF	FC_ACC2_HF	FC_ACCL_LF	FC_ACCL_HF	CAN_DISABLE = wDIGI_DISABLE	PSL_DISABLE	POR	F16_MEMORY	F16_UC_WD	F16_MECH_OVERLOAD_ACC2	F16_F_CHECK	F16_MEMORY_DATA_AND_DSP	F16_SW	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMIC_PSRR	F16_SUPPLY	F16_TEMP	F16_COBITE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC1	F16_INIT
Bus																									
ctm_apb_slv	00	x	x	x	x	x	x																		
misc_apb_slv	00	x	x	x	x	x	x																		
main_ctrl_apb_slv	00	x	x	x	x	x	x																		
dsp_apb_slv	00	x	x	x	x	x	x																		
dsp_ram_apb_slv	00	x	x	x	x	x	x																		
dsp_rom_apb_slv	00	x	x	x	x	x	x																		
hw_soon_apb_slv	00	x	x	x	x	x	x																		
conf_apb_slv	00	x	x	x	x	x	x																		
can_apb_slv	00	x	x	x	x	x	x																		
frontend_apb_slv	00	x	x	x	x	x	x																		
psi_apb_slv	00	x	x	x	x	x	x																		
spi_apb_slv	00	x	x	x	x	x	x																		
spi_mst_apb_slv	00	x	x	x	x	x	x																		
gpt_apb_slv	00	x	x	x	x	x	x																		
uc_sub_apb_slv	00	x	x	x	x	x	x																		
sfr_apb_slv	00	x	x	x	x	x	x																		
ahb_hang_up	00	x	x	x	x	x	x																		
Digital Test																									
ibist_err	00	x	x	x	x	x	x				1	1													
Memory																									
can_ramparity											1		1												
uc_rampar_error	00	x	x	x	x	x	x				x	1	1	1											
uc_ram_dpath	00	x	x	x	x	x	x				x	1	1	1											
uc_ram_ifa13	00	x	x	x	x	x	x				x	1	1	1											
uc_ram_soaf	00	x	x	x	x	x	x				x	1	1	1											
uc_rom_bist	00	x	x	x	x	x	x				x	1	1	1											
uc_otp_data_bist	00	x	x	x	x	x	x				x	1	1	1											
uc_otp_prog_bist	00	x	x	x	x	x	x				x	1	1	1											
uc_ram_toggle_missing	01	x	x	x	x	x	x																		
uc_rom_toggle_missing	01	x	x	x	x	x	x																		
otp_data_toggle_missing	01	x	x	x	x	x	x																		
otp_prog_toggle_missing	01	x	x	x	x	x	x																		

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Flag Name	Weight on FC's	Effect on Failure Counter (FC's) acts on failure counter...						Hw-Overwrite Ci-Flags on all channels to Ci-Status 10 and µC-Interrupt	CAN_DISABLE = MDGI_DISABLE	PSI_DISABLE	POR	16bit Cluster Flags													
		FC_YR_LF	FC_YR_HF	FC_ACC2_LF	FC_ACC2_HF	FC_ACC1_LF	FC_ACC1_HF					F16_MEMORY	F16_UC_WD	F16_MECH_OVERLOAD_ACC2	F16_F_CHECK	F16_MEMORY_DATA_AND_DSP	F16_SW	F16_DIGITAL	F16_MECH_OVERLOAD_RATE	F16_EMC_PSRR	F16_SUPPLY	F16_TEMP	F16_QBITE	F16_ST_FAILED	F16_MECH_OVERLOAD_ACC1
PinChecks																									
pc_vssa	01	x	x	x	x	x	x																		
pc_vssd	01	x	x	x	x	x	x																		
pc_psif_m	11	x	x	x	x	x	x					1													
pc_shd	01	x	x																						
pc_cs1	01			x	x	x	x																		
pc_cp	01	x	x																						
µC-Überwachung																									
uc_watchdog_err	00	x	x	x	x	x	x	x	x	1	1					1									
Bites																									
yrs_rate_seq_bit	00	x	x																						1
yrs_quad_seq_bit	00	x	x																						1
acc1_seq_bit	00					x	x																		1
acc2_seq_bit	00			x	x																				1
µC-Errors																									
uc_otp_prog_bist_initial								x																	1
uc_otp_data_bist_initial								x																	1
uc_otp_data_corrupt_header								x																	1
uc_otp_data_invalid_tuple								x																	1
uc_tuple_readback_mismatch								x																	1
uc_stack_check								x																	1
uc_hw_timeout								x																	1
uc_psi_async_timing		Reaction PSI-Specific in SW																							
uc_unrecoverable_error								x																	1
uc_rom_otp_sw_incompatible								x																	1
uc_can_psi_readback_mismatch								x																	1
uc_otp_data_open_bank	00	x	x	x	x	x	x	x																	1
uc_generic_error_flag_2	11																								1
uc_generic_error_flag_3	00	x	x	x	x	x	x	x																1	
uc_generic_error_flag_4	11																								1

uc_generic_error_flag_2	= uc_dsp_parity_err: Any parity error was detected when the uC sampled data from the DSP. The Parity will be handled application-specific (e.g. status-flag in PSI/CAN-message).
uc_generic_error_flag_3	= uc_registercheck_err: An error occurred during the CRC check of critical configuration registers (test carried out by the uC). Since this flag is handled within the tasks of the uc_watchdog_err, the frequency is the same.
uc_generic_error_flag_4	= uc_yrs_drive_restart: Indicator flag (no error) that is risen in case the yaw rate drive path can not be locked successfully in the first trial and needs to be restarted with a slightly different starting parameters.

7.4.5 Safety Control of Frequency

F07_10168 The main frequency of the sensor (incl. YRS, ACC, Digital Core incl. uC, DSP, PSI) is defined by the yaw rate PLL and hence from the CMG resonance frequency (see general description in {REF:F04_5742}).

As soon as the PLL unlocks (phase 3) because of an phase error (or, in PSI applications, because the DCO limit is reached, see next section), the flag yrs_pll_unlock is set (see description of flag in {REF:F07_9872}).

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The DCO frequency limitation in case of an PLL unlock is active only for PSI applications. This is due to PSI clock stability requirements of <1%. In all other applications (SPI, CAN) the DCO frequency limit is inactive and has no impact on flag yrs_pll_unlock (see change request 150).

7.4.6 Safety Control of Temperature

F07_9495 Temperatur surveillance limits for ctm_range are set as follows:

No flags are allowed in the range

-40 .. 135°C MM7.xyzC(CAN)5V

-40 .. 125°C MM7.xyzz(PSI)

Since

- the uncertainty in the temperature chamber (where no flag is allowed either) on device level is **5K**

- the sensor heats up himself by **10K** (MM7.xyzC 5V) resp. **15-17K** (MM7.xyzz(PSI)) compared to it's environment

- the temperature sensor has a uncertainty of +-5K (**10K**)

- the impact of ratiometry on the temperature measurement is ~**5K**,

the **upper flag limits** are set to 23.000 LSB (corresponding to 135...165°C).

The **lower flag limit** is set to -22.000 LSB (corresponding to -60...-40°C) (no self-heating considered since self-heating may only increase the temperature)

7.4.7 Safety Control of the Microcontroller

F07_10167 The functionality of the embedded µC is checked from the hardware SCON with a Challenge-Response-Scheme.

The HW SCON has a set of up to 36 challenge and response pairs.

During operation it issues an interrupt to the µC to fetch the next challenge from the HW SCON. The µC then has to compute and provide its response to the challenge.

In each uC cycle, one challenge will be handled (500us). If the µC delivers a wrong response or no response within a given time window (1ms @nominal CMG frequency), the error flag uc_watchdog_err will be raised. Due to the severity of the error the flag will not be deasserted during the current power on cycle.

After each correct response the next challenge will be used. Once the last challenge has been issued the watchdog will continue with the first challenge again.

Once the YRS frontend is settled (yrs_pll_unlock = 0 und yrs_agc_irregular = 0) the hw_scon starts to issue its challenges and expects responses.

In A-Sample, the response is trivial (no complex algorithms).

For B-Sample, refer to the following module test list:

The Module Tests describe a list of possible testing functions dedicated to test HW modules of the ARM Cortex-M0.

Implemented is the instruction set test, the register file test, ALU test, multiplier test and a test for the Shift & Permute unit.



7.4.7.1 Test for Instruction decoder (instruction set test)

F07_10206 The instruction decoder decodes the opcodes and generates the control signals for the various other hardware modules.

The instruction decoder test uses as much as possible of the defined instructions of the ARM Cortex-M0 instruction set. Thereby different addressing modes and alternative encodings are counted as separate instructions.

7.4.7.2 Register file test

F07_10208 The register file contains the 13 general purpose registers r0..r12, the stack pointer (SP=r13), the link register (LR=r14) and the program counter (PC=r15). The test focuses on the registers r0..r14 as they may be used as general purpose registers in a known context.

The Register file test is split into a basic stuck-at test and a register addressing test.

7.4.7.3 ALU test

F07_10210 The ALU has different data paths:

- the arithmetic calculations,
- the logic calculations,
- the address generation (using the same arithmetic logic as the arithmetic calculations),
- the carry and overflow Flags generated also from result of the arithmetic calculations,
- the AHB addresses generated from either the result of the address generation, the register read line A or the address of the prefetch unit,
- some AHB control and consistency check signals derived from the AHB addresses.

The test of the **arithmetic** logic consists of multiple operations using the different operators with multiple values each.

The core arithmetic can be checked by using the basic ADD and SUB (or ADC and SBC) instructions with multiple registered parameters.

The **logic calculations** are performed by the instructions AND (register) and EOR (register). The implementation of ORR instruction is unknown. As the logic is relatively simple, testing via basic stuck-at pattern as in the basic register stuck-at test is considered to be sufficient.

7.4.7.4 Multiplier test

F07_10212 The multiplier is tested by performing multiplications with a predefined set of instructions and expected responses.

7.4.7.5 Test for Shift & Permute unit

F07_10214 The shift & permute unit is responsible for two kinds of operations:

- shifting of parameters
 - permuting the bytes and halfwords of parameters when using byte or halfword instructions
- For the shifting test, both right and left shifting are being used with both immediate shifting amount and register stored shifting amount.

The code for the permute test uses the different byte/signed byte/halfword/signed halfword instructions with different parameters that are suitable for detecting faults both in the permutation itself (routing the data from/to the wrong byte/halfword) and in the data path (modifications of one or more bits in the data to transfer due to a fault).



7.4.8 Safety control of memory elements

- F07_1132 In addition to the DSP monitoring (see flags "dsp_...") and the Bus monitoring (see flags "apb_..."), the whole digital signal path is covered by a parity:
- there is a Parity Prediction for all decimation filters within the fast digital circuit.
- within DSP all data is covered with parity.
- during transport via the internal Bus, the sensor signals are also covered with a parity.

7.4.8.1 Safety control of µC-RAM

- F07_7037 µC RAM is tested by means of dedicated HW test units.
During start-up, SOAF and IFA13 tests of the RAM are performed.
During operation,
 - Continuous SOAF and IFA13 tests are performed which are invisible to SW execution on the µC.
 - RAM content is checked by means of parity bits for accesses by the µC

7.4.8.2 Safety control of µC-ROM

- F07_7038 Additional hardware for every ROM is implemented to test ROM content continuously.
A CRC check is performed over the whole ROM space.

7.4.8.3 Safety control of µC-OTP

- F07_7039 Additional hardware for every OTP is implemented to test OTP content continuously.
A CRC check is done for all programmed and CRC-secured OTP words.

7.4.8.4 Safety control of DSP-ROM

- F07_7040 The ROM for the DSP is continuously tested during the active phase of the DSP.
The following figure shows a scheme of the ROM-check module for DSP-ROM.

F07_1148

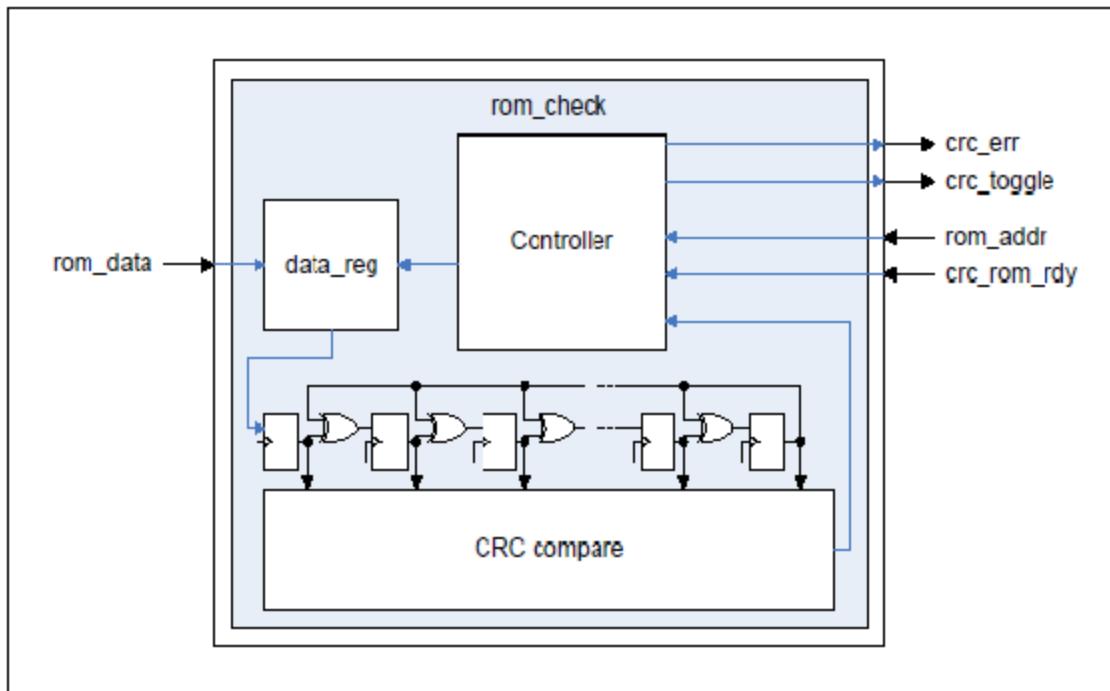


Figure 59: ROM-check module for DSP-ROM

F07_1149

The ROM-check module includes two functional blocks, a LFSR with XOR feedback to implement the CRC algorithm and a controller block to manage the execution and generate all status flags. Besides the shift register a data register is implemented to store the value of the ROM cell currently processed.

7.4.8.5 Safety control of DSP-RAM

F07_7041

The RAM for the DSP is continuously tested during the active phase of the DSP.

Figure 60 shows a Picture of DSP-RAM check architecture.

F07_1153

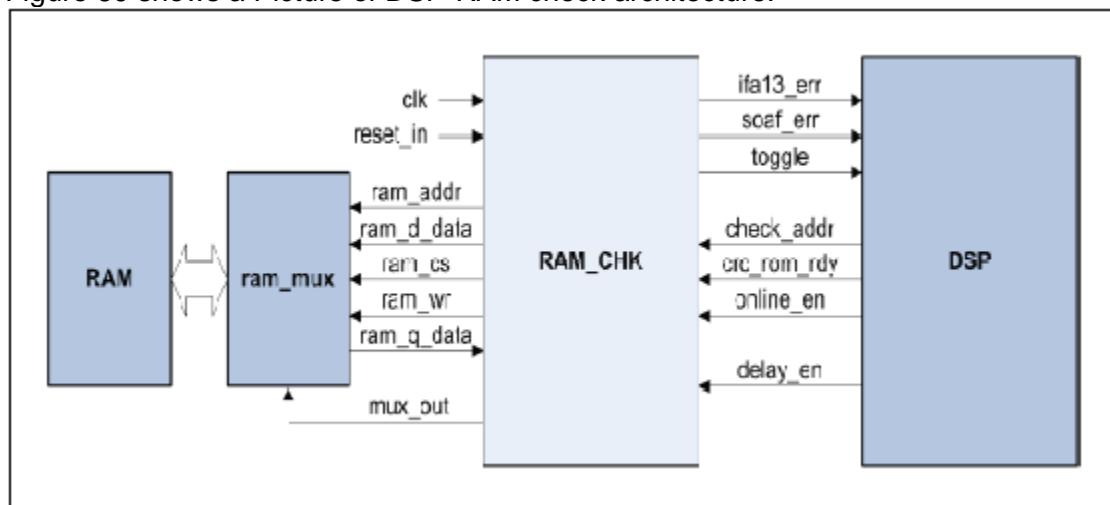


Figure 60: DSP-RAM check architecture

F07_7042

The following test is performed for RAM testing:

IFA9/13 (Inductive Fault Analysis) and SOAF (Stuck-at-Open Address Decoder Fault).



During start-up the IFA9/13 algorithm is performed like common MARCH test on the whole memory. In online mode, the IFA9/13 algorithm behaves like a test of a 2-cell memory. Instead of observing the whole memory and therefore writing and reading all cells, the test is performed with two cells, the base cell and the neighbour cell. The state of the memory is not altered by the test.

Every DSP RAM cell content is protected by a continuously running parity check. In addition, the calibration data which is transferred at startup from OTP into the DSP RAM, will be secured by additional CRC algorithm.

7.4.9 Safety control of CAN and PSI and SPI interface

F07_7034

To prevent any error state to propagate to the CAN and PSI interface, a CAN and PSI disable mechanism is implemented. Since these interfaces are actively controlled by the sensor itself, any error condition that potential has an influence on the correct behavior of those interfaces and which might prevent to signal this error by the interface itself results in a deactivation of the output pins of the interface. Therefore the TX pin for CAN and the PSI transmit signal is disabled right at the boundary of the sensor.

In this case the WDGI signal is the only means to signal an error condition to the outside.

Whenever a communication error is detected at the interface for an incoming message (e.g. a corrupt CRC), the interface will react immediately with an intentionally destroyed CRC (SPI) or invalidation of the message on controller level (CAN). This does not affect the channel status.

(PSI does not receive messages in normal operation, therefore "communication errors" may only be detected on ECU side. PSI BiDir, which is only being used during production, does not react until a CRC of the incoming message is valid.)

During operation, the uC always read back the data to be sent from PSI and CAN message buffer and compared to the intended content; any mismatch is indicated by the flag "uc_can_psi_readback_mismatch".

For SPI interface, see SPI Chapter "Error handling".

7.4.10 Electromechanical yaw rate and acceleration self tests

F07_7046

SMI7 provides the possibility to carry out electromechanical self tests with which the sensor elements can be stimulated electrically, resulting in mechanical excitations of the sensor, similar to external mechanical stimulations. Thus, the whole signal chain can be tested.

The sensor provides software routines for a BITE sequence (see 1.4.10.1.1) as well as for static BITE excitations (see 1.4.10.2).

7.4.10.1 BITE sequence

F07_7047

The BS and YR Bits are triggered in parallel according to the scheme below. The BS Bits timing raster and the DRS timing raster will be identical and will be "absolute timed" (see SW-PH DS_405) having a duration of 20ms per sequence.

If the tests are not passed, they will be repeated automatically up to a programmable number N times. If the test is still not passed even after having repeated the sequence N times, corresponding failure flags will be activated.

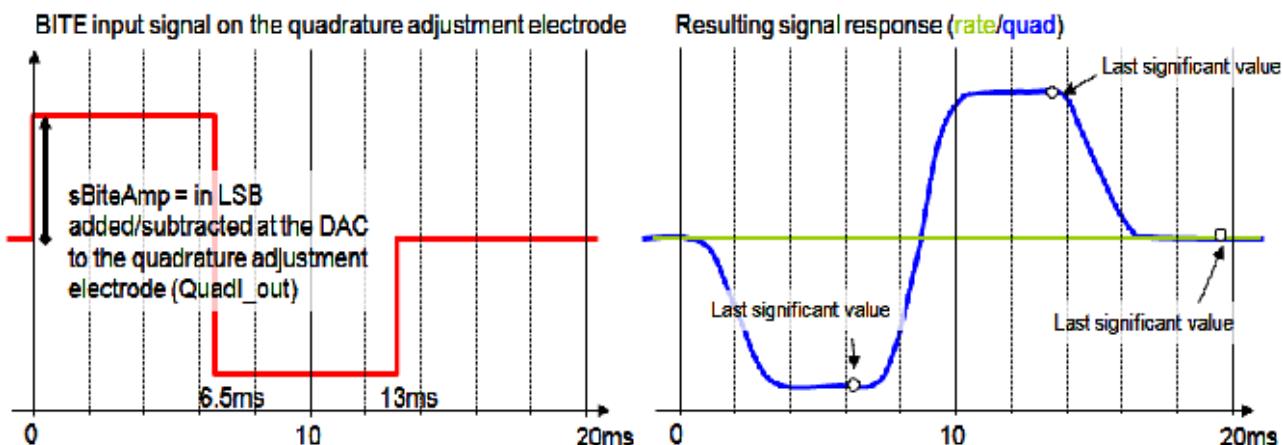


The BITE sequence applied to the channels plotted on the left-hand side, the resulting signal on the right-hand side:

F07_1211

S

Yaw Rate:



Acceleration:

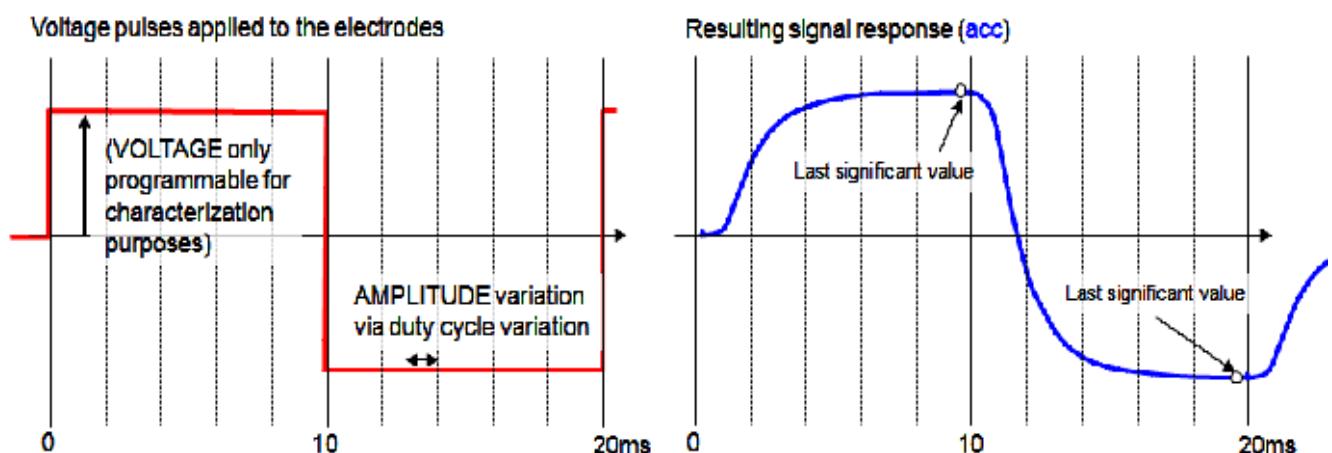


Figure 61: Timing of the Bite sequence

7.4.10.1.1 Description Yaw-Rate/Quad BITE sequence:

F07_7048

S

The YR/Quad BITE sequence consists of 3 possible pulses (ZERO, POS, NEG). The pulses are introduced in the quadrature control circuit and measured at the quadrature HF output (after cQ-Bite-Filter) and rate domain at the HF (400Hz) output of the DSP, respectively. The minimum step size will be 150°/s for each positive and negative pulse.

In the actual design the BITE sequence will be positive, negative and zero pulse.

The quadrature controller is stopped during sBITE and the output value is hold during the software trigger.

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SW assures that the yrs_quad_HF_tol evaluation is masked for ca. 40ms after BITE is switched off. This also means that the BITE condition b11 in the yaw rate CI flags will not be removed earlier than 40ms after the end of the YR Bite.

The yawrate sBITE lasts for 20ms. It contains a positive, a negative and a zero offset phase. The duration and order of these phases are as follows:

POS (6.5ms)

NEG (6.5ms)

ZERO (7ms)

The SCON-SW samples the BITE value at following time:

YRS_POS(6.5ms), YRS_NEG(13ms), YRS_ZERO(19.5ms)

7.4.10.1.2 Description of the Acceleration BITE sequence

F07_7049 The acceleration bite sequence consists of a positive (ACC1/2_HF_POS) and a negative (ACC1/2_HF_NEG) excitation. Test is passed if $|ACC1/2_HF_POS - ACC1/2_HF_NEG|$ is within temperature dependent limits. It has been shown by analysis of all available field failures that the separate evaluation of POS and NEG (relative to zero) did not reveal more failures than the evaluation of $|POS-NEG|$.

Temperature dependent trimming is done during the production tests. During production test trim settings are done to obtain at least 3g BITE amplitude.

The AMPLITUDE of the self-test is programmable by trimming the duty cycle of the excitation voltage.

The acceleration BITE sequence lasts for 20ms. It consists of a positive and a negative excitation. The duration and order of the phases are as follows:

POS (10ms)

NEG (10ms)

The SCON-SW samples the BITE value at following time:

ACC_POS(9.5ms), ACC_NEG(19.5ms)

When the self-test is switched on the sample frequency of the front end is reduced to half, i.e. the sample-time is 2^*Ts . Each Self-Test period consists of an actuation or excitation phase and a sense or measurement phase. These phases are of equal duration i.e. Ts , shown in the following figure:

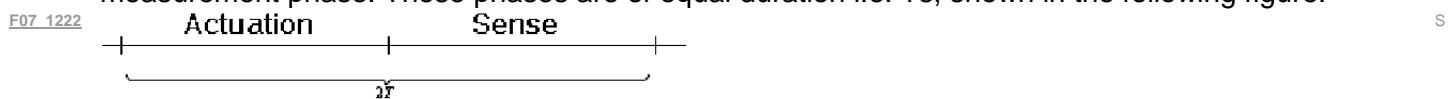


Figure 62: Acceleration Bite

7.4.10.1.3 Evaluation of signals

F07_7050 Signals are taken from HF (400Hz) output channels of DSP:

QUAD_HF after cQ-Bite Filter

RATE_HF

ACC1_HF

ACC2_HF

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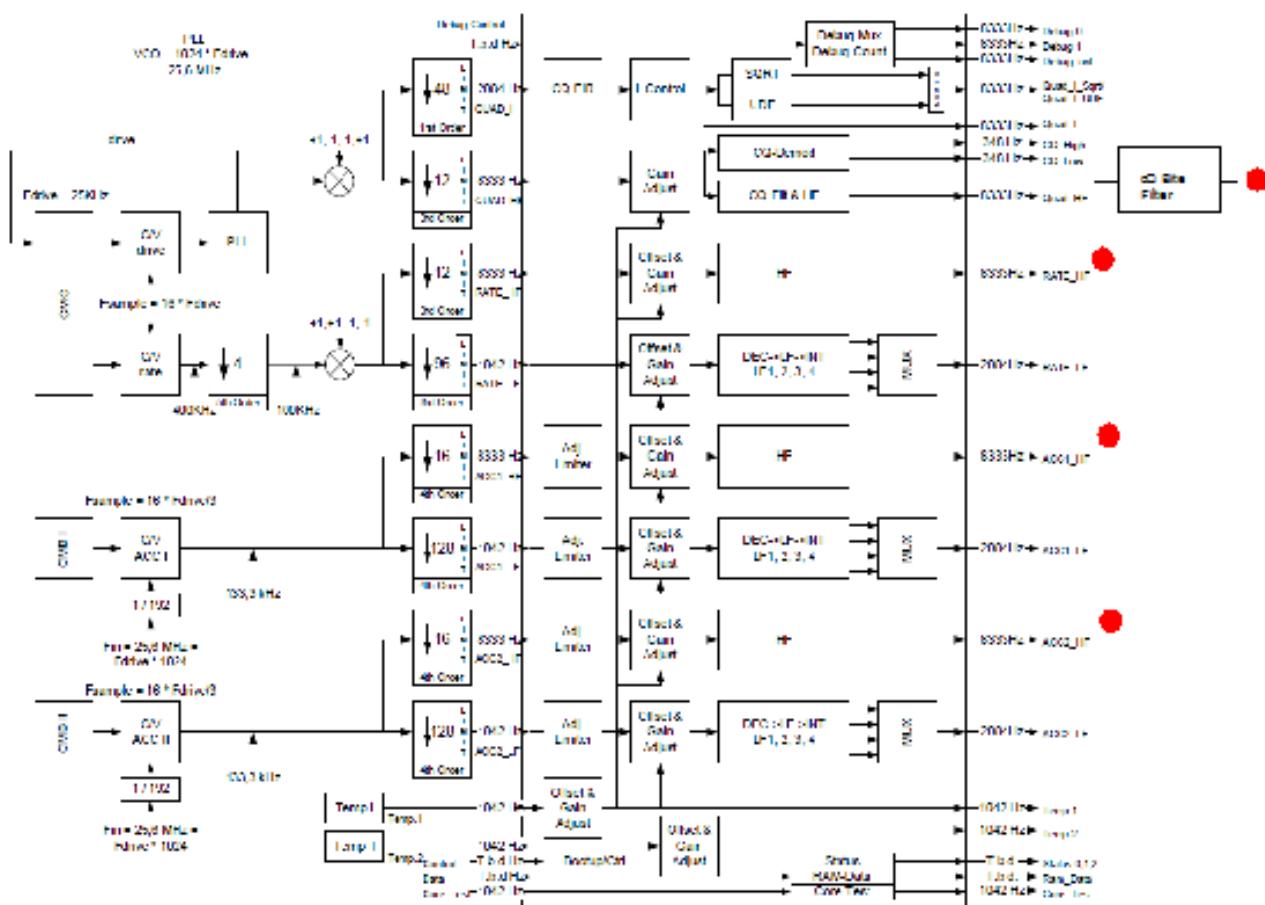


Figure 63: Evaluation points for Bite

F07_7051

Evaluation is done in the following way:

S

For the yaw rate / quad signal and the acceleration signals, the last values prior to switching the excitation is to be used for evaluation (corresponding to index “(t)” (see graph in {REF:F07_1211}).

The evaluation of the resulting flags

yrs_rate_seq_bite
yrs_quad_seq_bite
acc1_seq_bite and
acc2_seq_bite

is described in the flag list (see 1.4.3.1)

F07_7078

BITE Sequence evaluation cycle

S

At the beginning of the BITE sequence, the Channel Information (CI) bits of the corresponding channels will be set to b11 (might be already set from startup routine).

The programmed settings for the YR/Quad bite amplitude (sBiteAmp) as well as the Acceleration bite amplitude (duty cycle) will automatically be used by the Hardware.

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If the sequence is finished without positive result, the corresponding failure flags (yrs_rate_seq_bite, yrs_quad_seq_bite, acc1_seq_bite, acc2_seq_bite) will be activated, acting on the channel-specific failure counters (default: permanently and immediately).

After having switched off the BITE excitations, the SW waits for the filters to be flushed (see programmable parameter "BiteFilterFlushTime HF"/"BiteFilterFlushTime LF" {REF:F02_10336}), and assures that the yrs_quad_HF_tol evaluation won't start earlier than ca. 40ms after BITE is switched off (since the quad regulator needs this time to be fully functional again). This means that the earliest time to remove the b11 condition from the YR channels is the maximum of 40ms and the channel-specific FilterFlushTime (LF/HF). For the acceleration channels, the time to remove the b11 condition will be only the channel-specific BiteFilterFlushTime (LF/HF). The end of the service routine is the maximum waiting time.

If bite (or other) flags acted on the failure counters during the flush times, the CI flags will be set within the time specified assumed that the b11 condition is not set any more (b11 overwrites the failure counter results).

As long as the "Init or BITE condition" b11 is set, the result of the failure counters is overwritten by b11. Nevertheless, the failure counters work during the BITE period (incl. Filter Flush Times). As soon as the b11 status is removed, the status of the failure counters defines the general status.

For manual triggering of the BITE sequence, it can be chosen whether

YR and (ACC1+ACC2) YR_BITE = 1, ACC_BITE = 1
YR only YR_BITE = 1, ACC_BITE = 0
(ACC1+ACC2) only YR_BITE = 0, ACC_BITE = 1
excitation (and evaluation) shall be carried out:

Bite sequence:

```
if YR_BITE = 1 then
yrs_quad_int = 1
yrs_rate_int = 1
CI_YR_LF = b11 *
CI_YR_HF = b11 *

if ACC_BITE = 1 then
acc1_int = 1
acc2_int = 1
CI_ACC1_LF = b11 *
CI_ACC1_HF = b11 *
CI_ACC2_LF = b11 *
CI_ACC2_HF = b11 **might be set already from global startup
```

```
n=1
all_bites_nio = 1
```

```
while ((n<=Numb_of_repetitions+1) OR (all_bites_nio)) do
    if YR_BITE = 1 then Apply YR Bite
    if ACC_BITE = 1 then Apply ACC Bite
```



```
if (YR_BITE = 1) and (Bite_Limit_Check_Quad iO) then yrs_quad_int = 0
if (YR_BITE = 1) and (Bite_Limit_Check_Rate iO) then yrs_rate_int = 0
if (ACC_BITE = 1) and (Bite_Limit_Check_Acc1 iO) then acc1_int = 0
if (ACC_BITE = 1) and and (Bite_Limit_Check_Acc2 iO) acc2_int = 0
all_bites_nio = (YR_BITE AND (yrs_quad_int OR yrs_rate_int)) OR ((ACC_BITE AND (acc1_int
OR acc2_int))
n++
end while

if YR_BITE = 1 then
yrs_rate_seq_bite = yrs_rate_int
yrs_quad_seq_bite = yrs_quad_int

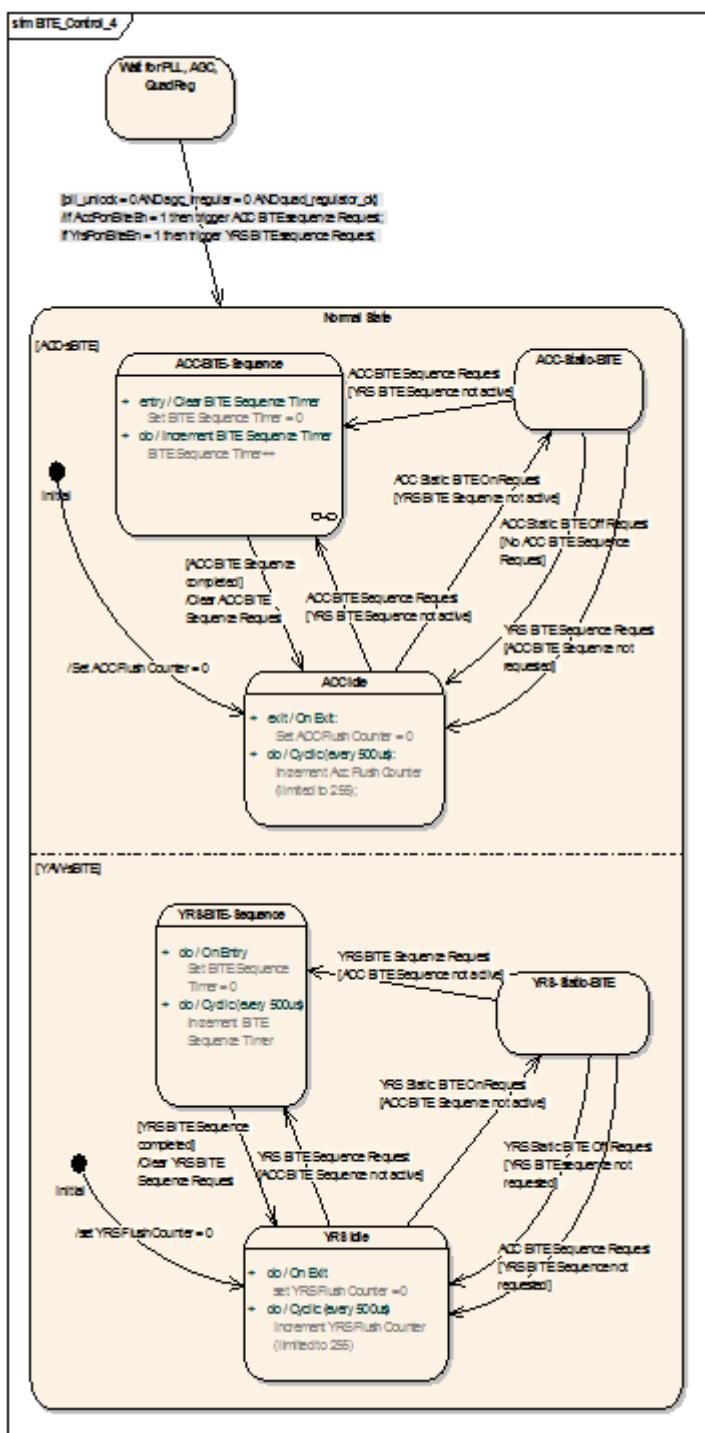
if ACC_BITE = 1 then
acc1_seq_bite = acc1_int
acc2_seq_bite = acc2_int
```

Filter Flush:

Wait LF_FLUSH_BITE_WAIT_TIME* , then remove b11 in LF channels
(but check failure counters instead)

Wait HF_FLUSH_BITE_WAIT_TIME* , then remove b11 in HF channels
(but check failure counters instead)

*see text concerning the waiting time necessary for the Quad-I-regulator to work properly after a BITE



7.4.10.1.4 Programmeable Parameters

F07_10177

Programmable parameters are

- the number of repetitions until BITE sequences are discontinued (0: single run, ..., 9: up to 10 runs as specified). See parameter "BiteConfig" in {REF:F02_10336}
- the BITE tolerances, see paramters in {REF:F02_10336}:
 - yrs_rate_seq_bite Tolerance pos-neg,



yrs_quad_seq_bite Tolerances pos-zero, neg-zero, pos-neg
 acc1_seq_bite Tolerance pos-neg
 acc2_seq_bite Tolerance pos-neg

- the BITE flush times "BiteFilterFlushTime HF", "BiteFilterFlushTime LF" in {REF:F02_10336}.

7.4.10.1.5 Read-out possibilities of the Bite sequence values

[F07_1287](#) The values that lead to the final flag status (valid or invalid) are stored in a register and are readable via all interfaces (incl. CC32in w/o password).

LastBite_Acc1_Pos
LastBite_Acc1_Neg
LastBite_Acc2_Pos
LastBite_Acc2_Neg
LastBite_QUAD_YR_Pos
LastBite_QUAD_YR_Neg
LastBite_QUAD_YR_Zero
LastBite_RATE_YR_Pos
LastBite_RATE_YR_Neg
LastBite_RATE_YR_Zero

7.4.10.1.6 Automatic triggering of the BITE sequence at startup

[F07_7184](#) If the flag PON_BITE_ACC and/or PON_BITE_YRS bits in the Reset Vector are set, the BITE sequence of the yaw rate and/or the two acceleration channels are carried out automatically after AGC Lock and QUAD_HF already regulated to zero (yrs_quad_HF_tol).

If no PON_BITE_xxx bit in the Reset Vector is set, the SW will anyhow wait for the filters to be flushed (see programmable parameter "BiteFilterFlushTime LF/HF") before removing the b11 condition of the CI flags, individually for each channel depending on HF or LF.

In order to guarantee the integrity of the safety concept, the customer needs to trigger the bite sequence for YR and ACC1+ACC2 at least once per power-on cycle, either by setting the PON_BITE-Flags in the Reset Vector or by triggering the BITE sequence manually (see following chapter 1.4.10.1.7)

7.4.10.1.7 Manual trigger of the BITE sequence

[F07_7185](#) The same sequence including the repetitions and evaluation and setting of the corresponding flags can also be triggered later on by a µC command (see µC Command Manual BITE Trigger, {REF:F02_9510}). The procedure is exactly the same as described in 1.4.10.1 including the evaluation, flag handling and flushing.

For the manually triggered Bite sequences, it can be chosen whether

- YR + ACC1 + ACC2
- YR only
- (ACC1 + ACC2) only

should be carried out and evaluated (including the corresponding flag handling and consequences for the quad regulator).



No other command can be triggered during the execution of the sequence.

7.4.10.2 Static BITEs

F07_7186 Static bites in any combinations (YR/QUAD + ACC) can be triggered via **µC service request** any time during normal operation. The main use will be for characterization purposes; nevertheless, CI will be set to b11 in the corresponding channels. S

No evaluation of the bite amplitudes takes place, nor will the amplitudes be stored in the registers described in 1.4.10.1.1.

4 bits are being used for triggering the excitations.

xx00	Acceleration bite off
xx01	Acceleration bite off
xx10	Acceleration1+2 negative bite
xx11	Acceleration1+2 positive bite
00xx	YR/Quad bite off
01xx	YR/Quad zero bite
10xx	YR/Quad pos bite
11xx	YR/Quad neg bite

The quad controller will be switched off as soon as the static yr/quad bite is activated (by HW), similar to the bite sequence. SW assures that the yrs_quad_HF_tol evaluations are not carried out during the bite.

The excitations will remain triggered as long as no switch off command is sent as a **separate service request**. Similar to the BITE sequence, after having switched off the BITE excitations, the SW waits for the filters to be flushed, and assures that the yrs_quad_HF_tol won't start earlier than ca. 40ms after BITE is switched off (since the quad regulator needs this time to be fully functional again). This means that the earliest time to remove the b11 condition from the YR channels is the maximum of 40ms and the channel-specific FilterFlushTime (LF/HF). For the acceleration channels, the time to remove the b11 condition will be only the channel-specific FilterFlushTime (LF/HF). The end of the service routine is the maximum waiting time.

The minimum HF flush time after BITEs is not only determined by the filter flush time but also by the time needed by the acceleration sensors to get back to zero position.

7.4.10.3 Timing overview of BITE sequence and static BITE

F07_1316

S

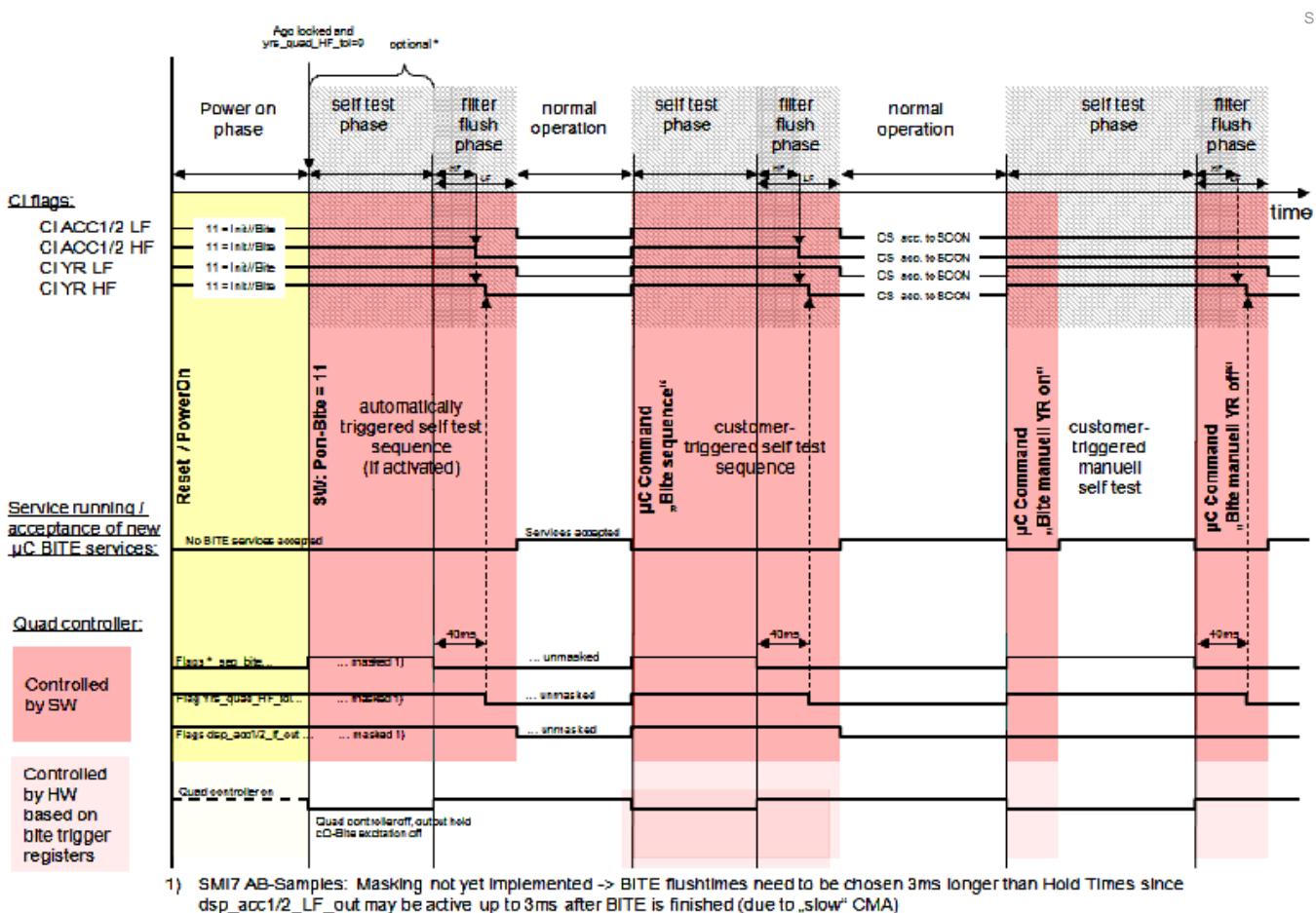


Figure 64: Timing of Bites and flags. *The BITE sequence at startup is optional and can be deactivated (see Reset Vector).

7.4.10.4 Continuous BITE of Acceleration and Yaw Rate

F07_1328

S

No implementation of an continuous electromechanical self test is foreseen due to unacceptable influence on sensor performance.

7.4.11 ACC disturbance detection

F07_10142

The acc disturbance detection is not a sensor failure flag. The disturbance detection is designed to detect high speed vibration events in the high bandwidth sigma delta modulator bit streams.

A weighted counter is used to sum up consecutive bittrains of same polarity. The weight can be calibrated in 8 steps with 3 bits with the following formula:

F07_10143

Weight (inc_value) = $1/(2^{\text{inc_value}})$ with inc_value = 0 ... 7

F07_10144 The start_value is a 16 bit value, which determines the start of the incremental adder.

F07_10145

The incremental is done with the formula:

$$y(0) = \text{start_value}$$

$$y(N+1) = Y(N) * (1 + \text{Weight}(inc_value))$$

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N is increased as long as the bit stream delivers a constant row of zeros or ones. If the sd bitstream switches from 0 to 1 (or 1 to 0) the counter value is transferred to the second counter and the first counter is reset and starts over again.

F07_10146 A second counter sums up the upper 8 bit values of the first counter and compares it with a programmable limit.

(Name: acc1_overload_limit, acc2_overload_limit)

F07_10147 Range of start value: 1...65535

F07_10148 Range of increment value: 1...1/128

F07_10149 Range of error limit: 0...4095

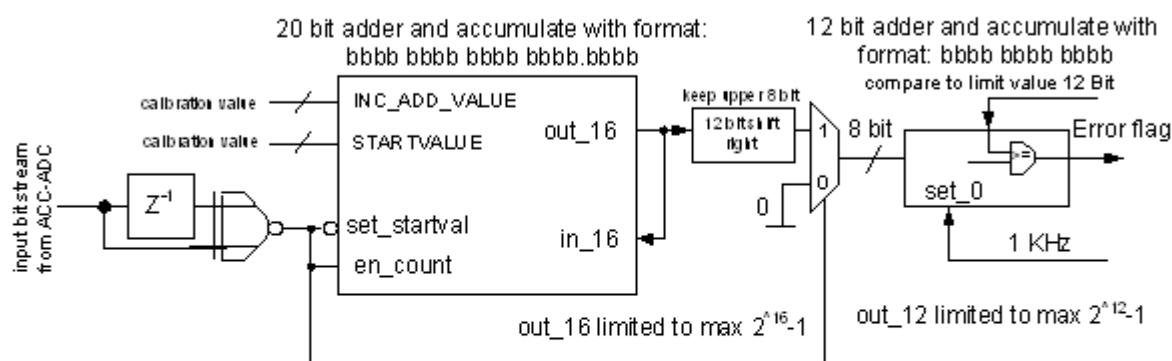
F07_10150 Time of Terrorsample: 1ms

F07_10151 The error flags have the names:

acc1_overload_det

acc2_overload_det

F07_10152 Picture of disturbance detection:

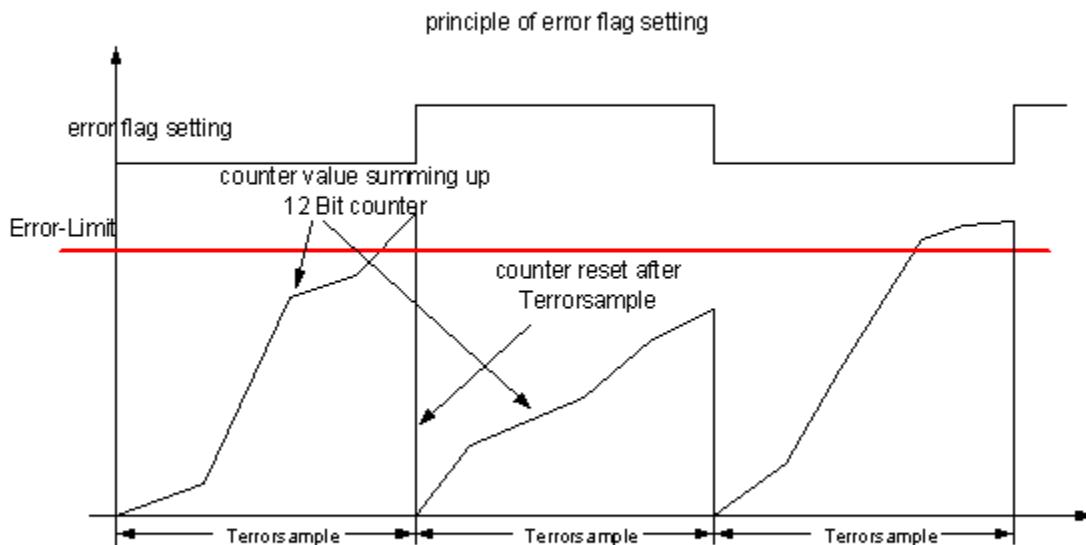


$$Y^0 = \text{STARTVALUE}$$

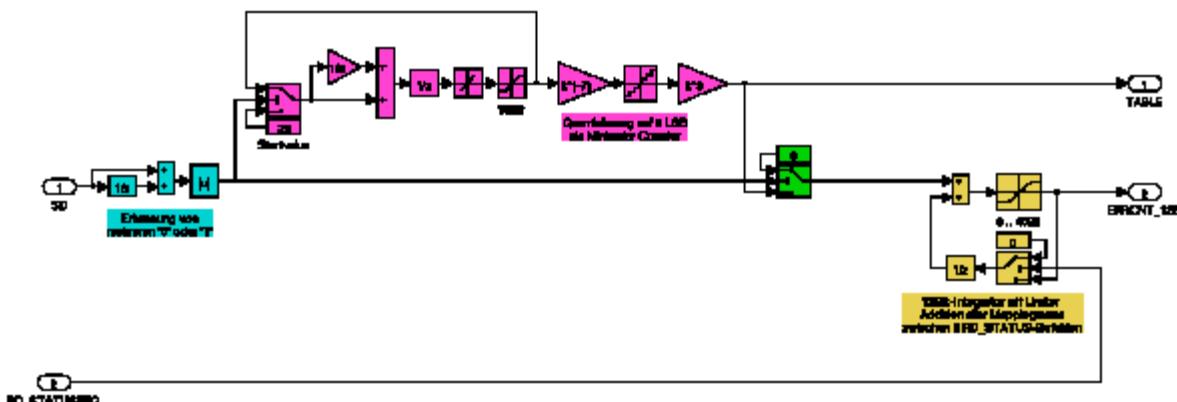
$$Y^{H1} = Y^1 * (1 + \text{INC_ADD_VALUE})$$

$$Y^{H1} = \text{LIMIT}(Y^{H1}) \leq 65535$$

F07_10153 Error flag behavior:



F07_10154



7.4.12 Expected external monitoring

F07_10170 Communication errors like wrong CRC/parity are assumed to be detected by the communication partners by 100%.

The wrong CRC/parity may be set by the sensor intentionally to indicate malfunctioning, but may also be a result of timing or amplitude problems of the communication signal (see 1.4.9).

A wrong CRC/parity may therefore indicate a malfunctioning of the sensor communication interfaces in a double way.



The error indicators of the SPI protocols (see {REF:F03_10601} for CC32in-SPI and {REF:F03_609} for OpenSPI) need to be evaluated by the communication partners since they may indicate a problem of the communication transfer (like missing clock pulses) or a fault of the sensor SPI interface.

An error in the CAN frequency is assumed to be detected 100% by the protocol partner (CRC failure, missing acknowledgement).

In case an expected frame is missing in a PSI message, all data of this message shall not be interpreted as valid (e.g. to prevent an acceleration frame (wrongly sent at a wrong position instead of a yaw rate frame) to be interpreted as a yaw rate).

For reasons of traceability, the serial numbers of the sensor (ASIC S/N, Module S/N and optionally Customer S/N, see {REF:F02_112}) shall be read out by the unit that communicates with the sensor and shall be made available to Development or Manufacturing site in case of questions or errors.

In SPI applications that use the voltage at RX for Autodetection of SPI ID, a shortcut to TX may lead to a wrong SPI ID. This needs to be detected by the system level (Sensor will not answer when being asked with the wrong ID).

When the functionality (2nd. Sensor) -> SPIM -> uC -> PSI -> (ECU) is being used, the correctness of the data of the 2nd Sensor must be checked as follows:

- either the complete content of the 2nd-Sensor-SPI-Message is being passed through to PSI by the SMI7 (incl. CRC), and the validity must be checked on ECU level
- or (in case the data is being transformed): the uC must
 - check the data consistency (CRC) of the incoming 2nd-Sensor-SPI-message,
 - perform the transformation and send the new data to the PSI block
 - read back the data from the PSI block
 - compare the read back data with the original incoming data via an inverse transformation

From the PSI interface to the ECU, the data is then being secured by a Manchester Code and CRC.

MERKER: CR131: Aufnahme kundenseitiger Check systematischer Abweichungen zb bzgl Einsatz Einzelkanäle in ASIL D Applikationen, insbes. homogener REdundanz

7.5 Forecast values for safety goals

F07_7043 Residual failure rates and metric values are estimated on the basis of a preliminary FTA/FMEDA. This was requested by the customer and is not required at module level by ISO26262.

The following failures (in sum: ~150) have been considered up to now regarding their occurrence probability, their monitoring (direct and indirect) and their impact on the individual top events in 11 different application configurations:

CMB failures (leakage, particles, mechanical breaks)

CMG failures (leakage, particles, mechanical breaks)

Chip-to-chip bond failures (bond rupture and shortage to neighbor bonds)

Acceleration frontends (failures of all blocks in both acceleration channels)

Yaw rate frontend (failures of all blocks in drive and detection path)

Digital part of ASIC (DSP, µC, bus system, interfaces, memory)

External bond failures (bond ruptures and shortages to neighbor bonds)

Voltage regulators

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Charge pump, temperature sensors, oscillator
SPI Master Functionality and interfaces
POR
SCON-ADC
external circuitry.

Safety Analysis Results can be found here: [21]

7.6 Safety validation

F07_1195 All failure modes that are accessible via experiment will be checked via experiment, together with their corresponding monitors (e.g., bond ruptures / short cuts, spring breaks in CMB/CMG, temperature or supply voltage out of range, ...). However, the largest part of the failure modes will not or inadequately be accessible by experiment (e.g., CMB particles, failures in the ASIC). Therefore, design considerations, failure injection methods and simulations will be used, together with adequate reviewing, for the validation of the safety concept. A complete validation plan will be worked out with and provided to CC/PJ-SMI7.

7.7 Flexibility and validity of the safety concept

F07_7045 It is technically possible to change almost all surveillance limits or debouncing settings on customer-level for application-specific needs. However, changing any settings in the surveillance limits and/or debouncing characteristics or deactivation of monitors or masking of flags may not be done without evaluating the effects on the safety concept.

Based on theoretical considerations, reducing the error counting limits, increasing the weights and/or tightening monitoring tolerances will not lead to a reduced safety concept (assuming that the safety targets and the fault tolerant time interval remains unchanged). No special characterization of these configurations will be done. The availability may drop; enough availability must be ensured by the system. Affected quality targets are to be accepted by the application.

Relaxing error counting limits or weights as well as opening monitoring tolerances or masking error detections may lead to a changed safety evaluation. If any changes of this kind are needed by the system, a change request to the project is to be filed with the aim to check the safety concept and the metrics calculation with the new settings and application-specific inertial, temperature and supply data, if relevant.

All parameters (including surveillance limits etc) that might be subject to changes on device / system level are listed in a white list (see {REF:F02_10336}). This list is stored in the sensor (ROM) and might be expanded by programming at final testing. This list must be agreed upon with the customer until final freeze of the PAV in order to prevent new part numbers.

In general, the sensor will be delivered in one configuration (60Hz-Filter, 5V VB-supply (->activated VB_low-voltage-monitoring, see {REF:F02_103}), SPI slave) including surveillance limits, debouncing settings etc for the default filter settings, and a set of recommended hold limits (for the failure counters) and filter flush times (after Bites) that will be described in the data sheet for each of the filter settings.

When changing the filter settings for the LF paths, the debouncing settings will have to be adapted, too. It is in the customers responsibility to change the debouncing settings and filter flush times after Bites together with the filter settings, otherwise, the safety concept cannot be guaranteed.



When changing to VDD3 supply, the VB_low-voltage monitoring must be deactivated.

According to the current concept, bite sequences as well as all slow value monitoring will be executed by the µC. Changes in the bite sequences and/or evaluation or the change of the way values are monitored will only be possible via a ROM mask.

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8. Terms and definitions

Term	Description
APB-BUS	internal bus connecting SPI, DSP, frontends and µC-bridge
BA	Bank Area or Bus Address
BGA	Ball Grid Array
BIST	Build In Self Test
BITE	Build In Test
DAC	Digital Analog Converter
DCO	Digital Controlled Oscillator
DSP	Digital Signal Processor
IFA	
LSFR	
OTP	One Time Programmable Memory
PON	Power ON
PW	Password
QA	Quality Assessment or "Quadratur Abgleich"
RAM	Random Access Memory
ROM	Read Only Memory
RV	Reset-Vector
RV-SW	Reset-Vector-Software
SOAF	
KT 1/2	Kipptische 1 oder 2
DT	Drehtisch
CI	Channel Information
SoC	System on Chip

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9. Measurement and Validation

9.1 Prolog

[F08a_9414](#) Based on the document [100503_SMI7xy_Sensor_parameter_description_v1_0.pdf](#) this document describes a subset of key parameters and hints for validation.

CC & AE follow the aim to develop best in class products possible in terms of quality, costs and schedule. Nevertheless quality targets within ppm-range are not achievable easily and all demands have to be combined with a confidence level. Within the development phase there is always a tradeoff between the number of samples to be tested and the confidence level necessary.

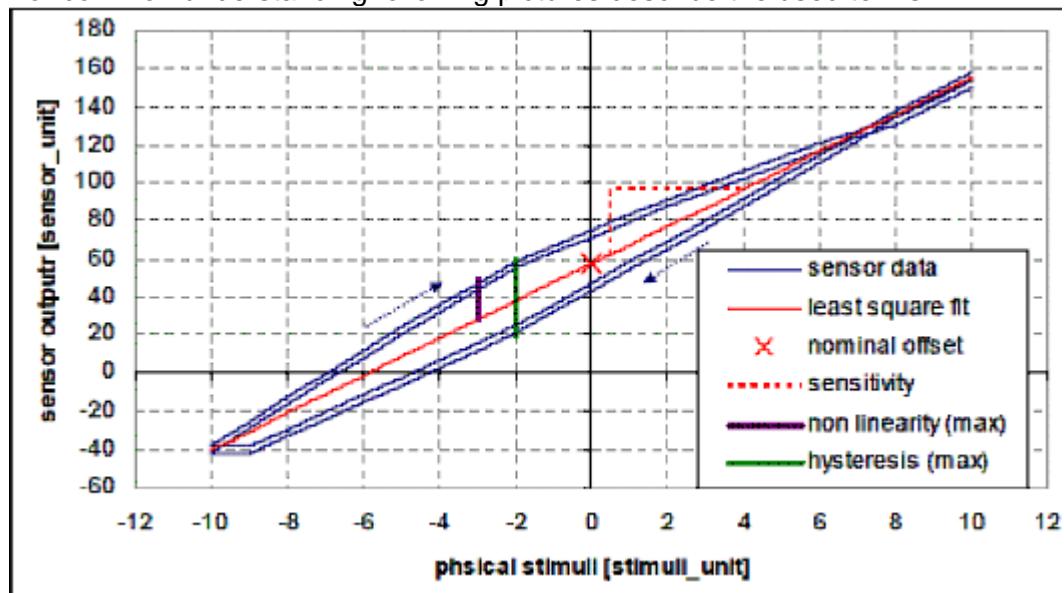
Further information can be found in [ISO_16750-1_Road vehicles - Environmental conditions and testing for electrical and electronic equipment.pdf](#) and [VDA Qualitätsmanagement in der Automobilindustrie - Zuverlässigkeitssicherung bei Automobilherstellern und Lieferanten.pdf](#)

Due to the experience of products already developed; definition and validation for a couple of parameters (e.g. vibration, noise, offset ...) has to be taken into focus. Measurements for these parameters are described in this document and have to be agreed with the customer as acceptance test. This document does not describe measurements that will be applied in production.

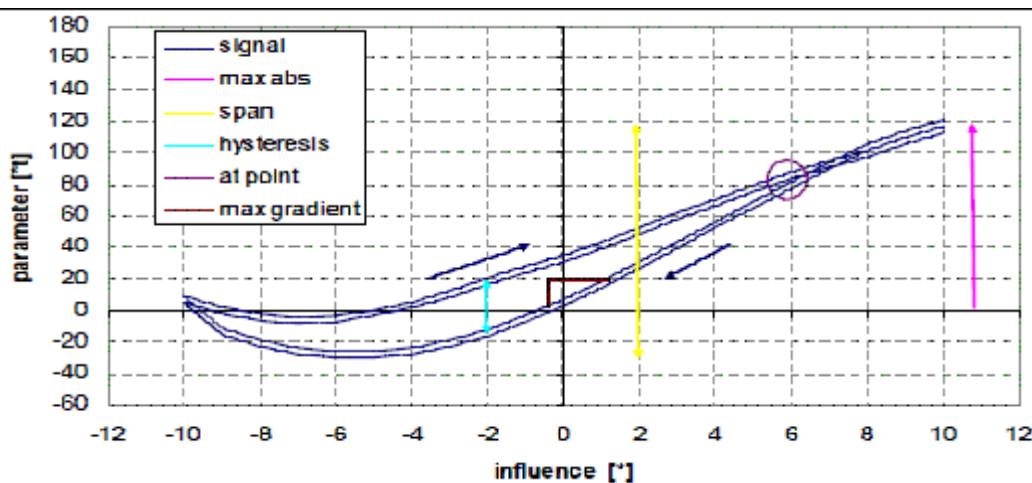
9.2 Parameters and measurements

9.2.1 Overview

[F08a_9429](#) For common understanding following pictures describe the used terms.



- Sensitivity slope of the LSF.
- Nonlinearity deviation of the sensitivity line.
- Hysteresis (sensitivity) max. delta between two sensitivity measurements with monotone rising and falling stimulus at one specific stimulus.



- Span max - min within the specified temperature range.
- Hysteresis (Offset) max. delta between two sensitivity measurements with monotone rising and falling stimulus at one specific stimulus.
- Max. gradient max. slope within measurement.

9.2.2 Bit Width and Output Range

F08a_9436

Given by design;

Validation could be done within verification of the output signals measured on centrifuge.

9.2.3 Sensitivity

F08a_9438

Function guaranteed by design;

Guaranteed by calibration for every part and measured.

Necessary measurement stimulus to achieve necessary accuracy and product quality will be derived within product development.

9.2.3.1 Acceleration

F08a_9441

Calibration is done at least at room temperature with a stimulus of $\pm 1G$. For improved accuracy additional equidistant points can be introduced between minimal and maximal stimulus. A LSF will be used calculate sensitivity.

9.2.3.2 Yaw Rate

F08a_9444

Calibration is done at least at room temperature with a stimulus that will be derived with samples. For improved accuracy additional equidistant points can be introduced between minimal and maximal stimulus. A LSF will be used calculate sensitivity.



9.2.4 Sensitivity Error

F08a_9446 The sensitivity error gives the difference between the nominal sensitivity and real sensitivity of every part over full scale measurement range.
Validation will be done for every part.

9.2.5 Resolution

F08a_9449 Given by design;
The resolution gives the smallest measureable change in the output value. Apply any stimuli⁵. Measure the Offset. Vary the applied stimuli. Measure the offset again. The smallest variation of the input for which the measured offset can be significantly distinguished gives the resolution of the sensor.
Good guess is an evaluation by sampling of adequate number of samples to separate resolution information and date (this will not be exactly possible due to noise - see figure).

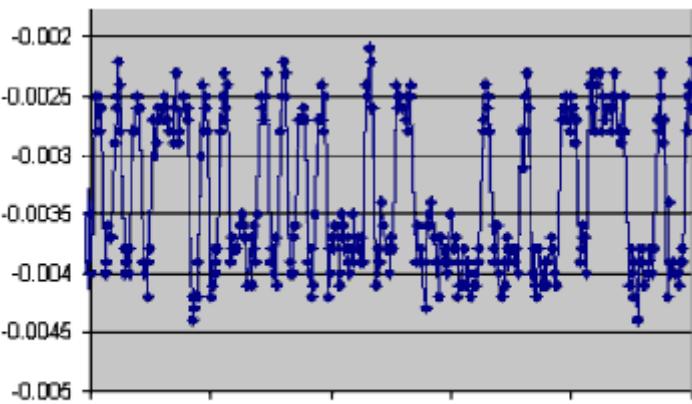


Figure 1: Resolution <2.2mG Verification MM5 – Acceleration (G over time)

F08a_9515⁵ Basically this parameter is specified for all stimuli which does not necessarily mean the zero stimuli. However, most often this parameter is (and may be) tested from zero stimuli an a very small stimuli.

9.2.6 Nonlinearity

F08a_9451 Given by design;

9.2.6.1 Acceleration

F08a_9453 Validation could be done by simulation and/or with centrifuge measurement.

9.2.6.2 Yaw Rate

F08a_9455 Validation could be done by simulation and in 5°/s steps ones for evaluation purpose.

9.2.7 Differential Nonlinearity

F08a_9457 Differential nonlinearity is linked to the step size, not the measurement range. It is calculated by dividing the deviation of two adjacent measurement points of sensitivity from the ideal (linear) sensitivity slope by the step size of 5°/s.

In AK sensor spec. diff. nonlinearity is defined as follows:

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Sensitivity Error [%] = MAX(|(Y(n+1) - Y(n)) / (X(n+1) - X(n)) - S|) / S * 100

S is the sensitivity (best fit), Y is measured rate signal, X is applied rate.

Example: at 100°/s applied yaw rate the sensor shows 101°/s and at 105°/s it shows 108°/s. Then the differential nonlinearity would be $((108^{\circ}/s - 101^{\circ}/s) / (105^{\circ}/s - 100^{\circ}/s) - 1) / 1 * 100 = 40\%$.

9.2.8 Offset

F08a 9460 High resolution in temperature steps (e.g. 1°C) allows finding failures as shown in the following plot.

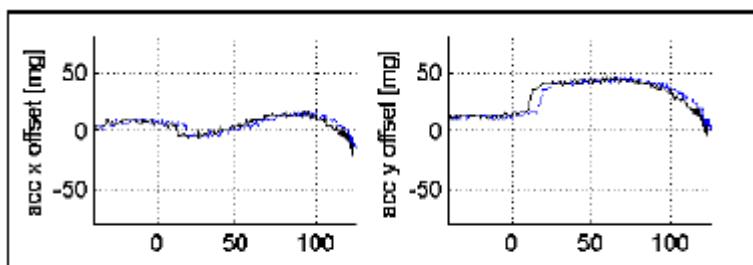


Figure 2: Failure in Offset over temperature in close temperature steps

This kind of measurements take a lot of time if they are used every measurement within the validation plan to proof the lifetime performance. Nevertheless it is useful e.g. to focus on NLIN-TKO.

Measurement of the key parameters (offset, sensitivity) should be performed with adequate steps and at the room, minimal and maximal specified temperature. To evaluate drifts the temperature cycles could be performed in the following way:

RT → ...e.g. 10°C steps... → TT → ... e.g. 10°C steps... → HT → ... e.g. 15°C steps... → RT

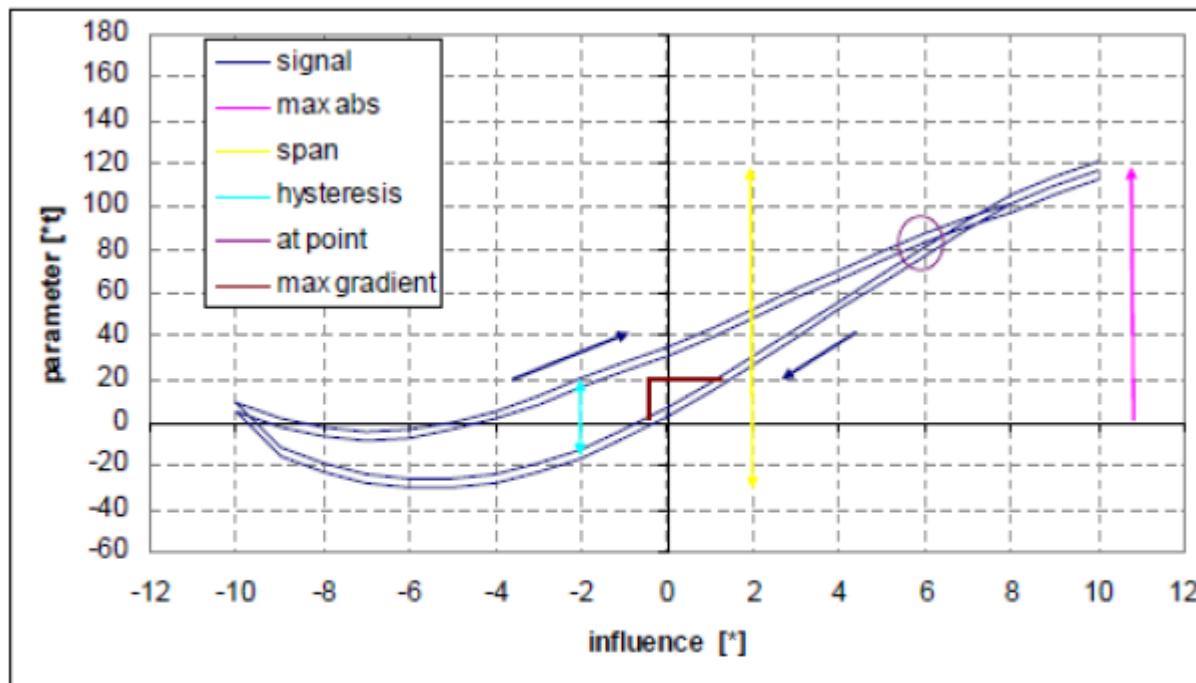
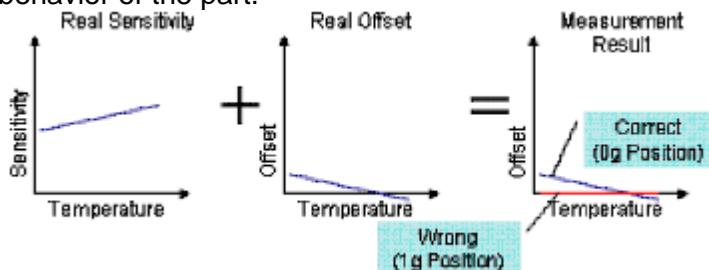


Figure 3: Parameter description for offset

9.2.8.1 Acceleration

F08a_9462 Offset measurements can only be done without stimulus because of a relevant failure due to sensitivity effects. An offset measurement with 1G stimulus would give a combination of the offset and sensitivity behavior of the part.



9.2.8.2 Short Term Drift Span

9.2.8.2.1 Short Term Drift Span at Constant Temperature

- F08a_9519 1. Measurement of start-up drift followed by 100x Pon/Poff cycles with SPI Simulyzer
-temperatures: -40°C, 25°C, 140°C
-rate offset, ACC1-, ACC2- offset
-start-up drift: 500ms - 10min
-Pon/Poff cycles(5s/5s)
-sample rate 62.5Hz, 500ms samples, LF2-filter, 5V SPI-mode
-8 parts soldered on PCB (IS420)
2. Calculate Span = [Max offset - Min offset] from measurement data for each part
3. Calculate [MW + 4s] from span values

9.2.8.2.2 Short Term Drift Span over Temperature

- F08a_9521 1. Measurement of start-up drift with SPI Simulyzer
-temperatures: -40°C, 25°C, 140°C
-rate offset, ACC1-, ACC2- offset
-start-up drift: 500ms - 10min
-sample rate 62.5Hz, 500ms samples, LF2-Filter, 5V SPI-mode
-8 parts soldered on PCB (IS420)
-calculate Span = [Max offset - Min offset] from measurement data for each part
-calculate mean and standard deviation
2. Measurement over temperature in DKT
-32 parts soldered on PCB (IS420) with RB lead-free solder profile
-temperature steps: -40°C, -25°C, 0°C, 25°C, 50°C, 75°C, 100°C, 125°C, 140°C
-the temperature chamber must be turned off during offset measurements
-128 samples, 62.5Hz sample rate, LF2-filter, 5V SPI-mode
-rate offset, ACC1-, ACC2- offset (MMM-values from +/-1g position)
-calculate Span = [Max offset - Min offset] from measurement data for each part
3. Calculate total mean from linear summation of span mean values from measurement [1.] and [2.]; total standard deviation from square summation of span standard deviation values from measurement [1. and 2.]. The worst-case start-up drift from measurement [1.] is
used.
$$\text{total drift span} = MW_1 + MW_2 + 4\left(\sqrt{\sigma_1^2 + \sigma_2^2}\right)$$



9.2.8.2.3 Short Term Drift Span overall

- F08a_9523 1. Measurement of start-up drift with SPI Simulyzer
 -temperatures: -40°C, 25°C, 140°C
 -start-up drift: 500ms - 10min
 -rate offset, ACC1-, ACC2- offset
 -sample rate 62.5Hz, 500ms samples, LF2-Filter, 5V SPI-mode
 -8 parts soldered on PCB (IS420)
 -calculate Span = [Max offset - Min offset] from measurement data for each part
2. Measurement over temperature in DKT
 -32 parts soldered on PCB (IS420) with RB lead-free solder profile,
 -measure parts in humidity-saturated condition after humidity storage 100h at
 85°C/85%r.h.; start DKT-measurement immediately after humidity storage
 -temperature steps: -40°C, -25°C, 0°C, 25°C, 50°C, 75°C, 100°C, 125°C, 140°C
 -at each temperature step, a measurement at 4.5V, 5.5V and 12V supply voltage is taken
 -the temperature chamber must be turned off during offset measurements
 -128 samples, 62.5Hz sample rate, LF2-filter, SPI-mode
 -rate offset, ACC1-, ACC2- offset (MMM-values from +/-1g position)
 -calculate Span = [Max offset - Min offset] from measurement data for each part
3. Calculate total mean from linear summation of span mean values from measurement [1.] and [2.]; total standard deviation from square summation of span standard deviation values from measurement [1. and 2.]. The worst-case start-up drift from measurement [1.] is used.

$$\text{total drift span} = MW_1 + MW_2 + 4\sqrt{\sigma_1^2 + \sigma_2^2}$$

9.2.8.3 Absolute Drift

- F08a_9525 1. Measurement of start-up drift with SPI Simulyzer
 -temperatures: -40°C, 25°C, 140°C
 -start-up drift: 500ms - 10min
 -rate offset, ACC1-, ACC2- offset
 -sample rate 62.5Hz, 500ms samples, LF2-Filter, 5V SPI-mode
 -8 parts soldered on PCB (IS420)
 -calculate Span = [Max offset - Min offset] from measurement data for each part
2. Evaluate measurement data for rate offset, ACC1-, ACC2- offset from lifetime validation (Erprobung) after single lifetime from high-tempearture storage path (passive, soldered on PCB) and temperature cycle path (passive, soldered on PCB). Calculate worst case mean value and standard deviation.
3. Calculate total mean from linear summation of span mean values from measurement [1.] and [2.]; total standard deviation from square summation of span standard deviation values from measurement [1. and 2.]. The worst-case start-up drift from measurement [1.] is used.

$$\text{total drift span} = MW_1 + MW_2 + 4\sqrt{\sigma_1^2 + \sigma_2^2}$$

Reference point is absolute 0 (i.e. 0mg, 0°/s)

9.2.8.4 Yaw Rate

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9.2.9 Sensitivity Hysteresis

F08a_9466 Given by design;

Measure the sensor output signal at all possible stimuli by increasing the stimuli inside the measurement range. Then measure the sensor output signal at all possible stimuli by decrease the stimuli inside the measurement range. The maximum difference between the first and the second measurement gives the hysteresis of the sensitivity.

9.2.10 Noise (rms, peak-peak)

F08a_9469 Noise is measured typically with 100 or 300 samples. For Gaussian noise distribution the peak-peak values are related to the rms value. Therefore peak-peak values and rms values have to be proved against each other in every measurement.

A good guess is, that peak values are within 6 sigma distance from the mean value, e.g. rms-measurements compared:

Parameter	RMS (=SIGMA)	Mean	Min	Max	Mean - 6Sigma	Mean + 6Sigma	Comment
ACCi_AC	0.0029 G	0.005 G	-0.0046 G	0.0147 G	-0.0124 G	0.0224 G	Peak - peak valid
ACCi_AC	0.0025 G	0.001 G	-0.0384 G	0.0075 G	-0.0145 G	0.0155 G	Peak - peak not valid

F08a_9514 Noise signal of the sensor is no white noise. Therefore it is also not to be assumed a Gaussian distribution but the given approx. can be still used for estimations.

The efficient number off samples for measurements has to be derived thin the development process. Value will be measured for every part in production.

9.2.11 Cross-axis sensitivity

F08a_9471 Given by design;

Validation could be done by measurements on the centrifuge.

9.2.12 Overload

F08a_9473 Given by design;

Verification by simulation

9.2.13 Vibration robustness

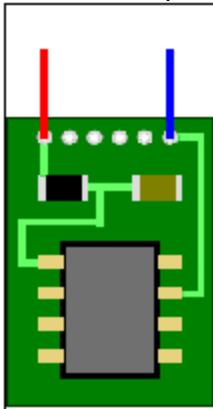
F08a_9475 HOWTO?

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9.2.14 PSRR

[F08a_9479](#) Circuit example for PSRR Measurement:



Failure Criteria:

- $|\text{Rate}| < 1^\circ/\text{s}$ (300°/s full scale)
- $|\text{Acceleration}| < 20\text{mg}$ (5g full scale)

VDD3-Mode:

Voltage ripple at VDD3 without setting any failure flags and output-signal within specified limits ($+/-1^\circ/\text{s}$; $+/-20\text{mG}$). For the frequency range 687kHz $+/-10\%$ and 812.5kHz $+/-10\%$ the acceleration limit is $+/-30\text{mg}$.

- Upcoming Status-Flags

function class A filter setting LF 60Hz & HF 400Hz for rate and acceleration
Inject specified Vpp at sensor supply circuit of VBAT/VDD3

- DC to 1Mhz with 200Hz Steps
- detailed measurement at failing frequencies $+/- 1\text{kHz}$ with 10Hz Steps
- current limitation to 200mA max.
- 200ms waiting time between applying of voltage ripple and start of measurement of output signal

9.2.15 EMC

[F08a_9481](#) Please see related EMC-Documents

9.2.16 Ratiometry

[F08a_9483](#) Offset, sensitivity, noise and occurring flags will be measured at High, Low and Room temperatures specified voltage supply range.

This measurement will be done for characterization purpose ones.

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10. Vibration

10.1 Yawrate

10.1.1 Requirement specification 1.0

#	Conditions	Ω	Unit
1	sin: 0...5Gexternal at ECU, ECU resonances up to 50 (=250 Ginternal over all), 0...50kHz, all axes	<0.1	°/s/ Gexternal
2	sin, 0...50kHz, sensitivity to angular acceleration, all axes	t.b.d.	°/s/ (°/s)
3	200Hz...30kHz, 45 Geff, DC and AC variations	<0.1	°/s/ G

F08b_9696 Provide transfer function of sensitivity versus frequency from 3dB frequency (i.e. 15Hz, 60Hz or 400Hz) to 50kHz with acceleration and angular acceleration in all 3 axis for all sensor channels, if behavior is non linear with respect to stimuli amplitude. Provide description of non linearity.

Provide transfer function of failure monitoring flag versus frequency from 3dB frequency (i.e. 15Hz, 60Hz or 400Hz) to 50kHz with acceleration and angular acceleration in all 3 axis for all sensor channels, if behavior is non linear with respect to stimuli amplitude. Provide description of non linearity.

A development report has to be provided to inform about factors which may influence the sensor within the application.

For all vibration topics, the sensor including its housing must be considered. Especially the transfer function of the housing must be included in all considerations.

The vibration sensitive areas must not be bigger than +/-10%. Target would be a +/-5% tolerance for all areas where the sensor is vibration sensitive.

The sensor should withstand common vibration sources as SMD elements giving vibration to the sensor by relaxing over time and temperature ("knackende Bauelemente"). The specification of such vibration environment: t.b.d V: CC/EPY5 mit AE/EDS3

10.1.2 Target specification

F08b_9404 Requirements of Table 1 can not be fulfilled by sensor due to technical boundaries.

Vibration robustness will be an important task during the development process. Boundaries will change during development process. A "Vibration-Team" will be set up within the project to ensure the focus and information exchange with the customer.

Actually it is not possible to measure the transfer function of the sensor within the frequency range from 200Hz ... 50kHz and accelerations up to 250G. Typical measurement ranges are 200Hz-30kHz@20g, 200Hz ... 4kHz@ 100g, 6-50kHz@100g(several shaker modes > 30kHz). It will be definitely not possible to measure up to 250G over the whole frequency range.

Vibration tests:

1. 200Hz-50kHz@20g sin-sweep
2. 200Hz-4kHz@100g sin-sweep
3. 6-50kHz@100g sin-sweep (several shaker modes > 30kHz)
4. whithe noise: 200Hz-30kHz; aeef=10g; aeef=20g
5. 200Hz/400Hz/1000Hz amp-sweep 0-100g

In the region of the above tests the DLF is verified by measurement.

Therefore measurements can only be provided up to certain acceleration; higher accelerations can only be estimated as far as modeling is possible.

According due to the estimation of DLFs an estimation (consisting of partially simulations, measurements or expert opinions) the failure monitoring flags versus frequency from 3dB frequency (i.e.

15Hz, 60Hz or 400Hz) to 50kHz with acceleration and angular acceleration in all 3 axis for all sensor channels will be provided within the product development process.

For all vibration topics, the sensor including its housing will be considered. Especially the transfer function of the housing will be included in all considerations. To find an optimal solution for the OEM and RB information about the second level package (ECU, SC, ...) shall be provided to the "Vibration-Team" and simultaneous development between AE & CC is necessary.

The vibration sensitive areas will be limited to +/-10% by reduction of the sensor frequency. Reduction of the tollerance (e.g. +/-5%) will be proved during development.

It is necessary to find suitable positions for the sensor within the second level package. Sources of vibration (PCB vibrations, other components ...) shall be avoided or have to be within the accepted limits.

10.1.3 DLF

F08b_9701 DLFs can differ during product development and in final product.

DLFs (allowed amplification (factor) by second level package) are calculated with following assumptions:

- Offset of 0.5°/s allowed
- Stimulation with 5G
- Linear acceleration stimulus
- Worst-Case over all parts

DLFs include the following types of interferences by external vibrations:

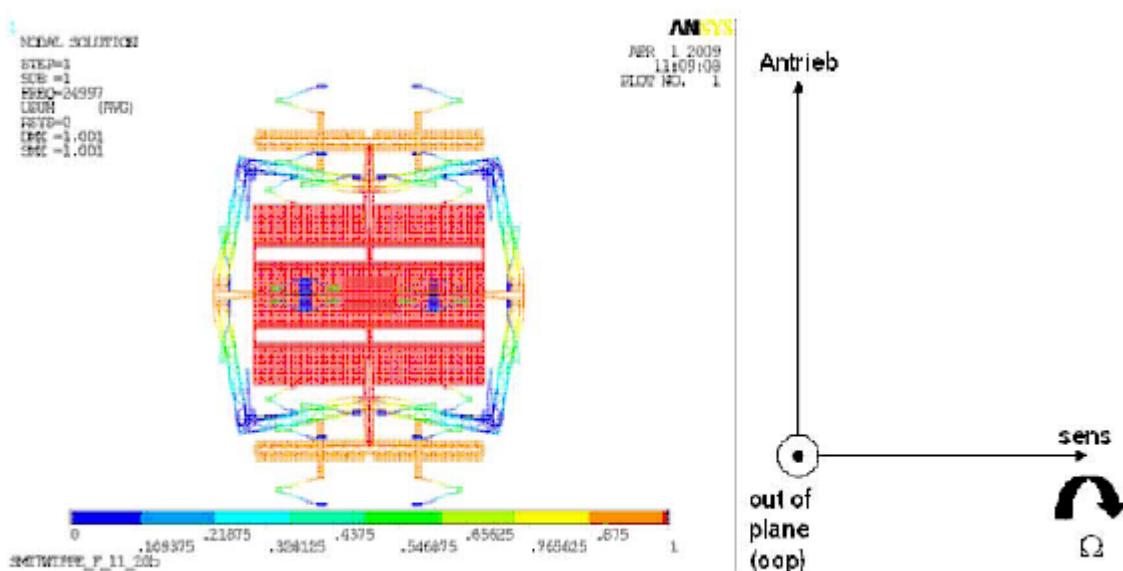
- Error sensitivities due to linear acceleration
- Error sensitivities due to angular acceleration
- Mechanical clipping accelerations of higher sensor modes

DLFs finally include the packge transfer function.

10.1.4 Ω_x sensor element (CMG240M)

10.1.4.1 Definition of the sensor axis

F08b_9408



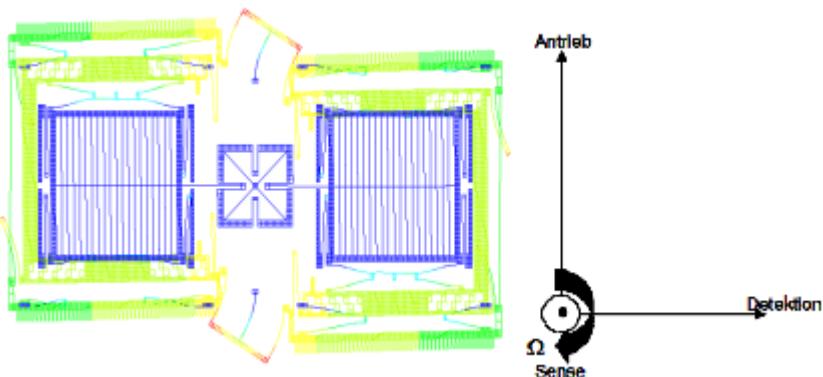
10.1.4.2 DLF

F08b_9703 File name: 20130905_DLF_SMI710_Wx_CMG241M_A10_Var01_V1.8

10.1.5 Ωz sensor element (CMG211N)

10.1.5.1 Definition of the sensor axis

F08b_9420



10.1.5.2 DLF

F08b_9704 File name: 20130828_DLF_CMG211_A5.xlsx

10.2 Acceleration

10.2.1 Requirement specification 1.0

#	Parameter	Conditions	Ω	Unit
1	Offset	sin: 0...5Gexternal at ECU, ECU resonances up to 50kHz (=250Ginternal over all), 0..50kHz, all axes	<0.5	G
2	Sensitivity	sin, 0...50kHz, sensitivity to angular acceleration, all axes	tbd	mG/(°/s) ²
3	Noise	200Hz ... 30kHz, 45Geff, DC and AC variations	<30	mG

F08b_9428

Provide transfer function of sensitivity versus frequency from 3dB frequency (i.e. 15Hz, 60Hz or 400Hz) to 50kHz with acceleration and angular acceleration in all 3 axis for all sensor channels, if behavior is non linear with respect to stimuli amplitude. Provide description of non linearity.

Provide transfer function of failure monitoring flag versus frequency from 3dB frequency (i.e. 15Hz, 60Hz or 400Hz) to 50kHz with acceleration and angular acceleration in all 3 axis for all sensor channels, if behavior is non linear with respect to stimuli amplitude. Provide description of non linearity.

A development report has to be provided to inform about factors which may influence the sensor within the application.

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For all vibration topics, the sensor including its housing must be considered. Especially the transfer function of the housing must be included in all considerations.

The vibration sensitive areas must not be bigger than +/-10%. Target would be a +/-5% tolerance for all areas where the sensor is vibration sensitive.

The sensor should withstand common vibration sources as SMD elements giving vibration to the sensor by relaxing over time and temperature ("knackende Bauelemente"). The specification of such vibration environment: t.b.d V: CC/EPY5 mit AE/EDS3

10.2.2 Target specification

F08b 9430

Requirements of Table 2 can not be fulfilled by sensor due to technical boundaries.

Vibration robustness will be an important task during the development process. Boundaries will change during development process. A "Vibration-Team" will be set up within the project to ensure the focus and information exchange with the customer.

Actually it is not possible to measure the transfer function of the sensor within the frequency range from 200Hz ... 50kHz and accelerations up to 250G. Typical measurement ranges are 200Hz-30kHz@20g, 200Hz ... 4kHz@ 100g, 6-50kHz@100g(several shaker modes > 30kHz). It will be definitely not possible to measure up to 250G over the whole frequency range.

Vibration tests:

1. 200Hz-50kHz@20g sin-sweep
2. 200Hz-4kHz@100g sin-sweep
3. 6-50kHz@100g sin-sweep (several shaker modes > 30kHz)
4. whithe noise: 200Hz-30kHz; aeef=10g; aeef=20g
5. 200Hz/400Hz/1000Hz amp-sweep 0-100g

In the region of the above tests the DLF is verified by measurement.

Therefore measurements can only be provided up to certain acceleration; higher accelerations can only be estimated as far as modeling is possible.

According due to the estimation of DLFs an estimation (consisting of partially simulations, measurements or expert opinions) the failure monitoring flags versus frequency from 3dB frequency (i.e. 15Hz, 60Hz or 400Hz) to 50kHz with acceleration and angular acceleration in all 3 axis for all sensor channels will be provided within the product development process.

For all vibration topics, the sensor including its housing will be considered. Especially the transfer function of the housing will be included in all considerations. To find an optimal solution for the OEM and RB information about the second level package (ECU, SC ...) shall be provided to the "Vibration-Team" and simultaneous development between AE & CC is necessary.

The vibration sensitive areas will be limited to +/-10% by reduction of the sensor frequency. Reduction of these areas (e.g. +/-5%) will be proved during development.

It is necessary to find suitable positions for the sensor within the second level package. Sources of vibration (PCB vibrations, other components ...) shall be avoided or have to be within the accepted limits.



10.2.3 Axy

10.2.3.1 DLF

F08b_9433 DLFs can differ during product development and in final product.

Currently valid DLF estimation can be found here: [DLF_B-Muster CMA625M_v12_2013_02_11_PH.xls](#)

10.2.4 Az

10.2.4.1 DLF

F08b_9436 DLFs can differ during product development and in final product.

Currently valid DLF estimation can be found here: [DLF_B-Muster CMA625M_v11_2013_02_11_PH.xls](#)

10.3 Changes

All	· Discussed smal changes - Mail 26.05.2010 Baus/Fürst · Update: Link of up-to-date XLS-Sheets	AE/ESI3-Ft	18.06.2010
1.4	· Included DLF for Ωz-Variant	AE/ESI1-Pd	25.06.2010
1.2; 2.4	· Changes according T&R-Meeting Baus/Neurohr/Fürst SIMPH-#: 23	AE/ESI3-Ft	21.07.2010
2.3; 2.4	· DLF update SMI7-BS auf Version 6	AE/ESI3-Gu	07.03.2011

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11. Referred documents and standards

Ref.	Description	SAP number / Norm / Link	Date
[01]	SMI7xy Requirement Specification V1.0	Link <Mitgeltende%20Dokumente%202.0/100503_SMI7xy_Technical Specification v1_0.pdf>	03.05.2010
[02]	SMI7xy Parameters Verification Description	Link <20100819_PH_SMI7xx_Measurement And Validation_2.1.pdf>	
[03]	SMI7xy Target Specification Vibration	Tbd.	Tbd.
[04]	CMG241M (x-sensorelement) Data Sheet		t.b.d.
[05]	CMG210M (z-sensorelement) Data Sheet		t.b.d.
[06]	CMA621M (Axy-sensorelement) Data Sheet		t.b.d.
[07]	CMA625M (Ayz-sensorelement) Data Sheet		t.b.d.
[10]	Moisture/ Reflow Sensitivity Classification for Plastic Integrated Circuit (IC) SMDs	IPC/JEDEC J-STD-020	?
[11]	Standard for Handling, Packing, Shipping and Use of Moisture Reflow Sensitive SMDs	IPC/JEDEC J-STD-033	?
[12]	SMI7xy Requirement Specification PSI5 V 2.1	Link	08.10.2012
[13]	Verfahrensvorschrift Fertigung	ABplus_90C_97_001_Bleifrei_Loeten_VV_1269918512	24.02.2010
[14]	<i>Requirement Specification Regarding Sensorcluster with CAN</i>	Link <Mitgeltende%20Dokumente%202.0/100503_SMI7xy_CAN_v1_0.pdf>	
[15]	Test flow SMI700 vorab	Link <20100519_Erprobungsablaufplan_3.0.pdf>	21.05.2010
[16]	EMV Test Plan	Link <Messplan_SMI7XX_29_04_2011_v32>	29.04.2011
[19]	Reliability qualification guideline for semiconductor devices	Nissan_Requirements_ASIC_SENSORS_ANNEK_K06-1 <Mitgeltende%20Dokumente%201.0/AB_Sensoren_45_D_16_A_001_Nissan_Requirements_ASIC_SENSORS_ANNEK_K06-1_d050721.pdf>	29.11.2009
[20]	The guideline for the acceleration sensors	Nissan_Requirements_ACCEL_SENSORS_ANNEK_K06-2 <Mitgeltende%20Dokumente%201.0/AB_Sensoren_45_D_16_A_002_Nissan_Requirements_ACCEL_SENSORS_ANNEK_K06-2_d050721.pdf>	24.02.2009
[21]	Safety Analysis SMI7	Link	18.06.2013

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		<p><<<<<<file:///L:\AENE\ne4\projects\inertial_sensors\smi700\External\35_Funktionale_Sicherheit\01_Safety_Documentation\Safety Analysis\SMI7-B\130618_Safety Analysis SMI7 v2.0.pdf>>>>>></p> <p>≥ or</p> <p>DOORS: doors://rt-doors-prod.rt.de.bosch.com/?version=2&prodID=0&urn=urn:telelogic::1-4703a8ec13874cb4-M-0000b480 Baseline 6.1</p>	
[22]	AEC-Q100 Validation plan	Link <20100723_AEC-Q100_Ablaufplan_0.1.pdf>	23.07.2010
[23]	SW-PH	20101104_PH_SMI7xx_SW_0.1.pdf	13.10.2010
[24]	PSI5 V2.0 + "Substandard Vehicle Dynamics"	110601_psi5_spec_v20_base 110601_psi5_spec_v20_vehicle dynamics control	30.03.2012
[25]	DSP-Register	file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne1/30_projects/30_asic/TI/TIG700_external/02 ASIC/01 Design-Spec/99_work/27_Register-Management/current/sDSP/sDSP_TrimMap.html	29.09.2011

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12. Responsibilities

F13_7758 If you have any queries please do not hesitate to contact one of the following persons depending on the chapter.

01 Introduction	Schellin Bernt (AE/ESI3)
02 Miscellaneous	Schellin Bernt (AE/ESI3), AVT: Hoefer Holger (AE/ESE6)
03 Electrical Interface	CAN: Schrimpf Thomas (AE/ESI2) SPI: Nopper Reinhard (AE/ESI1) PSI: Garic Diko (AE/ESI3)
04 Parameter Specification	Schellin Bernt (AE/ESI3) ACC: Wang Chunyu (AE/ESI3) YRS: Keck Marian (AE/ESI1)
05 Qualification Requirements	Antal Peter (AE/ESI-E-Bp), EMC/ESD: Petzold Klaus (AE/ESI1)
06 Customer Models	Benyei Zoltan (AE/ESI-S-Bp)
07 Safety Concept	Wienss Andreas (AE/ESI3)
08 Terms And Definitions	Schellin Bernt (AE/ESI3)
09 Measurement and Validation	Petzold Klaus (AE/ESI1)
10 Vibration	Keck Marian (AE/ESI1)
11 Referred Documents And Standards	Schellin Bernt (AE/ESI3)
12 Responsibilities	Schellin Bernt (AE/ESI3)