

**BOSCH**

Department AE/ESI

**Internal Datasheet  
SMA7**

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SAP: V2, DOORS: 5.3

Date 17/01/2022

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**Versions:**

V1.12: Initial version. Valid for A-samples and based on Pflichtenheft

V2.31: Valid for C1-samples. Includes several change requests (see project CR list) and updates based on A-samples

V3.1: Valid for C2-samples. Updated based on C1-sample performance, change requests and customer feedback.

V4.1: Final version. Valid for series production. Including all updates based on C2-sample characterization and qualification. Removed DFN.

V5.0: Update for QGC4. Valid for series production. Updated based on change requests and customer feedback. Added SMA765.

V5.1: Added new LGA 2<sup>nd</sup> source TTNr's. Updated based on post-QGC4 characterization and errata.

V5.2: Changed XSOC offset samples, unified 45° parameters.  
SAP V1, ECR 1039R15963

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## 1. Introduction

5161 The SMA7 sensors are acceleration sensors designed for crash sensing in automotive safety applications. The acceleration data is digitally transmitted via SPI or PSI5 interface.

### SPI Sensors

5162 The SPI sensors are central accelerometers for airbag control units in the passenger compartment. They transmit their data via bidirectional SPI interface.

The SMA760 is a two channel accelerometer with XY sensing directions and a measurement range of 128g. It is intended to be used for crash detection.

The SMA765 is a two channel accelerometer with XY sensing directions and a measurement range of 240g. It is intended to be used for crash detection.

The SMA720 is a two channel accelerometer with XZ sensing directions and a measurement range of 128g for X direction and 32g for Z direction. It is intended to be used for crash detection, roll-over detection and plausibility check.

All three SPI sensors use a SOIC8n package.

### PSI5 sensors

5163 The PSI5 sensors transmit their data with a two wire current interface. They are designed to be used as peripheral or upfront sensors in crash detection. This sensors are available as dual channel accelerometers with XY or XZ sensing direction and as single channel accelerometers with X, Y and Z sensing direction. The available measurement ranges are 30g, 60g, 120g 240g and 480g. Furthermore, it can be chosen between two different packages: The SOIC8n and the LGA (4x5mm<sup>2</sup>). The LGA package is a system-in-a-package (SIP) and contains all passive components, which are need to use the sensor. It is designed to be used in metal-clamps, which provide additional shielding against EMC. For details about possible combinations of package, range and sensing direction please refer to the next chapter.

5164 Main features of the sensors are:

- Full bipolar power-on self test of mechanical and electrical signal path
- On-chip digital FIR output filter
- On-Chip Oscillator with 17.9 MHz
- Development according ISO26262 standard
- Automotive temperature range: -40°C to +125°C

#### SPI sensors:

- supply voltage range 3.3V or 4.5V-11V
- 14bit resolution of data
- Two selectable SPI protocols:
  - BoschSPI (inframe)
  - SafeSPI (out-of-frame)

#### PSI5 sensors:

- supply voltage range 4.5 - 11V
- PSI5 V1.3 and V2.1 compatible communication interface (125 kBit/s or 189 kBit/s)
- Separate I\_DATA pin for generating Manchester code
  - configuration for synchronous data transmission with parallel and serial (daisy chain) bus and asynchronous data transmission
  - 10bit, 16bit or 20bit transmitted per datagram with transmission rates 1kHz, 2 kHz or 4kHz
  - Advanced transmission timing to enable PSI5 modes with high data density
- μCut functionality (short disconnection of power supply does not lead to reset of sensor)
- End of line programming via PSI5 FastBiDir (7.2 kbaud) interface
- Transmission of an individual part number during initialization
- 45 bits of customer specific initialization data within OTP
  - Option to deactivate fast offset cancellation after power-up and continuous slow offset cancellation during normal operation (after Init Phase 3)
  - Programmable polarity



5165

This product is solely intended for the above mentioned use. Its use is only permitted under the specified conditions and according to the environmental and loading conditions specified in this document. Any change in the product's operating environment from the original scope of validation, or use in applications not approved by Robert Bosch GmbH, must be communicated to and released by Robert Bosch GmbH.

## 1.1 Components within SMA7 Family

### 1.1.1 ECU Variants (SO8 Package, SPI communication)

4171

All components in this chapter are using a SOIC8 package and SPI communication interface.

#### 1.1.1.1 SMA760

5179

Part number 0273141273, 0273141561

ID	parameter / condition	min	typ	max	unit
190	Sensing Directions		X / Y		
191	Measurement range both channels		+/-128		g
192	Sensitivity both channels; @ 14bit		64		LSB/g
1982	CMA		CMA581R		

#### 1.1.1.2 SMA720

5180

Part number 0273141272, 0273141560

ID	parameter / condition	min	typ	max	unit
202	Sensing Directions		X / Z		
203	Measurement range X channel		+/-128		g
1985	Measurement range Z channel		+/-32		g
1986	Sensitivity X channel, @14bit		64		LSB/g
204	Sensitivity Z channel; @ 14bit		256		LSB/g
1987	CMA		CMA582R		

#### 1.1.1.3 SMA765

5500

Part number 0273141461

ID	parameter / condition	min	typ	max	unit
5358	Sensing Directions		X / Y		
5359	Measurement range both channels		240		g
5360	Sensitivity both channels; @ 14bit		32		LSB/g
5361	CMA		CMA584R		



### 1.1.2 Peripheral sensor with LGA 4x5 SiP (PSI5 communication)

4179

All components in this chapter are using the LGA 4 x 5 mm<sup>2</sup> package and the PSI5 communication interface.

#### 1.1.2.1 SMA780

5181

Part number SMA780: 0273141359, SMA780.1: 0273141490.

Collective number SMA780A: 1277340646 (includes SMA780 and SMA780.1).

In the following, all SMA780x variants are collected in the naming SMA780.

ID	parameter / condition	min	typ	max	unit
4195	Sensing Direction		X		
4196	Measurement range		120; 240		g
4197	Sensitivity 10bit PSI5		4; 2		LSB/g
4198	Sensitivity 16bit PSI5		64		LSB/g
4199	Resolution 16bit PSI5		1; 2		LSB
4200	CMA		CMA584R		

#### 1.1.2.2 SMA781

5182

Part number SMA781: 0273141360, SMA781.1: 0273141491.

Collective number SMA781A: 1277340647 (includes SMA781 and SMA781.1).

In the following, all SMA781x variants are collected in the naming SMA781.

ID	parameter / condition	min	typ	max	unit
285	Sensing Direction		Z		
286	Measurement range		120; 240; 480		g
287	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
288	Sensitivity 16bit PSI5		64		LSB/g
4096	Resolution 16bit PSI5		1; 2; 4		LSB
4182	CMA		CMA585R		

#### 1.1.2.3 SMA782

5183

Part number SMA782: 0273141294, SMA782.1: 0273141487.

Collective number SMA782A: 1277340643 (includes SMA782 and SMA782.1).

In the following, all SMA782x variants are collected in the naming SMA782.

ID	parameter / condition	min	typ	max	unit
271	Sensing Directions		X / Y		
272	Measurement range		120; 240		g
273	Sensitivity 10bit PSI5		4; 2		LSB/g
274	Sensitivity 16bit PSI5		64		LSB/g
4098	Resolution 16bit PSI5		1; 2		LSB



ID	parameter / condition	min	typ	max	unit
4180	CMA		CMA584R		

#### 1.1.2.4 SMA783

5184

Part number SMA783: 0273141295, SMA783.1: 0273141489.

Collective number SMA783A: 1277340645 (includes SMA783 and SMA783.1).

In the following, all SMA783x variants are collected in the naming SMA783.

ID	parameter / condition	min	typ	max	unit
278	Sensing Directions		X / Z		
279	Measurement range		120; 240; 480		g
280	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
281	Sensitivity 16bit PSI5		64		LSB/g
4097	Resolution 16bit PSI5		1; 2; 4		LSB
4181	CMA		CMA585R		

#### 1.1.2.5 SMA790

5185

Part number SMA790: 0273141364, SMA790.1: 0273141492.

Collective number SMA790A: 12733141648 (includes SMA790 and SMA790.1).

In the following, all SMA790x variants are collected in the naming SMA790.

ID	parameter / condition	min	typ	max	unit
4188	Sensing Direction		X		
4189	Measurement range		240; 480		g
4190	Sensitivity 10bit PSI5		2; 1		LSB/g
4191	Sensitivity 16bit PSI5		64		LSB/g
4192	Resolution 16bit PSI5		2; 4		LSB
4193	CMA		CMA588R		

#### 1.1.2.6 SMA792

5186

Part number SMA792: 0273141296, SMA792.1: 0273141488.

Collective number SMA792A: 1277340644 (includes SMA792 and SMA792.1).

In the following, all SMA792x variants are collected in the naming SMA792.

ID	parameter / condition	min	typ	max	unit
292	Sensing Directions		X / Y		
293	Measurement range		240; 480		g
294	Sensitivity 10bit PSI5		2; 1		LSB/g
295	Sensitivity 16bit PSI5		64		LSB/g
4095	Resolution 16bit PSI5		2; 4		LSB
4183	CMA		CMA588R		



### 1.1.3 Peripheral sensor with SO8 (PSI5 communication)

4201

All components in this chapter are using the SOIC8 package and the PSI5 communication interface.

#### 1.1.3.1 SMA750

5187

Part number 0273141356

ID	parameter / condition	min	typ	max	unit
2239	Sensing Direction		Y		
2240	Measurement range		120; 240; 480		g
2241	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
2242	Sensitivity 16bit PSI5		64		LSB/g
4085	Resolution 16bit PSI5		1; 2; 4		LSB
4202	CMA		CMA584R		

#### 1.1.3.2 SMA751

5188

Part number 0273141357

ID	parameter / condition	min	typ	max	unit
2246	Sensing Direction		Z		
2247	Measurement range		120; 240; 480		g
2248	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
2249	Sensitivity 16bit PSI5		64		LSB/g
4086	Resolution 16bit PSI5		1; 2; 4		LSB
4203	CMA		CMA585R		

#### 1.1.3.3 SMA752

5189

Part number 0273141298

ID	parameter / condition	min	typ	max	unit
2253	Sensing Directions		X / Y		
2254	Measurement range		120; 240; 480		g
2256	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
2257	Sensitivity 16bit PSI5		64		LSB/g
4087	Resolution 16bit PSI5		1; 2; 4		LSB
4204	CMA		CMA584R		

#### 1.1.3.4 SMA753

5190

Part number 0273141300

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ID	parameter / condition	min	typ	max	unit
2261	Sensing Directions		X / Z		
2262	Measurement range		120; 240; 480		g
2263	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
2264	Sensitivity 16bit PSI5		64		LSB/g
4088	Resolution 16bit PSI5		1; 2; 4		LSB
4205	CMA		CMA585R		

## 1.1.3.5 SMA755

5191

Part number 0273141358

ID	parameter / condition	min	typ	max	unit
2268	Sensing Direction		X		
2269	Measurement range		240; 480		g
2270	Sensitivity 10bit PSI5		2; 1		LSB/g
2271	Sensitivity 16bit PSI5		64		LSB/g
4089	Resolution 16bit PSI5		2; 4		LSB
4206	CMA		CMA588R		

## 1.1.3.6 SMA757

5192

Part number 0273141299

ID	parameter / condition	min	typ	max	unit
2282	Sensing Directions		X / Y		
2283	Measurement range		240; 480		g
2284	Sensitivity 10bit PSI5		2; 1		LSB/g
2285	Sensitivity 16bit PSI5		64		LSB/g
4091	Resolution 16bit PSI5		2; 4		LSB
4208	CMA		CMA588R		

## 1.1.3.7 SMA773

5364

Part number 0273141302

ID	parameter / condition	min	typ	max	unit
5313	Sensing Directions		X / Y		
5315	Measurement range		30; 60		g
5320	Sensitivity 10bit PSI5		16; 8		LSB/g
5321	Sensitivity 16bit PSI5		64		LSB/g
5322	Resolution		1		LSB

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ID	parameter / condition	min	typ	max	unit
	16bit PSI5				
5329	CMA		CMA581R		

**1.1.3.8 SMA774**

5365

Part number 0273141303

ID	parameter / condition	min	typ	max	unit
5324	Sensing Directions		X / Z		
5325	Measurement range		30; 60		g
5326	Sensitivity 10bit PSI5		16; 8		LSB/g
5327	Sensitivity 16bit PSI5		64		LSB/g
5328	Resolution 16bit PSI5		1		LSB
5330	CMA		CMA582R		

**1.1.3.9 SMA758**

5366

Part number 0273141301

ID	parameter / condition	min	typ	max	unit
2289	Sensing Direction		X		
2290	Measurement range		120; 240; 480		g
2291	Sensitivity 10bit PSI5		4; 2; 1		LSB/g
2292	Sensitivity 16bit PSI5		64		LSB/g
4092	Resolution 16bit PSI5		1; 2; 4		LSB
4209	CMA		CMA584R		

**1.2 Related Documents**

5387

- AK-LV27: Global Specification v1.20
- AK-LV27 Part2: Environmental Requirements and Validation v1.2
- AK-LV27 Part4: Sensor Simulation Model v2.0
- AK-LV27 Part6: XY Sensor Requirements v1.0
- PSI5 Specification Rev. 1.3 ([www.psi5.org](http://www.psi5.org))
- PSI5 Base Specification Rev. 2.1 ([www.psi5.org](http://www.psi5.org))
- PSI5 Specification Rev. 2.1 - Airbag Substandard ([www.psi5.org](http://www.psi5.org))
- AEC-Q100 Rev - H: Failure Mechanism Based Stress Test Qualification For Integrated Circuits ([www.aecouncil.com](http://www.aecouncil.com))
- BISS Rev. 2.0: Generic IC EMC Test Specification ([www.zvei.org](http://www.zvei.org))
- JEDEC MS-012F: Standard - Plastic Dual Small Outline (SO) Family, Gull Wing, 1.27 mm Pitch Package ([www.jedec.org](http://www.jedec.org))
- BOSCH Process Specification Manufacturing: Requirements for SMT and THT Devices (1 269 918 500, 13.12.2013)

5397

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- Nissan semiconductor spec  
(file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration\_sensors/sma76x/External/02\_Specification\_TCI/03\_PH/Documents/Linked/Nissan-semiconductor\_spec.pdf)
- Nissan Sensor spec  
(file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration\_sensors/sma76x/External/02\_Specification\_TCI/03\_PH/Documents/Linked/Nisssan\_sensor\_spec.pdf)
- Toyota ECU Spec  
(file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration\_sensors/sma76x/External/02\_Specification\_TCI/03\_PH/Documents/Linked/Toyota\_ECU\_spec.pdf)
- IPC/J-STD-020E: Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices ([www.jedec.org](http://www.jedec.org))
- IPC/J-STD-033C: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices ([www.jedec.org](http://www.jedec.org))

5483  
5484  
5398  
5399  
5478 EMC Testplan

Adobe Acrobat Document

- SMA7xx C2 Plattform EMV Erprobungsplan V2.4  
(file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration\_sensors/sma76x/External/07a\_EMV/C2-Sample/Testplan/16T3013\_SMA7xx\_C2\_Plattform\_EMV-Erprobungsplan\_V2\_4\_signed.pdf)

## 5480 EMC limits



Adobe Acrobat Document

- SMA7 Plattform EMV limits V1.3  
(file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration\_sensors/sma76x/External/07a\_EMV/C2-Sample/Testplan/20181119\_SMA7-Plattform\_EMV\_Limits\_v1\_3.pdf)
- Hyundai/KIA Engineering Specification: Specification for delamination criteria of automotive semiconductors (SPEC No. ES90000-02)



## 2. Functional description

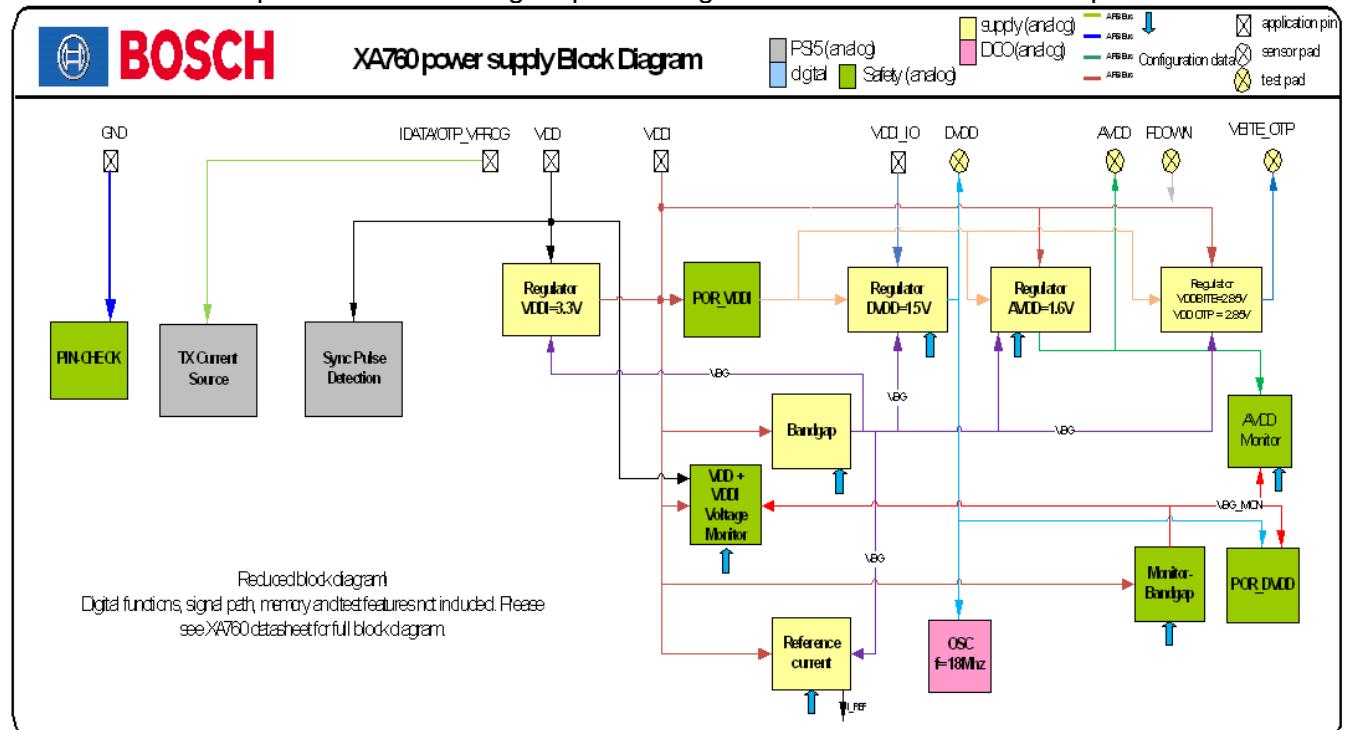
5166

The SMA7 acceleration sensors are all based upon a two-chip concept – the micro-machined mechanical sensing element (CMA) and a separate evaluation ASIC (XA760) both combined in one package.

On the sensor chip, a silicon surface micro-machined comb structure is used as a capacitive accelerometer. The structure forms a differential capacitor, consisting of a movable seismic mass suspended by silicon spring bars, and fixed counter electrodes. Due to acceleration in the sensing axis, the seismic mass deflects. This deflection results in a capacitance change which is evaluated by the ASIC. The micro-machined structures on the surface of the sensor chip are protected and hermetically sealed by a micro-machined silicon cap.

The detailed description of the ASIC signal processing can be found in the next chapter.

5520





## 2.1 Signal path

2186

The XA760 signalpath can process the acceleration signal from two capacitive MEMS acceleration sensors.

5167

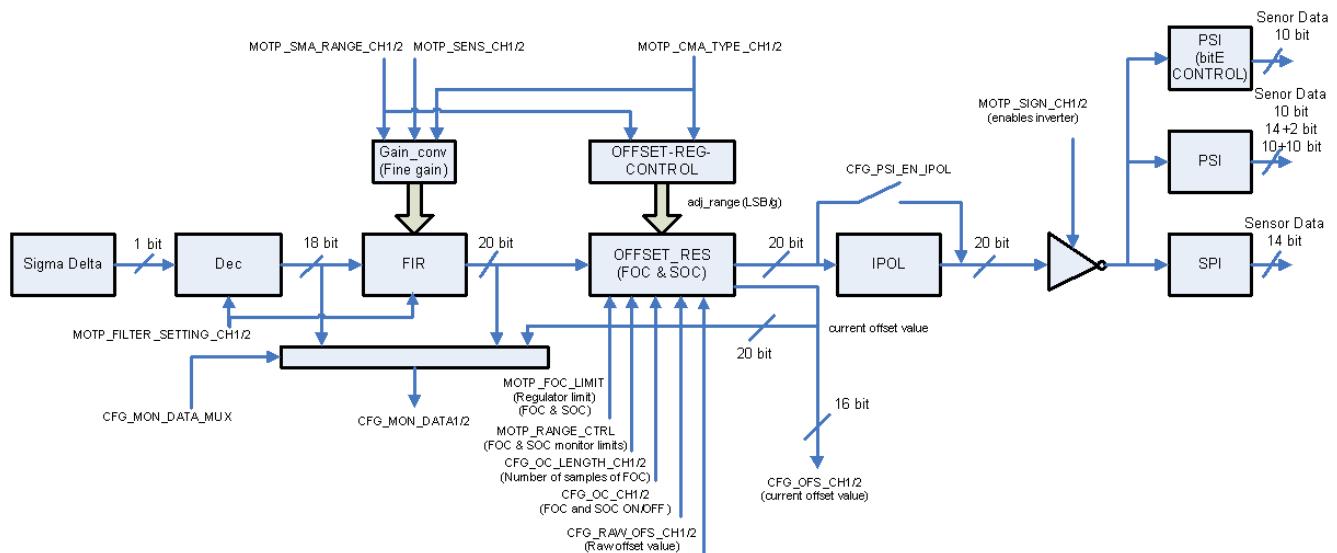
The schematic of SMA7 signal path is shown in the figure below. An acceleration signal along the sensitive axis of the MEMS element causes a change of the capacitances of the MEMS element. This change is converted by a  $\Delta$ -converter into a digital serial bit stream. Then, the digital values are low-pass filtered by a decimation filter and an FIR-filter. Afterwards the gain is adjusted and the offset subtracted. To guarantee low jitter and high performance linear interpolation takes place. The final bits for data transmission are derived from the output of the interpolator by truncation of a number of MSB or LSB. The details depend on the used communication mode.

4407

### Bit width

2141

Block diagram of the ASIC signal path:



2143

Schematic of the bitwidth:



Signal Path Modul /		Bit exponent n (Bit value $2^n$ in LSB unit)	Gains of Module
C/V conversion stage [V/dC/C]			*0.84
Sigma Delta Convert dC/C to Bitstream[1V]			*1.33
Overall analog front end gain product of C/V conversion stage and sigma delta modulates gains			*1.12
BITSTREAM(1 BIT)		0	
Decimation Filter: Filter values and convert bitstream to 18 Bit word.			*0.84375
DEC_OUT (18 BIT)		[17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0]	
FIR Filter: Filter values and apply gains. Specific gain depending on register settings.			*4 * 12324 * coarse_gain {MOTP_SENS_CH1/2} +0.25 512
FIR OUT (20 Bit)		[19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0]	
Offset-Regulator			*1
OFS (20 Bit)		[19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0]	
Output path: Adapt the output bitwidths by shifting and rounding			
Sensor Data Bits (10 Bit) Sensor Data PSI (10 Bit)		x x x x x x x x x x	*1/256
Sensor Data PSI (14+2 Bit), SMA=480g		x x x x x x x x x x	*1/128
Sensor Data PSI (14+2 Bit), SMA=240g		x x x x [16 15 14 13 12 11 10 9 8 7 6 5 4 3 0] 0b0 0b0	*1/2
Sensor Data PSI (14+2 Bit), SMA=120g		x x x x [16 16 15 14 13 12 11 10 9 8 7 6 5 4 3 0] 0b0 0b0	*1/4
Sensor Data PSI (14+2 Bit), SMA=60g		x x x x [16 16 16 15 14 13 12 11 10 9 8 7 6 5 4 3] 0b0 0b0	*1/8
Sensor Data PSI (14+2 Bit), SMA=30g		x x x x [16 16 16 16 15 14 13 12 11 10 9 8 7 6 5 4 3] 0b0 0b0	*1/16
Sensor Data PSI (14 Bit)		x x x x x x x x x x	*1/32
Overall signal path gain for MOTP_SENS_CH1/2 = 255			0.8735 or 1.7469 or 3.4939 or 6.9877

4408

2148

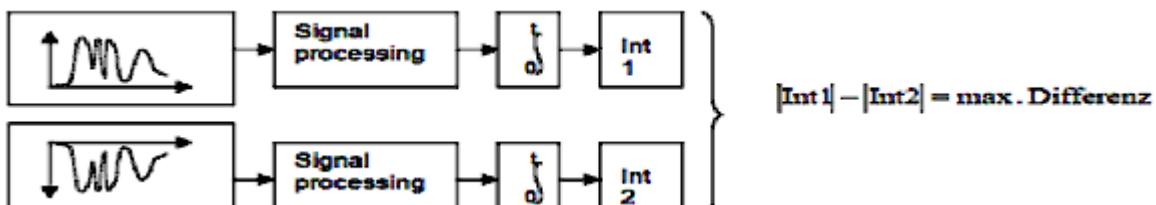
2151

2150

### Symmetry:

The signal path is symmetrical. This means, that a same but opposed signed input value leads to the same but opposed signed output value. Integration of the positive or the negative signal leads to a similar value (positive - negative).

The complete signal path uses symmetrical rounding, whenever the bit width is reduced.



ID	parameter / condition	min	typ	max	unit
2149	Maximum difference of the integrated output value for two opposed but similar input values over a defined time with a defined readout sampling rate (Difference =  integral of positive output values + Integral of negative output values )  Readout with 2kHz for 200ms		0	1	LSB

4409

4410

4411

### Timing:

Update rates and signal delays within the different blocks of the signal path:

[860 Hz filter setting](#)

Nominal update rate:

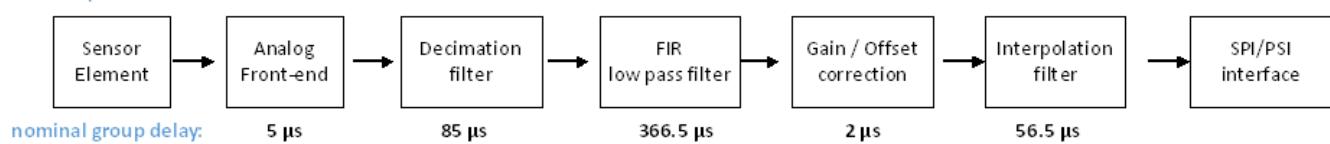
426 kHz

17.8 kHz

17.8 kHz

17.8 kHz

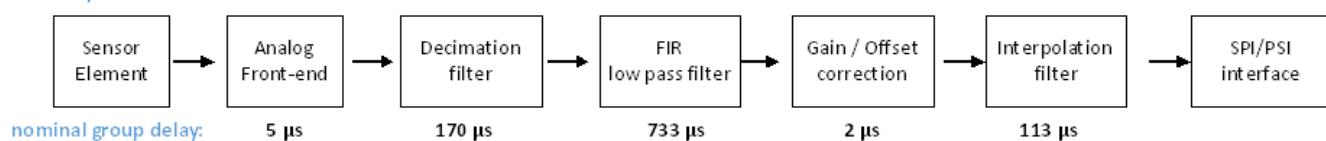
2.2 MHz



4412

430 Hz filter setting

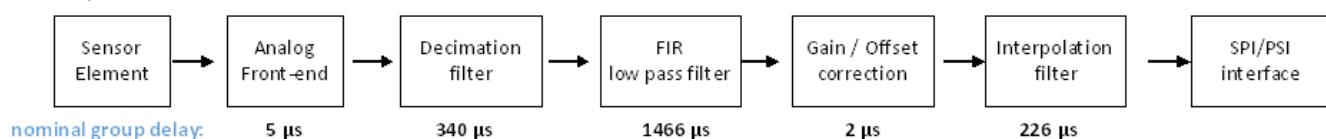
Nominal update rate:



4413

215 Hz filter setting

Nominal update rate:



4414

53 Hz filter setting

Nominal update rate:



3876

The following signal delays are referring to the group delay between applying an input signal (acceleration for SMA or dC/C for ASIC) and ASIC output interface. For the interpolator the group delay equals one sample period at interpolator output.

3958

The signal delays are valid for SPI and synchronous PSI communication.

3959

For asynchronous PSI communication, all values are reduced by the signal delay of the linear interpolator (no interpolation is used in this mode).

3960

The tolerance for all signal delays in the ASIC part of the signal path is identical to the oscillator tolerance.

3961

The step response (settling time) of the ASIC signal path equals two times the signal delay (group delay).

ID	parameter / condition	min	typ	max	unit
1696	Signal Delay 856Hz filter mode; incl. MEMS and Linear Interpolation			0.7	ms
1697	Signal Delay 430Hz filter mode; incl. MEMS and Linear Interpolation		1.15	1.21	ms
1699	Signal Delay PSI5, 30/60g-Types; 430Hz filter mode; asynchronous communication; incl. MEMS		1.04	1.09	ms
4551	Signal Delay PSI5, 120/240/480g-Types; 430Hz filter mode; asynchronous communication; incl. MEMS		0.99	1.04	ms
1698	Signal Delay 215Hz filter mode; incl. MEMS and Linear Interpolation		2.18	2.29	ms
3225	Signal Delay 53Hz filter mode; incl. MEMS and Linear Interpolation		8.25	8.65	ms
417	Signal Delay of Linear Interpolation 430Hz Filter-Mode		113		μs
4392	Signal Delay of Linear Interpolation		226		μs

**BOSCH**

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**Internal Datasheet  
SMA7**

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Date 17/01/2022

1.279.929.850

<b>ID</b>	<b>parameter / condition</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>unit</b>
	215Hz Filter-Mode				
4897	Signal Delay of Linear Interpolation 53Hz Filter-Mode		904		µs
2199	Signal delay MEMS only			126	µs
5462	Clipping of Signalprocessing SMA760, SMA720-X SMA773, SMA774-X 30/60/120 g range; decimation filter output	542			g
5463	Clipping of Signalprocessing SMA774-Z, SMA720-Z 30/60 range decimation filter output	318			g
5464	Clipping of Signalprocessing SMA752/765/750/753/751/783/781/757/755 120/240/480 g range decimation filter output	1794			g
5465	Clipping of Signalprocessing SMA760, SMA720-X 120 g range; FIR filter output	440			g
5466	Clipping of Signalprocessing SMA773, SMA774-X 30 g range; FIR filter output	110			g
5467	Clipping of Signalprocessing SMA773, SMA774-X 60 g range; FIR filter output	220			g
5468	Clipping of Signalprocessing SMA774-Z, 720-Z 30 g range; FIR filter output	64			g
5469	Clipping of Signalprocessing SMA774-Z 60 g range; FIR filter output	129			g
5470	Clipping of Signalprocessing SMA752/765/750/753/751/783/781 120 g range; FIR filter output	364			g
5471	Clipping of Signalprocessing SMA752/765/750/753/751/783/781/757/755 240 g range; FIR filter output	728			g
5472	Clipping of Signalprocessing SMA752/765/750/753/751/783/781/757/755 480 g range; FIR filter output	1456			g
4828	Sign of output value: If the capacity value between C1x and CMx pads is higher than the capacity between C2x and CMx pad (i.e. C1>C2), then the output of the signal path (SPI/PSI) will have a positive sign. For definition of C1x, CMx, C2x pads see ID3796 MOTP_SIGN_CHx=0				



## 2.1.1 Analog Frontend

2032

The analog frontend consists of C/V-converter and a sigma delta converter.

The differential capacitance change  $\Delta C/C$  in the micromachined sensor element, corresponding to an acceleration in the sensing axis, is C/V converted first. Then the voltage is converted into a digital serial bit stream by a  $\Delta\Sigma$  converter. The bitstream is then further processed by the digital signal path.

The decimated and filtered bitstream corresponds to the dC/C value.

ID	parameter / condition	min	typ	max	unit
366	Sampling Rate of the frontend tolerance identical to oscillator		426		kHz

5515

The frontend frequency equals  $f_{osc}/42$ .

ID	parameter / condition	min	typ	max	unit
364	Overall analog frontend gain, i.e. C/V converter and SDM		28/25		
2012	Noise with 430Hz filter			6.6	1e-5 dC/C

2028

A test mode of the frontend using ASIC internal capacitors instead of a connected CMA is implemented. These internal capacitors are implemented in pseudo-diff configuration

2029

During test mode the CM terminals of a wired CMA can be disconnected by ASIC internal switches.

2034

The frontend contains random chopping. The random chopping can be deactivated by OTP programming.

2128

There are no idle tones above specified noise floor after applying decimation and low pass filter.

## 2.1.2 Selftest

2887

For the sensor self-test the sensor-element is deflected by applying an electrical field (BITE = build in test). The BITE is covering a full testing of the complete signal evaluation path including the micro-machined sensor element and the evaluation ASIC. An electrostatic force causes a physical deflection of the seismic mass of the sensor element. The deflection can be applied in positive and negative direction.

5168

The BITE is executed automatically in PSI mode and must be triggered before EOP in SPI mode. This is described more in detailed in the corresponding interface chapters.

4393

The minimum selftest response is at least 10% of full range for SMA720 and SMA760. The minimum self test response is sufficient to use the BITE as startup monitor for sensing element and signal path according to the SMA7 functional safety requirements.

2044

There is no snapping of the sensor for external applied accelerations up to +/-25g, even if the specified Testsignalvoltage is applied.

2045

If the sensor is deflected until clipping/snapping due to an external acceleration >25g, the sensor will go back to normal BITE deflection as soon as there is no external acceleration anymore. (Assured by keeping the release voltage higher than the effective BITE voltage)

2197

There is no snapping of the sensor during normal operation (no testsignal applied).

2196

There is no stiction of the sensor during normal operation (no testsignal applied).

2040

The BITE voltage can be switched between two levels by an OTP bit. The correct setting is programmed during final test depending of the used MEMS element.

3712

After deactivation of the selftest (e.g. by SPI command) or the change of the FIR filter frequency it takes a certain time, before the data at the output is valid again (no more influence of the selftest). This is called filter flush time. This time is used to delay the deactivation the corresponding flags.

ID	parameter / condition	min	typ	max	unit
447	Filter flush time (TST-Flag deactivation delay) ECU-Types; 860Hz filter mode	1.74	2.06	2.40	ms
448	Filter flush time (TST-Flag deactivation delay)	2.61	2.98	3.336	ms



ID	parameter / condition	min	typ	max	unit
	ECU-Types; 430Hz filter mode				
449	Filter flush time (TST-Flag deactivation delay) ECU-Types; 215Hz filter mode	4.36	4.81	5.27	ms
451	Filter flush time (TST-Flag deactivation delay) ECU-Types; 53Hz filter mode	16.13	17.17	18.20	ms

### 2.1.3 Decimation filter

2047

The decimation filter is a third order filter that down-samples the 1 bit digital signal from the Delta Sigma ADC, by a factor of 24, 48, 96 or 384 into a 18 bit wide parallel data word. The data range is clipped in order to prevent an overflow.

4394

The transfer function is given by

$$H(z) = C * 1/D^3 * \left( \frac{1 - z^{-D}}{1 - z^{-1}} \right)^3$$

Decimation factor D can be 24, 48, 96, 384 and depends on the choose filter frequency.

ID	parameter / condition	min	typ	max	unit
2049	Gain of the decimation filter C		0.84375		

### 2.1.4 Low Pass Filter

2063

The filter is an FIR filter with the following coefficients  $b_i$ :  
 $\{9, 25, 52, 87, 125, 157, 176, 176, 157, 125, 87, 52, 25, 9\}$

3930

The transfer function is given by:

$$H(z) = \frac{\sum_{i=0}^{13} b_i z^{-i}}{\sum_{i=0}^{13} b_i}$$

368

Filter frequency is selectable for each channel individually.

For PSI5 application it can be selected by programming the OTP register MOTP\_FILTER\_SETTING\_CH1/2. For SPI it can be selected by writing the register CFG\_FILTER\_CH1/2.

4833

During the change of the filter frequency a short signal distortion is generated. This leads to wrong signal at the output within the step response time of the chosen filter. Therefore in SPI mode the ND or GS flag is activated after the change of the filter frequency to mark the invalid sensor data.

In PSI the time between changing the filter and sending acceleration data is longer than the step response. Therefore no invalid data can be transmitted. (Valid for 215Hz/ 430hz/ 860Hz filter; 53Hz filter not released for PSI applications).

2052

All specified values in this chapter are valid for the combination of decimation and low pass filter

369

Filter characteristics is comparable to an 3rd order bessel filter or better

2062

The filter has a frequency-independent, constant group delay .

2861

The phase is linear below 860Hz.

2064



There is no clipping of the data before low pass filtering. This is valid for all gain factors, which can be applied.

Filter frequency is programmable to 860Hz, 430Hz, 215Hz and 53Hz

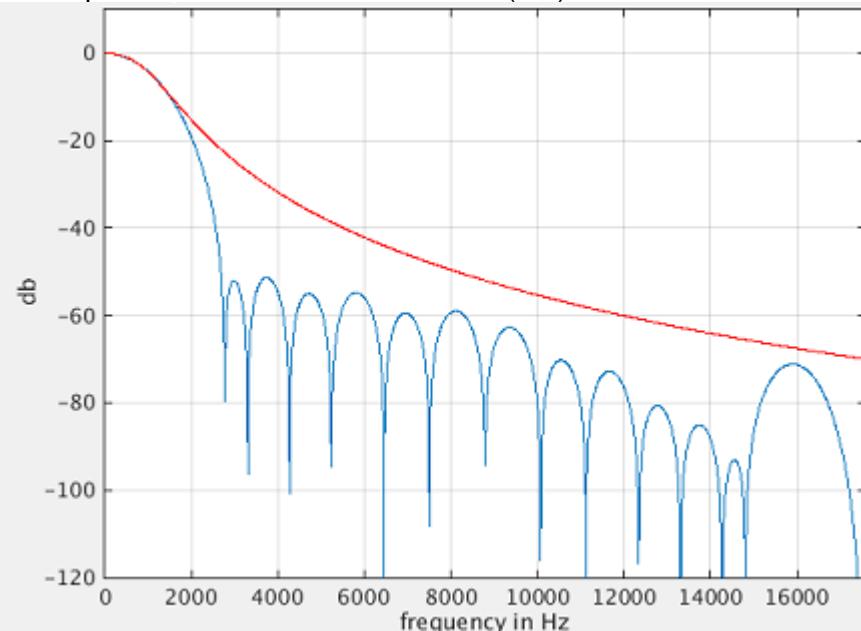
For SPI types SMA760 and SMA720 it is allowed to choose between the 430Hz, 215Hz and 53Hz mode.

For SPI type SMA765 it is allowed to choose between the 860Hz, 430Hz and 215Hz mode.

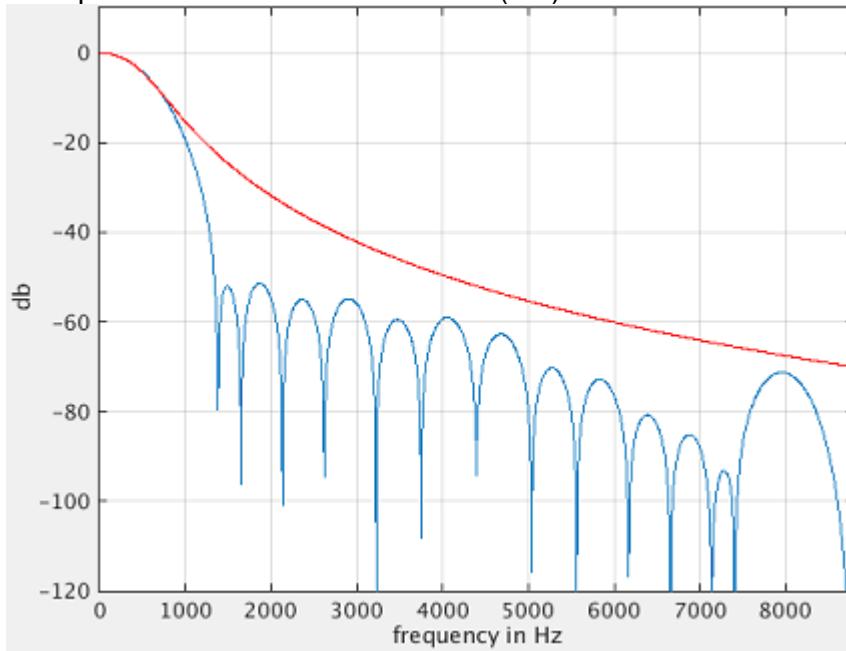
For the SMA773/774 it is only allowed to choose between 430Hz and 215Hz mode. For all other PSI5 types it is allowed to choose between the 860Hz, 430Hz and 215Hz mode.

#### Filter characteristics of the FIR filter:

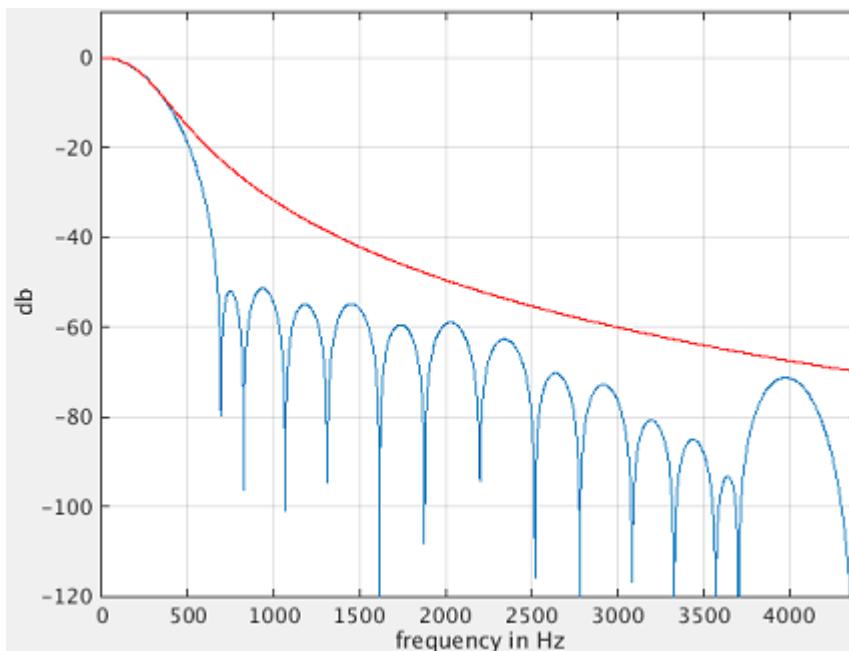
860Hz filter (blue) in comparison to 3rd order bessel filter (red):



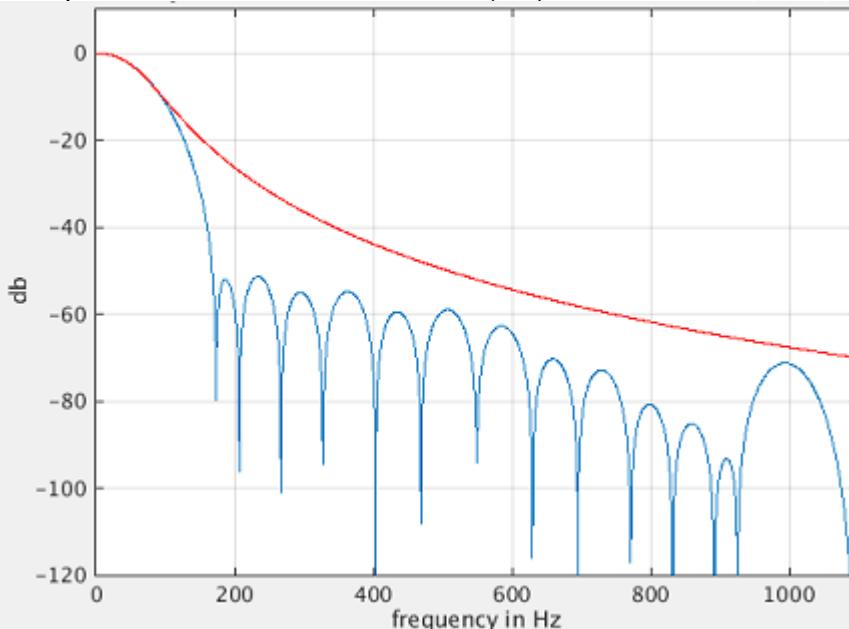
430Hz filter (blue) in comparison to 3rd order bessel filter (red):



215Hz filter (blue) in comparison to 3rd order bessel filter (red):



4401 53Hz filter (blue) in comparison to 3rd order bessel filter (red):



ID	parameter / condition	min	typ	max	unit
2133	Gain of the FIR filter all filter settings		1.2324		
2053	Nominal 3dB corner frequency 860 Hz Mode		860		Hz
2054	Nominal 3dB corner frequency 430 Hz Mode		430		Hz
2056	Nominal 3dB corner frequency 215 Hz Mode		215		Hz
2055	Nominal 3dB corner frequency 53 Hz Mode		53		Hz

2057

The tolerance of Cut-Off / 3db corner Frequency is identical to the tolerance of the oscillator.



ID	parameter / condition	min	typ	max	unit
4849	Stop band Attenuation 860Hz Filter Mode; incl. MEMS and Oscillator tolerance; 3kHz<f<7kHz	-50			dB
4851	Stop band Attenuation 860Hz Filter Mode; incl. MEMS and Oscillator tolerance; f>=7kHz	-58			dB
380	Stop Band Attenuation 430Hz Filter Mode; incl. MEMS and Oscillator tolerance; 1.5kHz<f<3.5kHz	-50			dB
381	Stop Band Attenuation 430Hz Filter Mode; incl. MEMS and Oscillator tolerance; f>=3.5kHz	-58			dB
382	Stop Band Attenuation 215Hz Filter Mode; incl. MEMS and Oscillator tolerance; 1.5kHz<f<3.5kHz	-50			dB
383	Stop Band Attenuation 215Hz Filter Mode; incl. MEMS and Oscillator tolerance; f>=3.5kHz	-60			dB
4403	Stop band Attenuation 53 Hz Filter Mode; incl. MEMS and Oscillator tolerance; 0.75kHz<f<1.75kHz	-50			dB
4405	Stop band Attenuation 53 Hz Filter Mode; incl. MEMS and Oscillator tolerance; f>1.75kHz	-60			dB

## 2.1.5 Gain and Sensitivity calibration

2134

After low pass filtering a coarse gain and a fine gain (sensitivity calibration) is applied.

2135

The fine gain can be adjusted in 256 steps by setting the gainword of the channel in OTP. It is calculated by:

$$\left( \frac{[gainword]}{b_{gain}} + a_{gain} \right) \cdot c_{gain}$$

ID	parameter / condition	min	typ	max	unit
3837	$a_{gain}$ (Constant adder for fine gain calculation)x		0.25		
3838	$b_{gain}$ (Constant factor for fine gain calculation)		512		
2190	$c_{gain}$ Additional constant multiplier of gain (to center fine gain range)		1		
411	Fine gain range	0.25		0.748	
3740	Range of gainword	0		255	

2140

The following coarse gain factors can be chosen by setting the OTP bits for [CMA\_type] and [SMA\_range]:

(green marked settings are used within the current SMA7 variants, grey marked are not released)



		CMA_type		
		120g	480g	800g
SMA_range		00	01	10
30g	011	Coarse Gain x4	not valid	not valid
60g	100	Coarse Gain x2	Coarse Gain x8	not valid
120g	000	Coarse Gain x1	Coarse Gain x4	Coarse Gain x8
240g	001	not valid	Coarse Gain x2	Coarse Gain x4
480g	010	not valid	Coarse Gain x1	Coarse Gain x2

## 2.1.6 Offset Cancellation

4415

The SMA7 includes a static and a fast and slow offset cancellation. The static offset cancellation corrects the signal by a constant value, which is programmed for each individual part during final test trimming. The fast offset cancellation (FOC) cancels the actual offset, when triggered. The slow offset cancellation (SOC) continuously cancels the actual offset with a fixed compensation rate.

ID	parameter / condition	min	typ	max	unit
397	Offset Cancelation Range (register width) FOC/SOC	-255		255	g
5457	Offset cancellation range SMA760/773/ 720-X/774-X CMA581R CMA582R-X	-45		45	g
5460	Offset cancellation range SMA720-Z/774-Z CMA582R-Z	-30		20	g
5458	Offset cancellation range SMA752/765/750/758/782/780 SMA753/783 -X CMA584R CMA585R-X	-85		85	g
5461	Offset cancellation range SMA753/783/751/781 -Z CMA585R-Z	-88		88	g
5459	Offset cancellation range SMA757/755/792/790 CMA588R	-120		120	g
399	Offset Cancelation Headroom Safety margin for system level (e.g. orientation; driving dynamics;...)	10			g

386

For FOC and SOC max. Range can be limited. The limit is stored in OTP as 8Bit MSB value with 1LSB/g.

4436

The limit is programmed during final test of the SMA. It is chosen in a way, that the sensor fulfills all spec parameters, as long as the offset (incl. the 10g headroom) is within this limits.

395

In case of exceeding the control range during SPI-operation in fast or slow offset compensation mode, the sensor sends a 'Sensor Defect' message. (offset cancellation error).

396

In case of exceeding the control range during SPI operation in fast or slow offset compensation mode, the sensor sends a failure flag. ("offset cancellation error channel1" or "offset cancellation error channel2").

4421

The FOC decreases the offset in steps, which can be calculated by dividing the initial Offset by the number of FOC samples. The sensor checks after each step, if the control range is exceeded. Therefore the FOC stops latest when reaching the control range plus one FOC step (initial offset/samples).

2067

If the Range bit in OTP is set to "0", no error occurs in case of overflow.



4031

After the offset regulator, the data is right shifted by 3 bits for the SPI mode and 7 bits for 10 bit PSI mode.

### 2.1.6.1 Static offset cancellation

2139

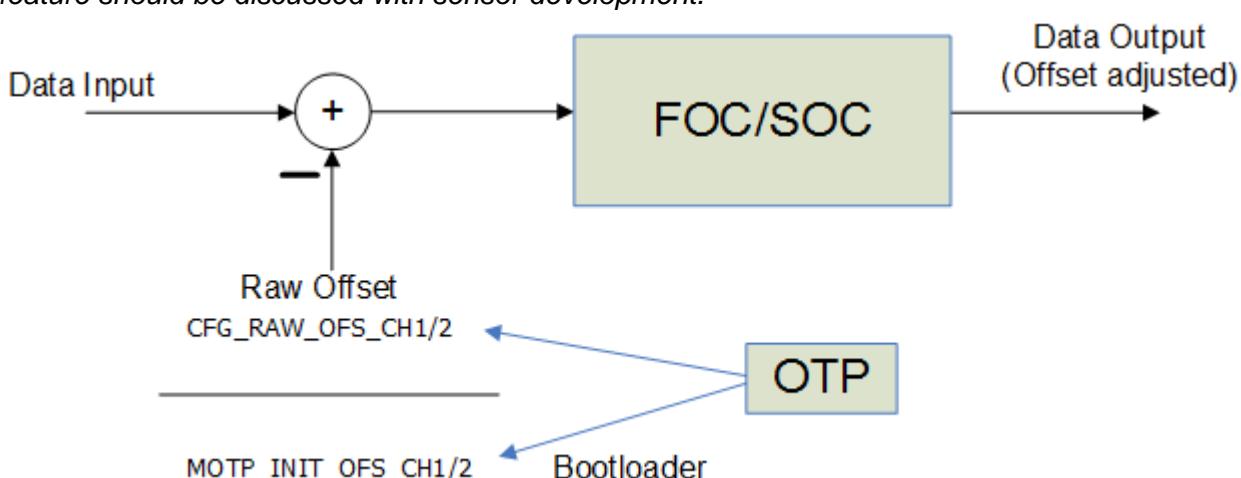
The raw offset values are stored in the OTP during final test with 32 LSB/g in the register MOTP\_INIT\_OFS\_CH1/2. The ASIC converts the stored values depending on the selected range (combination of PSI/SPI-mode, CMA\_type and SMA\_range).

2069

After power on of the sensor the rawoffset values from OTP are copied automatically in the MOTP and the register CFG\_RAW\_OFS\_CH1/2. The output signal is correct by the value in CFG\_RAW\_OFS\_CH1/2. There is no external trigger needed to start the static offset correction. But the value in CFG\_RAW\_OFS\_CH1/2 can be overwritten by PSI BiDir or SPI command (before EOP). This will change the correction value for the static offset cancelation.

*Remark: It is not recommended to change the value in CFG\_RAW\_OFS\_CH1/2. Use cases, which need this feature should be discussed with sensor development.*

4416



2070

If no fast or slow offset correction is triggered, the signal is permanently corrected by these values.

2071

If fast or slow offset correction is triggered no offset jump occurs. The dynamic offset cancellation starts from the already corrected output value.

### 2.1.6.2 Fast offset cancellation

385

Fast offset cancellation is implemented as averaging algorithm of a defined number of samples.

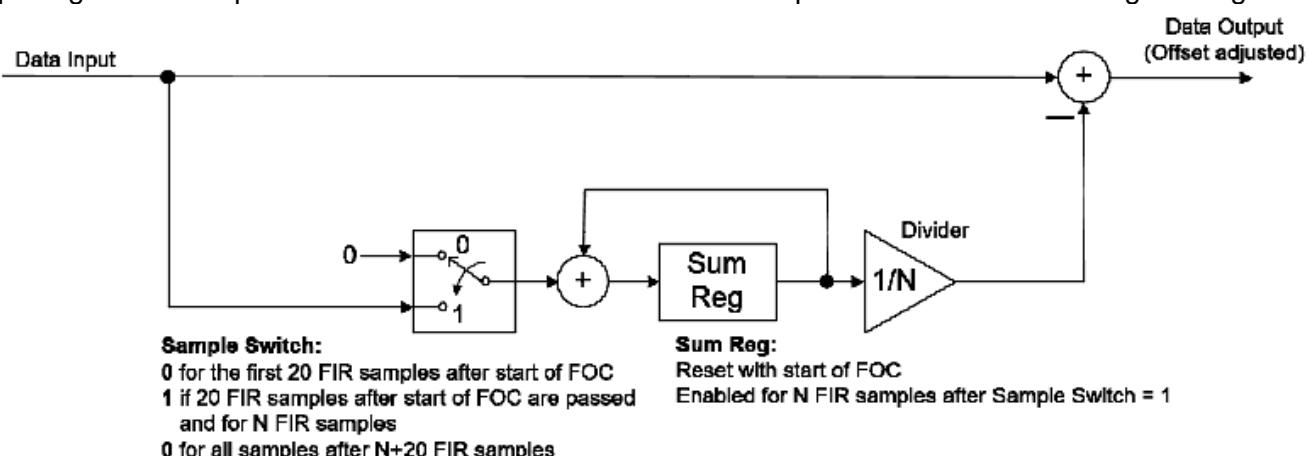
388

This is realized by calculating the mean value and subtracting it from the raw data.

5170

In detail this is shown in the block diagram below: The input acceleration signal is divided by the number of samples (N). This value is summed up for N cycles. The resulting average value is subtracted from input signal. This implementation leads to a "staircase" like ramp down of the offset during running FOC.

4417





3743 The first 20 samples are ignored, before starting the FOC. This assures, that all filters are settled and avoids unstable offset values after reset. (Assuming constant acceleration at input, to allow settling of the filters).

3744 Averaging of 64, 128, 256, 512 and 1024 samples can be selected in SPI-Mode. But only the following combinations are released for SMA720/SMA760:

**430Hz filter:** 512 and 1024 samples

**53Hz filter:** 64 and 128 samples

If other filter settings are needed, the FOC should be done with 430Hz filter and the filter frequency should be changed after FOC.

2072 In SPI mode the fast offset cancellation can be triggered by an SPI command before EOP.

4418 In PSI mode the FOC is triggered automatically during Initphase 1, if MOTP\_OFS\_FOC\_DISABLE is set to zero. It is always executed with 512 samples and a low pass filter setting of 430Hz.

2076 The offset cancellation is symmetrical to zero

ID	parameter / condition	min	typ	max	unit
400	FOC duration Peripheral-Types (430Hz, 512 samples)		60.0	62.8	ms
2075	FOC duration SPI-Types, 53Hz Filter, 64 samples		75.7	79.3	ms
3962	FOC duration SPI-Types, 53Hz Filter, 128 samples		133.5	139.6	ms
3964	FOC duration SPI-Types, 430Hz Filter, 512 samples		60.0	62.8	ms
3963	FOC duration SPI-Types, 430Hz Filter, 1024 samples		117.7	123.1	ms

3966 The FOC duration for other filter settings scales linear (e.g. for 215Hz filter the values are multiplied by 2, for 860Hz they are multiplied by 0.5).

3967 The formula is: (number\_of\_FOC\_samples + 20) \* sample\_time

### 2.1.6.3 Slow offset cancellation

2864 A slow offset cancellation is implemented.

2078 If activated, the slow offset cancellation continuously corrects the raw offset from the sensor element.

2081 It can be switched on and off via SPI commands. No failure flag is set after EOP if SOC is not started.

3829 Running the sensor without slow offset cancellation after EOP is possible. In Bosch SPI the status of the slow offset cancellation can be checked by reading monitor I data.

2082 In SPI mode the speed of the SOC can be selected before EOP between the two settings "SOC" and "XSOC" (extra slow offset cancellation).

2080 In PSI mode the SOC is started before end of init phase 3. To avoid unintended offsets directly after start-up, the SOC runs the first seconds with an increased speed setting ("MSOC", medium-slow offset cancellation). After the MSOC period expired, it is changed to the normal SOC speed.

When sampling data in BiDir using the 8.8 kHz Mode the following applies: If

MOTP\_OFS\_MSOC\_DISABLE=0, MSOC is started when entering 8.8 kHz Mode. It is not stopped by leaving 8.8 kHz mode, hence it runs as long as defined by MOTP\_MSOC\_DURATION.

If MOTP\_OFS\_MSOC\_DISABLE=1 is set prior to enabling 8.8kHz mode, MSOC is not executed. SOC is not active during 8.8kHz mode in neither of the two cases.

5089 There is no change in the output signal due to the change from MSOC to SOC speed.

393 Execution of SOC and MSOC in PSI mode can be deactivated independently by setting MOTP\_OFS\_SOC\_DISABLE and MOTP\_OFS\_MSOC\_DISABLE to one. If only MSOC is disabled, the sensor starts directly with SOC speed in Init 3.

2079 The SOC is symmetrical to zero.

2083 The Slow offset cancellation is realized by a common counter system.

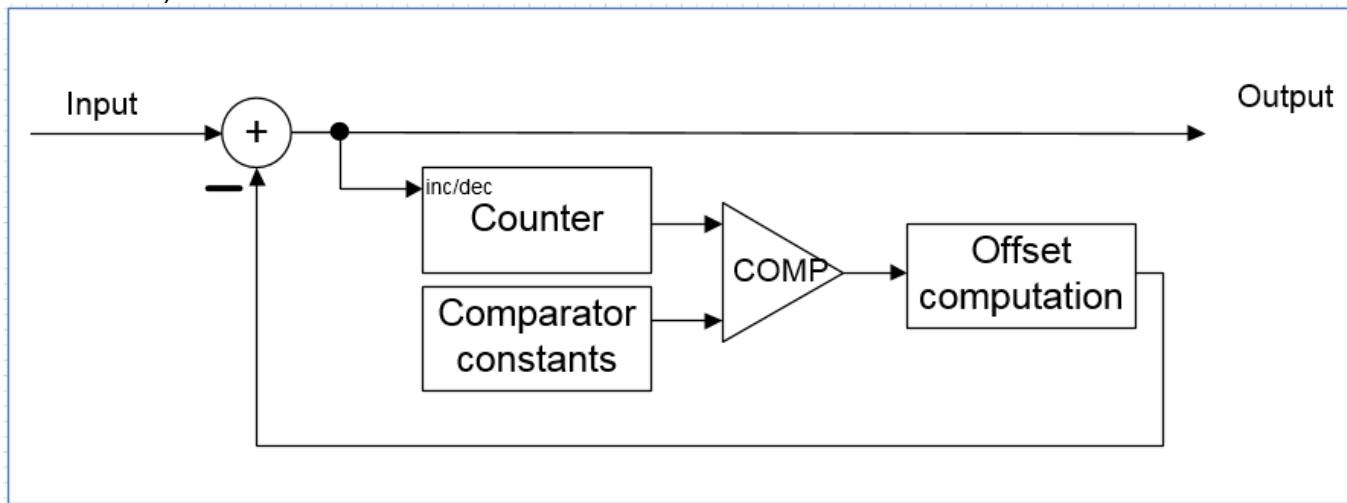


For each calculation cycle the output signal is calculated by subtraction of the current offset compensation value from the current input value.

For each calculation cycle the output signal is analyzed and depending on the result, the offset value (accumulated) is changed:

If the output signal is greater/less than zero, a counter is incremented/ decremented (see ASIC DS for more details).

4419



4420

Important: When slow offset cancellation is triggered via CFG\_OFFSET\_CONFIG, the content of CFG\_OC\_LENGTH must remain the same as that used for fast offset cancellation. In case CFG\_OC\_LENGTH bits are changed, the FOC must be retriggered

ID	parameter / condition	min	typ	max	unit
2131	Resolution of the SOC 14bit			0.5	LSB
5093	MSOC speed Peripheral-Types; referenced to 10bit PSI5		2		LSB/s
5095	MSOC speed Peripheral-Types; 16bit PSI5; SMA_range=120g		32		LSB/s
5096	Duration of MSOC period (afterwards the normal SOC speed will be applied) MOTP_MSOC_DURATION=1	7	7.5	7.8	s
403	SOC speed Peripheral-Types; referenced to 10bit PSI5		0.25		LSB/s
404	SOC speed Peripheral-Types; 16bit PSI5; SMA_range=120g		4		LSB/s
407	SOC speed ECU-Types; referenced to 14bit SPI		4		LSB/s
409	XSOC speed  Note: XSOC is not operational if filter frequency 53Hz is enabled. ECU-Types; referenced to 14bit SPI mode 2, mode 3; filter frequency 860Hz, 430Hz, 215Hz		0.2		LSB/s

2130

The tolerance of the SOC speed is identical to the oscillator tolerance

5298

For PSI 16bit modes the (M)SOC speed scales with the SMA\_range setting. E.g. the speed for 240g range is 2 times higher and for 480g range 4 times higher then in 120g range.



## 2.1.7 Linear interpolation

The sensor provides a linear interpolation of filter values. This interpolation scheme is utilized for SPI and all PSI Communication modes that trigger data transmission on an external Sync Pulse, namely all PSI modes except the asynchronous modes.

The interpolation can be disabled by PSI5 Bidir.

Remark: In PSI, the disabling is only effective when sampling via BiDir commands, it is not effective when sampling in run mode.

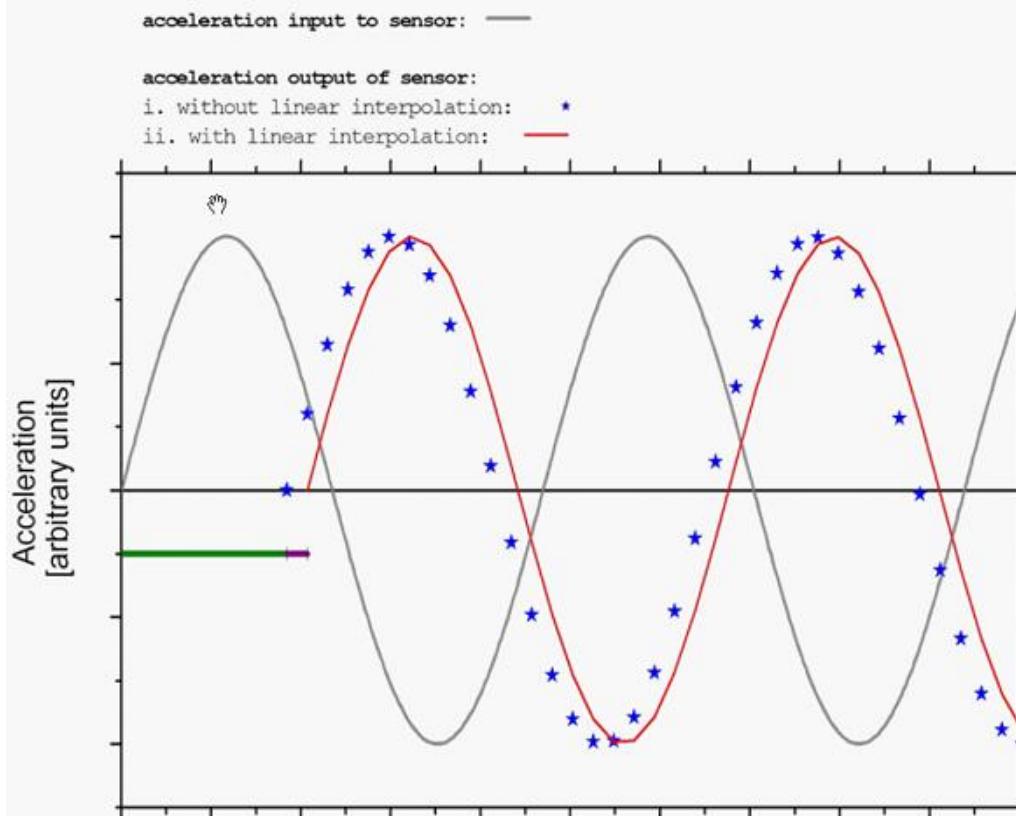
With activated linear interpolation, each transmitted sensor value to the ECU is interpolated between the two most recent sensor values that have been generated by the filter, adding an additional latency of one filter update period to the filter path.

The interpolation is performed with the resolution of the offset cancellation output.

After interpolation the sensor data outputs are adjusted depending on SPI/PSI modes by application of clipping, shifting and rounding operations.

ID	parameter / condition	min	typ	max	unit
419	Interpolation Steps all filter modes except 860Hz	252		252	step
4033	Interpolation Steps 860Hz filter	126		126	step
418	Update Rate of LIN output all modes; 860Hz and 430Hz filter		2.24		MHz
4035	Update Rate of LIN output all modes; 215Hz filter		1.12		MHz
4034	Update Rate of LIN output all modes; 53Hz filter		279		kHz

The tolerance of the update rate is given by the oscillator tolerance.





## 2.1.8 Inversion

- 2146 For PSI variants the output signal for each channel can be inverted by setting [MOTP\_SIGN\_CH1/2] in the OTP.  
 4423 For SPI variants the sign bit is already set during final test.

## 2.1.9 Interfaces

- 2153 The following chapters describe how the final sensor data for the SPI and the different PSI modi is generated. Further details about the interfaces can be found in the dedicated SPI and PSI chapters.  
 3872 The below sampling rate of the interface describes, at which frequencies the output register is updated with new values from the signal path. (Not taking into account additional values from interpolator)

ID	parameter / condition	min	typ	max	unit
3870	Sampling Rate @ SPI/PSI-Interface; 860Hz Mode	17.8			kHz
2189	Sampling Rate @ SPI/PSI-Interface; 430Hz Mode	8.9			kHz
3869	Sampling Rate @ SPI/PSI-Interface; 215Hz Mode	4.45			kHz
3871	Sampling Rate @ SPI/PSI-Interface; 53Hz Mode	1.11			kHz

### 2.1.9.1 SPI 14 bit

- 2155 The output data for SPI interface is clipped to 14bit (+8191/-8191 LSB).  
 3873 Overview of the sensitivity at SPI output. Green marked modes are used by the currently specified SMA types:

SPI 14Bit		CMA_type		
SMA_range		120g	480g	800g
30g	011	Coarse Gain x4 256 LSB/g	not valid	not valid
60g	100	Coarse Gain x2 128 LSB/g	Coarse Gain x8 128 LSB/g	not valid
120g	000	Coarse Gain x1 64 LSB/g	Coarse Gain x4 64 LSB/g	Coarse Gain x8 64 LSB/g
240g	001	not valid	Coarse Gain x2 32 LSB/g	Coarse Gain x4 32 LSB/g
480g	010	not valid	Coarse Gain x1 16 LSB/g	Coarse Gain x2 16 LSB/g

- 2194 The physical resolution at the interface is 1 LSB. This means, if the dC/C value at the S/D input is changed, the output changes in steps of 1 LSB.



### 2.1.9.2 PSI 10bit

2158

The 10bit PSI signal is generated by removing the last 4 bits of the 14bit signal and clipping the signal to +/-480LSB. A symmetric rounding is applied.

3907

Referring to the output of the offset regulator a shift of 7 bit is applied:

OFS (20 Bit)	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sensor Data PSI (10 Bit), SMA=480g		x	x	x	x	x	x	x	x	x	16	15	14	13	12	11	10	9	8	7
Sensor Data PSI (10 Bit), SMA=240g		x	x	x	x	x	x	x	x	x	16	15	14	13	12	11	10	9	8	7
Sensor Data PSI (10 Bit), SMA=120g		x	x	x	x	x	x	x	x	x	16	15	14	13	12	11	10	9	8	7
Sensor Data PSI (10 Bit), SMA=60g		x	x	x	x	x	x	x	x	x	16	15	14	13	12	11	10	9	8	7
Sensor Data PSI (10 Bit), SMA=30g		x	x	x	x	x	x	x	x	x	16	15	14	13	12	11	10	9	8	7

PSI frame 10 bit

9 8 7 6 5 4 3 2 1 0

3874

Overview of the sensitivity at 10bit PSI output. Green marked modes are used by the currently specified SMA types:

PSI 10Bit		CMA_type	120g	480g	800g
SMA_range					
30g	011	Coarse Gain x4 16 LSB/g	invalid send error message	invalid send error message	invalid send error message
	100	Coarse Gain x2 8 LSB/g	Coarse Gain x8 8 LSB/g	invalid send error message	invalid send error message
60g	000	Coarse Gain x1 4 LSB/g	Coarse Gain x4 4 LSB/g	Coarse Gain x8 4 LSB/g	Coarse Gain x8 4 LSB/g
	001	invalid send error message	Coarse Gain x2 2 LSB/g	Coarse Gain x4 2 LSB/g	Coarse Gain x4 2 LSB/g
120g	010	invalid send error message	Coarse Gain x1 1 LSB/g	Coarse Gain x2 1 LSB/g	Coarse Gain x2 1 LSB/g
	240g	invalid send error message	Coarse Gain x1 1 LSB/g	Coarse Gain x2 1 LSB/g	Coarse Gain x2 1 LSB/g
480g	010	invalid send error message	Coarse Gain x1 1 LSB/g	Coarse Gain x2 1 LSB/g	Coarse Gain x2 1 LSB/g

2195

The physical resolution at the interface is 1 LSB. This means, if the dC/C value at the S/D input is changed, the output changes in steps of 1 LSB.

### 2.1.9.3 PSI 14+2 bit

2161

This mode uses 14bit sensor data, but sends 16bit dataframes. The missing 2bit are filled with reasonable data. Details depend on the chosen [SMA\_range] setting in OTP.

2162

First the signal from the interpolator is clipped to +/-7680LSB.

2163

Afterwards the 14 bit data is embedded in the 16bit PSI frame depending on the [SMA\_range] according to the following table. All bits left of the defined MSB are added to fill up the 16bit frame (marked purple).



Signalpath																			
Output at PSI interface																			
SMA_range																			
480g	MSB = Bit no. 16	x	x	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
240g	MSB = Bit no. 15	x	x	14	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
120g	MSB = Bit no. 14	x	x	14	14	14	13	12	11	10	9	8	7	6	5	4	3	2	
60g	MSB = Bit no. 13	x	x	14	14	14	14	13	12	11	10	9	8	7	6	5	4	3	
30g	MSB = Bit no. 12	x	x	14	14	14	14	14	13	12	11	10	9	8	7	6	5	4	
PSI frame				16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

4424

The used 14 bits refer to the bits [16:3] of the offset regulator output.

2164

Missing bits on the right side (LSB) are filled with "0".

2165

Missing bits on the left side (MSB) are filled with the MSB of the 14bit sensor data.

2166

If bits from the sensor signal are discarded (30g/60g range), symmetrical rounding is applied.

2167

This leads to a constant sensitivity of 64 LSB/g at PSI output, independent of the chosen SMA\_range.

3875

Overview of the possible Gain factors and modes. Green marked modes are used by the currently specified SMA types:

PSI		CMA_type		
16Bit		120g	480g	800g
SMA_range	011	Coarse Gain x4 64LSB/g MSB = Bit no. 12	invalid send error message	invalid send error message
30g	100	Coarse Gain x2 64LSB/g MSB = Bit no. 13	Coarse Gain x8 64LSB/g MSB = Bit no. 13	invalid send error message
60g	000	Coarse Gain x1 64LSB/g MSB = Bit no. 14	Coarse Gain x4 64LSB/g MSB = Bit no. 14	Coarse Gain x8 64LSB/g MSB = Bit no. 14
120g	001	invalid send error message	Coarse Gain x2 64LSB/g MSB = Bit no. 15	Coarse Gain x4 64LSB/g MSB = Bit no. 15
240g	010	invalid send error message	Coarse Gain x1 64LSB/g MSB = Bit no. 16	Coarse Gain x2 64LSB/g MSB = Bit no. 16
480g				

## 2.2 $\mu$ -Cut feature

429

For PSI5 sensors a short open of the supply voltage shall not lead to a reset ( $\mu$ -Cut rejection feature).

430

$\mu$ -Cut: In the case of  $\mu$ -Cuts the Vss drops abruptly and  $I_s=0$  for a short time.

431

$\mu$ -Cuts within the specified limits ( $t_{\mu\text{Cut\_min}}$ ) do not lead to a malfunction or degraded performance of the sensor.

3840

Micro-cuts within the specified limits ( $t_{\mu\text{Cut\_min}}$ ) do not lead to a reset of the sensor.

433

Any data sent after a  $\mu$ Cut is fully in specification.

3839

During micro-cuts within the specified limits ( $t_{\mu\text{Cut\_min}}$ ) the internal processing must not be stopped or interrupted.

432



During a  $\mu$ -Cut within the specified limits ( $t_{\mu\text{Cut\_min}}$ ) the current interface may be switched off when the supply voltage is below ( $V_{dd\_min}$ ). This may lead to a loss of only one impacted message. In case of two channel sensors, the message of both channels can be impacted, if they are send in adjacent timeslots. No further messages are affected.

ID	parameter / condition	min	typ	max	unit
434	$\mu$ -Cut detection voltage (voltage at which the current interface may be switched off)  PSI5-Sensors			4.5	V
435	Minimum $\mu$ -Cut duration without Reset  PSI5-Sensors (SO8); $C_{VDDI} > 720\text{nF}$ ; including influences of supply voltage/regulator capacitor tolerance/temperature/...	33			$\mu\text{s}$
436	Minimum $\mu$ -Cut Duration without Reset  PSI5-Sensors (LGA or SO8) with $C_{VDDI} > 330\text{nF}$ ; including influences of supply voltage/regulator capacitor tolerance/temperature/...	15			$\mu\text{s}$
3980	Minimum $\mu$ -Cut duration without Reset  PSI5-Sensors (SO8); including influences of supply voltage/regulator capacitor tolerance/temperature/...; $C_{VDDI} > 220\text{nF}$	10			$\mu\text{s}$
437	Reentrance time after $\mu$ -Cut  Time after $\mu$ -Cut until PSI5 interface is reactivated			1	$\mu\text{s}$
438	Reentrance time after $\mu$ -Cut  Time after $\mu$ -Cut until quiescent current is stable (+/-2mA) and sensor work within specification			200	$\mu\text{s}$
4067	Reentrance time after $\mu$ -Cut  LGA types or $C_{VDDI} < 520\text{nF}$ ; Time after $\mu$ -Cut until quiescent current is stable (+/-0.5mA) and sensor work within specification			120	$\mu\text{s}$

439

Test method for  $\mu$ -Cut feature:  
every 1 ms for 4s without any reset of the sensor.

## 2.3 Oscillator jitter

4907

The oscillator jitter function is doing small variations of the oscillator frequency. This increases the EMC robustness. The max. variation and the repetition rate (modulation frequency) can be adjusted in final test via OTP. The step height of the variation is constant.

4908

The jitter functionality can be activated / deactivated by an OTP bit (MOTP\_JITTER\_OFF = 0/1 respectively).

4909

The nominal delta fosc variation can be adjusted in OTP (MOTP\_OSC\_MOD).

MOTP\_OSC\_MOD=0: +/- 0.295 oscillator frequency variation

MOTP\_OSC\_MOD=1: +/- 0.572 oscillator frequency variation

This value describes the jitter amplitude in percent.



4910

frequency of modulation is defined in OTP (MOTP\_OSC\_MOD\_FREQ)

MOTP\_OSC\_MOD\_FREQ=2'b00: 3.992 kHz

MOTP\_OSC\_MOD\_FREQ=2'b01: 3.493 kHz

MOTP\_OSC\_MOD\_FREQ=2'b10: 1.996 kHz

MOTP\_OSC\_MOD\_FREQ=2'b11: 0.991 kHz

This value describes, after which period a full variation of the oscillator frequency by OSC\_MOD is finished and a new cycle will be started.

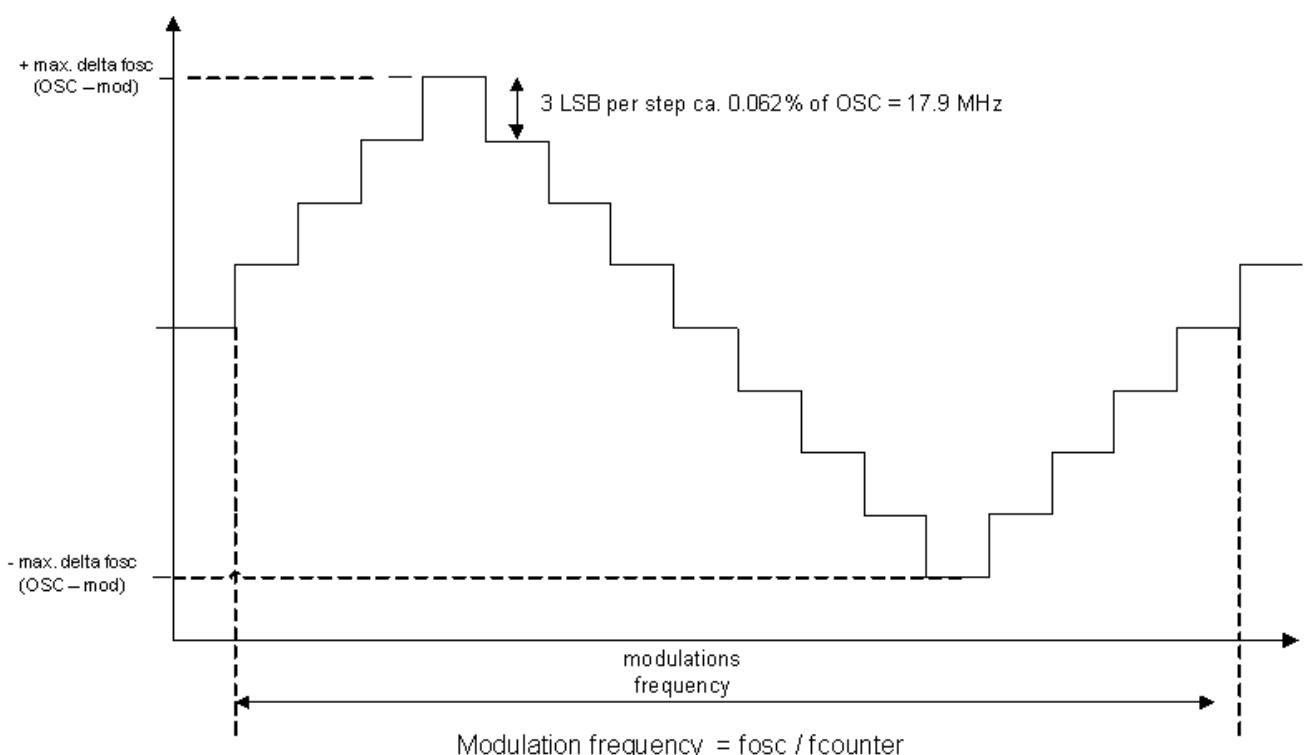
5171

For SMA7 the jitter is always activated and configured to MOTP\_OSC\_MOD=0 and MOTP\_OSC\_MOD\_FREQ=2'b10.

(Remark: Setting MOTP\_OSC\_MOD would lead to violation of ID3070 and is therefore not allowed).

4911

The figure below shows the schematic behaviour of the oscillator frequency over time with activated jitter. Max. delta fosc is set by MOTP\_OSC\_MOD. The modulation frequency is set by MOTP\_OSC\_MOD\_FREQ.





### 3. OTP and Programming

4114 OTP (One Time Programmable memory) is electrically programmable and UV erasable.  
 A memory cell represents Bit=0 if erased. By applying programming voltage the memory cell gets charged and then permanently represents Bit=1.

4115 The OTP is divided into 5 banks.

Scratch Area (0x00 - 0x0F): Carries lock bits and scratch activation code. Used to keep track of production/testing progress.

ASIC (0x10 - 0x1F): Programmed during ASIC wafer level testing.

SMA (0x20 - 0x37): Programmed during final testing.

PAS (0x38 - 0x47): Customer calibration

ECC (0x48 - 0x59): ECC storage area

Each of the ASIC/SMA/PAS bank is secured by its own 8-Bit CRC and lock bit. When the lock bit is set, the CRC check over the bank will be activated after bootloading and the register content will be monitored continuously by the CRC (see also chapter OTP CRC Handling).

*Note: OTP memory is not directly mapped into the XA760 address space. All relevant OTP data is transferred into the CONFIG\_REGS registers (MOTP registers) by the bootloader before normal operation starts.*

ID	parameter / condition	min	typ	max	unit
2026	The scratch area contains bits that are used in final test. These bits are not visible in MOTP and are not included in CRC calculation. They have no function in the ASIC.		6		Bit

496 OTP programming and testing is possible with SPI and PSI5-BiDir communication.

3721 In PSI5-BiDir only VDD, IDATA and GND Pin are needed for programming. VDD and IDATA are shorted.

497 Therefore it is possible to program all peripheral-application-specific parameters of SMA7 using bidirectional communication via the GND/VSS two-wire interface.

5053 There are basically two different ways to access the OTP of SMA7:

- OTP access executed by bootloader operation. These operations are controlled by the registers described below. This is the standard method for OTP access.
- Direct OTP access via OTP wrapper. This function is only intended for use in dedicated tests and is not further described in this document.

A more detailed description of the OTP programming can be found in the dedicated XA760 OTP programming guide.

#### 3.1 OTP control registers

##### 3.1.1 Register **BOOTLOADER\_ADDRESS (0x80)**

4469 The register contains the following fields:

**BL\_SADDR[4:0]** Start block address for bootloading read/program access

Absolute OTP block start address for bootloading or programming transactions triggered by bits *BL\_START\_READ* or *BL\_START\_PROG* in register *BOOTLOADER\_CONTROL*.

The range *BL\_SADDR* to *BL\_EADDR* defines the applied address range of the bootloading or programming transaction.

**BL\_EADDR[12:8]** End block address for bootloading read/program access

Absolute OTP block end address for bootloading or programming transactions triggered by bits *BL\_START\_READ* or *BL\_START\_PROG* in register *BOOTLOADER\_CONTROL*.



Note that this register is only accessible in EXTENDED MODE or EXTENDED TEST MODE.

### 3.1.2 Register **BOOTLOADER\_CONTROL (0x82)**

4467

The register contains the following fields:

**BL\_START\_PROG [0]** Start Bootloader controlled OTP programming if set.

Writing to this bit will trigger a Bootloader controlled OTP programming transaction. The source of the programming values are the MOTP shadow register area corresponding to the dedicated OTP block addresses *BL\_SADDR* to *BL\_EADDR* and the destination corresponds to an OTP area of the same block address range. The address relationship between block addresses and APB register addresses are given by the OTP content table. Note that this bit is self-resetting and will always read zero. Due to some register gaps in the MOTP area the corresponding OTP areas will always programmed with zero.

**BL\_START\_READ [1]** Start Bootloader controlled OTP transfer into shadow registers if set.

Writing to this bit will trigger a Bootloader controlled OTP read transaction. The source of the programming values is the OTP memory area defined by *BL\_SADDR* to *BL\_EADDR* and the destination corresponds the MOTP shadow register area. The address relationship between block addresses and APB register addresses are given by the OTP content table. Note this bit is self-resetting and will always read zero. Due to some register gaps in the MOTP area the corresponding OTP values read will have no effect.

**BL\_MOTP\_CALC\_CRC [2]** Recalculate MOTP CRC if set.

Writing to this bit will trigger a Bootloader controlled update of the reference CRC values of all three MOTP regions based on the current MOTP contents. As a result a previously occurred CRC error will not appear any more. Reading this bit shows the activity state of the CRC calculation process: 0: CRC calculation done; 1: CRC recalculation busy

**BL\_PROG\_BYTE [3]** Selects if the OTP block or the single byte programming mode shall be used:

0:(Standard) Block wise OTP programming. Programs complete OTP blocks inclusive ECC.

Programming source is the MOTP shadow register area corresponding to the dedicated OTP block addresses *BL\_SADDR* to *BL\_EADDR* and the destination corresponds to the OTP area of the corresponding block address range. The address relationship between block addresses and APB register addresses are given by the OTP content table, see chapter 11.1.8.

1: Single byte OTP programming (*for test purpose only. Not released for customer use!*). Programs a single byte without ECC. The OTP byte address is specified by the OTP block address (otp\_block\_address.block\_addr) and the byte offset

(BOOTLOADER\_CONTROL.BL\_PROG\_BYTE\_ADDR). The OTP byte address is calculated according to the following formula:

OTP\_address = otp\_block\_address.block\_addr \* 4 +  
BOOTLOADER\_CONTROL.BL\_PROG\_BYTE\_ADDR

**BL\_PROG\_BYTE\_ADDR [5:4]** Selects the byte position for the single byte programming mode:

Defines the byte position within a single OTP block:

0: byte 0; corresponds to user\_data0.user\_data0(7:0)

1: byte 1; corresponds to user\_data0.user\_data0(15:8)

2: byte 2; corresponds to user\_data1.user\_data1(7:0)

3: byte 3; corresponds to user\_data1.user\_data1(15:8)

This field is don't care if the single byte programming mode is disabled.

**BL\_IGNORE\_REGIONS[10:8]** Resets corresponding effective lockbit if set.

Each bit clears an effective lockbit corresponding to a certain MOTP region. The lockbit to region correspondence is as follows:

**BL\_IGNORE\_REGIONS[8]:** MOTP ASIC region lockbit

**BL\_IGNORE\_REGIONS[9]:** MOTP SMA region lockbit

**BL\_IGNORE\_REGIONS[10]:** MOTP PAS region lockbit

As a result an OTP programming transaction to one of these regions will never be blocked if the corresponding *BL\_IGNORE\_REGIONS* bit is set. Further a lockbit transferred from OTP memory will not lead to a locked MOTP region if the corresponding *BL\_IGNORE\_REGIONS* bit is set.



**BL\_BYPASS\_CALC\_CRC [11]** Bypass programming of calculated CRC if set.

If this bit is not set then internally calculated CRC values will be used during Bootloader controlled OTP programming for each region.

If this bit is set then the MOTP stored CRC values will be used during Bootloader controlled OTP programming for each region.

**OTP\_MASK\_CRC [12]** Masks OTP CRC failure status if set to 1.

**OTP\_VPROG\_ENA [13]** Enables the OTP programming voltage. (Only for test purpose. During bootloader controlled programming, the bootloader automatically enables VPROG.)

**BL\_PROG\_LOCKBITS [14]** Transfer of all lock bits from shadow register to OTP if set. OTP.

The enabling of this bit will enable a Bootloader controlled OTP programming transaction of all 3 lock bits from shadow register MOTP\_SCRATCH\_LOCK to OTP. The execution is only done if a bootloader programming is started with BL\_START\_PROG.

Note that the lock bits are transferred without ECC programming.

**BL\_PROG\_MODE [15]** OTP programming mode:

0: bit-serial programming

1: byte-mode programming

It is mandatory to use bit-serial programming ('0') to ensure a stable programming voltage.

Note that this register is only accessible in EXTENDED MODE or EXTENDED TEST MODE.

### 3.1.3 Register BOOTLOADER\_STATUS (0x84)

5059

**BL\_BUSY [0]** Status: ongoing bootloader transaction if '1'

**BL\_READ\_DONE [1]** Status: bootloader transfer from OTP to shadow registers done, if '1'

**MOTP\_CRC ASIC\_ERR [2]** CRC status of ASIC region, failure if bit is set

**MOTP\_CRC SMA\_ERR [3]** CRC status of SMA region, failure if bit is set

**MOTP\_CRC PAS\_ERR [4]** CRC status of PAS region, failure if bit is set

**PROGRAM\_ERR [5]**

Programming error if programming operation triggered:

- while otp is not enabled

- while otp is not in program mode

- while otp is programming

0: no error detected

1: error detected

The flag is reset to 0 before start of a bootloader programming cycle (BL\_START\_PROG=1).

**VPROG\_ERR [6]**

Programming undervoltage error detection status:

0: no error detected

1: error detected

The flag is reset to 0 before start of a bootloader programming cycle (BL\_START\_PROG=1).

### 3.1.4 Register MARGIN\_TEST\_CONFIG1 (0x86)

5060

**MARGIN\_START [0]** Start a margin test if '1'

**MARGIN\_MODE [1]** Margin flow selection

0: margin flow 0: general margin flow (enables Off State Margin and Margin-Level)

1: margin flow 1: margin threshold flow (enables iterative Margin-Level test)

**MARGIN\_TEST\_LOCKBITS [2] (0 = off; 1 = on)**; lockbit check requires that at least one of the configuration registers MARGIN\_TEST ASIC, MARGIN\_TEST SMA or MARGIN\_TEST PAS = 1

**MARGIN\_TEST ASIC [3]** Enable ASIC area (0 = off; 1 = on)

**MARGIN\_TEST SMA [4]** Enable SMA area (0 = off; 1 = on)

**MARGIN\_TEST PAS [6]** Enable PAS area (0 = off; 1 = on)

**MARGIN\_LEVEL\_SELECT [7:6]** Select margin level:

0,3: use MOTP\_MARGIN\_LEVEL\_PROG (flow 0 only)



- 1: use MOTP\_MARGIN\_LEVEL\_RETEST (flow 0 only)  
 2: use MARGIN\_TEST\_CONFIG2.MARGIN\_START\_LEVEL (flow 0 and flow 1)

### 3.1.5 Register MARGIN\_TEST\_CONFIG2 (0x88)

5061

**MARGIN\_START\_LEVEL** [6:0] Read margin test level selectable by MARGIN\_LEVEL\_SELECT.  
**MARGIN\_STEP\_SIZE** [11:8] Stepsize for iterative increase the read margin level in flow 1.  
 Range 1..15 (0 configures a stepsize of 16)

### 3.1.6 Register MARGIN\_TEST\_RESULT (0x8A)

5062

**MARGIN\_BUSY** [0] Status: ongoing margin test if '1'  
**MARGIN\_DONE** [1] Status: margin test done done, if '1'  
**MARGIN\_RESULT** [4] Status: Total margin result (flow0 and flow1):  
 0 = no error  
 1 = margin test error detected  
**MARGIN\_RESULT\_LEVEL** [14:8] Status: Margin result level for iterative margin test (flow 1).  
 Reflects the lowest margin level measured with positive margin test result.

### 3.1.7 Register MARGIN\_TEST\_RESULT\_DETAIL (0x8C)

5063

**MARGIN\_RESULT\_OFF\_LOCKBIT** [0] Status: Off State Margin test result of lock bits (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_OFF ASIC** [1] Status: Off State Margin test result of ASIC area (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_OFF SMA** [2] Status: Off State Margin test result of SMA area (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_OFF PAS** [3] Status: Off State Margin test result of PAS area (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_LEV\_LOCKBIT** [4] Status: Margin-level test result of lock bits (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_LEV ASIC** [5] Status: Margin-level test result of ASIC area (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_LEV SMA** [6] Status: Margin-level test result of SMA area (flow0):  
 0 = test passed  
 1 = error detected  
**MARGIN\_RESULT\_LEV PAS** [7] Status: Margin-level test result of PAS area (flow0):  
 0 = test passed  
 1 = error detected

Note: the result is only valid if the corresponding tests has been enabled.

## 3.2 Programming Flow

ID	parameter / condition	min	typ	max	unit
2925	Programming Voltage IDATA to GND	7.3	7.4	7.5	V



ID	parameter / condition	min	typ	max	unit
498	Programming Temperature	-40		125	°C
2926	Additional Programming Current at IDATA pin	0		1.2	mA
5064	Wait time after programming per 32bit block in bit serial programming			5.04	ms

3695  
1490

The programming of the OTP is only possible, if the extended mode or extended test mode is activated. The following flow shall be used to program the OTP. The flow is intended to be used for programming a complete OTP area (ASIC, SMA or PAS) and write the corresponding lockbits in one step:

1. Activate extended mode (by entering PSI BiDir service mode this is done automatically).
2. Check that bootloader is idle, read BOOTLOADER\_STATUS until BL\_READ\_DONE = 1
3. Write the intended data to the corresponding MOTP registers by SPI or PSI BiDir. It is recommended to program the complete PAS area in one step. In this case also the correct CRC must be written in the corresponding MOTP register. Writing the required data to the MOTP can be done with the multiwrite command in PSI BiDir. *Remark: Automatic calculation of CRC by the sensor is possible, but in this case read back after programming is mandatory.*
4. Write the lock bits to the register MOTP\_SCRATCH\_LOCK (0x3E), if lock bits shall be programmed. E.g. for PAS area lock bit, set MOTP\_SCRATCH\_LOCK [15] to 1. *Remark: When one or more lock bits are already set, writing to MOTP\_SCRATCH\_LOCK causes for PSI5-Variants the error code -491 to be sent. For SPI-Variants TFF / RE Flag is generated. The lockbit will be programmed despite the error message.*
5. *For automatic CRC calculation: write BL\_MOTP\_CALC\_CRC = 1 in BOOTLOADER\_CONTROL.*
6. *For automatic CRC calculation: wait min. 200 us until calculation finished.*
7. Set block address range to be programmed in register BOOTLOADER\_ADDRESS (0x80) (address 0x0E to 0x11 for PAS area).
8. Apply programming voltage at IDATA. The voltage must be stable before the programming is started.
9. Write BL\_START\_PROG = 1 and BL\_PROG\_LOCKBITS = 1 in BOOTLOADER\_CONTROL. *For manually calculated CRC: Also write BL\_BYPASS\_CALC\_CRC = 1.*
10. Wait for programming time, here for 4 blocks: 20.16 ms
6. Read BOOTLOADER\_STATUS (0x84). Check that bootloader is idle: BL\_BUSY = 0 and BL\_READ\_DONE = 1. Check no programming errors have occurred: PROGRAM\_ERR = 0 and VPROG\_ERR = 0. (Value of the complete register must be 0x2). If this register shows any other flags after programming, a correct programming cannot be assured and the part must be scrapped.
10. It is recommended to read back the values of the programmed OTP blocks and check, that the correct data was programmed. This can be done by reading the MOTP content after a restart or after a manual transfer from OTP to MOTP as described below.
11. It is mandatory to do a margin read test of all OTP areas after programming. Margin read flow is described below. If the margin test fails, a correct programming cannot be assured and the part must be scrapped.

Generally always complete 32bit blocks need to be programmed and each block must be programmed only one time. Programming one block several times with different values may lead to corrupted ECC values. Writing OTP blocks several times with identical values leads to accumulated charge on the OTP cell, even if all data bits are '0'. Therefore the probability of write disturbs increases with the number of rewrites.



### 3.3 Read OTP

ID	parameter / condition	min	typ	max	unit
5065	Wait time after reading per 32bit block			8	μs

4118

Reading OTP is done by copying the OTP content to the MOTP and reading the MOTP afterwards. The programmed OTP area should be read after programming, to ensure the programming was successful.

The following flow is used:

1. Activate extented mode (by entering PSI BiDir service mode this is done automatically).
2. Set block address range to be read in register BOOTLOADER\_ADDRESS (0x80) (address 0xE to 0x11 for PAS area).
3. Read BOOTLOADER\_STATUS (0x84). Check that BL\_BUSY=0.
4. Start reading from OTP to MOTP by setting BL\_START\_READ [1]=1 in BOOTLOADER\_CONTROL (0x82) register.

Optional: If the area for the read access is already secured by lockbits, the lockbits must be ignored. If the read access is done directly after programming (without restart), this step is not necessary.

Otherwise this must be done by setting the corresponding bits in BL\_IGNORE\_REGIONS [10:8] in BOOTLOADER\_CONTROL (0x82) register.

5. Wait for the reading time. E.g. for PAS area min.  $4 * 8\mu s = 32\mu s$ . No SPI or PSI interface access allowed during this time.
6. Read BOOTLOADER\_STATUS (0x84). Check that BL\_BUSY=0.
7. Read the selected MOTP register. E.g. by PSI Multiread command.

Remark: The lockbits are not transferred during a manual read access. They are only transferred during bootloading after restart!

It is also possible to read the OTP using the OTP wrapper. This is usually only needed for test and characterisation needs. Therefore this is described in the ASIC designspec in detail.

### 3.4 Margin Test

4119

Margin read tests are used to verify the quality of programmed OTP cells. It must be executed after every programming of the OTP on all OTP areas, which are already locked.

1494

To reduce test times the margin test is executed by the ASIC automatically after receiving the corresponding SPI or PSI BiDir command. Afterwards the result can be read from the MARGIN\_TEST\_RESULT (0x8A) register.

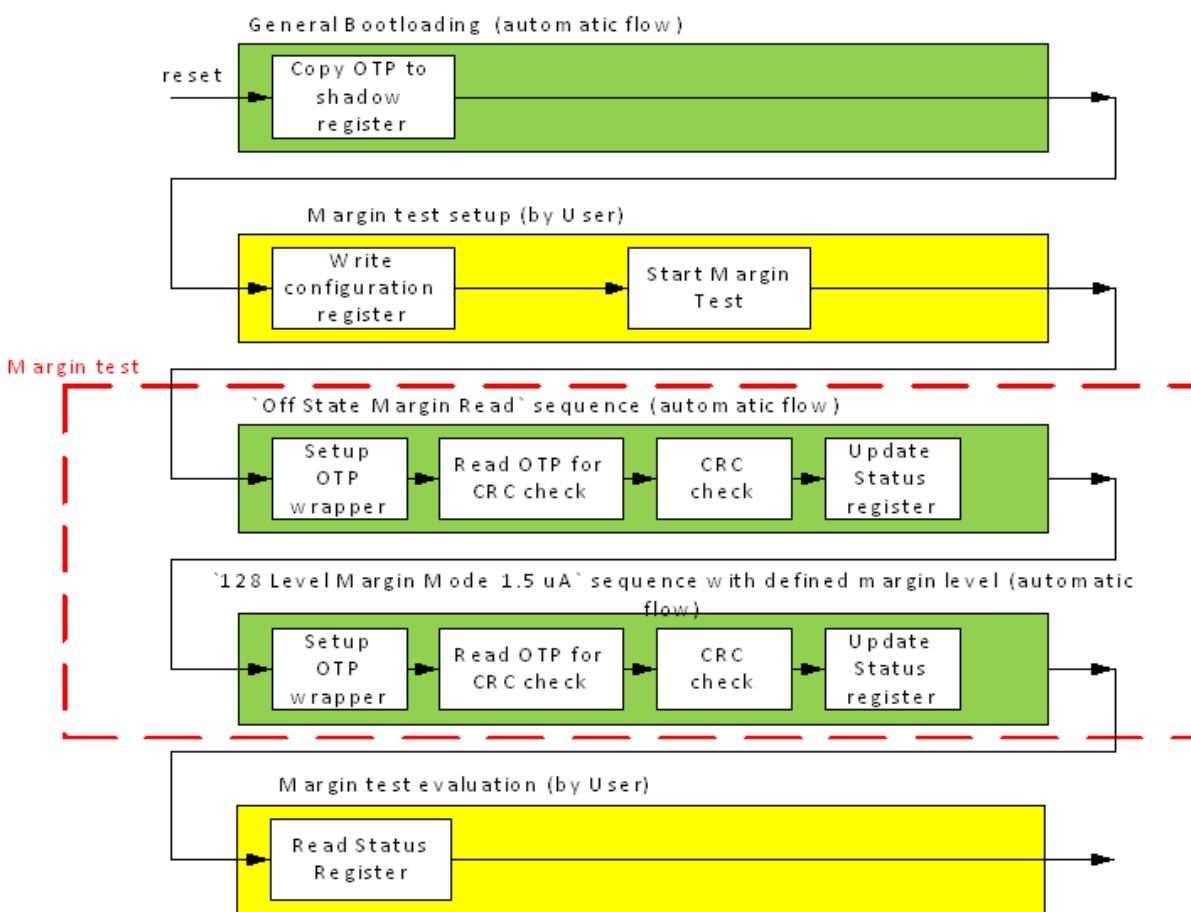
4120

#### Standard margin flow (flow 0)

The following flow chart shows the basic sequence of margin flow (flow 0).

The green boxes show the tasks which are automatically executed by the bootloader.

The yellow boxes are the tasks where a user initiates any tasks to run the margin test: setup configuration registers, start test, read results.



As shown the flow 0 consists of 2 sequentially executed margin tests (red box).

ID	parameter / condition	min	typ	max	unit
5067	Duration of margin flow 0			400	μs

5070

To get a correct margin test result, it must be selected, if the test is done directly after programming or if it is a retest, which is done with a much higher delay after programming. Directly after programming means within a time window of max. 10s. Retest can be done earliest after 53h. Between 10s and 53h no valid margin read test is possible. Usually the retest feature is used for OTP areas which were already programmed in earlier production steps.

E.g. after programming the PAS area, this area must be checked within 10s with **MARGIN\_LEVEL\_SELECT=0**. Additionally all other areas (ASIC/SMA) must be checked with the retest feature (**MARGIN\_LEVEL\_SELECT=1**).

1493

Before starting a margin test for a OTP area, the lock bit for this area must be set. To execute the automatic flow, the following steps must be executed:

1. Activate extended mode (by entering PSI BiDir service mode this is done automatically).
2. Read **BOOTLOADER\_STATUS** (0x84). Check that **BL\_READ\_DONE = 1**.
3. Start margin test by writing the configuration to **MARGIN\_TEST\_CONFIG1** (0x86):

**MARGIN\_START [0] = 1**

**MARGIN\_MODE [1] = 0**

**MARGIN\_TEST ASIC [2]** set to '1' if ASIC area shall be tested

**MARGIN\_TEST SMA [3]** set to '1' if SMA area shall be tested

**MARGIN\_TEST PAS [4]** set to '1' if PAS area shall be tested



**MARGIN\_TEST\_LOCKBITS [2]** set to '1' if lockbits shall be tested; lockbit check requires that at least one of the configuration registers MARGIN\_TEST ASIC, MARGIN\_TEST\_SMA or MARGIN\_TEST\_PAS = 1

#### **MARGIN\_LEVEL\_SELECT [6:5]**

set to '0' for margin test directly after programming (max. 10s)

set to '1' for retest of margin level more than 53h after programming

4. Wait for min. 400μs. During this time no communication is allowed.

5. Read Register MARGIN\_TEST\_RESULT (0x8A). Expected result:

**MARGIN\_BUSY [0]** = 0

**MARGIN\_DONE [1]** = 1

**MARGIN\_RESULT [4]**

0 = no error

1 = margin test error detected

6. Optional: Read MARGIN\_TEST\_RESULT\_DETAIL (0x8C) for detailed results.

#### **Flow 1 (for characterisation purpose)**

Flow 1 increases the margin level step by step to find the minimum possible margin level. It is only intended for characterisation and is described in the XA760 designspec in detail.

Additionally it is possible to read the OTP after margin test, to check each single bit.

When leaving extended mode or extended test mode or PSI service mode after a margin test the user must execute a reset in order to initialize the CRC generator. Otherwise a CRC error may occur.

### **3.5 CRC and lock bit handling**

The three separate areas in the OTP (ASIC, SMA, PAS) are secured separately by a 8 Bit CRC and a lockbit each.

ASIL\_D

#### **CRC generator:**

ASIL\_D

polynomial =  $0x12F (x^8 + x^5 + x^3 + x^2 + x + 1)$

initial value = 0xFF

Input bitwidth = 16 bit

Output bitwidth = 8 bit

The generator is fed with data from the higher OTP address down to data from the lower OTP address within an OTP area.

The CRC can be programmed to OTP by 2 different ways:

#### **First method:**

The Bootloader can be used to program the reference CRC values for each of the three shadow register regions (ASIC, SMA and PAS). Note that the CRC calculation has to be triggered before the actual programming flow as described above.

If a Bootloader controlled OTP programming has been triggered (*BL\_START\_PROG* field in *BOOTLOADER\_CONTROL* register)

by default the source for the CRC values to be programmed will be the calculated CRC values. The calculated CRC values are based on the momentarily MOTP shadow registers. Note that after this procedure, the CRC values programmed and boot loaded later, will always be based on a correct CRC reference.

#### **Second method: (recommended)**

The CRC values stored in the MOTP shadow registers will be used as programming source if the bit of *BL\_BYPASS\_CALC\_CRC* field of *BOOTLOADER\_CONTROL* register has been set before OTP



programming start. With this procedure the proper reference CRC values must be calculated externally and stored into the MOTP registers before programming.

*This method is recommended, because it ensures, that missing data in MOTP (e.g. due to communication problems prior to programming) will lead to a wrong CRC.*

After bootloading has been finished, the bootloader does cyclic CRC checks.

If an incorrect CRC is calculated an error code will be send over PSI and a flag over SPI (see also SPI/PSI chapter).

MOTP CRC checks starts right after bootloading has been performed (bootloading\_done) and is enabled if the bit OTP\_MASK\_CRC in the register *BOOTLOADER\_CONTROL* is not set.

Note that the MOTP CRC checks are disabled if extended mode or extended test mode is active.

Additionally MOTP CRC checks are also disabled right between first and second access to registers *CFG\_SOFTRESET* or *CFG\_EXT\_MODE* to avoid side effects by internal bootloader APB bus accesses.

485

### Lock bits

ASIL\_D

An active lockbit protects the associated OTP and MOTP region from programming or write access and is mandatory for all three regions (ASIC, SMA, PAS) after programming.

A lockbit can be activated only if it was previously programmed into OTP memory (with one) and transferred by the bootloader into the corresponding MOTP register. A direct SPI or PSI write to a MOTP lockbit will not activate the protection but can be used for a following OTP programming via bootloader. If a Bootloader controlled OTP programming has been triggered (using *BOOTLOADER\_CONTROL.BL\_START\_PROG*) the MOTP lock bits will be the source for the lock bits to be programmed when *BL\_PROG\_LOCKBITS* is set.

If at least one lockbit is set in the MOTP a subsequent write operation to *MOTP\_SCRATCH\_LOCK* is causing the following error condition depending on the used interface:

- PSI5: Error code -491 is returned.
- Bosch SPI: TFF is transmitted in the following SPI frame (no CRC error in immediate answer).
- Safe SPI: RE flag is returned in the answer frame.

If an additional lockbit is now set in *MOTP\_SCRATCH\_LOCK* and a lockbit programming operation is triggered over the bootloader then the operation is executed correctly despite the error message.

If the bit *BOOTLOADER\_CONTROL.BL\_IGNORE\_REGIONS* has been set previously all MOTP lock bits will be reset and zeros will be programmed into OTP. Ignoring already set lockbits will also prevent the interface from sending an error when writing a lockbit that is intended to be programmed via bootloader.

### 3.6 Overview of OTP Content

4112

The following table shows the OTP content of SMA7 products:



**BOSCH**

Department AE/ESI

# Internal Datasheet

## SMA7

Page - 43 / 237 -  
SAP: V2, DOORS: 5.3  
Date 17/01/2022

1.279.929.850

APB address (hex)	Block-Address (hex)	OTP Address (hex)	OTP Address (dec)	Content								
				7 (15)	6 (14)	5 (13)	4 (12)	3 (11)	2 (10)	1 (9)	0 (8)	
3E	0	0	0									Scratch area
		1	1	<b>Lock bit PAS</b>	<b>Lock bit SMA</b>	<b>Lock bit ASIC</b>						
		2	2									
		3	3									
		4	4	FINAL TESTING BITS								
		5	5									
		6	6									
		7	7	FINAL TESTING BITS								
		8	8									
		9	9	FINAL TESTING BITS								
		A	10									
		B	11									
0	3	C	12	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	
2		D	13	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	<b>SN_0</b>	
E	14	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	
F	15	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	<b>SN_1</b>	
4	16	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	<b>SN_2</b>	
6	17	18	<b>PSL_REF_SEL</b>	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	MARGIN_LEVEL_PROG	
8	19	20	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	Can't be used (SAC)	
A	21	22	Can't be used (lock bit)	Can't be used (lock bit)	Can't be used (lock bit)	CALIB_VBG	CALIB_VBG	CALIB_VBG	CALIB_VBG	CALIB_VBG	CALIB_VBG	
17	23	24	VMON_AVDD_OV	VMON_AVDD_OV	VMON_AVDD_OV	VMON_AVDD_UV	VMON_AVDD_UV	VMON_AVDD_UV	VMON_AVDD_UV	VMON_AVDD_UV	VMON_AVDD_UV	
C	25	26	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	ANAREG_CAL	
E	27	28	CALIB_OSC	CALIB_OSC	CALIB_OSC	CALIB_OSC	CALIB_OSC	CALIB_OSC	CALIB_OSC	CALIB_OSC	CALIB_OSC	
10	29	30	OSC_TC	OSC_TC	OSC_TC	OSC_TC	OSC_TC	OSC_TC	OSC_TC	OSC_TC	OSC_TC	
12	31	32	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	
14	33	34	MOTP_DCM_DIS	SPI_driver_strength	BITE_voltage_level_ch2	BITE_voltage_level_ch1	RC mode					
16	35	36	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	RANGE_CTRL	
18	37	38	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	SENS_CH1	
1A	39	40	MSOC_DURATION	MSOC_ENABLE	BITE_TOI_SCALE_SEL	CIA_TYPE_CH2	CIA_TYPE_CH2	CIA_TYPE_CH2	CIA_TYPE_CH2	CIA_TYPE_CH2	CIA_TYPE_CH2	
1C	41	42	43	44	45	BITES_CH1_TOL_LOW	BITES_CH1_TOL_LOW	BITES_CH1_TOL_LOW	BITES_CH1_TOL_LOW	BITES_CH1_TOL_LOW	BITES_CH1_TOL_LOW	
1E	46	47	GND_MEMS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	UVAS_DISABLE	
20	48	49	OSC_MOD_FREQ	OSC_MOD_FREQ	TM_NOERR	JITTER_OFF	FOC_MEAN	BITES_SIGN_CH2	BITES_SIGN_CH2	BITES_SIGN_CH2	BITES_SIGN_CH2	

4554

22	B	2E	46									
24	C	2F	47	Extended Device ID	Extended Device ID	Extended Device ID	Extended Device ID	Extended Device ID	Extended Device ID	Extended Device ID	Extended Device ID	
26		30	48	INIT_OFS_CH1	INIT_OFS_CH1	INIT_OFS_CH1	INIT_OFS_CH1	INIT_OFS_CH1	INIT_OFS_CH1	INIT_OFS_CH1	INIT_OFS_CH1	
28	D	31	49	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	SMA
2A		32	50	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	INIT_OFS_CH2	
2C	E	33	51	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	SENS_CH2	
2E		34	52	53	52	53	52	53	52	53	52	
2A	35	54	55	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	
2C	F	36	56	MANUFACT_CODE	MANUFACT_CODE	MANUFACT_CODE	MANUFACT_CODE	MANUFACT_CODE	MANUFACT_CODE	MANUFACT_CODE	MANUFACT_CODE	
2E		37	57	SENSOR_TYPE	SENSOR_TYPE	SENSOR_TYPE	SENSOR_TYPE	SENSOR_TYPE	SENSOR_TYPE	SENSOR_TYPE	SENSOR_TYPE	
30	G	38	58	SGB_HOUSING_CODE	SGB_HOUSING_CODE	SGB_HOUSING_CODE	SGB_HOUSING_CODE	SGB_HOUSING_CODE	SGB_HOUSING_CODE	SGB_HOUSING_CODE	SGB_HOUSING_CODE	
32		39	59	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	
34	H	40	60	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	SGB_CODE_CUSTOMER	PAS
36		41	61	SGB_MANU_DATE	SGB_MANU_DATE	SGB_MANU_DATE	SGB_MANU_DATE	SGB_MANU_DATE	SGB_MANU_DATE	SGB_MANU_DATE	SGB_MANU_DATE	
38	I	42	62	PST_BLANKETIME	PST_BLANKTIME	PST_BLANKTIME	PST_BLANKTIME	PST_BLANKTIME	PST_BLANKTIME	PST_BLANKTIME	PST_BLANKTIME	
3A		43	63	SGB_LINE_NO	SGB_LINE_NO	SGB_LINE_NO	SGB_LINE_NO	SGB_LINE_NO	SGB_LINE_NO	SGB_LINE_NO	SGB_LINE_NO	
44	J	44	64	OSSC_MON_ERR_CNT_LIMIT	OSSC_MON_ERR_CNT_LIMIT	PST1_REVISION	PST1_SETTING_CH2	PST1_SETTING_CH2	PST1_SETTING_CH2	PST1_SETTING_CH2	PST1_SETTING_CH2	
46		45	65	SIGN_CH2	SIGN_CH2	FOC_LIMIT	FOC_LIMIT	FOC_LIMIT	FOC_LIMIT	FOC_LIMIT	FOC_LIMIT	
48	K	47	66	PSL_MODE	PSL_MODE	PSL_MODE	PSL_MODE	PSL_MODE	PSL_MODE	PSL_MODE	PSL_MODE	
50		48	67	OSSC_MON_EN	OSSC_MON_EN	OSSC_MON_SYNC_MON_MIN	OSSC_MON_SYNC_MON_MIN	OSSC_MON_SYNC_MON_MIN	OSSC_MON_SYNC_MON_MIN	OSSC_MON_SYNC_MON_MIN	OSSC_MON_SYNC_MON_MIN	
52	L	49	68	OPS_MSOC_DISABLE	OPS_MSOC_DISABLE	SMA_RANGE_CH2	SMA_RANGE_CH2	SMA_RANGE_CH2	SMA_RANGE_CH2	SMA_RANGE_CH2	SMA_RANGE_CH2	
54		50	69	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	OSSC_MON_ERR_CNT_UP	
56	M	51	70	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	Can't be used	
58		52	71	CRC	CRC	CRC	CRC	CRC	CRC	CRC	CRC	
60	N	53	72	not used	not used	ECC 0						
62		54	73	not used	not used	ECC 1						
64	O	55	74	not used	not used	ECC 2	ECC					
66		56	75	not used	not used	ECC 3						
68	P	57	76	not used	not used	ECC 4						
70		58	77	not used	not used	ECC 5						
72	Q	59	78	not used	not used	ECC 6						
74		60	79	not used	not used	ECC 7						
76	R	61	80	not used	not used	ECC 8						
78		62	81	not used	not used	ECC 9						
80	S	63	82	not used	not used	ECC A						
82		64	83	not used	not used	ECC B						
84	T	65	84	not used	not used	ECC C						
86		66	85	not used	not used	ECC D						
88	U	67	86	not used	not used	ECC E						
90		68	87	not used	not used	ECC F						
92	V	69	88	not used	not used	ECC 10						
94		70	89	not used	not used	ECC 11						



### 3.7 Wafer Level Area (ASIC)

3608

This area contains all Bits for the trimming at EWS. The details are defined by the ASIC project.

#### 3.7.1 Content/Functionalities

ID	parameter / condition	min	typ	max	unit
504	<b>[Serial number]</b>  Unique serial number for every single SMA. Programmed during ASIC EWS.		48		Bit
505	<b>[CRC and Lock bit for wafer level area]</b>		8 + 1		Bit

503

- Bits for calibration on Waferlevel (e.g. Bandgap; monitors,...). Detailed specification in ASIC Design spec.

### 3.8 Module Level Area (SMA)

3609

This area contains the trimming information from final test.

#### 3.8.1 Content/Functionalities

ID	parameter / condition	min	typ	max	unit
509	<b>[OUT_PSI/OUT_SPI]</b>  SPI/PSI disable bits: SPI=0, PSI=0: The ASIC listens and answers to SPI. The ASIC accepts PSI command, but does not answer (PSI current sink deactivated). With this setting the sensor will execute a PSI Init 1 phase after power-up. SPI=1, PSI=0: The ASIC only listens and responds to PSI communication SPI=0, PSI=1: The ASIC only listens and responds to SPI communication 11: Not valid		2		Bit
510	<b>[CMA_TYPE_CHx]</b>  Four Bits (two bits per channel) to document CMA Type. This information is needed to generate init data9 in combination with [SMA_Range] from satellite level area. It is also used to determine amplification factor and LSB/g setting. 0b00 = 120g 0b01 = 480g 0b10 = 800g 0b11 = not valid		2 x 2		Bit
511	<b>[SENS_CHx]</b>  Used to set the fine gain trimming. Range 0..255		2 x 8		Bit
512	<b>[BITE_CHx_TOL_LOW/UP]</b> unsigned values		4 x 8		Bit



ID	parameter / condition	min	typ	max	unit
	Limits for BITE check during PSI initphase. Upper and lower limit for each channel. No function in SPI. Range 0..255				
513	<b>[RANGE_CTRL]</b>  Sets the max. correction range for FOC and SOC with 1LSB/g. Range 0..255. Programming a '0' will disable FOC/SOC error.		8		Bit
5384	<b>[MSOC_ENABLE]</b>  Enable Medium Speed Offset Cancellation (MSOC).		1		Bit
5385	<b>[MSOC_DURATION]</b>  MSOC active period: 0 = 3.7 sec 1 = 7.4 sec		1		Bit
514	<b>[BITE_CHx_REF_POS/NEG]</b> signed values  32 Bit to store positive and negative selftest new part values for each channel. These bits are for documentation purpose only and have no functional relevance for the ASIC. They are stored with 2 LSB/g for SMA760, with 4LSB/g for SMA720 and with 1LSB/g for all other SMA. Range -128..+127		4 x 8		Bit
515	<b>[INIT_OFS_CHx]</b>  14 bits per channel to store new part value of raw offset during trimming. Raw offset is stored with 32LSB/g (max. value +/- 255g).		2 x 14		Bit
525	<b>[BITE_VOLTAGE_LEV_CHx]</b>  Bit to change selftest voltage for adaptation to MEMS: 0 = 1.34 V 1 = 2.4 V		2 x 1		Bit
5406	<b>[BITE_TOL_SCALE_SEL]</b>  BITE tolerance scaling factor for {SMA_RANGE=0, CMA_TYPE=0}: 0 = scaling factor 0.5 1 = scaling factor 2		1		Bit
5407	<b>[SPI_DS]</b>  SPI pad driver strength.		1		Bit
524	<b>[EXT_DEV_ID]</b>  Used to store an extended device ID which can be read out over SPI or PSI BiDir. The content in hexadecimal representation corresponds to the last two digits of the SMA7 variant (e.g. 0x53 for SMA753).		8		Bit
519	<b>[JITTER_OFF]</b>  Deactivate the EMC jitter of the oscillator. This bit is relevant for both applications, peripheral (PSI) and ECU (SPI).		1		Bit



ID	parameter / condition	min	typ	max	unit
2018	<b>[OSC_MOD_FREQ]</b> Select EMC jitter modulation frequency: 0b00 = 4 kHz 0b01 = 3.5 kHz 0b10 = 2 kHz 0b01 = 1 kHz		2		Bit
2019	<b>[OSC_MOD]</b> Configure frequency variation for EMC jitter: 0 = +/- 0.424 % 1 = +/- 0.823 %		1		Bit
521	Bits to disable separately Over- and Undervoltage detection Monitors: <b>[OVSI_DISABLE]</b> <b>[OVA_DISABLE]</b> <b>[UVS_DISABLE]</b> <b>[UVSI_DISABLE]</b> <b>[UVA_DISABLE]</b> <b>[GND_MEMS_DISABLE]</b> <b>[GND_EXT_DISABLE]</b>		7 x 1		Bit
5386	<b>[DCM_DIS]</b> Disable Die-Corrosion-Monitor. Can be overwritten by configuration register (SPI). Must be set to '0'. (Deactivation of DCM not released).		1		Bit
522	<b>[C_CUT_DISABLE]</b> Disable startup C-loss feature in peripheral application. This bit is relevant only for peripheral mode. In SPI mode, startup C-loss can be activated by SPI command.		1		Bit
2021	<b>[RC_MODE]</b> Activate random chopping: 0b00= Random Chopping (with noise-shaping) 0b01= White Noise Chopping 0b10= No Chopping 0b11= No Chopping (switches inverted compared to 0b10)		2		Bit
2022	<b>[TM_NOERR]</b> Supress the PSI5 error transmission		1		Bit
547	<b>[BITE_SIGN_CHx]</b> Invert the sign for PSI5 BITE evaluation.		2		Bit
2024	<b>[FOC_MEAN]</b> 0: The mean value of 512 samples is taken and compared with the limit for residual offset 1: One sample is taken after FOC and compared with the limit for residual offset <i>In async mode or sync mode with 250µs syncpulse distance always only one sample is</i>		1		Bit



ID	parameter / condition	min	typ	max	unit
	<i>taken (independent of the OTP bit). Additionally the setting of FOC_mean does not influence the number of samples during Initphase 2 (transmitted, if PAS lockbit is not set).</i>				
516	[CRC and Lock bit for SMA area]		8+1		Bit

### 3.9 Customer Area (PAS)

3610

This area contains customer specific configurations. It can be programmed at final-test at Bosch or by customer, depending on the sensor type. For SPI variants, this section is being programmed during final-test.

#### 3.9.1 Content/Functionalities

ID	parameter / condition	min	typ	max	unit
535	<b>[SAMPLE_TIMING]</b> Activate data sample time feature. This is relevant only for peripheral mode. 0b00 = sampling 6µs after sync-pulse 0b01 = sampling 49µs after sync-pulse 0b11 = sampling T_bit/2 before first data bit (D0-bit)		2		Bit
536	<b>[FILTER_SETTING_CHx]</b> Select output filter frequency for each channel individually. Those bits are relevant for peripheral mode only. In SPI mode, filter frequency can be selected by SPI command. 0b00 = 430 Hz 0b01 = 215 Hz 0b10 = 860 Hz 0b11 = 53 Hz		2 x 2		Bit
538	<b>[MANUFACT_CODE]</b> Manufacturer code to be transmitted in Initialization phase of PSI5. Not relevant for SPI.		8		Bit
539	Bits to be transmitted in initialization phase (no function). These Bits are arranged in successional in OTP registers to facilitate value reading in ECU mode:  <b>[SGB_HOUSING_CODE]</b> 6 bits satellite housing code <b>[SGB_CODE_CUSTOMER]</b> 12 bits sensor code customer <b>[SGB_MANU_DATE]</b> 14 bits satellite manufacturing date <b>[SGB_LINE_NO]</b> 4 bits satellite line no <b>[SGB_LOT_NO]</b> 4 bits satellite lot number <b>[PAS_GEN]</b> 4 bits satellite generation <b>[SGB_AXIS_CHx]</b> 2 + 2 bits satellite-axis <b>[COMPATIBILITY_BIT]</b> 1 bit for backward compatibility		49		Bit



ID	parameter / condition	min	typ	max	unit
540	<b>[PSI_MODE]</b>  Select PSI5 communication mode.		7		Bit
4078	<b>[ADV_TIMING]</b>  0: Advanced timing for PSI5 communication disabled, communication timing based on internal oscillator 1: Advanced timing for PSI5 communication enabled, communication timing based on sync pulse distance		1		Bit
541	<b>[SO_TRISTATE_EN]</b>  Permanently set SO Pad to tristate. Relevant in peripheral mode only. Default = SO active. For analysis purpose, this bit can be overridden by BiDir command.		1		Bit
542	<b>[SMA_RANGE_CHx]</b>  Set individual measurement ranges for each channel. Depending on different MEMS types, some configurations might be forbidden. In case of an invalid configuration, the error code "invalid configuration" is being raised in PSI5 mode.  0b000 = 120g 0b001 = 240g 0b010 = 480g 0b011 = 30g 0b100 = 60g		2 x 3		Bit
545	<b>[FOC_DISABLE] [MSOC_DISABLE] [SOC_DISABLE]</b>  Deactivate fast, medium and/or slow offset cancellation. This bits are relevant for peripheral (PSI5) application only. In SPI Mode, offset cancellation has to be triggered separately by SPI command.		3		Bit
546	<b>[FOC_LIMIT]</b>  Select FOC limit. This bit is relevant for peripheral mode only. Value = 0 means offset is not checked. In SPI, residual offset is checked by system. The limit is programmed in LSB (referred to the 10 bit PSI output), <u>not</u> in LSB/g. For the 16bit PSI output ,1 LSB in the OTP equals 16LSB at the PSI interface. As the 16bit PSI output has a constant sensitivity of 64LSB/g, the OTP values in this case have a weight of 4LSB/g.  <i>Note: As the limit is always programmed in LSB, different SMA_range settings will lead to different limits in g for the 10bit mode.</i>		6		Bit
548	<b>[SIGN_CHx]</b>  Invert the output signal for each channel at the last stage. This bit is relevant for both		2		Bit



ID	parameter / condition	min	typ	max	unit
	applications, peripheral (PSI) and ECU (SPI). If this Bit is set to one, the sign of the signal and the sign of the limits for BITE test are inverted.				
2027	<b>[PSI5_REVISION]</b>  Select PSI5 rev 1.3 or 2.1, transmitted during init phase.		1		Bit
2941	<b>[DC_SOFT_SO_EN]</b>  Daisy-Chain soft-switch enable. Has to be set to 0 (feature not usable).		1		Bit
3968	<b>[SENSOR_TYPE]</b>  These bits are transmitted in init-phase 2 for PSI5 variants (function of sensor is not altered).		4		Bit
5418	<b>[PSI_BLANK_EN]</b>  Enable PSI5 sync pulse blanking time.		1		Bit
5419	<b>[PSI_BLANK_TIME]</b>  Defines PSI5 sync pulse blanking time: 0 = blanking time calculated by 250us - OSC_MON_ACC_MIN 1 = blanking time calculated by 500us - OSC_MON_ACC_MIN		1		Bit
5412	<b>[OSC_MON_EN]</b>  Global enable for OSC monitoring.		1		Bit
5417	<b>[OSC_MON_ERR_CNT_RESET]</b>  Behaviour of OSC error counter if a pair of valid sync pulses is detected: 0 = Decrement the counter with OSC_MON_ERR_CNT_DOWN 1 = Reset the error counter		1		Bit
5415	<b>[OSC_MON_SYNC_MON_MIN]</b>  Timing definition of OSC monitor window: 0 = +/-7% 1 = +/-8%		1		Bit
5413	<b>[OSC_MON_ACC_MAX/MIN]</b>  Minimum tolerance border to detect valid PSI5 sync pulses: 0b00 = +/-8% 0b01 = +/-9% 0b10 = +/-10% 0b11 = +/-12%		2 x 2		Bit
5414	<b>[OSC_MON_ERR_CNT_UP/DOWN]</b>  Adjustable positive and negative slope (stepsize) of the OSC monitor error counter: 0b00 = +/-1 0b01 = +/-2 0b10 = +/-4 0b11 = +/-8		2 x 2		Bit
5416	<b>[OSC_MON_ERR_CNT_LIMIT]</b>		3		Bit

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ID	parameter / condition	min	typ	max	unit
	Threshold value for the OSC monitor error counter: 0b000 = 0.125s 0b001 = 0.25s 0b010 = 0.5s 0b011 = 1.0s 0b100 = 2.0s 0b101 = 4.0s 0b110 = 8.0s 0b111 = 16.0s				
549	<b>[CRC and Lock bit for module level area]</b>		8 + 1		Bit



## 4. Configuration registers

### 4.1 Adress map

4132

The following table shows the register address map of XA760:

link:

[file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration\\_sensors/sma76x/External/02\\_Specification\\_TCI/11 ASIC design spec/XA760 CA/XA760 AddrMap.html](file:///bosch.com/dfsrb/DfsDE/LOC/Rt/AENE/ne4/projects/acceleration_sensors/sma76x/External/02_Specification_TCI/11 ASIC design spec/XA760 CA/XA760 AddrMap.html)

### 4.2 Access restrictions

4134

r== read access

w== write access

#### Normal Mode

MOTP (0x00 - 0x3e)	r before EOP; no access if EOP_EN=1
CFG (0x40 - 0x72)	r/w before EOP; r if EOP_EN=1, except 0x6e softreset
CFG (0x74 - 0x8e)	no access
OTP-Wrapper (0xc0 - 0xe6)	no access

#### Extended Mode

MOTP (0x00 - 0x3e)	r/w
CFG (0x40 - 0x72)	r/w
CFG (0x74 - 0x7E)	r
CFG (0x80 - 0x82,0x86 - 0x88)	r/w
CFG (0x84,0x8A - 0x8C)	r
OTP-Wrapper (0xc0 - 0xe6)	r/w

#### Extended Testmode

MOTP (0x00 - 0x3e)	r/w
CFG (0x40 - 0x72)	r/w
CFG (0x74 - 0x7C)	r/w
CFG (0x80 - 0x82,0x86 - 0x88)	r/w
CFG (0x84,0x8A - 0x8C)	r
OTP-Wrapper (0xc0 - 0xe6)	r/w

Config register 0x7E is a PSI test register that requires the PSI to be active.

Config register CFG\_TEST\_CONFIG5 is a PSI test register that requires the PSI to be active. Within the described modes there might be several additional write enable conditions (e.g. MOTP registers are writable only if lockbits are cleared). These conditions are given in the HTML register map.

### 4.3 CRC for safety related Configuration Registers

3858

To make sure the safety related data in the configuration registers are not corrupt during operation, the following information is secured by CRC:

- SPI Voltage mode selection (CFG\_VOLTAGE\_MODE)
- SPI protocol selection (CFG\_SPI\_PROTOCOL)
- Offset cancellation mode (off/SOC/XSOC/FOC); for both channels (CFG\_OC\_CHx in CFG\_OFFSET\_CONFIG)
- number of offset cancellation steps for FOC; for both channels (CFG\_OC\_LENGTH\_CHx in CFG\_OFFSET\_CONFIG)

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- FIR filter frequency selection; for both channels (CFG\_FILTER\_CHx)
- Static raw offset correction (CFG\_RAW\_OFS\_CHx)

The CRC will be updated if any of the safety related data is re-configured via SPI.

4135

#### CRC-Parameters

48 CRC-relevant data bits

8 CRC-bits

polynomial = 0x12F ( $x^8 + x^5 + x^3 + x^2 + x + 1$ )  
initial value = 0xFF

#### 4.4 Extended Mode

646

The Extended Mode gets active after writing the specific magic code (0x7B) to the field CFG\_MAGIC\_CODE\_7B in register CFG\_EXT\_MODE.

With the same access CFG\_EXT\_M=1 has to be set in CFG\_EXT\_MODE.

One write access is needed to activate Extended Mode.

3697

This mode is accessible from Bosch SPI and Safe SPI.

4170

The extended mode gets automatically activated for PSI service mode (CFG\_PSI\_SM\_EN = 1).

#### 4.5 Extended test mode

3708

The Extended Testmode gets active after writing the specific magic code (0x5C) to the field CFG\_MAGIC\_CODE\_5C in register CFG\_EXT\_MODE.

With the same access CFG\_EXT\_TM=1 has to be set in CFG\_EXT\_MODE.

Two consecutive write accesses are needed to activate Extended Testmode.

3699

BoschSPI: 0x39972004

The extend test mode grants read/write access to additional CFG registers. Therefore additional test functions, including the following, are available:

3700

- Enable internal test capacitors for frontend (IntCaps)
- Enable/disable PSI current sink (PAS2ONE and PAS2ZERO test)
- Mask all monitor flags in PSI5 mode
- Enable SPI communication
- Multiplexing of internal signal to SO-Pin (e.g. SGND, VBG, DVDD, AVDD, IREF, UREF\_BITE)
- Readout acceleration data at output of decimation filter
- Readout acceleration data at output of FIR filter
- Readout of the offset register (the whole bit width of offset regulator)

4038

4904 This means, the following outputs of the digital signal processing chain can be traced by SPI register access:

- DEC output of channel 1 (18 bit)
- DEC output of channel 2 (18 bit)
- FIR output of channel 1 (20 bit)
- FIR output of channel 2 (20 bit)
- Offset data of channel 1 (20 bit)
- Offset data of channel 2 (20 bit)

These signals can be read by:

- CFG\_MON\_DATA1.CFG\_MON\_DATA\_15\_0 (bit 15:0 of the corresponding trace signal)
- CFG\_MON\_DATA2.CFG\_MON\_DATA\_31\_16 (bit 31:16 of the corresponding trace signal, unused LSBs are set to 0)

The signal selection (multiplexing to the output registers CFG\_MON\_DATA1/2) is done by:

- CFG\_MON\_DATA\_MUX, see register map



4905

There is a register read mechanism (freeze mechanism) implemented which tightly couples CFG\_MON\_DATA1 and CFG\_MON\_DATA2:

- Before any read access to CFG\_MON\_DATA1 or CFG\_MON\_DATA2 both registers are in an unfrozen state.
- An initial read access to CFG\_MON\_DATA1 causes a common freeze of CFG\_MON\_DATA1 and CFG\_MON\_DATA2.

The frozen state of both registers is kept until CFG\_MON\_DATA2 is read. This means, only a sequential register read access to CFG\_MON\_DATA2 causes a common release of the frozen state of both registers.

- An initial read access to CFG\_MON\_DATA2 causes a common freeze of CFG\_MON\_DATA2 and CFG\_MON\_DATA1.

The frozen state of both registers is kept until CFG\_MON\_DATA1 is read. This means, only a sequential register read access to CFG\_MON\_DATA1 causes a common release of the frozen state of both registers.

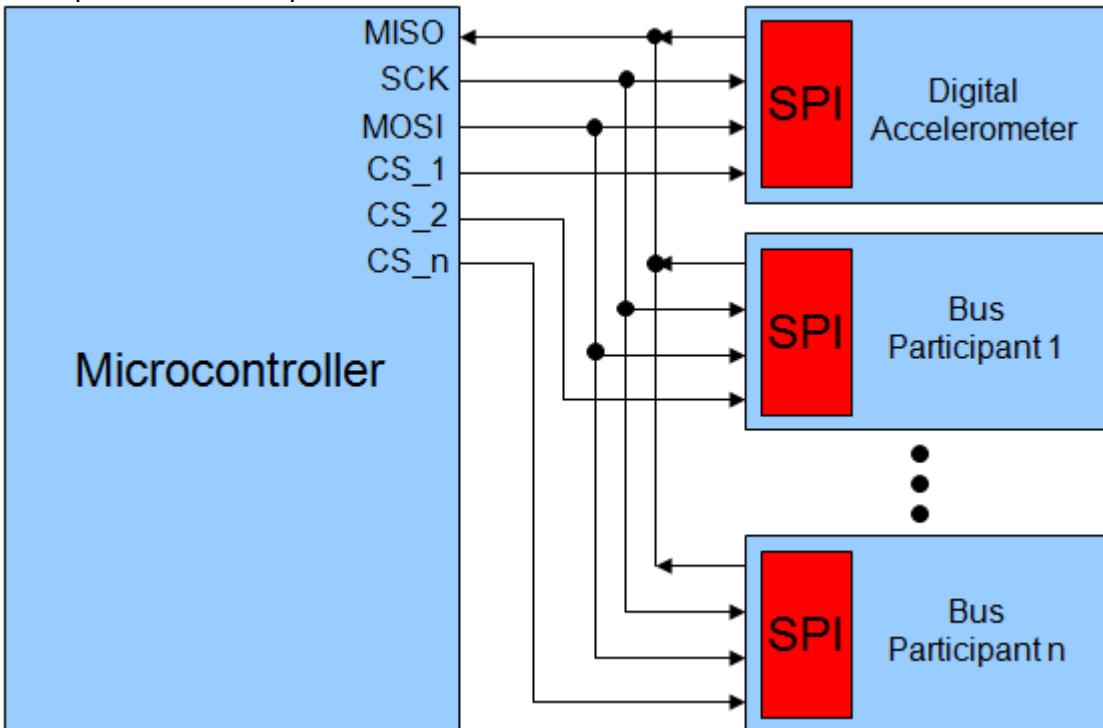
This is a safety mechanism in order to ensure that the data on both monitor registers are associated to each other.



## 5. SPI Interface

### 5.1 Hardware Layer

The SMA7 provides a bi-directional 3.3V serial peripheral interface (SPI) for communication with the ECU via a 32 bit data word size. The sensor always operates in slave mode whereas the microcontroller unit (MCU) provides the master function. The interface consists of 4 signals as shown below.  
 Principal SPI bus setup:



#### Serial clock (SCK):

Input for master clock signal. This clock determines the speed of data transfer and all receiving and sending is done synchronous to this clock.

#### Chip Select (CSB):

CSB activates the SPI interface. As long as CSB is high, the IC does not accept the clock signal or data and the output SO is in high impedance. Whenever CSB is in a low logic state, data can be transferred from the microcontroller and vice versa.

#### Serial Input (MOSI):

Data input is latched synchronized by SCK clock.

#### Serial Output (MISO):

Data output synchronized by SCK clock.

ID	parameter / condition	min	typ	max	unit
2945	SPI Input Voltage V_IH Hi-Voltage	0.7*Vddi		Vddi	V
2946	SPI Input Voltage V_IL Low-Voltage	-0.05		0.3*Vddi	V
2947	SPI Output Voltage V_IH Hi-Voltage	0.8*Vddi		Vddi	V
2948	SPI Output Voltage V_IL Low-Voltage	0		0.2*Vddi	V



ID	parameter / condition	min	typ	max	unit
4815	maximum dynamic over-/undershoot voltage CSB/SCK/MOSI; min or max value applied for less than 25ns per half SCK period	-0.8		4.27	V
2949	SPI Input Current Hi-Current CSB-Pin; Low-current SI/SCK-Pin	-10		10	µA
2950	SPI Input Current Low-Current CSB-Pin	-70	-35	-20	µA
4812	SPI Input Current High-Current SI/SCK-Pin	20	35	70	µA
2951	SPI Input Pull-up Resistor CSB-Pin	39	100	129	kOhm
4813	SPI Input Pull-down Resistor SI/SCK-Pin	44	100	133	kOhm
2952	Input Capacitance CSB-/SI-/SCK-Pin	0.7	1.01	6	pF
2953	Output Capacitance SO-Pin	0.7	1.01	6	pF
2954	Input voltage hysteresis CSB-/SI-/SCK-Pin	0.6			V

## 5.2 SPI Protocol

573 It is possible to choose between two SPI protocols, the Safe SPI protocol, and the Bosch SPI protocol.  
 574 The Bosch SPI protocol is an in-frame protocol whereas the Safe SPI protocol is an off-frame protocol.  
 575 The selection is carried out via SPI command.

576 In the below definition tables of the SPI frames, any “-“in MOSI corresponds to a “don’t-care-bit”, i.e. it can be arbitrary chosen without any effect on the sensor. In MISO it corresponds to high impendancy SO status.

## 5.3 Power-on Phase to Normal Operation

### 5.3.1 Selection of SPI

579 After release of the automatic power-on reset circuit, the SPI protocol (either Bosch or Safe SPI) is selected by an initial SPI command sent by the master. Two SPI SI registers are listening to MO (master



out): One SI register 'MOSI1' operating in Safe SPI mode, the other SI register 'MOSI2' in Bosch SPI mode.

580  
581

For each protocol, the selection command is defined as described in the following.

Sensor resumes in Safe SPI mode and deactivates the MOSI2 register only after receiving:

WR PROT SEL: protocol selection to switch between Bosch SPI 0xFF00FF00 and Safe SPI 0x00FF00FF																																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SI	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		

582

Sensor resumes in Bosch SPI mode and deactivates the MOSI1 register only after receiving:

WR PROT_SEL: protocol selection to switch between Bosch SPI 0xFF00FF00 and Safe SPI 0x00FF00FF																																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SI	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		

4558

Comment: Depending on the detailed timing of the ECU also seven or nine "1" instead of eight (e.g. 007F007F) can activate the SafeSPI protocol.

583

The sensor resumes its operation in Safe SPI mode only upon receiving the Safe SPI selection key in the Safe SPI SI register. This ensures that by the Safe SPI key cannot be interpreted as Bosch SPI key by the Bosch SPI SI register.

The sensor resumes its operation in Bosch SPI mode only upon receiving the Bosch SPI selection key in the Bosch SPI SI register. This ensures that by the Bosch SPI key cannot be interpreted as Safe SPI key by the Safe SPI SI register.

3691

Before protocol selection, all other commands except protocol selection are ignored.

3905

The Protocol Selection is not done and locked, till a correct Protocol Selection Calibration-Command is received.

585

The selected protocol can only be changed after a hard reset.

584

Immediately after SPI selection the sensor is waiting for the voltage mode selection.

Other commands will be executed, but no response is send, as SO stays in high impedance.

(Executed means: In case of a write command the corresponding register value is changed, which may trigger functions like e.g. FOC or BITE)

3906

The SO stays at high impedance till a correct Protocol Selection and Voltage Mode Selection is done.

### 5.3.2 Selection of Voltage Mode

587

The SMA7 supports two different voltage modes (supply voltage ranges).

588

Voltage mode selection command has to be sent as second command after protocol selection.

590

The selected voltage mode can only be changed after a hard reset.

591

Available modes are:

592

- 0010 and 0100: Supply = 4.5V - 11V (Vdd); SPI = 3.3V (14bit sensor data)
- 1000: Supply = 3.13V - 3.47V (Vddi); SPI = 3.3V (14Bit sensor data)

594

All other combinations are not accepted.

5076

### 5.3.3 Test Phase

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Offset cancellation using CFG\_OFFSET\_CONFIG:

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- The command "WR\_OFFSET\_CANCELLATION" is only accepted before EOP.

600

- The FOC is actively triggered by SPI Command.

601

- Retriggering of FOC is possible.

5114

- Triggering FOC for one channel, while the FOC for the other channel is active may lead to RE/TFF/CRC errors. Therefore, if FOC is needed for both channels, it shall be triggered with one command for both channels. Alternatively, only one channel can be triggered (write b00 for the not used channel) and the other channel can be triggered after FOC of first channel is finished.

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- After FOC is finished the fields OFF1 and OFF2 (in "WR\_OFFSET\_CANCELLATION" command) must be reset to 0 explicitly before restarting FOC. There is no automatically reset implemented for OFF1 and OFF2.

602



- If SOC is needed it must be triggered manually before EOP. It is not allowed to change between slow and extra slow offset cancellation. Once one offset cancellation speed has been chosen, it must remain the same.
- If SOC is triggered, the number of samples (OC length1 & 2) must be kept the same as in previous FOC command. OC length 1 & 2 shall only be changed in combination with retriggering of FOC (otherwise consequence would be an offset jump).
- FOC and SOC are not possible at the same time.
- Deactivation of SOC and triggering of FOC is possible within the same command.
- FOC cannot be deactivated manually (except by softreset). FOC state is left automatically after FOC is finished.
- FOC cannot be triggered during active selftest.
- Default = FOC/SOC deactivated; OC-length 64 steps.
- If neither FOC nor SOC is triggered, only the stored raw offset value is subtracted from the offset.

#### Self test using CFG\_SBITE\_MODE:

The build-in selftest needs to be activated during initialization by the SPI command WR\_TEST\_MODE. Afterwards the value of the selftest signal can be read by RD\_SENSOR\_DATA command. The measured value shall be compared to the reference values, which are stored in the OTP. High deviations between stored and measured values indicate a defect of the sensor.

- The command "WR\_TEST\_MODE" activates and deactivates the self test. It is only accepted before EOP.
- The initial self test value is saved in the OTP at Robert Bosch final tests and can be read with the "RD\_BITE\_CH1/2" commands.
- It is possible and recommended to set the self test setup for both channels simultaneously.
- FOC and SOC shall be deactivated before triggering self test.
- Self test cannot be activated during active SOC or FOC.
- Default = self test deactivated.
- The selftest state can only be left by deactivating the selftest with "WR\_TEST\_MODE" or by performing a softreset.

The selftest can be triggered independently for each channel.

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*Comment: Triggering the selftest independent is only allowed for characterization purpose. In the application it is mandatory to trigger the selftest of both channels simultaneously.*

Setting CFG\_TMD\_Chx=0b01 leads to an electrostatic force between C1x and CMx and therefore will result in a positive signal in combination with the connected MEMS.

Setting CFG\_TMD\_Chx=0b10 leads to an electrostatic force between C2x and CMx and therefore will result in a negative signal in combination with the connected MEMS.

ID	parameter / condition	min	typ	max	unit
452	Selftest Build Up Time  ECU-Types; deviation from final value <2%; 860Hz filter mode			2.40	ms
453	Selftest Build Up Time  ECU-Types; deviation from final value <2%; 430Hz filter mode			3.36	ms
454	Selftest Build Up Time  ECU-Types; deviation from final value <2%; 215Hz filter mode			5.27	ms
455	Selftest Build Up Time  ECU-Types; deviation from final value <2%; 53Hz filter mode			18.20	ms



4898

EOP using CFG\_EOP\_EN:

- The only possibility to exit EOP is via soft reset.
- EOP cannot be activated during active FOC or BITE
- After EOP neither BITE nor FOC is possible

4900

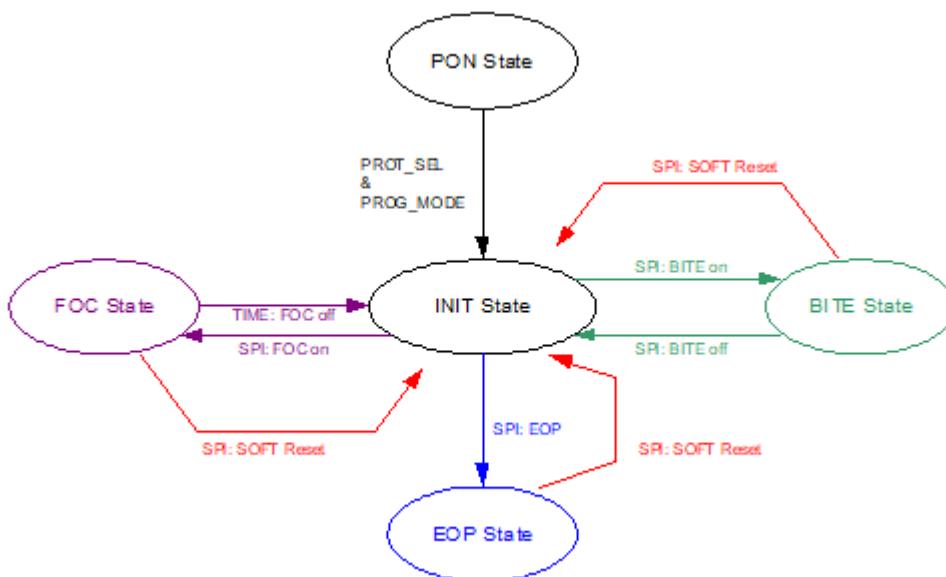
The sensor hardware makes certain restrictions to the usage of SPI commands when one of these functions is active:

-FOC State (Fast Offset Cancellation) and

-BITE State (Built in test)

-EOP State (End of programming) (In this context, EOP is also considered as a function)

All allowed commands in the specific function are defined in the following diagram:



617

C-loss detection:

- The initial C-loss detection can be triggered with the "WR\_CONFIG\_1" command.
- Default = switched off.
- The initial C-loss detection works only, if the sensor is supplied with VDD (6.7V mode). In 3.3V mode the test can be triggered, but will always be passed (no error flag will be set).

620

SPI communication during the C-loss test can disturb the test and may lead to wrong test results.

Therefore it is not allowed to send further SPI commands within the duration of the C-loss test.

*Remark: It can be checked, that the test was executed by reading back CFG\_F\_C\_CUT\_TRIGGER in WR\_CONFIG\_1. This bit stays active for the blocking time (specified below). In BoschSPI additionally the C-loss flag in monitor I register can be checked.*

ID	parameter / condition	min	typ	max	unit
4261	Duration of the C-loss test  (After this time the test is finished, but the corresponding monitor flag may be extended depending on the used SPI protocol)	9.5	10	30	µs
4844	C-loss monitor blocking time  After starting the C-loss test, it cannot be started again within the blocking time. After the blocking time the test can be started again	484	513	536	µs



### 5.3.4 Configuration

Filter configuration:

- The FIR filter 3-db frequency can be selected with the "WR\_CONFIG\_1" command. If (X)SOC shall be used, it is mandatory to choose the filter frequency before starting (X)SOC.
- The FIR filter 3-db frequency can be selected as 860Hz, 430Hz, 215Hz, or 53Hz. (Remark: 860Hz filter configuration is not released for SMA720 and SMA760)
- Default = 430Hz.

For SPI Types SMA720 and SMA760 only 430Hz, 215Hz and 53Hz are released.

### 5.3.5 Switch to Normal Operation

After the "WR\_END\_OF\_PROG" command has been sent to the SMA, only read access to the configuration and test registers is possible. The only allowed write access is the "WR\_SOFT\_RESET" command.

Command allowance:

Command	before protocol selection		before SPI voltage selection		before EOP		after EOP	
	Read	Write	Read	Write*	Read	Write	Read	Write
PROT_SEL	x	✓	x	x	x	✓	x	x
MODE	x	x	x	✓	✓	x	✓	x
SENSOR_DATA	x	x	x	x	✓	x	✓	x
SID (only Bosch SPI)	x	x	x	✓	✓	✓	✓	x
OFFSET_REG	x	x	x	x	✓	x	✓	x
OFFSET_CANCELLATION	x	x	x	✓	✓	✓	✓	x
CLOCK_COUNTER	x	x	x	x	✓	x	✓	x
SELFTEST	x	x	x	✓	✓	✓	✓	x
MONITOR_DATA	x	x	x	x	✓	x	✓	x
CONFIG	x	x	x	✓	✓	✓	✓	x
SOFT_RESET	x	x	x	✓	✓	✓	✓	✓
END_OF_PROG	x	x	x	✓	✓	✓	✓	x
RAW_OFFSET	x	x	x	x	✓	✓	✓/x**	x
BITE_REF_VALUE	x	x	x	x	✓	x	x	x
SERIAL	x	x	x	x	✓	x	x	x

\* Commands before voltage mode selection are executed. But no response is send, because SO is in Tristate. Therefore it is not allowed to send any commands, except "voltage mode selection" in this state.

\*\* For CFG\_RAW\_OFS\_CH1/2 read access after EOP is only possible in BoschSPI, but not in SafeSPI. Recommended initialization phase (all non optional steps need to be performed, to be compliant with the safety requirements):

- SPI protocol selection.
- Voltage mode selection.
- Reading monitor register. (optional)
- Reading Device ID.
- Reading 48 bit serial number. (optional)
- Trigger fast offset cancellation (Ch1 / Ch2). (optional)
- Trigger C-loss detection (6.7V mode only)
- Check oscillator frequency.
- Activate and evaluate selftest (Ch1 / Ch2).
- Read acceleration data and evaluate residual offset. (Needs to be compared with applications specific limits)
- Setup the filter frequency (Ch1 / Ch2).
- Setup the slow offset cancellation (Ch1 / Ch2). (optional)
- EOP.



- 5304 • Normal operation (sampling acceleration values).

It is mandatory to choose the filter frequency before starting (X)SOC.

It is not allowed to change between the slow and extra slow offset cancellation. Once one offset cancellation speed has been chosen, it must remain the same.

#### 5.4 Soft Reset

643 To release a Soft Reset, the "WR\_SOFT\_RESET" command must be executed twice consecutively with no other command in between (except "RD\_SOFT\_RESET" itself). If the command was sent only once or any other command is sent in between, no reset will be triggered and the internal counter is set to 0.

5083 In SafeSPI only valid commands between the two softreset commands interrupt the softreset execution. This means, commands with wrong CRC or wrong bit length will have no influence on softreset execution, as there is no bus access with such commands.

In BoschSPI any command (except RD/WR\_SOFT\_RESET), even with wrong CRC or wrong bit length will set the internal counter to 0, as long as it contains at least 8 SCK clock cycles .

5529 Remark: Answer to RD\_SOFTRESET is always 0x0000 (by design).

644 After soft reset all the registers are set to default except for the protocol selection and voltage mode selection and a new initialization phase needs to be performed.

2966 After soft reset the CRC of all internal registers is set to the startup value. The CRC is readable via RD\_Mode command. Initial CRC is already correct --> no CRC-Flag after soft reset.

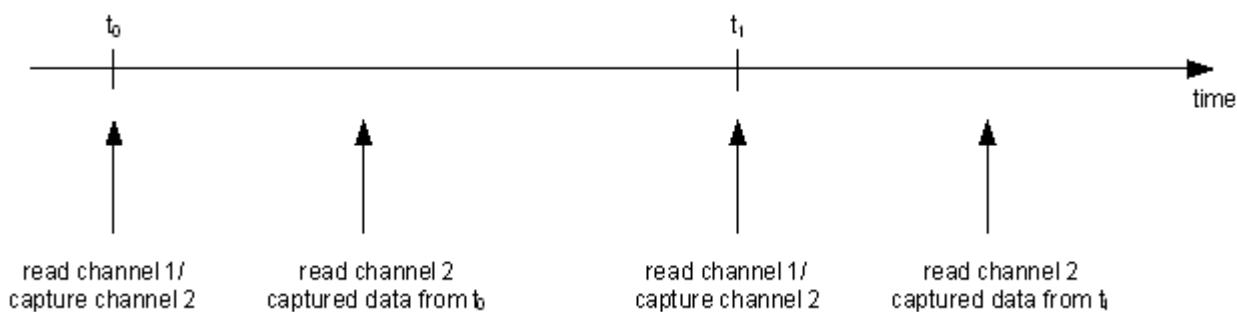
ID	parameter / condition	min	typ	max	unit
4238	Time SO is in tristate after softreset (after this time the sensor is ready for SPI communication)	100		3000	µs
4894	Time the sensor answers with ND or RE flag after soft reset  SafeSPI	3.85	4	4.35	ms
5207	Time the sensor answers with ND flag after hard reset  SafeSPI; supply voltage in spec	3.85	4.2	5.0	ms
4895	Time the sensor answers with GS flag after soft reset  BoschSPI			3.35	ms

#### 5.5 SPI Data Capturing

652 The Bosch SPI protocol features data capturing for the sensor data of channel 2. This means the sensor data of channel 2 is captured (stored in sensor internally) during every channel 1 request and available for read out at a later point in time.

654 With this concept, the sensor data of both channels can be transmitted with the same time stamp of capturing.

655 Sampling scheme of data capturing:



## 5.6 Safe SPI (Out of Frame)

Communication between slave and master is realized by 32bit data word (MSB transmitted first). The maximum transmission rate is 10Mbaud.

A so-called out off frame protocol is used, i.e., each transfer is completed through a sequence of two phases. The answer of a given request is sent within the next frame having the same CSB active.

The CSB active level is low.

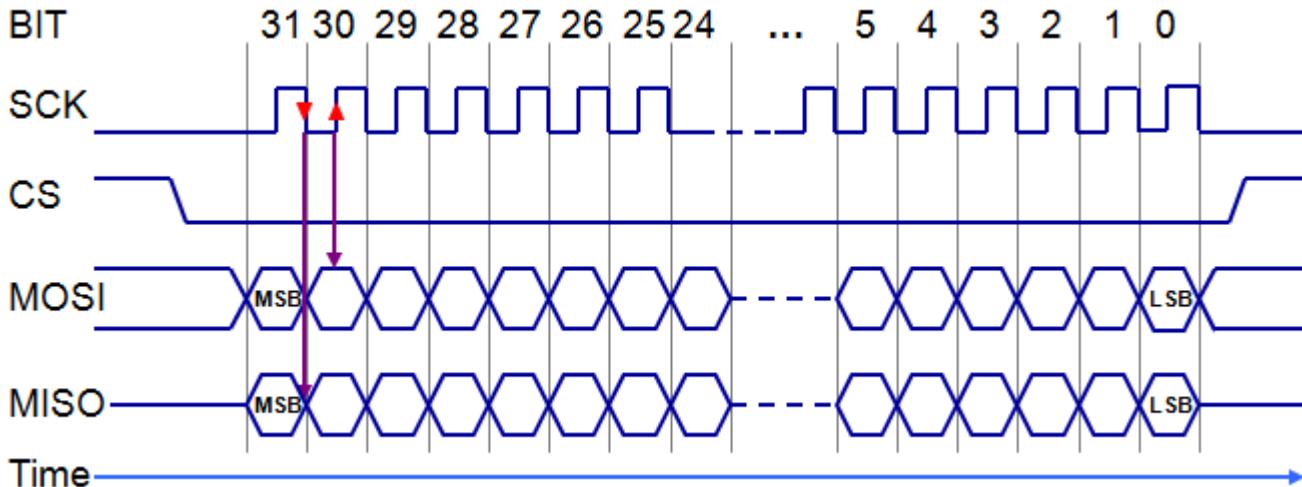
The SCK idle level is low (CPOL = Polarity = 0).

The information at "Slave In" (SI) is taken over by the sensor with the rising edge of SCK, whereas the sensor sets the output level at "Slave out" (SO) with the falling edge of SCK (Phase = 0).

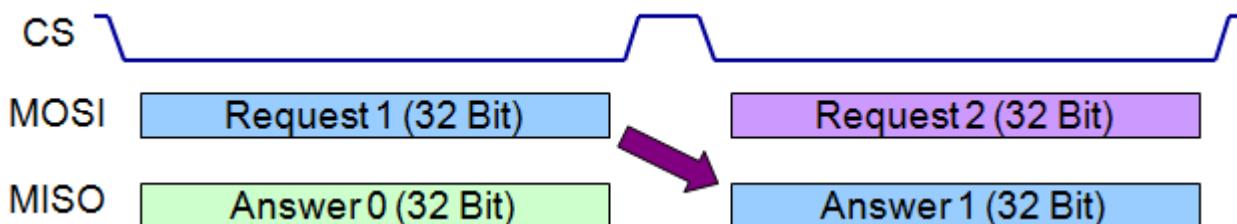
Upon the last falling edge at SCK within each data word, the sensor sets the output SO to low.

Therefore, upon CSB going active for the next transmission the level at SO is always low.

Description of physical layer:



Out of frame sensor answer:

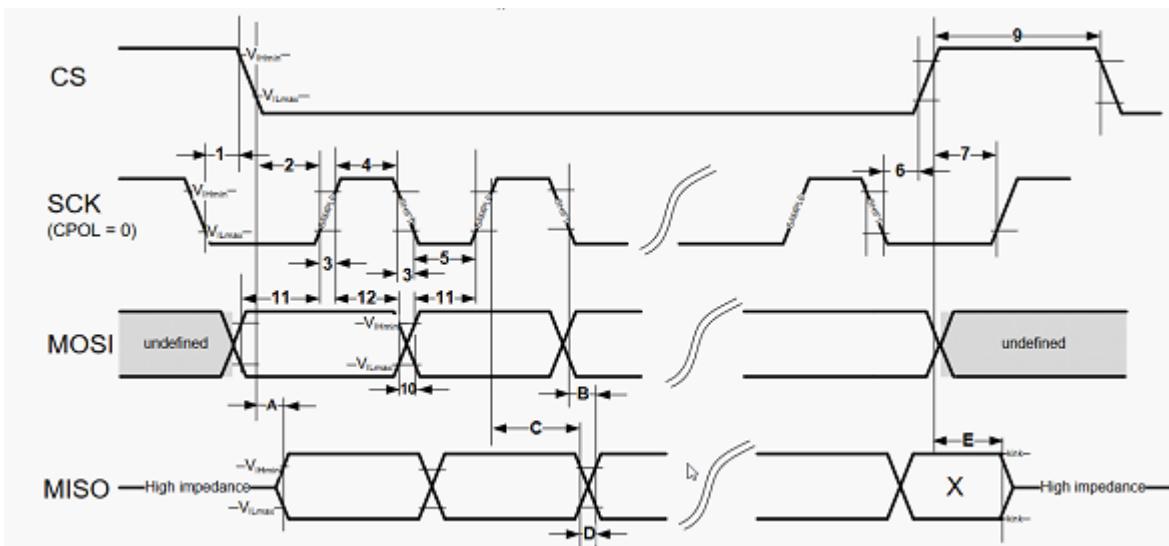


Not used bits in the 16 bit data block of the sensor answer will be "0".

All MOSI Bits noted with "-" are DON'T CARE bits and have no influence.

### 5.6.1 Interface Timing

Safe SPI timing:



ID	parameter / condition	min	typ	max	unit
788	- SPI clock frequency *) fOP	2.5 **)	10	10.5	MHz
791	SCK period = 1/max_SPI_clk as specified in ID 788 *) tSCK	95.2			ns
5523	1 SCK disable lead time for 10 MHz, max load Requirement for master	10			ns
949	2 SCK enable lead time (CPHA = 0) for 10 MHz mode, @ Cload= 100 pF Requirement for master	40			ns
792	3 Clock (SCK) fall time *) C load [0, 100] pF Requirement for master	5		13	ns
793	3 Clock (SCK) rise time *) C load [0, 100] pF Requirement for master	5		13	ns
789	4 Clock (SCK) high time *) as defined by clock duty cycle of 50% and clock rise/fall time tWSCKlh Requirement for master	$\frac{1}{2} \cdot tSCK - 13$			ns
790	5 Clock (SCK) low time *) tWSCKl	$\frac{1}{2} \cdot tSCK - 13$			ns

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<b>ID</b>	<b>parameter / condition</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>unit</b>
	Requirement for master				
801	6 SCK enable lag time *) t <sub>lag</sub> Requirement for master	20			ns
5302	7 SCK disable lag time	10			ns
953	8 Sequential transfer delay, after read access *) for 10 MHz mode, max load Requirement for master	300			ns
954	8 Sequential transfer delay, after write access *) for 10 MHz mode, max load Requirement for master	450			ns
5303	10 MOSI rise/fall time @C_load=100pF Requirement for master	0		13	ns
794	11 Data input (MOSI) setup time *) ts <sub>u</sub>	10			ns
795	12 Data input (MOSI) hold time *) th <sub>i</sub>	20			ns
796	A MISO data valid time (CS) Data output (SO) access time *) Requirement for slave			40	ns
797	B MISO data valid time (SCK) Data output (SO) valid after SCK (@100pF) *) @100 pF Requirement for slave			32	ns
798	C Data output (SO) hold time *) Requirement for slave	0			ns
5301	D MISO rise/fall time @C_load=100pF Requirement for slave	0		16	ns
799	E MISO data disable lag time *) Requirement for slave			50	ns



803

\*) Reference values are 20% and 80% of SPI voltage.

5087

\*\*) Device is also working with lower SPI frequencies. Due to possible noise-issues, it is recommended to use SPI clocks with &gt; 2.5 MHz. Using clock frequencies below can result in higher acceleration signal noise.

668  
672

These commands are used to request acceleration sensor data.

Read sensor data commands (14Bit):

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MOSI	SEN	-	CH1	CH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2	CRC1	CRC0			
	1	-	1/0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1/0	1/0	1/0			
MISO	SEN	-	CH1	CH0	TST	SF3	SF2	SF1	SF0	NRO	-	S1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	-	-	S0	CRC2	CRC1	CRC0
	1	-	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	-	0/1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0/1	1/0	1/0	1/0	

673

MOSI sensor data:

Bit	Name	Description
SEN	Sensor bit	0=non sensor data request 1=Sensor data request
CH_n	Channel select	00=Channel1 01=Channel2 10=na 11=na
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit31...Bit3)

674

MISO sensor data:



Bit	Name	Description
CH_n	Channel select	00=Channel1 01=Channel2 10=na 11=na
S_n	Signal mode	00= Valid data 01=Error (non valid data) 10=not used 11=Initialization data
D_n	Data	Sensor data: 14Bit acceleration data
SF_n	Status flag	0000 = Sensor in normal operation 0001 = SPI transmission error 0010 = request error 0011 = condition not correct 0100 = no data available 0101 = end of programming not set 0110 = undervoltage error of regulator VDDA 0111 = ground loss detection 1000 = undervoltage error of supply VDDI 1001 = undervoltage error of supply VDD
TST	Selftest flag	0=Selftest not active 1=Selftest active
SEN	Sensor bit	0=non sensor data response 1=Sensor data response
NRO	Non regular operation	0= normal operation 1= No regular operation
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit31...Bit3)

5068

Acceleration data is captured from the output of the interpolation filter at the rising edge of CSB of the request frame (applies for sensor commands only).

### 5.6.3 Non-Acceleration Data Commands

676

These commands are used to write/read the sensor control and status registers.

679

In case of an invalid setting (inside the 16-bit data) the sensor ignores the whole command and responds with a request error.

680

Non sensor data read commands:

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
MOSI	SEN	-	OP1	OP0	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	Adr0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2	CRC1	CRC0				
MISO	SEN	0	1	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	-	S1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S0	CRC2	CRC1	CRC0

681

Non sensor data write commands:

	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
MOSI	SEN	0	-	OP1	OP0	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	Adr0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	-	CRC2	CRC1	CRC0	
MISO	SEN	0	1	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	-	S1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S0	CRC2	CRC1	CRC0

682

MOSI non sensor data:



Bit	Name	Description
SEN	Sensor bit	0=non sensor data request 1=Sensor data request
OP_n	Operation Code	00=na 01=Write ASIC register 10=na 11=Read ASIC register
Adr_n	Data	Register/command adress
D_n	Data	Non sensor data write: 16Bit non acceleration data
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit31...Bit3)

683

MISO non sensor data:

Bit	Name	Description
OP_n	Operation Code	00=na 01=Write ASIC register 10=na 11=Read ASIC register
S_n	Signal mode	00= Valid data 01=Error (non valid data) 10=not used 11=Initialization data
D_n	Data	Non sensor data: 16Bit non acceleration data
SF_n	Status flag	0000 = Sensor in normal operation 0001 = SPI transmission error 0010 = request error 0011 = condition not correct 0100 = no data available 0101 = end of programming not set 0110 = undervoltage error of regulator VDDA 0111 = ground loss detection 1000 = undervoltage error of supply VDDI 1001 = undervoltage error of supply VDD
TST	Selftest flag	0=Selftest not active 1=Selftest active
SEN	Sensor bit	0=non sensor data response 1=Sensor data response
NRO	Non regular operation	0= normal operation 1= No regular operation
CRC_n	CRC-Code	3 bit CRC-Code (covering Bit31...Bit3)

#### 5.6.4 CRC Calculation

685

To check integrity of the sensor signals (SO) and commands (SI) to the sensor 3 bit CRC (cyclic redundancy check) is used. There are 29 CRC-relevant data bits (bit 31 to 3) for MISO and MOSI.

ASIL\_D

686

The CRC calculation is specified by:

---

- Polynomial =  $1 + x + x^3$
- Initial value = 0b101
- Target value = 0b000

ASIL\_D

ASIL\_D

ASIL\_D



## 5.6.5 Error Management

The Safe SPI32 frame contains a cumulative failure flag for the monitor flag registers I and II (NRO/S) and a four-bit status flag (SF\_3 – SF\_0).

### 5.6.5.1 SF (Status flags)

691 Status flags:

ASIL\_D

Name	Name long	SF-code (SF_3 - SF_0)	Activation conditions	Failure priority	SF/NRO masks data (all bits "0") [yes=all bits "0"; no=data not masked]
SE	SPI transmission error	0001	set to '1' for request (SI) frame violation (incorrect number of SCK pulses more or less than 32 pulses).	1	yes
			set to '1' for request (SI) CRC violation		acceleration command: yes; other commands: no
			The message including SE has always SEN_bit=0, to mark this frame as a non-acceleration command.		
RE	request error	0010	Set if SPI-command allowance matrix is violated set during the stabilization period after Soft-reset state (response to any non-acceleration command during the stabilization period will be a RE) invalid value written for registers with enumeration fields invalid commands set if C-loss test is running: - for all non-sensor commands, with exception of access to sensor data registers (CFG_DATA_ACC_CH1/2, CFG_DATA_ACC_CH2_CAPT)	2	yes
CNC	condition not correct	0011	set to '1' if sensor data for channel 3 or 4 has been requested (CH1/0 = 0b10 or CH1/0 = 0b11).	3	yes
ND	no data available	0100	set during the stabilization period after hard or soft reset state (response to any acceleration command during the stabilization period will be a ND) set to '1' if sensor data for channel 1 or 2 has been requested while the fast offset cancelation is running. Set if C-loss test is running Set during the stabilization time after change of the cutoff frequency of any channel. Flag stays active for the filter flush times (TST deactivation delay), which are specified in the signal path chapter.	4	yes
EOP	end of programming not set	0101	set as long as EOP is not set.		no
UVA	undervoltage error of internal regulator	0110	set if undervoltage on analog supply (internal) is detected		no
GND	ground loss detection	0111	set if a ground loss is detected	7	no
UVSI	undervoltage error of supply VDDI	1000	set during undervoltage situation at Vddi	8	no
UVS	undervoltage error of supply VDD	1001	set during undervoltage situation at Vdd	9	no

694 All status flags except for the GND (ground loss detection status) stay active as long as the activation condition is present.

ASIL\_D

A ground loss condition (and hence a GND status) is detected during each request or response frame and is not immediately flagged in the same frame. Instead it is latched until the end of the following response or request frame.

4893 If a write command at MOSI is answered with a RE flag, then the value of the addressed register will not change. I.e. a non-valid write request will not only lead to RE flag, but will also never be executed.

### 5.6.5.2 TST (Self test active flag)

696 This flag indicates that the Sensor-Self-Test is active. The flag stays active after the Self-Test was deactivated for the worst-case filter-flush-time of the used filter setting. The deactivation delays are specified in the self test chapter.

ASIL\_D

697 0 = self test is not active

ASIL\_D

1 = self test is/was active



### 5.6.5.3 NRO (Non regular operation flag)

699

Non regular operation flag:

ASIL\_D

Name	Name long	Activation conditions
NRO	no regular operation flag	cumulative error flag of monitor I register, except SOC1/2 flag and for monitor II register, except FOC1/2. Set to '1' if at least one of the following monitor flags is set and the failure condition is still present: OC1, OC2, NoCLK, OTP, Lock, OTP_ECC, EXT_M, CD, ME, DCM or OVSI

### 5.6.5.4 S (Signal mode flag)

702

The signal mode "S" flag is a summary flag: It shows 0b01 ("error data") if NRO bit is set or if status flag is not equal to 0b000 (normal operation) and SF is not equal to 0b0101 (EOP not set). This and all other combinations can be found in this table.

703

Signal mode flag:

ASIL\_D

S_n	Signal mode	00=Valid data: Valid for T ST=0 and NRO=0 and SF_n="0000"
		01=Error: Valid for NRO=1 or (SF?"0000" and SF?"0101")
		10=not used
		11=Initialization data: Valid for (TST=1 or SF="0101") and NRO="0"

### 5.6.5.5 Monitor Register

705

Monitor I register:

ASIL\_D



Position	Name	Name long	Activation conditions	Relevant for acceleration data from channel1	Relevant for acceleration data from channel2	Relevant for no acceleration data
0	OC1	offset cancellation error in channel 1	set if offset cancellation of channel 1 out of limit	yes	no	yes
1	OC2	offset cancellation error in channel 2	set if offset cancellation of channel 2 out of limit	no	yes	yes
2	not used	Not used	Not used	no	no	no
3	not used	Not used	Not used	no	no	no
4	No CLK	no clock	set if clock of on-chip oscillator is absent	yes	yes	yes
5	Not used	Not used	Not used	no	no	no
6	OTP	memory error of OTP data	set if the content of the MEMORY has an error. This error is detected by the cyclic redundancy check.	yes	yes	yes
7	Lock	lockbit error	set if at least one of the OTP lock bits is not set	yes	yes	yes
8	OTP ECC	OTP ECC BIST Error	set if the OTP wrapper detects an error in the ECC BIST logic detected in front of the bootloading process	yes	yes	yes
9	EXT_M	Extended mode	Set if the device is in extended mode or extended test mode (mode for internal test purpose)	yes	yes	yes
10	SOC1	slow offset cancellation inactive in channel 1	set if slow offset cancellation is inactive in channel 1 after EOP <b>no influence on NRO flag</b>	no	no	no
11	SOC2	slow offset cancellation inactive in channel 2	set if slow offset cancellation is inactive in channel 2 after EOP <b>no influence on NRO flag</b>	no	no	no
12	CD	capacity loss detection error	set if C-loss detection is running *1)	yes	yes	yes
13	Not used	Not used	Not used	no	no	no
14	ME	mirror error of device configuration data	set if CRC fails for configuration registers of filter setting, voltage mode selection or protocoll selection	yes	yes	yes
15	DCM	Die edge corrosion monitor	set if the continuous die corrosion monitor detects an open in the monitor via-chain	yes	yes	yes

\*1) Remark: As during C-loss test also the RE/ND-flag is set, the CD-flag cannot be read directly. But it is used, to trigger also the NRO flag during the C-loss test.



<b>Position</b>	<b>Name</b>	<b>Name long</b>	<b>Activation conditions</b>	<b>Relevant for acceleration data from channel1</b>	<b>Relevant for acceleration data from channel2</b>	<b>Relevant for nonacceleration data</b>	<b>NRO masks data (all bits "0") [yes=at bits "1"; no=data not masked]</b>	<b>For non- and acceleration data</b>
0	FOC1	fast offset cancellation active in channel 1	set if fast offset cancellation is running in channel 1	no	no	no	no	
1	FOC2	fast offset cancellation active in channel 2	set if fast offset cancellation is running in channel 2	no	no	no	no	
2	Not used	Not used	Not used	no	no	no	no	
3	Not used	Not used	Not used	no	no	no	no	
4	Not used	Not used	Not used	no	no	no	no	
5	OVSI	over voltage supply (VDDI)	set permanently (until reset) if over voltage is detected at VDDI	no	no	no	no	
6	Not used	Not used	Not used	no	no	no	no	
7	Not used	Not used	Not used	no	no	no	no	
8	Not used	Not used	Not used	no	no	no	no	
9	Not used	Not used	Not used	no	no	no	no	
10	Not used	Not used	Not used	no	no	no	no	
11	Not used	Not used	Not used	no	no	no	no	
12	Not used	Not used	Not used	no	no	no	no	
13	Not used	Not used	Not used	no	no	no	no	
14	Not used	Not used	Not used	no	no	no	no	
15	Not used	Not used	Not used	no	no	no	no	

707

All monitor bits stay active as long as the failure mode is present.

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### 5.6.6 Instruction Set

710

Instruction Overview:


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 1.279.929.850

Name	Description	Header	16 bit Data (in case of "read" commands only for sensor response; "don't care" bits are "0" in the sensor response)															
WR_PROT_SEL	protocol selection to switch between Bosch SPI and Open SPI	0x00F	Hex = 0xFF00FF															
WR_MODE	voltage mode selection	0x140	voltage mode															
RD_MODE	read voltage and protocol mode	0x340	Register CRC															
RD_DEVICE_ID	read device ID	0x342	extended device ID															
RD_REVISION_ID	read revision ID	0x344	device ID															
RD_SENSOR_DATA_CH1	read sensor data of channel 1 (14Bit)	0x800	revision ID															
RD_SENSOR_DATA_CH2	read sensor data of channel 2 (14Bit)	0x900	S1_13 - S1_0															
RD_OFFSET_REG_CH1	read the register with the current offset cancellation value	0x352	S2_13 - S2_0															
RD_OFFSET_REG_CH2	read the register with the current offset cancellation value	0x354	16 bit offset data															
WR_OFFSET_CANCELLATION	trigger FOC/SOC	0x158	16 bit offset data															
RD_OFFSET_CANCELLATION	read the status of the offset cancellation	0x358	OC length2															
RD_CLOCK_COUNTER	read the current value of the clock counter	0x35A	OFF2															
WR_TEST_MODE	trigger build in self test	0x162	OC length1															
RD_TEST_MODE	read the status of the build in selftest	0x362	OFF1															
RD_MONITOR_I_DATA	read monitor 1 data	0x364	TMD2															
RD_MONITOR_II_DATA	read monitor 2 data	0x366	TMD1															
WR_CONFIG_1	write configuration for C-loss detection and oscillator monitoring	0x168	Monitor I flags															
RD_CONFIG_1	read configuration for C-loss detection and oscillator monitoring	0x358	Monitor II flags															
WR_SOFT_RESET	reset of the component (SO only for the first transmission)	0x16E	Filter2															
WR_END_OF_PROG	locking command, after EOP only read commands allowed, also DEMAND_SOFT_RESET	0x170	Filter1															
RD_BITE_CH1	read BITE OTP value of channel 1	0x31A	End of programming															
RD_BITE_CH2	read BITE OTP value of channel 2	0x31C	positive BITE OTP channel CH1															
RD_RAW_OFFSET_CH1	read RAW OFFSET OTP value of channel 1	0x3XX	negative BITE OTP channel CH1															
RD_RAW_OFFSET_CH2	read RAW OFFSET OTP value of channel 2	0x3XX	positive BITE OTP channel CH2															
RD_SERIAL1	read serial number bit15 - bit0	0x300	RAW OFFSET OTP channel CH2															
RD_SERIAL2	read serial number bit31 - bit16	0x302	serial number (SN15 - SN0)															
RD_SERIAL3	read serial number bit47 - bit32	0x304	serial number (SN31 - SN16)															

711 Note: Headers are bits 31-20 of MOSI commands.

### 5.6.6.1 WR\_PROT\_SEL

713 WR\_PROT\_SEL: protocol selection to switch between Bosch SPI 0xFF00FF00 and Safe SPI 0x00FF00FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

### 5.6.6.2 WR\_MODE

715 WR\_MODE: set voltage mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SI	0	-	0	1	0	1	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0	-			
SO	-	-	0	1	TST	SF3 - SF0	NRO	-	S1	Reg CRC																0	0	0	PRO	voltage mode	S0	CRC2 - CRC0

#### Voltage Mode:

0010: Supply = 4.5V-11V (Vdd); SPI = 3.3V (14Bit sensor data)

0100: Supply = 4.5V-11V (Vdd); SPI = 3.3V (14Bit sensor data)

1000: Supply = 3.13V-3.47V (Vdd); SPI = 3.3V (14Bit sensor data)

all other combinations = not allowed --> no voltage mode selected (SO stay in tristate)

#### PRO:

0: Bosch SPI

1: Safe SPI

#### Reg CRC:

Contains the CRC for error detection within the configuration registers

### 5.6.6.3 RD\_MODE

717 RD\_MODE: read voltage and protocol mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0	-		
SO	-	1	1	TST	SF3 - SF0	NRO	-	S1	Reg CRC																0	0	0	PRO	voltage mode	S0	CRC2 - CRC0

#### Voltage Mode:

0010: Supply = 4.5V-11V (Vdd); SPI = 3.3V (14Bit sensor data)



0100: Supply = 4.5V-11V (Vdd); SPI = 3.3V (14Bit sensor data)  
 1000: Supply = 3.3V (Vddi); SPI = 3.3V (14Bit sensor data)

**PRO:**

0: Bosch SPI

1: Safe SPI

**Req\_CRC:**

Contains the CRC for error detection within the configuration registers

**5.6.6.4 RD\_DEVICE\_ID**

719

RD\_DEVICE\_ID: read device ID

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	extended device ID										device ID										S0	CRC2 - CRC0	

**Extended device ID:**

individual value for each member of SMA7 family

**Device ID:**

fix value for SMA7 family

**5.6.6.5 RD\_REVISION\_ID**

721

RD\_REVISION\_ID: read revision ID

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	0	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S0	CRC2 - CRC0		

**5.6.6.6 RD\_SENSOR\_DATA\_CH1 (14bit)**

727

RD\_SENSOR\_DATA\_CH1: read sensor data of channel 1 (clipping to +/-8191LSB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	1	-	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	1	-	0	0	TST	SF3 - SF0	NRO	-	S1	S1_13 - S1_0										0	0	S0	CRC2 - CRC0									

**5.6.6.7 RD\_SENSOR\_DATA\_CH2 (14bit)**

729

RD\_SENSOR\_DATA\_CH2: read sensor data of channel 2 (clipping to +/-8191LSB)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	1	-	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	1	-	0	1	TST	SF3 - SF0	NRO	-	S1	S1_13 - S1_0										0	0	S0	CRC2 - CRC0									

**5.6.6.8 RD\_OFFSET\_REG\_CH1**

731

RD\_OFFSET\_REG\_CH1: read the register with the current offset cancellation value (Register will be changed by FOC &amp; SOC)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	1	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	16 bit offset data										0	0	S0	CRC2 - CRC0									

The 16bit refer to the 16 MSB of the 20bit Offsetregister. The 4 LSB of the register are not transmitted (no rounding applied).

Please note, that the initial static raw offset correction value is not included in this register. The initial value can be read with RD\_RAW\_OFFSET.



## 5.6.6.9 RD\_OFFSET\_REG\_CH2

733

RD\_OFFSET\_REG CH2: read the register with the current offset cancellation value (Register will be changed by FOC &amp; SOC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	1	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0		
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	16 bit offset data																S0	CRC2 - CRC0				

The 16bit refer to the 16 MSB of the 20bit Offsetregister. The 4LSB of the register are not transmitted (no rounding applied).

Please note, that the initial static raw offset correction value is not included in this register. The initial value can be read with RD\_RAW\_OFFSET.

3949

Conversion of 16 bit offset data channel to sensor output values:

Conversion factor is 2 for 14bit SPI sensor output. This means the SPI output has two times the sensitivity (in LSB/g) than the value read from the offset register.

example: "16 bit offset data channel 2"=200 LSB ==> 400 LSB sensor channel output correction value at SPI interface

## 5.6.6.10 WR\_OFFSET\_CANCELLATION

735

WR\_OFFSET\_CANCELLATION: start FOC or SOC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	0	1	0	1	0	1	1	0	0	0	-	-	-	-	-	OC length 2	OFF2	OC length 1	OFF1	-	CRC2 - CRC0								
SO	0	-	0	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	OC length 2	OFF2	OC length 1	OFF1	S0	CRC2 - CRC0								

OFF1:

00: offset cancellation channel 1 switched off -->default

01: slow offset cancellation channel 1 switched on (SOC)

10: slow offset cancellation channel 1 switched on (XSOC)

11: fast offset cancellation channel 1 switched on

OFF2:

00: offset cancellation channel 2 switched off -->default

01: slow offset cancellation channel 2 switched on (SOC)

10: slow offset cancellation channel 2 switched on (XSOC)

11: fast offset cancellation channel 2 switched on

OC length1&2:

000: 64 samples --> default

001: 128 samples

010: 256 samples

011: 512 samples

100: 1024 samples

all other values are not executed and lead to a RE

## 5.6.6.11 RD\_OFFSET\_CANCELLATION

737

RD\_OFFSET\_CANCELLATION: read the status of the offset cancellation

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	1	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0		
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	OC length 2	OFF2	OC length 1	OFF1	S0	CRC2 - CRC0								

OFF1:

00: offset cancellation channel 1 switched off

01: slow offset cancellation channel 1 switched on (SOC)

10: slow offset cancellation channel 1 switched on (XSOC)

11: fast offset cancellation channel 1 switched on

OFF2:



- 00: offset cancellation channel 2 switched off  
 01: slow offset cancellation channel 2 switched on (SOC)  
 10: slow offset cancellation channel 2 switched on (XSOC)  
 11: fast offset cancellation channel 2 switched on

OC length1&2:

- 000: 64 samples  
 001: 128 samples  
 010: 256 samples  
 011: 512 samples  
 100: 1024 samples

all other values are not executed and lead to a RE

## 5.6.6.12 RD\_CLOCK\_COUNTER

739

RD\_CLOCK\_COUNTER: read the current value of the clock counter register

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	1	1	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1																					S0	CRC2 - CRC0	

Counter frequency = 2.25MHz

## 5.6.6.13 WR\_TEST\_MODE

753

WR\_TEST\_MODE: trigger build in self test

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	0	1	0	1	1	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	TMD2	TMD1	-	CRC2 - CRC0					
SO	0	-	0	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMD2	TMD1	S0	CRC2 - CRC0				

TMD1:

- 00: switch off self test channel 1 -->default  
 01: pos. amplitude of self test channel 1  
 10: neg. amplitude of self test channel 1  
 11 = not defined --> RE

TMD2:

- 00: switch off self test channel 2 -->default  
 10: pos. amplitude of self test channel 2  
 01: neg. amplitude of self test channel 2  
 11 = not defined --> RE

## Remark:

Self test of channel 1 and 2 can be de/activated within one command. Please note the different bit value for pos./neg. amplitude for ch1/2.

## 5.6.6.14 RD\_TEST\_MODE

755

RD\_TEST\_MODE: read the status of the build in self test

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	1	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0				
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMD2	TMD1	S0	CRC2 - CRC0				

TMD1 :

- 00: switch off test channel 1  
 01: pos. amplitude of self test channel 1  
 10: neg. amplitude of self test channel 1

TMD2:



00: switch off test channel 2  
 10: pos. amplitude of self test channel 2  
 01: neg. amplitude of self test channel 2

### 5.6.6.15 RD\_MONITOR\_I\_DATA

757 RD\_MONITOR\_I\_DATA: read the monitor I register

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	1	0	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0				
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1																				S0	CRC2 - CRC0		

### 5.6.6.16 RD\_MONITOR\_II\_DATA

759 RD\_MONITOR\_II\_DATA: read the monitor II register

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	1	0	0	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0				
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S0	CRC2 - CRC0		

### 5.6.6.17 WR\_CONFIG\_1

761 WR\_CONFIG\_1: write configuration for C-loss and Filter setting:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	0	1	0	1	1	0	1	0	0	0	-	-	-	-	-	-	-	-	DCM_DIS	C_loss	-	Filter 2	Filter 1	-	CRC2 - CRC0					
SO	0	-	0	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S0	CRC2 - CRC0		

#### C-loss:

0 = no initial C-loss detection running -->default

1 = activation of initial C-loss detection (Stays active for typ. 513µs after triggering. This is a blocking time until the C-loss test can be started again. Any further write access during the blocking time has no effect. After the blocking time the test can be started again.)

#### DCM-DIS (disable die corrosion monitor):

0= DCM activated (default)

1= DCM deactivated (not released, do not use)

#### Filter 1 (filter frequency of channel 1):

00 = 430 Hz --> default

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

#### Filter 2 (filter frequency of channel 2):

00 = 430 Hz --> default

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

### 5.6.6.18 RD\_CONFIG\_1

763 RD\_CONFIG\_1: read configuration for C-loss and Filter setting:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	1	0	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0				
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S0	CRC2 - CRC0		

#### C-loss:

0 = no initial C-loss detection running



1 = initial C-loss detection is currently running (Stays active for typ. 513µs after triggering. This is a blocking time until the C-loss test can be started again. )

#### DCM-DIS (disable die corrosion monitor):

0 = DCM activated (default)

1 = DCM deactivated (not released, do not use)

#### Filter 1 (filter frequency of channel 1):

00 = 430 Hz

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

#### Filter 2 (filter frequency of channel 2):

00 = 430 Hz

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

#### 5.6.6.19 WR\_SOFT\_RESET

769

**WR\_SOFT\_RESET:** reset of the component (SO only for the first transmission); has to be sent 2 times

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	-	CRC2 - CRC0		
SO	0	-	0	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S0	CRC2 - CRC0			

0x16e00ad4

#### 5.6.6.20 WR\_END\_OF\_PROG

771

**WR\_END\_OF\_PROG:** locking command, after EOP only read commands allowed (except WR\_SOFT\_RESET)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	0	1	0	1	1	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	CRC2 - CRC0		
SO	0	-	0	1	TST	SF3 - SF0	NRO	-	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	S0	CRC2 - CRC0		

#### 5.6.6.21 RD\_BITE\_CH1

773

**RD\_BITE\_CH1:** read BITE OTP value of channel 1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
SI	0	-	1	1	0	0	0	1	1	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0						
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	positive BITE OTP channel CH1												negative BITE OTP channel CH1												S0	CRC2 - CRC0

positive BITE OTP channel CH1 / negative BITE OTP channel CH1:

**SMA720/773:**

-32g...+31g: end-of-line saved BITE values in 4LSB/g (signed value; two's complement)

example: 0b10110100 (Bit19...Bit12) ==> -19g

**SMA760/774:**

-64g...+63g: end-of-line saved BITE values in 2LSB/g (signed value; two's complement)

example: 0b10110100 (Bit11...Bit4) ==> -38g

**All other variants:**

-256g...+254g: end-of-line saved BITE values in 0.5LSB/g (signed value; two's complement)

#### 5.6.6.22 RD\_BITE\_CH2

775

**RD\_BITE\_CH2:** read BITE OTP value of channel 2

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
SI	0	-	1	1	0	0	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0						
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	positive BITE OTP channel CH2												negative BITE OTP channel CH2												S0	CRC2 - CRC0



positive BITE OTP channel CH1 / negative BITE OTP channel CH1:

**SMA720/773:**

-32g...+31g: end-of-line saved BITE values in 4LSB/g (signed value; two's complement)  
example: 0b10110100 (Bit19...Bit12) ==> -19g

**SMA760/774:**

-64g...+63g: end-of-line saved BITE values in 2LSB/g (signed value; two's complement)  
example: 0b10110100 (Bit11...Bit4) ==> -38g

**All other variants:**

-256g...+254g: end-of-line saved BITE values in 0.5LSB/g (signed value; two's complement)

### 5.6.6.23 RD\_RAW\_OFFSET\_CH1

777 RD\_RAW\_OFFSET\_CH1: read RAW OFFSET OTP value of channel 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	0	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	RAW OFFSET OTP channel CH1																		0	0	S0	CRC2 - CRC0

14 bit raw offset data channel 1:

Raw offset is stored with 32LSB/g

### 5.6.6.24 RD\_RAW\_OFFSET\_CH2

779 RD\_RAW\_OFFSET\_CH2: read RAW OFFSET OTP value of channel 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	1	0	1	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	RAW OFFSET OTP channel CH2																		0	0	S0	CRC2 - CRC0

14 bit raw offset data channel 2:

Raw offset is stored with 32LSB/g

### 5.6.6.25 RD\_SERIAL1

781 RD\_SERIAL1: read serial number I

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	serial number (SN15 - SN0)																		S0	CRC2 - CRC0		

### 5.6.6.26 RD\_SERIAL2

783 RD\_SERIAL2: read serial number II

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	0	0	0	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	serial number (SN31 - SN16)																		S0	CRC2 - CRC0		

### 5.6.6.27 RD\_SERIAL3

785 RD\_SERIAL3: read serial number III

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	-	1	1	0	0	0	0	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC2 - CRC0			
SO	0	-	1	1	TST	SF3 - SF0	NRO	-	S1	serial number (SN47 - SN32)																		S0	CRC2 - CRC0		

## 5.7 Bosch SPI (In Frame)

805 Communication between slave and master is realized by 32bit data word (MSB transmitted first).

806 The maximum transmission rate is 10Mbaud.

807 An in-frame protocol is used. The answer of a given request is sent immediately within the same frame.

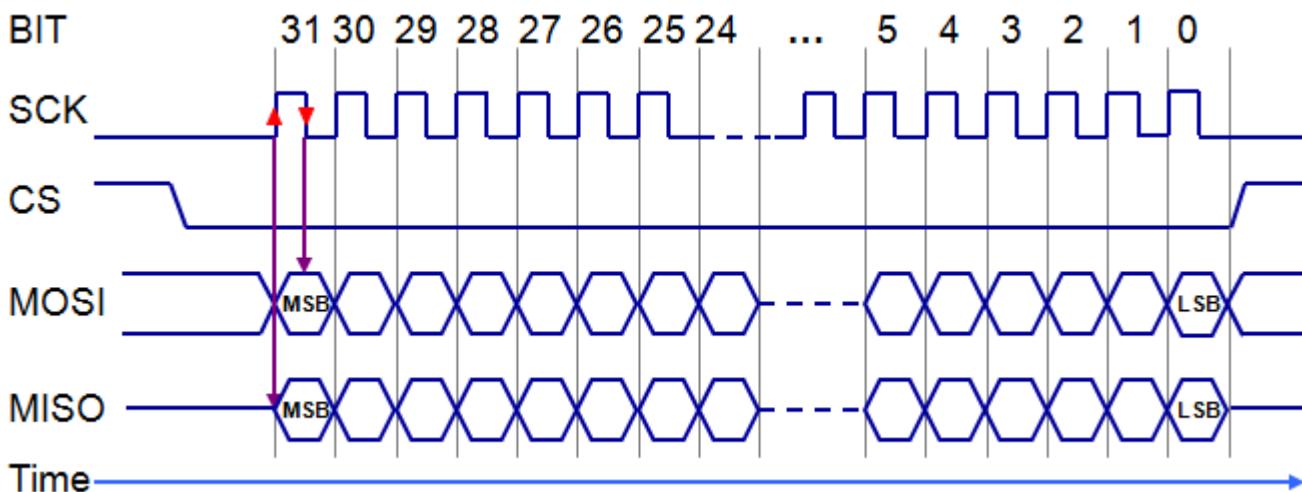
808 The CSB active level is low.

809 The SCK idle level is low (Polarity = 0).

810 The information at "Slave In" (SI) is taken over by the sensor with the falling edge of SCK, whereas the sensor sets the output level at "Slave out" (SO) with the rising edge of SCK (Phase = 1).

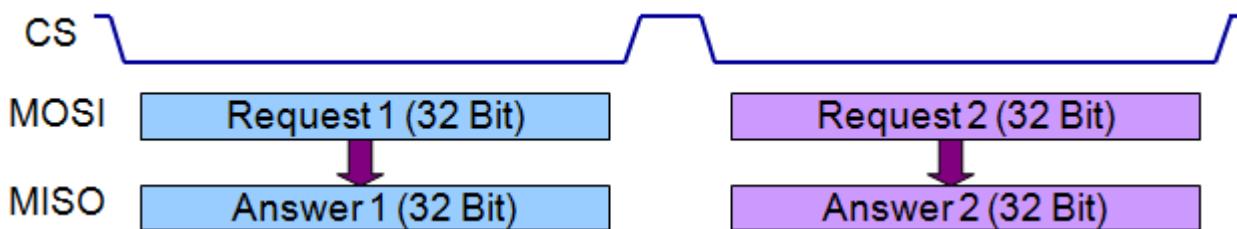


Description of physical layer:



812

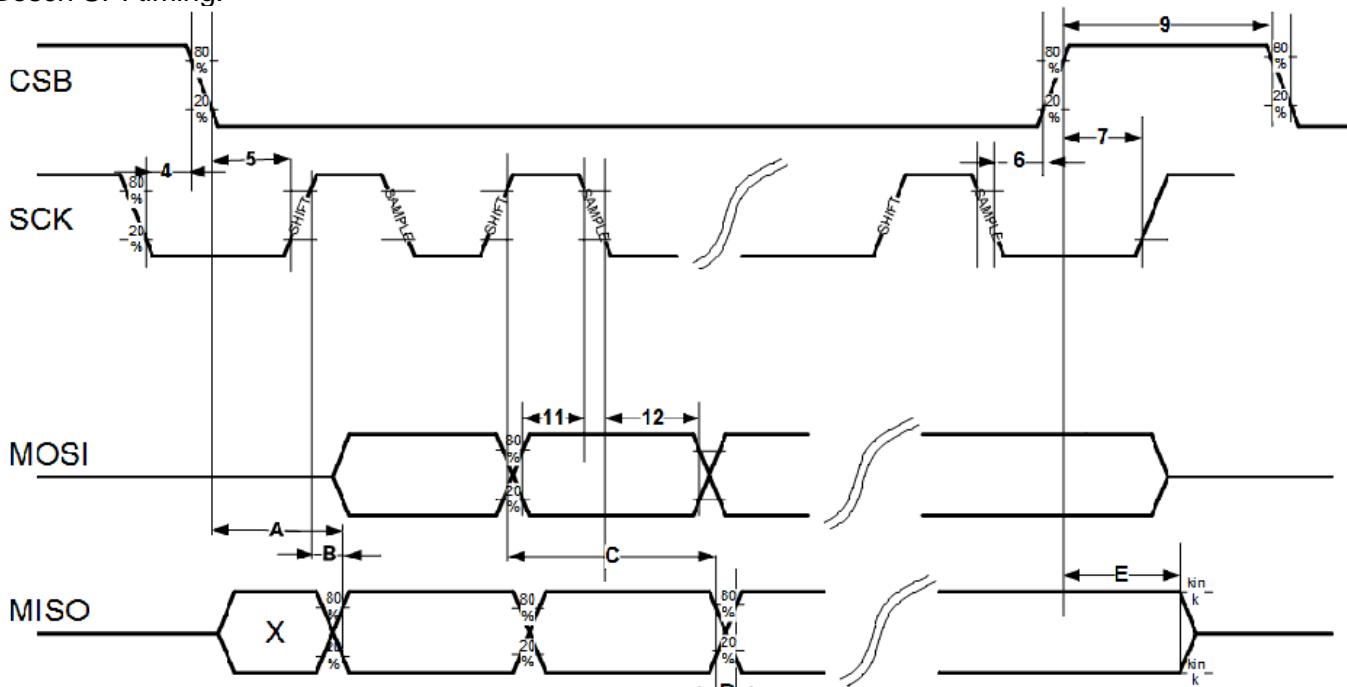
In frame sensor answer:



### 5.7.1 Interface Timing

941

Bosch SPI timing:



ID	parameter / condition	min	typ	max	unit
942	- SPI clock frequency	2.5 *)	10	10.5	MHz
943	A SO data valid time (CSB) minimum drive frequency			40	ns



ID	parameter / condition	min	typ	max	unit
944	B SO data valid time (SCK) C_load = 100 pF			32	ns
945	C SO data hold time minimum drive frequency	half clock period + switch time			ns
946	D SO rise / fall time minimum drive frequency			15	ns
947	E SO data disable lag time minimum drive frequency			50	ns
948	4 SCK disable lead time for 10 MHz, max load	10			ns
950	5 SCK enable lead time (CPHA = 1) for 10 MHz, max load	95		500000 *)	ns
951	6 SCK enable lag time for 10 MHz, max load	95			ns
952	7 SCK disable lag time for 10 MHz, max load	10			ns
955	9 Sequential transfer delay Bosch SPI for read and write access  for 10 MHz, max load	200			ns
4867	9 Sequential transfer delay Bosch SPI in case of unsuccessful write request  (This time is required for proper generation of TFF-flag in the next frame. If this time is not observed then TFF-flag can be delayed until the 2nd frame following the write error) for 10 MHz, max load;	410			ns
957	11 SI data setup time for 10 MHz mode, max load	10			ns
958	12 SI data hold time for 10 MHz mode, max load	20			ns

5088

\*) Device is also working with lower SPI frequencies. Due to possible noise-issues, it is recommended to use SPI clocks with > 2.5 MHz. Using clock frequencies below can result in higher acceleration signal noise.

FRT is not valid with lower SPI frequencies, in this cases with lower frequencies is one SPI frame with corrupted data possible.



### 5.7.2 Acceleration Data Commands

These commands are used to request sensor data.

Not used bits in the 16 bit data block of the sensor answer will be "0".

Not used bits in the SI request are don't care (displayed as "0" and gray background).

Read sensor data commands (14Bit):

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	S	channel	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0			
SO	status	S	SID																							0	0	gs	CRC		

MOSI sensor data:

Bit	Name	Description
S	Sensor bit	0 = non sensor data request 1 = Sensor data request
CH	Channel select	00000 = Channel1 10000 = Channel2 10001 = Channel2 captured
CRC	CRC-Code	3 bit CRC-Code (covering bit 5 to bit 31)

MISO sensor data:

Bit	Name	Description
status	Status flags	Bit 31 = TFF Bit 30 = TST Bit 29 = EOP Bit 28 = 0 (not used) Bit 27 = TF (Temporary fault) Bit 26 = PF (Permanent fault)
S	Sensor bit	0 = Non sensor data request 1 = Sensor data request
SID	sensor ID	Programmable identifier for sensordata CH1/2
data	Acceleration data	14 bit Acceleration data (two's complement) in 16 bit block
gs	general status	0 = normal operation 1 = No regular operation (Monitor flag active)
CRC	CRC-Code	3 bit CRC-Code (covering bit 3 to bit 26)

Acceleration data is captured from the output of the interpolation filter when the 23rd bit of the request frame has been received (applies for data request frames)

### 5.7.3 Non-Acceleration Data Commands

These commands are used to write/read the sensor control and status registers.

Not used bits in the SI request are don't care (displayed as "0" and gray background).

Non sensor data read commands:

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SI	S	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	status	S	0	0	0	0	0	0																		16 bit output data	0	gs	CRC		

Non sensor data write commands:

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SI	S	Adr7	Adr6	Adr5	Adr4	Adr3	Adr2	Adr1	1	0	0																16 bit input data	CRC	0	0			
SO	status	S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC

MOSI non sensor data:



Bit	Name	Description
S	Sensor bit	0 = non sensor data request 1 = Sensor data request
instruction	instruction	Adr7 to Adr1 corresponding to bit 7 to bit 1 of address; Last bit (Adr0) of address is omitted
data	Data	16 bit non acceleration data (don't care for read access)
CRC	CRC-Code	3 bit CRC-Code (covering bit 5 to bit 31)

826

MISO non sensor data:

Bit	Name	Description
status	Status flags	Bit 31 = TFF Bit 30 = TST Bit 29 = EOP Bit 28 = 0 (not used) Bit 27 = TF (Temporary fault) Bit 26 = PF (Permanent fault)
S	Sensor bit	0 = non sensor data request 1 = Sensor data request
data	Data	16 bit non acceleration data (don't care for write access)
gs	general status	0 = normal operation 1 = Sensor defect / no regular operation (Monitor flag active)
CRC	CRC-Code	3 bit CRC-Code (covering bit 3 to bit 26)

## 5.7.4 CRC Calculation

828

To check integrity of the sensor signals (SO) and commands (SI) to the sensor 3 bit CRC (cyclic redundancy check) is used. There are 27 CRC-relevant data bits (bit 31 to 5 for MOSI and bits 26 to 3 for MISO).

ASIL\_D

829

The CRC calculation is specified by:

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830

- Polynomial =  $1 + x + x^3$
- Initial value = 0b111
- Target value = 0b000

ASIL\_D

831

ASIL\_D

832

ASIL\_D

## 5.7.5 Error Management

### 5.7.5.1 TFF (Transfer Failure Flag)

835

This flag indicates that an error occurred in the last SPI transmission.

ASIL\_D

836

Possible errors that lead to this are:

---

837

- SPI frame doesn't have 32 SCK pulses
- Transmitted bus address is not part of the address space
- Transmitted bus address is protected in the current mode
- Write of an illegal setting into a register with an enumerated value field
- CRC of transmitted command at SI is wrong
- internal bus error ( read access on the bus failed or bus timing error happened)
- command is unknown / undefined

ASIL\_D

838

ASIL\_D

839

ASIL\_D

3018

ASIL\_D

4149

ASIL\_D

4151

ASIL\_D

4152

ASIL\_D

0 = No error detected

ASIL\_D

1 = Error detected

840

If a write command at MOSI is answered with a TFF, then the value of the addressed register will not change. I.e. a non-valid write request will not only lead to TFF, but will also never be executed.

### 5.7.5.2 CRC toggling

4155

CRC toggling inverts the last bit of the CRC of the sensor answer to generate a wrong CRC.

4154



4156

CRC toggling is done everytime a TFF flag is generated, except in the case of a SPI frame, which does not have 32 SCK pulses and except if an EOP command is send during running FOC.

CRC toggling is done in the same frame as the error condition occurred, whereas the TFF flag is generated in the next frame.

842

This flag indicates that the Sensor-Self-Test is active. The flag stays active for both channels for the worst-case filter flush time of the selected filters after the Self-Test was deactivated.

843

0 = self test is not active  
1 = self test is/was active

ASIL\_D

845

This flag indicates that the EOP-command was not sent during the power-on-cycle. After the EOP-command was sent, the ECU has only a limited access to the internal registers.

846

0 = End Of Programming transmitted  
1 = End Of Programming not transmitted

ASIL\_D

ASIL\_D

848

This flag indicates that a temporary fault is active.

849

0 = No error detected  
1 = Error detected

ASIL\_D

ASIL\_D

851

This flag indicates that a permanent fault is active.

852

0 = No error detected  
1 = Error detected

4158

The PF has a higher priority then the TF flag. Therefore the TF flag will not be transmitted anymore in case of a permanent fault.

ASIL\_D

ASIL\_D

854

General status flag:

ASIL\_D

Name	Name long	Activation conditions
gs	general status flag	cumulative error flag of monitor I and II register (set to '1' if at least one of the monitor flags is set and the failure condition is still present) Also set after change of filter frequency and softreset to mark temporary invalid sensor data.

855

The GS-flag is not set if a latched monitor flag is active but the failure mode is not present anymore (except the delay extension, see "Remark delayed GS flag"). It is also not set if SOC1 or SOC2 is active. The GS flag is also used to mark invalid sensor data after softreset and after changes of the FIR filter frequency setting. I.e. after changing the filter frequency of at least one channel, the GS flag is set and stays active for the filter flush times of the new filter setting. If two different filter settings are chosen for the two channels, the sensor uses the filter setting with the lower cornerfrequency to determine filter flush time. E.g. setting Ch1 to 430Hz and Ch2 to 53Hz will lead to a GS flag, which is active for the flush time of the 53Hz filter.

ASIL\_D

4832

The sensor data during this period maybe wrong, due to an offset error, which appears during the change of the filter setting.

The filter flush times (TST flag deactivation delay) are specified in the TST flag chapter above.



## 5.7.5.8 Monitor Register

857

ASIL\_D

## Monitor I register:

Position	Name	Name long	Activation conditions	General Status Flag (GS)	Flag delayed	Temporary Fault (TF)	Permanent Fault (PF)	Latched until readout
0	OC1	offset cancellation error in channel 1	set if offset cancellation of channel 1 out of limit	yes	no	yes	no	yes
1	OC2	offset cancellation error in channel 2	set if offset cancellation of channel 2 out of limit	yes	no	yes	no	yes
2	not used	not used	not used	no	no	no	no	no
3	not used	not used	not used	no	no	no	no	no
4	No CLK	no clock	set if clock of on-chip oscillator is absent	yes	no	no	no	no
5	Not used	Not used	Not used	no	no	no	no	no
6	OTP	memory error of OTP data	set if the content of the MEMORY has an error. This error is detected by the cyclic redundancy check.	yes	no	no	yes	no
7	Lock	lockbit error	set if at least one of the OTP lock bits is not set	yes	no	no	yes	no
8	OTP ECC	OTP ECC Bist Error	set if the OTP wrapper detects an error in the ECC BIST logic detected in front of the bootloading process	yes	no	no	yes	no
9	EXT_M	Extended mode	Set if device is in extended mode or extended test mode (mode for internal test purpose)	yes	no	yes	no	yes
10	SOC1	slow offset cancellation channel 1	Set if slow offset cancellation of channel 1 is not active	no	no	no	no	no
11	SOC2	slow offset cancellation channel 2	Set if slow offset cancellation of channel 2 is not active	no	no	no	no	no
12	CD	capacity loss detection error	Set when C-loss test is triggered and stays active when the test is running.	yes	yes	yes	no	yes
13	Not used	Not used	Not used	no	no	no	no	no
14	ME	mirror error of device configuration data	set if CRC fails for configuration registers of filter setting, voltage mode selection or protocol selection	yes	no	no	yes	no
15	DCM	Die edge corrosion monitor	Set if the continuous die edge corrosion monitor detects an open in the via chain	yes	no	yes	no	yes

858

ASIL\_D

## Monitor II register:



Position	Name	Name long	Activation conditions	General Status Flag (GS)	Flag delayed	Temporary Fault (TF)	Permanent Fault (PF)	Latched until readout
0	EOP	end of programming	end of programming command not sent	yes	no	yes	no	no
1	UVS	undervoltage error of supply VDD	set during undervoltage situation at Vdd	yes	yes	yes	no	yes
2	UVSI	undervoltage error of supply VDDI	set during undervoltage situation at Vddi	yes	yes	yes	no	yes
3	UVA	undervoltage error of regulator VDDA	set if undervoltage on analog supply (internal) is detected	yes	yes	yes	no	yes
4	GND_EXT	External GND loss detected	Set if connection between GND pin and PCB GND is lost	yes	yes	yes	no	yes
5	OVSI *)	Ovvoltage VDDI	Set if overvoltage at VDDI pin is detected	yes	yes	yes	no	yes
6	GND_MEMS	MEMS GND loss detected	Set if GND connection between MEMS and ASIC is broken	yes	yes	yes	no	yes
7	Not used	Not used	Not used	no	no	no	no	no
8	FOC_Busy_CH1	Fast offset cancellation channel 1 busy	set if fast offset cancellation channel 1 is busy	yes	no	yes	no	yes
9	FOC_Busy_CH2	Fast offset cancellation channel 2 busy	set if fast offset cancellation channel 2 is busy	yes	no	yes	no	yes
10	Not used	Not used	Not used	no	no	no	no	no
11	Not used	Not used	Not used	no	no	no	no	no
12	Not used	Not used	Not used	no	no	no	no	no
13	Not used	Not used	Not used	no	no	no	no	no
14	Not used	Not used	Not used	no	no	no	no	no
15	Not used	Not used	Not used	no	no	no	no	no

\*) this flag is only readable in testmode. During normal operation with inframe protocol the sensor disables the SPI communication (SO in tristate), if an overvoltage at VDDI is detected. This is done to protect the ECU receiver circuit against overvoltage at SO pin.

859

All monitor bits stay active as long as the failure mode is present. After the failure mode disappears, latched flags (column "Latched until readout" = "yes") will be only reset to "0" after reading the monitor register at least one time. Not latched flags (column "Latched until readout" = "no") are reset to "0", once the failure mode disappears.

ASIL\_D

860

If the error flag has an influence on the signal path, the active phase of this flag and of the GS-flag will be extended (see table of monitor flags "Flag delayed"). The extension starts after the original error is no more there and will stay active for times specified below.

4846

The extension of the active phase of delayed flags (see table of monitor flags "Flag delayed") is done by a common shared counter for all flags with this property. If more then one delayed flag is active at the same time, therefore all delayed flags will be kept active until none of the failure modes is present anymore (plus the flag delay time).

4160

As these times are higher then the step response time of the corresponding filter setting, it is ensured, that no wrong data will be transmitted without failure flag.

4163

In case of different filter settings for the two channels of the sensor, the lowest filter setting is used for the flag delay of both channels.

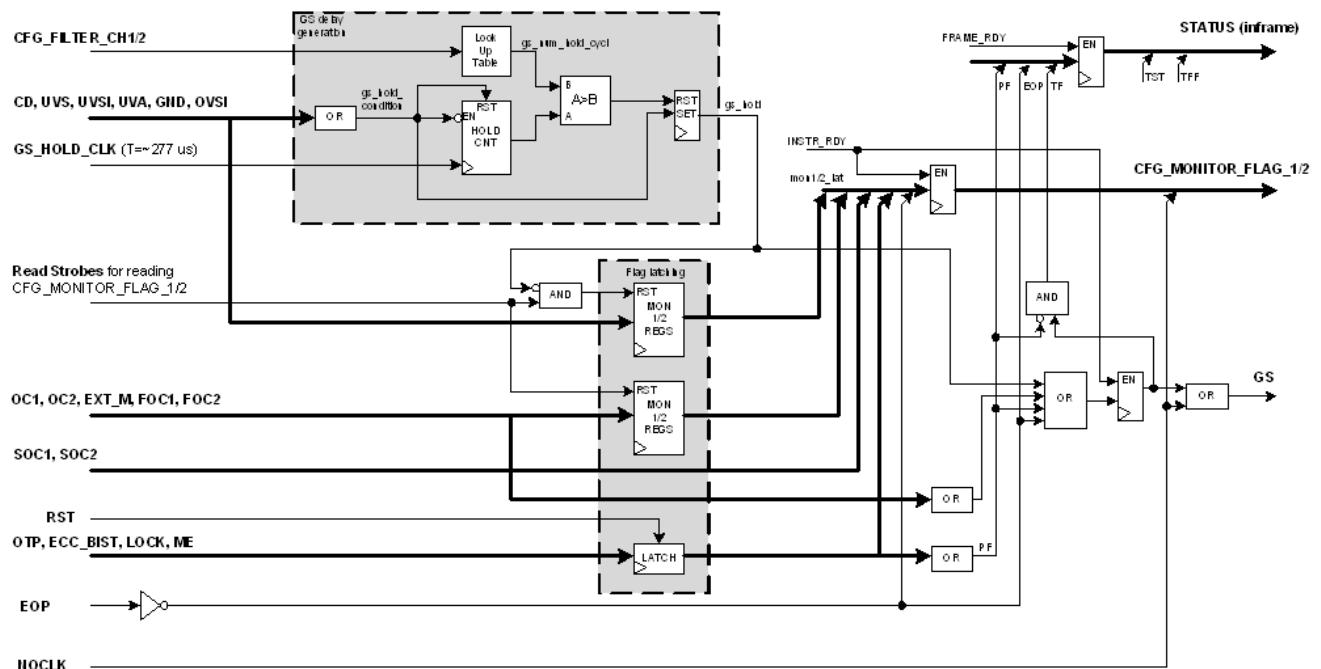
ID	parameter / condition	min	typ	max	unit
4162	Flag delay time 860Hz filter	1.52	1.72	1.92	ms
4166	Flag delay time 430Hz filter	2.18	2.41	2.64	ms
4165	Flag delay time	4.36	4.70	5.04	ms



ID	parameter / condition	min	typ	max	unit
	215Hz filter				
4164	Flag delay time 53Hz filter	16.14	17.06	17.97	ms

4159

A schematic view of flag latching and handling for BoschSPI is shown below:



### 5.7.6 Instruction Set

862

Instruction Overview:



Name	description	16 bit Data (in case of "read" commands only for sensor response; in case of "write" commands only for request)															
WR_PROT_SEL	protocol selection to switch between Bosch SPI and Open SPI	Hex = FF00FF00															
WR_MODE	voltage mode selection	voltage mode															
RD_MODE	read voltage and protocol mode	Register CRC															
RD_DEVICE_ID	read device ID	Extended device ID															
RD_REVISION_ID	read revision ID	device ID															
RD_SENSOR_DATA_CH1	read sensor data of channel 1	revision ID															
RD_SENSOR_DATA_CH2	read sensor data of channel 2	S1_13 - S1_0															
RD_CAPTURED_DATA_CH2	read captured sensor data of channel 2	S1_13 - S1_0															
WR_SID	write the safety ID to the assigned channel	14 bit captured data channel 2															
RD_SID	read the safety ID to the assigned channel	SID2															
RD_OFFSET_REG_CH1	read the register with the current offset cancellation value	SID1															
RD_OFFSET_REG_CH2	read the register with the current offset cancellation value	16 bit offset data															
WR_OFFSET_CANCELLATION	trigger FOC/SOC	16 bit offset data															
RD_OFFSET_CANCELLATION	read the status of the offset cancellation	OC length2															
RD_CLOCK_COUNTER	read the current value of the clock counter (captured value in case of automatic system clock monitoring)	OFF2															
WR_TEST_MODE	trigger build in self test	OC length1															
RD_TEST_MODE	read the status of the build in self test	OFF1															
RD_MONITOR_I_DATA	read monitor 1 data	Monitor flags															
RD_MONITOR_II_DATA	read monitor 2 data	Monitor flags															
WR_CONFIG_1	write configuration for filter and C-loss detection	DCM C loss															
RD_CONFIG_1	read configuration for filter and C-loss detection	DCM C loss															
WR_SOFT_RESET	reset of the component (SO only for the first transmission)	Filter CH2 Filter CH1															
WR_END_OF_PROG	locking command, after EOP only read commands allowed, also DEMAND_SOFT_RESET	Soft reset															
RD_BITE_CH1	read BITE OTP value of channel 1	End of programming															
RD_BITE_CH2	read BITE OTP value of channel 2	positive BITE OTP channel CH1 negative BITE OTP channel CH1															
RD_RAW_OFFSET_CH1	read RAW OFFSET OTP value of channel 1	positive BITE OTP channel CH2 negative BITE OTP channel CH2															
RD_RAW_OFFSET_CH2	read RAW OFFSET OTP value of channel 2	RAW OFFSET OTP channel CH1															
RD_SERIAL_1	read serial number bit15 - bit0	RAW OFFSET OTP channel CH2															
RD_SERIAL_2	read serial number bit31 - bit16	serial number (SN15 - SN0)															
RD_SERIAL_3	read serial number bit47 - bit32	serial number (SN31 - SN16)															
		serial number (SN47 - SN32)															

863

The data received during a write access is written to the internal registers at the rising edge of the CSB signal, if exactly 32 SPI clock pulses have been counted during CSB = active (=low level).

#### 5.7.6.1 WR\_PROT\_SEL

865

Protocol selection to switch between Bosch SPI X"FF00FF00" and Safe SPI X"00FF00FF":

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
SI	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0				
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#### 5.7.6.2 WR\_MODE

867

Set voltage mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0									
SI	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	voltage mode	CRC	0	0												
SO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#### Voltage Mode:

0010: Supply = 4.5V-11V (Vdd); SPI = 3.3V

0100: Supply = 4.5V-11V (Vdd); SPI = 3.3V

1000: Supply = 3.3V (Vdd); SPI = 3.3V

all other combinations = not allowed --> no voltage mode selected (SO stay in tristate)

#### 5.7.6.3 RD\_MODE

869

Read voltage and protocol mode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
SI	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0										
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PRO	voltage mode	gs	CRC										



all other combinations = not allowed --> no voltage mode selected (SO stay in tristate)

PRO:

0: Bosch SPI

1: Safe SPI

Reg CRC:

Contains the CRC for error detection within the configuration registers

#### 5.7.6.4 RD\_DEVICE\_ID

871

Read device ID:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	Extended device ID						device ID						gs	CRC						

Extended device ID:

individual value for each member of SMA7 family. The hex-value of the extended device ID is identical to the last two digits of the SMA name.

E.g. 0x60 for SMA760.

Device ID:

0x76 (fix value for all SMA7 products)

#### 5.7.6.5 RD\_REVISION\_ID

873

Read revision ID:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SI	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	revision ID (SWR)	revision ID (MSR)	gs	CRC	

revision ID (SWR) defines the "Full mask revision"

revision ID (MSR) defines the "Metal fix revision"

A-samples: 0x00

C1-samples: 0x10

C2-samples: 0x20

Series: 0x20

#### 5.7.6.6 RD\_SENSOR\_DATA\_CH1

875

Read sensor data of channel 1 (clipping to +/-8191LSB):

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	
SO	TFF	TST	EOP	0	TF	PF	0	SID1						S1_13 - S1_0						0	0	0	gs	CRC								

#### 5.7.6.7 RD\_SENSOR\_DATA\_CH2

877

Read sensor data of channel 2 (clipping to +/-8191LSB):

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	
SO	TFF	TST	EOP	0	TF	PF	1	SID2						S1_13 - S1_0						0	0	0	gs	CRC								

#### 5.7.6.8 RD\_CAPTURED\_DATA\_CH2

879

Read captured sensor data of channel 2 (clipping to +/-8191LSB):

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	
SO	TFF	TST	EOP	0	TF	PF	1	SID2						S1_13 - S1_0						0	0	0	gs	CRC								

#### 5.7.6.9 RD\_SID

885

Read the sensor ID to the assigned channel:



SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
SI	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC	0

## 5.7.6.10 WR\_SID

887

Write the sensor ID to the assigned channel:

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC	0

SID1:

00001: sensor ID for channel 1 --&gt;default

SID2:

00010: sensor ID for channel 2 --&gt;default

## 5.7.6.11 RD\_OFFSET\_REG\_CH1

889

Read the register with the current offset cancellation value of FOC and SOC (Register will be changed by FOC &amp; SOC):

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC	0

*The 16bit refer to the 16 MSB of the 20bit Offsetregister. The 4LSB of the register are not transmitted (no rounding applied).*

Please note, that the initial static raw offset correction value is not included in this register. The initial value can be read with RD\_RAW\_OFFSET.

## 5.7.6.12 RD\_OFFSET\_REG\_CH2

891

Read the register with the current offset cancellation value of FOC and SOC (Register will be changed by FOC &amp; SOC):

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC	0

*The 16bit refer to the 16 MSB of the 20bit Offsetregister. The 4LSB of the register are not transmitted (no rounding applied).*

Please note, that the initial static raw offset correction value is not included in this register. The initial value can be read with RD\_RAW\_OFFSET.

Conversion of 16 bit offset data channel to sensor output values:

Conversion factor is 2 for 14bit SPI sensor output. This means the SPI output has two times the sensitivity (in LSB/g) than the value read from the offset register.

example: "16 bit offset data channel 2"=200 LSB ==&gt; 400 LSB sensor channel output correction value at SPI interface

## 5.7.6.13 WR\_OFFSET\_CANCELLATION

895

Start FOC or SOC:

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC	0

OFF1:

00: offset cancellation channel 1 switched off --&gt;default

01: slow offset cancellation channel 1 switched on (SOC)

10: slow offset cancellation channel 1 switched on (XSOC)

11: fast offset cancellation channel 1 switched on

OFF2:



- 00: offset cancellation channel 2 switched off -->default  
 01: slow offset cancellation channel 2 switched on (SOC)  
 10: slow offset cancellation channel 2 switched on (XSOC)  
 11: fast offset cancellation channel 2 switched on

OC length1&2:

- 000: 64 samples --> default  
 001: 128 samples  
 010: 256 samples  
 011: 512 samples  
 100: 1024 samples  
 all other values are not executed

## 5.7.6.14 RD\_OFFSET\_CANCELLATION

897

Read the status of the offset cancellation:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

OFF1:

- 00: offset cancellation channel 1 switched off  
 01: slow offset cancellation channel 1 switched on (SOC)  
 10: slow offset cancellation channel 1 switched on (XSOC)  
 11: fast offset cancellation channel 1 switched on

OFF2:

- 00: offset cancellation channel 2 switched off  
 01: slow offset cancellation channel 2 switched on (SOC)  
 10: slow offset cancellation channel 2 switched on (XSOC)  
 11: fast offset cancellation channel 2 switched on

OC length1&2:

- 000: 64 samples  
 001: 128 samples  
 010: 256 samples  
 011: 512 samples  
 100: 1024 samples

## 5.7.6.15 RD\_CLOCK\_COUNTER

899

Read the current value of the clock counter register:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

Counter frequency = 2.25MHz

## 5.7.6.16 WR\_TEST\_MODE

901

Trigger build in self test:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMD2	TMD1	CRC	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

TMD1:

- 00: switch off self test channel 1 -->default  
 01: pos. amplitude of self test channel 1  
 10: neg. amplitude of self test channel 1  
 11 = not defined

TMD2:

- 00: switch off self test channel 2 -->default  
 10: pos. amplitude of self test channel 2  
 01: neg. amplitude of self test channel 2  
 11 = not defined

## Remark:

Self test of channel 1 and 2 can be de/activated within one command. Please note the different bit value for pos./neg. amplitude for ch1/2.

## 5.7.6.17 RD\_TEST\_MODE

903

Read the status of the build in self test:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0			
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMD2	TMD1	gs	CRC			

TMD1 :

- 00: switch off test channel 1  
 10: pos. amplitude of self test channel 1  
 10: neg. amplitude of self test channel 1

TMD2:

- 00: switch off test channel 2  
 10: pos. amplitude of self test channel 2  
 01: neg. amplitude of self test channel 2

## 5.7.6.18 RD\_MONITOR\_I\_DATA

905

Read the monitor I register:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0			
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

## 5.7.6.19 RD\_MONITOR\_II\_DATA

907

Read the monitor II register:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0			
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

## 5.7.6.20 WR\_CONFIG\_1

909

Write configuration for C-loss, filter and DCM:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

C-loss:

- 0 = no initial C-loss detection running -->default  
 1 = activation of initial C-loss detection (Stays active for typ. 513µs after triggering. This is a blocking time until the C-loss test can be started again. Any further write access during the blocking time has no effect. After the blocking time the test can be started again.)

Filter 1 (filter frequency of channel 1):

00 = 430 Hz --&gt; default

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

Filter 2 (filter frequency of channel 2):

00 = 430 Hz --&gt; default

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

DCM-DIS (disable die corrosion monitor):

0 = DCM activated (default)

1 = DCM deactivated (not released, do not use)

## 5.7.6.21 RD\_CONFIG\_1

911

## Read configuration for C-loss, filter and DCM:

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0	gs	CRC	

C-loss:

0 = no initial C-loss detection running

1 = initial C-loss detection is currently running (Stays active for typ. 513µs after triggering. This is a blocking time until the C-loss test can be started again.)

Filter 1 (filter frequency of channel 1):

00 = 430 Hz

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

Filter 2 (filter frequency of channel 2):

00 = 430 Hz

01 = 215 Hz

10 = 860 Hz

11 = 53 Hz

DCM-DIS (disable die corrosion monitor):

0 = DCM activated (default)

1 = DCM deactivated (not released, do not use)

## 5.7.6.22 WR\_SOFT\_RESET

913

Soft Reset of the component (SO only for the first transmission); has to be sent 2 times :

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x378015bc

## 5.7.6.23 WR\_END\_OF\_PROG

915

Locking command, after EOP only read commands allowed, except WR\_SOFT\_RESET:

SI	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



## 5.7.6.24 RD\_BITE\_CH1

917 Read BITE OTP value of channel 1:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	positive BITE OTP channel CH1																	negative BITE OTP channel CH1	gs	CRC

positive BITE OTP channel CH1 / negative BITE OTP channel CH1:

**SMA720/773:**

-32g...+31g: end-of-line saved BITE values in 4LSB/g (signed value; two's complement)

example: 0b10110100 (Bit11...Bit4) ==&gt; -19g

**SMA760/774:**

-64g...+63g: end-of-line saved BITE values in 2LSB/g (signed value; two's complement)

example: 0b10110100 (Bit19...Bit12) ==&gt; -38g

**All other variants:**

-256g...+254g: end-of-line saved BITE values in 0.5LSB/g (signed value; two's complement)

## 5.7.6.25 RD\_BITE\_CH2

919 Read BITE OTP value of channel 2:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	positive BITE OTP channel CH2																	negative BITE OTP channel CH2	gs	CRC

positive BITE OTP channel CH2 / negative BITE OTP channel CH2:

**SMA720/773:**

-32g...+31g: end-of-line saved BITE values in 4LSB/g (signed value; two's complement)

example: 0b10110100 (Bit11...Bit4) ==&gt; -19g

**SMA760/774:**

-64g...+63g: end-of-line saved BITE values in 2LSB/g (signed value; two's complement)

example: 0b10110100 (Bit19...Bit12) ==&gt; -38g

**All other variants:**

-256g...+254g: end-of-line saved BITE values in 0.5LSB/g (signed value; two's complement)

## 5.7.6.26 RD\_RAW\_OFFSET\_CH1

921 Read RAW OFFSET OTP value of channel 1:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC

14 bit raw offset data channel 1:

Raw offset is stored always with 32LSB/g

## 5.7.6.27 RD\_RAW\_OFFSET\_CH2

923 Read RAW OFFSET OTP value of channel 2:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC

14 bit raw offset data channel 2:

Raw offset is stored always with 32LSB/g

## 5.7.6.28 RD\_SERIAL1

925 Read serial number I:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC

## 5.7.6.29 RD\_SERIAL2

927 Read serial number II:

**BOSCH**

Department AE/ESI

# Internal Datasheet

## SMA7

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Date 17/01/2022

1.279.929.850

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

### 5.7.6.30 RD\_SERIAL3

929

Read serial number III:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC			

### 5.7.6.31 WR\_EXT\_MODE

931

Command to activate the extended mode:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	gs	CRC		

Extended mode is active, if EXT=1.

933

Command to read the status of the extended mode:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SI	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC	0	0		
SO	TFF	TST	EOP	0	TF	PF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXT	gs	CRC		



## 6. PSI5 Interface

The PSI5 interface of the SMA7 is conform with the PSI5 specification rev. 1.3 and 2.1 (base specification in combination with the airbag sub standard) for the modes and requirements given below. The only exception is the maximum clock drift rate per dataframe for legacy receivers (see chapter 6.1.3). For this point SMA7 is only compliant with PSI5 specification rev. 2.3.

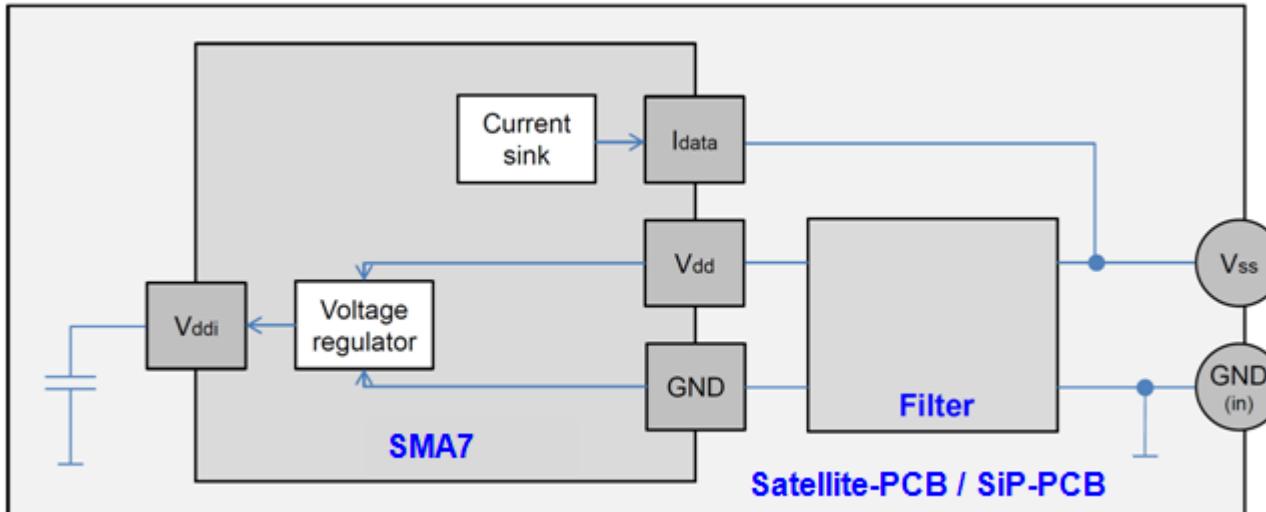
There are no relevant differences between PSI5 specification rev 1.3 and 2.1, except a compatibility bit, which is send in Initphase 2.

### 6.1 Hardware Layer

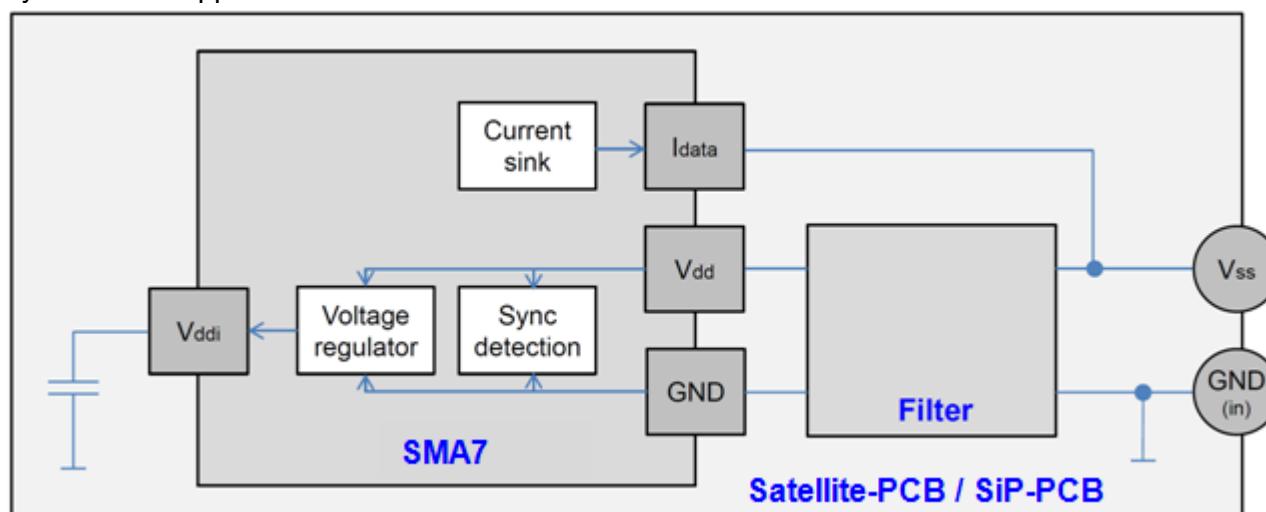
#### 6.1.1 I\_data Pin and Supply Voltage Connections

The SMA7 is supplied with power via the supply wires (named VSS and GND(in)). Sensor data is transmitted to the ECU by modulating current pulses onto the positive supply wire. The SMA7 is supplied with power and recognizing syncpulses via the VDD pin of the sensor. The IDATA pin of SMA7 ASIC is used for current modulation.

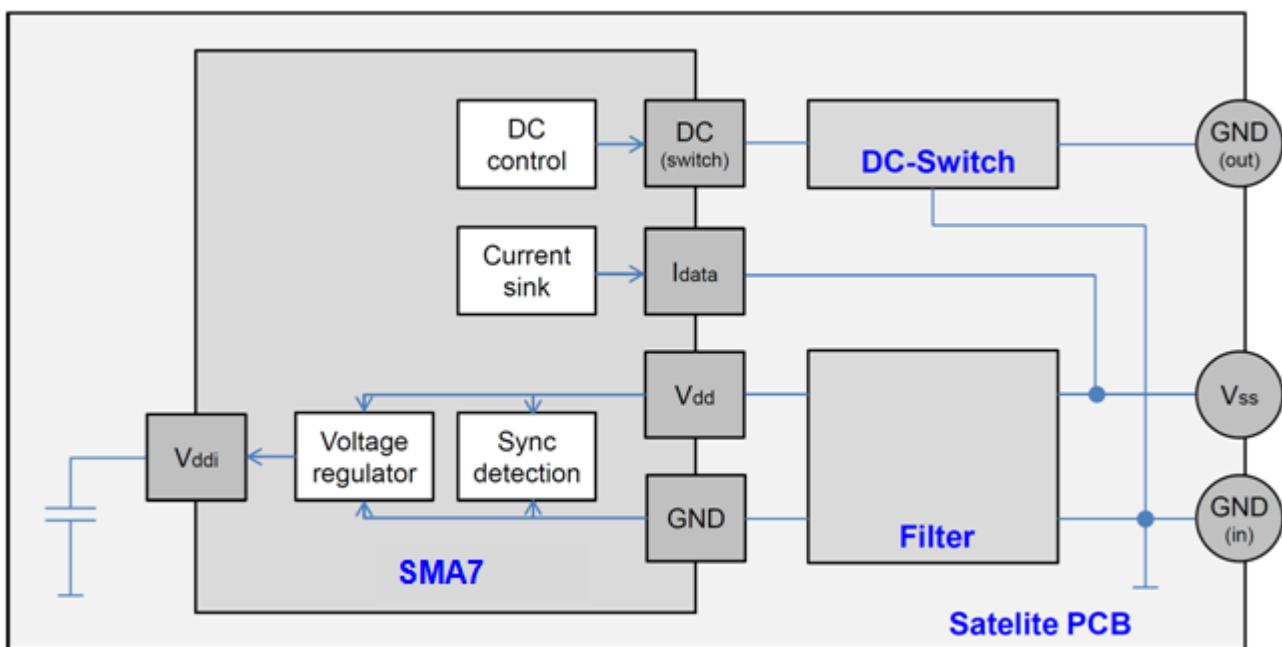
Asynchronous application:



Synchronous application:



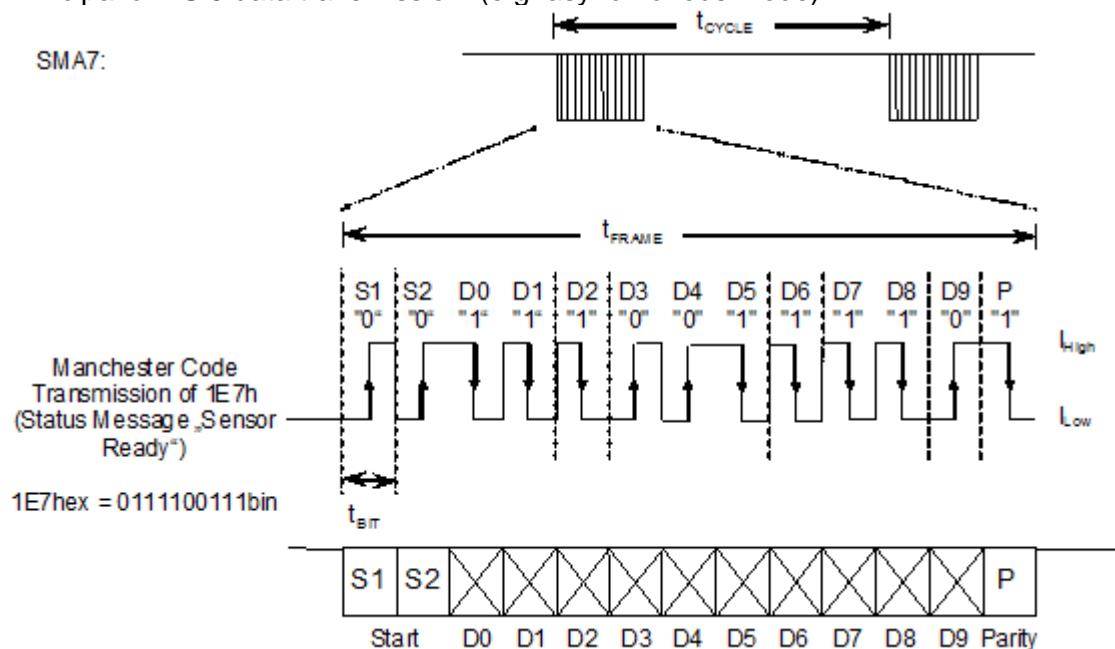
Daisy chain application (the pin DC equals the pin SO in SMA7):



### 6.1.2 Manchester Coding

After the start-up and initialization phase of the sensor, acceleration data is periodically transmitted in a digital format to the ECU via the current interface as shown in the figure below:

Principal of PSI5 data transmission: (e.g. asynchronous mode)



Manchester coding is used for data transmission. A logic "0" is represented by a rising slope and a logic "1" by a falling slope in the middle of each bit. The logic levels are determined by a modulation of the current on the power supply lines.

A "low" level ( $I_{Low}$ ) is represented by the quiescent current consumption of the sensor, a "high" level ( $I_{High}$ ) by  $I_{Low} + \Delta I$ .

The bit time  $t_{BIT}$ , data frame time  $t_{FRAME}$  and message repetition time  $t_{CYCLE}$  are dependent on the transmission mode selected by the application and are specified in section transmission modes.



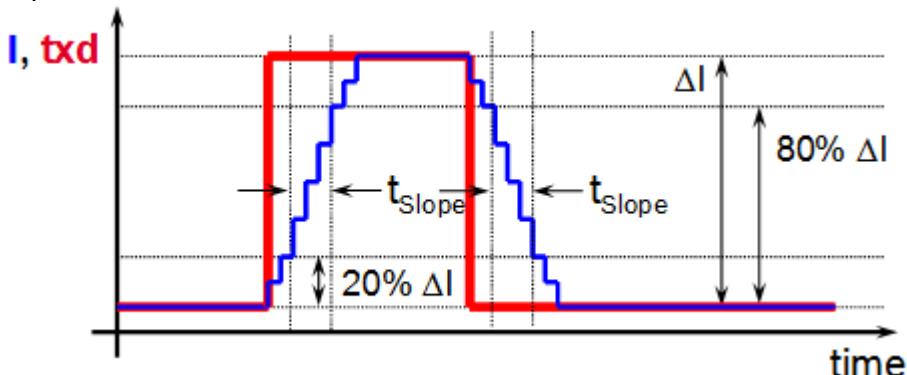
### 6.1.3 Slope Control

The transition time between  $I_{Low}$  and  $I_{High}$  of the current sink is controlled by an active slope shaping circuit within the ASIC as shown in the diagram below. The slope shaping is implemented as an 8 bit digital vector 'txd\_vec'. Each bit in this vector controls a single current sinks. The digital state of the sink current (i.e.  $\Delta I$  switched on/off) is controlled internally via the digital signal 'txd'.

If a rising edge is scheduled on txd the first current sinks is turned on by assigning '1' to bit 0 of txd\_vec. With  $f=f_{osc}/2$  an additional '1' is shifted from right into the txd\_vec until all current sinks are activated after 8 cycles.

On a falling edge of txd, the current sinks are turned off in reverse order of their activation by shifting in '0' from left into txd\_vec until all current sinks are turned off.

Slope control of Manchester code:



ID	parameter / condition	min	typ	max	unit
3068	Sink Current Step Step 1, 2, 7 and 8		2.6		mA
3069	Sink Current Step Step 3, 4, 5 and 6		3.9		mA
995	Sink Current $\Delta I$ $\Delta I = I_{high} - I_{low}$	22	26	30	mA
996	Sink Current Edge Duration $t_{slope}$ 20% – 80% of $\Delta I$	350	503	600	ns
997	Sink Current Edge Duration $t_{slope}$ 80% – 20% of $\Delta I$	350	503	600	ns
999	Bit Time $t_{bit}$ 125 kBps modes	7.6	8.1	8.4	$\mu s$
1000	Bit Time $t_{bit}$ 189 kBps modes	5	5.4	5.6	$\mu s$
3070	Maximum Clock Drift Rate During data frame			1	%
3071	Maximum Clock Drift Rate Over time			1	%/s
3072	Duty Cycle of Bit	49	50	51	%



ID	parameter / condition	min	typ	max	unit
	Duty cycle of manchester code				

### 6.1.4 Synchronization Signal Detection

1002 The receiver unit can synchronize the sensor reply by modulating a synchronization pulse on the supply voltage. The sensor will detect the increase of the supply voltage at the VDD pin and deliver a signal with a defined timing in reference to the synchronization pulse.

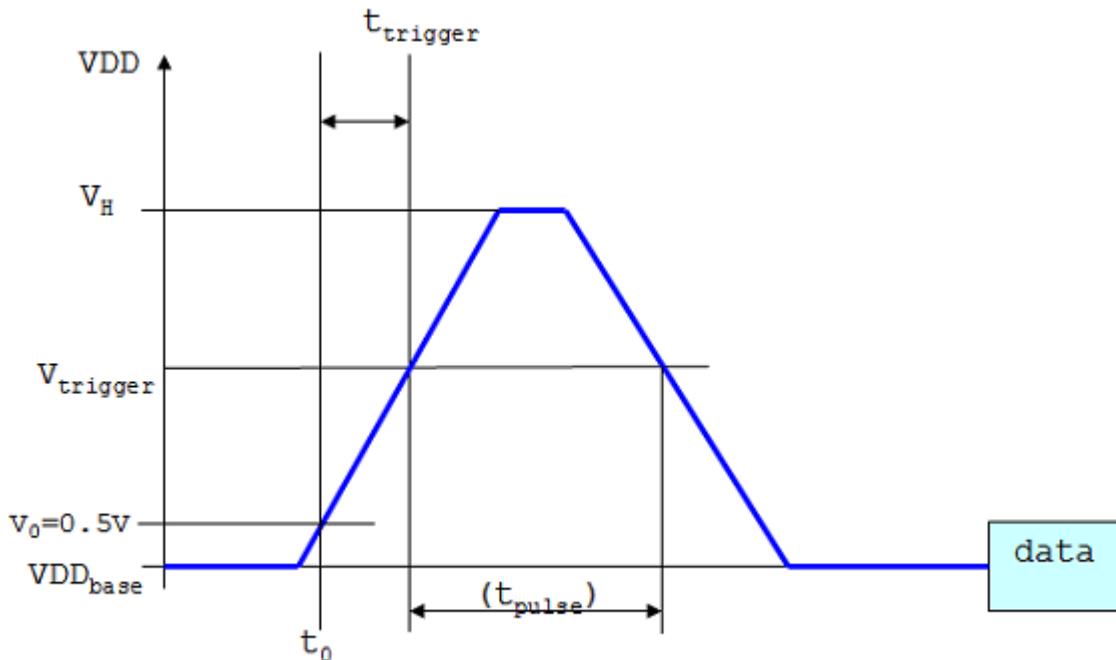
1003 The SMA7 will recognize the synchronization pulse if the conditions as shown in the graphic and table below are fulfilled.

1004 The recognition scheme is as follows: The SMA7 evaluates how many clock cycles (fosc= 18 MHz nominal) the voltage at the VDD pin is above  $V_{trigger}$ .

1006 The voltage at VDD shall not exceed the maximum sync pulse height for proper sync pulse recognition.

1007 The synchronization pulse sent by the ECU shall be conform to PSI5 specification v1.3 and v2.1.

1008 Detection of synchronization pulses:



1064 For synchronous modes the sensor is responding after a fixed amount of time after SYNC detection, which is specified at the corresponding transmission mode.

All timings in sync modes are referred to  $t_0$ , if not stated otherwise.

ID	parameter / condition	min	typ	max	unit
1009	Supply Voltage at Vdd $V_{DD_{base}}$	4.5		11	V
1010	Sync Pulse height $V_H - V_{DD_{base}}$	3.5		5.5	V
4062	Sync threshold $V_{trigger} - V_{DD_{base}}$	1.4		2.6	V
1012	Slew Rate of Sync Pulse at $t_{edge}$ rising edge	0.43	0.75	1.5	V/ $\mu$ s



ID	parameter / condition	min	typ	max	unit
3076	Slew Rate of Sync Pulse at $t_{edge}$ falling edge	-1.5			V/ $\mu$ s
1013	Sync pulse duration $t_{pulse}$ (above $V_{trigger}$ )	10		35	$\mu$ s
3077	Sync Pulse Detection Time (time above threshold to accept sync pulse) $t_{pulse}$ (above $V_{trigger}$ ); tolerance defined by oscillator tolerance	6.5	6.83	7.3	$\mu$ s

- 3074 All values concerning sync pulse recognition (sensor trigger threshold, acceptance time) are also achieved in combination with the Pi filter of the LGA SiP for the full tolerance range of the values of the passive components.
- 3977 In detail this means: There is no relevant change of the slew rate by the Pi-filter. But the Pi-filter can add a delay of 1.2 $\mu$ s - 2.7 $\mu$ s to the sync pulse. This will add to the specified sync pulse detection time. But the sum of delay and detection time is within minimum specified syncpulse time of 10 $\mu$ s. And the delay is within the 3 $\mu$ s which are allowed by PSI5-Spec.

#### 6.1.4.1 Blanking time for sync pulse

- 4780 The SMA7 provides a blanking time feature, which is globally enabled by an OTP bit in the customer area (MOTP\_PAS\_CONFIG\_4.MOTP\_PSI\_BLANK\_EN).
- 4781 If this feature is enabled, all sync pulses within the time  $t_{blank}$  after the recognition of a valid sync pulse are ignored.
- 4782 ECU cycle time of the used PSI mode must be set by the customer with the OTP bit (MOTP\_PAS\_CONFIG\_4.MOTP\_PSI\_BLANK\_TIME). This setting must be aligned with the chosen PSI5 communication mode.

MOTP_PSI_BLANK_TIME	ECU cycle time
0b0	250 $\mu$ s
0b1	500 $\mu$ s

The blanking time feature is only available for 250 $\mu$ s and 500 $\mu$ s sync modes. For all other modes (700 $\mu$ s, 1000 $\mu$ s) it must be disabled.

- 4783 The applied blanking time is calculated from the programmed cycle time by subtracting a percent value ( $t_{sync\_acc\_min}$ ).  
 $t_{blank} = t_{cycle} - t_{sync\_acc\_min}$
- 4784  $t_{sync\_acc\_min}$  can be configured by the OTP register MOTP\_PAS\_CONFIG\_7.MOTP\_OSC\_MON\_ACC\_MIN within the following range:

MOTP_OSC_MON_ACC_MIN	$t_{sync\_acc\_min}$
0b00	-8%
0b01	-9%
0b10	-10%
0b11	-12%

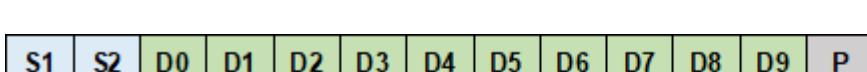
- 4785 The blanking time is not active in PSI BiDir service mode.

## 6.2 Data Link Layer



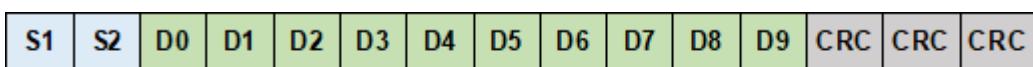
### 6.2.1 Data Frame

1016 A PSI5 data frame sent by SMA7 consists of the following bits:  
 1017 1.) P10P..., A10P... and S10P... modes



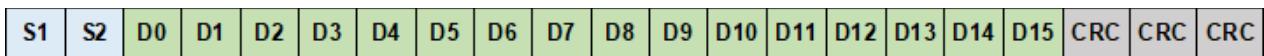
- 1018 • Two start bits (S1 = S2 = "0")
- 1019 • Ten data bits (D0...D9)
- 1020 • One parity bit (P = even parity)

1021 2.) P10CRC...modes



- 1022 • Two start bits (S1 = S2 = "0")
- 1023 • Ten data bits (D0...D9)
- 1024 • 3 bit CRC (generator polynom =  $1 + x + x^3$ )

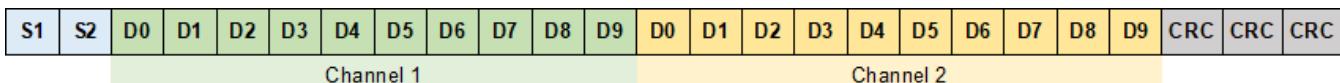
1025 3.) P16CRC...modes



- 1026 • Two start bits (S1 = S2 = "0")
- 1027 • Sixteen data bits (D0...D15, containing 14 data bits)
- 1028 • 3 bit CRC (generator polynom =  $1 + x + x^3$ )

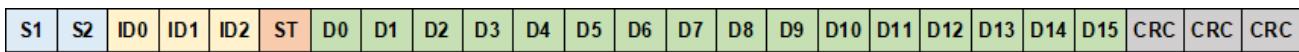
3614 In this mode only 14 of the 16 bits are used to send acceleration data from the signal path. The other two bits are filled with dummy informations. For details see the interface description in the signal path section (Chapter 2).

1029 4.) P20CRC...modes (2 x 10 Bit)



- 1030 • Two start bits (S1 = S2 = "0")
- 1031 • Twenty data bits (D0...D19 = D0...D9 of Ch1 + D0...D9 of Ch2)
- 1032 • 3 bit CRC (generator polynom =  $1 + x + x^3$ )

1033 4.) P20CRC...modes (16 + 4 Bit)



- 1034 1. Two start bits (S1 = S2 = "0")
- 1036 2. Three channel ID bits (ID0...ID2)
  - 1035 • Ch1= "000"
  - 1035 • Ch2= "001"
- 1037 3. One status flag (ST = 0 --> "Sensor OK"; ST = 1 --> "Sensor defect")
- 1038 4. Sixteen data bits (D0...D15, containing 14 data bits)
- 3615 5. Three bit CRC (generator polynom =  $1 + x + x^3$ )



In this mode only 14 of the 16 bits are used to send acceleration data from the signal path. The other two bits are filled with dummy information. For details see the interface description in the signal path section (Chapter 2).

Depending on the selected communication mode, the length of one data frame is 13 bits (P10P..., A10P... and S10P... modes), 15 bits (P10CRC...modes), 21 bits (P16CRC...modes.) or 25 bits (P20CRC...modes).

Data are transmitted with LSB first.

Data frames are sent periodically if asynchronous transmission modes have been chosen.

For all synchronous transmission modes, data are sent only after having received a synchronization pulse.

If the option "error detection with parity bit" is chosen, error detection is realized with even parity, e.g., if the number of ones among D0 – D9 is odd then P=1, if the number of ones is even the P=0. The parity bit option is available for all P10P..., A10P... and S10P... modes.

If the option "error detection with CRC" is chosen, error detection is realized with 3bit CRC . The CRC option is available for all P10CRC..., P16CRC... and P20CRC...modes.

The CRC calculation is specified by:

- Polynomial =  $1 + x + x^3$
- Initial value = 0b111
- Target value = 0b000

## 6.2.2 Data Range

The SMA7 transmits different types of messages by using the two's compliment coding scheme:

- Acceleration Data
- Status and Error Codes
- Identification Data

In the following table the data ranges of the 10 bit and 16 bit data word are defined:

10bit		16bit		Signification	Range
Dec	Hex	Dec	Hex		
511	1FF	32767	7FFF	Reserved (ECU internal use)	Status & error messages
500	1F4	32000	7D00	Sensor defect	
487	1E7	31231	79FF	Sensor ready, all lock bits set	
486	1E6	31104	7980	Sensor ready, lockbits for preprogrammed OTP areas (ASIC/SMA) set	
485	1E5	31103	797F	Sensor ready, "no error mode" selected	
482	1E2	30848	7880	BiDir Communication: RC "Error"	
481	1E1	30847	787F	BiDir Communication: RC "Ok"	
480	1E0	30720	7800	Highest positive Sensor signal	Sensor output signal
0	000	0	0000		
-480	220	-30720	8800	Smallest negative Sensor signal	
-481	21F	-30721	87FF	Status data 1111 or error code	
-496	210	-31744	8400	Status data 0000 or error code	
-497	20F	-31745	83FF	Block ID 16 and 32	Block IDs and Data for Transmission during Init 2 and Error codes for transmission during Init 3 and normal operation.
-512	200	-32768	8000	Block ID 1 and 17	

For sensors with a data word length of more than 10 bit, the data range scales as described above. Furthermore, the following definition is effective: status and initialization data words of range 2 and 3 are filled up with the value of the bit corresponding to the "D0" bit in the 10 Bit data word (possibility to check for stuck bits in the receiver).

**Mapping of Status & Initialization Data**16 Bit  
Data Word

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

10 Bit  
Data Word

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1	1	1

Example  
"Block ID 16"  
0x20F

"2"	"0"	"F"
-----	-----	-----

### 6.2.3 Special Codes

1056

During initialization phase 2 special codes are used for data transmission: Block ID codes and Status Data.

1057

For each block ID (ID1 – ID 32) and each value of status data (0000 – 1111) a data word is assigned as shown in the following table:

1058



Block ID (Dec)	10 bit Code (Dec)	10bit Code (Hex)	16 bit Code (Dec)	16bit Code (Hex)
1 & 17	-512	0x200	-32768	8000
2 & 18	-511	0x201	-32641	807F
3 & 19	-510	0x202	-32640	8080
4 & 20	-509	0x203	-32513	80FF
5 & 21	-508	0x204	-32512	8100
6 & 22	-507	0x205	-32385	817F
7 & 23	-506	0x206	-32384	8180
8 & 24	-505	0x207	-32257	81FF
9 & 25	-504	0x208	-32256	8200
10 & 26	-503	0x209	-32129	827F
11 & 27	-502	0x20A	-32128	8280
12 & 28	-501	0x20B	-32001	82FF
13 & 29	-500	0x20C	-32000	8300
14 & 30	-499	0x20D	-31873	837F
15 & 31	-498	0x20E	-31872	8380
16 & 32	-497	0x20F	-31745	83FF

Status Data (Bin)	10 bit Code (Dec)	10bit Code (Hex)	16 bit Code (Dec)	16bit Code (Hex)
0000	-496	0x210	-31744	8400
0001	-495	0x211	-31617	847F
0010	-494	0x212	-31616	8480
0011	-493	0x213	-31489	84FF
0100	-492	0x214	-31488	8500
0101	-491	0x215	-31361	857F
0110	-490	0x216	-31360	8580
0111	-489	0x217	-31233	85FF
1000	-488	0x218	-31232	8600
1001	-487	0x219	-31105	867F
1010	-486	0x21A	-31104	8680
1011	-485	0x21B	-30977	86FF
1100	-484	0x21C	-30976	8700
1101	-483	0x21D	-30849	877F
1110	-482	0x21E	-30848	8780
1111	-481	0x21F	-30721	87FF

## 6.2.4 Error codes

1369

Possible error codes for SMA7:

ASIL\_D

Type of error	error code 10bit		error code 16bit		priority number	Transmission in all active channels	channel-specific
	decimal value	Hex value	decimal value	Hex value			
OTP integrity check error	-491	215	-31361	857F	1	yes	
OTP integrity check error customer area	-490	216	-31360	8580	2	yes	
Lock-Bit-Error	-489	217	-31233	85FF	3	yes	
Undervoltage Error (AVDD,VDDI)	-493	213	-31489	84FF	4	yes	
GND connection error (GND_EXT and GND_MEMS)	-484	21C	-30976	8700	6	yes	
Invalid Configuration	-488	218	-31232	8600	7	yes	
Slow offset cancellation error channel 1	-496	210	-31744	8400	8		yes
Fast offset cancellation error channel 1	-495	211	-31617	847F	9		yes
Self test failure: Neg/Pos Test channel 1	-494	212	-31616	8480	10		yes
Slow offset cancellation error channel 2	-487	219	-31105	867F	11		yes
Fast offset cancellation channel 2	-486	21A	-31104	8680	12		yes
Self test failure: Neg./Pos test channel 2	-485	21B	-30977	86FF	13		yes
Oscillator monitor error	-483	21D	-30849	877F	14	yes	
Die-edge delamination monitor	-492	214	-31488	8500	15	yes	
MUX Error/Send data error channel 1 and 2	-481	21F	-30721	87FF	16	yes	

4354



If there is more than one sensor error, the error with the lowest (numerical) priority number is transmitted. All errors will be latched i.e. once they occur then the corresponding error code (depending upon Error priority) will be send till reset is done.

#### Explanation of Error flags:

- OTP integrity check error is set, if the stored CRC value does not match to the calculated CRC value from the memory content of the ASIC and SMA OTP region. The CRC is only checked if the corresponding lock bit is set. ASIL\_D
- OTP integrity check error customer area is set, if the stored CRC value does not match to the calculated CRC value from the memory content of the customer-programmed OTP region. The CRC is only checked if the corresponding lock bit is set. ASIL\_D
- Lock bit error is set, if one of the lockbits, of the pre-programmed OTP regions, is not set. ASIL\_D
- Undervoltage error is set if undervoltage of VDDI or internal voltage is detected. ASIL\_D
- GND-connection error is set if a sensor internal GND loss or a GND pin loss is detected. ASIL\_D
 

*Remark: External GND loss also leads to loss of communication. Therefore this flag is only visible for internal GND loss.*
- Invalid configuration is set if:
  1. Amplification factor does not match to sensor type (setting of SMA\_range does not match to the programmed CMA\_type) ASIL\_D
  2. Selected PSI5 Mode is not defined ASIL\_D
- Slow offset cancellation error channel 1 or channel 2 is set if the maximum correction value is exceeded. *(A SOC error code is transmitted only while an SOC is in active state. Otherwise error codes caused by any other error are transmitted according to their priority.)* ASIL\_D
- Fast offset cancellation error channel 1 or channel 2 is set if:
  1. The absolute residual output value during offset check in Init phase 2 is bigger than the programmed threshold. The offset check is also done, if the FOC is deactivated by MOTP\_OFS\_FOC\_DISABLE. To deactivate the offset check, the register MOTP\_FOC\_Limit can be set to "0". ASIL\_D
  2. The maximum correction value limit is exceeded. ASIL\_D
- Self test failure channel 1 or channel 2 is set if the Self test is not passed. ASIL\_D
- Multiplexer error is set if the Manchester code being send is different from the internal generated sampled acceleration value. The error is not triggered, if any other error flag in this channel is triggered. ASIL\_D

## 6.3 Power-On Phase and Initialization

### 6.3.1 Summary

After a power-on or under-voltage reset the sensor performs 3 initialization phases with different durations, depending on the sensor configuration.

ID	parameter / condition	min	typ	max	unit
1322	Init Phase 1 Async. Modes	57.57	61	63.63	ms
1323	Init Phase 1 Sync. Modes	57.57	61	63.63	ms
1324	Init Phase 2 Async. Modes; 256 x 229µs	55.32	58.6	61.16	ms
1325	Init Phase 2 500µs Sync. Modes; 256 x 500µs	*)	128	*)	ms
3855	Init Phase 2	*)	64	*)	ms



ID	parameter / condition	min	typ	max	unit
	250µs Sync. Modes; 256 x 250µs				
5119	Init Phase 2 1000µs Sync. Modes; 256 x 1000µs	*)	256	*)	ms
5120	Init Phase 2 700µs Sync. Modes; 256 x 700µs	*)	179.2	*)	ms
1326	Init Phase 3 Async. Modes; 32 x 229µs	6.91	7.33	7.65	ms
1327	Init Phase 3 500µs Sync. Modes; 16 x 500µs	*)	8	*)	ms
3856	Init Phase 3 250µs Sync. Modes; 16 x 250µs	*)	4	*)	ms
5121	Init Phase 3 1000µs Sync. Modes; 16 x 1000µs	*)	16	*)	ms
5122	Init Phase 3 700µs Sync. Modes; 16 x 700µs	*)	11.2	*)	ms

1328

\*) The duration of the init phases 2 and 3 is based on the number of transmitted messages. For the sync and parallel bus modes, a rate of the sync pulse transmission of 2kHz/4kHz (i.e.  $t_{CYCLE} = 500\mu s/250\mu s$ ) for nominal case is assumed. The tolerance is related to the oscillator tolerance of the ECU, which must be within +/-1%.

5300

For 1000 µs- modes, it is not allowed to send sync pules after power on within the bidir activation time, which is specified in ID 4364.

1329

During the initialization phase 1 there is no data transmission.

1330

In the initialization phase 2 the sensor is tested and status data is send. (If lock bit is not set, sensor data is sent).

1331

In the initialization phase 3 the sensor status is transmitted.

4042

If a P20CRC mode with 10+10bit is used, then the individual status data or error code of each channel is send in the 10bit, which correspond to this channel. E.g. if the sensor is configured to send Ch1 data with D0-D9 and Ch2 data with D10-D19, then the status data of Ch1 will also be send with D0-D9 and for Ch2 with D10-D19.

1332

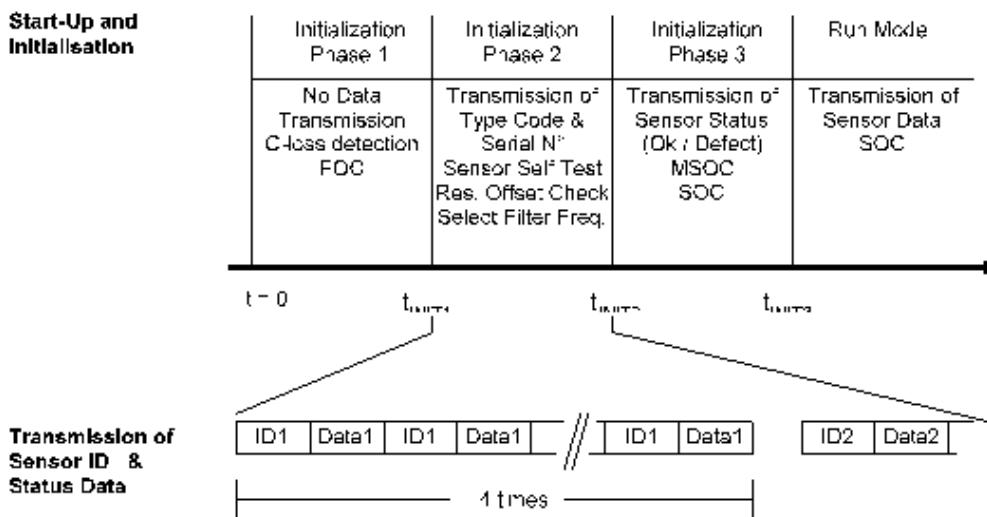
If the sensor is defect, a specific "Sensor Defect" information is sent until the sensor is powered off.

1333

Otherwise the SMA7 proceeds to normal operation mode and transmits sensor data.

1334

PSI5 communication - sensor initialization:



1336 In asynchronous and synchronous mode, the sensor goes automatically to initialization Phase 1 after Reset.

1337 In daisy chain mode the sensor goes in init phases only after RUN command.

1338 During Init-Phase 1 the sensor performs the fast offset cancellation with 512 samples and the C-loss detection and does not transmit data to the ECU.

391 Execution of fast offset cancellation during init phase can be deactivated in the OTP by setting [OFS\_FOC\_DISABLE] to 1.

### 6.3.3 Initialization Phase 2

1340 The Status Data sends information such as the manufacturers, the type of sensor, measurement range, production time, serial number, etc. to the production and end users.

1341 Before transmitting the Status Data, an identification-code (ID Code) will be sent (ID1-IDn).

1342 Every Status Data is sent 4 times. That means one gets ID code and data word alternating 4 times, one after the other. This is done in 2 pages.

1343 Page 1:

ID1, Data1, ID1, Data1, ID1, Data1, ID1, Data1, ID1, Data1, ID2, Data2, ID2, Data2, ID2, Data2, ID2, Data2, ....  
ID15, Data15, ID15, Data15, ID15, Data15, ID15, Data15, ID16, Data16, ID16, Data16, ID16, Data16, ID16, Data16,

Page 2:

ID1, Data17, ID1, Data17, ID1, Data17, ID1, Data17, ID2 , Data18, ID2, Data18, ID2, Data18, ID2, Data18, .... ID16, Data32, ID16, Data32, ID16, Data32, ID16, Data32.

1344 Initialization data Page 1:



Status Data	Index	Description	origin	Mapping		MOTP [bit]
				BIN	BIN-MOTP	
Data_1	0	Protocol revision	constant & OTP	0b01X0	X	MOTP_PSI5_REVISION [0]
Data_2	1	Number of data blocks (bit 7:4)	constant	0b0010	NA	NA
Data_3	2	Number of data blocks (bit 3:0)	constant	0b0000	NA	NA
Data_4	3	Manufacturer code (bit 7:4)	OTP	0bXXXX	X	MOTP_MANUFACT_CODE[7:4]
Data_5	4	Manufacturer code (bit 3:0)	OTP	0bXXXX	X	MOTP_MANUFACT_CODE[3:0]
Data_6	5	Sensor generation	OTP	0bXXXX	X	MOTP_PAS_GEN[3:0]
Data_7	6	Sensor type acceleration sensor	OTP	0bXXXX	X	MOTP_SENSOR_TYPE[3:0]
Data_8	7	Sensor parameter (sensor axis channel 1/2)	OTP	X	MOTP_SGB_AXIS_CH1/2[1:0]	
		Sensor parameter (filter setting for channel 1/2, bit 1)	OTP		Y	MOTP_FILTER_SETTING_CH1/2[1]
Data_9	8	Sensor parameter (SMA range, re-mapped acc. AK-LV27, for details see below)	OTP	0bXXXX	X (but re-mapped)	MOTP_SMA_RANGE_CH1/2[2:0]
		Sensor parameter (filter setting for channel 1/2, bit 0)	OTP	X	MOTP_FILTER_SETTING_CH1/2[0]	
		Compatibility mode	OTP		Y	MOTP_COMPATIBILITY_BIT[0]
Data_10	9	SGB housing code (bit 5:4)	OTP	0bXYZZ	Z	MOTP_SGB_HOUSING_CODE[5:4]
Data_11	10	SGB housing code (bit 3:0)	OTP	0bXXXX	X	MOTP_SGB_HOUSING_CODE[3:0]
Data_12	11	Sensor code customer (bit 11:8)	OTP	0bXXXX	X	MOTP_SGB_CODE_CUSTOMER[11:8]
Data_13	12	Sensor code customer (bit 7:4)	OTP	0bXXXX	X	MOTP_SGB_CODE_CUSTOMER[7:4]
Data_14	13	Sensor code customer (bit 3:0)	OTP	0bXXXX	X	MOTP_SGB_CODE_CUSTOMER[3:0]
Data_15	14	SG manufacturing date (bit 13:12)	constant & OTP	0b00XX	X	MOTP_SGB_MANU_DATE_H[5:4]
Data_16	15	SG manufacturing date (bit 11:8)	OTP	0bXXXX	X	MOTP_SGB_MANU_DATE_H[3:0]

1345

## Initialization data Page 2:

Data_17	16	SG manufacturing date (bit 7:4)	OTP	0bXXXX	X	MOTP_SGB_MANU_DATE_L[7:4]
Data_18	17	SG manufacturing date (bit 3:0)	OTP	0bXXXX	X	MOTP_SGB_MANU_DATE_L[3:0]
Data_19	18	SGB line number (bit 3:0)	OTP	0bXXXX	X	MOTP_SGB_LINE_NO[3:0]
Data_20	19	SGB lot number (bit 7:4)	OTP	0bXXXX	X	MOTP_SGB_LOT_NO[3:0]
Data_21	20	SMA series number (bit 47-44)	OTP	0bXXXX	X	MOTP_ASIC_SN_2[15:12]
Data_22	21	SMA series number (bit 43-40)	OTP	0bXXXX	X	MOTP_ASIC_SN_2[11:8]
Data_23	22	SMA series number (bit 39-36)	OTP	0bXXXX	X	MOTP_ASIC_SN_2[7:4]
Data_24	23	SMA series number (bit 35-32)	OTP	0bXXXX	X	MOTP_ASIC_SN_2[3:0]
Data_25	24	SMA series number (bit 31-28)	OTP	0bXXXX	X	MOTP_ASIC_SN_1[15:12]
Data_26	25	SMA series number (bit 27-24)	OTP	0bXXXX	X	MOTP_ASIC_SN_1[11:8]
Data_27	26	SMA series number (bit 23-20)	OTP	0bXXXX	X	MOTP_ASIC_SN_1[7:4]
Data_28	27	SMA series number (bit 19-16)	OTP	0bXXXX	X	MOTP_ASIC_SN_1[3:0]
Data_29	28	SMA series number (bit 15-12)	OTP	0bXXXX	X	MOTP_ASIC_SN_0[15:12]
Data_30	29	SMA series number (bit 11-8)	OTP	0bXXXX	X	MOTP_ASIC_SN_0[11:8]
Data_31	30	SMA series number (bit 7-4)	OTP	0bXXXX	X	MOTP_ASIC_SN_0[7:4]
Data_32	31	SMA series number (bit 3-0)	OTP	0bXXXX	X	MOTP_ASIC_SN_0[3:0]

1346

## Options for Init Data 1 - "Protocol revision":

Protocol description	Value
PSI5 1.3	0100
PSI5 2.1	0110

The protocol revision can be chosen, by setting the corresponding OTP bit. *The bit has no other function.*

1347

## Options for Init Data 4/5 - "Manufacturer" (acc. PSI5 rev. 1.3):

Manufacturer (PSI5 rev 1.3)	Sensor ID Data 4	Sensor ID Data 5
Autoliv	0100	0000
Bosch	0001	0000
Continental	1000	0000
TRW	0101	0100
Other sensor manufacturers	tbd	tbd

The list is only an example of possible values. The 8 bit are programmable.

1348

## Options for Init Data 4/5 - "Manufacturer" (acc. PSI5 rev. 2.1):



Manufacturer (PSI5 rev 2.1)	Sensor ID Data 4	Sensor ID Data 5
Autoliv	0100	0001
Bosch	0100	0010
Continental	0100	0011
TRW	0101	0100
Other sensor manufacturers	tbd	tbd

The list is only an example of possible values. The 8 bit are programmable.  
3969 Options for Init Data 7 - "Sensor type"

Sensor type	Value (Data7)
High-g	0001
Low-g	0010

The list is only an example of possible values. The 4 bit are programmable.  
1349 Options for Init Data 8 - "Sensor satellite axis" (acc. AK-LV27):

Sensor satellite axis	Sensor ID (Data8)
Satellite sensing axis $\alpha$	0100
Satellite sensing axis $\beta$	0000
Satellite sensing axis $\gamma$	1000

The list is only an example of possible values. The 4 bit are programmable.  
1350 The parameters  $\alpha$ ,  $\beta$ , and  $\gamma$  are intended to indicate the sensitive direction of a peripheral sensor and depend on how the customer mounts the SMA7 into a car. These parameters have no influence on the signal path of the sensor. They enable the user to program SMA7 such that the mounting orientation according to AK-LV 27 can be transmitted via PSI5.

1351 Options for Init Data 9 - "Sensor range" (acc. AK-LV27):

Sensor Range	Sensor ID Data9
30g	0110
60g	0111
120g	1000
240g	1001
480g	1010

1352

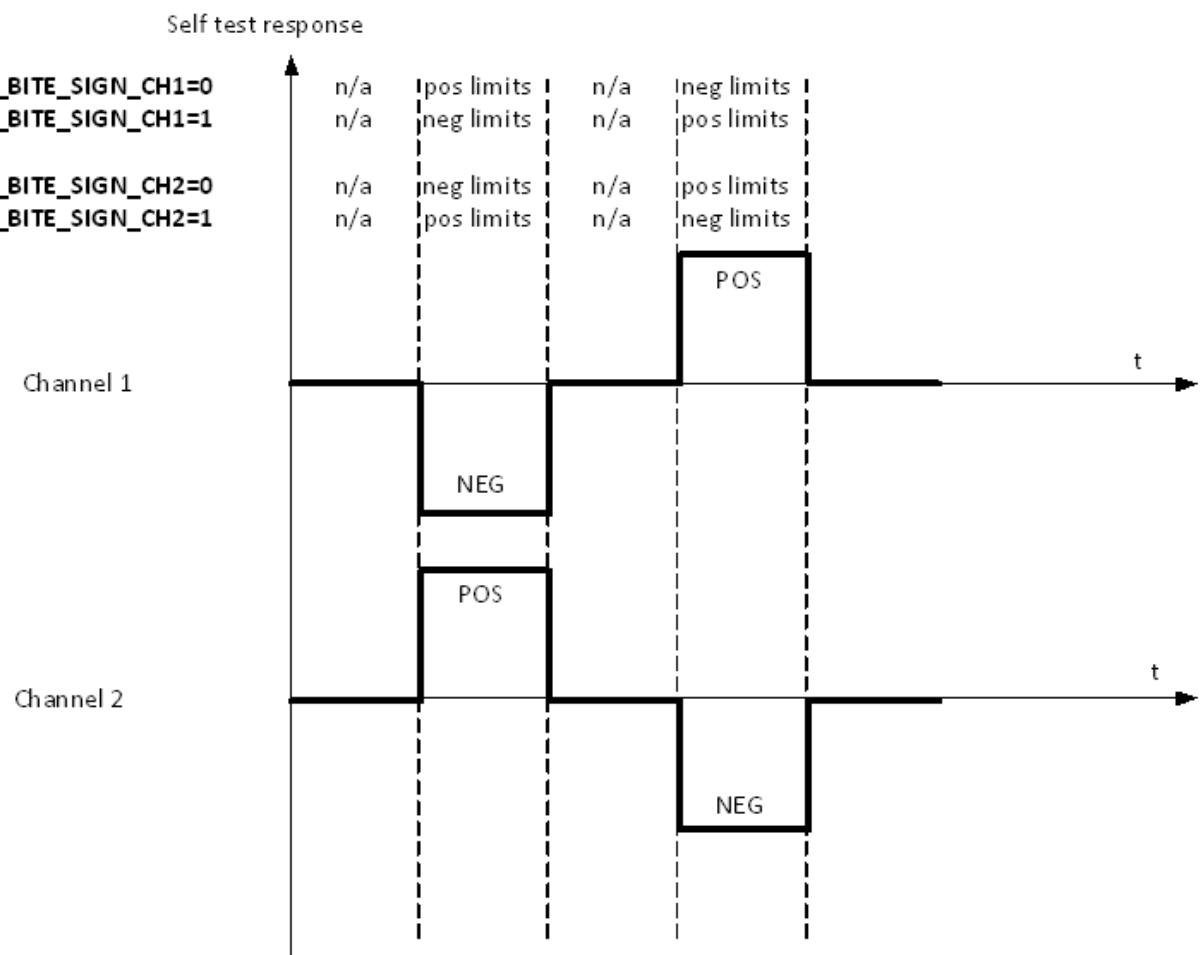
Options for Init Data 10 - "Filter frequency":



Sensor filter frequency	Sensor ID Data8, Bit 0	Sensor ID Data10, Bit 3
Filter 53Hz	1	1
Filter 215Hz	0	1
Filter 430Hz	0	0
Filter 860Hz	1	0

*Info: Settings for 53Hz, 215Hz, 430Hz are as in SMA6*

- 1353 When the lock bit for customer programmable parameters is not set, during initialization phase 2 acceleration data will be transmitted. This is done by replacing each second status data telegram with the acceleration data word BSn. The overall duration of Iniphase2 is not influenced by this.
- 1354 During initialization phase 2 internally the selftest is applied, thus by evaluation of the BSn telegrams also the selftest response can be measured.
- 1355 If lockbit is set to one, then no acceleration data are transmitted in Initphase 2.
- 1356 Initialization data for lock bit for customer programmable parameters is not set:  
ID1, Data1, ID1, Sensor Data, ID1, Data1, ID1, Sensor Data, ID2, Data2, ID2, Sensor Data, ID2, Data2, ID2, Sensor Data, ....
- 442 Selftest is triggered automatically during Initialization phase 2 on CH1 and CH2 for four times positive deflection and four times negative deflection. Each deflection of Ch1 and Ch2 has to be in opposite direction. Selftest is passed if one positive and one negative deflection per channel is inside limits.
- 4830 Bite deflections are done in opposite direction for channel 1 and channel 2. Ch1 is first deflected in negative, then in positive direction (referring to MOTP\_SIGN\_CHx=0, otherwise the direction is inverted at the PSI Interface):



3617

The evaluation of the selftest is done by comparing the stored limits with the actual BITE value. For the negative BITE the limits are inverted. The implementation is shown in the picture below. The red lines are the limits for the selftest.

The limits are always compared to the output signal of a 10bit PSI mode.

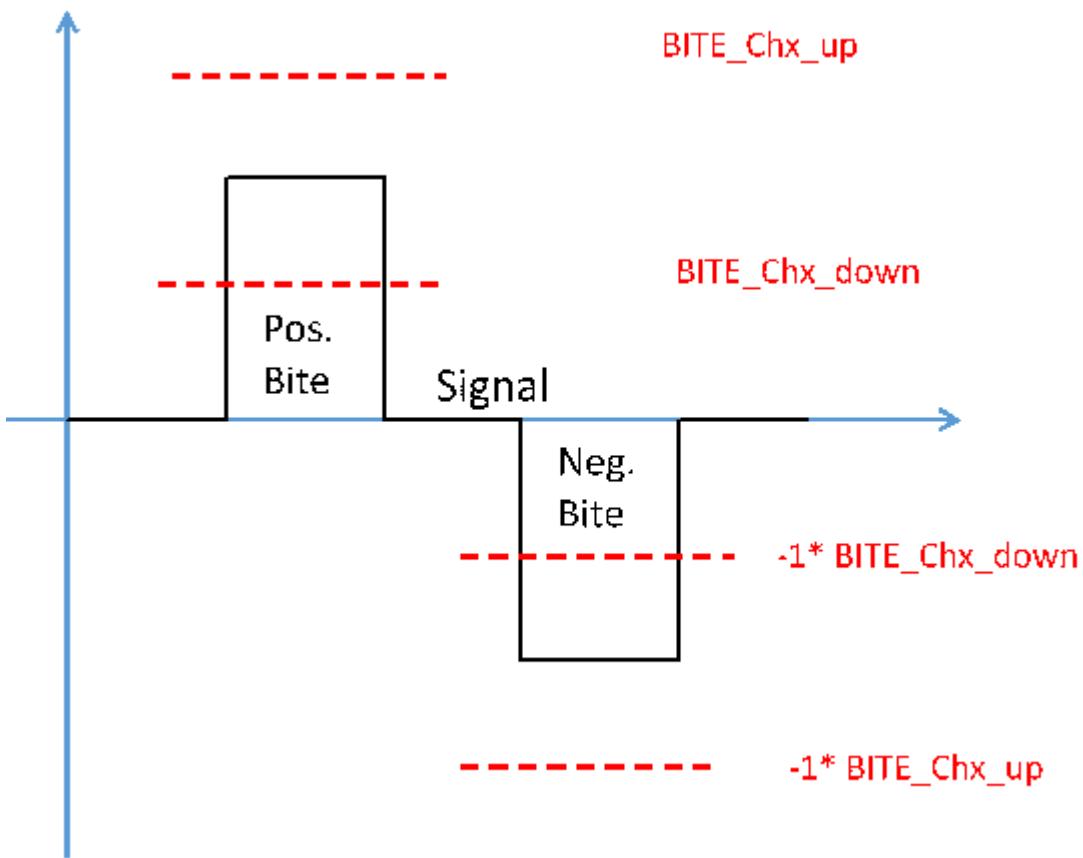
To measure the actual BITE value one sample is taken before applying the selftest voltage and one sample is taken with positive and negative selftest voltage applied. The measured offset, which was measured before applying the voltage, is subtracted from the measured BITE values before comparing them with the limits.

444

Two values for BITE limits per channel are stored in OTP as 8bit value (no sign bit) : Bite\_up and Bite\_dn. These Limits are stored separately for CH1 and CH2.

3620

Signal and tolerance band for channel 1 with the condition [BITE\_sign\_ch1]=0. (For channel 2 the behaviour is inverted. I.e. in this case the check is first done with negative limits.)

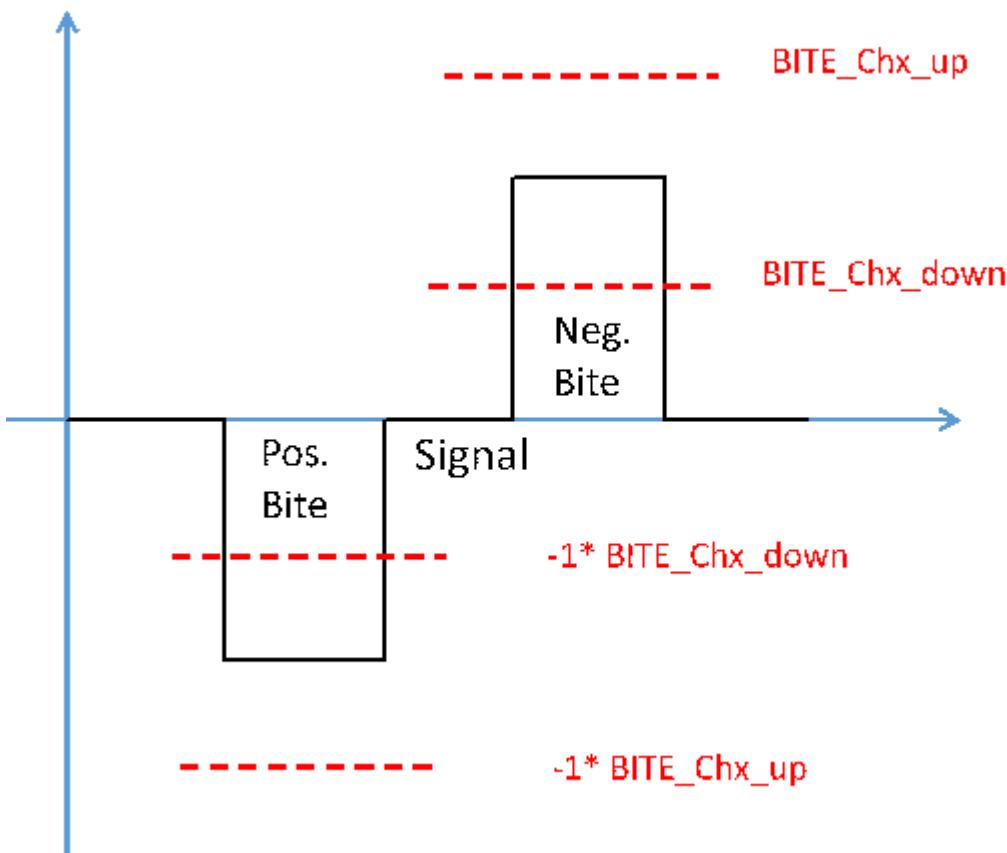


3622

With the [BITE\_sign\_chx] bits in OTP, it is possible to change the sign of the used limits for each channel. The bit only changes the sign of the limits. It has no influence on the signal.

3623

Signal and tolerance band for channel 1 with the condition [BITE\_sign\_ch1]=1. (For channel 2 the behaviour is inverted. I.e. in this case the check is first done with positive limits.) *The inversion of the signal is not done by [BITE\_sign\_chx], but by the MEMS element.*



4831 To pass the BITE test in current implementation the MOTP\_BITE\_SIGN\_CHx bits must be set to 0b1 for both channels.

443 BITE evaluation in PSI mode is done before inverter. Therefore the setting of the [sign\_chx] bit has no influence on the BITE sign.

3932 In PSI mode during BITE the gain of the digital signal path is halved (/2). This applies only to Normal PSI and not to Bidirectional PSI.

445 Bite limits are scaled according to used MEMS and sensitivity range.

3970 The BITE limits from OTP are scaled with the following factors (referring to 10bit PSI):

		CMA_type		
		120g	480g	800g
SMA_range		00	01	10
30g	011	factor 2	NA	NA
60g	100	factor 1	factor 1	NA
120g	000	0.5 if MOTP_BITE_TOL_SCALE_SEL=0 2 if MOTP_BITE_TOL_SCALE_SEL=1	factor 2	factor 2
240g	001	NA	factor 1	factor 1
480g	010	NA	factor 0.5	factor 0.5

3971 The following table shows which sensitivities are used to store the values in the OTP and which are the sensitivities during PSI BITE evaluation (referring to 10bit PSI):



		CMA_type			
10 bit		120g	480g	800g	
SMA_range		BITE limit in OTP			Sensitivity at Output
30g	011	4 LSB/g	NA	NA	8 LSB/g
60g	100	4 LSB/g	4 LSB/g	NA	4 LSB/g
120g	000	4LSB/g if MOTP_BITE_TOL_SCALE_SEL=0 1LSB/g if MOTP_BITE_TOL_SCALE_SEL=1	1 LSB/g	1 LSB/g	2 LSB/g
240g	001	NA	1 LSB/g	1 LSB/g	1 LSB/g
480g	010	NA	1 LSB/g	1 LSB/g	0.5 LSB/g

4081

This implementation leads to the following scaling factors for the 16bit PSI output:

		CMA_type			
		120g	480g	800g	
SMA range		00	01	10	
30g	011	8	NA	NA	NA
60g	100	8	8	NA	NA
120g	000	8 if MOTP_BITE_TOL_SCALE_SEL=0 32 if MOTP_BITE_TOL_SCALE_SEL=1	32	32	32
240g	001	NA	32	32	32
480g	010	NA	32	32	32

The following table shows which sensitivities are used to store the values in the OTP and which are the sensitivities during PSI BITE evaluation (referring to 16 bit PSI):

		CMA_type			
16 bit		120g	480g	800g	
SMA_range		BITE limit in OTP			Sensitivity at Output
30g	011	4 LSB/g	NA	NA	32 LSB/g
60g	100	4 LSB/g	4 LSB/g	NA	32 LSB/g
120g	000	4LSB/g if MOTP_BITE_TOL_SCALE_SEL=0 1LSB/g if MOTP_BITE_TOL_SCALE_SEL=1	1 LSB/g	1 LSB/g	32 LSB/g
240g	001	NA	1 LSB/g	1 LSB/g	32 LSB/g
480g	010	NA	1 LSB/g	1 LSB/g	32 LSB/g

446

Bite is evaluated after Sensitivity calibration and offset regulation.

3894

During selftest the 430Hz filter mode is used, regardless of the filter setting in OTP.

3621

If all four selftest attempts failed for at least one channel, a "sensor defect" message is send.

ID	parameter / condition	min	typ	max	unit
2891 ASIL_D	Self Test Duration (PSI5) PSI5-Types; ( 3.6ms * 4 * 4 )	55.0	57.6	61.5	ms

3625

In the OTP [FOC\_limit] the maximum allowed residual offset in LSB is stored. In Initphase 2, the remaining offset is compared with this value. This is only done after the BITE evaluation is finished.

It is done by taking one sample, if:

- the OTP bit [FOC\_mean]=1 or
- the OTP bit [FOC\_mean]= 0 and asynchronous mode is selected or
- the OTP bit [FOC\_mean]= 0 and synchronous mode with 250µs is selected



If the remaining offset exceeded the stored limits, the sensor sends a "sensor defect" message in Initphase 3.

3933 If the OTP bit [FOC\_mean]=0 and a synchron mode with 500µs or higher syncpulse is selected, the remaining offset is evaluated by taking 512 samples and calculating the average value of this samples. This average is compared with the limit from OTP [FOC\_limit].

If the remaining offset exceeded the stored limits, the sensor sends a "sensor defect" message in Initphase 3.

5402 For all SMA7 types FOC\_mean=0 is programmed during final test.

5401 For synchronous communication modes with 350 us sync pulse distance it is mandatory to set MOTP\_FOC\_MEAN=1. Otherwise the BITE test and FOC mean time calculation would exceed the duration of the init 2 phase.

4355 If [FOC\_limit] is set to 0, the check of the residual offset is deactivated.

### 6.3.4 Initialization Phase 3

1358 After having completed initialization phase 2, the sensor transmits a status message.

1359 If the fast offset cancellation and the self test were passed successfully, a message is transmitted indicating that the sensor is ready for normal operation.

1360 If an error was detected, the sensor will send the status message "Defect" and the corresponding error code, as detailed below.

1391 Before end of Init phase 3 the sensor activates the slow offset cancellation, if the OTP bit [OFS\_SOC\_DISABLE]=0.

#### 6.3.4.1 Sensor Status "OK"

1362 The actual "Sensor Status OK" message to be sent depends on the lock status of the sensor. As long as the lock bit of the customer OTP area has not been set but lock bits L0 and L1 (Wafer level and SMA area) have been set, the sensor sends the status message "Sensor Ready, unlocked" (+486).

1363 Upon setting all lock bits a successful initialization is confirmed by "Sensor Ready" (+487, 0x1E7).

1364 Having transmitted this sequence of sensor ready messages (32 times for asynchronous modes or 16 times for synchronous modes), the SMA7 will start to send acceleration data.

#### 6.3.4.2 Sensor Status "Defect"

1366 If an error was detected the sensor will transmit a sequence of the corresponding error message during initialization phase 3 until power-down.

1367 The sensor sends the following sequence of error messages to the ECU:

ASIL\_D

Message 1 - 0x1F4 (+500 = "Sensor Defect")

Message 2 - 0x1F4 (+500 = "Sensor Defect")

Message 3 - 0x1F4 (+500 = "Sensor Defect")

...

Message 14 - 0x1F4 (+500 = "Sensor Defect")

Message 15 - 0x1F4 (+500 = "Sensor Defect")

Message 16 - Error Code

Message 17 - 0x1F4 (+500 = "Sensor Defect")

Message 18 - Error Code

Message 19 - 0x1F4 (+500 = "Sensor Defect")

Message 20 - Error Code

... till power down

4356 The following table shows the detailed behaviour in case of incorrect lock bits:



Prom_lock_bit (2-0) (MOTP_LOCK_BIT_PAS/SMA/ASIC)	Sensor message in INIT3	Send value in INIT
000	sensor defekt + general asic failure	+500/1F4
001	sensor defekt + general asic failure	+500/1F4
010	sensor defekt + general asic failure	+500/1F4
011	sensor ready, unlocked (lock_bit 0,1 set)	+486/1E6
100	sensor defekt + general asic failure	+500/1F4
101	sensor defekt + general asic failure	+500/1F4
110	sensor defekt + general asic failure	+500/1F4
111	sensor ready, locked (all bits are set)	+487/1E7

### 6.3.5 Normal Operation

1390 If the initialization phase 3 was completed with the “Sensor Status: OK” message (“Sensor Ready, unlocked” (+486) or “Sensor Ready” (+487, 0x1E7)), SMA7 will enter the normal operation mode. If no error is detected, the sensor will transmit acceleration data according to the chosen PSI5 mode until power-down.

1393 If an error was detected during normal operation the sensor will transmit the status “defect” datagram and the corresponding error-code datagram starting with the next datagram till power down. ASIL\_D

## 6.4 Transmission Modes

### 6.4.1 Summary of Transmission Modes

1061 The SMA7 features a variety of asynchronous and synchronous communication modes as described in the following sections. The transmission modes are denominated according to the definition given by PSI5 specification v1.3 and 2.1 and are summarized in the table below.



## Overview of PSI modes (1/4):

PSI_Mode (dec.)	PSI_Mode (bin)	Channel	Communication mode	Sync/Async	Word length	Data-rate	Time-slots	Timeslot Nr.	Sequence of Data	Sensor Data Bits	Advanced timing applicable
0	0000000	1 & 2	PSIS-P16CRC 500/2L	Sync	21	125	2	1:2	Sync 1 2 Sync 1 2 ....	14	no
1	0000001	2	PSIS-A10P 25Q'1L	Async	13	125	-	-	2 2 2 2 2 ....	10	no
2	0000010	1	PSIS-A10P 25Q'1H	Async	13	189	-	-	1 1 1 1 1 ....	10	no
3	0000011	2	PSIS-A10P 25Q'1H	Async	13	189	-	-	2 2 2 2 2 ....	10	no
4	0000100	1	PSIS-P10P 500/3L	Sync	13	125	3	1	Sync 1 .. Sync 1 .. ....	10	no
5	0000101	1	PSIS-P10P 500/3L	Sync	13	125	3	2	Sync 1 .. Sync 1 .. ....	10	no
6	0000110	1	PSIS-P10P 500/3L	Sync	13	125	3	3	Sync .. 1 Sync .. 1 ....	10	no
8	0001000	1	PSIS-P10P 500/4H	Sync	13	189	4	1	Sync 1 .. Sync 1 .. ....	10	no
9	0001001	1	PSIS-P10P 500/4H	Sync	13	189	4	2	Sync 1 .. Sync 1 .. ....	10	no
10	0001010	1	PSIS-P10P 500/4H	Sync	13	189	4	3	Sync .. 1 Sync .. 1 ....	10	no
11	0001011	1	PSIS-P10P 500/4H	Sync	13	189	4	4	Sync .. 1 Sync .. 1 ....	10	no
14	0001110	1	PSIS-S10P500/3L	Sync	13	125	3	-	....	10	no
15	0001111	2	PSIS-S10P500/3L	Sync	13	125	3	-	....	10	no
16	0010000	2	PSIS-P10P 500/3L	Sync	13	125	3	1	Sync 2 .. Sync 2 .. ....	10	no
17	0010001	2	PSIS-P10P 500/3L	Sync	13	125	3	2	Sync 2 .. Sync 2 .. ....	10	no
18	0010010	2	PSIS-P10P 500/3L	Sync	13	125	3	3	Sync .. 2 Sync .. 2 ....	10	no
20	0010100	2	PSIS-P10P 500/4H	Sync	13	189	4	1	Sync 2 .. Sync 2 .. ....	10	no
21	0010101	2	PSIS-P10P 500/4H	Sync	13	189	4	2	Sync 2 .. Sync 2 .. ....	10	no
22	0010110	2	PSIS-P10P 500/4H	Sync	13	189	4	3	Sync .. 2 Sync .. 2 .. ....	10	no
23	0010111	2	PSIS-P10P 500/4H	Sync	13	189	4	4	Sync .. 2 Sync .. 2 .. ....	10	no
26	0011010	1	PSIS-S10P500/4H	Sync	13	189	4	-	....	10	no
27	0011011	2	PSIS-S10P500/4H	Sync	13	189	4	-	....	10	no
28	0011100	1	PSIS-A10P 25Q'1L	Async	13	125	-	-	1 1 1 1 1 ....	10	no
29	0011101	1 & 2	PSIS-P10P 500/4H	Sync	13	189	4	1:2	Sync 1 2 .. Sync 1 2 .. ....	10	no
30	0011110	1 & 2	PSIS-P10P 500/4H	Sync	13	189	4	3:4	Sync .. 1 2 Sync .. 1 2 ....	10	no
32	0100000	1	PSIS-P16CRC 500/2L	Sync	21	125	2	1	Sync 1 .. Sync 1 .. ....	14	no
33	0100001	1	PSIS-P16CRC 500/2L	Sync	21	125	2	2	Sync 1 .. Sync 1 .. ....	14	no
34	0100010	1 & 2	PSIS-P20CRC 500/2L (16+4bits)	Sync	25	125	2	1:2	Sync 1 2 Sync 1 2 ....	14	yes
35	0100011	2 & 1	PSIS-P20CRC 500/2L (16+4bits)	Sync	25	125	2	1:2	Sync 2 1 Sync 2 1 ....	14	yes
36	0100100	1	PSIS-P20CRC 500/2L(16+4bits)	Sync	25	125	2	1	Sync 1 .. Sync 1 .. ....	14	yes
37	0100101	1	PSIS-P20CRC 500/2L(16+4bits)	Sync	25	125	2	2	Sync 1 .. Sync 1 .. ....	14	yes
38	0100110	1 & 2	PSIS-P10CRC 500/4H	Sync	15	189	4	1:2	Sync 1 2 .. Sync 1 2 .. ....	10	yes
39	0100111	2 & 1	PSIS-P10CRC 500/4H	Sync	15	189	4	1:2	Sync 2 1 .. Sync 2 1 .. ....	10	yes



**BOSCH**

Department AE/ESI

## Internal Datasheet SMA7

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Date 17/01/2022

1.279.929.850

PSI_Mode (dec.)	PSI_Mode (bin)	Channel	Communication mode	Sync/ Async	Word length	Data- rate	Time- slots	Timeslot Nr.	Sequence of Data	Sensor Data Bits	Advanced timing applicable
40	0101000	1	PSI5 P10CRC 500/3L	Sync	15	125	3	1	Sync 1 · Sync 1 · ...	10	yes
41	0101001	1	PSI5 P10CRC 500/3L	Sync	15	125	3	2	Sync 1 · Sync 1 · ...	10	yes
42	0101010	1	PSI5 P10CRC 500/3L	Sync	15	125	3	3	Sync 1 · Sync 1 · ...	10	yes
43	0101011	1 & 2	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	1:2	Sync 12 · Sync 12 · ...	14	yes
44	0101100	2	PSI5 P10CRC 500/3L	Sync	15	125	3	1	Sync 2 · Sync 2 · ...	10	yes
45	0101101	2	PSI5 P10CRC 500/3L	Sync	15	125	3	2	Sync 2 · Sync 2 · ...	10	yes
46	0101110	2	PSI5 P10CRC 500/3L	Sync	15	125	3	3	Sync 2 · Sync 2 · ...	10	yes
48	0110000	1	PSI5 P10CRC 500/4H	Sync	15	189	4	1	Sync 1 · Sync 1 · ...	10	yes
49	0110001	1	PSI5 P10CRC 500/4H	Sync	15	189	4	2	Sync 1 · Sync 1 · ...	10	yes
50	0110010	1	PSI5 P10CRC 500/4H	Sync	15	189	4	3	Sync 1 · Sync 1 · ...	10	yes
51	0110011	1	PSI5 P10CRC 500/4H	Sync	15	189	4	4	Sync 1 · Sync 1 · ...	10	yes
52	0110100	2	PSI5 P10CRC 500/4H	Sync	15	189	4	1	Sync 2 · Sync 2 · ...	10	yes
53	0110101	2	PSI5 P10CRC 500/4H	Sync	15	189	4	2	Sync 2 · Sync 2 · ...	10	yes
54	0110110	2	PSI5 P10CRC 500/4H	Sync	15	189	4	3	Sync 2 · Sync 2 · ...	10	yes
55	0110111	2	PSI5 P10CRC 500/4H	Sync	15	189	4	4	Sync 2 · Sync 2 · ...	10	yes
56	0111000	1	PSI5 P16CRC 500/3H	Sync	21	189	3	1	Sync 1 · Sync 1 · ...	14	no
57	0111001	1	PSI5 P16CRC 500/3H	Sync	21	189	3	2	Sync 1 · Sync 1 · ...	14	no
58	0111010	1	PSI5 P16CRC 500/3H	Sync	21	189	3	3	Sync 1 · Sync 1 · ...	14	no
60	0111100	2	PSI5 P16CRC 500/3H	Sync	21	189	3	1	Sync 2 · Sync 2 · ...	14	no
61	0111101	2	PSI5 P16CRC 500/3H	Sync	21	189	3	2	Sync 2 · Sync 2 · ...	14	no
62	0111110	2	PSI5 P16CRC 500/3H	Sync	21	189	3	3	Sync 2 · Sync 2 · ...	14	no
63	0111111	2 & 1	PSI5 P10P 500/3L	Sync	13	125	3	1:2	Sync 21 · Sync 21 · ...	10	no
64	1000000	1	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	1	Sync 1 · Sync 1 · ...	14	yes
65	1000001	1	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	2	Sync 1 · Sync 1 · ...	14	yes
66	1000010	1	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	3	Sync 1 · Sync 1 · ...	14	yes
67	1000011	1 & 2	PSI5 P10CRC 500/3L	Sync	15	125	3	1:2	Sync 12 · Sync 12 · ...	10	yes
68	1000100	2	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	1	Sync 2 · Sync 2 · ...	14	yes
69	1000101	2	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	2	Sync 2 · Sync 2 · ...	14	yes
70	1000110	2	PSI5 P20CRC 500/3H (16+4bits)	Sync	25	189	3	3	Sync 2 · Sync 2 · ...	14	yes
71	1000111	2 & 1	PSI5 P10CRC 500/3L	Sync	15	125	3	1:2	Sync 21 · Sync 21 · ...	10	yes
72	1001000	1 & 2	PSI5 P20CRC 500/3H (10+10bits)	Sync	25	189	3	1	Sync 12 · Sync 12 · ...	10+10	yes
73	1001001	1 & 2	PSI5 P20CRC 500/3H (10+10bits)	Sync	25	189	3	2	Sync 12 · Sync 12 · ...	10+10	yes
74	1001010	1 & 2	PSI5 P20CRC 500/3H (10+10bits)	Sync	25	189	3	3	Sync 12 · Sync 12 · ...	10+10	yes
75	1001011	1 & 2	PSI5 P10P 500/3L	Sync	13	125	3	1:2	Sync 12 · Sync 12 · ...	10	no
76	1001100	2 & 1	PSI5 P20CRC 500/3H (10+10bits)	Sync	25	189	3	1	Sync 21 · Sync 21 · ...	10+10	yes
77	1001101	2 & 1	PSI5 P20CRC 500/3H (10+10bits)	Sync	25	189	3	2	Sync 21 · Sync 21 · ...	10+10	yes
78	1001110	2 & 1	PSI5 P20CRC 500/3H (10+10bits)	Sync	25	189	3	3	Sync 21 · Sync 21 · ...	10+10	yes
79	1001111	2 & 1	PSI5 P16CRC 500/2L	Sync	21	125	2	1:2	Sync 21 · Sync 21 · ...	14	no



## Overview of PSI modes (continued; 3/4):

PSI_Mode (dec.)	PSI_Mode (bin)	Channel	Communication mode	Sync/Async	Word length	Data-rate	Time-slots	Timeslot Nr.	Sequence of Data	Sensor Data Bits	Advanced timing applicable
80	1010000	2	PSIS P16CRC 500/2L	Sync	21	125	2	1	Sync 2 · Sync 2 · ....	14	no
81	1010001	2	PSIS P16CRC 500/2L	Sync	21	125	2	2	Sync 2 · Sync 2 · ....	14	no
82	1010010	2 & 1	PSIS P10P 500/4H	Sync	13	189	4	1,2	Sync 2 1 · Sync 2 1 · ....	10	no
83	1010011	2 & 1	PSIS P10P 500/4H	Sync	13	189	4	3,4	Sync · 2 1 Sync · 2 1 ....	10	no
84	1010100	2	PSIS P20CRC 500/2L(16+4bits)	Sync	25	125	2	1	Sync 2 · Sync 2 · ....	14	yes
85	1010101	2	PSIS P20CRC 500/2L(16+4bits)	Sync	25	125	2	2	Sync · 2 Sync · 2 · ....	14	yes
86	1010110	1 & 2	PSIS P16CRC 500/3H	Sync	21	189	3	1,2	Sync 1 2 · Sync 1 2 · ....	14	no
87	1010111	2 & 1	PSIS P16CRC 500/3H	Sync	21	189	3	1,2	Sync 2 1 · Sync 2 1 · ....	14	no
88	1011000	1	PSIS P10P 250/1L	Sync	13	125	1	1	Sync 1 · Sync 1 · ....	10	no
89	1011001	2 & 1	PSIS P20CRC 500/3H (16+4bits)	Sync	25	189	3	1,2	Sync 2 1 · Sync 2 1 · ....	14	yes
90	1011010	1 & 2	PSIS P20CRC 250/1H (10+10bits)	Sync	25	189	1	1	Sync 12 · Sync 12 · ....	10+10	no
91	1011011	2 & 1	PSIS P20CRC 250/1H (10+10bits)	Sync	25	189	1	1	Sync 21 · Sync 21 · ....	10+10	no
92	1011100	2	PSIS P10P 250/1L	Sync	13	125	1	1	Sync 2 · Sync 2 · ....	10	no
93	1011101	1 & 2	PSIS P20CRC 500/2L (10+10bits) 4 KHz sampling	Sync	25	125	2	1,2	Sync 12 12 Sync 12 12 · ....	10+10	yes
94	1011110	1 & 2	PSIS P20CRC 500/2L (10+10bits) 4 KHz sampling	Sync	25	125	2	1,2	Sync 21 21 Sync 21 21 · ....	10+10	yes
95	1011111	1 & 2	PSIS P20CRC 500/2H (10+10bits) 4 KHz sampling	Sync	25	189	2	1,2	Sync 12 12 Sync 12 12 · ....	10+10	no
96	1100000	1 & 2	PSIS P20CRC 500/2H (10+10bits) 4 KHz sampling	Sync	25	189	2	1,2	Sync 21 21 Sync 21 21 · ....	10+10	no
97	1100001	1 & 2	PSIS P10CRC 500/4H	Sync	15	189	4	3,4	Sync · 1 2 Sync · 1 2 · ....	10	yes
98	1100010	2 & 1	PSIS P10CRC 500/4H	Sync	15	189	4	3,4	Sync · 2 1 Sync · 2 1 · ....	10	yes
99	1100011	1	PSIS P16CRC 1000/4H	Sync	21	189	4	1	Sync 1 · Sync 1 · ....	16	no
100	1100100	1	PSIS P16CRC 1000/4H	Sync	21	189	4	2	Sync 1 · Sync 1 · ....	16	no
101	1100101	1	PSIS P16CRC 1000/4H	Sync	21	189	4	3	Sync · 1 · Sync · 1 · ....	16	no
102	1100110	1	PSIS P16CRC 1000/4H	Sync	21	189	4	4	Sync · 1 · Sync · 1 · ....	16	no
103	1100111	2	PSIS P16CRC 1000/4H	Sync	21	189	4	1	Sync 2 · Sync 2 · ....	16	no
104	1101000	2	PSIS P16CRC 1000/4H	Sync	21	189	4	2	Sync 2 · Sync 2 · ....	16	no
105	1101001	2	PSIS P16CRC 1000/4H	Sync	21	189	4	3	Sync 2 · Sync 2 · ....	16	no
106	1101010	2	PSIS P16CRC 1000/4H	Sync	21	189	4	4	Sync · 2 Sync · 2 · ....	16	no
107	1101011	1 & 2	PSIS P16CRC 1000/4H	Sync	21	189	4	1,2	Sync 1 2 · Sync 1 2 · ....	16	no
108	1101100	1 & 2	PSIS P16CRC 1000/4H	Sync	21	189	4	3,4	Sync 1 2 Sync 1 2 · ....	16	no
8*	0001000	1	PSIS P10P 250/2H	Sync	13	189	2	1	Sync 1 · Sync 1 · ....	10	no
9*	0001001	1	PSIS P10P 250/2H	Sync	13	189	2	2	Sync · 1 · Sync · 1 · ....	10	no
20*	0010100	2	PSIS P10P 250/2H	Sync	13	189	2	1	Sync 2 · Sync 2 · ....	10	no
21*	0010101	2	PSIS P10P 250/2H	Sync	13	189	2	2	Sync 2 · Sync 2 · ....	10	no
29*	0011101	1 & 2	PSIS P10P 250/2H	Sync	13	189	2	1,2	Sync 1 2 · Sync 1 2 · ....	10	no
82*	1010010	2 & 1	PSIS P10P 250/2H	Sync	13	189	2	1,2	Sync 2 1 · Sync 2 1 · ....	10	no

\*) These mode use the same OTP programming as the corresponding P10P-500/4H modes. They can also be used as P10P-250/2H



PSI_Mode (dec.)	PSI_Mode (bin)	Channel	Communication mode	Sync/Async	Word length	Data-rate	Time-slots	Timeslot Nr.	Sequence of Data	Sensor Data Bits	Advanced timing applicable
99 *	1100011	1	PSI5_P16CRC-700/4H	Sync	21	189	4	1	Sync 1 ... Sync 1 ...	16	no
100 *	1100100	1	PSI5_P16CRC-700/4H	Sync	21	189	4	2	Sync 1 ... Sync 1 ...	16	no
101 *	1100101	1	PSI5_P16CRC-700/4H	Sync	21	189	4	3	Sync 1 ... Sync 1 ...	16	no
102 *	1100110	1	PSI5_P16CRC-700/4H	Sync	21	189	4	4	Sync 1 ... Sync 1 ...	16	no
103 *	1100111	2	PSI5_P16CRC-700/4H	Sync	21	189	4	1	Sync 2 ... Sync 2 ...	16	no
104 *	1101000	2	PSI5_P16CRC-700/4H	Sync	21	189	4	2	Sync 2 ... Sync 2 ...	16	no
105 *	1101001	2	PSI5_P16CRC-700/4H	Sync	21	189	4	3	Sync 2 ... Sync 2 ...	16	no
106 *	1101010	2	PSI5_P16CRC-700/4H	Sync	21	189	4	4	Sync 2 ... Sync 2 ...	16	no
107 *	1101011	1 & 2	PSI5_P16CRC-700/4H	Sync	21	189	4	1,2	Sync 1 2 ... Sync 1 2 ...	16	no
108 *	1101100	1 & 2	PSI5_P16CRC-700/4H	Sync	21	189	4	3,4	Sync 1 2 ... Sync 1 2 ...	16	no

\*) These modes use the same OTP programming as the corresponding PSI5-P16CRC-1000/4H modes.  
They can also be used as PSI5-P16CRC-700/4H.

#### 6.4.2 Asynchronous Data Transmission

The sensor sends data to the ECU periodically without any external synchronization pulse.  
The data has been sampled about 5µs before start of transmission.

ID	parameter / condition	min	typ	max	unit
3090	Sampling time  (The internal sensor data which need to be sent as PSI datagram is sampled at a particular instance of time.)  Async Modes; Time after start of S1 bit	105	112	120	ns

Any  $t_{CYCLE}$ , the actual sensor value is transmitted in a 13 bit message.

Each message consists of two start bits S1=0 and S2=0, 10 data bits D0-D9 and one even parity bit P.  
One sensor data block is represented by one PSI5 data frame of length  $t_{FRAME} = 13 \cdot t_{BIT}$

##### 6.4.2.1 A10P-250/1L

ID	parameter / condition	min	typ	max	unit
1084	Datagram frame time  $t_{Frame} = 13 \cdot t_{Bit}$	98.8	105.3	109.2	µs
1085	Cycle time (sensor)  $t_{Cycle}$	216.7	229.0	239.6	µs

##### 6.4.2.2 A10P-250/1H

ID	parameter / condition	min	typ	max	unit
1092	Datagram frame time  $t_{Frame} = 13 \cdot t_{Bit}$	65	70.2	72.8	µs
1093	Cycle time (sensor)	216.7	229.0	239.6	µs



ID	parameter / condition	min	typ	max	unit
	t <sub>Cycle</sub>				

#### 6.4.3 Synchronous Data Transmission

1098 In synchronous transmission modes the sensors send their datagrams time-shifted to the ECU. A time slot is assigned to each sensor in which it sends the data.

1099 The synchronization is achieved by a voltage synchronization pulse sent by the ECU. All sensors in the bus configuration are numbered by hard programming.

1100 Sensor 1 sends after a defined time of after having received the sync pulse. Sensor 2 sends after a delay, so Sensor 1 can finish its transmission etc.

##### 6.4.3.1 Sampling time

4717 The sample timing (time point at which sensor data is captured at the output of the signal processing chain) is defined by 2 OTP bits (MOTP\_SAMPLE\_TIMING) in register MOTP\_PAS\_CONFIG\_6. It can be configured for all sync modes except 500µs modes with 4kHz sample rate (PSI-mode #93-#96):

ID	parameter / condition	min	typ	max	unit
3089	Sampling time (option 1)  Sync modes  OTP bit[SAMPLE_TIMING]=b00; Time after reaching V <sub>trigger</sub> ; for both channels	5.91	6.26	7.0	µs
4718	Sampling time (option2), no advanced transmission timing  Sync modes OTP bit[SAMPLE_TIMING]=b01; Referred to t <sub>or</sub> ; for both channels	46.3	49.2	52.0	µs
4719	Sampling time (option2) with advanced transmission timing (ATT) active  sync pulse distance (t_cycle)=500µs With activated ATT the sample timing is adjusted depending on the sync pulse distance in the same way as the transmission timing.  OTP bit[SAMPLE_TIMING]=b01; Referred to t <sub>or</sub> ; for both channels	48.2	48.8	50.4	µs
4720	Sampling time (option 4), 125kBit Mode, no advanced transmission timing  OTP bit[SAMPLE_TIMING]=0b11; Time before data D0 bit in the corresponding time slot. Exception PSI 16+4 bit mode: Time before data ID0 bit in the corresponding time slot.	3.69	4	4.38	µs
4722	Sampling time (option 4), 189kBit Mode, no advanced transmission timing  OTP bit[SAMPLE_TIMING]=0b11; Time before data D0 bit in the corresponding time slot.	2.42	2.69	2.92	µs



ID	parameter / condition	min	typ	max	unit
	Exception PSI 16+4 bit mode: Time before data ID0 bit in the corresponding time slot.				
4723	Sampling time (option 4), 125kBit Mode, with advanced transmission timing (ATT) active  sync pulse distance ( $t_{cycle}$ )=500μs With activated ATT the sample timing is adjusted depending on the sync pulse distance in the same way as the transmission timing.  OTP bit[SAMPLE_TIMING]=0b11; Time before data D0 bit in the corresponding time slot. Exception PSI 16+4 bit mode: Time before data ID0 bit in the corresponding time slot.	3.66	4	4.38	μs
4724	Sampling time (option 4), 189kBit Mode, with advanced transmission timing (ATT) active  sync pulse distance ( $t_{cycle}$ )=500μs With activated ATT the sample timing is adjusted depending on the sync pulse distance in the same way as the transmission timing.  OTP bit[SAMPLE_TIMING]=0b11; Time before data D0 bit in the corresponding time slot. Exception PSI 16+4 bit mode: Time before data ID0 bit in the corresponding time slot.	2.3	2.67	2.98	μs

4725

For the PSI modes with 500μs sync pulse distance and 4kHz sample rate (Mode #93 - #96) sampling time option 1 (OTP bit[SAMPLE\_TIMING]=b00) must be used.

ID	parameter / condition	min	typ	max	unit
4726	Sampling time (option 1), data for first time slot  OTP bit[SAMPLE_TIMING]=b00; Time after reaching $V_{trigger}$ ; for both channels; Modes #93-96; $t_{sample}$ 1	5.91	6.26	7.00	μs
5292	Sampling time (option 1), data for second time slot, without advanced transmission timing (ATT) active  PSI mode = {#95 #96}, “sample_timing” bits in OTP = 0b00, advanced timing = OFF	243.1	257.6	269.4	μs
4727	Sampling time (option 1), data for second time slot, with advanced transmission timing (ATT) active  sync pulse distance ( $t_{cycle}$ )=500μs With activated ATT the sample timing is adjusted depending on the sync pulse distance in the same way as the transmission timing.	253.3	256.0	259.4	μs



ID	parameter / condition	min	typ	max	unit
	OTP bit[SAMPLE_TIMING]=b00; Time after reaching $V_{trigger}$ ; for both channels; Modes #93,94 ; t_sample 2				

#### 6.4.3.2 Advanced transmission timing (ATT)

- 4855 Some synchronous transmission modes require the advanced transmission timing feature to fulfil the PSI5 timing requirements and avoid bus collisions on the PSI5 bus. If a mode needs ATT or not, is documented in the overview of the transmission modes and in the detailed description of every mode. It is mandatory to activate ATT for the modes, which need it, and deactivate it for all other modes.
- 4856 Advanced timing gets activated by setting OTP bit MOTP\_ADV\_TIMING=1.
- 4854 Target of advanced timing is to adjust the PSI transmission parameters
- a) start times of single time slots within a PSI frame
  - b) time slot length

This is needed as both parameters are based on internal oscillator clock. Therefore the tolerance of this parameters equals the tolerance of the internal oscillator, if ATT is deactivated.

Examples:

1. Internal oscillator faster than nominal frequency:

Without advanced timing sending of time slots would happen earlier, time slot length would be shortened.

2. Internal oscillator slower than nominal frequency:

Without advanced timing sending of time slots would happen later, time slot length would be prolonged.

Advanced timing uses the distance between syncpulses as a frequency reference to do adjustment of upper transmission parameters. This keeps the time slot start at their defined default positions and the time slot lengths at their nominal value.

- 4857 If Advanced Timing is active, then the numbers of internal oscillator clock cycles per synchronization cycle (sync pulse period) is counted. The measured number of clock cycles per synchronization cycle is compared to the nominal number. Depending on the deviation the start time of the time slot and the bit rate are modified at the next synchronization cycle.  
For example, if the measured number of clock cycles is higher than the typical value then oscillator clock frequency is higher than typical. In this case, at the next synchronization cycle frame transmission is started at higher time slot counter values to compensate for the higher clock frequency. Further, subsequent data bits are started at higher bit rate counter values to compensate for the higher clock frequency.  
When advanced timing is in-active, slot start time and bit rate are set to typical values, no adjustment is done.

- 4858 If advanced timing is activated, the sensor needs at least two valid sync pulse to do a correct timing adjustment. Therefore if advanced timing is activated, the sensor will not answer to the first received sync pulse after end of phase Init 1. Instead it will start communication after having received the second valid sync pulses after end of phase Init 1. (If ATT is deactivated it will answer after the first valid sync pulse in phase Init 2.) This behaviour assures that the first transmission will already have the correct timings.

- 4859 For application on the same PSI bus, it is recommended to use only sensors, which use the same advanced transmission timing algorithm.

- 4860 The following table shows the deviation ranges detected and the derived timing adjustments:



Index	F <sub>osc,lower</sub> [MHz]	F <sub>osc,upper</sub> [MHz]	Timing Correction
0	<16.2		(*)
1	16.20	16.92	-5.5%
2	16.92	17.10	-4.5%
3	17.10	17.28	-3.5%
4	17.28	17.46	-2.5%
5	17.46	17.64	-1.5%
6	17.64	17.82	-0.4%
7	17.82	18.18	0.6%
8	18.18	18.36	1.6%
9	18.36	18.54	2.6%
10	18.54	18.72	3.6%
11	18.72	18.90	4.6%
12	18.90	19.08	5.6%
13	19.08	19.80	6.6%
14	>19.8		(*)

(\*) If the oscillator frequency or the period between two consecutive sync pulses results in a measured deviation exceeding the maximum range of +/-10% within one observation period (distance between two consecutive sync pulses) then the last valid timing adjustment value will be retained.

4912

Example: Assuming a nominal start time of first time slot of 49µs and an actual oscillator frequency of 18.5MHz. Without advanced timing this will result in a slot start time of  $49\mu s \times 17.9\text{MHz} / 18.5\text{MHz} = 47.41\mu s$ .

With activated ATT this will be corrected by 2.6%:  $47.41\mu s \times 1.026 = 48.64\mu s$  (this equals a remaining error of 0.7% instead of 3.3%).

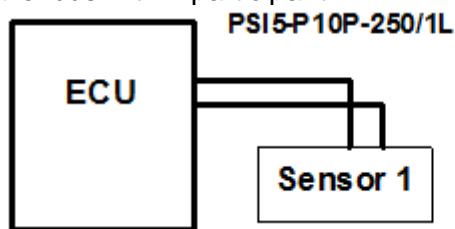
#### 6.4.3.3 P10P-250/1L

1113

In the PSI5-P10P-250/1L bus configuration a maximum number of one sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

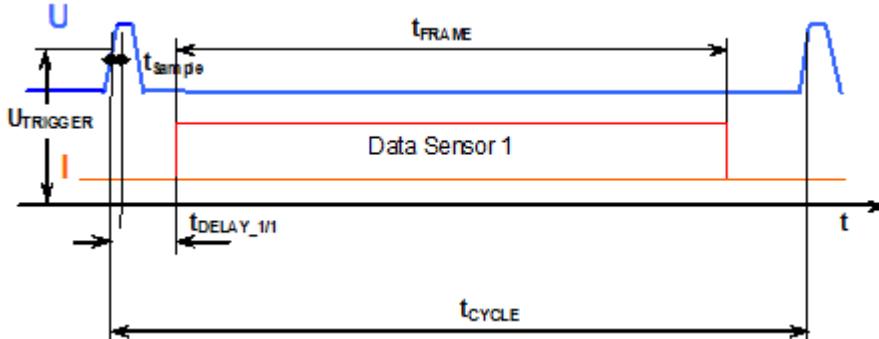
1114

Setup of PSI5 parallel bus with 1 participant:



1117

Timing of PSI5 parallel bus with 1 participant:



1118

The following timing has to be guaranteed by the ECU and sensors.



ID	parameter / condition	min	typ	max	unit
1119	Start of datagram $t_{delay\_1/1}$	44.1	50.1	54.4	μs
1120	End of datagram	143.7	154.7	163.6	μs
1121	Bit time $t_{Bit}$		8.1		μs
1122	Datagram frame time $t_{Frame} = 13 \cdot t_{Bit}$		104.6		μs
1123	Cycle time (ECU) *) $t_{Cycle}$	247.5	250	252.5	μs

1124

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

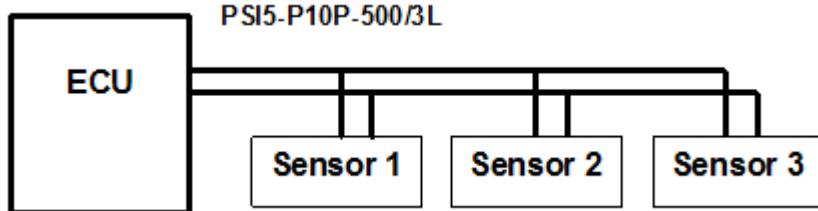
#### 6.4.3.4 P10P-500/3L

1126

In the PSI5-P10P-500/3L bus configuration a maximum number of three sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

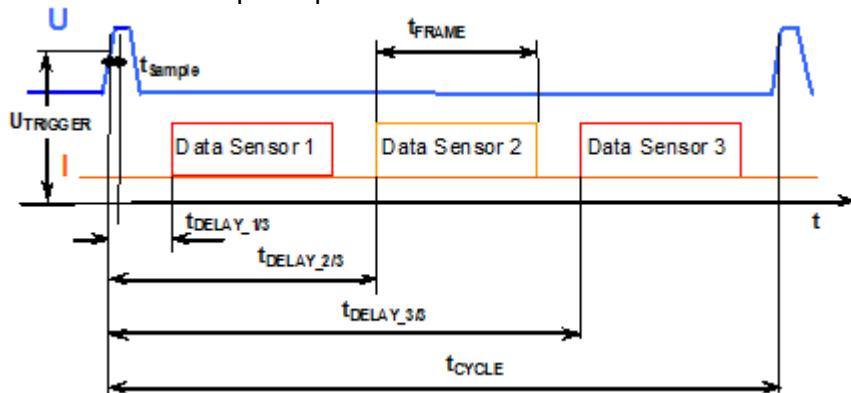
1127

Setup of PSI5 parallel bus with 3 participants:



1131

Timing of PSI5 parallel bus with 3 participants:



1132

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
1133	Start of 1 <sup>st</sup> datagram $t_{delay\_1/3}$	44.1	50.1	54.4	μs
1134	End of 1 <sup>st</sup> datagram	143.7	154.7	163.6	μs
1135	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/3}$	181.6	194.4	205.1	μs



ID	parameter / condition	min	typ	max	unit
1136	End of 2 <sup>nd</sup> datagram	281.2	299.0	314.3	µs
1137	Start of 3 <sup>rd</sup> datagram $t_{delay\_3/3}$	329.7	350.0	367.5	µs
1138	End of 3 <sup>rd</sup> datagram	429.3	454.6	476.6	µs
1139	Bit time $t_{Bit}$		8.1		µs
1140	Datagram frame time $t_{Frame} = 13 \cdot t_{Bit}$		104.6		µs
1141	Gap time between time slots $t_{Gap}$	8.4			µs
1142	Cycle time (ECU) *) $t_{Cycle}$	495	500	505	µs

1143

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

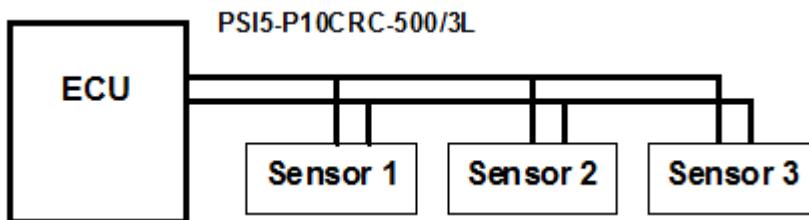
#### 6.4.3.5 P10CRC-500/3L

1145

In the PSI5-P10CRC-500/3L bus configuration a maximum number of three sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

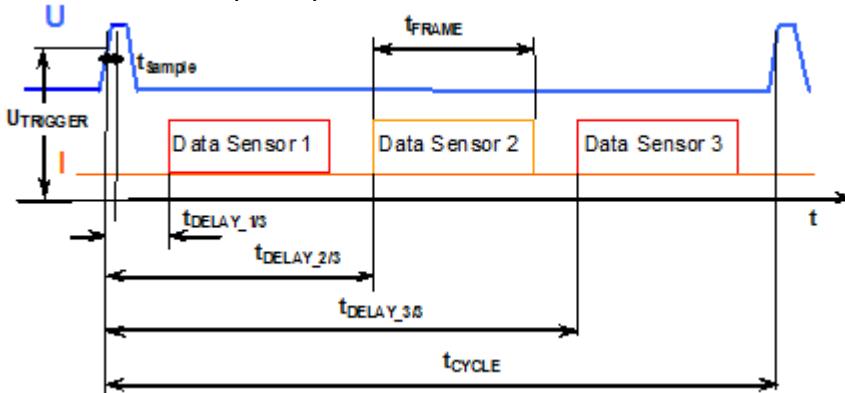
1146

Setup of PSI5 parallel bus with 3 participants:



1150

Timing of PSI5 parallel bus with 3 participants:



1151

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision. For this mode advanced transmission timing (ATT) must be activated to guarantee proper timing (already incl. in the following timings).

4357



ID	parameter / condition	min	typ	max	unit
1152	Start of 1 <sup>st</sup> datagram $t_{delay\_1/3}$	45.2	48.9	51.9	µs
1153	End of 1 <sup>st</sup> datagram	162.6	168.9	174.6	µs
1154	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/3}$	184.8	190.4	194.5	µs
1155	End of 2 <sup>nd</sup> datagram	302.2	310.4	317.3	µs
1156	Start of 3 <sup>rd</sup> datagram $t_{delay\_3/3}$	335.4	342.6	348.3	µs
1157	End of 3 <sup>rd</sup> datagram	452.7	462.6	470.8	µs
1158	Bit time $t_{Bit}$		8.1		µs
1159	Datagram frame time $t_{Frame} = 15 \cdot t_{Bit}$		120		µs
1160	Gap time between time slots $t_{Gap}$	8.4			µs
1161	Cycle time (ECU) <sup>*)</sup> $t_{Cycle}$	495	500	505	µs

1162

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

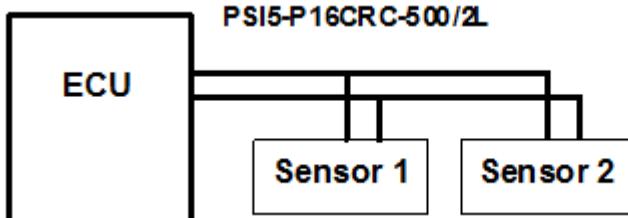
#### 6.4.3.6 P16CRC-500/2L

1164

In the PSI5-P16CRC-500/2L bus configuration a maximum number of two sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

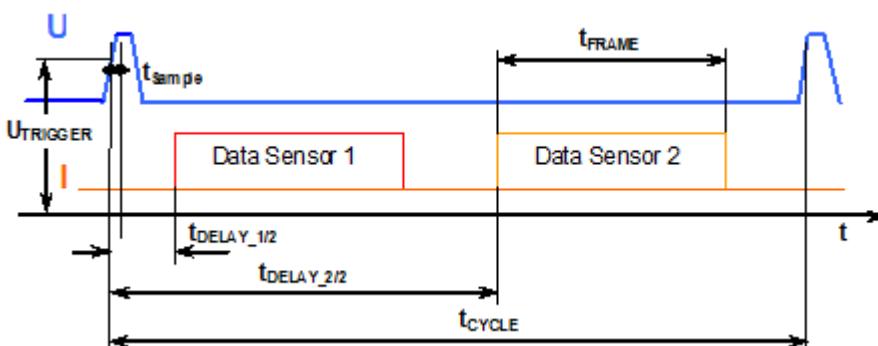
1165

Setup of PSI5 parallel bus with 2 participants:



1169

Timing of PSI5 parallel bus with 2 participants:



1170

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
1171	Start of 1 <sup>st</sup> datagram $t_{\text{delay\_1/2}}$	44.1	50.1	54.4	μs
1172	End of 1 <sup>st</sup> datagram	205.0	219.0	230.8	μs
1173	Start of 2 <sup>nd</sup> datagram $t_{\text{delay\_2/2}}$	256.5	273.1	287.2	μs
1174	End of 2 <sup>nd</sup> datagram	417.4	442.0	463.6	μs
1175	Bit time $t_{\text{bit}}$		8.1		μs
1176	Datagram frame time $t_{\text{frame}} = 21 \cdot t_{\text{bit}}$		168.9		μs
1177	Gap time between time slots $t_{\text{gap}}$	8.4			μs
1178	Cycle time (ECU) $t_{\text{cycle}}$	495	500	505	μs

1179

\*) The "Cycle Time (ECU)" stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

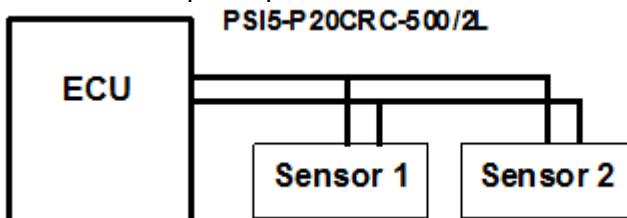
#### 6.4.3.7 P20CRC-500/2L

1181

In the PSI5-P20CRC-500/2L bus configuration a maximum number of two sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

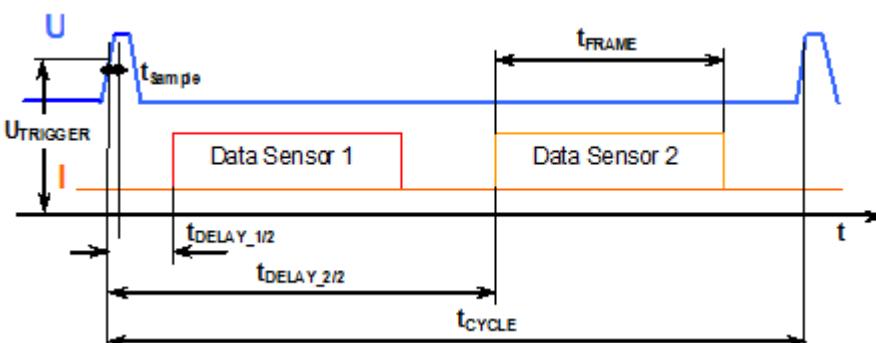
1182

Setup of PSI5 parallel bus with 2 participants:



1186

Timing of PSI5 parallel bus with 2 participants:

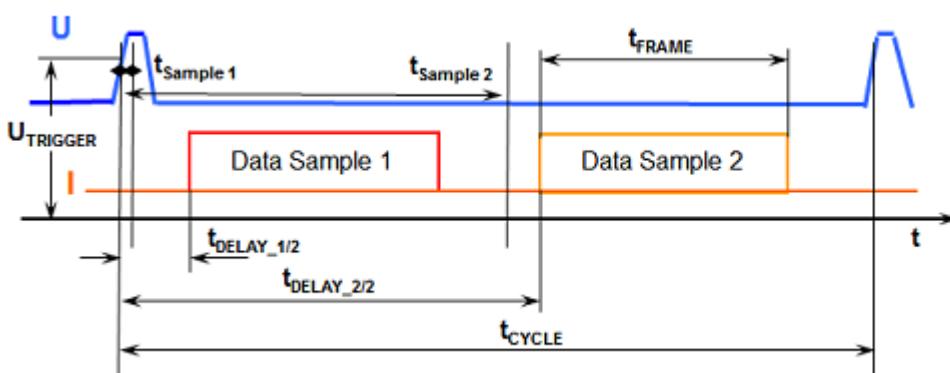


4733

This mode can also be used to send samples with 4kHz update rate, if the corresponding modes #93 or #94 are selected. In this case one sensor uses both timeslots. In the first timeslot the data from  $t_{sample1}$  is send. In the second timeslot the data from  $t_{sample2}$  is send.

4732

Timing of PSI5 parallel bus in 4kHz sampling configuration:



1187

4358

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision. For this mode advanced transmission timing (ATT) must be activated to guarantee proper timing (already incl. in the following timings).

ID	parameter / condition	min	typ	max	unit
1188	Start of 1 <sup>st</sup> datagram $t_{delay\_1/2}$	44.4	48.3	50.9	µs
1189	End of 1 <sup>st</sup> datagram	240.0	248.3	255.6	µs
1190	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/2}$	268.6	275.2	280.3	µs
1191	End of 2 <sup>nd</sup> datagram	464.5	475.2	484.8	µs
1192	Bit time $t_{Bit}$		8.1		µs
1193	Datagram frame time $t_{Frame} = 25 \cdot t_{Bit}$		200		µs
1194	Gap time between time slots $t_{Gap}$	8.4			µs
1195	Cycle time (ECU) $t_{Cycle}$	495	500	505	µs

1196

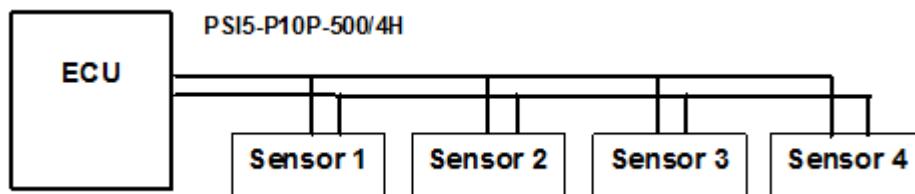


<sup>1198</sup>) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

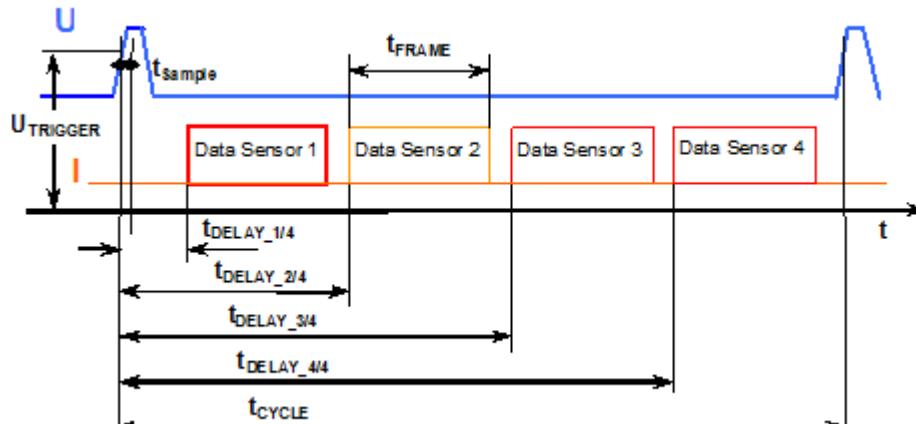
#### 6.4.3.8 P10P-500/4H

<sup>1199</sup> In the PSI5-P10P-500/4H bus configuration a maximum number of four sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

Setup of PSI5 parallel bus with 4 participants:



<sup>1203</sup> Timing of PSI5 parallel bus with 4 participants:



<sup>1204</sup> The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
1205	Start of 1 <sup>st</sup> datagram $t_{delay\_1/4}$	44.1	50.1	54.4	µs
1206	End of 1 <sup>st</sup> datagram	110.5	119.8	127.2	µs
1207	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/4}$	139.5	150.2	158.9	µs
1208	End of 2 <sup>nd</sup> datagram	205.9	219.9	231.7	µs
1209	Start of 3 <sup>rd</sup> datagram $t_{delay\_3/4}$	245.9	261.9	275.6	µs
1210	End of 3 <sup>rd</sup> datagram	312.3	331.7	348.3	µs
1211	Start of 4 <sup>th</sup> datagram $t_{delay\_4/4}$	363.3	385.3	404.3	µs
1212	End of 4 <sup>th</sup> datagram	429.7	455.0	477.1	µs
1213	Bit time $t_{Bit}$		5.4		µs



ID	parameter / condition	min	typ	max	unit
1214	Datagram frame time $t_{Frame} = 13 \cdot t_{Bit}$		69.7		μs
1215	Gap time between time slots $t_{Gap}$	5.6			μs
1216	Cycle time (ECU) *) $t_{Cycle}$	495	500	505	μs

1217

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

#### 6.4.3.9 P10P-250/2H

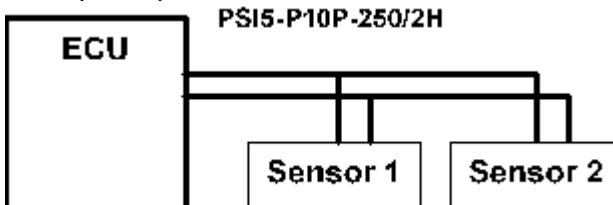
4751

In the PSI5-P10CP-250/2H bus configuration a maximum number of two sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

Except the ECU cycle time, this mode is identical to P10P-500/4H.

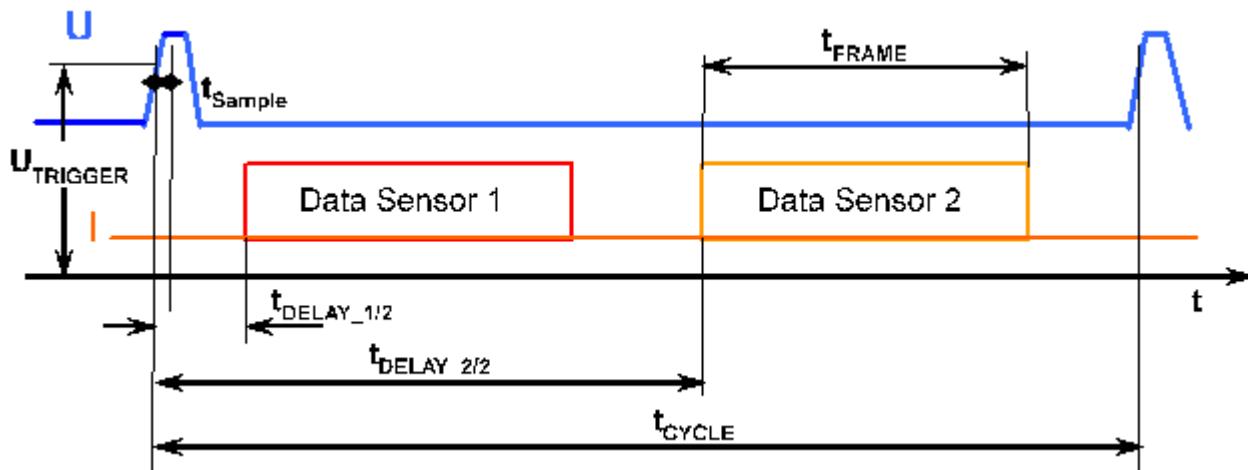
4752

Setup of PSI5 parallel bus with 2 participants:



4753

Timing of PSI5 parallel bus with 2 participants:



4754

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
4755	Start of 1st datagram $t_{delay\_1/2}$	44.1	50.1	54.4	μs
4756	End of 1st datagram	110.5	119.8	127.2	μs
4757	Start of 2nd datagram $t_{delay\_2/2}$	139.5	150.2	158.9	μs
4758	End of 2nd datagram	205.9	219.9	231.7	μs



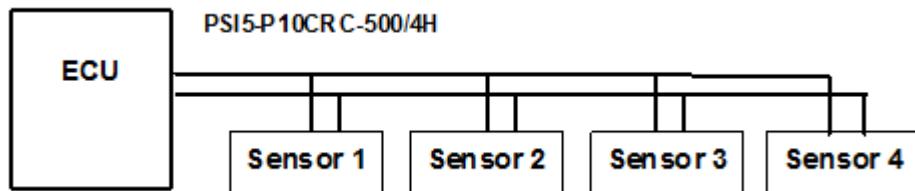
ID	parameter / condition	min	typ	max	unit
4759	Bit time $t_{\text{Bit}}$		5.4		$\mu\text{s}$
4760	Dataframe time $t_{\text{Frame}} = 13 \cdot t_{\text{Bit}}$		69.7		$\mu\text{s}$
4761	Gap time $t_{\text{Gap}}$	5.6			$\mu\text{s}$
4762	Cycle time (ECU) *) $t_{\text{Cycle}}$	247.5	250	252.5	$\mu\text{s}$

4763 \*) The "Cycle Time (ECU)" stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

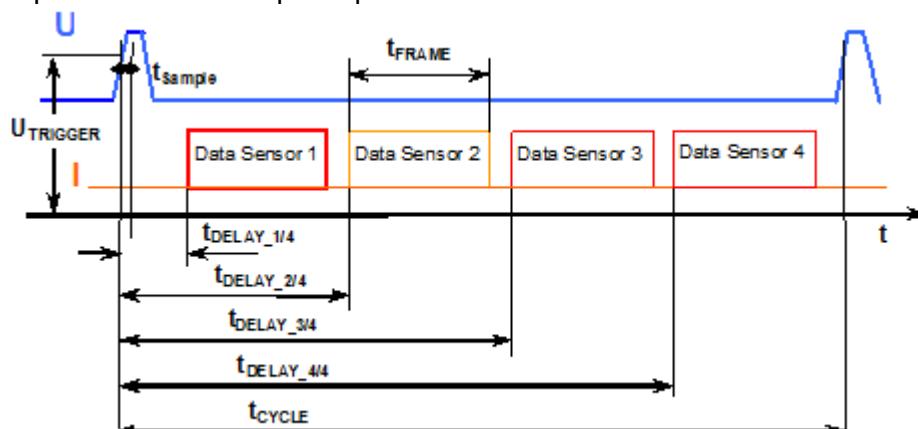
#### 6.4.3.10 P10CRC-500/4H

1219 In the PSI5-P10CRC-500/4H bus configuration a maximum number of four sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

1220 Setup of PSI5 parallel bus with 4 participants:



1224 Timing of PSI5 parallel bus with 4 participants:



1225 The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.  
4359 For this mode advanced transmission timing (ATT) must be activated to guarantee proper timing (already incl. in the following timings).

ID	parameter / condition	min	typ	max	unit
1226	Start of 1 <sup>st</sup> datagram $t_{\text{delay\_1/4}}$	45.7	49.8	52.3	$\mu\text{s}$
1227	End of 1 <sup>st</sup> datagram	123.4	129.8	133.9	$\mu\text{s}$
1228	Start of 2 <sup>nd</sup> datagram	145.1	150.3	154.0	$\mu\text{s}$



ID	parameter / condition	min	typ	max	unit
	$t_{\text{delay\_2/4}}$				
1229	End of 2 <sup>nd</sup> datagram	222.9	230.3	235.5	µs
1230	Start of 3 <sup>rd</sup> datagram $t_{\text{delay\_3/4}}$	255.4	261.9	266.9	µs
1231	End of 3 <sup>rd</sup> datagram	333.3	341.9	348.4	µs
1232	Start of 4 <sup>th</sup> datagram $t_{\text{delay\_4/4}}$	377.4	385.1	391.3	µs
1233	End of 4 <sup>th</sup> datagram	455.3	465.1	472.9	µs
1234	Bit time $t_{\text{Bit}}$		5.4		µs
1235	Datagram frame time $t_{\text{Frame}} = 15 \cdot t_{\text{Bit}}$		80		µs
1236	Gap time between time slots $t_{\text{Gap}}$	5.6			µs
1237	Cycle time (ECU) *) $t_{\text{Cycle}}$	495	500	505	µs

1238

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

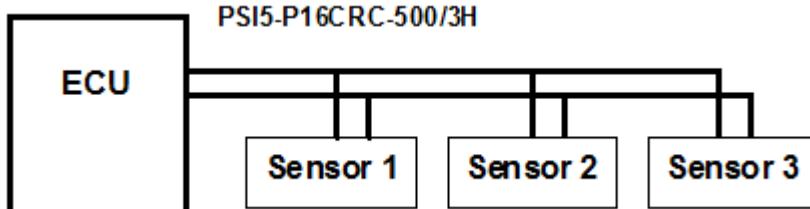
#### 6.4.3.11 P16CRC-500/3H

1240

In the PSI5-P16CRC-500/3H bus configuration a maximum number of three sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

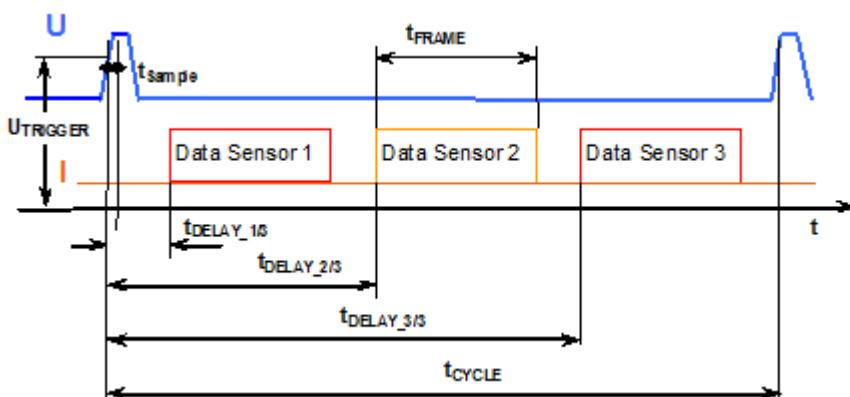
1241

Setup of PSI5 parallel bus with 3 participants:



1245

Timing of PSI5 parallel bus with 3 participants:



1246

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
1247	Start of 1 <sup>st</sup> datagram $t_{\text{delay\_1/3}}$ ; with ATT	44.8	48.9	51.4	μs
5537	Start of 1 <sup>st</sup> datagram $t_{\text{delay\_1/3}}$ ; no ATT; -4.2..+3% Oscillator	44.1	49.2	53.5	μs
1248	End of 1 <sup>st</sup> datagram with ATT	153.6	160.9	165.6	μs
5540	End of 1 <sup>st</sup> datagram no ATT; -4.2..+3% Oscillator	153.4	161.82	171.1	μs
1249	Start of 2 <sup>nd</sup> datagram $t_{\text{delay\_2/3}}$ ; with ATT	184.8	190.4	194.5	μs
5541	Start of 2 <sup>nd</sup> datagram $t_{\text{delay\_2/3}}$ ; no ATT; -4.2..+3% Oscillator	182.5	191.77	202.3	μs
1250	End of 2 <sup>nd</sup> datagram with ATT	293.7	302.4	308.5	μs
5542	End of 2 <sup>nd</sup> datagram no ATT; -4.2..+3% Oscillator	291.9	304.39	319.9	μs
1251	Start of 3 <sup>rd</sup> datagram $t_{\text{delay\_3/3}}$ ; with ATT	335.4	342.6	348.3	μs
5543	Start of 3 <sup>rd</sup> datagram $t_{\text{delay\_3/3}}$ ; no ATT; -4.2..+3% Oscillator	330.9	344.62	361.9	μs
1252	End of 3 <sup>rd</sup> datagram with ATT	444.1	454.6	462.5	μs
5544	End of 3 <sup>rd</sup> datagram no ATT; -4.2..+3% Oscillator	440.3	457.24	479.4	μs
1253	Bit time $t_{\text{bit}}$		5.4		μs
1254	Datagram frame time		112		μs



ID	parameter / condition	min	typ	max	unit
	$t_{Frame} = 21 \cdot t_{Bit}$				
1255	Gap time between time slots $t_{Gap}$	5.6			μs
1256	Cycle time (ECU) *) $t_{Cycle}$	495	500	505	μs

1257

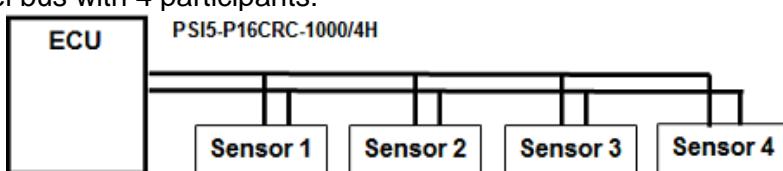
\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

#### 6.4.3.12 P16CRC-1000/4H and P16CRC-700/4H

5142

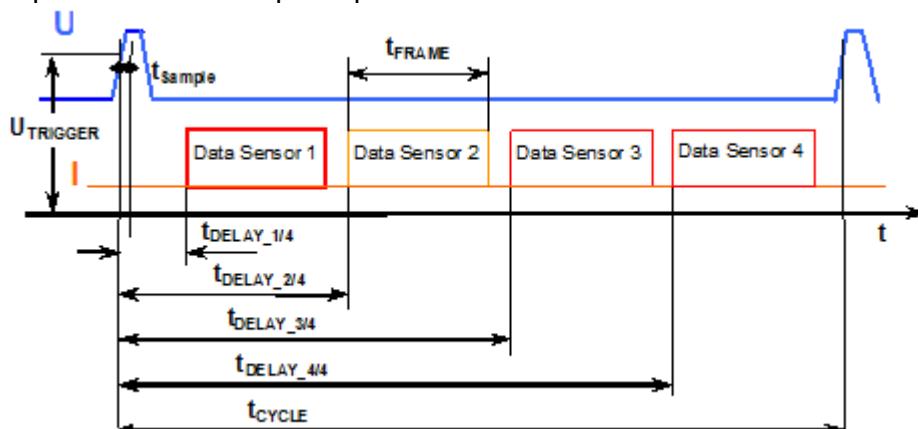
In the PSI5-P10CRC-1000/4H and P16CRC-700/4H bus configuration a maximum number of four sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus. Both modes are identical regarding the sensor timings. They only use a different cycle time for the ECU. Setup of PSI5 parallel bus with 4 participants:

5143



5144

Timing of PSI5 parallel bus with 4 participants:



5145

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
5147	Start of 1 <sup>st</sup> datagram $t_{delay\_1/4}$	44.1	50.1	54.4	μs
5148	End of 1 <sup>st</sup> datagram	151.4	162.7	172.0	μs
5149	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/4}$	181.6	194.4	205.1	μs
5150	End of 2 <sup>nd</sup> datagram	288.9	307.1	322.7	μs
5151	Start of 3 <sup>rd</sup> datagram $t_{delay\_3/4}$	331.8	352.2	369.8	μs



ID	parameter / condition	min	typ	max	unit
5152	End of 3 <sup>rd</sup> datagram	439.1	464.8	487.4	µs
5153	Start of 4 <sup>th</sup> datagram $t_{delay\_4/4}$	501.3	530.1	555.5	µs
5154	End of 4 <sup>th</sup> datagram	608.5	642.7	673.0	µs
5155	Bit time $t_{Bit}$		5.4		µs
5156	Datagram frame time $t_{Frame} = 21 \cdot t_{Bit}$		112.6		µs
5157	Gap time between time slots $t_{Gap}$	5.6			µs
5158	Cycle time (ECU) *) $t_{Cycle}$ P16CRC-1000/4H	990	1000	1010	µs
5160	Cycle time (ECU) *) $t_{Cycle}$ P16CRC-700/4H	693	700	707	µs

5159

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

5299

For 1000 µs- modes, it is not allowed to send sync pulses after power on within the bidir activation time, which is specified in ID 4364.

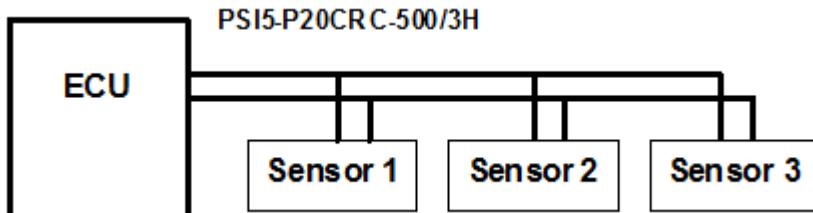
#### 6.4.3.13 P20CRC-500/3H

1259

In the PSI5-P20CRC-500/3H bus configuration a maximum number of three sensors are connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

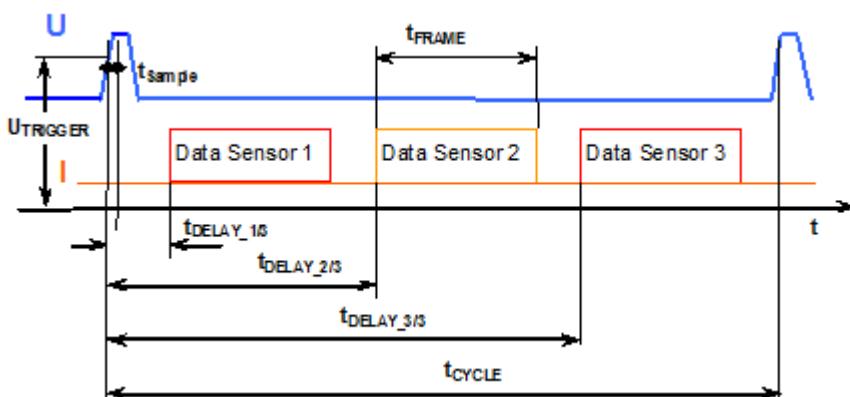
1260

Setup of PSI5 parallel bus with 3 participants:



1264

Timing of PSI5 parallel bus with 3 participants:

1265  
4361

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision. For this mode advanced transmission timing (ATT) must be activated to guarantee proper timing (already incl. in the following timings).

ID	parameter / condition	min	typ	max	unit
1266	Start of 1 <sup>st</sup> datagram $t_{\text{delay\_1/3}}$	44.4	48.1	50.9	μs
1267	End of 1 <sup>st</sup> datagram	174.3	181.4	186.0	μs
1268	Start of 2 <sup>nd</sup> datagram $t_{\text{delay\_2/3}}$	192.1	197.2	201.7	μs
1269	End of 2 <sup>nd</sup> datagram	322.1	330.5	336.4	μs
1270	Start of 3 <sup>rd</sup> datagram $t_{\text{delay\_3/3}}$	342.4	350.2	355.5	μs
1271	End of 3 <sup>rd</sup> datagram	472.2	483.5	491.3	μs
1272	Bit time $t_{\text{bit}}$		5.4		μs
1273	Datagram frame time $t_{\text{frame}} = 25 \cdot t_{\text{bit}}$		133.3		μs
1274	Gap time between time slots $t_{\text{gap}}$	5.6			μs
1275	Cycle time (ECU) $t_{\text{cycle}}$	495	500	505	μs

1276

\*) The "Cycle Time (ECU)" stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

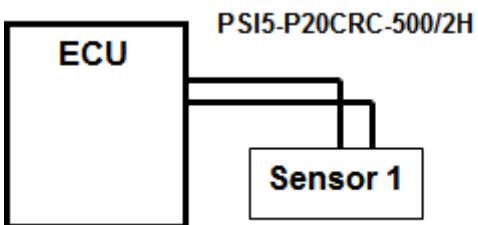
#### 6.4.3.14 P20CRC-500/2H

4735

In the PSI5-P20CRC-500/2H bus configuration a maximum number of one sensor is connected in parallel to the ECU. The ECU and the sensors are linked via the bus.

4736

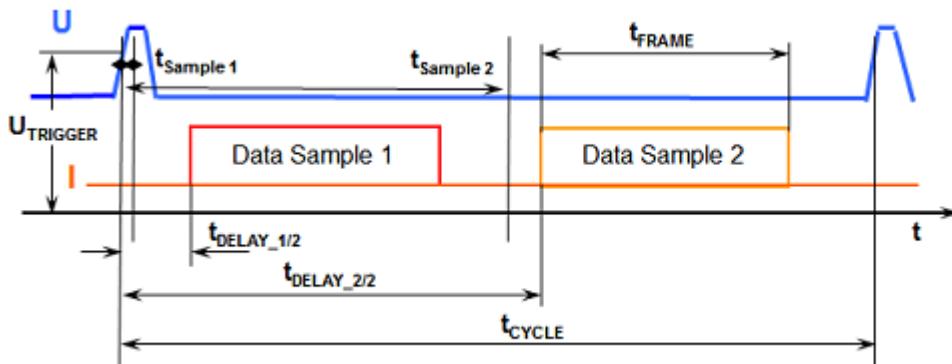
Setup of PSI5 parallel bus with 1 participant:



4738

This mode sends samples with 4kHz update rate (Mode #95 and #96). In the first timeslot the data from  $t_{sample1}$  is send. In the second timeslot the data from  $t_{sample2}$  is send.

Timing of PSI5 parallel bus in 4kHz sampling configuration:



4739

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
4741	Start of 1st datagram $t_{delay\_1/2}$	44.1	50.1	54.4	
4742	End of 1st datagram	171.8	184.2	194.4	
4743	Start of 2nd datagram $t_{delay\_2/2}$	256.5	273.1	287.2	
4744	End of 2nd datagram	384.2	407.2	427.2	
4745	Bit time $t_{Bit}$		5.4		µs
4746	Datagram frame time $t_{Frame} = 25 \cdot t_{Bit}$		133.3		µs
4747	Gap between time slots $t_{Gap}$	5.6			µs
4748	Cycle time ECU *) $t_{Cycle}$	495	500	505	µs

4749

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

#### 6.4.3.15 P20CRC-250/1H

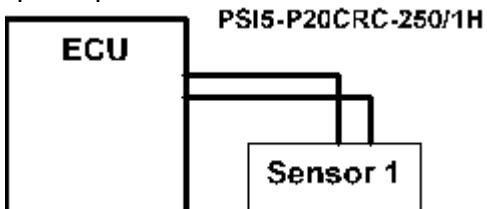
4765

In the PSI5-P20CRC-250/1H bus configuration a maximum number of one sensor is connected to the ECU. The ECU and the sensor are linked via the bus.



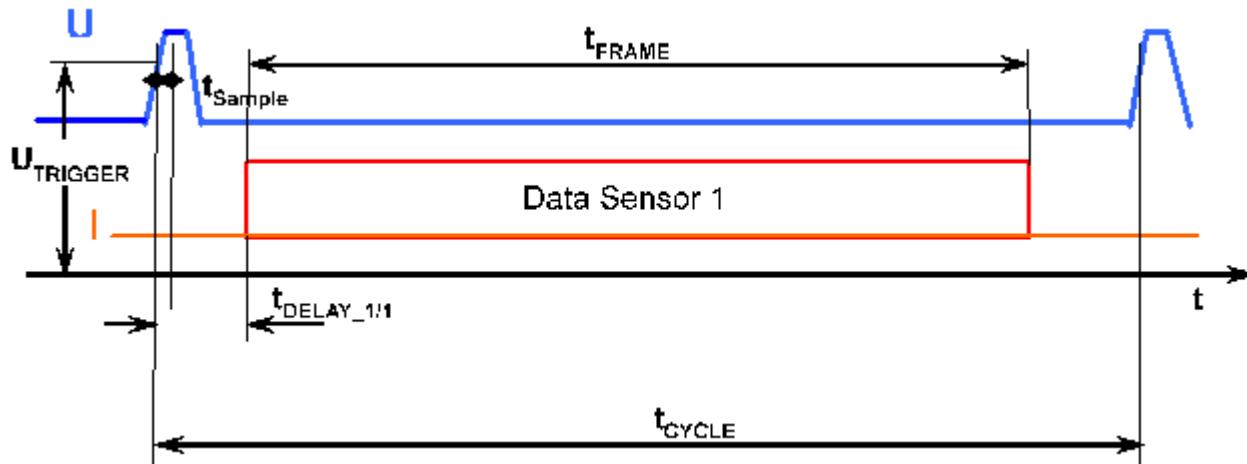
4766

Setup of PSI5 parallel bus with 1 participant:



4767

Timing of PSI5 parallel bus with 1 participant:



4768

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
4769	Start of 1st datagram $t_{\text{delay\_1/2}}$	44.1	50.1	54.4	$\mu\text{s}$
4770	End of 1st datagram	171.8	184.2	194.4	$\mu\text{s}$
4773	Bit time $t_{\text{Bit}}$		5.4		$\mu\text{s}$
4774	Dataframe time $t_{\text{Frame}} = 25 \cdot t_{\text{Bit}}$		133.3		$\mu\text{s}$
4776	Cycle time (ECU) * $t_{\text{Cycle}}$	247.5	250	252.5	$\mu\text{s}$

4777

\*) The "Cycle Time (ECU)" stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

#### 6.4.4 Daisy chain data transmission

1278

In PSI5 serial bus mode, sensors are connected in a "Daisy Chain" configuration to the ECU. By default, the sensor has no address and can be connected to each position on the bus.

1279

During start-up, each sensor receives an individual address and then passes the supply voltage to the following sensor subsequently.

1280

For SMA7 this is realized by an external switch which connects GND to the next sensor in the bus. The switches are controlled through SO pin of the previous sensor.

1282

The addressing is realized by bidirectional communication from the ECU to the sensor by using a specific sync signal pattern.

1283

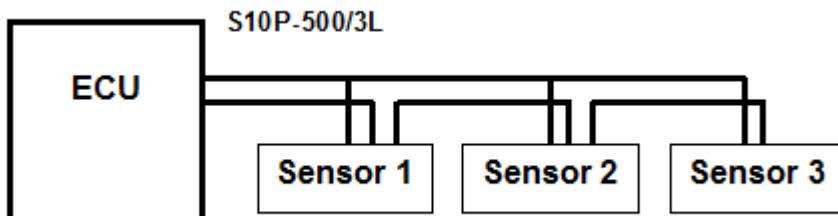


After having assigned the individual addresses, the sensors start to transmit data in their corresponding time slot in the same way as specified in the parallel bus topology. The addressing is described in section PSI5 bidirectional communication.

#### 6.4.4.1 S10P-500/3L

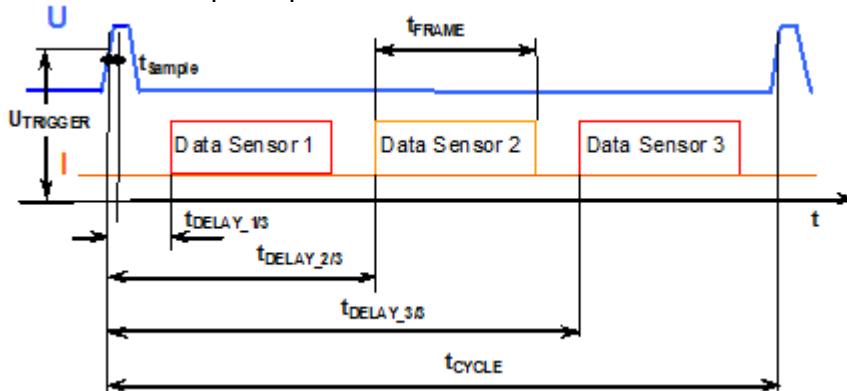
1281

Setup of PSI5 serial bus with 3 participants:



1285

Timing of PSI5 serial bus with 3 participants:



1286

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
1287	Start of 1 <sup>st</sup> datagram $t_{delay\_1/3}$	44.1	50.1	54.4	µs
1288	End of 1 <sup>st</sup> datagram	143.7	154.7	163.6	µs
1289	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/3}$	181.6	194.4	205.1	µs
1290	End of 2 <sup>nd</sup> datagram	281.2	299.0	314.3	µs
1291	Start of 3 <sup>rd</sup> datagram $t_{delay\_3/3}$	329.7	350.0	367.5	µs
1292	End of 3 <sup>rd</sup> datagram	429.3	454.6	476.6	µs
1293	Bit time $t_{Bit}$		8.1		µs
1294	Datagram frame time $t_{Frame} = 13 \cdot t_{Bit}$		104.6		µs
3108	Gap time between time slots $t_{Gap}$	8.4			µs
1295	Cycle time (ECU) <sup>1)</sup>	495	500	505	µs



ID	parameter / condition	min	typ	max	unit
	$t_{Cycle}$				

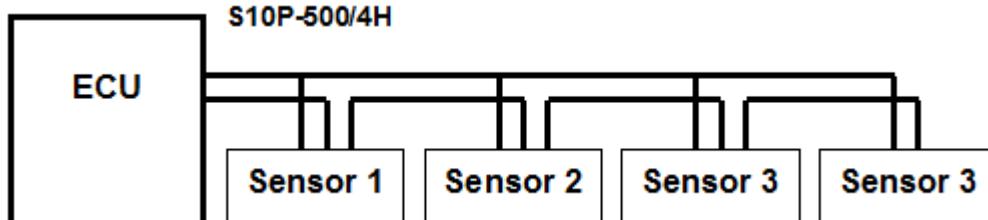
1296

) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

#### 6.4.4.2 S10P-500/4H

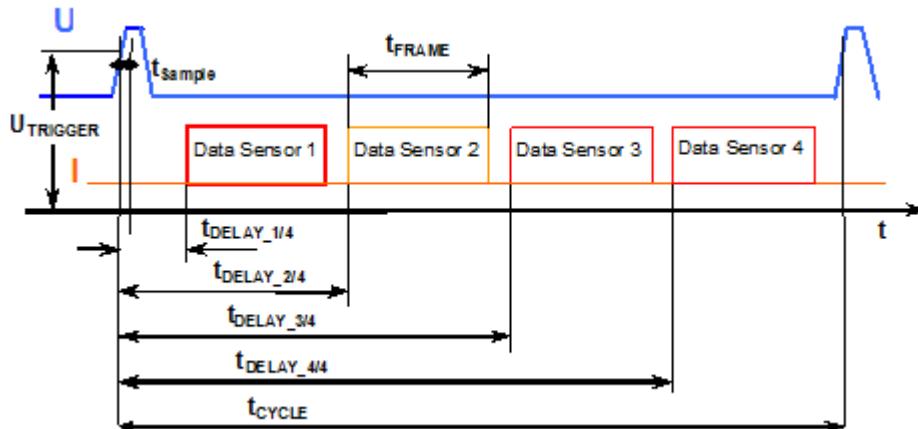
1301

Setup of PSI5 serial bus with 4 participants:



1305

Timing of PSI5 serial bus with 4 participants:



1306

The following timing has to be guaranteed by the ECU and sensors, in order to avoid datagram collision.

ID	parameter / condition	min	typ	max	unit
1307	Start of 1 <sup>st</sup> datagram $t_{delay\_1/4}$	44.1	50.1	54.4	µs
1308	End of 1 <sup>st</sup> datagram	110.5	119.8	127.2	µs
1309	Start of 2 <sup>nd</sup> datagram $t_{delay\_2/4}$	139.5	150.2	158.9	µs
1310	End of 2 <sup>nd</sup> datagram	205.9	219.9	231.7	µs
1311	Start of 3 <sup>rd</sup> datagram $t_{delay\_3/4}$	245.9	261.9	275.6	µs
1312	End of 3 <sup>rd</sup> datagram	312.3	331.7	348.3	µs
1313	Start of 4 <sup>th</sup> datagram $t_{delay\_4/4}$	363.3	385.3	404.3	µs
1314	End of 4 <sup>th</sup> datagram	429.7	455.0	477.1	µs
1315	Bit time		5.4		µs



ID	parameter / condition	min	typ	max	unit
	$t_{Bit}$				
1316	Datagram frame time $t_{Frame} = 13 \cdot t_{Bit}$		69.7		μs
3110	Gap time between time slots $t_{Gap}$	5.6			μs
1317	Cycle time (ECU) *) $t_{Cycle}$	495	500	505	μs

1318

\*) The “Cycle Time (ECU)” stated in the table above has to be guaranteed by the ECU in order to avoid datagram collision because of oscillator tolerances in the involved components. Cycle times mentioned below refer to the minimum repetition rates for non-overlapping transmission.

4464

The following calculations from PSI 5 spec v2.1 are used to define the PSI timings for all modes.

4450

For time slot = 1:

4451

Earliest Start of 1<sup>st</sup> datagram ( $t^1_{ES}$ ) = tSlot 1 Start +  $T_{Trig\ min}$

4452

Nominal Start of 1<sup>st</sup> datagram ( $t^1_{NS}$ ) >= tSlot 1 Start / (1 - (1 / CT))

4453

Programmed Nominal Start of 1<sup>st</sup> datagram ( $t^1_{NS,prog}$ ) =  $t^1_{NS}$  rounded to used quantization (e.g. 467ns for 2.25MHz step with +/-5% tolerance)

4454

Latest Start of 1<sup>st</sup> datagram ( $t^1_{LS}$ ) >=  $t^1_{NS,prog} * (1 + (1 / CT)) + T_{Trig\ max}$

4455

Earliest End of 1<sup>st</sup> datagram ( $t^1_{EE}$ ) >=  $t^1_{ES} + M^1 * T_{BIT} * (1 - (1 / CT))$

4456

Latest End of 1<sup>st</sup> datagram ( $t^1_{LE}$ ) >=  $t^1_{LS} + M^1 * T_{BIT} * (1 + (1 / CT))$

4457

For time slot 2...N:

4458

Earliest Start of N<sup>th</sup> datagram ( $t^N_{ES}$ ) >=  $t^{N-1}_{LE} + T_{GAP} + T_{Trig\ min}$

4459

Nominal Start of N<sup>th</sup> datagram ( $t^N_{NS}$ ) >= ( $t^{N-1}_{LE} + T_{GAP}$ ) / (1 - (1 / CT))

4460

Programmed Nominal Start of N<sup>th</sup> datagram ( $t^N_{NS,prog}$ ) =  $t^N_{NS}$  rounded to used quantization (e.g. 444ns for 2.25MHz step)

4461

Latest Start of N<sup>th</sup> datagram ( $t^N_{LS}$ ) >=  $t^N_{NS,prog} * (1 + (1 / CT)) + T_{Trig\ max}$

4462

Earliest End of N<sup>th</sup> datagram ( $t^N_{EE}$ ) >=  $t^N_{ES} + M^N * T_{BIT} * (1 - (1 / CT))$

4463

Latest End of N<sup>th</sup> datagram ( $t^N_{LE}$ ) >=  $t^N_{LS} + M^N * T_{BIT} * (1 + (1 / CT))$

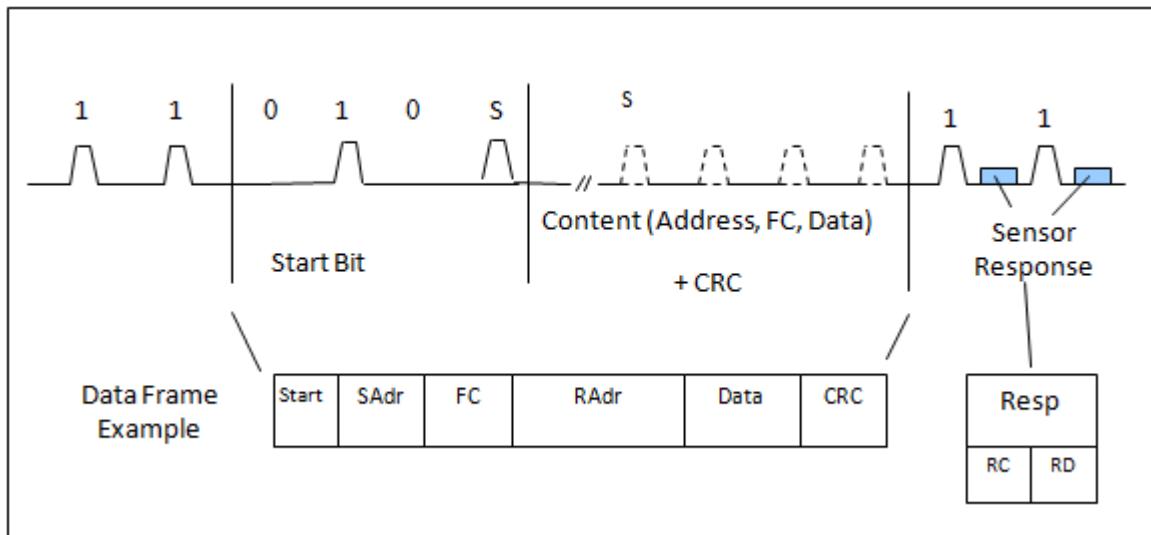


## 7. PSI5 BiDir Interface

SMA7 features as communication protocol for communication with the sensor the PSI5 bidirectional communication mode. This protocol can be used for the following purposes:

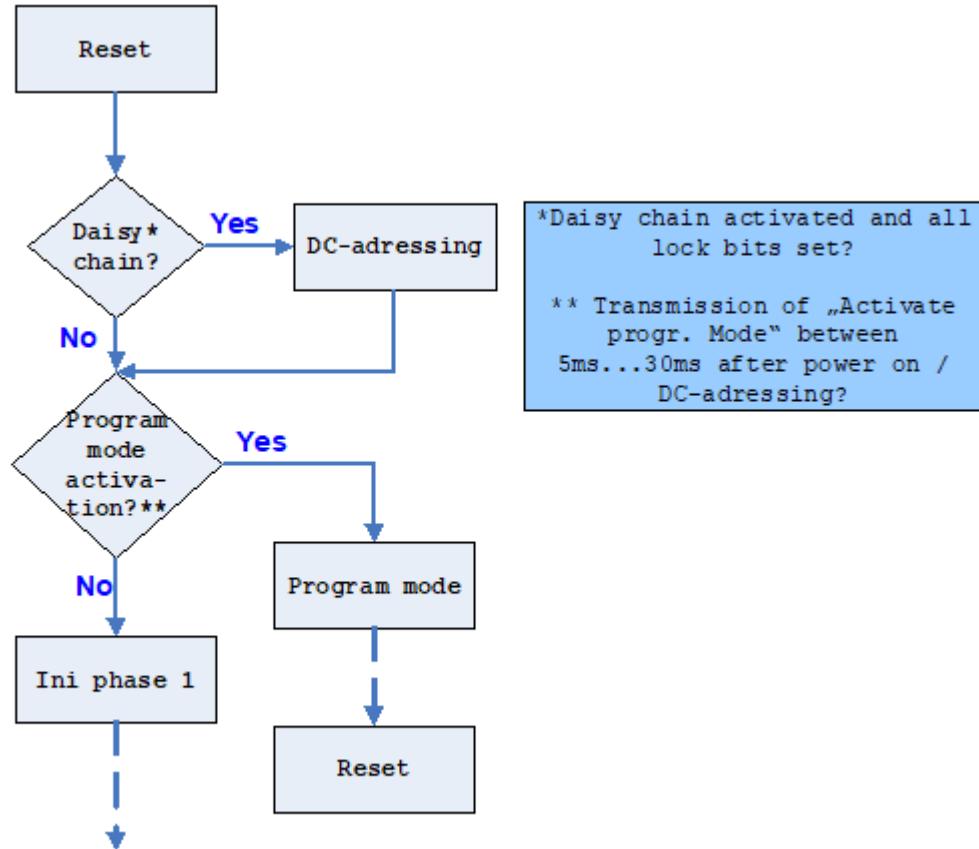
- PROM programming
- Daisy chain initialization

Principal bi-directional communication:



There are two operational modes for bidirectional communication: programming the OTP (service mode) and configuring sensor addresses for Daisy Chain operation. These two modes have to be accessed differently after a sensor reset.

Daisy chain addressing/BiDir activation (example flow):





1402 Slow BiDir-mode from SMA6 not supported anymore.

## 7.1 Hardware Layer

1404 During programming with the PSI5 bidirectional mode only one sensor is connected to the tester.

1405 Bidirectional communication is established in the following manner.

1406 Communication ECU to sensor:

1407 Instructions are sent to the sensor by making use of the synchronization pulses.

1408 A logical "1" is represented by the presence of a synchronization pulse during the appropriate time interval, and a logical "0" by the absence of a synchronization pulse. This is called "tooth gap" method.

1409 Communication sensor to ECU:

1410 The sensor responds during bidirectional communication in service mode with the standard PSI5 P10P-500/4H mode in timeslot 1.

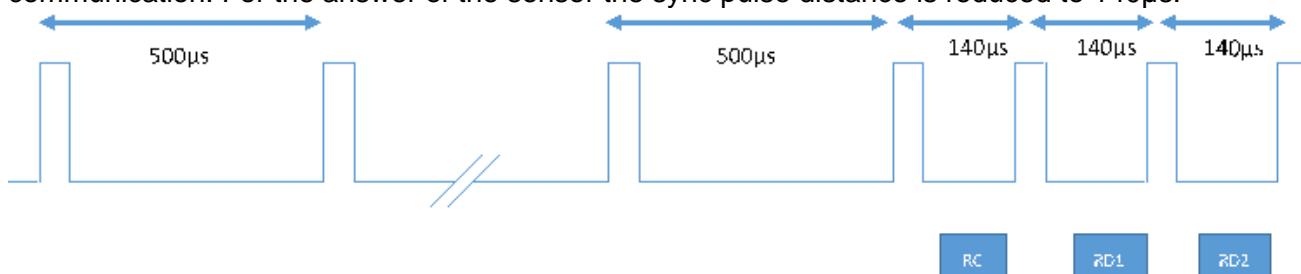
In daisy chain mode it responds with the selected daisy chain transmission mode (S10P-500/3L or S10P-500/4H) in timeslot 1.

### 7.1.1 PSI5 BiDir Timing

#### Service mode:

First command to activate service mode:

To activate the service mode the master sends sync pulses with 500µs distance for master to sensor communication. For the answer of the sensor the sync pulse distance is reduced to 140µs.

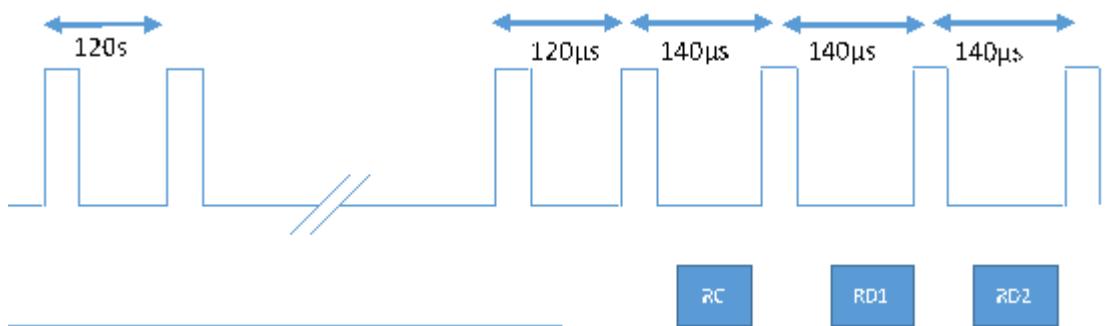


4364 The complete frame to activate service mode must be send within 5ms - 30ms after power on.

ID	parameter / condition	min	typ	max	unit
1417	Syncpulse distance Master to sensor communication all sync pulses before RC-sync	495	500	505	µs
1418	RC-Sync Timing relative to previous sync pulse; current modulation is 189kbps	495	500	505	µs
1419	RD1-Sync Timing relative to previous sync pulse; current modulation is 189kbps	138.6	140	141.4	µs
1420	RD2-Sync Timing relative to previous sync pulse; current modulation is 189kbps	138.6	140	141.4	µs

1421 All further commands during service mode:

4365 For master to sensor communication during service mode a syncpulse distance of 120µs is used. For the answer of the sensor the sync pulse distance is increased to 140µs.

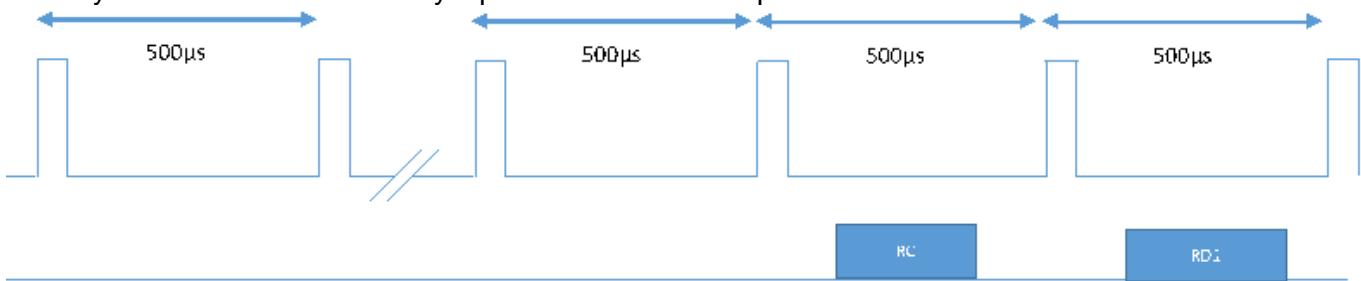


ID	parameter / condition	min	typ	max	unit
1426	Syncpulse distance Master to sensor communication all sync pulses before RC-sync	118.8	120	121.2	µs
1427	RC-Sync Timing relative to previous sync pulse; current modulation is 189kbps	118.8	120	121.2	µs
1428	RD1-Sync Timing relative to previous sync pulse; current modulation is 189kbps	138.6	140	141.4	µs
1429	RD2-Sync Timing relative to previous sync pulse; current modulation is 189kbps	138.6	140	141.4	µs

1430  
4366

During daisy chain initialization:

In daisy chain mode a constant syncpulse distance of 500µs is used for the bidirectional communication.



ID	parameter / condition	min	typ	max	unit
1435	Syncpulse distance all syncpulses	495	500	505	µs

## 7.2 Data Link Layer

1439

The sensor will only start decoding a new instruction after it has sent all response datagrams of the previous instruction.

### 7.2.1 Frame

1441

Short frame (used for daisy chain initialization):

Start	SAddr	FC	CRC	Resp
0   1   0   S   A0   A1   A2   S   F0   F1   F2   S   C2   C1   C0	RC   RD1			



1442

X-Long frame (used for programming mode):

Start	SAdr	FC	RAdr	Data	CRC	Resp			
0	1	0	S	A0 A1 A2 S	F0 F1 F2 S	X0-X7 + Sync Bits	D0-D7 + Sync Bits	C2 C1 S C0	RC RD1 RD2

4369

Please notice, that SAdr, FC, RAdr and Data is transmitted with least significant bit first, to be aligned with standard PSI5 specifications.

ID	parameter / condition	min	typ	max	unit
1443	Short frame length incl. stuffing bits/RD/RC		17		
1444	X-Long frame length incl. stuffing bits/RD/RC		40		
1445	Short frame duration 2kHz transmission rate	8.08	8.5	8.93	ms
1446	X-Long frame duration 8.3kHz transmission rate	4.6	4.84	5.08	ms

1447

Frame overview (allowed values for BiDir frames):

Bidirectional Communication: Function Codes					
Instruction	Sadr (A2-A0)	FC (F2-F0)	Signification	Response	
				O.K.	Error
Short data frames					
SetAddr	000	001-110	Set sensor address in daisy chain mode and close bus switch (by FC)	RC = "OK" RD = Address	RC = "Error"
Run	111	000	Sensors to enter "run" mode (Broadcast)	RC = "OK" RD = "0000"	RD = "Error Code"
XLong data frames					
Read	001	000	Read from sensor register address	RC = "OK" RD1 = Data RD2 = Data	RC = "Error"
Write		001	Write to sensor register address	RC = "OK" RD1 = "0000"	RD1 = "Error Code"
Multi-Write		101	Write complete customer OTP area with a single command	RD2 = "0000"	RD2 = "0000"

The detailed description of the mentioned function codes can be found in the chapter "operation modes" below.

## 7.2.2 Start Sequence

1449



In order to ensure a reliable start of bidirectional communication, the receiver shall send at least three consecutive sync pulses as "111". Afterwards each instruction sent to the sensor is starting with the sequence "010" and instruction decoding starts with the first "0" bit.

1450 If the system controller continues sending "111", instead of sending "010", the sensor will just treat the "111" as new synchronization between receiver and sensor.

1451 Any error in the start bits "010" will not trigger an error message but will end the decoding of the present frame. Hence, without a detection of "010" after the "111" the sensor keeps waiting for the next command. It will stay in this state until a correct command is received or until a power down.

### 7.2.3 Stuffing Bits

1453 As a consecutive train of "zeros" may lead to a loss of synchronization between ECU and sensor, "bit stuffing" is required to ensure proper synchronization. In the communication with SMA7, one stuffing bit "S" with value "1" has to be inserted after sending 3 bits of information.

1454 If service mode or daisy chain mode is activated, any missing stuffing bit will end the decoding immediately and a framing error will be sent.

### 7.2.4 SAdr (Sensor Address)

1456 Sensor address is used to address the sensor during the bidirectional communication.

### 7.2.5 Function Codes

1458 Function codes are used to define the bidirectional commands (e.g. as daisy chain addressing or read/write command in programming mode).

### 7.2.6 RAdr (Register Address)

1460 Register address block is used to define the register that will be read or written during a programming mode command. This block is only available for X-long frame.

### 7.2.7 Data

1462 Data block is used to define the information that will be written to the addressed register during a programming mode command. This block is only available for X-long frame.

### 7.2.8 CRC

1464 The CRC calculation is specified by:

- 1465   • Polynomial =  $1 + x + x^3$   
1466   • Initial value = 0b111  
1467   • Target value = 0b000  
1468   • The start bits and the stuffing bits are ignored for computing the CRC bits

### 7.2.9 Return Code/Data

1470 The sensor responds with current modulated Manchester code, which has 2 start bits, 10 Data bits and 1 bit for parity check.

1471 In the case of a "Short frame", two datagrams are sent from sensor in at least 2 sync-cycles: a return code RC and return data RD.

1472 In the case of a "XLong frame", three datagrams are sent in at least 3 sync-cycles: a return code RC and two return data RD.

1473 Return codes RC:



Bidirectional Communication: Return Code	
Dataword (10 bit)	Return Code RC
+482	"Error" (Failure during communication; see "Error Handling")
+481	"OK" (Command accepted)

1474

Return data values:

Dataword (10 bit)	Data value	Comment
-496	0000	Also default value for write accesses
-495	0001	
...	...	
-482	1110	
-481	1111	

### 7.2.10 Error handling

1476

Error codes:

Dataword (10 bit)	Error Code	Mnemonic	Mode	Comment
-495	0001	Framing	Prog & Daisy Chain	Framing error, e.g. missing stuffing bit or sync error *)
-494	0010	CRC	Prog & Daisy Chain	CRC error
-493	0011	Sensor Address	Daisy Chain	Wrong Sensor address
-492	0100	FC	Prog & Daisy Chain	Wrong function code
-491	0101	Memory address	Prog	Memory address not existing or config register write protected
-490	0110	Write Protect	Prog	MOTP address write protected by active lockbit

\*) Upon having detected a framing error, the Framing Error message will be sent as soon as the next sync pulse has been recognized, without waiting for the end of the instruction. If a framing error occurs before the XLong or Short frame format is detected, a short frame error message with two datagrams will be sent.

### 7.3 Service mode

4370

The service mode can be used to program the OTP of PSI types. Also in this mode read/write access to configuration registers is available.

4371

After activation of the PSI service mode, the "Extended mode" is automatically activated.

5102

After entering PSI service mode the Extended Mode as well as the Extended Testmode cannot be left, except by performing a soft-reset or power-on reset. If service mode is left by sending "Enter run mode"



command the extend mode/ extended test mode stays activated. This especially means, that no CRC check is done. To avoid this a power-on reset is recommended.

### 7.3.1 Instruction Set

4368

#### Sensor address:

For communication in service mode always Sensor address = "001" should be used. Using of all other addresses except "000" and "111" will not lead to an error, but is not released for customer use.

1482

The instruction set includes the following commands:

#### 7.3.1.1 Activate service mode

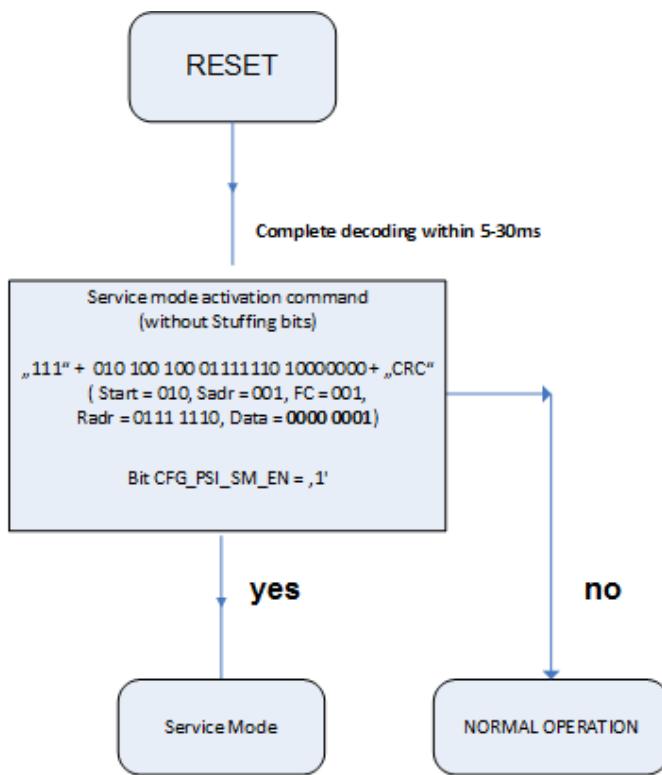
4373

For the activation command the special sync pulse timing, which are described in the timing chapter, must be used.

1483

FC (F2-F0)	0b001
Radr	0x7E
Data	0x1

4372



#### 7.3.1.2 Read single register

1484

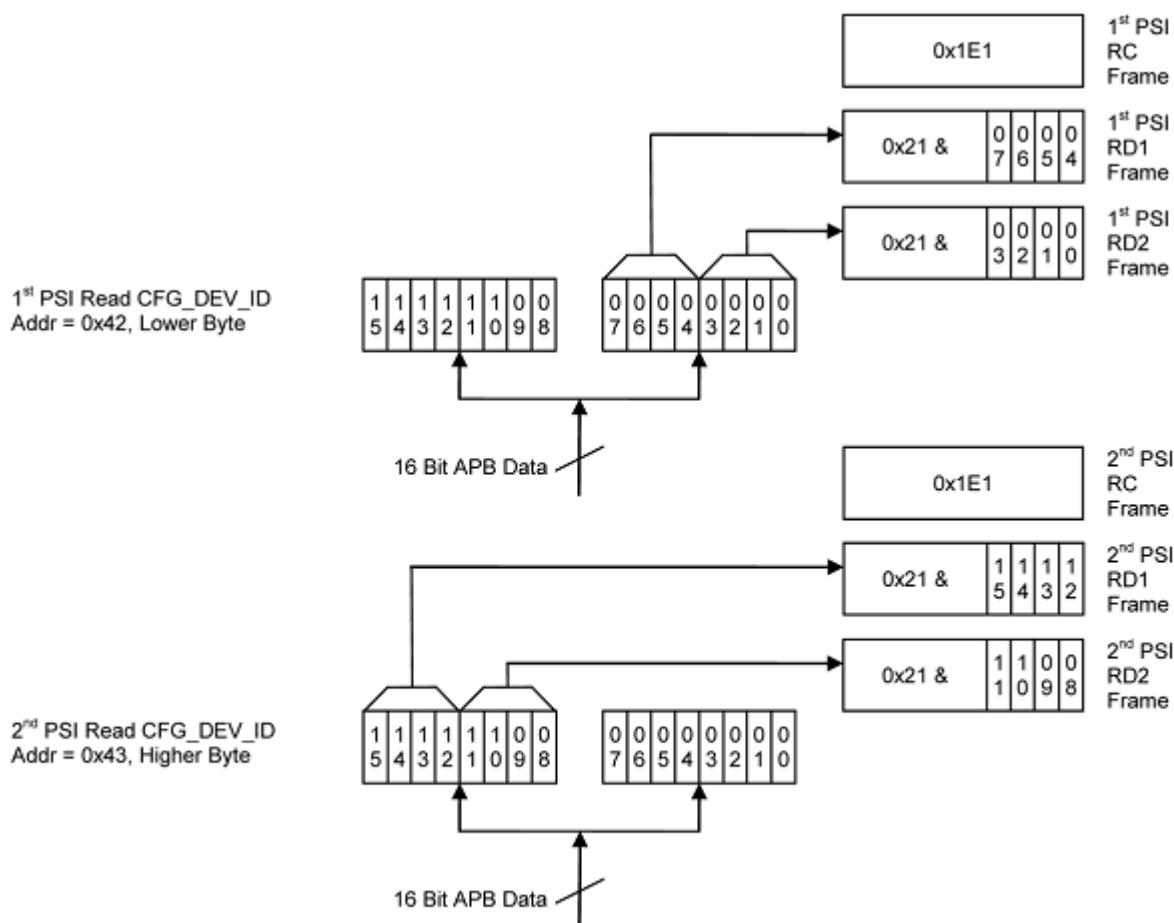
FC (F2-F0)	0b000
Radr	8bit register adress
Data	0x00

4375

With this command 8 bits of a register can be read. Using the even address values from the registermap will return the lower 8 bits of a register. Using the corresponding odd address, will return the upper 8 bits. The 8 bits are split to 4 + 4 bit between RD1 and RD2.

4376

Example of 4+4 bit PSI transfer:



4377

CA-Si behaviour: Functionality described below does not behave as specified: The freezing mechanism for registers **CFG\_MON\_DATA1** does not work irrespective of the access sequence.

**CFG\_MON\_DATA1** is frozen following a read access to register **CFG\_MON\_DATA1**. PSI BiDir must not be used to read **CFG\_mon\_data1/2**.

Target behaviour:

In case of reading data from the register **CFG\_MON\_DATAx**, a certain sequence of accesses is needed: Bit 07 down to 00 of **CFG\_MON\_DATA1** at address 0x5C shall be the target of the first access. Bit 15 down to 08 of **CFG\_MON\_DATA1** at address 0x5D shall be the target of the second access. Bit 07 down to 00 of **CFG\_MON\_DATA2** at address 0x5E shall be the target of the third access. If this order of accesses is taken care of then all three data Byte belong to the same sample. When the first of these Registers is accessed the contents of the other Register is frozen until the second Register is read.

4037

The above described reading scheme is valid for all registers, except:

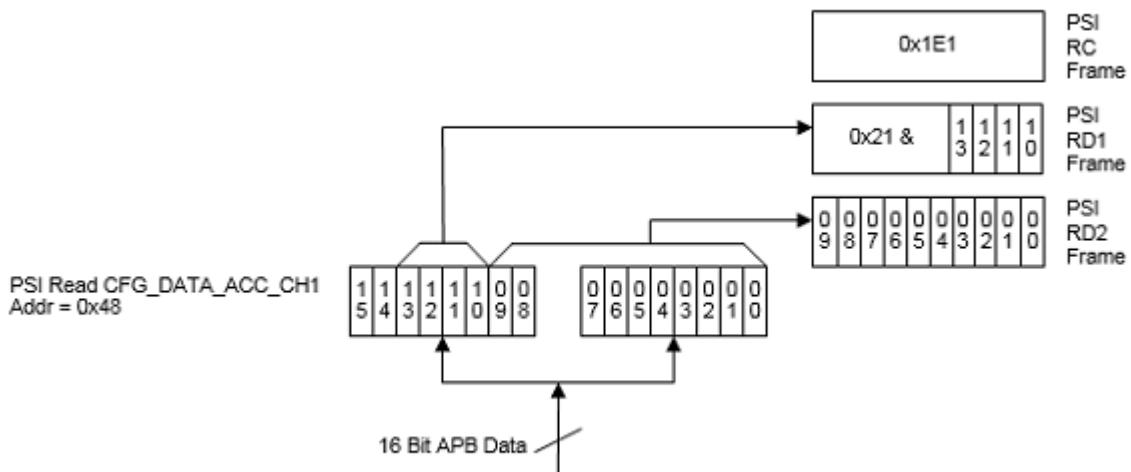
**CFG\_DATA\_ACC\_CH1** (0x48),

**CFG\_DATA\_ACC\_CH2** (0x4A),

**CFG\_DATA\_ACC\_CH2\_CAPT** (0x4C)

To allow reading the 14bit acceleration data in this register with one command, the data is split to 4 + 10 bit between the RD1 and RD2 response.

Example of 4 + 10 bit PSI data transfer:



### 7.3.1.3 Write single register

FC (F2-F0)	0b001
Radr	8bit register adress
Data	8bit data

With this command 8 bits of a register can be written. Using the even address values from the registermap will write the lower 8 bit of a register. Using the corresponding odd address, will write the upper 8 bit.

### 7.3.1.4 Multi register read

FC (F2-F0)	0b001
Radr	0x7E
Data	0x21

With this command the complete OTP can be read by only sending one BiDir command. After receiving this command the ASIC sends the content of the complete OTP as response. The response starts with the RC frame and the memory size is send in the first two RD frames. The sensor transmits first the content of register 0x00 to 0x3A (OTP Nibble 0 to OTP Nibble 119), then 16bits of zero (OTP Nibble 120 to OTP Nibble 123), and then content of register 0x3E (OTP Nibble 124 to OTP Nibble 127).

Comment: The 16bits of zero are send, because MOTP address 3C is not existing.

Sensor response for multi read instructions:

RC 10 bit (w/o header)	RD1_0 (6 bit header)	RD1_1 (6 bit header)	RD1_2 (6 bit header)	RD1_n+2 (6 bit header)	.....	RD1_129 (6 bit header)	RD2 (6 bit header)
"OK"	OTP length high nibble	OTP length low nibble	OTP nibble 0	OTP nibble n	.....	OTP nibble 127	"0000"

### 7.3.1.5 Multi register write (customer area)



FC (F2-F0)	0b101
Radr	0x2C
Data	128 bit data for complete customer area of MOTP (0x2C-0x3A), except lockbit

3685

With these command the shadow register of the complete customer area (PAS) can be changed by sending only one single command. When sending the corresponding command (Multiwrite PAS) the master sends a data field with a length of 128 bit, which is identical to the size of corresponding OTP area.

#### 7.3.1.6 Enter 8.8kHz mode

3686

For channel 1:

FC (F2-F0)	0b001
Radr	0x7E
Data	0x03

4387

For channel 2:

FC (F2-F0)	0b001
Radr	0x7E
Data	0x05

#### 7.3.1.7 Enter run mode

3723

FC (F2-F0)	0b110
Radr	don't care
Data	don't care

#### 7.3.1.8 Read extended Device ID

3138

FC (F2-F0)	0b000
Radr	0x43
Data	0x00

With this instruction the extend device ID is read. It is equal to the last two digits of the SMA type in hex-values and can therefore be used to identify the sensor type.

E.g.: SMA785 --> ext. dev. ID= 0x85

#### 7.3.1.9 Further BiDir commands:

3139

- Self test activation and read out.

3722

Triggering the selftest of both channels is possible with a single command.

3724

- Command to change offset cancellation mode and select number of samples for fast offset cancellation. This is possible by a single 6bit command (per channel). Hint: The value of MOTP\_OFS\_FOC/SOC\_DISABLE must not be changed. Otherwise FOC execution of FOC via BiDir may not work.

3684



- Margin test commands to perform a margin test as described in the PROM chapter (e.g. set margin level, perform test). Setting the margin level and triggering the margin test can be done with a single command.

### 7.3.2 OTP programming

OTP programming and margin test can be done with PSI BiDir communication as described in the OTP chapter.

A sample programming flow for the customer area of PSI types could be done as described below:

- enter BiDir mode
- optional: Check MOTP content with multi-read command
- write customer area of MOTP, using Multi write command
- write lockbit of customer area in register 0x3E with single register write
- start programming of OTP via bootloader as described in OTP chapter by using single register write
- optional: Check MOTP content with multi-read command
- perform margin read test as described in OTP chapter by using single register write

### 7.3.3 8.8 kHz asynchronous Mode

From BiDir service mode the activation of 8.8kHz ( $t=114\mu s$ ) asynchronous transmission mode is possible . By using this transmission mode a higher sampling frequency at the applied signal can be reached.

In this mode 10bit are send every  $114.7\mu s$  with a rate of 125kbps.

When entering the 8.8 kHz mode, the sensor keeps the current setup of the MOTP and config registers. This means that it can be configured by service mode before entering.

If MOTP\_OFS\_MSOC\_DISABLE=0, MSOC is started when entering 8.8 kHz Mode. It is not stopped by leaving 8.8 kHz mode, hence it runs as long as defined by MOTP\_MSOC\_DURATION.

If MOTP\_OFS\_MSOC\_DISABLE=1 is set prior to enabling 8.8kHz mode, MSOC is not executed.

By sending a sync-pulse from the master this mode will be terminated and switched back to the service mode.

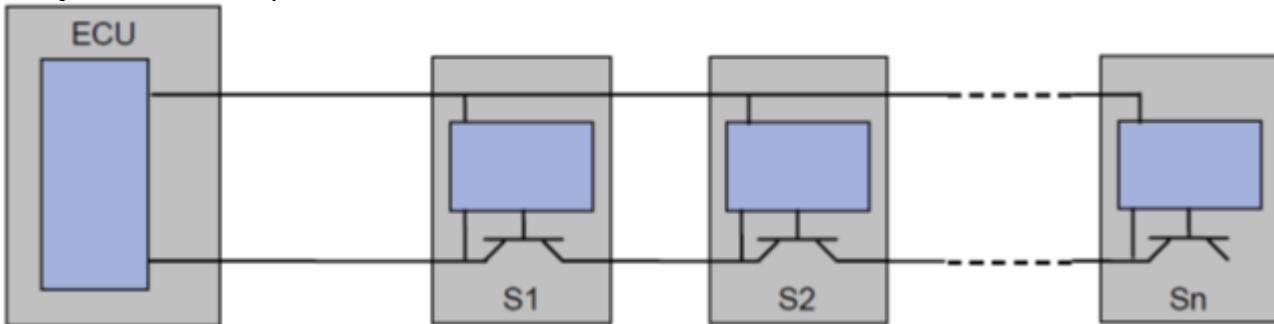
Note: When leaving the service mode, after 8.8kHz mode was activated, the init phases are not executed correctly.

### 7.4 Daisy Chain mode

In PSI5 serial bus mode, sensors are connected in a "Daisy Chain" configuration to the ECU. By default, the sensor has no address and can be connected to each position on the bus. During startup, each sensor receives an individual address and then passes the supply voltage to the following sensor subsequently.

In SMA7 it is realized through external switches which connect the GND of the sensors in serial bus mode. The switches are controlled by the daisy chain driver pin of the previous sensor.

Daisy chain bus setup:





The addressing is realized by bidirectional communication from the ECU to the sensor using a specific sync signal pattern. After having assigned the individual addresses, the sensors start to respond in their corresponding time slot in the same way as specified for the parallel bus topology.

1500 To initialize the daisy chain mode all lockbits have to be set.

1501 After having assigned an address to a sensor the external switch is switched on.

1502 If the addressing was successful, the sensors go to Parallel Bus mode upon receiving a "Run" command.

1503 However, if the addressing was not successful, the sensors can only leave this status with an external reset.

1504 During the addressing phase the error codes are sent in the time slot 1.

#### 7.4.1 Instruction Set

1506 Daisy chain initialization instructions:

Sadr	FC (F0,F1,F2)	Signification
000	000	Address of an unprogrammed sensor
000	100	slot #1
000	010	slot #2
000	110	slot #3
000	001	slot #4 (only P10P500/4H-mode)
000	101	reserved
000	011	reserved
000	111	Broadcast address to all sensors

#### 7.4.2 Initialization Flow

1508 Sensor addresses can be assigned by using the SetAdr instruction.

1509 After setting a valid sensor address the selected time slot will be used to respond as well as the external daisy chain transistor is switched on by the daisy chain driver pin signal.

1510 Daisy chain driver pin is (high) activated at the Trig time by the first Sync Pulse after sensor response.

1511 During the addressing phase the error codes are sent in the time slot 1. So the collision of an Error-Code and the unintentional respond of another sensor (e.g. via EMC influence) is avoided.

1512 In each configuration it has to be noticed that only one channel per sensor can be selected. The daisy-chain configuration is therefore only available for single axis sensors.

1513 Sensors have to be programmed in the inverse order. This has to be done to omit collisions in the first timeslot because the first time slot is the default answer slot of unprogrammed daisy chain sensors.

1514 3-Sensor bus:

- First programming process: sensor 1 -> slot #3
- Second programming process: sensor 2 -> slot #2
- Third programming process: sensor 3 -> slot #1

1515 4-Sensor bus:

- First programming process: sensor 1 -> slot #4
- Second programming process: sensor 2 -> slot #3
- Third programming process: sensor 3 -> slot #2
- Fourth programming process: sensor 4 -> slot #1

1516 If the sensor already has a valid address, it will just ignore the SetAdr command and send no response back.

1517 Additionally the run command will not take effect until a valid daisy chain address has been set.



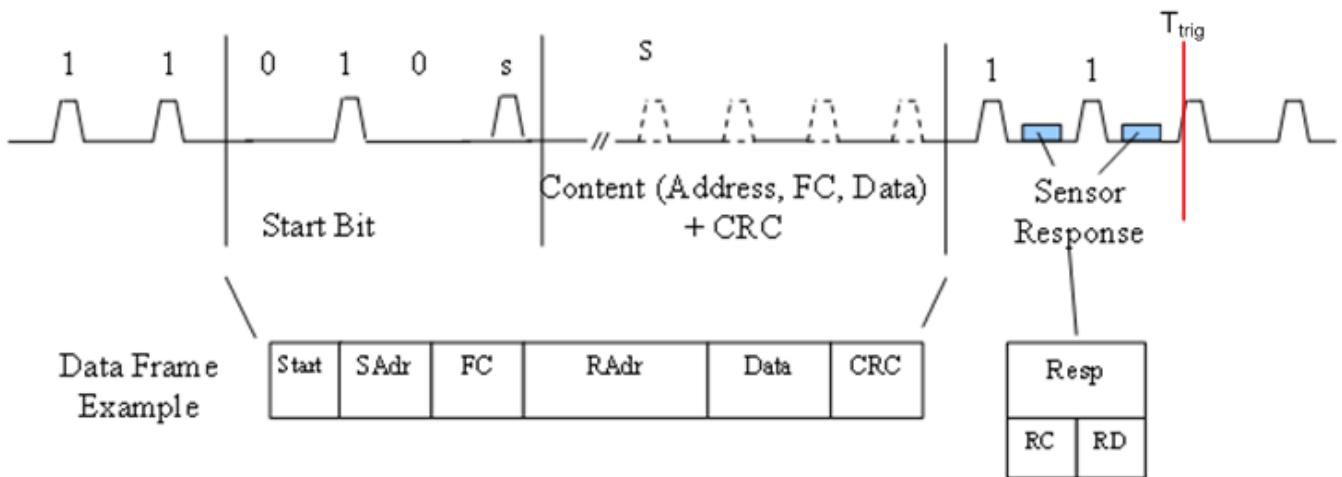
The restart of the sensor (normal startup with Init phase 1-3) is performed after the final bit of the last datagram of the response has been sent by the sensor. If no valid address is set and run command is send, the sensor will respond with "Sensor Address not supported" error message.

### 7.4.3 Daisy Chain Switch

After having programmed a daisy chain communication mode, the daisy chain driver pin (SO-pin) of SMA7 will function as switch for an external daisy chain transistor.

After address assignment, daisy chain will be activated (high) at the trigger time,  $T_{trig}$  of the first detected sync pulse after sensor response.

Daisy chain driver timing:



ID	parameter / condition	min	typ	max	unit
3146	Daisy Chain Driver Voltage Daisy chain driver inactive	0		0.2*Vddi	V
3147	Daisy Chain Driver Voltage Daisy chain driver active	0.8*Vddi		Vddi	V



## 8. Application

### 8.1 Packaging

The mold compound flammable rating for all packages is equal or above the standard UL-STD94-V-0 requirement or IEC 60695-11-10

In accordance with ROHS and the EU End of Life Vehicle Ordinance, there is no lead (Pb) in the sensor MSL classification refers to IPC/J-STD-020.

Wire bond material is gold.

ID	parameter / condition	min	typ	max	unit
2909	Bond wire thickness	19	20	21	µm

### 8.2 SOIC8 Package

#### 8.2.1 Mechanical properties

The SOIC8 is conform to JEDEC MS-012F for SOICn packages.

The housing SO8 is released for a soldering stencils thickness of 120µm and 150µm.

- Possibility of visual inspection of solder joints
- Suitable for conformal coating
- No delamination according the criteria in the referred documents from Hyundai.
- No dedicated manufacturing processes at Tier 1
- No change of PCB technology required (compared to SMA6)

It is qualified for MSL1, according to IPC/J\_STD\_020 and IPC/J\_STD\_033.

The SOIC8 uses an inverted leadframe.

Leadframe/substrate material: Cu

Intermediate layer material of terminal plating of Leadframe: preplated LF; Ni(bottom layer)/Pd(middle layer)/Au-Ag(top layer)

Lead finish material of terminal plating of Leadframe: Ni/Pd/Au-Ag preplated finish

Die attach method: film die attach

Die attach material (adhesive for ASIC and MEMS): Hitachi FH9011(25um)

Wire bond method: Thermal ultrasonic bonding

The sensing element (g-cell) is placed next to pin1 to guarantee a direct coupling in case pin1 is used as reference pin for sensor mounting in PCB layout.

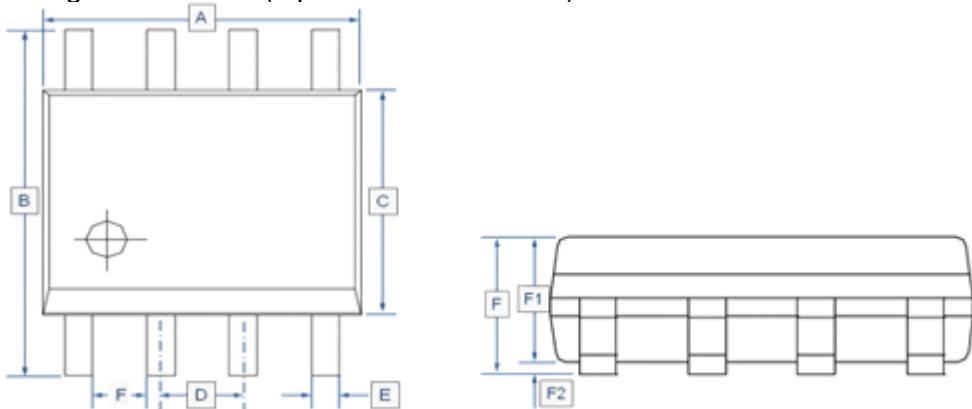
ID	parameter / condition	min	typ	max	unit
5198	Thermal resistance (Rth) between internal heat source (ASIC) and ambient. End of leadfingers fixed at ambient temperature.		100		K/W
2917	Package Resonance First resonance frequency; SO8; X-direction	28	37	50	kHz
2918	Package Resonance First resonance frequency; SO8; Y-direction	31	43	48	kHz



ID	parameter / condition	min	typ	max	unit
2919	Package Resonance First resonance frequency; SO8; Z-direction	30	45	69	kHz
2920	Package Resonance Q-factor of first resonance frequency; SO8; X-direction		75		
2921	Package Resonance Q-factor of first resonance frequency; SO8; Y-direction		110		
2922	Package Resonance Q-factor of first resonance frequency; SO8; Z-direction		75		

4473

Package dimensions (top view and side view):

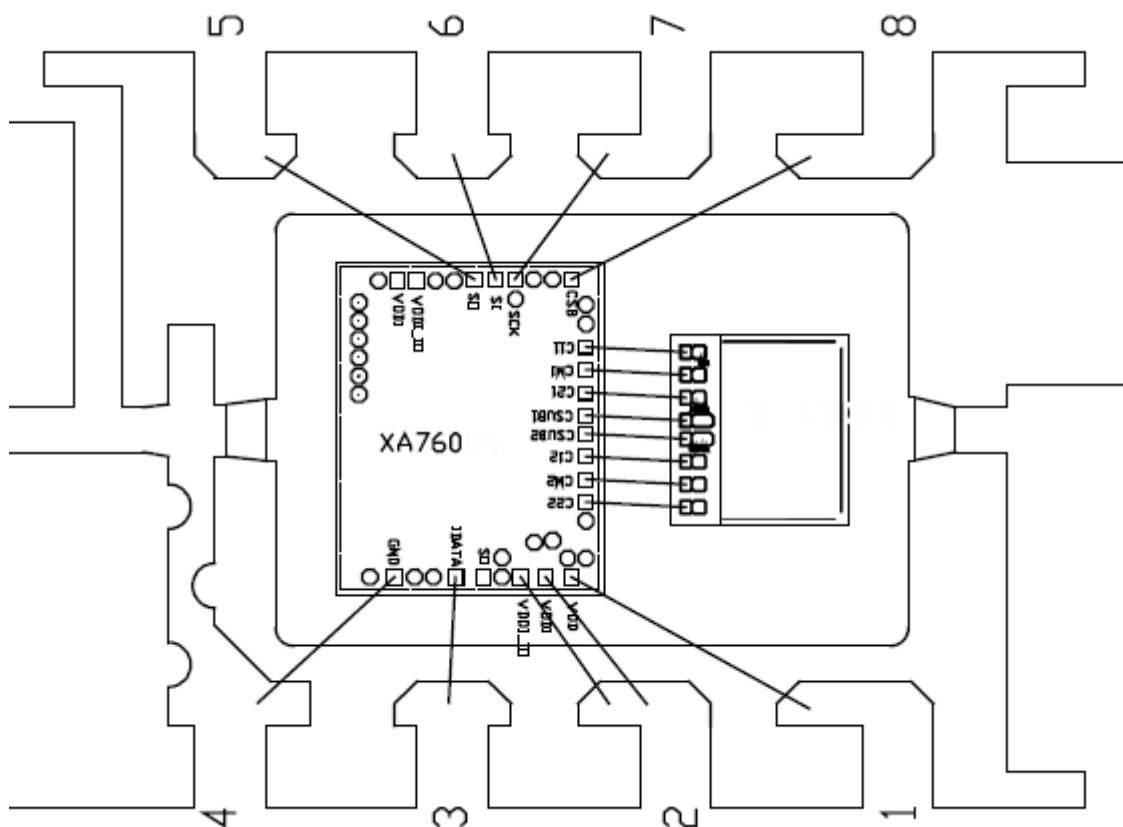


ID	parameter / condition	min	typ	max	unit
4474	Footprint in X-direction A		4.9		mm
4475	Footprint in Y-direction B		6		mm
4476	Dimension in Y-direction C		3.9		mm
4477	Leadfinger pitch D		1.27		mm
4478	Leadfinger width E		0.41		mm
4479	Height overall F		1.7		
4480	Height mold F1		1.5		mm

4481

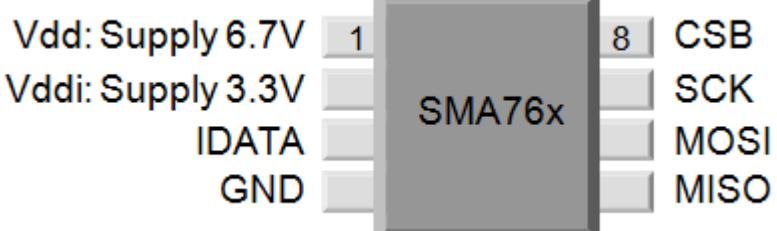


For more details about dimensions please refer to JEDEC MS-012F for SOICn packages  
A closed ground plane in the top layer of the PCB is recommended under the SMA. Otherwise electro-magnetic radiation from wires below the SMA may lead to disturbance of the sensor signal. Especially the area between pin 2 and pin 7 is sensitive to electro-magnetic interference.  
Bonddiagram and chip geometries (bottom view):



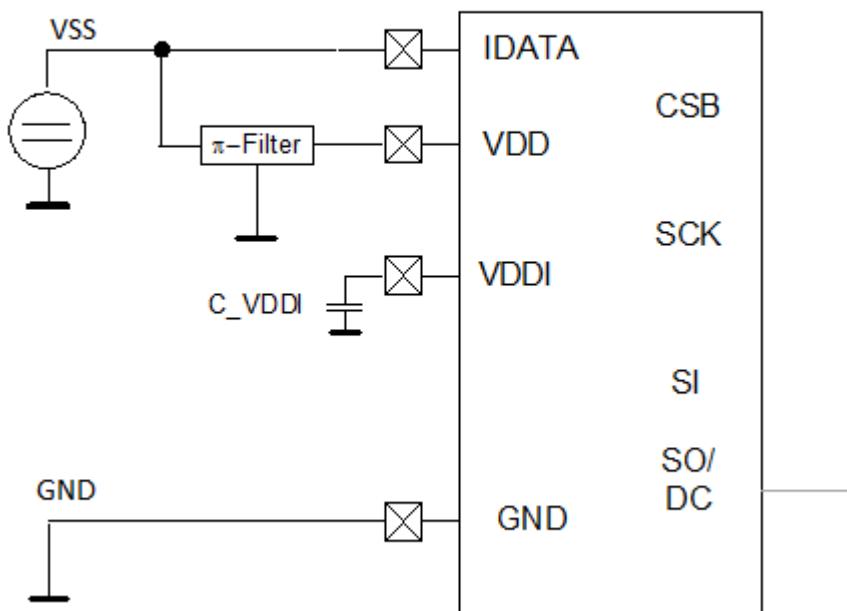
<Picture>

Pinout SOIC8 :



### 8.2.2 PSI mode

Application circuit PSI

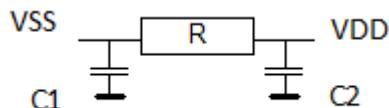
PSI  
(Mode 1)4255  
4256

The pins CSB, SCK and SI are only for final test and needs to be open /unconnected in PSI applications. The MISO pin can be used for daisy chain applications (please see PSI chapter for details). Otherwise it must also be open/unconnected.

4254

To fulfill all requirements from PSI5 spec, a filter circuit needs to be applied at VDD. Application of this filter needs to be done with regard to the overall system and is in responsibility of the customer.

For EMC tests the following Pi-filter has been used:



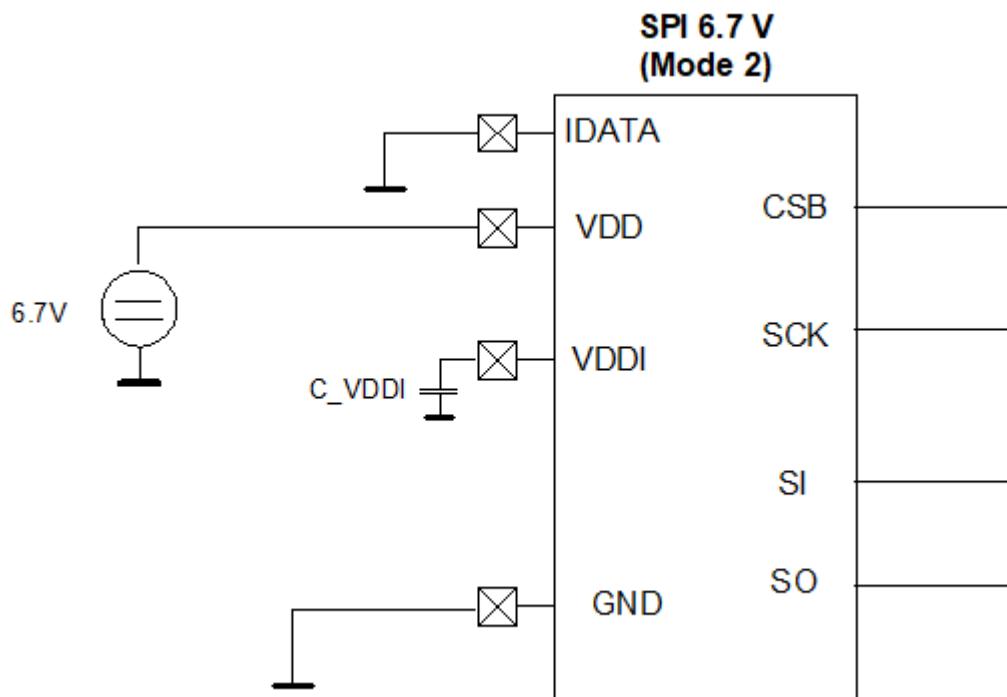
With C1=2.2nF, C2=15nF, R=62 Ohm

ID	parameter / condition	min	typ	max	unit
4253	External capacitor at VDDI	220	470	1300	nF

### 8.2.3 6.7V SPI mode (mode 2)

4257

Application circuit 6.7V SPI mode:



1547

**Application circuit:**

Only one mandatory external capacitor (connected at Vddi) is required.

During the EMC evaluation of the sensor nevertheless an additional capacitor connect to VDD is used to simulate capacitance of the VDD line the application. EMC performance may depend on the capacitance at VDD pin.

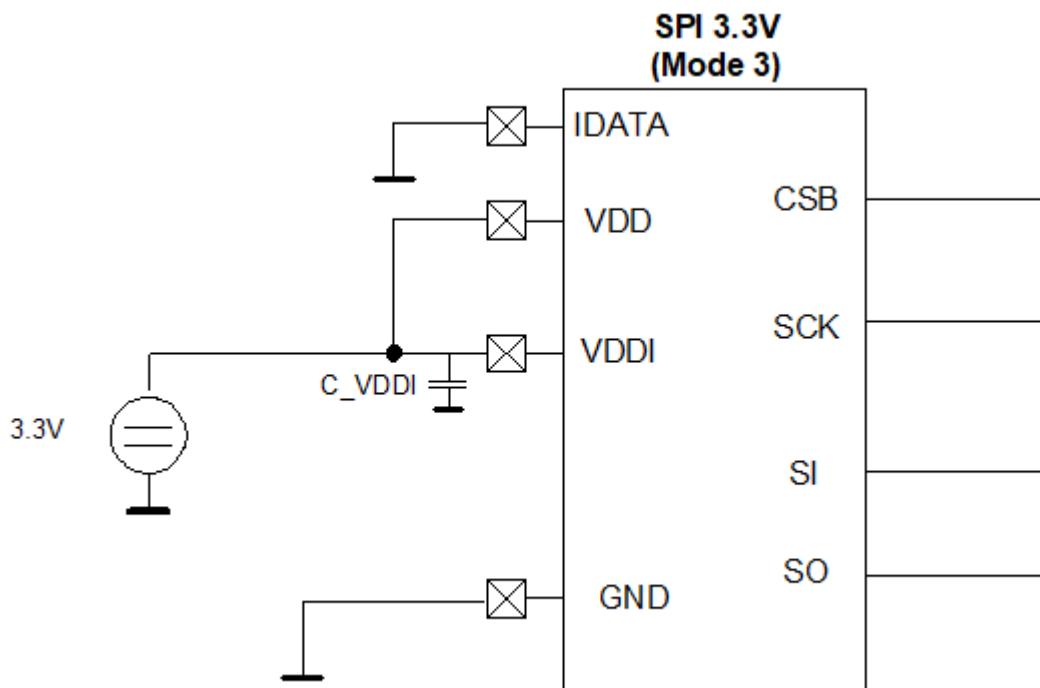
ID	parameter / condition	min	typ	max	unit
1548	External capacitor at VDDI 6.7V-mode	220	470	1300	nF
4259	Optional external capacitor at VDD 6.7V mode	0	100 *)	2600	nF

5521 \*) EMC conducted immunity tests performed with 100nF.

**8.2.4 3.3V SPI mode (mode 3)**

4258

Application circuit 3.3V SPI mode:



ID	parameter / condition	min	typ	max	unit
1549	External capacitor at VDDI 3.3V-mode; all capacitors on the supply line can be taken into account	220			nF

## 8.3 System in Package within LGA

1558 for Sensor Types SMA780/781/782/783/790/791/792/793

### 8.3.1 Mechanical properties

1580 The sensor module is suitable for application in PAS6e produced in 2k technology.  
5474 LGA is only released for further processing in 2k technology according to "RBEM-Process". The second level packaging has an influence on temperature effects on the sensor offset. Any other 2<sup>nd</sup> level packaging technology needs to be released explicitly.

For release of the 2k process in additional RB plants the offset behavior over temperature has to be characterized.

4536 The MSL classification is MSL3.

1578 Contact pads are made of material which is suitable for soldering.

3787 Substrate material: 2 layer -- Core: Mitsubishi CCL-HL832NS, Solder resist: Tayo PSR 4000 AUS320

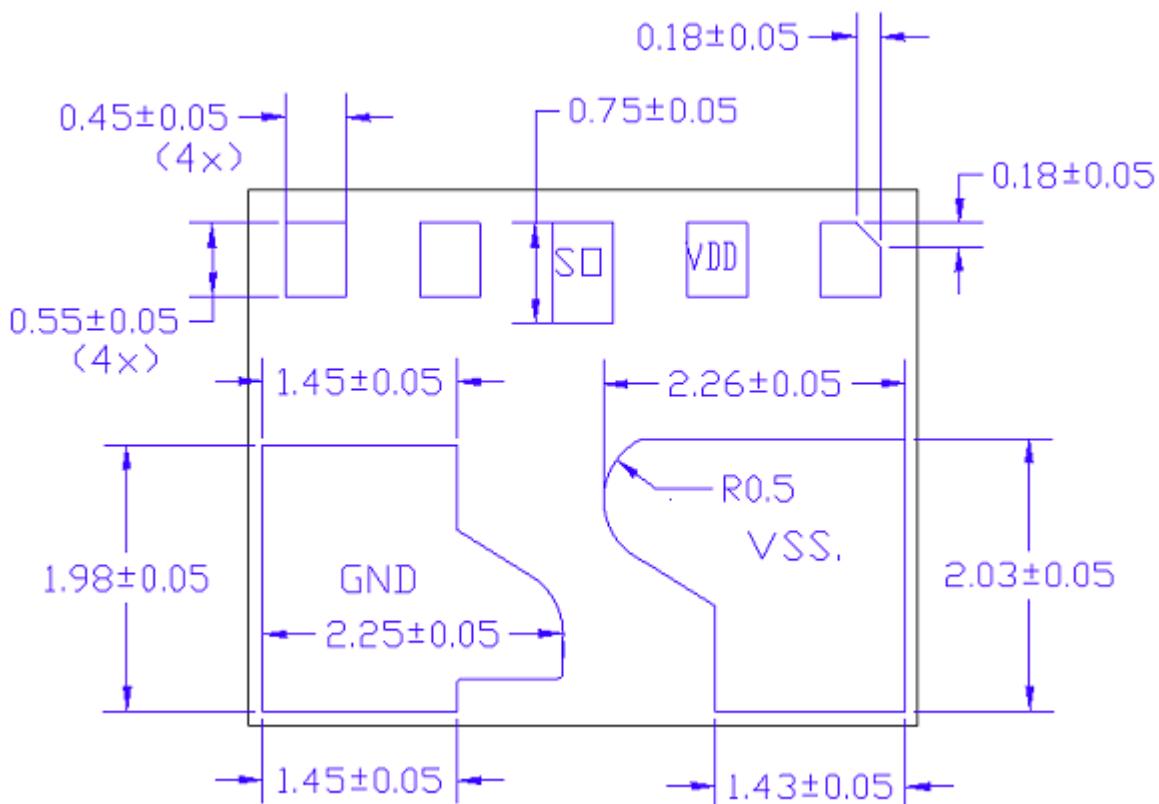
3789 Lead finish material: Cu – Ni – Au

3790 Die attach method: wet die attach

3791 Die attach material: ABLEBOND 2025D

3792 Wire bond method: thermosonic ball wedge

1560 Pinout (Top view):



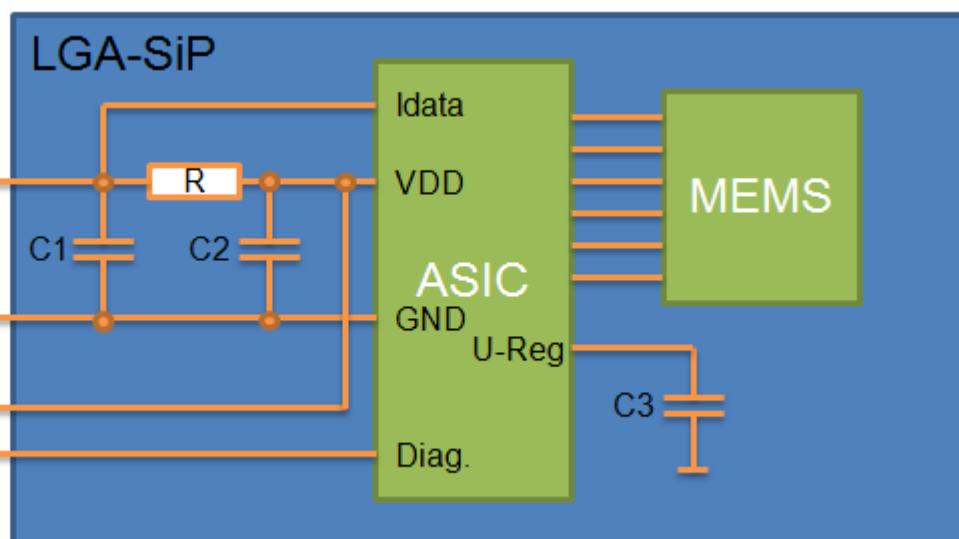
ID	parameter / condition	min	typ	max	unit
1563	Package dimensions along X	4.9	5	5.1	mm
1561	Package dimensions along Y	3.9	4	4.1	mm
1564	Package dimensions along Z	1.46	1.55	1.64	mm
1565	Flatness of surface  On molded side at room temperature. Shape is concave (edges are highest points.)			100	µm
1576	Clearance between pads	450			µm
1577	Clearance between diagnosis- and Vss/GND-pads	450			µm
3895	Size of labeling of LGA -->to be specified				mm

### 8.3.2 Application circuit PSI

1566

SiP-Circuit:

The SMA7 is designed as a system in a package (SIP). The package comprises all passive electronic components required for operation as satellite (see Circuit Diagram).



4499

For application only VSS and GND must be connected. VDD (Pi filter diagnostic) and SO (diagnosis) must be unconnected / open.

ID	parameter / condition	min	typ	max	unit
1567	R	-10%	62	+10%	Ohm
1568	C1	-40%	2.2	+40%	nF
1569	C2	-40%	15	+20%	nF
1570	C3	-27%	470	+11%	nF

1572

The passive components are dimensioned to be fully functional for all applied voltages at the SMA7 inputs within the specified voltage range (including sync pulse, ripple, and dynamic influences).

1574

All functionalities (i.e.  $\mu$ Cut; EMC;...) are as specified over the whole tolerance band of the C3 capacitor. All mandatory components are already integrated in the LGA package.

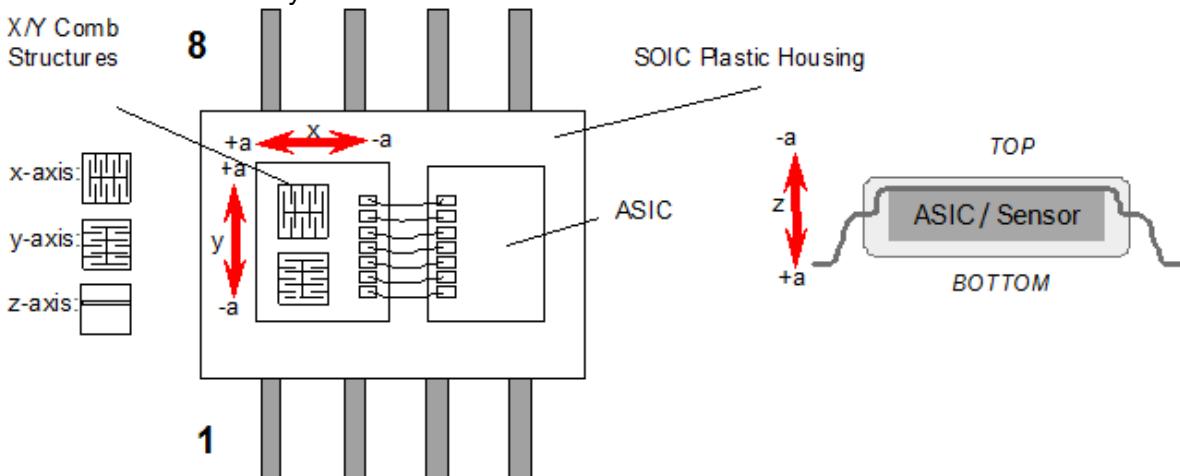
4498

## 8.4 Sensor Signal Orientation

### 8.4.1 SO8 SPI (SMA760/720/765)

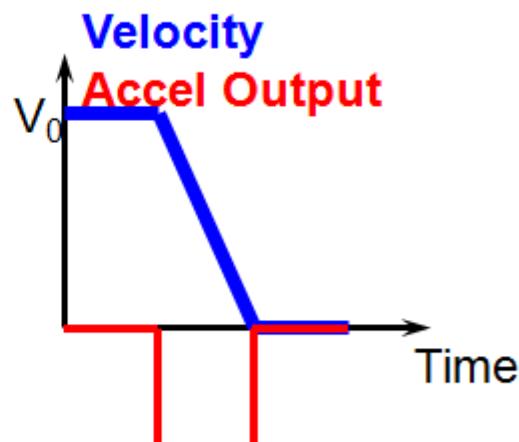
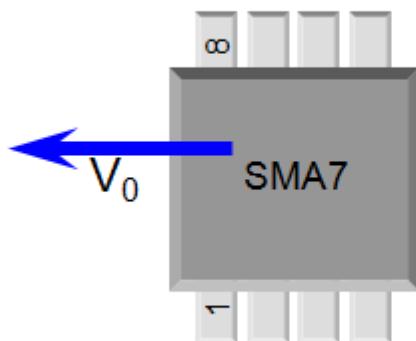
1584

SO8 SPI coordinate system:



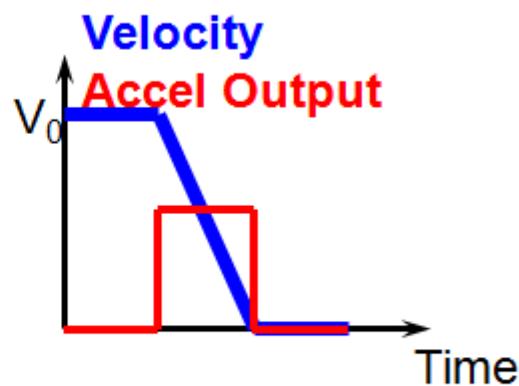
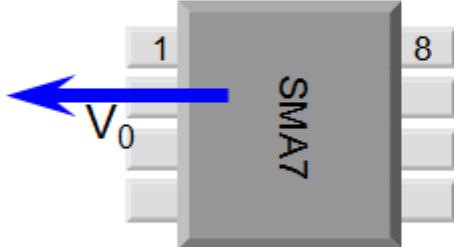
1585

Signal Polarity X (Channel1):



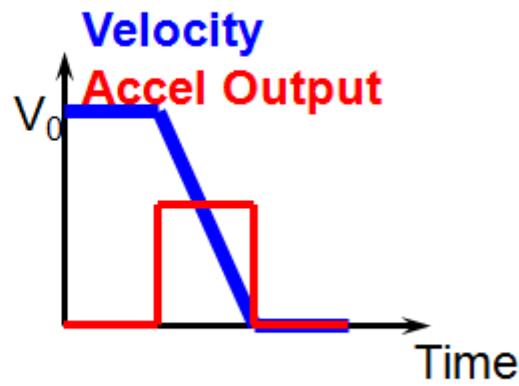
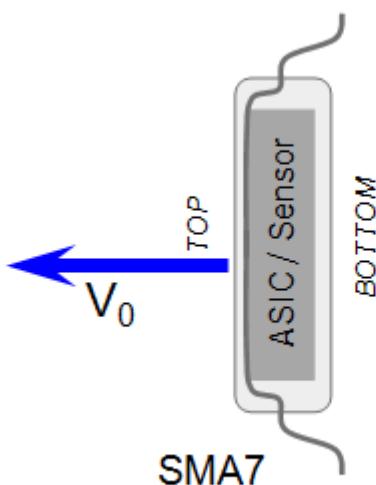
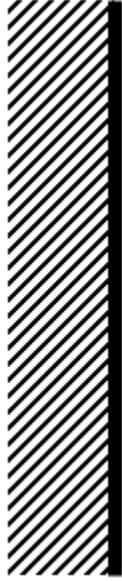
1586

Signal Polarity Y (Channel 2):



1587

Signal Polarity Z (Channel 2):



5236



Remark: For SMA765, SMA720, and SMA760 the sign bit for channel 1 is set to 0 and the sign bit for channel 2 is set to 1 during final test. This results in the shown polarities.

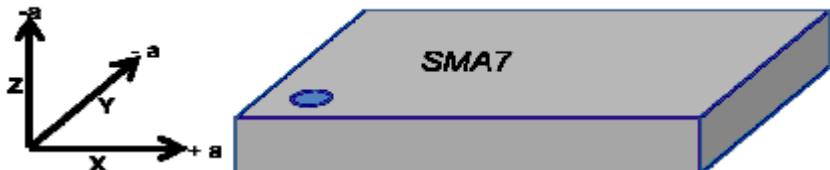
#### 8.4.2 LGA PSI5 (SMA780/781/782/783/790/791/792/793)

4503

All direction are valid, if sign bits in OTP are set to "0". Signal signs can be inverted by setting the sign bits by customer.

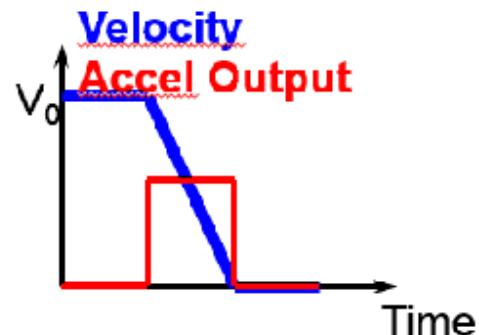
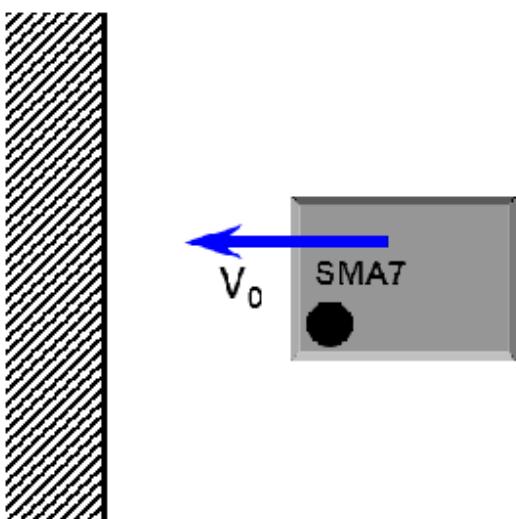
1594

LGA coordinate system:



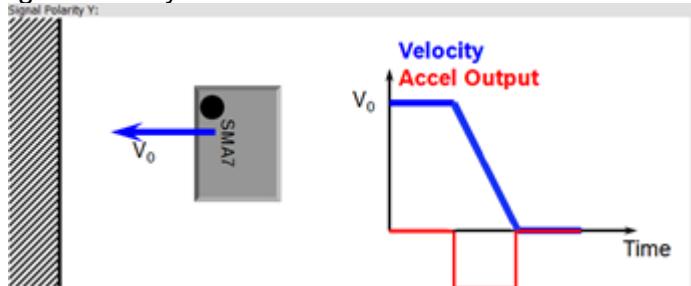
1596

Signal Polarity X:



1595

Signal Polarity Y:

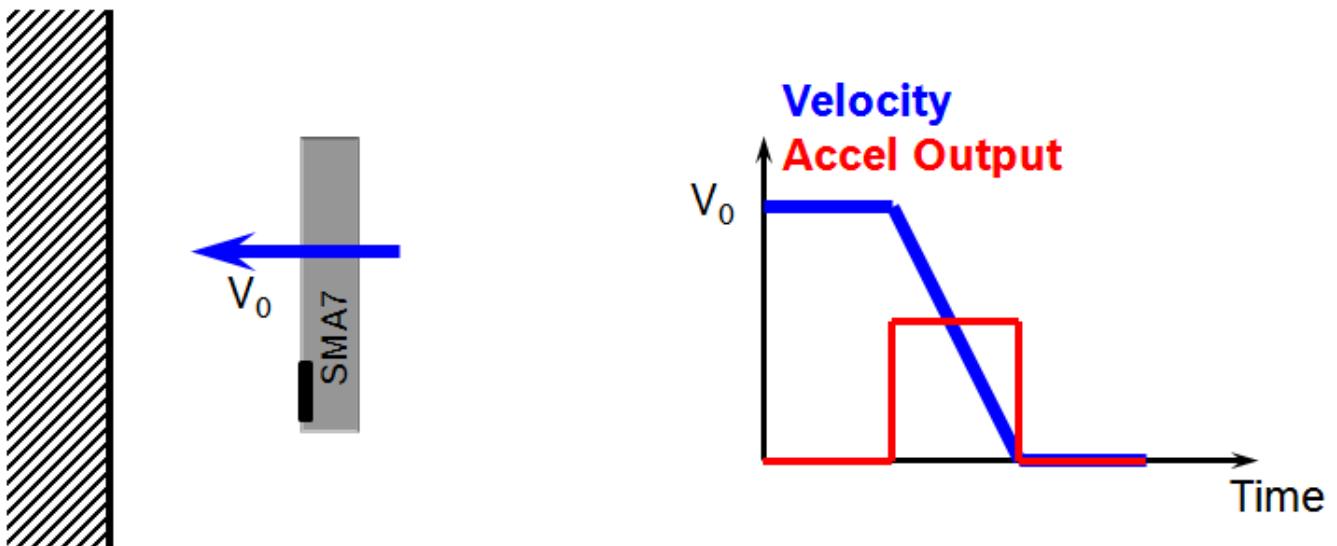


Time

Velocity  
Accel Output

1597

Signal Polarity Z:



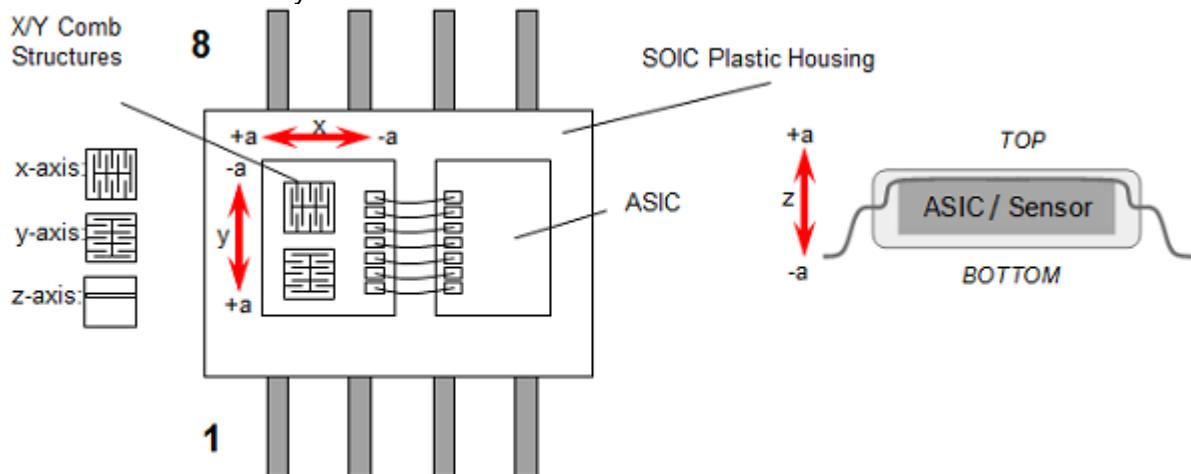
#### 8.4.3 SO8 PSI5

4504

All direction are valid, if sign bits in OTP are set to "0". Signal signs can be inverted by setting the sign bits by customer.

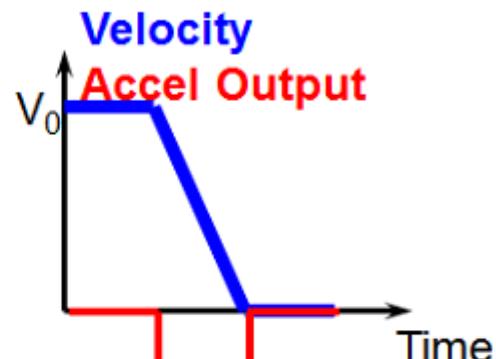
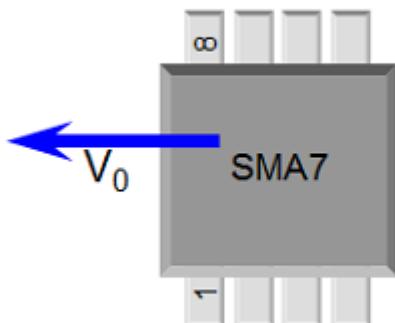
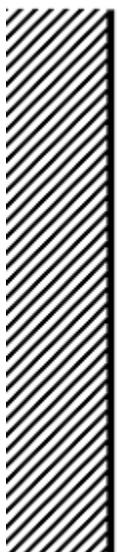
3171

SO8 PSI5 coordinate system:



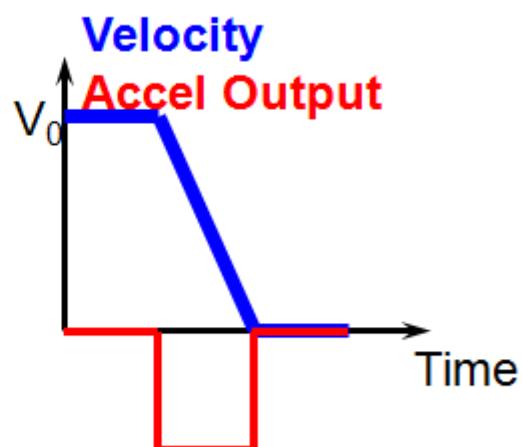
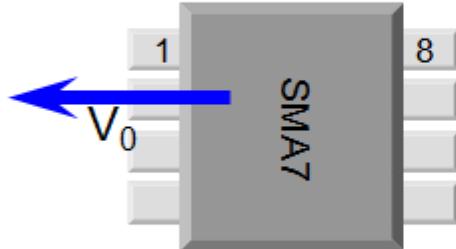
3172

Signal Polarity X:



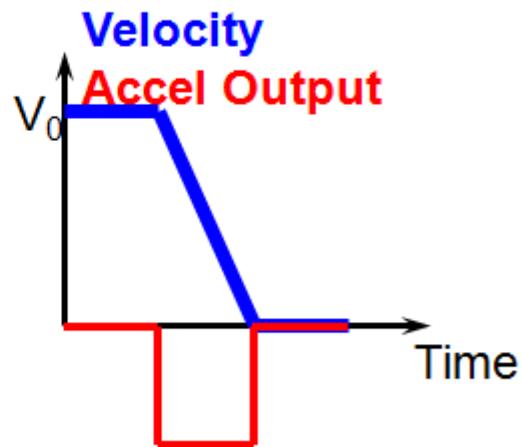
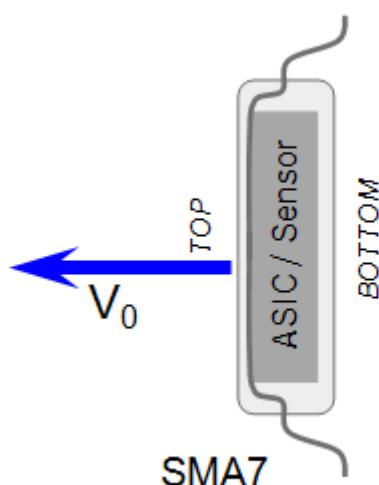
3173

Signal Polarity Y:



3174

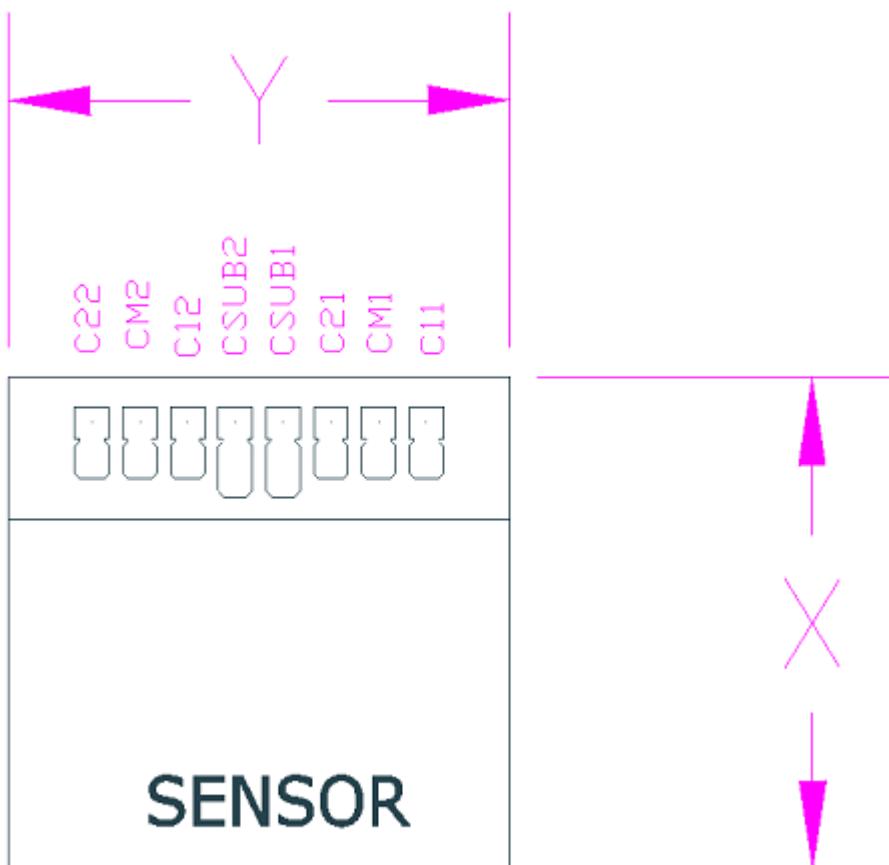
Signal Polarity Z:





## 8.5 MEMS physical dimensions

2840 Semiconductor material: silicon  
2841 MEMS process: PSB5MM8 with eutectic bonding.  
2842 Backside metallization: none.  
2843 Surface passivation material: none  
3808 Pinout:

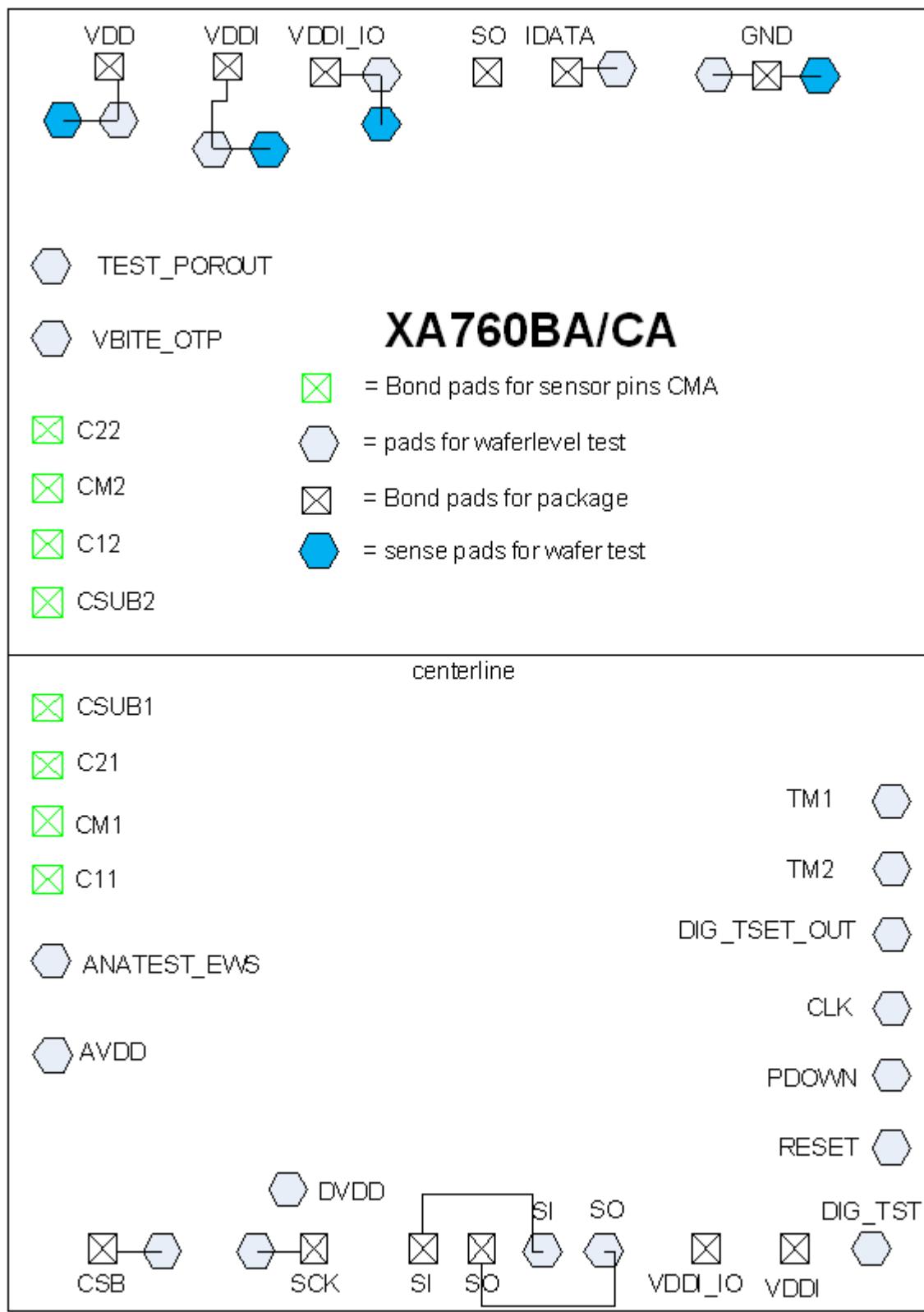


ID	parameter / condition	min	typ	max	unit
3773	Die dimension in X direction XY-types incl. Scribeline		1.02		mm
3774	Die dimension in Y direction XY-types incl. Scribeline		1.09		mm
4500	Die dimension in X direction XZ-types incl. Scribeline		1.15		mm
4501	Die dimension in Y direction XZ-types incl. Scribeline		1.3		mm
2845	Total Die thickness		550		µm
3775	Thickness substrate wafer		350		µm
3776	Thickness cap wafer		200		µm



## 8.6 ASIC physical dimensions

2849 Semiconductor material: silicon  
2850 Semiconductor technology (Process name): TSMC 0.13um CMOS High-Voltage Mixed-Signal Based  
Low-Power BCD  
2851 Backside metallization material: none  
2852 Contact metallization material: Tungsten  
2853 Surface passivation material: silicon nitrite  
3796 Pinout:



X

3799 SO and the VDDI pads are needed at two different positions to fulfill all package requirements. They are bonded depending on the package.

**BOSCH**

Department AE/ESI

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1.279.929.850

ID	parameter / condition	min	typ	max	unit
3777	Die dimension in X direction incl. Scribeline			1.55	mm
3778	Die dimension in Y direction incl. Scribeline			1.92	mm
3955	Die thickness after backgrinding		380		µm

3798

The two neighbouring VDDI pads are connected (short-circuited) in the package.



## 9. Parameters

1639 The sensor is designed to fulfill all requirements in this section after storage- and manufacturing process on module level on PCB or in PAS6e 2nd Level package. *Comment: Verification and qualification in 2nd level package is in responsibility of the customer.*

1640 All parameters in this section are guaranteed with at least 4 sigma over lifetime and under all of the specified operating conditions (e.g. temperature range, temperature sweeps with max. rate).

1641 For performance under EMC and PSRR conditions please refer to the corresponding chapters.  
For this document, 1G equals to 9.81m/s<sup>2</sup>.

### 9.1 Absolute Maximum Ratings

1643 All conditions within the absolute maximum ratings must not lead to any damage.

1644 Behaviour of the sensor for a supply voltage above the operating conditions, but inside absolute maximum rating is characterized for typical parts. No violation of spec parameters or irregular behaviour was observed.

*Comment: It is not allowed to use the sensor with voltages outside the operating conditions, even if the behaviour is described in the datasheet! For supply voltage below the operating conditions, but inside absolute maximum ratings the sensor is always in safe state.*

ID	parameter / condition	min	typ	max	unit
1645	Supply Voltage Vddi to GND; all modes	-0.3		+3.6	V
1647	Supply Voltage Vdd to GND	-0.3		+18	V
1648	Supply Voltage Vdd/Idata to GND (PSI5)	-0.3		+18	V
3207	Reverse Current Vdd/Idata to GND (PSI5); max. 100ms; voltage limited to max. -16.5V by ECU			160	mA
2172	Maximum Voltage *) CSB/SCK/MOSI/MISO (in tristate) to GND; all modes	-0.3		+3.6	V
1651	Maximum Voltage Not used pins to GND (PSI5)	-0.3		+3.6	V
3208	Drop height x, y,z-axis and/or random			1.5	m
3394	Mechanical shock t<1ms x,y,z-axis	-1000		+1000	g
3209	Mechanical shock t<0.5ms x,y,z-axis	-2000		+2000	g



ID	parameter / condition	min	typ	max	unit
3396	Mechanical shock  PSI5-types; 120g, 240g, 480g range; t<0.5ms  x,y,z- axis	-3000		+3000	g
1853	Mechanical shock  PSI5-types; 120g, 240g, 480g range; t<0.1ms;  x,y,z- axis	-5000		+5000	g

5199

\*) Higher voltage at SPI pins is allowed for limited time as specified in the SPI chapter.

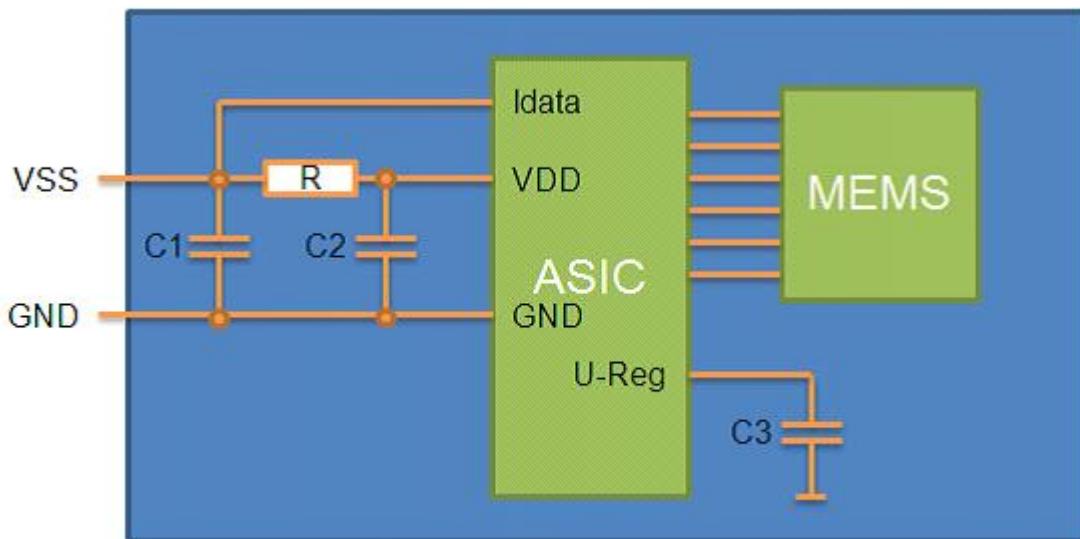
## 9.2 ESD robustness

ID	parameter / condition	min	typ	max	unit
3210	ESD – Voltage (any Pin)  HBM (acc. AECQ100)  IEC61340-3-1  VDD, VDDI, IDATA, SI, SO, CSB, CLK, GND	-2.0		+2.0	kV
3211	ESD – Voltage (any Pin)  MM (acc. AECQ100)  IEC61340-3-2  VDD, VDDI, IDATA, SI, SO, CSB, CLK, GND	-0.2		+0.2	kV
3212	ESD – Voltage (any Pin)  CDM (acc. AECQ100)  SI, CLK, GND	-0.5		+0.5	kV
3213	ESD – Voltage (Corner Pin)  CDM (acc. AECQ100)	-0.75		+0.75	kV
3603	ESD – Voltage  CDM (acc. AECQ100)  VDD, VDDI, GND, CSB, SO, IDATA	-0.75		+0.75	kV
1836	ESD Voltage HBM  Vdd; Idatal; GND for PSI5 devices; acc. AEC-Q100	-4		+4	kV
3931	ESD Voltage HBM  all internal pins	-800		+800	V
3456	<ul style="list-style-type: none"> <li>• <b>ESD (VDD, IDATA, GND)</b> <ul style="list-style-type: none"> <li>• Test acc. ISO10605 Limit class III (150pF/330Ohm)</li> <li>• discharge applied at VSS incl. target protection network (see picture below)</li> </ul> </li> </ul>	-8		+8	kV



ID	parameter / condition	min	typ	max	unit
	<ul style="list-style-type: none"> <li>GND is not connected (floating) during test</li> <li>3 discharges each voltage</li> </ul> Usage of Pi-Filter with nominal 2.2nF (C1, Vss side), 47Ohm (R) and 4.7nF (C2, Vdd side). Idata connected directly to Vss				

3924



Testsetup for ID3456, all other pins are not connected

### 9.3 Operating Conditions

1653

1654

Under all conditions listed below, the specification limits has to be fulfilled.

The ICs shall be used in Electronic Devices with an IP Code (International Protecting Rating) better or equal IP51 according the actually valid ISO 20653 Standard.

ID	parameter / condition	min	typ	max	unit
1656	Operation Temperature SPI types	-40	+25	+125	°C
2181	Operation Temperature LGA, VDD<8V all PSI modes	-40	+23	+125	°C
2178	Operation Temperature LGA, VDD>8V, synchronous single channel mode with parity bit	-40	+23	+125	°C
2180	Operation Temperature LGA, VDD>8V, synchronous dual channel mode/Asynchronous mode/ CRC modes	-40	+23	+120	°C
3917	Operation Temperature SO8, VDD<8V, all PSI modes	-40	+25	+125	°C



ID	parameter / condition	min	typ	max	unit
3916	Operation Temperature SO8, VDD>8V, P16CRC-500/2L and P20CRC-500/2L	-40	+25	+120	°C
3915	Operation Temperature SO8, VDD>8V, all other PSI modes	-40	+25	+125	°C
2174	Junction Temperature incl. selfheating of 15K	-40	+25	+140	°C

2176

For LGA the operating temperature refers to the ambient temperature outside of a PAS6e 2nd level package.

1674

For LGA application a thermal resistance of 111K/W is assumed for the combination of 1st and 2nd level package. (Value taken from SMA580 with PAS6).

ID	parameter / condition	min	typ	max	unit
1665	Temperature Gradient During Operation	-6		+6	K/min
1667	Supply Voltage SPI Vddi to GND (3.3V-SPI-Mode)	+3.13	+3.3	+3.47	V
1669	Supply Voltage SPI Vdd to GND (6.7V-SPI-Mode)	+4.5	+6.7	+11	V
1670	Supply Voltage PSI  <i>Please note, that VDD/IDATA are internal pins in case of LGA housing.</i> Vdd/Idata to GND	+4.5		+11	V
1672	Supply Voltage PSI Vss to GND (LGA package)	+5	6.7	+11	V
3887	Slew Rate of Supply Voltage Vdd, VDDI or Idata to GND	0.0005		1000	V/ms
3218	Maximum power-up time (sensor is ready for SPI communication) after hard reset.  SPI mode; C_VDDI=1300nF; VDD_slope or VDDI_slope = 5.5V/ms			3	ms

## 9.4 Electrical Characteristics

ID	parameter / condition	min	typ	max	unit
1676	Supply Current SPI-Mode;		3.2	4.9	mA
1681	Supply Current	+4		+6	mA



ID	parameter / condition	min	typ	max	unit
	Vdd+Idata to GND (PSI5); Supply voltage in spec				
1688	Supply Current Settling Time PSI5; Supply current within Spec; Current ripple Vdd/Idata to GND within +/-2mA; current limitation of source min. 50mA; after Supply voltage is in spec			5	ms
4470	Supply Current Drift Vdd to GND; over temperature and lifetime; +/- 4mA for whole bus (PSI5); after Initphase 1	-1		+1	mA
4471	Supply Current Driftrate Vdd to GND; over temperature and lifetime; +/- 1mA/s for whole bus (PSI5); after Initphase 1	-0.25		+0.25	mA/s
3222	Supply Current Ripple Vdd to GND (PSI5); after end of Init phase 1	-1		+1	mA
1683	Supply Current Influence of 2nd level package to tolerance window of LGA-SiP-Types is taken into account for tolerance calculation (mean value)		+0.02		mA
1684	Supply Current Influence of 2nd level package to tolerance window of LGA-SiP-Types is taken into account for tolerance calculation (Standard deviation)		0.02		mA
1685	Sink Current Vdd/Idata to GND (PSI5)	+22	+26	+30	mA
1686	Sink Current Influence of 2nd level package to tolerance window of LGA-SiP-Types is taken into account for tolerance calculation (mean value)		+0.1		mA
1687	Sink Current Influence of 2nd level package to tolerance window of LGA-SiP-Types is taken into account for tolerance calculation (Standard deviation)		0.08		mA
4241	Inrush/Startup Current 6.7V -Mode			100	mA
3220	Inrush/Startup Current 6.7V -Mode; C_VDDI=470nF or smaller			60	mA
3221	Short Current 6.7V -Mode, Short of VDDI to GND			350	mA
3223	Regulator Voltage	3.13		3.47	V



ID	parameter / condition	min	typ	max	unit
	Vddi to GND (6.7V-SPI-Mode)				
1692	Oscillator Frequency  <i>Note: Where not explicitly stated, timings are calculated with -4.2% ... +5.0% oscillator tolerance.</i> Including all mechanical stress from package	17.148 -4.2	17.9	18.437 +3.0	MHz %
1694	Oscillator Frequency  Influence of 2nd level package to tolerance window of LGA-SiP-Types has to be taken into account for tolerance calculation (mean value)		+0.3		%
1695	Oscillator Frequency  Influence of 2nd level package to tolerance window of LGA-SiP-Types has to be taken into account for tolerance calculation (Standard deviation)		0.05		%

## 9.5 Static Sensor Signal

3559

All values in this chapter are valid under static conditions (0Hz input signal).

### 9.5.1 Sensitivity

3557

Smallest measurable signal change is 1LSB (physical resolution, assuming no noise is present) for all modes, except 16bit PSI.

3230

This corresponds to 15,6mg for SMA760 and SMA720 X-Channel und 3,9mg for SMA720 Z-Channel .

4263

#### SPI types:

ID	parameter / condition	min	typ	max	unit
3234	Sensitivity SMA720/760; XY-Channel; 14Bit	61.8 -5	64	67.2 5	LSB/g %
3235	Sensitivity SMA720; Z-Channel; 14Bit	238.08 -7	256	273.92 +7	LSB/g %
5440	Sensitivity SMA765; 240g-Mode;	30.4 -5	32	33.6 +5	LSB/g %

4262

#### PSI5 types:

ID	parameter / condition	min	typ	max	unit
1707	Sensitivity 10 Bit PSI5-Types; 30g-Mode	14.88 -7	16	17.12 +7	LSB/g %
1708	Sensitivity PSI5-Types; 60g-Mode; 10 Bit	7.44 -7	8	8.56 +7	LSB/g %
1709	Sensitivity PSI5-Types; 120g-Mode; 10 Bit	3.72 -7	4	4.28 +7	LSB/g %



ID	parameter / condition	min	typ	max	unit
1710	Sensitivity PSI5-Types; 240g-Mode; 10 Bit	1.86 -7	2	2.14 +7	LSB/g %
1711	Sensitivity PSI5-Types; 480g-Mode; 10 Bit	0.93 -7	1	1.07 +7	LSB/g %
3238	Sensitivity PSI5-Types; 16 Bit, all ranges	59.52 -7	64	68.48 7	LSB/g %
1712	Sensitivity Influence of 2nd level package to tolerance window of LGA-SiP-Types has to be taken into account for tolerance calculation (mean value)		0		LSB/g
1713	Sensitivity Influence of 2nd level package to tolerance window of LGA-SiP-Types has to be taken into account for tolerance calculation (Standard deviation)		0.01		LSB/g
3239	Sensitivity Drift Lifetime; PSI5-Types	-5		+5	%
3240	Sensitivity Drift Temperature; PSI5-Types; typical values *1)	-0.03		+0.03	%/K
3241	Sensitivity Drift Ratiometrie; PSI5-Types; typical values *1)	-0.5		+0.5	%

4108

\*1) characterized parts are within this corridor; statistical fitting methods are used to reduce error from measurement equipment

ID	parameter / condition	min	typ	max	unit
1774	Crossaxis Sensitivity all Packages; 3sigma; Around X-/Y-/Z-Axis	-3.5 -2	0 0	+3.5 +2	% °
3288	Crossaxis Sensitivity SO8 Package; 3sigma; incl. PCB mounting	-3.6	0	+3.6	%

4843

The non linearity of the sensitivity is defined as the relative difference between the sensor output signal and a straight line fit of this signal. It is normalized to the full scale range (FS). As full scale the max. excitation in both directions is used. I.e. 240g for a +/-120g sensor. All values are also valid for sensors with max. raw offset.

The specification is also valid, if the straight line fit is done separately for positive and negative signals. In this case the max. excitation in one direction can be used as full scale range. I.e. 120g for a +/-120g sensor.



ID	parameter / condition	min	typ	max	unit
4264	Non Linearity of Sensitivity  SPI-types; XY-channels of PSI types; Z-channels of PSI-types with 30g, 60g and 120g range	-1		+1	%FS
4267	Non Linearity of Sensitivity  Z-channels of SMA751, 753, 781, 783  240g and 480g range	-1.5		+1.5	%FS
3290	Non Linearity of Sensitivity  SMA760, SMA720-X; FS defined as +/-5g	-100 -2		+100 +2	mg %FS
3291	Non Linearity of Sensitivity  SMA720-Z; FS defined as +/-5g	-50 -1.0		+50 +1.0	mg %FS
5383	Non Linearity of Sensitivity  SMA720-Z; FS defined as +/-2g	-20 -1.0		+20 +1.0	mg %FS
3289	Angular Acceleration Sensitivity  XY-channels of PSI5-Types	-5		+5	$\mu\text{g}^*\text{s}^2/\text{rad}$
5439	Angular Acceleration Sensitivity  Z-channels of PSI5-Types	-160		+160	$\mu\text{g}^*\text{s}^2/\text{rad}$

### 9.5.2 Range

ID	parameter / condition	min	typ	max	unit
3243	Full Scale Range  SMA720/760 XY-Channel	-128		+128	g
3244	Full Scale Range  SMA720;  Z-Channel	-32		+32	g
3245	Full Scale Range  PSI5-Types; 30g-Mode	-30		+30	g
3246	Full Scale Range  PSI5-Types; 60g-Mode	-60		+60	g
3247	Full Scale Range  PSI5-Types; 120g-Mode	-120		+120	g
3248	Full Scale Range  PSI5-Types; 240g-Mode  SMA765	-240		+240	g
3249	Full Scale Range	-480		+480	g



ID	parameter / condition	min	typ	max	unit
	PSI5-Types; 480g-Mode				

3561

All full scale range specifications are for nominal sensitivity. The sensitivity tolerance needs to be added or subtracted.

### 9.5.3 Noise

4269

#### Noise RMS

4268

Noise\_RMS is defined as the standard deviation of at least 10.000 samples taken with a sample rate of 2kHz. (As offset is not part of the noise, the standard deviation is used.)

4270

#### SPI types:

ID	parameter / condition	min	typ	max	unit
1716	Noise_RMS , SMA720/760, XY-channels 430Hz-Mode; SOC/XSOC		35	+50	mg
5441	Noise_RMS, 240g range SMA765 430Hz-Mode; SOC active		140	+200	mg
3572	Noise_RMS, SMA720/60, XY-channel 53Hz-Mode; XSOC active		14	20	mg
3565	Noise_RMS , SMA720/760, XY-channels 430Hz-Mode + 51Hz SW-Filter *3); XSOC/SOC active		12.5	+20	mg
1714	Noise_RMS, SMA720, Z-channel 53Hz-Mode; XSOC active		10	+12.5	mg
3562	Noise_RMS, SMA720, Z-channel 430Hz-Mode + 51Hz SW-Filter *3; XSOC active		10	+12.5	mg
3566	Noise_RMS 45°, SMA760 430Hz-Mode; SOC active; 45° calculation *4)		35	+80	mg
3570	Noise_RMS 45°, SMA760 SMA760; 430Hz-Mode + 51Hz SW Filter (*3) or 53Hz-Mode; XSOC active *4)		15	+40	mg

4271

#### PSI5 types:

ID	parameter / condition	min	typ	max	unit
1719	Noise_RMS, PSI5, 30/60g range SMA773/774 430Hz-Mode; 10 Bit; SOC active		35	+50	mg
4272	Noise_RMS, PSI5, 30/60g range SMA773/774 430Hz-Mode; 16 Bit mode; SOC active		35	+50	mg
1721	Noise_RMS,PSI5, 120g range		140	+200	mg

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<b>ID</b>	<b>parameter / condition</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>unit</b>
	SMA750/751/752/753/780/781/782/783 430Hz-Mode; 10 Bit; SOC active				
4273	Noise_RMS,PSI5, 120g range  SMA750/751/752/753/780/781/782/783 430Hz-Mode; 16Bit mode; SOC active		140	+200	mg
5562	Noise_RMS,PSI5, 120g/240g/480g range  SMA750/751/752/753/780/781/782/783 215Hz-Mode; 10/16 Bit; SOC active		100	+150	mg
5563	Noise_RMS,PSI5, 120g/240g/480g range  SMA750/751/752/753/780/781/782/783 860Hz-Mode; 10/16 Bit; SOC active		200	+290	mg
1727	Noise_RMS,PSI5, 480g range  SMA750/751/752/753/781/783 430Hz-Mode; 10 Bit; SOC active		140	+200	mg
4275	Noise_RMS,PSI5, 480g range  SMA750/751/752/753/781/783 430Hz-Mode; 16 Bit mode; SOC active		140	+200	mg
1729	Noise_RMS, PSI5, 480g range  SMA755/757/790/792 430Hz-Mode; 10 Bit; SOC active		250	+400	mg
4277	Noise_RMS, PSI5, 480g range  SMA755/757/790/792 430Hz-Mode; 16 Bit mode; SOC active		250	+400	mg
5564	Noise_RMS,PSI5, 240g/480g range  SMA755/757/790/792 215Hz-Mode; 10/16 Bit; SOC active		190	+290	mg
5565	Noise_RMS,PSI5, 240g/480g range  SMA755/757/790/792 860Hz-Mode; 10/16 Bit; SOC active		390	+570	mg
1723	Noise_RMS,PSI5, 240g range  SMA750/751/752/753/780/781/782/783 430Hz-Mode; 10 Bit; SOC active		140	+200	mg
4274	Noise_RMS,PSI5, 240g range  SMA750/751/752/753/780/781/782/783 430Hz-Mode; 16 Bit mode; SOC active		140	+200	mg
1725	Noise_RMS, PSI5, 240g range  SMA755/757/790/792 430Hz-Mode; 10 Bit; SOC active		270	+400	mg
4276	Noise_RMS, PSI5, 240g range  SMA755/757/790/792		270	+400	mg



ID	parameter / condition	min	typ	max	unit
	430Hz-Mode; 16 Bit mode; SOC active				
1731	Noise_RMS  Influence of 2nd level package to tolerance window of LGA-SiP-Types has to be taken into account for tolerance calculation (mean value; Testing Conditions: 2.000 Samples)		-0.02		LSB
1732	Noise_RMS  Influence of 2nd level package to tolerance window of LGA-SiP-Types has to be taken into account for tolerance calculation (Standard deviation; Testing Conditions: 2.000 Samples)		0.05		LSB

4278

3574

5172

4279

**Noise\_Peak**

The limit for Noise\_Peak is defined as +/- 4 \* Noise\_RMS. This means that all data points of a measurement are with at least 4 sigma within the Noise\_peak limits. (This is equivalent to a probability of 1:15787 to find a data point, which is outside the limits). All noise measurements are done with at least 10.000 samples at a sample rate of 2kHz.

Remark: If Noise\_Peak is not calculated by Noise\_RMS, but directly measured, all values need to be rounded up to full LSB.

**SPI types:**

ID	parameter / condition	min	typ	max	unit
1733	Noise_Peak, SMA720, Z-channel  430Hz-Mode + 51Hz SW-Filter (*3); SOC active	-50	0	+50	mg
3266	Noise_Peak, SMA720, Z-channel  53Hz-Mode; XSOC active	-50		+50	mg
3268	Noise_Peak, SMA720, Z-channel  430Hz-Mode + 51Hz SW Filter (*3); XSOC active	-50		+50	mg
1735	Noise_Peak, SMA720/760, XY-channels  430Hz-Mode; SOC/XSOC active	-200	0	+200	mg
3263	Noise_Peak, SMA720/760, XY-channels  430Hz-Mode + 51Hz SW Filter (*3); XSOC active	-80		+80	mg
3267	Noise_Peak, SMA720, X-channel  53Hz-Mode; XSOC active	-80		+80	mg
3264	Noise_Peak, SMA760, 45°  430Hz-Mode; SOC active; 45°  (*4)	-320		+320	mg
3265	Noise_Peak, SMA760, 45°  430Hz-Mode + 51Hz SW Filter (*3); XSOC active; 45°  (*4)	-160		+160	mg



ID	parameter / condition	min	typ	max	unit
5442	Noise_Peak, 240g range; SMA765 430Hz-Mode; SOC active	-800	0	+800	mg

3298

\*3)

## 51Hz SW-Filter

MATLAB implementation for 2khz sample rate:

a = [1, -25/32]; b=[7/32, 0]; %51Hz filter

temp = filter(b, a, rawdata);

output = filter(b, a, temp);

3299

\*4)

## 45° Application

$$X = (CH1 - CH2) / \text{SQRT}(2)$$

$$Y = (CH1 + CH2) / \text{SQRT}(2)$$

4280

## PSI5 types:

ID	parameter / condition	min	typ	max	unit
3272	Noise_Peak, PSI5, 30g range SMA773/774 10 Bit; 430Hz-Mode; SOC active	-200 -4	0 0	+200 +4	mg LSB
3273	Noise_Peak, PSI5, 60g range SMA773/774 10 Bit; 430Hz-Mode; SOC active	-200 -2	0 0	+200 +2	mg LSB
4281	Noise_Peak, PSI5, 30/60g range SMA773/774/775 16 Bit mode; 430Hz-Mode; SOC active	-13	0	+13	LSB
1738	Noise_Peak, PSI5, 120g range SMA750/751/752/753/780/781/782/783 10 Bit; 430Hz-Mode; SOC active	-800 -4	0 0	+800 +4	mg LSB
1740	Noise_Peak, PSI5, 240g range SMA750/751/752/753/780/781/782/783 10 Bit; 430Hz-Mode; SOC active	-800 -2	0 0	+800 +2	mg LSB
4283	Noise_Peak, PSI5, 120/240g range, 480g range where applicable SMA750/751/752/753/780/781/782/783 16 Bit mode; 430Hz-Mode; SOC active	-52	0	+52	LSB
1742	Noise_Peak, PSI5, 240g range SMA755/757/790/792 10 Bit; 430Hz-Mode; SOC active	-1.6 -4	0 0	+1.6 +4	g LSB
1746	Noise_Peak, PSI5, 480g range SMA755/757/790/792; SMA783/781/751/753 10 Bit; 430Hz-Mode; SOC active	-1.6 -2	0 0	+1.6 +2	g LSB
4284	Noise_Peak, PSI5, 240/480g range SMA755/757/790/792 16 Bit mode; 430Hz-Mode; SOC active	-103	0	+103	LSB



ID	parameter / condition	min	typ	max	unit
1744	Noise_Peak, ,PSI5, 480g range  SMA750/752 10 Bit; 430Hz-Mode; SOC active	-800 -1	0 0	+800 +1	mg LSB
4285	Noise_Peak, ,PSI5, 480g range  SMA750/752 16 Bit mode; 430Hz-Mode; SOC active	-52	0	+52	LSB

#### 9.5.4 Offset

4286

The residual offset after FOC is the remaining offset directly after startup and initialization of the sensor at 0g input. It depends on the used FOC setting. It is defined as the mean value of 10000 samples with a sample rate of 2kHz and deactivated SOC. (This means, that with an activated SOC the values will be equal to or better than specified.)

5516

The residual offset without SOC is the maximum offset during one power-on phase, if the sensor is used with FOC, but without SOC or XSOC. It is defined as the mean value of 10000 samples with a sample rate of 2kHz and for 0g input.

5517

The residual offset without FOC is the maximum offset, if the sensor is used without FOC and without SOC or XSOC. It is defined as the mean value of 10000 samples with a sample rate of 2kHz and for 0g input.

ID	parameter / condition	min	typ	max	unit
3825	Residual Offset after FOC  SMA760/720-X 430Hz Filter ;256 or 512 samples FOC (32ms/64ms); referenced to 14bit SPI; without disturbance	-2 -31	0 0	+2 +31	LSB mg
3920	Residual Offset after FOC  SMA760/720-X 430Hz Filter;1024 samples FOC (128ms); referenced to 14bit SPI; without disturbance	-1.5 -23.5	0 0	+1.5 +23.5	LSB mg
3826	Residual Offset after FOC  SMA720-Z 430Hz; 512 samples FOC (64ms); referenced to 14bit SPI; without disturbance	-6 -23.5	0 0	+6 +23.5	LSB mg
3827	Residual Offset after FOC  SMA720-Z 430Hz; 1024 samples FOC (128ms); referenced to 14bit SPI; without disturbance	-5 -19.5	0 0	+5 +19.5	LSB mg
4312	Residual Offset after FOC  SMA720-Z 53Hz; 64 samples FOC (64ms); referenced to 14bit SPI; without disturbance	-8 -31	0 0	+8 +31	LSB mg
4313	Residual Offset after FOC  SMA720-Z	-5 -19.5	0 0	+5 +19.5	LSB mg

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ID	parameter / condition	min	typ	max	unit
	53Hz; 128 samples FOC (128ms); referenced to 14bit SPI; without disturbance				
5473	Residual Offset after FOC  SMA765 SMA765, 430 Hz, OC length = 512 samples without disturbances	-16	0	+16	LSB
4322	Residual offset without FOC  SMA760/720-X	-8		8	g
4323	Residual offset without FOC  SMA720-Z	-5		5	g
5443	Residual offset without FOC  SMA765	-25		25	g
5370	Residual offset without SOC  SMA760/SMA720-X	-4		4	g
5369	Residual offset without SOC  SMA720-Z	-2		2	g

3921

Remark: Applying an external low pass filter (e.g. 50Hz) in addition to the internal filter (e.g. 430Hz) does not reduce the residual offset after FOC.

4320

**PSI5 types:**

ID	parameter / condition	min	typ	max	unit
4321	Residual Offset after FOC  Peripheral-Types; 10bit; without disturbances	-1	0	+1	LSB
4324	Residual offset without FOC  SMA773/SMA774-X (30/60g, SO8, XY)	-8		8	g
5372	Residual offset without SOC  SMA773/SMA774-X	-4		4	g
4327	Residual offset without FOC  SMA774-Z (30/60g, SO8, XZ)	-5		5	g
5378	Residual offset without SOC  SMA774-Z	-2		2	g
4326	Residual offset without FOC  SMA750/752 (120/240/480g, SO8, XY)	-25		25	g
5373	Residual offset without SOC  SMA750/752	-22		22	g
4329	Residual offset without FOC  SMA755/757 (480 g, SO8, XY)	-50		50	g
5374	Residual offset without SOC  SMA755/757	-35		35	g



ID	parameter / condition	min	typ	max	unit
4330	Residual offset without FOC  SMA751/753-X (120/240/480g, SO8, XZ)	-30		30	g
5375	Residual offset without FOC  SMA751/753-Z (120/240/480g, SO8, XZ)	-50		50	g
5376	Residual offset without SOC  SMA751/753-X (120/240/480g, SO8, XZ)	-25		25	g
5377	Residual offset without SOC  SMA751/753-Z (120/240/480g, SO8, XZ)	-30		30	g

4287

The offset is the remaining long-term offset of a running sensor at 0g input. The values are valid after running the FOC and running the SOC for at least 5s or the XSOC for at least 100s. It is defined as the mean value of 10.000 samples for SOC and 10.000 samples for XSOC. Each with a sample rate of 2kHz.

4290

#### SPI types:

ID	parameter / condition	min	typ	max	unit
1763	Offset  SMA720/760 SOC active  Full temperature range with temperature gradient <= 6K/min	-0.5	0	+0.5	LSB
1764	Offset 45°  SMA760 SOC active  Full temperature range with temperature gradient <= 6K/min *4)	-0.5	0	+0.5	LSB
1765	Offset  SMA720/760 XSOC active  Constant temperature	-0.5	0	+0.5	LSB
1766	Offset 45°  SMA760 XSOC active  Constant temperature *4)	-0.5	0	+0.5	LSB
5577	Offset  SMA720-Z XSOC active; 53 Hz filter  Full temperature range with temperature gradient <= 3K/min	-0.75	0	+0.75	LSB
5578	Offset	-1.5	0	+1.5	LSB

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ID	parameter / condition	min	typ	max	unit
	SMA720-Z XSOC active; 53 Hz filter  Full temperature range with temperature gradient <= 6K/min				
5579	Offset  SMA720-X XSOC active; 430 Hz filter  Full temperature range with temperature gradient <= 3K/min	-1.25	0	+1.25	LSB
5580	Offset  SMA720-X XSOC active; 430 Hz filter  Full temperature range with temperature gradient <= 6K/min	-2.5	0	+2.5	LSB
5581	Offset, Offset 45°  SMA760 XSOC active; 430 Hz filter  Full temperature range with temperature gradient <= 3K/min	-0.75	0	+0.75	LSB
5582	Offset, Offset 45°  SMA760 XSOC active; 430 Hz filter  Full temperature range with temperature gradient <= 6K/min	-1.5	0	+1.5	LSB
5444	Offset  SMA765 SOC active  32 LSB/g	-4	0	+4	LSB

4289

\*4)

45° Application

$$X = (CH1 - CH2) / \text{SQRT}(2)$$

$$Y = (CH1 + CH2) / \text{SQRT}(2)$$

4291

**PSI types:**

ID	parameter / condition	min	typ	max	unit
1767	Offset, PSI5 types, 10 Bit  SOC active	-0.5	0	+0.5	LSB
4914	Offset, PSI5 types 16 bit  all types except SMA755, 757, 790, 792 SOC active	-8	0	+8	LSB
5082	Offset, PSI5 types 16bit	-16	0	+16	LSB



ID	parameter / condition	min	typ	max	unit
	SMA755, 757, 790, 792 SOC active				

### 9.5.5 Moving average offset

3601

The sliding moving average of 100 values (MA100) is calculated from the 0 g sensor signal (X) in the following way:

$$\text{MA100}(t_0) = (X(t_0) + X(t_0-t) + X(t_0-2t) + \dots + X(t_0-99t)) / 100$$

These calculated signal is with a probability of 4 standard deviations (1:15787) within the limits given below.

3602

The sliding moving average of 10 values (MA10) is calculated from the 0 g sensor signal (X) in the following way:

$$\text{MA10}(t_0) = (X(t_0) + X(t_0-t) + X(t_0-2t) + \dots + X(t_0-9t)) / 10$$

These calculated signal is with a probability of 4 standard deviations (1:15787) within the limits given below.

4296

#### SPI types:

4292

The residual moving average offset is the remaining offset directly after startup and initialization of the sensor at 0 g input. It is defined as the sum of the residual offset (defined above) and the corresponding long-term moving average offset (defined below). This means, that the calculated moving average signal directly after FOC is with a probability of 4 standard deviations within the limits specified below. As the residual offset is measured without SOC, it also means, that with an activated SOC the values will be equal or better, then specified.

ID	parameter / condition	min	typ	max	unit
4298	Residual Moving average offset MA100  SMA720-Z 53Hz-Mode; 64 FOC samples (64ms)	-55		+55	mg
4305	Residual Moving average offset MA100  SMA720-Z 53Hz-Mode; 128 FOC samples (128ms)	-40		+40	mg
4314	Residual Moving average offset MA100  SMA720-Z 430Hz-Mode + 51Hz SW Filter (*3); 512 samples FOC (64ms)	-45		+45	mg
4315	Residual Moving average offset MA100  SMA720-Z 430Hz-Mode + 51Hz SW Filter (*3); 1024 samples FOC (128ms)	-40		+40	mg
4299	Residual Moving average offset MA100  SMA720-X 53Hz-Mode; 64 FOC samples (64ms)	-75		+75	mg
4311	Residual Moving average offset MA100  SMA720-X	-75		+75	mg



ID	parameter / condition	min	typ	max	unit
	53Hz-Mode; 128 FOC samples (128ms)				
4302	Residual Moving average offset MA100 SMA760, SMA720-X 430Hz-Mode + 51Hz SW Filter (*3); 512 or 1024 FOC samples (64/128ms)	-75		+75	mg
4301	Residual Moving average offset MA10 SMA760, SMA720-X 430Hz-Mode; 512 or 1024 FOC samples (64ms/128ms)	-120		+120	mg
4303	Residual Moving average offset MA10, 45° SMA760 430Hz-Mode; (*4); 512 or 1024 FOC samples (64/128ms)	-120		+120	mg
4304	Residual Moving average offset MA100, 45° SMA760 430Hz-Mode + 51Hz SW Filter (*3); (*4); 512 or 1024 FOC samples (64/128ms)	-100		+100	mg

4293

The moving average offset is the remaining long-term offset of a running sensor at 0 g input. The values are valid after running the FOC and running the SOC for at least 5s or the XSOC for at least 100s (if not stated otherwise). After this time the calculated moving average signal is with a probability of 4 standard deviations within the limits specified below. It is defined for a sample rate of 2 kHz.

4295

**SPI types:**

ID	parameter / condition	min	typ	max	unit
3282	Moving average offset MA100 SMA720-Z 53Hz-Mode; XSOC active; Full temperature range with temperature gradient <= 6K/min	-20		+20	mg
3283	Moving average offset MA100 SMA720-X 53Hz-Mode; XSOC active; Full temperature range with temperature gradient <= 6K/min	-50		+50	mg
3284	Moving average offset MA100 SMA720-Z 430Hz-Mode + 51Hz SW Filter (*3); XSOC active; Full temperature range with temperature gradient <= 6K/min	-20		+20	mg
3278	Moving average offset MA10 SMA760, SMA720-X	-100		+100	mg

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ID	parameter / condition	min	typ	max	unit
	430Hz-Mode; XSOC active; Full temperature range with temperature gradient <= 6K/min				
3279	Moving average offset MA100  SMA760, SMA720-X 430Hz-Mode + 51Hz SW Filter (*3); XSOC active; Full temperature range with temperature gradient <= 3K/min	-50		+50	mg
5585	Moving average offset MA100  SMA760, SMA720-X 430Hz-Mode + 51Hz SW Filter (*3); XSOC active; Full temperature range with temperature gradient <= 6K/min	-60		+60	mg
3280	Moving average offset MA10, 45°  SMA760 430Hz-Mode; XSOC active; Full temperature range with temperature gradient <= 6K/min (*4)	-100		+100	mg
3281	Moving average offset MA100, 45°  SMA760 430Hz-Mode + 51Hz SW Filter (*3); XSOC active; Full temperature range with temperature gradient <= 3K/min (*4)	-50		+50	mg
5586	Moving average offset MA100, 45°  SMA760 430Hz-Mode + 51Hz SW Filter (*3); XSOC active; Full temperature range with temperature gradient <= 6K/min (*4)	-60		+60	mg
5445	Moving average offset MA10  SMA765 430Hz Mode; SOC active; 32 LSB/g  5s after startup;	-12	0	+12	LSB

3599

\*3)

51 Hz SW-Filter

MATLAB implementation for 2 kHz sample rate:

a = [1, -25/32]; b = [7/32, 0]; %51Hz filter

temp = filter(b, a, rawdata);

output = filter(b, a, temp);

3600

\*4)

45° Application

$$X = (CH1 - CH2) / \text{SQRT}(2)$$

$$Y = (CH1 + CH2) / \text{SQRT}(2)$$

4294

**PSI5 types:**

The values of the PSI moving average offset are valid after running the FOC and running the SOC for the specified time. After this time the calculated moving average signal is with a probability of 3 standard deviations within the limits specified below. It is defined for a sample rate of 2 kHz.



ID	parameter / condition	min	typ	max	unit
1768	Moving average offset MA10  all PSI5 types 10 Bit; 430Hz Mode; SOC active; 5s after startup	-1	0	+1	LSB
4915	Moving average offset MA10  all PSI5 types all types except SMA755, 757, 790, 792 16 Bit; 430Hz Mode; SOC active; 5s after startup;	-24	0	+24	LSB
5081	Moving average offset MA10  SMA755, 757, 790, 792 16 Bit; 430Hz Mode; SOC active; 5s after startup;	-48	0	+48	LSB

### 9.5.6 Clipping

ID	parameter / condition	min	typ	max	unit
1780	Mechanical Clipping, SMA720/760 XY-channels and SMA773/774 XY channels  (incl. electrostatic effects)	+/-220	+/-300 (SMA760/773) +/-290 (SMA720/774)		g
1781	Mechanical Clipping  SMA774 Z-channel and SMA720 Z-channel incl. electrostatic effects	+/-100	+170/-140		g
1782	Mechanical Clipping  SMA751/753/781/783 incl. electrostatic effects	+/-960	+/-1230 (X) +1430/-1240 (Z)		g
4066	Mechanical Clipping  SMA750/752/780/782/765 incl. electrostatic effects	+/-960	+/-1260		g
1784	Mechanical Clipping  SMA755/757/790/792 incl. electrostatic effects	+/-1500	+/-2020		g
1787	Interface Clipping  SPI interface; 14 Bit	-8191		+8191	LSB
1788	Interface Clipping  PSI5 interface; 10 Bit	-480		+480	LSB



### 9.5.7 BITE

ID	parameter / condition	min	typ	max	unit
4426	Selftest tolerance SMA720; relative to stored values	-12	0	+12	%
1795	Selftest tolerance SMA760; relative to stored values	-10	0	+10	%
3296	Selftest tolerance PSI5-Types; relative to stored values, SMA765	-30	0	+30	%
3297	Selftest tolerance PSI5-Types; relative to stored values for new part @T= 15°C - 55°C	-5	0	+5	%
5450	self test SMA760/773 CMA581R	15		50	g
5451	self test SMA720/774 -X CMA582R	12.8		31	g
5452	self test SMA720/774 -Z CMA582R	7		32	g
5453	self test SMA752/765/750/758/782/780/757/755/792/790, SMA753/783 -X CMA584R, CMA588R, CMA585R-X	41		197	g
5456	self test SMA753/783/751/781 -Z CMA585R-Z	23		227	g

## 9.6 Dynamic sensor signal

### 9.6.1 Cut-off Frequency

ID	parameter / condition	min	typ	max	unit
379	Tolerance of Cutoff Frequency for all filters specified below incl. Oscillator tolerance	-5	0	+5	%

4340

### SPI types:

ID	parameter / condition	min	typ	max	unit
373	Nominal Cutoff Frequency SMA760/SMA720-X 430Hz Filter Mode; incl. MEMS		423		Hz
5085	Nominal Cutoff Frequency		415		Hz

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ID	parameter / condition	min	typ	max	unit
	SMA720-Z 430Hz Filter Mode; incl. MEMS				
374	Nominal Cutoff Frequency SMA720/760 215Hz Filter Mode; incl. MEMS		215		Hz
375	Nominal Cutoff Frequency SMA720/760 50Hz Filter Mode; incl. MEMS		53		Hz

4339

**PSI5 types:**

ID	parameter / condition	min	typ	max	unit
4008	Nominal Cutoff Frequency SMA750/752/780/782/765  860Hz Filter Mode; incl. MEMS		849		Hz
4347	Nominal Cutoff Frequency SMA755/757/790/792 860Hz Filter Mode; incl. MEMS		855		Hz
4346	Nominal Cutoff Frequency SMA751/753/781/783 X-channel 860Hz Filter Mode; incl. MEMS		849		Hz
4345	Nominal Cutoff Frequency SMA751/753/781/783 Z-channel 860Hz Filter Mode; incl. MEMS		834		Hz
4342	Nominal Cutoff Frequency all PSI5 types with 120/240/480g range; SMA765 430Hz Filter Mode; incl. MEMS		429		Hz
4350	Nominal Cutoff Frequency SMA773/774-X 430Hz Filter Mode; incl. MEMS		423		Hz
5086	Nominal Cutoff Frequency SMA774-Z 430Hz Filter Mode; incl. MEMS		415		Hz
4341	Nominal Cutoff Frequency all PSI5 types; SMA765 215Hz Filter Mode; incl. MEMS		213		Hz

4351

For SMA773/774 (30/60g range) the use of the 860 Hz filter setting is not allowed.

**9.6.2 Resonance frequencies**

353

No common resonance frequency of package and MEMS (incl. soldering effects) up to 60 kHz

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<b>ID</b>	<b>parameter / condition</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>unit</b>
2309 not set	Natural Frequency CMA581R		8.9		kHz
5486 not set	Natural Frequency CMA582R-X		9.1		kHz
5487 not set	Natural Frequency CMA582R-Z		5.1		kHz
5488 not set	Natural Frequency CMA584R		18.3		kHz
5489 not set	Natural Frequency CMA588R		23.6		kHz
5490 not set	Natural Frequency CMA585R-X		18.3		kHz
5491 not set	Natural Frequency CMA585R-Z		10.3		kHz
2308 not set	Damping of MEMS CMA581R		1.8		
5492 not set	Damping of MEMS CMA582R-X		2.1		
5493 not set	Damping of MEMS CMA582R-Z		1.7		
5494 not set	Damping of MEMS CMA584R		1.7		
5495 not set	Damping of MEMS CMA588R		1.5		
5496 not set	Damping of MEMS CMA585R-X		1.7		
5497 not set	Damping of MEMS CMA585R-Z		1.3		

352

The MEMS-designs are overcritically damped. (Lehr-damping &gt; 1/SQRT(2))

<b>ID</b>	<b>parameter / condition</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>unit</b>
356	Frequency range without resonances of package or MEMS SMA760, SMA720-X	0		20	kHz
4084	Frequency range without resonances of package or MEMS SMA720-Z	0		17	kHz



ID	parameter / condition	min	typ	max	unit
4110	Frequency range without resonances of package or MEMS  PSI-types, SMA765	0		1.5	kHz

493

The specified limits for offset and noise are not exceeded, if a high frequent signal in the range of  $2\text{kHz} < f < 20\text{kHz}$  with an amplitude of 5g or lower is applied (e.g. vibration of the PCB). This is valid for X, Y and Z direction of the vibration and 430Hz filter setting.

*Comment: In the range below 2kHz the specified behaviour of the low pass filtering is also valid (already specified in the chapter "FIR-filter").*

### 9.6.3 Transfer Function

3515

The offset error for vibration requirements is specified in terms of an applied quasi-static sinusoidal stimulus in any direction. The stimulus has specified peak amplitudes in certain frequency ranges. It is a linear acceleration. If the stimulus is not exceeded, the offset error stays within specified limits.

The offset error refers to the delta between expect value (e.g. from spec or simple model) and real value.

The offset error and DLF include package effects.

ID	parameter / condition	min	typ	max	unit
3516	<p>The offset error of SMA760 and SMA720-X is smaller then <b>+/-0.3g</b> for the following combinations of frequency and acceleration amplitude:</p> <ul style="list-style-type: none"> <li>• 0 - 1kHz: 80g</li> <li>• 1 - 3kHz: 100g</li> <li>• 3 - 5kHz: 150g</li> <li>• 5 - 10kHz: 200g</li> <li>• 10 – 30kHz: 400g</li> <li>• 30 – 50kHz: 35g</li> <li>• 50 – 60kHz: 400g</li> <li>• &gt;60kHz: 1000g</li> </ul> <p>430Hz filter; 53Hz filter; 430Hz filter + 51Hz SW-filter; acceleration in X,Y,Z direction (worst-case)</p>				
3517	<p>The offset error of SMA720-Z is smaller then <b>+/-0.3g</b> for the following combinations of frequency and acceleration amplitude:</p> <ul style="list-style-type: none"> <li>• 0 - 1kHz: 65g</li> <li>• 1 - 2kHz: 75g</li> <li>• 2 - 3kHz: 100g</li> <li>• 3- 5kHz: 130g</li> <li>• 5 - 10kHz: 200g</li> <li>• 10 – 30kHz: 350g</li> <li>• 30 – 40 kHz: 150g</li> <li>• 40 – 70kHz: 4g</li> </ul>				

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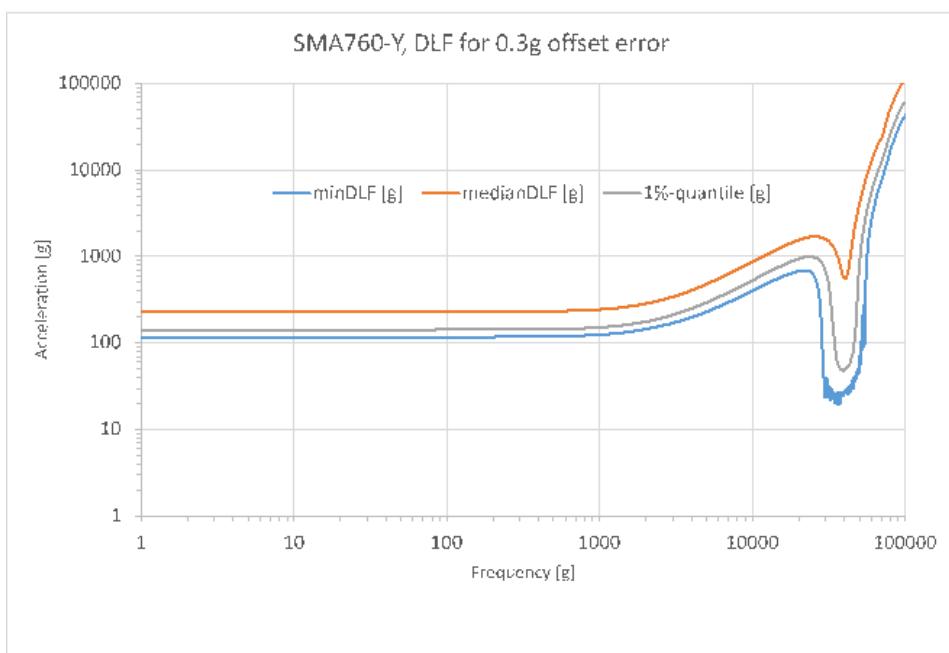
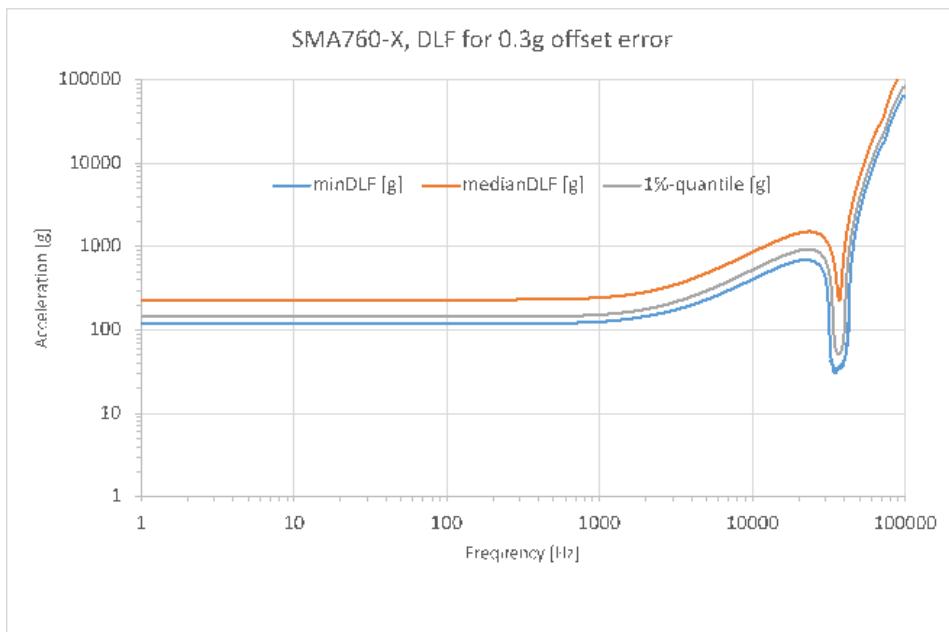
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ID	parameter / condition	min	typ	max	unit
	<ul style="list-style-type: none"><li>• 70 - 85kHz: 50g</li><li>• &gt;85kHz: 400g</li></ul> <p>53Hz filter and 430Hz-mode + 51Hz SW Filter; acceleration in X,Y,Z direction (worst-case)</p>				

1932

DLF (Dynamic Load Function) for SMA760 for offset error +/-0.3g.

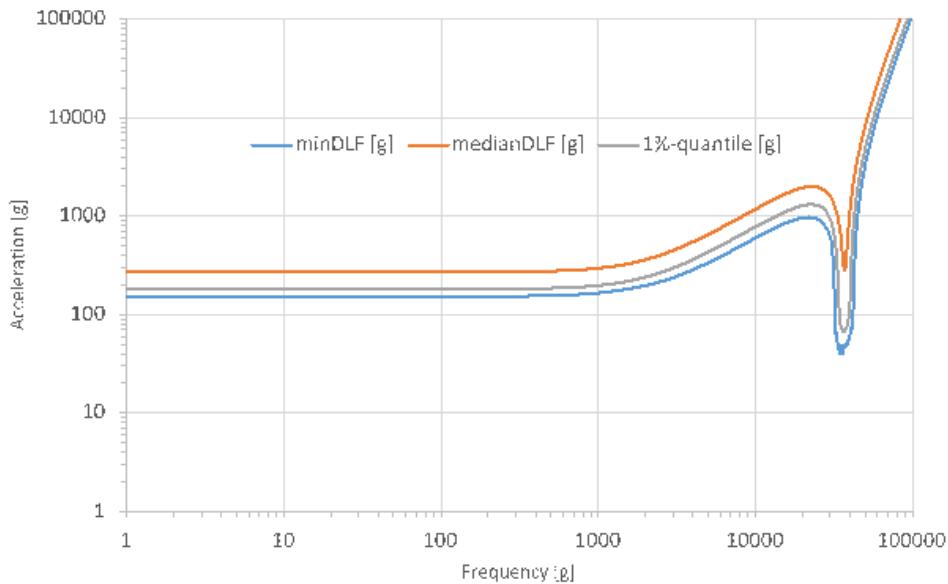


5475

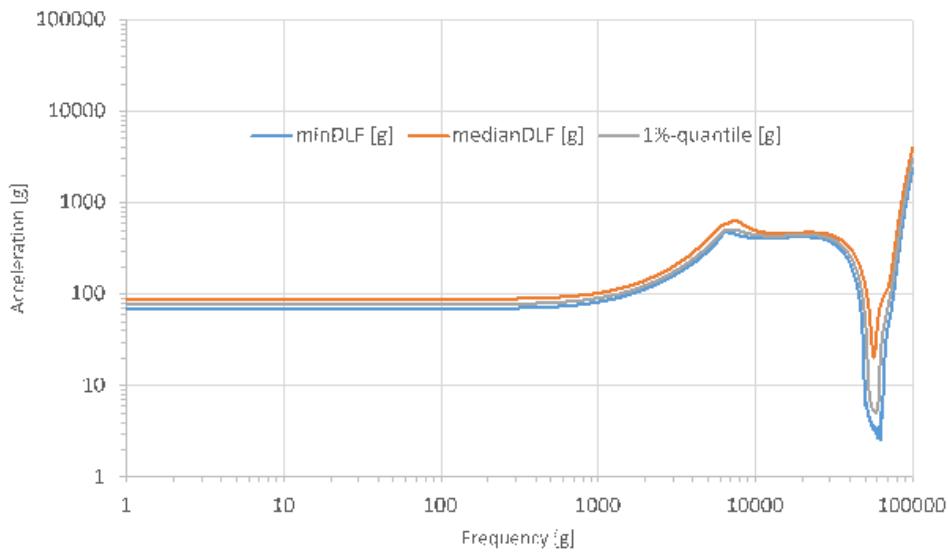
DLF (Dynamic Load Function) for SMA720 for offset error +/-0.3g.



SMA720-X, DLF for 0.3g offset error



SMA720-Z, DLF for 0.3g offset error

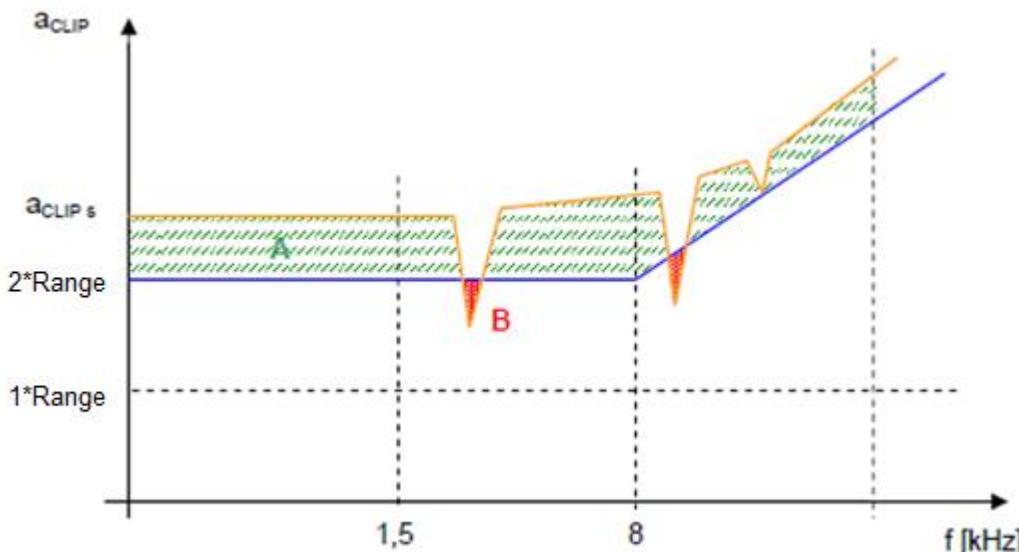


ID	parameter / condition	min	typ	max	unit
2306 not set	Dynamic clipping PSI5-Types; f<1.5kHz SMA765	2* Range			g
2307 not set	Dynamic clipping PSI5-Types + SMA765; 1.5kHz < f < 20kHz; (Integral below 2*Range) < (5% of Integral above 2 * Range)	1*Range			g



ID	parameter / condition	min	typ	max	unit
3910	Increase of dynamic clipping PSI5 types with 120/240/480g range  PSI5-Types + SMA765; f >8kHz	0.5			g/Hz
4352	Increase of dynamic clipping PSI5 types with 30/60g range  PSI5-Types; f >8kHz;	0.1			g/Hz

4015



ID	parameter / condition	min	typ	max	unit
1789	Overload without residual effect SPI-Types; Sensor in specification after shock	+1000			g
1790	Overload Recovery time SPI-Types (Definition of recovery time: Delay caused by dynamic clipping; Test method: 2ms half sine puls with amplitude of 350g); *1)			0.2	ms
1791	Overload Recovery time SPI-Types (Definition of recovery time: Delay caused by dynamic clipping; Test method: min. 1ms half sine puls with amplitude of 1000g); *1)			0.2	ms
1792	Overload Recovery time PSI5-Types (Definition of recovery time: Delay caused by dynamic clipping; Test method: min. 1ms half sine puls with amplitude of 1500g); *1)			0.2	ms
1793	Overload Recovery time			0.2	ms

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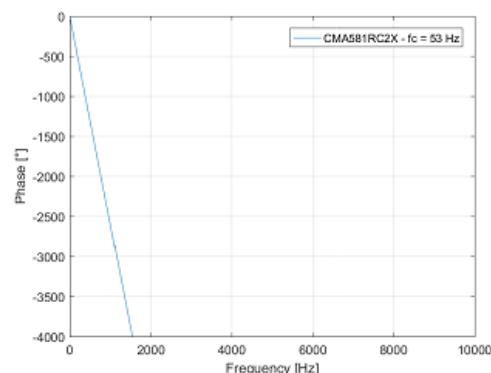
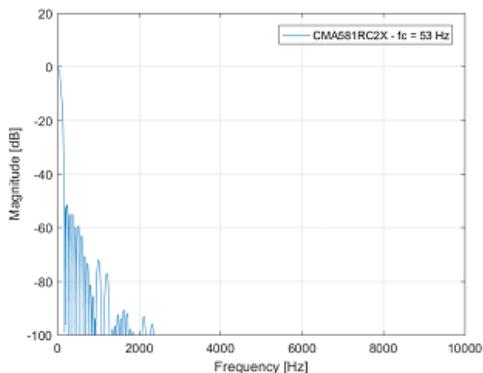
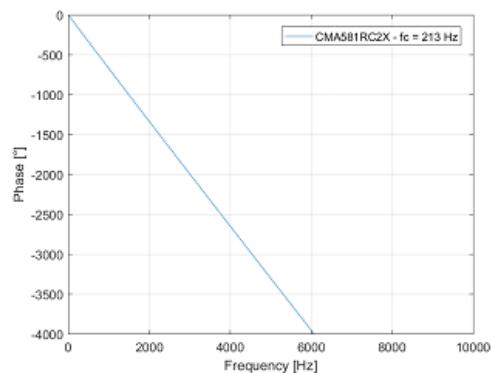
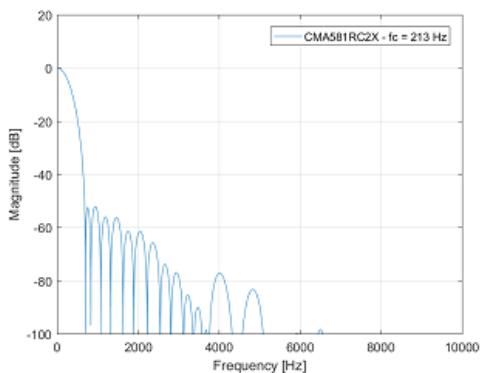
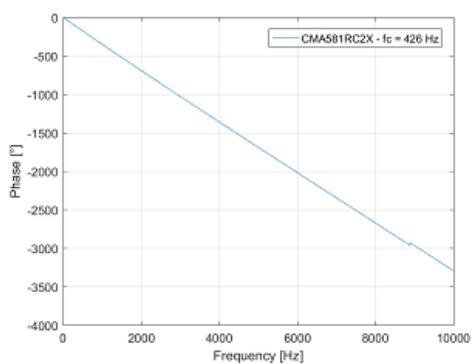
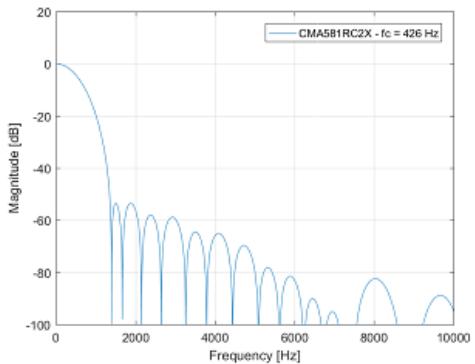
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ID	parameter / condition	min	typ	max	unit
	PSI5-Types (Definition of recovery time: Delay caused by dynamic clipping; Test method: min. 0.5ms half sine puls with amplitude of 2500g); *1)				

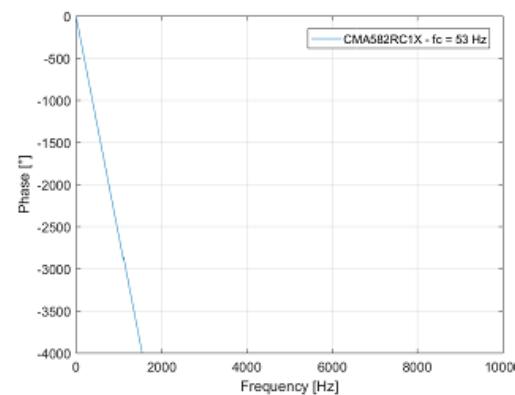
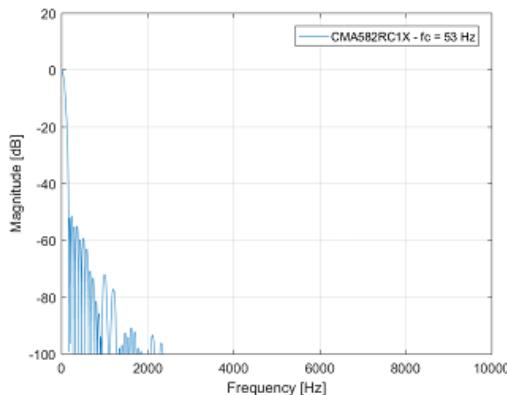
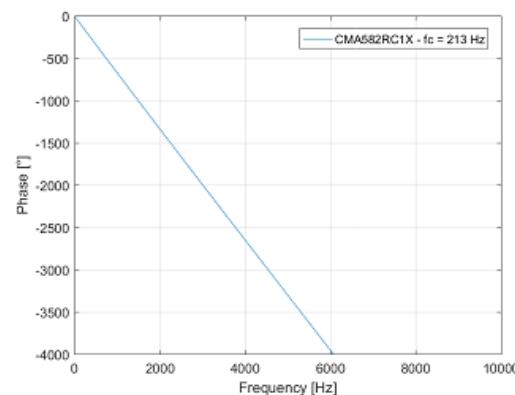
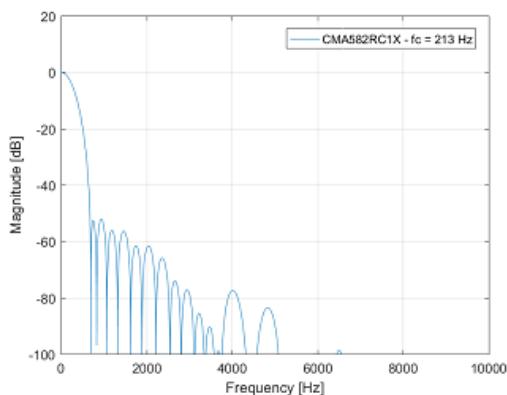
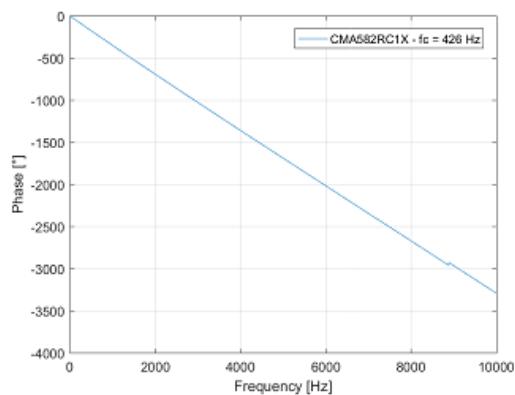
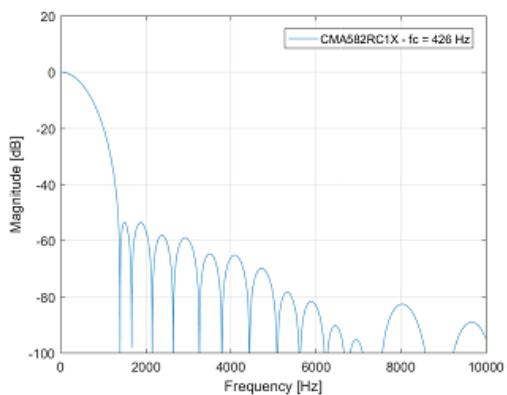
5530

Simulated typical transfer function of CMA581R incl. singal path (without Interpolator):



5531

Simulated typical transfer function of CMA582R-X incl. singal path (without Interpolator):

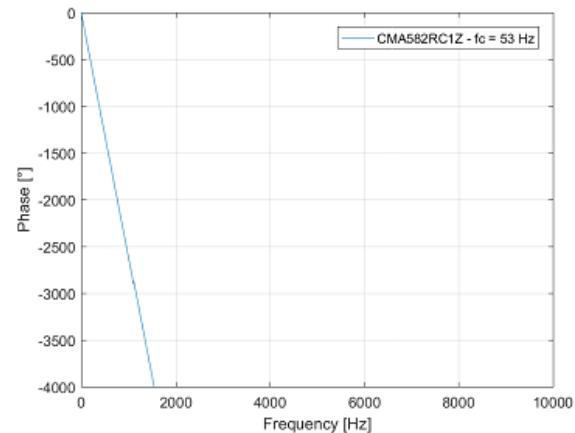
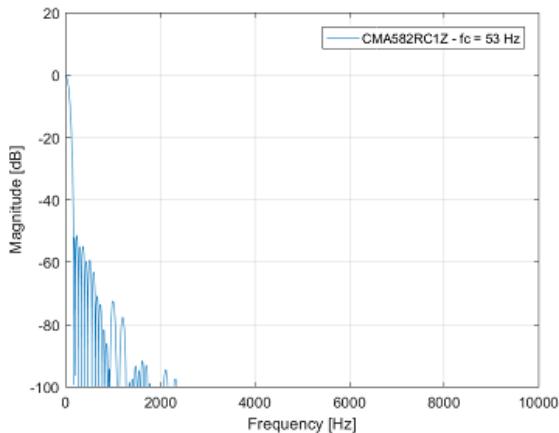
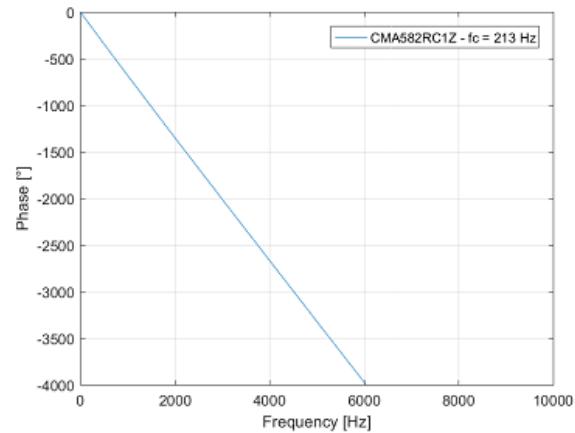
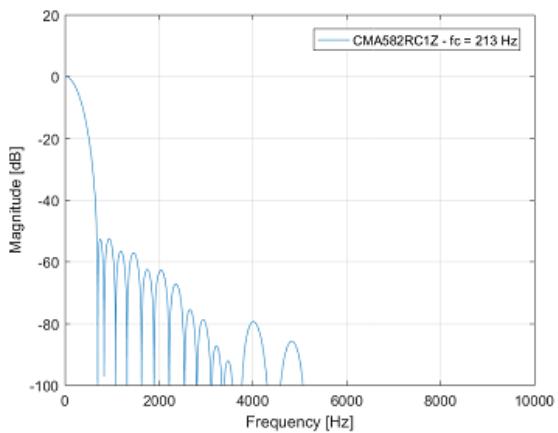
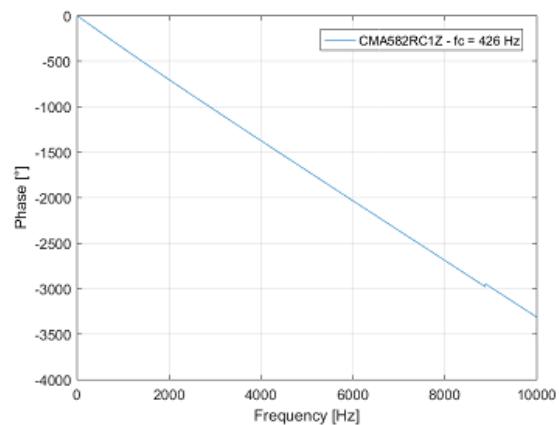
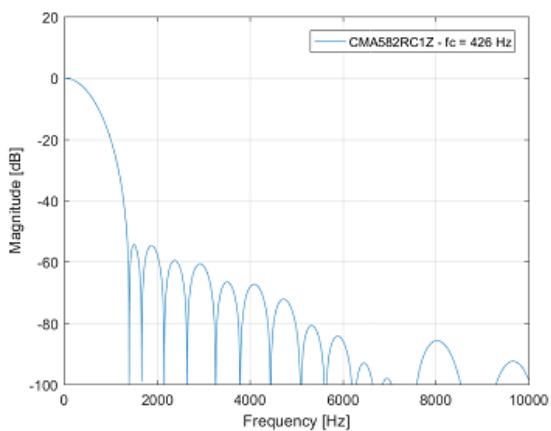


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## 10. Functional Safety

### 10.1 General Functional Safety

5423

The complete safety analysis results and Sensor safety concept are only valid when all safety relevant monitors are activated and evaluated.

ASIL\_D

The user is responsible for not using individual monitors and must evaluate this at system level.

#### 10.1.1 Scope

3315

The sensor operates exclusively in safe state within the safety goals. Safety goals are described in the following sections. Residual failure rates are evaluated in Safety Analysis.

ASIL\_D

3317

Single faults, that lead to minimum one violation of the safety targets are monitored either initially (during startup of the sensor) or periodically (during operation).

ASIL\_D

4544

Temperature profiles for safety analysis (internal customer):

ASIL\_D

Temperature [°C]	Operation time [h]	
	T-profile 105°C (ECU, PAS, RoSe)	T-profile 120°C (UFS)
120	0	150
115	0	1200
105	150	0
100	1350	0
80	2250	9750
60	3000	0
40	8250	0
25	0	3000
-40	0	900

5211

Fault Reaction Time (FRT) for detecting faults and activating corresponding failure reaction.

ASIL\_D

Exceptions:

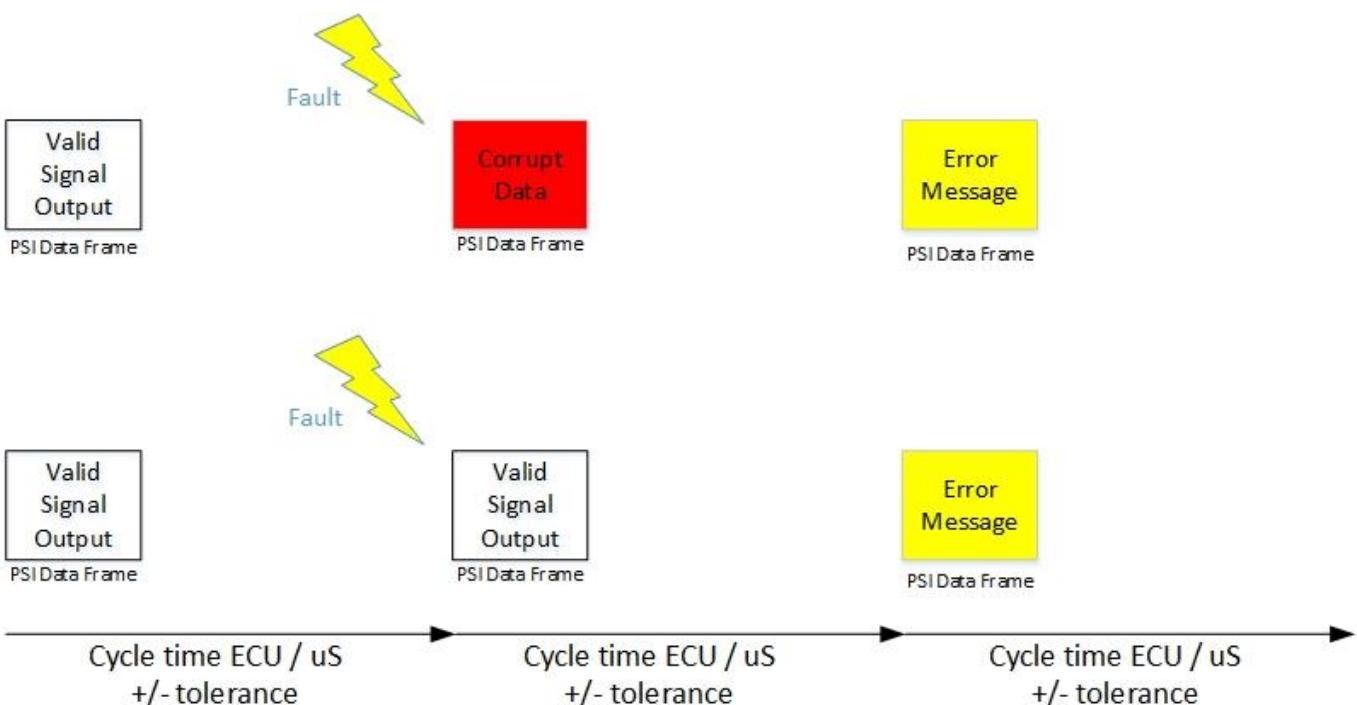
- Applies to all monitors, except the oscillator monitor
- In case of fault detected during or just before the transmission of current data frame, one frame with corrupt data is allowed, but next data frame must be the error message.

#### Unique aspect in PSI Mode:

For mode 1 operation (PSI5 with Sync pulse distance/cycle time >=500us) the following interpretation applies:

#### Example:

PSI5 Mode with 500us Sync pulse distance  
 $T_{FRT} = 2 * 500\text{us} = 1000\text{us}$



### 10.1.2 Required Initialisation during start up

5425 At least once at the end of the init phase, it must be verified that the sensor is working faultlessly and that the init phase has been successfully completed. ASIL\_D

Bosch SPI: GS Flag=0

Safe SPI: NRO FFlag=0

PSI: no Errorcode

#### 10.1.2.1 In SPI Mode

5438 In order to ensure a correct init phase, it must be checked for each transmitted command that the CRC is correct. ASIL\_D

Alternative :

Each write command of a register must be secured with a followed read command of the respective register

5258 **To be performed at system level during Startup** ASIL\_D

See details in chapter 5.6.5 and 5.7.5



What	Description	How	Limit assumption		Reference in PH
			low	high	
BITE	Besides BITE tests of acceleration channels (see section 2.2.2) must be initiated at start up and evaluated in order to check the functionality of the sensor element and the complete signal path.	Trigger and evaluate	SMA760: -10% SMA720: -12% SMA765: -30% +Application tolerances	SMA760: +10% SMA720: +12% SMA765: +30% +Application tolerances	9.5.7
C-Loss Monitoring	C-Loss Monitor must be triggered during init phase. If test is failed Sensor will go to reset state	Trigger C-Loss detection and evaluate Sensor state afterwards	Sensor goes not go to reset		10.5.4
Residual Offset after FOC	Either the ECU triggers the FOC in the sensor or the ECU performs the fast offset cancellation itself in the algo. In every case the residual offset after fast offset cancellation must be checked	Read and evaluate Sensor acc. data after FOC	Safety Limits + Application tolerances		9.5.4

### 10.1.2.2 in PSI Mode

5426

In order to ensure a correct init phase, it must be checked for each transmitted command that the CRC or Parity Bit is correct.

ASIL\_D

5259

#### To be performed at system level during Startup

See details in chapter 6.2.4

ASIL\_D

What	Description	How	Limit assumption	Reference in PH
Check Sensor Ready Message at the End of Init Phase 3	In order to ensure a correct init phase, the ECU has to check that the sensor send the "Sensor Ready" message at the End of init Phase 3	wait and evaluate Sensor Ready message. relevant code is +487 or 0xE7	received Sensor Ready Message	6.3.4.1
Residual Offset check after init phase	The sensor checks the residual offset itself. Limits are stored in OTP and selected by customer.	Read and evaluate Sensor acc. data after Init Phase	Safety Limits + Application tolerances	9.5.4

5260

Moreover, if a BITE-Error (BITE out of Limit) or Offset cancellation- Error (OC1 Monitor or OC2 Monitor only detected in one channel, it doesn't naturally mean that the other channel still works properly. As BITE and FOC are not activated repeatedly all the time, in this case, the sensor signal from both channels should be discarded due to safety reasons.

ASIL\_D

### 10.1.3 Required General Sensor Failure Monitoring in Run mode

5430

In order to ensure a correct working Sensor and a valid Signal, the ECU has to check following

ASIL\_D

#### 10.1.3.1 SPI Mode

5427

**The application must be able to recognize a failure of the sensor with the flags at any time.**

ASIL\_D

##### Bosch SPI:

GS flag have to be checked all the time in the system.

##### Safe SPI:



NRO flag and Status-Flag Bits have to be checked all the time in the system.

5428

**CRC**

ASIL\_D

In order to ensure a correct transmission / communication between system and sensor, the CRC of SPI communication at SO has to be checked all the time in the system.

5429

**Oscillator**

ASIL\_D

SPI OSC MONITOR +/-10% (Spec limits + assumption ECU Level) (see chapter 9.4)

5437

In case FOC and/or SOC/XSOC is deactivated, the assumption for Safety Concept is that a comparable Offset Cancellation on ECU Level is implemented.

ASIL\_D

5268

**FOC and SOC/XSOC in ECU**

ASIL\_D

If The offset cancellation is implemted in ECU following limits are required

- FOC and SOC/XSOC in ECU: it needs to be checked that the maximum Offset cancellation value is equal or smaller then the specified residual offset without FOC (see chapter 9.5.4). In addition an application specific marging can be applied (e.g. drive dynamic and mounting position)

-Only SOC/XSOC in ECU: it needs to be checked that the maximum slow Offset cancellation value is equal or smaller then the specified residual offset without SOC/XSOC (see chapter 9.5.4). In addition an application specific marging can be applied (e.g. drive dynamic and mounting position)

-only FOC in ECU

not allowed

### 10.1.3.2 PSI5 Mode

5261

**The application must be able to recognize a failure of the sensor with the flags at any time.**

ASIL\_D

-Errorcodes

-Parity Bit/CRC Error

-Manchester Code Error

In general, a Errorcode indicates that the acceleration signal is not valid.

5431

**CRC/Parity Bit**

ASIL\_D

In order to ensure a correct transmission/ communication between system and sensor, the CRC/Parity Bit of PSI5 communication has to be checked all the time in the system.

5424

In case FOC and/or SOC/XSOC is deactivated, the assumption for Safety Concept is that a comparable Offset Cancellation on ECU Level is implemented.

ASIL\_D

5432

**FOC and SOC/XSOC in ECU**

ASIL\_D

If The offset cancellation is implemted in ECU following limits are required

- FOC and SOC/XSOC in ECU: it needs to be checked that the maximum Offset cancellation value is equal or smaller then the specified residual offset without FOC (see chapter 9.5.4). In addition an application specific marging can be applied (e.g. drive dynamic and mounting position)

Only SOC/XSOC in ECU: it needs to be checked that the maximum slow Offset cancellation value is equal or smaller then the specified residual offset without SOC/XSOC (see chapter 9.5.4). In addition an application specific marging can be applied (e.g. drive dynamic and mounting position)

-only FOC in ECU

not allowed



### 10.1.4 Safe State

5257

The safe state is the state a sensor may go to, if any safety criterion is violated. There are three states possible. If technical possible, criterion a) should be used:

ASIL\_D

- a) SPI: status flag/Communication CRC Error
- b) PSI5: Errorcode/wrong checksum/Manchestercode for response
- c) no response / no communication

### 10.1.5 Fault Reaction Time

5253

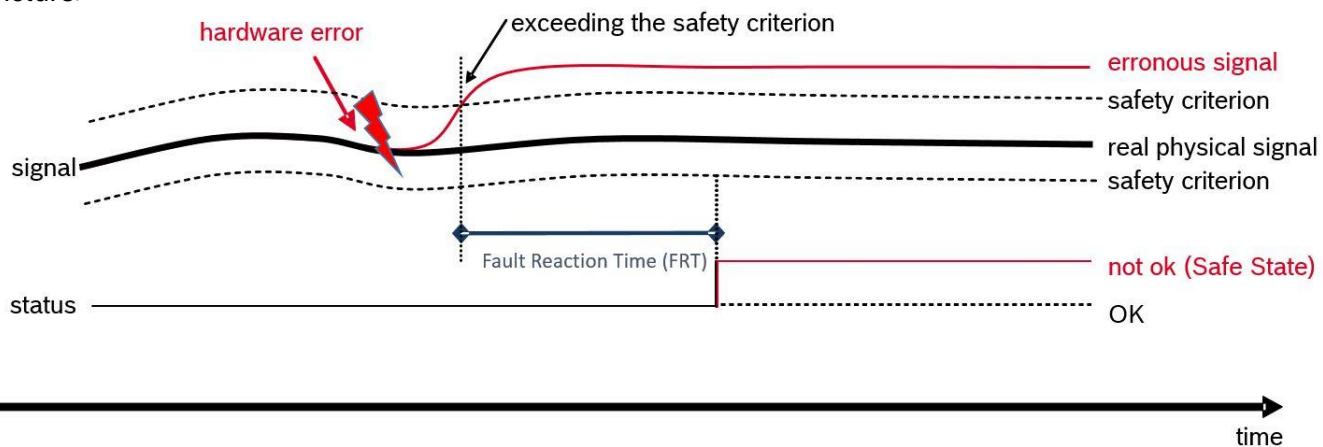
The target fault reaction time (FRT) is measured from the time, when any safety criterion is violated until the sensor is brought into any of its safe states

ASIL\_D

5256

<Picture>

ASIL\_D



## 10.2 Airbag ECU Application

### 10.2.1 General

1812

The SMA7 development process is according to ASIL-D.

---

The ASIL classification of the SMA7 requirements are defined by the ISO26262 DOORS-attribute. Thus the corresponding development is applied.

3726

The sensor is designed for application in homogenous or heterogeneous redundant systems (ASIL D).

4428

The safety specifications for the Airbag ECU application apply to the variants SMA760 (X and Y-Channel) and the X-channel of the SMA720.

ASIL\_D

### 10.2.2 Safety goals - Airbag ECU Application

3630

#### System Safety Goal ATOP01:

Avoid inadvertent activation of an occupant safety device in absence of a relevant crash condition

ID	parameter / condition	min	typ	max	unit
3321 ASIL_D	Safety Limit SMA760 SMA720 X-channel	-1		+1	g
3631 ASIL_D	<b>ATOP01.01:</b> During operation the sensor sends acceleration data (Ch 1) via SPI with a value over threshold without a physical stimulus and without entering a safe state.			10	FIT



ID	parameter / condition	min	typ	max	unit
	Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g				
3632 ASIL_D	Target for single point fault metric (ATOP01.01)   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g	90			%
3633 ASIL_D	Target for latent fault metric (ATOP01.01)   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g	60			%
3634 ASIL_D	Fault Reaction Time (FRT)(ATOP01.01)   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g			0.5	ms
3635 ASIL_D	<b>ATOP01.02:</b> During operation the sensor sends acceleration data (Ch 2) via SPI with a value over threshold without a physical stimulus and without entering a safe state.   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g			10	FIT
3636 ASIL_D	Target for single point fault metric (ATOP01.02)   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g	90			%
3637 ASIL_D	Target for latent fault metric (ATOP01.02)   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g	60			%
3638 ASIL_D	Fault Reaction Time (FRT) (ATOP01.02)   Physical stimulus   ≤ 1g;   Sensor output signal deviation to physical stimulus   ≥ 1g			0.5	ms
3639 ASIL_D	<b>ATOP01.03:</b> During operation the sensor sends acceleration data via SPI on both channels at the same time with values over threshold, with same signs without a corresponding physical stimulus and without entering a safe state.			10	FIT



ID	parameter / condition	min	typ	max	unit
	Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g				
3640 ASIL_D	Target for single point fault metric (ATOP01.03)   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g	90			%
3641 ASIL_D	Target for latent fault metric (ATOP01.03)   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g	60			%
3642 ASIL_D	Fault Reaction Time (FRT)(ATOP01.03)   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g			0.5	ms
3643 ASIL_D	<b>ATOP01.04:</b> During operation the sensor sends acceleration data via SPI on both channels at the same time with values over threshold, with opposite signs without a corresponding physical stimulus and without entering a safe state.   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g			10	FIT
3644 ASIL_D	Target for single point fault metric (ATOP01.04)   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g	90			%
3645 ASIL_D	Target for latent fault metric (ATOP01.04)   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g	60			%
3646 ASIL_D	Fault Reaction Time (FRT)(ATOP01.04)   Sensor output signal difference between channel 1 and 2   / SQRT(2) ≥ 1g			0.5	ms

3648

**System Safety Goal ATOP03:**

Avoid wrong deployment of occupant safety devices in case of a crash condition and no indication is given in advance

ID	parameter / condition	min	typ	max	unit
3649 ASIL_D	<b>ATOP03.01:</b> During operation the sensor sends acceleration data (Ch 1) via SPI with values lower than the values corresponding to the physical stimulus without entering a safe state.   Sensor output signal   ≤   0,93 * physical stimulus			10	FIT
3650 ASIL_D	Target for single point fault metric (ATOP03.01)   Sensor output signal   ≤   0,93 * physical stimulus	90			%



ID	parameter / condition	min	typ	max	unit
3651 ASIL_D	Target for latent fault metric (ATOP03.01)   Sensor output signal   ≤   0,93 * physical stimulus	60			%
3652 ASIL_D	Fault Reaction Time (FRT) (ATOP03.01) (Internal Customers)   Sensor output signal   ≤   0,93 * physical stimulus			1	h
5293 ASIL_D	Fault Reaction Time (FRT) (ATOP03.01) (External Customers)   Sensor output signal   ≤   0,93 * physical stimulus			0.5	ms
3653 ASIL_D	<b>ATOP03.02:</b>  During operation the sensor sends acceleration data (Ch 2) via SPI with values lower than the values corresponding to the physical stimulus without entering a safe state.   Sensor output signal   ≤   0,93 * physical stimulus			10	FIT
3654 ASIL_D	Target for single point fault metric (ATOP03.02)   Sensor output signal   ≤   0,93 * physical stimulus	90			%
3655 ASIL_D	Target for latent fault metric (ATOP03.02)   Sensor output signal   ≤   0,93 * physical stimulus	60			%
3656 ASIL_D	Fault Reaction Time (FRT) (ATOP03.02) (Internal Customers)   Sensor output signal   ≤   0,93 * physical stimulus			1	h
5295 ASIL_D	Fault Reaction Time (FRT) (ATOP03.02) (External Customers)   Sensor output signal   ≤   0,93 * physical stimulus			0.5	ms

## 10.3 Airbag Satellite Application

### 10.3.1 General Requirements

1815

The sensor is designed for application in homogenous or heterogeneous redundant systems (ASIL D).

4429

The safety specifications for the Airbag Satellite application apply to all PSI5 variants.

### 10.3.2 Safety goals - Airbag Satellite Application

3673

**System Safety Goal ATOP01:**



Avoid inadvertent activation of an occupant safety device in absence of a relevant crash condition

ID	parameter / condition	min	typ	max	unit
3729 ASIL_D	Safety Limit	-3		+3	g
3665 ASIL_D	<b>ATOP01.01</b> (PAS application with temperature profile 105°C):  During operation the sensor sends acceleration data (Ch 1) via PSI with a value over threshold without a physical stimulus and without entering a safe state.   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g			10	FIT
3666 ASIL_D	Target for single point fault metric (ATOP01.01)    Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g	90			%
3667 ASIL_D	Target for latent fault metric (ATOP01.01)    Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g	60			%
3668 ASIL_D	Fault Reaction Time (FRT) (ATOP01.01)    Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g			0.5	ms
4546 ASIL_D	<b>ATOP01.01</b> (UFS application with temperature profile 120°C):  During operation the sensor sends acceleration data (Ch 1) via PSI with a value over threshold without a physical stimulus and without entering a safe state.   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g			17.11	FIT
3669 ASIL_D	<b>ATOP01.02</b> (PAS application with temperature profile 105°C):  During operation the sensor sends acceleration data (Ch 2) via PSI with a value over threshold without a physical stimulus and without entering a safe state.   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g			10	FIT
4547 ASIL_D	<b>ATOP01.02</b> (UFS application with temperature profile 120°C):			10	FIT



ID	parameter / condition	min	typ	max	unit
	During operation the sensor sends acceleration data (Ch 2) via PSI with a value over threshold without a physical stimulus and without entering a safe state.   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g				
3670 ASIL_D	Target for single point fault metric (ATOP01.02)   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g	90			%
3671 ASIL_D	Target for latent fault metric (ATOP01.02)   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g	60			%
3672 ASIL_D	Fault Reaction Time (FRT) (ATOP01.02)   Physical stimulus   ≤ 3g;   Sensor output signal deviation to physical stimulus   ≥ 3g			0.5	ms

3674

**System Safety Goal ATOP03:**

Avoid wrong deployment of occupant safety devices in case of a crash condition and no indication is given in advance

ID	parameter / condition	min	typ	max	unit
3675 ASIL_D	<b>ATOP03.01:</b> During operation the sensor sends acceleration data (Ch 1) via PSI with values lower than the values corresponding to the physical stimulus without entering a safe state.   Sensor output signal   ≤   0,93 * physical stimulus			10	FIT
3676 ASIL_D	Target for single point fault metric (ATOP03.01)   Sensor output signal   ≤   0,93 * physical stimulus	90			%
3677 ASIL_D	Target for latent fault metric (ATOP03.01)   Sensor output signal   ≤   0,93 * physical stimulus	60			%
3678 ASIL_D	Fault Reaction Time (FRT) (ATOP03.01) (Internal Customers)   Sensor output signal   ≤   0,93 * physical stimulus			1	h
5296 ASIL_D	Fault Reaction Time (FRT) (ATOP03.01) (External Customers)			0.5	ms



ID	parameter / condition	min	typ	max	unit
	Sensor output signal   ≤   0,93 * physical stimulus				
3679 ASIL_D	<b>ATOP03.02:</b>  During operation the sensor sends acceleration data (Ch 2) via PSI with values lower than the values corresponding to the physical stimulus without entering a safe state.   Sensor output signal   ≤   0,93 * physical stimulus			10	
3680 ASIL_D	Target for single point fault metric (ATOP03.02)    Sensor output signal   ≤   0,93 * physical stimulus	90			%
3681 ASIL_D	Target for latent fault metric (ATOP03.02)    Sensor output signal   ≤   0,93 * physical stimulus	60			%
3682 ASIL_D	Fault Reaction Time (FRT) (ATOP03.02)  (Internal Customers)   Sensor output signal   ≤   0,93 * physical stimulus			1	h
5297 ASIL_D	Fault Reaction Time (FRT) (ATOP03.02)  (External Customers)   Sensor output signal   ≤   0,93 * physical stimulus			0.5	ms

## 10.4 RoSe Plausibility Check

### 10.4.1 General

1817

The sensor is designed for application in homogenous or heterogeneous redundant systems (ASIL D).

4430

The safety specifications for the RoSe plausibility application apply to both channels of the SMA720 and SMA760.

### 10.4.2 Safety goals - RoSe Plausibility Check

ID	parameter / condition	min	typ	max	unit
3659 ASIL_D	<b>ATOP01 (RoSe):</b>  During operation, the sensor sends acceleration data via SPI with values <b>higher</b> than the values corresponding to the physical stimulus without entering a safe state.   Sensor output signal deviation to physical stimulus   ≥ 0.4g			10	FIT
3319 ASIL_D	Safety Limit	-0.4		+0.4	g



ID	parameter / condition	min	typ	max	unit
	SMA720/760; 430Hz filter and 430Hz-Mode + 51Hz SW-Filter *)				
3898 ASIL_D	Offset Jump	-0.4		+0.4	g
3899 ASIL_D	Offset Drift total offset within FRT	-0.4		+0.4	g
3900 ASIL_D	Sensitivity error	-7		+7	%
3901 ASIL_D	Signal delay ( $f_{3\text{DB}}$ ) 430Hz filter			1.21	ms
5200 ASIL_D	Signal delay ( $f_{3\text{DB}}$ ) 53Hz filter			9	ms
3902 ASIL_D	Signal freeze	-0.4		+0.4	g
3903 ASIL_D	Signal noise (p2p)	-0.6		+0.6	g
3904 ASIL_D	Signal deviation (EMC) Peak value	-0.4375		+0.4375	g

3322

\*)

51 Hz SW-Filter;

MATLAB implementation:

 $a = [1, -25/32]; b=[7/32, 0]; %51Hz filter$ 

temp = filter(b, a, rawdata);

output = filter(b, a, temp);

ID	parameter / condition	min	typ	max	unit
3660 ASIL_D	Target for single point fault metric (ATOP01 RoSe)    Sensor output signal deviation to physical stimulus   $\geq 0.4\text{g}$	90			%
3661 ASIL_D	Target for latent fault metric (ATOP01 RoSe)    Sensor output signal deviation to physical stimulus   $\geq 0.4\text{g}$	60			%
3662 ASIL_D	Fault Reaction Time (FRT) (ATOP01 RoSe)    Sensor output signal deviation to physical stimulus   $\geq 0.4\text{g}$			50	ms
4082 ASIL_D	<b>ATOP03 (RoSe):</b>  During operation, the sensor sends acceleration data via SPI with values <b>lower</b> than the values corresponding to the physical stimulus without entering a safe state.			10	FIT
4137 ASIL_D	Safety Limit  SMA720/760	-0.1		+0.1	g
4139 ASIL_D	Offset Jump	-0.1		+0.1	g



ID	parameter / condition	min	typ	max	unit
4140 ASIL_D	Offset Drift total offset within FRT	-0.1		+0.1	g
4141 ASIL_D	Sensitivity error z channel	-7		+7	%
4157 ASIL_D	Sensitivity error x or y channel	-5		+5	%
4142 ASIL_D	Signal delay ( $f_{3\text{DB}}$ ) 430Hz filter			1.21	ms
5201 ASIL_D	Signal delay ( $f_{3\text{DB}}$ ) 53Hz filter			9	ms
4143 ASIL_D	Signal freeze	-0.1		+0.1	g
4144 ASIL_D	Signal noise (p2p) 430Hz filter	-0.4		+0.4	g
4145 ASIL_D	Signal deviation (EMC) Peak value	-0.4375		+0.4375	g
4146 ASIL_D	Target for single point fault metric (ATOP03 RoSe)    Sensor output signal deviation to physical stimulus   $\geq 0.1\text{g}$	90			%
4147 ASIL_D	Target for latent fault metric (ATOP03 RoSe)    Sensor output signal deviation to physical stimulus   $\geq 0.1\text{g}$	60			%
4148 ASIL_D	Fault Reaction Time (FRT) (ATOP03 RoSe)    Sensor output signal deviation to physical stimulus   $\geq 0.1\text{g}$			1	h

## 10.5 Safety Concept and Monitors

### 10.5.1 External Voltage monitoring

422

#### Low voltage behavior (VDD/VDDI):

ASIL\_D

Sensor is always in safe state: Either working fully in spec ( $U \geq Vdd_{\text{min}}$  resp.  $U \geq vdd_{\text{min}}$ ) or "no communication" or "Failure flag" ( $U < Vdd_{\text{min}}$  resp.  $U < vdd_{\text{min}}$ ). No gray zone allowed.

2878

#### High voltage behavior (VDDI):

ASIL\_D

Sensor is always in safe state: Either working fully in spec ( $U \leq Vdd_{\text{max}}$ ) or "no communication" or "Failure flag" ( $U > Vdd_{\text{max}}$ ). No gray zone allowed. For voltages above maximum ratings, sensor may be damaged.

4431

#### VDD low voltage detection:

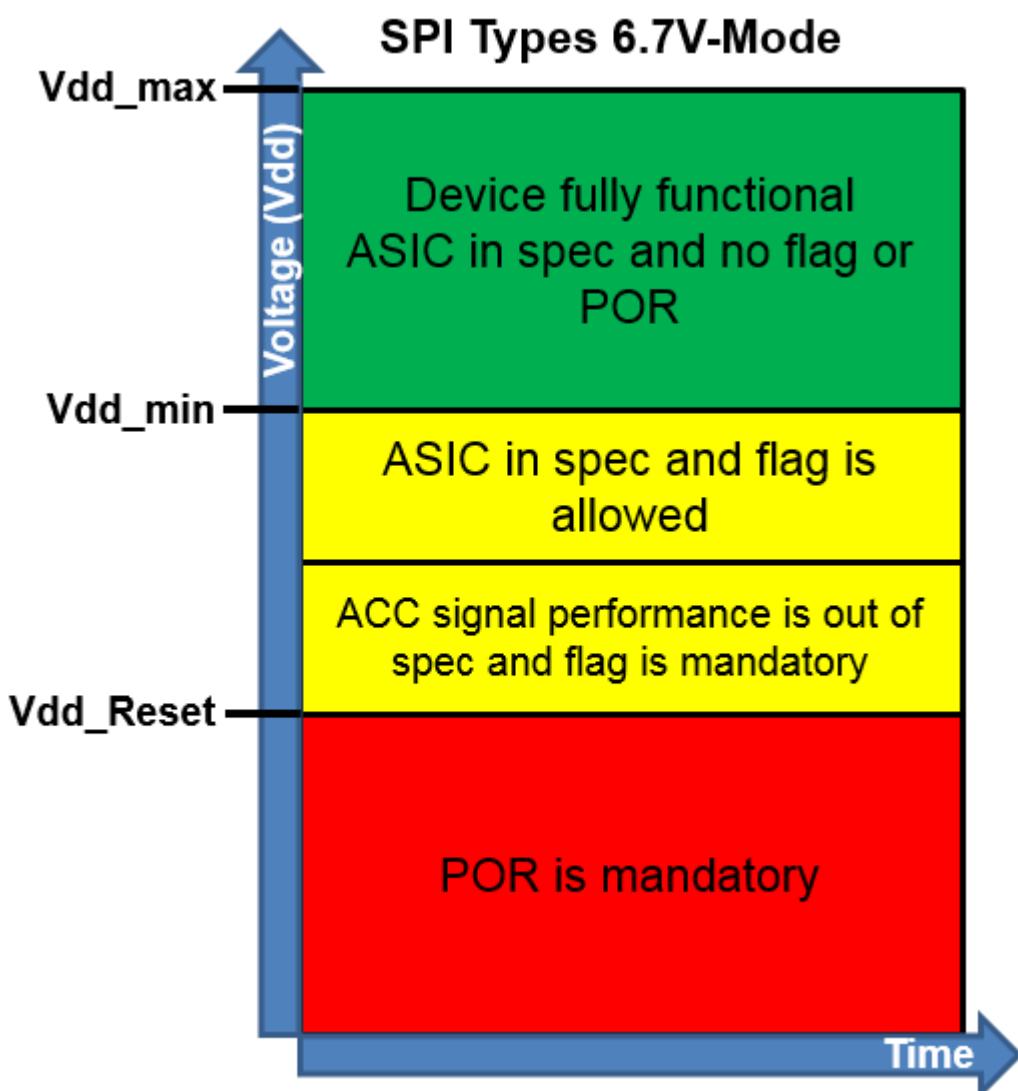
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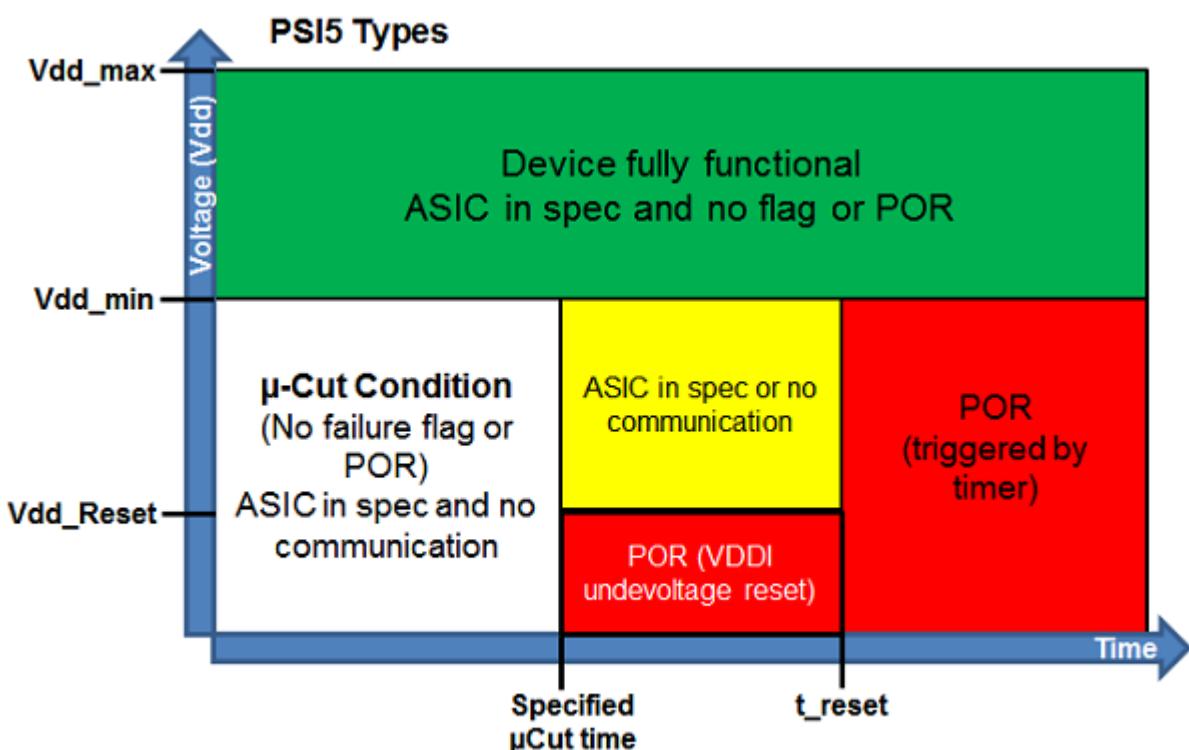


ID	parameter / condition	min	typ	max	unit
2879 ASIL_D	<p>Low Voltage Detection Threshold (PSI mode and 6.7 V SPI mode)</p> <p><i>(Below this threshold a flag will be triggered in SPI mode and communication will be disabled in PSI5 mode. Additionally in PSI5 a reset of the digital logic is triggered after the below specified t_reset)</i></p> <p>Vdd_min</p>	4.33	4.424	4.5	V
4079 ASIL_D	<p>Time during which the supply voltage at VDD is below Vdd_reset to initiate a reset.</p> <p><i>This means, that the undervoltage monitor triggers a reset of the digital logic after this time, if an undervoltage is detected. Anyway a complete loss of supply voltage will much earlier lead to a power-on reset (see description of <math>\mu</math>-Cut feature).</i></p> <p>t_reset</p> <p>PSI-mode</p>	3		5	ms
4842 ---	<p>VDD reset voltage</p> <p>(at this voltage the VDDI_reset threshold is reached at VDDI. This leads to an immediate power-on reset)</p> <p>VDD_reset;</p> <p>SPI 6.7V and PSI mode</p>	2.5		4.5	V

427 Low Voltage detection Scheme 6.7V-SPI-Mode:

ASIL\_D





4432

## VDDI low voltage- / high voltage detection:

ID	parameter / condition	min	typ	max	unit
2880 ASIL_D	Low Voltage Detection Threshold (all modes) Vddi_min	3.0	3.076	3.13	V
425 ASIL_D	Under Voltage Reset Threshold (all modes) Vddi_Reset	2.5	2.71	3.05	V
5522 ---	Hysteresis of VDDI under voltage reset		70		mV
4080 ASIL_D	Time supply voltage at VDDI is below Vddi_Reset to initiate a reset.  3.3V SPI-mode		1	5000	µs
2883 ASIL_D	High Voltage Detection Threshold (SPI 3.3V mode) Vddi_max	3.47	3.54	3.6	V

4433

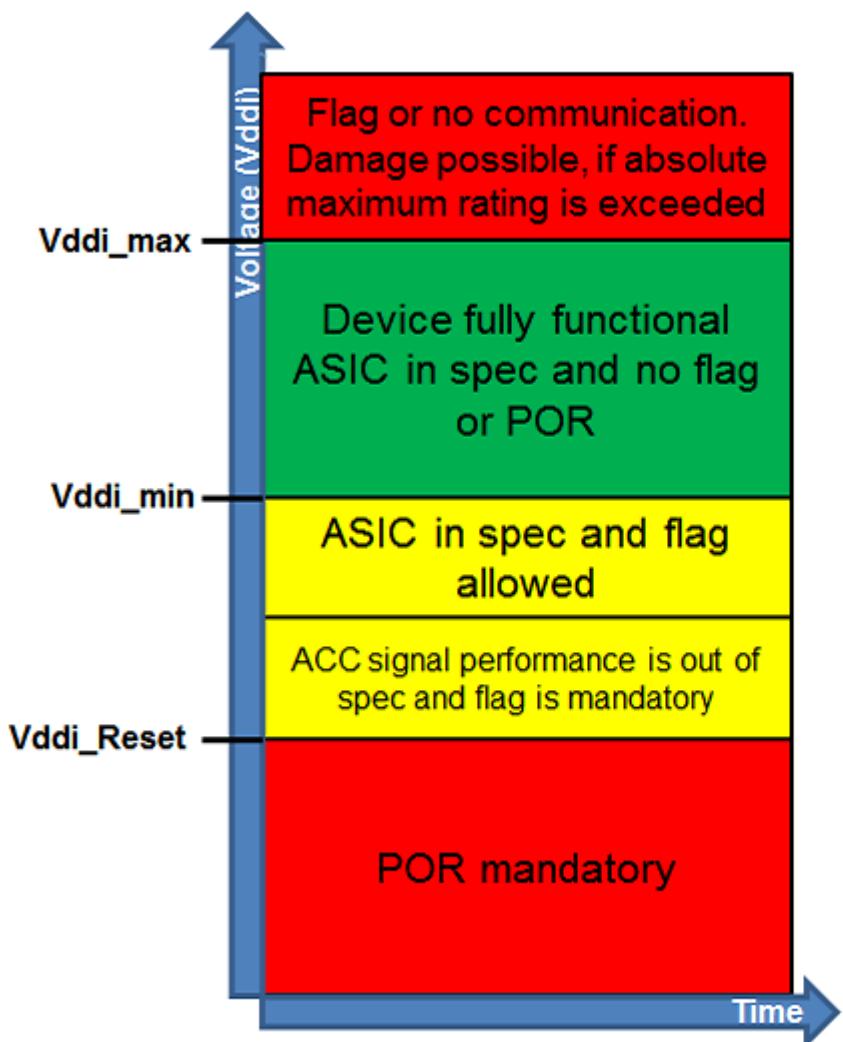
## Behavior in case of VDDI high voltage detection:

- PSI-mode: no communication (until reset)
- Bosch-SPI (inframe): no communication, SO in tristate (until soft- or hard reset)
- Open-SPI (off frame): error flag is set

426

## VDDI Voltage detection Scheme:

ASIL\_D



### 10.5.2 Internal Voltage Monitoring

ID	parameter / condition	min	typ	max	unit
3821 ASIL_D	AVDD low voltage detection leads to undervoltage flag over PSI or SPI interface, respectively. AVDD low	1.520	1.553	1.59	V
3822 ASIL_D	AVDD high voltage detection leads to no communication over PSI or SPI interface, respectively. AVDD high	1.59	1.640	1.675	V
3823 ASIL_D	DVDD Power-On-Reset leads to reset over PSI or SPI interface, respectively. DVDD low	1.330	1.367	1.465	V
3824 ASIL_D	DVDD high voltage detection leads to reset over PSI or SPI interface, respectively. DVDD high	1.570	1.61	1.65	V



### 10.5.3 Band Gap Monitoring

458

The ASIC uses two independent voltage (Band Gap) references. One as reference for voltage regulators and one as reference for voltage monitors.

ASIL\_D

If one of the bandgaps is generating a wrong output this will change the voltage levels of the regulators or the detection threshold of the monitors. This ensures, that a defect of one bandgap leads to an over- or undervoltage error.

### 10.5.4 C-loss detection

463

A start-up check of capacitor at VDDI is implemented. The monitor checks, if a capacitor is connected or not. For this purpose the supply from VDD to VDDI is shortly disconnected. If there is no capacitor connected, the voltage at VDDI will drop rapidly, which is detected by the ASIC. This monitor is working only if the sensor is supplied over VDD (PSI-Mode or SPI 6.7V Mode).

ASIL\_D

ID	parameter / condition	min	typ	max	unit
5202 ---	Detection threshold (value of C_VDDI)	28	62	135	nF

465

466

467

ID	parameter / condition	min	typ	max	unit
3843 ASIL_D	Offset after C-loss  SMA760/720  SMA773/774	-0.2	0	+0.2	g
3844 ASIL_D	Offset after C-loss  SMA780/781/782/783/750/751/752/753	-0.8	0	+0.8	g
3845 ASIL_D	Offset after C-loss  SMA790/792/755/757	-1.6	0	+1.6	g

2896

In case of a C-loss during run time the oscillator frequency is within the specification.

ASIL\_D

### 10.5.5 Oscillator Monitoring

#### 10.5.5.1 SPI mode

469

ASIC provides a 16bit wrap around clock counter, that can be read out via SPI. Based on the counter value the frequency of the sensor oscillator can be calculated by the ECU. (The frequency is not monitored internally by the sensor).

ASIL\_D

ID	parameter / condition	min	typ	max	unit
473 ASIL_D	Clock counter update rate  SPI-Types	2.137	2.25	2.363	MHz

#### 10.5.5.2 PSI mode (optional mechanism - not part of safety Concept)

4788

In PSI mode a monitor for the internal oscillator frequency is available. This monitor can be activated by the OTP bit MOTP\_PAS\_CONFIG\_6.MOTP\_OSC\_MON\_EN by the customer.



4789 If oscillator monitoring is enabled the blanking time feature is enabled automatically. (This means also, that it requires correct programming of the ECU cycle time in MOTP\_PAS\_CONFIG\_4.MOTP\_PSI\_BLANK\_TIME).

4790 The monitor detects failures of the internal sensor clock by evaluating the sync pulse distance. I.e. it compares the frequency of the internal clock vs. the frequency of the ECU clock, which generates the sync pulses.

4791 The first valid sync pulse detected starts a monitor cycle.

4792 A monitor cycle is defined by 4 timing windows:

1. blanking window:

Sync pulses within this window are considered to be implausible.

The blanking window corresponds to the blanking time ( $t_{blank}$ , described in PSI Interface chapter). This is a blanking time where no sync pulses are accepted and evaluated.

4793 2. lower and higher tolerance oscillator monitor window:

Sync pulses within this window are still within a plausible range, but outside of the specified tolerances of internal and ECU clock. Therefore this indicates a malfunction of the internal oscillator.

Lower monitor window spans from end of blanking window ( $t_{sync\_acc\_min}$ ) up to beginning of acceptance window ( $t_{sync\_mon\_min}^{(low)}$ ). Higher monitor window spans from end of acceptance window ( $t_{sync\_mon\_min}^{(high)}$ ) to  $t_{sync\_acc\_max}$ .

If a sync pulse is detected within this windows:

- the sync pulse is accepted
- an error counter is incremented (stepsize = MOTP\_PAS\_CONFIG\_7.MOTP\_OSC\_MON\_ERR\_CNT\_UP)
- the monitor cycle is restarted

4794 3. Acceptance window

If a sync pulse is within this window, it is within the spec of the internal and ECU clock plus a margin of 2%.

The acceptance window spans between the two monitor windows (between  $t_{sync\_mon\_min}^{(low/high)}$ ).

If a sync pulse is detected within this window:

- the sync pulse is accepted
- the error counter is decremented or reset, depending on the setting of MOTP\_PAS\_CONFIG\_2.MOTP\_OSC\_MON\_ERR\_CNT\_RESET and MOTP\_PAS\_CONFIG\_7.MOTP\_OSC\_MON\_ERR\_CNT\_DOWN
- the monitor cycle is restarted

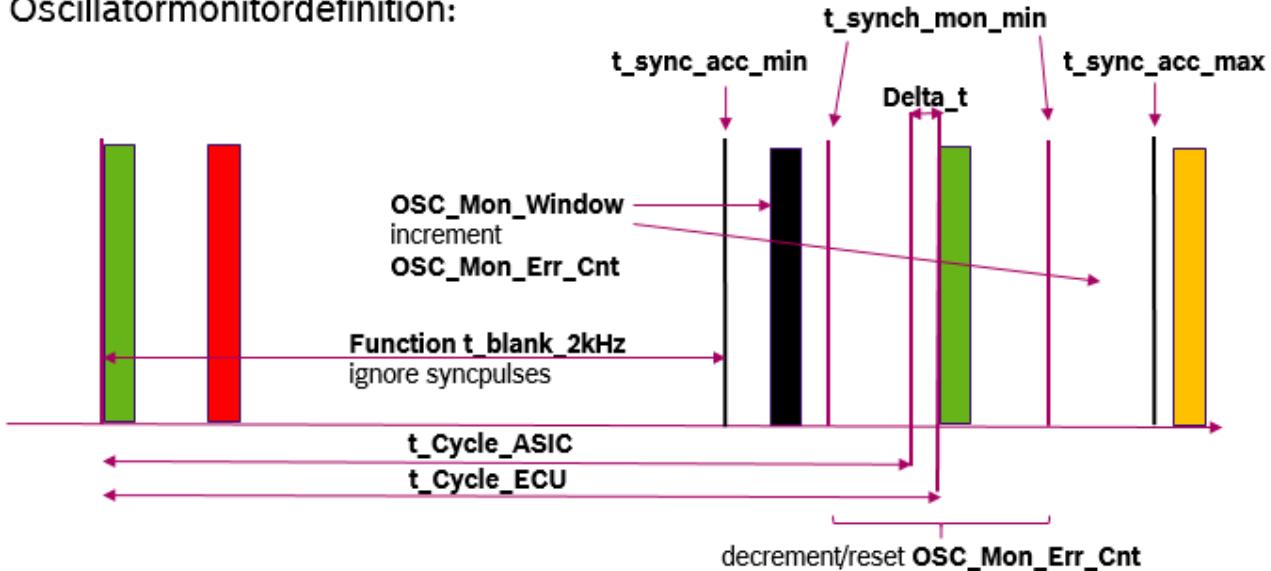
4795 If all time windows are past without detection of any sync pulse, the error counter is not incremented or decremented. Then the next sync pulse is treated as valid one and a new monitor cycle is restarted.

4796



# Oscillatormonitor

## ► Oscillatormonitordefinition:



- Green = Valid sync pulse, timing in spec
- Red = Syncpulse in blankout time
- Black = Syncpulse in monitor detection window
- Yellow = Syncpulse after **t\_sync\_acc\_max**

4800

The oscillator monitor error flag is set permanently, if the configured error counter threshold (OSC\_Mon\_Error\_Cnt\_thres) is reached. The counter threshold is calculated from the configured qualification time, step size of counter increment (OSC\_Mon\_Error\_Cnt\_up) and ECU cycle time:  $OSC\_Mon\_Err\_Cnt\_thres=OSC\_Mon\_Err\_Cnt\_Up * qual\_time / cycle\_time$

4801

This means, that the qualification time of the error is independent from the cycle time and chosen increment/decrement step size. The different settings for increment/decrement step size can be used to adjust the sensitivity of the monitor by choosing different step sizes for increase and decrease of the counter values.

4797

The following parameters of the monitor can be configured:

4798

Width of the acceptance window (**t\_sync\_mon\_min**) relative to ECU cycle time (250µs or 500µs):

Configured in MOTP\_PAS\_CONFIG\_6.MOTP\_OSC\_MON\_SYNC\_MON\_MIN

MOTP_OSC_MON_SYNC_MON_MIN	<b>t_sync_mon_min</b>
0b0	+/-7%
0b1	+/-8%

It is recommended to set this value to 8% (5% sensor clock tolerance + 1% ECU clock tolerance + 2% margin)

4799

Earliest and latest time to consider a sync pulse as valid (**t\_sync\_acc\_min/t\_sync\_acc\_max**):

The time is set relative to the chosen ECU cycle time. It is configured in MOTP\_PAS\_CONFIG\_7.MOTP\_OSC\_MON\_ACC\_MIN and MOTP\_PAS\_CONFIG\_7.MOTP\_OSC\_MON\_ACC\_MAX.

MOTP_OSC_MON_ACC_MIN/MAX	<b>t_sync_acc_min</b>	<b>t_sync_acc_max</b>
0b00	-8%	+8%
0b01	-9%	+9%
0b10	-10%	+10%
0b11	-12%	+12%



4802

Qualification time:

If the sync pulse are permanently within the monitor window, the error flag is raised after this time. It is configured in MOTP\_PAS\_CONFIG\_5.MOTP\_OSC\_MON\_ERR\_CNT\_LIMIT

MOTP_OSC_MON_ERR_CNT_LIMIT	Qualification time [s]
0b000	0.125
0b001	0.25
0b010	0.5
0b011	1
0b100	2
0b101	4
0b110	8
0b111	16

4803

Increment/decrement step size of Error counter:

Determines the step size for an increase of the error counter, if the sync pulse is within the monitor window. Respectively the decrement of the error counter, if the syncpulse is within the acceptance window.

This is configured in MOTP\_PAS\_CONFIG\_7. MOTP\_OSC\_MON\_ERR\_CNT\_UP and MOTP\_OSC\_MON\_ERR\_CNT\_DOWN

MOTP_OSC_MON_ERR_CNT_UP/DOWN	Increment step size	Decrement step size
0b00	+1	-1
0b01	+2	-2
0b10	+4	-4
0b11	+8	-8

4804

Counter reset behaviour:

Defines, if the error counter is decremented by MOTP\_OSC\_MON\_ERR\_CNT\_DOWN or if it is reset to "0", if a sync pulse within the acceptance window is detected. It is configured in MOTP\_PAS\_CONFIG\_2.MOTP\_OSC\_MON\_ERR\_CNT\_RESET

MOTP_OSC_MON_ERR_CNT_RESET	
0b00	Decrement counter
0b01	Reset counter to "0"

## 10.5.6 SPI Multiplexer Monitor

480

A swapping of channels - e.g. by single faults (Einzelfehler) - is avoided. Channel ID 1/2 is always sent in combination with sensor Data channel 1/2.

ASIL\_D

481

CRC creation is done before "multiplexing" of Bits.

ASIL\_D

5174

This design measures assure, that it can be detected, if data of the wrong channel is send due to a single fault in the channel multiplexer. In this case CRC and/or Channel ID would be wrong.

---

## 10.5.7 GND Loss Monitoring

3742

To assure safe pinning the sensor includes a GND loss monitor. The monitor detects an open of the GND pin and an open of the bond wires between ASIC and MEMS ground.

ASIL\_D

4810

The two cases are mapped on different bits in CFG\_MONITOR\_FLAG\_2. But in PSI mode and SafeSPI both cases are combined in one error code (PSI error code or SF flag value).

---

4917

An open at the external GND pin may also lead to reset of the sensor. This is also a safe state. It depends on the detailed envirmental conditions (temperature, load capacities, supply voltage,...) and can vary from part to part, wether a a reset or a GND loss error is trigered by external GND open.

---



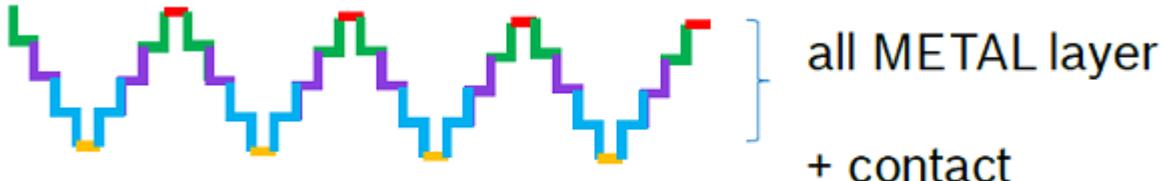
### 10.5.8 Die edge corrosion monitor (optional mechanism - not part of safety Concept)

4807

The die edge corrosion monitor is a protection feature to detect corrosion at the die edge of the ASIC. It consists of a resistor chain/ ring around the die edge and an evaluation circuit to detect the breaking of that chain. Each resistor unit in the chain consists of Top metal down to silicon connected through interconnects (vias and contacts). This unit is repeated to cover the entire periphery of the ASIC die. In case of corrosion, the chain breaks causing a discontinuity. This discontinuity can be detected by passing a current through this resistor chain and monitoring voltage across it.

5476

Schematic cross section:



4808

The monitor can be deactivated by the OTP bit MOTP\_SMA\_CONFIG\_1. MOTP\_DCM\_DIS or via SPI in register CFG\_CONFIG\_1

5436

For all SMA7 variants the monitor is enabled in OTP. Disabling the monitor by customer is not allowed, as this option is not released.

To enable deactivation, additional release and evaluation on system level would be required.

ID	parameter / condition	min	typ	max	unit
4809	Qualification time for break of the resistor chain  error flag is set, after a continuous open of the chain is detected for this time		180		µs



## 11. Handling and Storage

X-Ray inspection is possible with 2 gray for single shot and 6 gray for multiple shot (max. 3 times inspection).

Automatic X-ray inspection (AXI) with an electron acceleration voltage of  $\leq 160\text{ kV}$  is allowed during production without any reliability reduction. (For example, no reduction of the specified data retention performance of Non Volatile Memories NVMs).

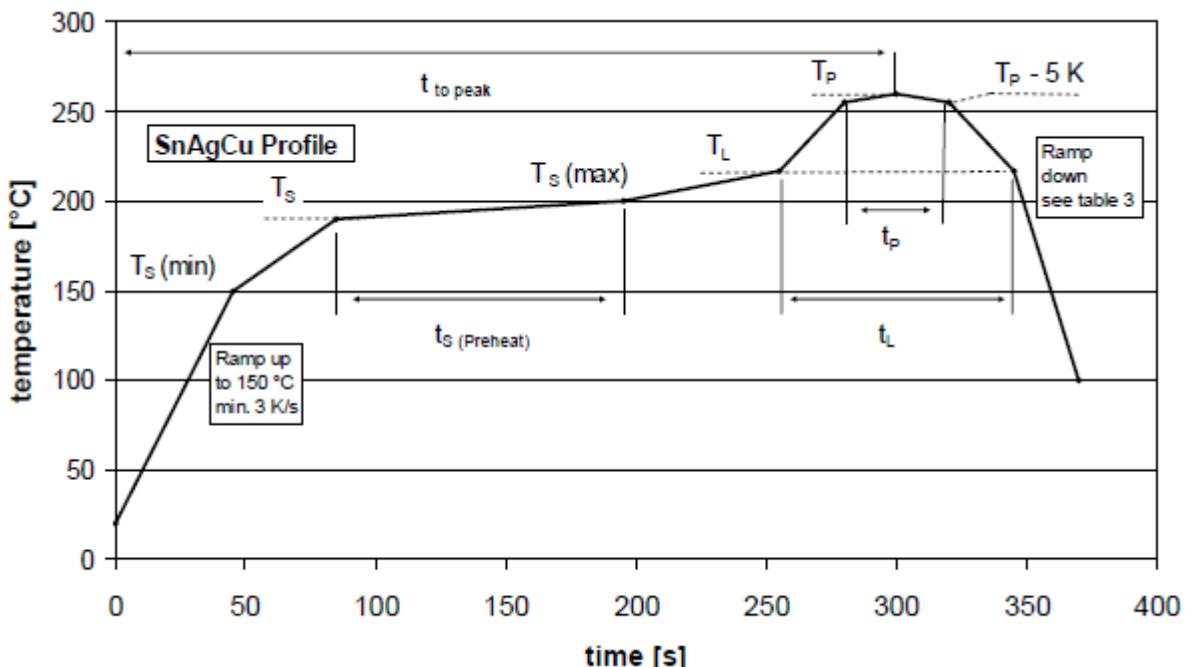
Automatic Optical inspection (AOI) is allowed during production without any reliability reduction.  
Handling, Packing and shipping must be conform with IPC/J-033

### 11.1 Soldering

The IC (housings) are qualified for Pbfree reflow soldering according standard AE/QMS requirements. Release for max. 3 reflow soldering cycles. Repair and manual soldering of the sensor is not permitted. For mounting SMA7 onto a PCB, a lead-free reflow-soldering profile has been qualified. This profile is adequate both for using a lead-containing soldering process as well as for using a lead-free soldering process.

Package class is 1 (small device).

Temperature Profile:





Profile Features	Class 1 (small)	Class 2 (large)	Class 3 (very large)
<b>Preheat</b>			
Ramp-Up Rate 20 °C to 150 °C	min. 3 K/s (average value over 10 s)		
Soak Temperature (min): $T_S(\text{min})$	150 °C		
Soak Temperature: $T_S$	190 °C		
Soak Temperature (max): $T_S(\text{max})$	200 °C		
Soak Time ( $T_S$ to $T_S(\text{max})$ ): $t_S(\text{Preheat})$	min. 110 s		
Time between $T_S(\text{max})$ and $T_L$	10 - 85 s		
<b>Peak</b>			
Ramp-Up Rate from 200°C to $T_{\text{peak}}$	0,5 K/s - 3 K/s (average value over 10 s)		
Liquidus Temperature: $T_L$	217 °C		
Time above Liquidus Temperature: $t_L$	min. 90 s		
Peak Temperature: $T_P$	260 (- 0) °C	250 (- 0) °C	245 (- 0) °C
Time within 5 °C of Actual Peak Temperature: $T_P - 5 \text{ K}$	min. 40 s	min. 30 s	min. 30 s
<b>Cooling</b>			
Ramp-Down Rate from Peak Temperature	see table 3 (average over 10s)		
<b>General</b>			
Time to Peak: $t_{\text{to peak}}$	min. 300 s		

**Table 3:** Ramp Down Rate According to Thickness and Volume

Thickness \ Volume	< 350 mm <sup>3</sup>	350-2000 mm <sup>3</sup>	> 2000 mm <sup>3</sup>
< 1,6 mm	-6 K/s	-6 K/s	-6 K/s
1,6 - 2,5 mm	-4 K/s	-4 K/s	-4 K/s
> 2,5 mm	-4 K/s	-4 K/s	-4 K/s

## 11.2 Rework

5238

The SMA7 can be removed from the PCB and replaced by a spare one. Repair of the solder joints is not allowed.

For the removal of an SMA7 special rework equipment has to be used, which controls the temperature profile. The same profile as for reflow-soldering is needed. Before a new SMA7 can be soldered on the PCB, the solder residuals have to be removed.

Potential failure parts have to be removed very carefully, because the removal process itself can cause defects and failures. A local dry bake according to the package's moisture sensitivity level has to be applied at the SMA7 position before removal.

Mechanical removal from the PCB is not recommended.

## 11.3 Shipping

1805

The SMA7 is delivered to the final assembly line packaged in reels.

5209

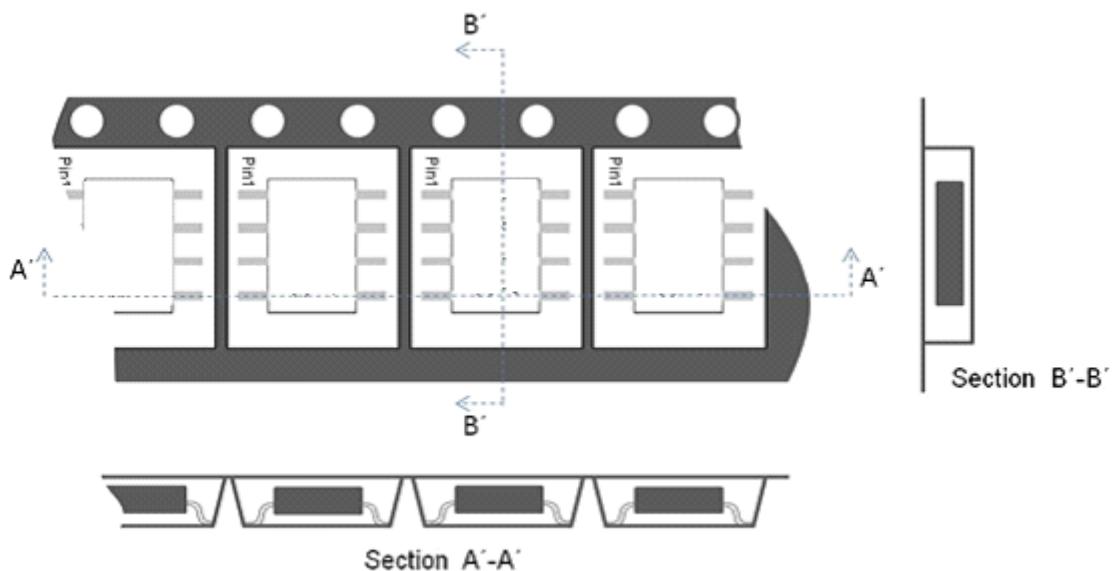
The sensor must not be handled as bulk good.

3305

The components are delivered in ESD-protected tape and reel (DIN IEC 60286-3).

1808

The pin orientation is consistent for all devices in the tape as shown in the figure below.



ID	parameter / condition	min	typ	max	unit
1807	Reel size SO8			4000	pcs.
5411	Reel size LGA			4800	pcs.

1809

Outer package has to be specified.

3306

In a typical reel sensors with different date codes are packed. The oldest date code will be printed on the reel-lable. Single part traceability is guaranteed by unique 48-Bit serial number. The single serial numbers of all parts per reel are stored and known.

It is possible to merge lots (different date codes) with

- small assembly lots with quantity less than the target final test lot size.
- retest lots which contains rejects from the final test (contact failures or rejects due to equipment related failure) and from tape&reel, electrically tested as good part (misplaced parts in tape, picking failures, contact failures, visual read error of marking (pseudo failures)).

3307

The reel labeling includes part number, quantity, date code, lot number and barcode.

ID	parameter / condition	min	typ	max	unit
3309	Maximum Lot Size SOIC8 Lot size during packaging			4000	pcs./reel
5485	Maximum Lot Size LGA Lot size during packaging			4800	pcs./reel
3311	Chips per ASIC-Wafer (+/-1000pcs. resolution)		22000		pcs.
3312	Chips per MEMS-Wafer X/Z (+/-1000pcs. resolution)		17000		pcs.
5367	Chips per MEMS-Wafer		23000		pcs.



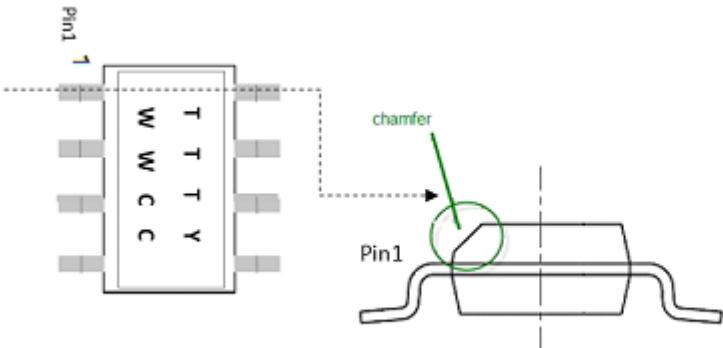
ID	parameter / condition	min	typ	max	unit
	X/Y (+/-1000pcs. resolution)				

## 11.4 Traceability

- 360 Each sensor gets an individual serial number, which identifies it as a unique part. A part history with changes is archived.
- 4017 The ASIC contains a 8bit Revision ID to identify the design revision. The first 4 bit are for full mask redesigns. The second 4 bit are for metal fixes.  
The ID can be read from register 0x44 CFG\_REV\_ID by SPI and PSI BiDir command.
- 4018 The ASIC contains a 4bit internal Revision ID to identify internal design revisions.  
The ID can be read by SPI and PSI BiDir command.

### 11.4.1 Package Marking

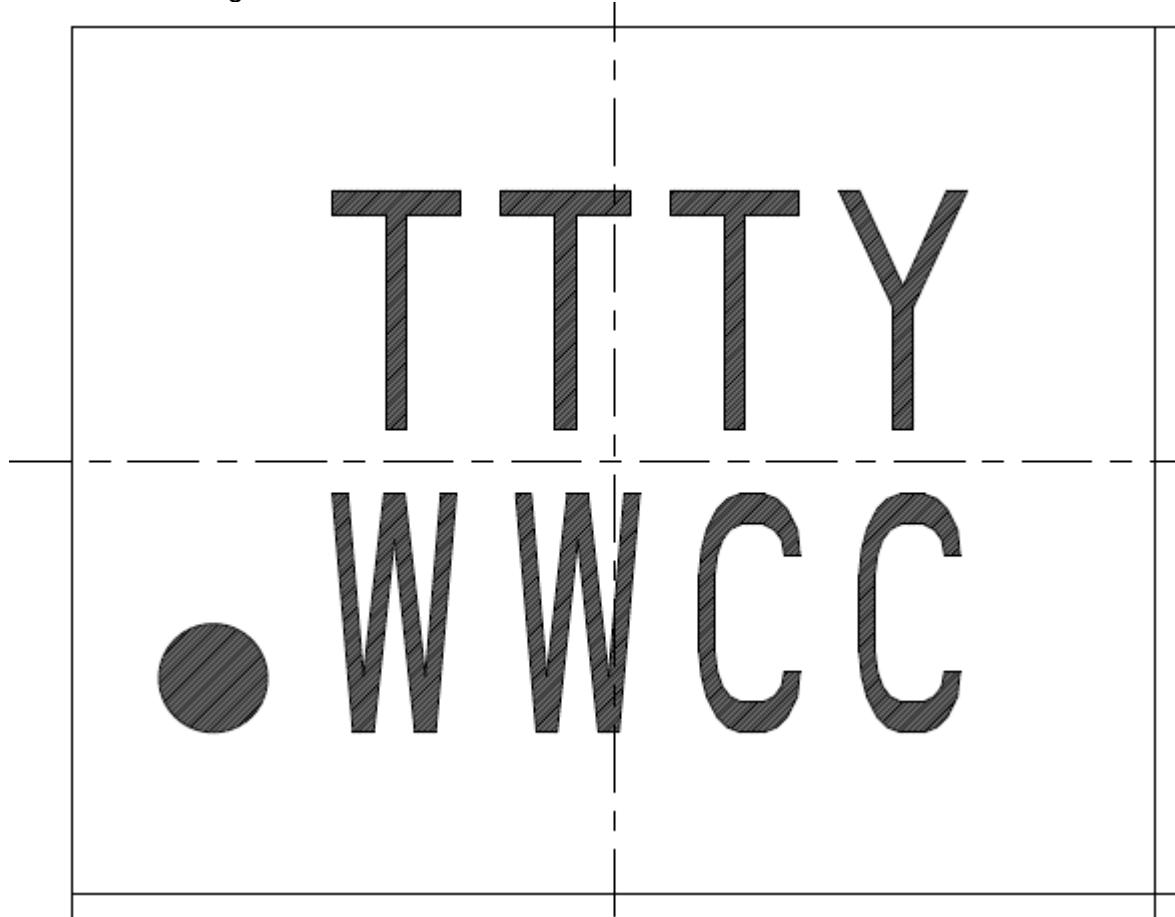
- 5212 SOIC8 lasermarking:



5409



LGA lasermarking:



1611

1600

1602

5239

Packages are traceable with vision systems or reel information readers used in RB factories.  
The laser marking encodes the following information:

- **TTT** = The last three digits of the SMA7 part number. For identical hardware variants always the number of the two channel variant is used (see table below).



Laser-marking	SMA type	TTNR part number
272	SMA720	<b>0273.141.272</b> 0273.141.560
	SMA774	0273.141.303
273	SMA760	<b>0273.141.273</b> 0273.141.561
	SMA773	0273.141.302
298	SMA750	0273.141.356
	SMA752	<b>0273.141.298</b>
	SMA758	0273.141.301
299	SMA755	0273.141.358
	SMA757	<b>0273.141.299</b>
300	SMA751	0273.141.357
	SMA753	<b>0273.141.300</b>
294	SMA780	0273.141.359
	SMA782	<b>0273.141.294</b>
295	SMA781	0273.141.360
	SMA783	<b>0273.141.295</b>
296	SMA790	0273.141.364
	SMA792	<b>0273.141.296</b>
487	SMA780.1	0273.141.490
	SMA782.1	<b>0273.141.487</b>
489	SMA781.1	0273.141.491
	SMA783.1	<b>0273.141.489</b>
488	SMA790.1	0273.141.492
	SMA792.1	<b>0273.141.488</b>

1603

- **WW** = Date code, the work week.
- **Y** = Date code, the production year with modulo 36:
  - 2010 = 0
  - 2011 = 1
  - ...
  - 2020 = A
  - 2021 = B
  - ...
  - 2045 = Z

1601

- **CC** = 2 alphanumeric digits, combined information of packaging provider and lot counter.  
The lot counter is package specific and reset every work week.

#### 11.4.2 ASIC Serial Number

1604

The following data can be identified by the ASIC serial number:

1605

- Assembly site
- Wafer fabrication lot
- Individual die tracking
- Process control data
- Wafer test data
- Final (packaged) test data

1606

1607

1608

1609

1610



## 11.5 Handling Specification

5208

Micro-mechanical sensors are designed to sense acceleration with high accuracy even at low signal amplitudes and contain highly sensitive structures inside the sensor element. The sensors are protected against mechanical shock up to several thousand g's (1 g = 9.81 m/s<sup>2</sup>). However, these limits can be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping of the sensor onto hard surfaces, torque limiters, etc.

3520

There are no special requirements for production line handling, except those stated in the section „Absolute maximum ratings”. Nevertheless it shall be taken into account, that MEMS sensors can theoretically be damaged by high-g vibrations. To avoid this, it is recommended to choose processes with low mechanical load to the device whenever possible.

For Bosch internal handling, it is recommended to apply the valid Manufacturing Process Specification with respect to milling.

5117

Standard ESD guidelines must be respected during handling & transport (for specified ESD values see the corresponding chapter).



## **12. Verification**

4083

The sensor module is designed to also fulfill requirements in this document, which refers to the application in 2nd level package (PAS level). Nevertheless all verification and qualification requirements, which include 2nd level packaging are in the responsibility of the customer.

### **12.1 Qualification and Robustness**

#### **12.1.1 General Requirements**

1826

The IC is AEC-Q100 tested.

1827

The IC qualification is conform to the Bosch QA process (Questionnaire, Pre-Assessment, Deliverables, Joint Qualification etc.).

1829

The IC fulfills the above referenced lifetime requirements for semiconductor devices of the NISSAN MOTOR COMPANY and Toyota.

4693

Based on SMA7 qualification and SMA73x A sample pre-qualification a delta-qualification has to be performed on final design (MEMS/AVT/ASIC that will be released for series production).

#### **12.1.2 Coating**

3417

SMA760 and SMA720 are released for conformal coating.

Coating material:

- HumiSeal 1B51NSLU/521EU PB60 from Humiseal

5175

Moulding, potting and coating with further materials:

SO8 component generally able for moulding, coating and potting.

Specific process parameters for moulding/coating or potting on second level package (type, geometry, processing) has to be released individually by customer in cooperation with sensor development.

### **12.2 Mission Profile**

3604

All mission profiles are alternative use cases. The profiles are not cumulative.

3606

All temperatures are ambient temperatures. The junction temperature can be up to 15 K higher.

#### **12.2.1 Operation profiles**

3188

**Generic profile:**

Temperature	Operation Time
-------------	----------------

105°C	750h
-------	------

100°C	1500h
-------	-------

80°C	6000h
------	-------

60°C	4500h
------	-------

40°C	1500h
------	-------

-40°C	750h
-------	------

sum:	15000h
------	--------

4239

**Profiles for SPI applications:**

Temperature	Operation Time
-------------	----------------

-40°C...40°C	8250h
--------------	-------

40°C...60°C	3000h
-------------	-------

60°C...80°C	2250h
-------------	-------

80°C...100°C	1350h
--------------	-------

100°C...105°C	150h
---------------	------

sum:	15000h
------	--------

Application: AB12 platform (SPI)  
(VDDmax = 7.15V,



T<sub>A</sub> = 125°C), SO8

3189

Temperature Operation Time

-40°C...40°C 38654h

40°C...60°C 18586h

60°C...80°C 2250h

80°C...100°C 1350h

100°C...105°C 150h

sum: 60990h

Application: Hybrid vehicles (SPI)

(VDDmax = 7.15V,

T<sub>A</sub> = 125°C), SO8

4240

**Profiles for PSI applications:**

1614

Temperature Operation Time

125°C 150h

100°C 750h

80°C 3600h

60°C 5100h

25°C 3600h

-20°C 1500h

-40°C 300h

sum: 15000h

Application: Sensor Cluster

1615

Temperature Operation Time

-40°C 480h

23°C 1600h

82°C 5200h

115°C 640h

125°C 80h

sum: 8000h

Application: PSI5,

SO8, LGA

(from AK-LV27)

3187

Temperature Operating Time

-40°C...-10°C 2560h

-10°C...15°C 12160h

15°C...30°C 16000h

30°C...40°C 7680h

40°C...50°C 6080h

50°C...55°C 1440h

55°C...60°C 960h

60°C...65°C 464h

65°C...70°C 281.6h

70°C...75°C 145.6h

75°C...80°C 108.8h

80°C....90°C 67.2h

90°C...100°C 35.2h

100°C...104°C 17.6h

sum: 48000h

Application: DGS Hybrid Battery

(VDDmax = PSI5,

T<sub>A</sub> = 105°C), LGA, SO8



## 12.2.2 Storage Temperature

1622

The IC has to cover a storage time for at least 15 years = 131400h in original packages or higher quality storage packages.

Storage time = primary storage time + n x secondary storage time

Valid primary storage time >= 365 days ; useable time of new material before requalification/reactivation/refreshing according supplier instruction.

Valid secondary storage time >= 365 days ; useable time of new material after requalification / reactivation / refreshing according supplier instruction.

Valid number of requalification / reactivation / refreshing according >= 14

Valid IC storage temperature range [10, 30]°C

1623

The IC inserted on a PCB within the ECU has to cover an ECU storage time for at least 15 years = 131400h.

For data retention purpose a reactivation / refreshing / according supplier instructions is accepted after an ECU storage time of >= 8 years. Valid ECU = IC inserted storage temperature [10,30]°C

ID	parameter / condition	min	typ	max	unit
1655	Non-Operation Temperature all types	-55	+25	+150	°C
1666	Temperature Gradient SO8; During Non-Operation	-20		+20	K/min

3198

### Generic profile:

Temperature Storage Time

-40°C...10°C 100h

10°C...25°C 92000h

25°C...30°C 26300h

30°C...40°C 12900h

40°C...90°C 98h

90°C...130°C 2h

sum: 131400h

5518

### Storage time:

Temperature Storage Time (Sensor in ECU)

-55°C...10°C 50h

10°C...30°C 131400h

30°C...70°C 500h

sum: 131950h

Application: AB12 platform and Hybrid vehicles, DGS Hybrid Battery

3195

Temperature Storage Time (Sensor)

-55°C...10°C 50h

10°C...30°C 8760h

30°C...70°C 50h

125°C...130°C 1h

sum: 8861h

Storage Time at supplier (Rt) not considered.

Application: AB12 platform and Hybrid vehicles, DGS Hybrid Battery



Note: Cumulative to "Storage Time (Sensor in ECU)"

1624      Temperature Storage Time

150°C      500h

sum:      500h

5519      **Non-operating:**

3196      Temperature Non-Operating Time

-40°C...20°C      39930h

20°C...40°C      14520h

40°C...60°C      10890h

60°C...80°C      6534h

80°C...85°C      726h

sum:      72600h

Application: Hybrid vehicles

4903      Temperature Non-Operating Time

-40°C...20°C      47075h

20°C...40°C      17118h

40°C...60°C      12838h

60°C...80°C      7703h

80°C...85°C      856h

sum:      85590h

Application: DGS Hybrid Battery

1626      Temperature Non-Operating Time

-40°C...20°C      73656h

20°C...40°C      26784h

40°C...60°C      20088h

60°C...80°C      12053h

80°C...85°C      1339h

sum:      133920h

Application: AB12

1618      Temperature Non Operation Time \*\*)

-40°C...20°C      64020h

20°C...40°C      23280h

40°C...60°C      17460h

60°C...80°C      10476h

80°C...85°C      1164h

sum:      116400h

1620      \*\*) If battery supply is applicable ICs are supplied with battery voltage of 6....16V with limited supply current (IC in RESET, SLEEP MODE, limited power dissipation)

### 12.2.3 Operation Requirements

4550      The sensor is designed and tested to withstand the following lifetime requirements:

- 54000 Temperature Changes (from cold start to operation)
- 10950 Temperature Changes (56K in average)
- 15years Life Time

ID	parameter / condition	min	typ	max	unit
4896	<ul style="list-style-type: none"> <li>• 17 years lifetime</li> <li>SPI types</li> </ul>				

- 1633
- 1637
- 15000h Operation time
  - 300000km Mileage



- 3202
- 12410 cold start (2 per day) with 54K temperature change
  - 12410 warm start (2 per day) with 30K temperature change

1843 The IC withstands a fast temperature change between  $T_{low}$  and  $T_{high}$  according to DIN IEC 68, Part 2-14 (passive test, IC is not supplied).

### Test Conditions

$T_{low}$ :	-40°C
$T_{high}$ :	125°C
Duration at $T_{low}$ and $T_{high}$ :	30 min
Shift-time:	<= 10 sec
Cycles:	50

1845 The IC is fully in specification (full temperature and voltage range) during and after applying 300000 (=10 times in every operation hour) start up cycles up to steady state.

## 12.3 EMC

4260 The specified values are valid with the application circuit and external components defined in the application chapter above.

### 12.3.1 Testconditions

4527 The sensor is designed and tested with the requirements from the referenced EMC testplan.

### 12.3.2 EMC limits (immunity)

4511 During EMC immunity test conditions the following spec limits are valid.

4512 SPI types:

4514 The spec limits and the parameter definition for SMA720 and SMA760 are summarized in the referenced EMC limit document.

4513 PSI types:

ID	parameter / condition	min	typ	max	unit
4515	Signal during disturbance (Peak value) 30g range; 10bit mode	-8		+8	LSB
4519	Signal during disturbance (Peak value) 60g range; 10bit mode	-6		+6	LSB
4518	Signal during disturbance (Peak value) 10bit mode; SO8; DPI	-4		+4	g
4520	Signal during disturbance (Peak value) 10bit mode; SO8; RIT	-1		+1	g

### 12.3.3 System level requirements

3428 Sensor in SO8 package is able to fulfill also EMC requirements on typical 2nd level. (No special measures like shielding on 2nd level shall be needed). For LGA the metal clamp of the PAS6e or a comparable shielding is necessary.

1867 The design of the module makes sure that the module in combination with the PAS6e 2<sup>nd</sup> level package fulfills the EMC requirements, which are specified below for 2nd level packages.



4530

More precisely, the EMC requirements are fulfilled by SMA7 in combination with a PAS6e 2<sup>nd</sup> level package using the same metallic clamp insert (Einlegeteil=ELT) as PAS6 (drawing number 1274477721, current version: 02) and identical outer dimensions of the inner part (typically made of silicone, "Lolly", drawing number 1274477725, current version: 01) and outer part (typically made of thermoplast, drawing number 1275101046, current version: 00) of the package as PAS6.

This chapter summarizes all requirements, which must be met on system level. The sensor is designed to fulfill the requirements, but verification/testing is in the responsibility of the customer.

#### 12.3.3.1 IC-Stripline-RE

3441

- **Radiated Emission IC-Stripline**
  - Test acc. IEC61967-8
  - Limit class III: K

#### 12.3.3.2 IC-Stripline-RI

3443

- **Radiated Emission IC-Stripline**
  - Test acc. IEC62132-8
  - Limit class III: 800V/m

#### 12.3.3.3 Direct Transient Coupling

3445

- **Direct Transient Coupling**
  - Test acc. IEC62215-3
  - Only for global Pins (with target protection network)
  - Limit class III: ISO 1 (-150V); ISO 2 (+112V); ISO 3a (-220V); ISO 3b (+150V)
  - Test can be performed only if customer provides target protection network

#### 12.3.3.4 Capacitive Transient Coupling

3447

- **Capacitive Transient Coupling with 1nF**
  - Test acc. IEC62215-3
  - Only for global Pins (with target protection network)
  - Limit class III: ISO 3a (-220V); ISO 3b (+150V)
  - Test can be performed only if customer provides target protection network

#### 12.3.3.5 BCI

1882

RF Immunity - Bulk Current Injection (BCI) (ISO 11452-4) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference documents

#### 12.3.3.6 Antenna (Immunity)

1884

RF Immunity - Antenna Irradiation (ISO 11452-2) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference documents

#### 12.3.3.7 MT

1886

RF Immunity to hand portable transmitters (AK-LV 27 Teil 3) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference documents

#### 12.3.3.8 Transient

1888

Conducted transients: Immunity of harness (ISO 7637-3) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference documents



## 12.3.3.9 Magnetic field

1890 Magnetic Field Immunity (ISO 11452-8) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference documents

## 12.3.3.10 Capacitive Voltage Measurement

1892 RF Emission - Capacitive Voltage Measurement (AK-LV27 Teil3) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference

## 12.3.3.11 Antenna (Emmission)

1894 RF Emissions of 125kbps/189kbps - Antenna Measurement (CISPR25, ch. 6.4) according to Generic\_EMC\_Specification for\_peripheral\_Sensors, see reference documents

## 12.3.3.12 J-OEM

4228 **EQ/IC09** from 28401NDS02\_Rev6

Immunity to ignition high voltage

4229 **EQ/IR05** from 28401NDS02\_Rev6

Immunity to handy transmitters

4230 **RI130** from MES\_PW67602\_RevB

Coupled Immunity pulse auf PSI und GND

4231 **RI150** from MES\_PW67602\_RevB

Coupled Immunity sinus auf PSI und GND

4232 **RI115** from MES\_PW67602\_RevB

RF immunity to hand portable transmitters

4233 **RI114** from MES\_PW67602\_RevB

ALSE for sensor

5422 The following requirements from Generic\_EMC\_Specification for\_peripheral\_Sensors v2.0 are fulfilled, as described in PAS6s/f EMC validation sheet:

- BCI OL
- CCV
- ESDH
- ESDI
- REA
- RIA
- RIM
- TOL-CCC
- TOL-ICC

## 12.4 PSRR

4245 The specified values are valid with the application circuit and external components defined in the application chapter above.

4242 **PSI (Mode1):**

ID	parameter / condition	min	typ	max	unit
3461	Maximum Rating PSRR  PSI5 SOIC8; Without failure flag; 1.8kHz...300kHz; U_vdd + U_base >= U_vdd_min; U_vdd + U_base <= U_vdd_max	-1		+1	V
3462	Maximum Rating PSRR	-0.3		+0.3	V

**BOSCH**

Department AE/ESI

**Internal Datasheet  
SMA7**

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SAP: V2, DOORS: 5.3  
Date 17/01/2022  
1.279.929.850

ID	parameter / condition	min	typ	max	unit
	PSI5 SOIC8; Without failure flag; 300kHz...2.5MHz; U_vdd + U_base >= U_vdd_min; U_vdd + U_base <= U_vdd_max				
4023	Maximum Rating PSRR  PSI5 SOIC8; Without failure flag; 2.5MHz...10MHz; U_vdd + U_base >= U_vdd_min; U_vdd + U_base <= U_vdd_max	-0.3		+0.3	V
3466	PSRR Noise_RMS  PSI5 SOIC8; Uvdd = 4.7V + 400mVpp; 100Hz...2.5MHz			in Spec	LSB
3469	PSRR Noise_RMS  PSI5-SiP; Uvdd = 5.05V + 100mVpp; 100Hz...1MHz			in Spec	LSB

4243

**SPI 3.3V (mode 3):**

ID	parameter / condition	min	typ	max	unit
3464	PSRR Noise_PP, SMA760/SMA720-X  SPI; Uvddi = 3.3V + 330mVpp; 100Hz...2.5MHz; @ half-s/d multiples; @14Bit			0.8	LSBpp/mV
3467	PSRR Noise_PP, SMA760/SMA720-X  SPI; Uvddi = 3.3V + 330mVpp; 100Hz...2.5MHz; between half-s/d multiples; @14Bit			0.6	LSBpp/mV
4834	PSRR Noise_PP, SMA720-Z  SPI; Uvddi = 3.3V + 330mVpp; 100Hz...2.5MHz; @ half-s/d multiples; @14Bit			2.24	LSBpp/mV
4835	PSRR Noise_PP, SMA720-Z  SPI; Uvddi = 3.3V + 330mVpp; 100Hz...2.5MHz; between half-s/d multiples; @14Bit			1.68	LSBpp/mV
5447	PSRR Noise_PP, SMA765  SPI; Uvddi = 3.3V + 330mVpp; 100Hz...2.5MHz; @ half-s/d multiples; @14Bit			1.6	LSBpp/mV
5448	PSRR Noise_PP, SMA765  SPI; Uvddi = 3.3V + 330mVpp; 100Hz...2.5MHz; between half-s/d multiples; @14Bit			1.2	LSBpp/mV

4244

**SPI 6.7V (mode 2):**

ID	parameter / condition	min	typ	max	unit
3468	PSRR Noise_RMS  SPI 6.7V mode; Uvdd = 4.7V +/- 200mV; 100Hz...2.5MHz; step size 200Hz			in Spec	LSB



ID	parameter / condition	min	typ	max	unit
3477	PSRR Offset  SPI; 6.7V mode; Uvdd = 4.7V +/- 200mV; 100Hz...2.0MHz; step size 200Hz			in Spec	LSB
3479	PSRR Noise_Peak  SPI; 6.7V mode; Uvdd = 4.7V +/- 200mV; 100Hz...2.0MHz; step size 200Hz			in Spec	LSB

1935

Selfheating in SPI, Mode 2, VDD=6.7V for:

- normal operation: max. 3.3K
- worst-case from Pin-FMEA regarding selheating is VDDI short to GND. In this case the typ. max. temperature of the sensor is 160°C at RT and 180°C at HT.

3524

No sensor specific test over temperature or at a non ambient temperature (~25°C) after soldering will be necessary to achieve any performance or quality goals.



C-SC2: Confidential

<b>Schlüssel:</b> RBGA-5332958	<b>Status:</b> Abgeschlossen >> Freigegeben	<b>aktueller Bearbeiter:</b> Nicht zugewiesen	<b>Antragsteller:</b> Sachsenweger Matthias (AE/ESI3.2)	<b>Erstellt:</b> 27.01.2022
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### RB Allgemeiner Genehmigungsdurchlauf

#### Datensicherheit

Diese Anwendung ist für die Verarbeitung von Daten bis Schutzklasse 2 freigegeben (Vertraulichkeit: C-SC2, Verfügbarkeit: A-SC2, Integrität: I-SC2 - siehe [Sicherheitsstufen-Richtline](#))

#### Archivierungs-Periode

Die Standard-Aufbewahrungszeit beträgt 3 Jahre (beginnend 6 Monate nachdem die Anfrage geschlossen wurde). Anfragen-Level Archivierungseinstellungen kann der Anfragende in einem Einstellungs-Tab festlegen.

#### Einschränkungen

Es ist nicht erlaubt diese Anwendung für Prozesse einzusetzen, die eine Betriebsratsgenehmigung erfordern (nur für Deutschland relevant) oder Anfragen, die SC3 Daten beinhalten.

Ich habe die Nutzungsbedingungen gelesen und bin damit einverstanden.

Kurzbeschreibung:\* Datasheet SMA7 update

Verwendung im Email Betreff und bei der Suche der Anträge / Entwürfe.

Vorname: Matthias

Nachname: Sachsenweger

Abteilung: AE/ESI3.2

Kostenstelle: 208011

Telefonnummer: +49(7121)35-36685

Standort: Reutlingen

Standortkürzel

Company Code 2080

Auftrag  
für  
andere

Freigabe von Produkten und  
Produktänderungen mit  
Produksicherheit- oder  
Produkthaftungsrelevanz  
(entsprechend [CD 00214](#))

Dieses Feld ist nur für die folgenden Anwendungsfälle relevant  
 1) Freigabe von sicherheitsrelevanten Produkten entsprechend der gültigen Version der CD 00214 Kapitel 4.2.8 „Freigabe von sicherheitsrelevanten Produkten“ und  
 2) Freigaben von den Änderungen eines bestehenden Produkts nach SOP entsprechend der gültigen Version der CD 00214 Kapitel 4.8 „Änderungswesen nach SOP“

I confirm that the product has achieved the required level of safety

Beschreibung:\*

Dear colleagues,  
please find attached the updated SMA7 data sheet for your signature.

## Changes since last valid version:

- Added new FT TTNR for SMA720 (0273141560) and SMA760 (0273141561) for RBAC
- Adjusted PSI Sync Pulse Detection Time t\_pulse from typ. 7.11 us to [6.5, 6.83, 7.3] us [MIN, TYP, MAX]
- Highlighted necessity for setting lockbits after programming

All changes are marked in yellow in the document with suffix "highlighted".

With best regards,  
Matthias Sachsenweger

Externer Link zu  
weiterführenden  
Informationen

Bitte geben Sie Internetlinks mit vorangestelltem http:// bzw. https:// an.

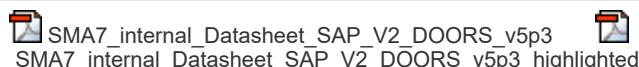
Details: (Falls  
erforderlich)

Wenn eine Zeile hinzugefügt wird, müssen  
beide Spalten, Feld und Wert, ausgefüllt  
werden

**Hinweis:**

- Jede Tabellenzelle kann mit beliebigen Texten oder Zahlen befüllt werden.
- Das Klicken auf Hinzufügen fügt eine weitere Reihe in der Tabelle ein.
- Wenn Sie Details angeben möchten (z.B. IBM ist der Supplier), fügen Sie bitte in der Spalte "Feld" Supplier und in der Spalte "Wert" IBM hinzu.

Anhänge:

**Genehmiger Segment 1**

Genehmigungs-  
ablauf:

Seriell

Seriell bedeutet, alle Genehmiger müssen  
nacheinander genehmigen.

Parallel bedeutet, alle Genehmiger  
bekommen den Antrag gleichzeitig.

Genehmiger:

► Reuter Sabrina  
(AE/ESI3.2)

**(Project manager or product-responsible department/individual(s) according  
to CD 00214)**

**Optional: Genehmiger Segment 2**

Genehmigungs-  
ablauf:

Parallel

Seriell bedeutet, alle Genehmiger müssen  
nacheinander genehmigen.

Parallel bedeutet, alle Genehmiger  
bekommen den Antrag gleichzeitig.

Paralleler Workflow:

Sobald einer der Genehmiger ablehnt, wird  
der Antrag geschlossen

Genehmiger:

► Ullmann Dirk  
(AE/ESI)

**CCs ►** Dertinger Armin (AE/ESI4), Neuhaeuser Marc (AE/ESI4.1), Stoll Oliver  
(AE/ESI3), Schneider Katharina (AE/ESI4.1), Weissel Florian (AE/ESI3.2),

► Bisshopink Georg  
(AE/ESE)

**CCs ►** Kress Katharina (AE/PAS1.1), Liedtke Laura (AE/PAS1.1), Domdey Desislava  
(AE/PAS1),

► Reutter Annette  
(RtP1/PRM-SCO)

**CCs ►** Bolz Uwe (RtP1/PRM2-SCO), Metzger Lars (RtP1/PRM2-SCO), Carle Wolfgang  
(RtP1/PRM2-SCO),

► Balz Stefan (CC-  
OSS/EPH)

**CCs ►** Simsek Tugba (CC-OSS/EPH1), Jusufi Faton (CC-OSS/EPH1), Lindemann  
Timo (CC-OSS/EPH1), Schruellkamp Michael (CC-OSS/EPH1),

**Information senden, wenn Antrag genehmigt oder abgelehnt wurde**

Informieren, wenn  
Antrag genehmigt  
wurde:

[Redacted]

Informieren, wenn  
Antrag abgelehnt  
wurde:

[Redacted]

**Archiv-Einstellungen**

Beginne Archiv bei

6

Monaten

Speichere Archiv für

420

Monate

Link zur Zentralanweisung: [Information Governance and Storage on Image or Data Media](#)

Für weitere Informationen zum WorkON Archiv: [bitte hier klicken](#)

**Genehmiger Kommentare**

**Genehmiger-Kommentare**

Erlaube Kommentare während des Arbeitsablaufs/Genehmigung

Falls nicht ausgewählt, kann der Genehmiger keine Kommentare während des Genehmigungsprozesses erstellen

**Genehmiger können während des Genehmigungsvorgangs Anhänge hinzufügen**

Hinzufügen von Anlagen während des Genehmigungsworkflows zulassen

Die Genehmiger können keine Anhänge hochladen, wenn die Option nicht angeklickt ist

**Vorlage**

Diese Vorlagen-Sektion ist optional. Sie ist ein bequemer Weg um Inhalte und Workflows durch das Laden der passenden Vorlage einzutragen. Dies kann Ihre eigene oder eine mit Ihnen geteilte Vorlage sein.

Falls keine Vorlage verfügbar ist, können Sie Ihre eingetragenen Daten als neue Vorlage speichern, welche dann geladen werden kann.

Keine Vorlage

Genehmigungen / Bewertungen [Kommentare](#) [Änderungshistorie](#) [Alle](#)

Funktion	bearbeitet (von)	Datum / Uhrzeit (GMT +01:00)	Kommentar
Project manager or product-responsible department/individual(s) according to CD 00214	Check and Approve (Reuter Sabrina (AE/ESI3.2))	31. January 2022 09:24	
	Genehmigen (Bischopink Georg (AE/ESE))	31. January 2022 09:42	
	Genehmigen (Ullmann Dirk (AE/ESI))	31. January 2022 10:15	
	Genehmigen (Balz Stefan (CC-OSS/EPH))	01. February 2022 07:12	
	Genehmigen (Reutter Annette (RtP1/PRM-SCO))	01. February 2022 19:06	