KHALID M. AL-HAWAJ

Al-Waha, Al-Qatif, Saudi Arabia
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RESEARCH INTERESTS

Computer Architecture, Vector Architectures, VLSI, Digital Design, Processing-In-Memory, Compute-In-Memory, SRAM Memory

EDUCATION

Cornell University *2015 - 2022*
Doctor of Philosophy in Electrical & Computer Engineering
Advisor: Professor Christopher Batten
Thesis Title: Ephemeral Vector Engines

Harvard University *2012 - 2015*
Masters of Engineering in Engineering Sciences
Advisor: Professor David Brooks
Thesis Title: Unified Cache

King Fahd University of Petroleum and Minerals *2004 - 2009*
Bachelor of Science in Computer Engineering
Overall GPA: 3.95 / 4.00
Core GPA: 4.00 / 4.00

PUBLICATIONS

Khalid Al-Hawaj, Tuan Ta, Nick Cebry, Shady Agwa, Olalekan Afuye, Eric Hall, Courtney Golden, Alyssa Apsel, and Christopher Batten. "EVE: Ephemeral Vector Engines". *In 2023 29th IEEE International Symposium on High-Performance Computer Architecture (**HPCA-29**)*. IEEE, 2023

Tuan Ta, Khalid Al-Hawaj, Nick Cebry, Yanghui Ou, Eric Hall, Courtney Golden, and Christopher Batten. "big.VLITTLE: On-Demand Data-Parallel Acceleration for Mobile Systems on Chip". *In 2022 55th IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, pages 181–198. IEEE, 2022

Helena Caminal, Kailin Yang, Srivatsa Srinivasa, Akshay Krishna Ramanathan, Khalid Al-Hawaj, Tianshu Wu, Vijaykrishnan Narayanan, Christopher Batten, and José F Martínez. "CAPE: A Content-Addressable Processing Engine". *In 2021 IEEE International Symposium on High-Performance Computer Architecture (**HPCA**)*, pages 557–569. IEEE, 2021

Khalid Al-Hawaj, Olalekan Afuye, Shady Agwa, Alyssa Apsel, and Christopher Batten. "Towards a Reconfigurable Bit-serial/Bit-parallel Vector Accelerator Using In-Situ Processing-In-SRAM". *In 2020 IEEE International Symposium on Circuits and Systems (**ISCAS**)*, pages 1–5. IEEE, 2020

Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, and Ronald G Dreslinski. "A 1.4 Ghz 695 Giga RISC-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS". *In 2019 Symposium on VLSI Circuits (**VLSI**)*, pages C30–C31, 2019

Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, and Ronald G. Dreslinski. "Evaluating Celerity: A 16-nm 695 Giga-RISC-V Instructions/s Manycore Processor With Synthesizable PLL". *IEEE Solid-State Circuits Letters (**ISSCL**)*, 2(12):289–292, 2019

Scott Davidson, Shaolin Xie, Christopher Torng, Khalid Al-Hawai, Austin Rovinski, Tutu Ajayi, Luis Vega, Chun Zhao, Ritchie Zhao, Steve Dai, Aporva Amarnath, Bandhav Veluri, Paul Gao, Anuj Rao, Gai Liu, Rajesh K. Gupta, Zhiru Zhang, Ronald Dreslinski, Christopher Batten, and Michael Bedford Taylor. "The Celerity Open-Source 511-Core RISC-V Tiered Accelerator Fabric: Fast Architectures and Design Methodologies for Fast Chips". *IEEE Micro*, 38(2):30–41, 2018

Christopher Torng, Shunning Jiang, Khalid Al-Hawaj, Ivan Bukreyev, Berkin Ilbeyi, Tuan Ta, Lin Cheng, Julian Puscar, Ian Galton, and Christopher Batten. "A New Era of Silicon Prototyping in Computer Architecture Research". *In RISC-V Day Workshop*, 2018

Ji Kim, Shunning Jiang, Christopher Torng, Moyang Wang, Shreesha Srinath, Berkin Ilbeyi, Khalid Al-Hawaj, and Christopher Batten. "Using Intra-Core Loop-Task Accelerators to Improve the Productivity and Performance of Task-Based Parallel Programs". *In 2017 50th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, pages 759–773. IEEE, 2017

Khalid Musa Al-Hawaj, Yuan Zhou, and Zhiru Zhang. "A New Approach to Automatic Memory Banking Using Trace-Based Address Mining". *In Proceedings of the 2017 ACM/SIGDA International Symposium on Field- Programmable Gate Arrays (**FPGA**)*, pages 179–188, 2017

Scott Davidson, Khalid Al-Hawaj, Austin Rovinski. "Celerity: An Open Source RISC-V Tiered Accelerator Fabric". *In Symposium on High Performance Chips (**Hot Chips**)*, 2017

Khalid Al-Hawaj, Simone Campanoni, Gu-Yeon Wei, David Brooks. "Unified Cache: A Case for Low-Latency Communication". *3rd International Workshop on Parallelism in Mobile Platforms (**PRISM**)*. Portland, OR, USA. June 13-17, 2015

ACADEMIC EXPERIENCE

Batten Research Group Aug, 2015 - Dec, 2022
Graduate Research Assistant *Cornell University*

- *Ephemeral Vector Engines* – lead the effort in developing a SRAM-based compute-in-memory (S-CIM) solution to alleviate the area overhead associated with vector execution in general-purpose compute systems
- *big.VLITTLE Architecture* – contributed to developing a novel on-demand reconfigurable next-generation vector architecture for heterogeneous mobile system-on-chip with minimal area overheads
- *Content Addressable Processing Engine in collaboration with M3 Architecture Group* – contributed to the effort in developing a content addressable processing engine leveraging vector execution as the programming abstraction.
- *Celerity Chip* – lead the design and implementation of the AgileBNN accelerator as part of the broader Celerity chip effort.
- *Developments in gem5* – lead the design and implementation of multiple projects in gem5: an integrated vector unit supporting RISC-V RVV extension, a decoupled vector engine supporting RISC-V RVV extension, and a RoCC-inspired interface enabling decoupled accelerator integration with the O3 CPU model. I also contributed to the development of an in-order CPU model and few enhancements/extensions in gem5.
- *Developments in GCC Toolchain* – implemented support for RISC-V RVV extension in GCC and GNU binary utilities (binutils).

VLSIArch Aug, 2012 - Jan, 2015
Masters of Engineering Student *Harvard University*

- *Helix Project* – lead the design and implementation of unified cache leveraging a LEON3 SPARC core. Unified cache is able to lower the parallelization overhead, thus allowing a chip multi-processor system to accelerator small and large loops alike. Unified cache showcase the importance and of pro-active and decoupled coherence of synchronization signals and data in enabling automatic compiler parallelization. Unified cache is able to demonstrate its findings on a physical chip multi-processor running a full operating system.

WORK EXPERIENCE

King Fahd University of Petroleum and Minerals Dec., 2022 - *Present*
Assistant Professor *Dhahran, Kingdom of Saudi Arabia*

- Working as part of the department of computer engineering in the College of Computing and Mathematics.
- Courses taught: COE292, COE301

King Fahd University of Petroleum and Minerals May, 2015 - Dec., 2022
Lecturer *Dhahran, Kingdom of Saudi Arabia*

- On-leave pursuing my Ph.D. degree at Cornell University
- Helped developing new course materials for digital design

King Fahd University of Petroleum and Minerals Nov., 2011 - May, 2015
Graduate Assistant *Dhahran, Kingdom of Saudi Arabia*

- On-leave pursuing my Masters of Engineering at Harvard University.
- Worked with Professor Alaaeldin Amin on research pertaining to computer arithmetic

Saudi Arabia Basic Industry Company (SABIC) July, 2009 - Nov., 2011
Software Analyst - SAP PP Consultant *Al-Jubail, Kingdom of Saudi Arabia*

- *EMDAD Project* – I assumed the position for steel production planning consultant in the EMDAD project. I primarily lead the implementation, testing, and verification of SAP PP/DS in HADEED. During the new implementation, I lead the effort to introduce a new production planning process. I also lead re-vitalizing and re-hauling assisted detailed scheduling. I also contributed crucially to re-hauling and reassessing the sales and logistics processes to align with the new production planning process.

TEACHING EXPERIENCE

King Fahd University of Petroleum and Minerals Spring, 2023
Instructor
COE-301: Computer Organization

King Fahd University of Petroleum and Minerals Spring, 2023
Instructor
COE-292: Introduction to Artificial Intelligence

Cornell University Spring, 2020
Lead Graduate Teaching Assistant
ECE-5745: Complex Digital ASIC Design

Cornell University Fall, 2017
Lead Graduate Teaching Assistant
ECE-4750: Introduction to Computer Architecture