

## 1. Description

## 1.1. Project

Project Name	JAVELIN
Board Name	NUCLEO-H743ZI2
Generated with:	STM32CubeMX 6.6.1
Date	12/30/2022

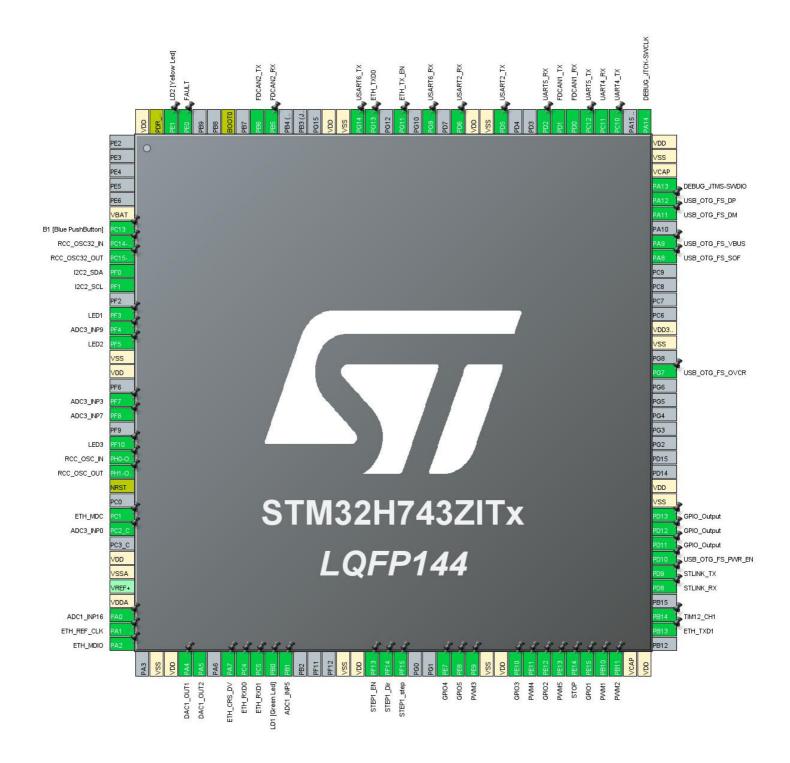
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

## 1.3. Core(s) information

Core(s)	ARM Cortex-M7

## 2. Pinout Configuration



## 3. Pins Configuration

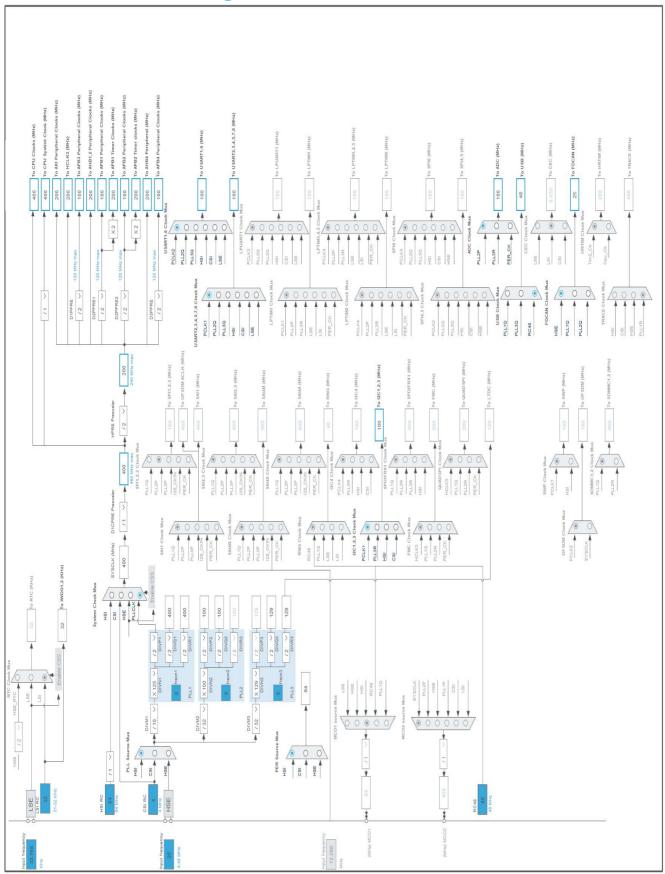
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	B1 [Blue PushButton]
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
13	PF3 *	I/O	GPIO_Output	LED1
14	PF4	I/O	ADC3_INP9	
15	PF5 *	I/O	GPIO_Output	LED2
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	ADC3_INP3	
20	PF8	I/O	ADC3_INP7	
22	PF10 *	I/O	GPIO_Output	LED3
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
28	PC2_C	I/O	ADC3_INP0	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	ADC1_INP16	
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	
41	PA5	I/O	DAC1_OUT2	
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
46	PB0 *	I/O	GPIO_Output	LD1 [Green Led]
47	PB1	I/O	ADC1_INP5	

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
51	VSS	Power		
52	VDD	Power		
53	PF13 *	I/O	GPIO_Output	STEP1_EN
54	PF14 *	I/O	GPIO_Output	STEP1_Dir
55	PF15 *	I/O	GPIO_Output	STEP1_step
58	PE7 *	I/O	GPIO_Output	GPIO4
59	PE8 *	I/O	GPIO_Output	GPIO5
60	PE9	I/O	TIM1_CH1	PWM3
61	VSS	Power	TIWI_OITI	1 WWO
62	VDD	Power		
63	PE10 *	I/O	GPIO_Output	GPIO3
64	PE11	I/O	TIM1_CH2	PWM4
65	PE12 *	I/O	GPIO_Output	GPIO2
66	PE13	I/O	TIM1_CH3	PWM5
67	PE14 *	I/O	GPIO_Output	STOP
68	PE15 *	I/O	GPIO_Output	GPIO1
69	PB10	I/O	TIM2_CH3	PWM1
70	PB11	I/O	TIM2_CH4	PWM2
71	VCAP	Power	TIME_OTIA	1 VVIVIZ
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	
75	PB14	I/O	TIM12_CH1	
77	PD8	I/O	USART3_TX	STLINK_RX
78	PD9	I/O	USART3_RX	STLINK_TX
79	PD10 *	I/O	GPIO_Output	USB_OTG_FS_PWR_EN
80	PD11 *	I/O	GPIO_Output	00B_010_10_1 WI(_EIV
81	PD12 *	I/O	GPIO_Output	
82	PD13 *	I/O	GPIO_Output	
83	VSS	Power	01 10_0uipui	
84	VDD	Power		
92	PG7	I/O	GPIO_EXTI7	USB_OTG_FS_OVCR
94	VSS	Power	OI IO_EXTII	030_010_13_0701
95	VDD33_USB	Power		
100	PA8	I/O	USB_OTG_FS_SOF	
101	PA9	I/O	USB_OTG_FS_VBUS	
103	PA9	I/O	USB_OTG_FS_DM	
104	PA12	1/0	USB_OTG_FS_DP	
105	PA13 (JTMS/SWDIO)	I/O Bower	DEBUG_JTMS-SWDIO	
106	VCAP	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
111	PC10	I/O	UART4_TX	
112	PC11	I/O	UART4_RX	
113	PC12	I/O	UART5_TX	
114	PD0	I/O	FDCAN1_RX	
115	PD1	I/O	FDCAN1_TX	
116	PD2	I/O	UART5_RX	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	USART2_RX	
124	PG9	I/O	USART6_RX	
126	PG11	I/O	ETH_TX_EN	
128	PG13	I/O	ETH_TXD0	
129	PG14	I/O	USART6_TX	
130	VSS	Power		
131	VDD	Power		
135	PB5	I/O	FDCAN2_RX	
136	PB6	I/O	FDCAN2_TX	
138	воото	Boot		
141	PE0	I/O	GPIO_EXTI0	FAULT
142	PE1 *	I/O	GPIO_Output	LD2 [Yellow Led]
143	PDR_ON	Reset		
144	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

## 4. Clock Tree Configuration



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## 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	JAVELIN
Project Folder	C:\Users\joshh\CLionProjects\ProjectJAVELIN
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.10.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LWIP_Init	LWIP
4	MX_USART3_UART_Init	USART3
5	MX_IWDG1_Init	IWDG1
6	MX_FDCAN1_Init	FDCAN1
7	MX_FDCAN2_Init	FDCAN2
8	MX_TIM12_Init	TIM12
9	MX_TIM16_Init	TIM16
10	MX_ADC3_Init	ADC3
11	MX_ADC1_Init	ADC1

Rank	Function Name	Peripheral Instance Name
12	MX_I2C2_Init	I2C2
13	MX_TIM1_Init	TIM1
14	MX_TIM2_Init	TIM2
15	MX_UART4_Init	UART4
16	MX_USART2_UART_Init	USART2
17	MX_DAC1_Init	DAC1
18	MX_UART5_Init	UART5
19	MX_USART6_UART_Init	USART6
20	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS

# 6. Power Consumption Calculator report

#### 6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev8

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

### 6.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

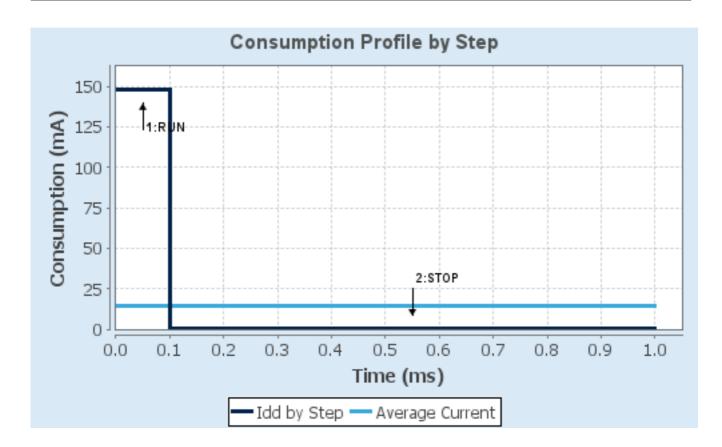
## 6.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.46	124.98
Category	In DS Table	In DS Table

### 6.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001
-	-	_	DMIPS

### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

7.1. ADC1

IN5: IN5 Single-ended IN16: IN16 Single-ended 7.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 4

Resolution ADC 16-bit resolution

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Left Bit Shift No bit shift

Conversion Data Management Mode Regular Conversion data stored in DR register only

Low Power Auto Wait Disabled

ADC\_Regular\_ConversionMode:

Enable Regular ConversionsEnableEnable Regular OversamplingDisableNumber Of Conversion1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

ChannelChannel 5Sampling Time1.5 CyclesOffset NumberNo offsetOffset Signed SaturationDisable

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

7.2. ADC3 mode: IN0

IN3: IN3 Single-ended

mode: IN7 mode: IN9

mode: Vbat Channel

mode: Temperature Sensor Channel

mode: Vrefint Channel7.2.1. Parameter Settings:

#### ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 16-bit resolution

Scan Conversion Mode Enabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Left Bit Shift No bit shift

Conversion Data Management Mode Regular Conversion data stored in DR register only

Low Power Auto Wait Disabled

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling

Enable \*

Oversampling Right Shift No bit shift for oversampling

Oversampling Ratio 2

Regular Oversampling Mode Oversampling Continued Mode

Triggered Regular Oversampling Single trigger for all oversampled conversions

Number Of Conversion 3

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Temperature Sensor \*

Sampling Time 387.5 Cycles \*

Offset Number No offset
Offset Signed Saturation Disable
Rank 2 \*

Channel Vbat \*

Sampling Time 32.5 Cycles \*

Offset Number No offset
Offset Signed Saturation Disable
Rank 3 \*

Channel Vrefint \*

Sampling Time 32.5 Cycles \*

Offset Number No offset
Offset Signed Saturation Disable

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

#### **7.3. CORTEX M7**

#### 7.3.1. Parameter Settings:

#### **Speculation default mode Settings:**

Speculation default mode Disabled

**Cortex Interface Settings:** 

CPU ICache Enabled \*
CPU DCache Enabled \*

#### **Cortex Memory Protection Unit Control Settings:**

MPU Control Mode Background Region Privileged accesses only + MPU Disabled

during hard fault, NMI and FAULTMASK handlers \*

**Cortex Memory Protection Unit Region 0 Settings:** 

MPU Region Enabled \*

MPU Region Base Address 0x30040000 \*

MPU Region Size 32KB \*

MPU SubRegion Disable 0x0 \*

MPU TEX field level level 1 \*

MPU Access Permission ALL ACCESS PERMITTED \*

MPU Instruction Access

**DISABLE**\*

MPU Shareability Permission DISABLE
MPU Cacheable Permission DISABLE
MPU Bufferable Permission DISABLE

**Cortex Memory Protection Unit Region 1 Settings:** 

MPU Region Enabled \*

MPU Region Base Address 0x30040000 \*

MPU Region Size 256B \*
MPU SubRegion Disable 0x0 \*
MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED \*

MPU Instruction Access

MPU Shareability Permission

MPU Cacheable Permission

MPU Bufferable Permission

ENABLE \*

MPU Bufferable Permission

ENABLE \*

**Cortex Memory Protection Unit Region 2 Settings:** 

MPU Region Disabled

Cortex Memory Protection Unit Region 3 Settings: MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings: MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region

Disabled

Cortex Memory Protection Unit Region 6 Settings: MPU Region Disabled

**Cortex Memory Protection Unit Region 7 Settings:**MPU Region Disabled

Cortex Memory Protection Unit Region 8 Settings: MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

**Cortex Memory Protection Unit Region 10 Settings:** 

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region

Disabled

**Cortex Memory Protection Unit Region 13 Settings:** 

MPU Region Disabled

**Cortex Memory Protection Unit Region 14 Settings:** 

MPU Region Disabled

**Cortex Memory Protection Unit Region 15 Settings:** 

MPU Region Disabled

7.4. DAC1

OUT1 connected to: only external pin OUT2 connected to: only external pin

7.4.1. Parameter Settings:

**DAC Out1 Settings:** 

Mode selected Normal Mode
Output Buffer Enable
Trigger None

User Trimming Factory trimming

**DAC Out2 Settings:** 

Mode selected Normal Mode
Output Buffer Enable
Trigger None

User Trimming Factory trimming

**7.5. DEBUG** 

**Debug: Serial Wire** 

7.6. ETH

Mode: RMII

7.6.1. Parameter Settings:

**General: Ethernet Configuration:** 

Warning The ETH can work only when RAM is pointing at 0x24000000

Note PHY Driver must be configured from the LwIP 'Platform Settings' top right tab

Ethernet MAC Address 00:80:E1:00:00:00

Tx Descriptor Length 4

First Tx Descriptor Address 0x30000200 \*

Rx Descriptor Length 4

First Rx Descriptor Address 0x30000000 \*

Rx Buffers Length 1536

#### 7.7. FDCAN1

#### mode: Activated

#### 7.7.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format Classic mode Mode Normal mode Auto Retransmission Disable Transmit Pause Disable Disable Protocol Exception Nominal Sync Jump Width 1 Data Prescaler Data Sync Jump Width Data Time Seg1 Data Time Seg2 Message Ram Offset 0 Std Filters Nbr 0 Ext Filters Nbr 0 Rx Fifo0 Elmts Nbr 0

Rx Fifo0 Elmt Size 8 bytes data field

Rx Fifo1 Elmts Nbr 0

Rx Fifo1 Elmt Size 8 bytes data field

Rx Buffers Nbr 0

Rx Buffer Size 8 bytes data field

Tx Events Nbr0Tx Buffers Nbr0Tx Fifo Queue Elmts Nbr0

Tx Fifo Queue Mode FIFO mode
Tx Elmt Size 8 bytes data field

**Clock Calibration Unit:** 

Clock Calibration Disable

**Bit Timings Parameters:** 

Nominal Time for one Bit

Nominal Prescaler 16

Nominal Time Quantum 640.0 \*

Nominal Time Seg1 2

Nominal Time Seg2 2

Nominal Baud Rate 312500 \*

3200 \*

#### **7.8. FDCAN2**

#### mode: Activated

#### 7.8.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format Classic mode Mode Normal mode Disable Auto Retransmission **Transmit Pause** Disable Protocol Exception Disable Nominal Sync Jump Width 1 Data Prescaler 1 Data Sync Jump Width 1 Data Time Seg1 Data Time Seg2 Message Ram Offset 0 Std Filters Nbr 0 Ext Filters Nbr 0 Rx Fifo0 Elmts Nbr 0

Rx Fifo0 Elmt Size 8 bytes data field

Rx Fifo1 Elmts Nbr 0

Rx Fifo1 Elmt Size 8 bytes data field

Rx Buffers Nbr 0

Rx Buffer Size 8 bytes data field

 Tx Events Nbr
 0

 Tx Buffers Nbr
 0

 Tx Fifo Queue Elmts Nbr
 0

Tx Fifo Queue Mode FIFO mode
Tx Elmt Size 8 bytes data field

**Clock Calibration Unit:** 

Clock Calibration Disable

**Bit Timings Parameters:** 

Nominal Prescaler 16

Nominal Time Quantum 640.0 \*

Nominal Time Seg1 2
Nominal Time Seg2 2

Nominal Time for one Bit 3200 \*

Nominal Baud Rate 312500 \*

#### 7.9. I2C2

12C: 12C

#### 7.9.1. Parameter Settings:

#### Timing configuration:

Custom Timing Disabled

I2C Speed Mode Fast Mode \*

I2C Speed Frequency (KHz)400Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled

Timing 0x009034B6 \*

#### **Slave Features:**

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled

Primary slave address 0

#### 7.10. IWDG1

mode: Activated

#### 7.10.1. Parameter Settings:

#### **Watchdog Clocking:**

IWDG counter clock prescaler

IWDG window value

4095

IWDG down-counter reload value

4095

#### 7.11. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

### 7.11.1. Parameter Settings:

**Power Parameters:** 

SupplySource PWR\_LDO\_SUPPLY

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

**RCC Parameters:** 

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 16
HSI Calibration Value 32

**System Parameters:** 

VDD voltage (V) 3.3

Flash Latency(WS) 2 WS (3 CPU cycle)

Product revision rev.Y

**PLL range Parameters:** 

PLL1 clock Input range

PLL2 input frequency range

Between 4 and 8 MHz

Between 2 and 4 MHz

PLL1 clock Output range

Wide VCO range

Wide VCO range

7.12. SYS

**Timebase Source: TIM17** 

7.13. TIM1

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3

7.13.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 16 bits value) 0
auto-reload preload Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

**BRK Sources Configuration** 

Digital Input
COMP1
COMP2
Disable
DFSDM
Disable

#### **Break And Dead Time management - BRK2 Configuration:**

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

**BRK2 Sources Configuration** 

Digital Input
 COMP1
 COMP2
 Disable
 DFSDM
 Disable

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

#### **Clear Input:**

Clear Input Source Disable

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

#### **PWM Generation Channel 2:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

#### **PWM Generation Channel 3:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

#### 7.14. TIM2

Channel3: PWM Generation CH3
Channel4: Forced Output CH4

#### 7.14.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value ) 4294967295
Internal Clock Division (CKD) No Division
auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

#### **Clear Input:**

Clear Input Source Disable

#### **PWM Generation Channel 3:**

Mode PWM mode 1

Pulse (32 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

#### **Forced Output Channel 4:**

Mode Forced Active

Pulse (32 bits value) 0
Output compare preload Disable
CH Polarity High

#### 7.15. TIM12

**Channel1: PWM Generation CH1** 

### 7.15.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division
auto-reload preload Enable \*

**Clear Input:** 

Clear Input Source Disable

**PWM Generation Channel 1:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

#### 7.16. TIM16

mode: Activated

#### 7.16.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Enable \*

#### 7.17. UART4

#### **Mode: Asynchronous**

#### 7.17.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None

Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable **Data Inversion** TX and RX Pins Swapping Disable Enable Overrun Enable DMA on RX Error MSB First Disable

#### 7.18. UART5

#### **Mode: Asynchronous**

#### 7.18.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

**Advanced Features:** 

Auto Baudrate Disable
TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable

Data InversionDisableTX and RX Pins SwappingDisableOverrunEnableDMA on RX ErrorEnableMSB FirstDisable

#### 7.19. USART2

#### **Mode: Asynchronous**

#### 7.19.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

#### **Advanced Features:**

Disable Auto Baudrate Disable TX Pin Active Level Inversion **RX Pin Active Level Inversion** Disable Disable Data Inversion Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

#### 7.20. USART3

#### **Mode: Asynchronous**

#### 7.20.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable **Data Inversion** TX and RX Pins Swapping Disable Enable Overrun Enable DMA on RX Error MSB First Disable

#### 7.21. USART6

#### **Mode: Asynchronous**

#### 7.21.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Data Inversion Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

7.22. USB\_OTG\_FS

Mode: Device\_Only

Activate\_VBUS: VBUS sensing

mode: Activate\_SOF

7.22.1. Parameter Settings:

Speed Full Speed 12MBit/s

Enable internal IP DMA Disabled
Low power Disabled
Battery charging Enabled
Link Power Management Disabled
Use dedicated end point 1 interrupt Disabled
VBUS sensing Enabled
Signal start of frame Enabled

#### 7.23. FREERTOS

Interface: CMSIS\_V2

#### 7.23.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.3.1 CMSIS-RTOS version 2.00

MPU/FPU:

ENABLE\_MPU Disabled ENABLE\_FPU Enabled \*

Kernel settings:

USE\_PREEMPTION Enabled

CPU\_CLOCK\_HZ SystemCoreClock

TICK\_RATE\_HZ 1000
MAX\_PRIORITIES 56
MINIMAL\_STACK\_SIZE 128
MAX\_TASK\_NAME\_LEN 16

USE\_16\_BIT\_TICKS Disabled
IDLE\_SHOULD\_YIELD Enabled
USE\_MUTEXES Enabled
USE\_RECURSIVE\_MUTEXES Enabled
USE\_COUNTING\_SEMAPHORES Enabled
QUEUE\_REGISTRY\_SIZE 8

USE\_APPLICATION\_TASK\_TAG Disabled

ENABLE\_BACKWARD\_COMPATIBILITY Enabled

USE\_PORT\_OPTIMISED\_TASK\_SELECTION Disabled

USE\_TICKLESS\_IDLE Disabled

USE\_TASK\_NOTIFICATIONS Enabled

RECORD\_STACK\_HIGH\_ADDRESS Enabled \*\*

#### Memory management settings:

Memory Allocation Dynamic / Static

TOTAL\_HEAP\_SIZE 65536 \*

Memory Management scheme heap\_4

#### **Hook function related definitions:**

USE\_IDLE\_HOOK Disabled

USE\_TICK\_HOOK Disabled

USE\_MALLOC\_FAILED\_HOOK Disabled

USE\_DAEMON\_TASK\_STARTUP\_HOOK Disabled

CHECK\_FOR\_STACK\_OVERFLOW Disabled

#### Run time and task stats gathering related definitions:

GENERATE\_RUN\_TIME\_STATS

USE\_TRACE\_FACILITY

USE\_STATS\_FORMATTING\_FUNCTIONS

Enabled \*

#### Co-routine related definitions:

USE\_CO\_ROUTINES Disabled MAX\_CO\_ROUTINE\_PRIORITIES 2

#### Software timer definitions:

USE\_TIMERS Enabled
TIMER\_TASK\_PRIORITY 2
TIMER\_QUEUE\_LENGTH 10
TIMER\_TASK\_STACK\_DEPTH 256

#### Interrupt nesting behaviour configuration:

LIBRARY\_LOWEST\_INTERRUPT\_PRIORITY 15
LIBRARY\_MAX\_SYSCALL\_INTERRUPT\_PRIORITY 5

#### Added with 10.2.1 support:

MESSAGE\_BUFFER\_LENGTH\_TYPE size\_t
USE\_POSIX\_ERRNO Disabled

#### **CMSIS-RTOS V2 flags:**

USE\_OS2\_THREAD\_SUSPEND\_RESUME Enabled
USE\_OS2\_THREAD\_ENUMERATE Enabled
USE\_OS2\_EVENTFLAGS\_FROM\_ISR Enabled
USE\_OS2\_THREAD\_FLAGS Enabled
USE\_OS2\_TIMER Enabled
USE\_OS2\_MUTEX Enabled

#### 7.23.2. Include parameters:

#### Include definitions:

vTaskPrioritySet Enabled Enabled uxTaskPriorityGet Enabled vTaskDelete vTaskCleanUpResources Disabled Enabled vTaskSuspend Enabled vTaskDelayUntil Enabled vTaskDelay Enabled xTaskGetSchedulerState Enabled xTaskResumeFromISR xQueueGetMutexHolder Enabled Disabled xSemaphoreGetMutexHolder Disabled pcTaskGetTaskName Enabled uxTaskGetStackHighWaterMark Enabled xTaskGetCurrentTaskHandle Enabled eTaskGetState Disabled xEventGroupSetBitFromISR Enabled xTimerPendFunctionCall Disabled xTaskAbortDelay Disabled xTaskGetHandle Disabled uxTaskGetStackHighWaterMark2

#### 7.23.3. Advanced settings:

#### Newlib settings (see parameter description first):

USE\_NEWLIB\_REENTRANT Enabled \*

#### Project settings (see parameter description first):

Use FW pack heap file

#### 7.24. LWIP

#### mode: Enabled

Advanced parameters are not listed except if modified by user.

#### 7.24.1. General Settings:

#### **LwIP Version:**

LwIP Version (Version of LwIP supported by CubeMX \*\* CubeMX specific \*\*) 2.1.2

**IPv4 - DHCP Options:** 

LWIP\_DHCP (DHCP Module)

Disabled \*

**IP Address Settings:** 

IP\_ADDRESS (IP Address) 192.168.000.123 \*

Enabled

NETMASK\_ADDRESS (Netmask Address) 255.255.255.000 \*

GATEWAY\_ADDRESS (Gateway Address) 192.168.000.001 \*

**RTOS Dependency:** 

WITH\_RTOS (Use FREERTOS \*\* CubeMX specific \*\*)

CMSIS\_VERSION (CMSIS API Version used)

RTOS\_USE\_NEWLIB\_REENTRANT (RTOS used - 1)

Enabled

**Platform Settings:** 

PHY Driver Choose/LAN8742

**Protocols Options:** 

 LWIP\_ICMP (ICMP Module Activation)
 Enabled

 LWIP\_IGMP (IGMP Module)
 Disabled

 LWIP\_DNS (DNS Module)
 Disabled

 LWIP\_UDP (UDP Module)
 Enabled

 MEMP\_NUM\_UDP\_PCB (Number of UDP Connections)
 4

 LWIP\_TCP (TCP Module)
 Enabled

 MEMP\_NUM\_TCP\_PCB (Number of TCP Connections)
 5

## 7.24.2. Key Options:

#### Infrastructure - OS Awarness Option:

NO\_SYS (OS Awarness)

OS Used

**Infrastructure - Timers Options:** 

LWIP\_TIMERS (Use Support For sys\_timeout) Enabled

Infrastructure - Core Locking and MPU Options:	Facility
SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled
Infrastructure - Heap and Memory Pools Options:	
MEM_SIZE (Heap Memory Size)	16360 *
LWIP_RAM_HEAP_POINTER (RAM Heap Pointer)	0x30044000 *
Infrastructure - Internal Memory Pool Sizes:	
MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1
Pbuf Options:	
PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	12 *
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	16360 *
IPv4 - ARP Options:	
LWIP_ARP (ARP Functionality)	Enabled
Callback - TCP Options:	
TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9
Network Interfaces Options:	
LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled
NETIF - Loopback Interface Options:	
LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
Infrastructure - Threading Options:	
TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	24
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	16360 *
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6

DEFAULT\_ACCEPTMBOX\_SIZE (Default Mailbox Size for Incoming Connections) 6

**Thread Safe APIs - Netconn Options:** 

LWIP\_NETCONN (NETCONN API) Enabled

**Thread Safe APIs - Socket Options:** 

LWIP\_SOCKET (Socket API) Enabled

LWIP\_COMPAT\_SOCKETS (BSD-style Socket Functions Names) 1

LWIP\_SOCKET\_OFFSET (Socket Offset Number) 0

 LWIP\_SOCKET\_SELECT (Select for Socket)
 Enabled

 LWIP\_SOCKET\_POLL (Poll for Socket)
 Enabled

7.24.3. PPP:

**PPP Options:** 

PPP\_SUPPORT (PPP Module) Disabled

7.24.4. IPv6:

**IPv6 Options:** 

LWIP\_IPV6 (IPv6 Protocol) Disabled

7.24.5. HTTPD:

**HTTPD Options:** 

LWIP\_HTTPD (LwIP HTTPD Support \*\* CubeMX specific \*\*)

Disabled

7.24.6. SNMP:

**SNMP Options:** 

LWIP\_SNMP (LwIP SNMP Agent) Disabled

7.24.7. SNTP/SMTP:

**SNTP Options:** 

LWIP\_SNTP (LWIP SNTP Support \*\* CubeMX specific \*\*)

Disabled

**SMTP Options:** 

LWIP\_SMTP (LWIP SMTP Support \*\* CubeMX specific \*\*)

Disabled

#### 7.24.8. MDNS/TFTP:

#### **MDNS Options:**

LWIP\_MDNS (Multicast DNS Support \*\* CubeMX specific \*\*)

Disabled

**TFTP Options:** 

LWIP\_TFTP (TFTP Support \*\* CubeMX specific \*\*)

Disabled

#### 7.24.9. Perf/Checks:

#### Sanity Checks:

LWIP\_DISABLE\_TCP\_SANITY\_CHECKS (TCP Sanity Checks) Disabled LWIP\_DISABLE\_MEMP\_SANITY\_CHECKS (MEMP Sanity Checks) Disabled

#### **Performance Options:**

LWIP\_PERF (Performace Testing for LwIP)

Disabled

#### 7.24.10. Statistics:

#### **Debug - Statistics Options:**

LWIP\_STATS (Statictics Collection)

Disabled

#### 7.24.11. Checksum:

#### **Infrastructure - Checksum Options:**

CHECKSUM\_BY\_HARDWARE (Hardware Checksum \*\* CubeMX specific \*\*) Enabled Disabled LWIP\_CHECKSUM\_CTRL\_PER\_NETIF (Generate/Check Checksum per Netif) Disabled CHECKSUM\_GEN\_IP (Generate Software Checksum for Outgoing IP Packets) Disabled CHECKSUM\_GEN\_UDP (Generate Software Checksum for Outgoing UDP Packets) CHECKSUM\_GEN\_TCP (Generate Software Checksum for Outgoing TCP Packets) Enabled \* CHECKSUM\_GEN\_ICMP (Generate Software Checksum for Outgoing ICMP Packets) Enabled CHECKSUM\_GEN\_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets) Disabled CHECKSUM\_CHECK\_IP (Generate Software Checksum for Incoming IP Packets) Disabled CHECKSUM\_CHECK\_UDP (Generate Software Checksum for Incoming UDP Packets) Disabled CHECKSUM\_CHECK\_TCP (Generate Software Checksum for Incoming TCP Packets) Enabled \* CHECKSUM\_CHECK\_ICMP (Generate Software Checksum for Incoming ICMP Packets) Enabled CHECKSUM\_CHECK\_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets) Disabled

#### 7.24.12. Debug:

LwIP	Main	Debugging	Options:
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LWIP\_DBG\_MIN\_LEVEL (Minimum Level)

ΑII

## 7.24.13. Platform Settings:

Driver\_PHY LAN8742

<sup>\*</sup> User modified value

## 8. System Configuration

## 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	
/.501	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PF4	ADC3_INP9	Analog mode	No pull-up and no pull-down	n/a	
	PF7	ADC3_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PF8	ADC3_INP7	Analog mode	No pull-up and no pull-down	n/a	
	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDI O)	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWC LK)	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB5	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB6	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14- OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM3
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM4
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM5
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM1
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM2
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX
USART6	PG9	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG14	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_ FS	PA8	USB_OTG_FS_ SOF	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USB_OTG_FS_ VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green Led]
	PF13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STEP1_EN
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STEP1_Dir
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STEP1_step
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO4
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO5
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO3
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO2
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STOP
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO1
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_PWR_EN
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS_OVCR
	PE0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	FAULT
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Yellow Led]

### 8.2. DMA configuration

nothing configured in DMA service

### 8.3. BDMA configuration

nothing configured in DMA service

#### 8.4. MDMA configuration

nothing configured in DMA service

# 8.5. NVIC configuration

# 8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	15	0		
System tick timer	true	15	0		
Ethernet global interrupt	true	5	0		
TIM16 global interrupt	true	5	0		
TIM17 global interrupt	true	15	0		
PVD and AVD interrupts through EXTI line 16		unused			
Flash global interrupt		unused			
RCC global interrupt	unused				
EXTI line0 interrupt	unused				
ADC1 and ADC2 global interrupts	unused				
FDCAN1 interrupt 0	unused				
FDCAN2 interrupt 0	unused				
FDCAN1 interrupt 1	unused				
FDCAN2 interrupt 1	unused				
EXTI line[9:5] interrupts	unused				
TIM1 break interrupt	unused				
TIM1 update interrupt	unused				
TIM1 trigger and commutation interrupts	unused				
TIM1 capture compare interrupt	unused				
TIM2 global interrupt	unused				
I2C2 event interrupt	unused				
I2C2 error interrupt	unused				
USART2 global interrupt	unused				
USART3 global interrupt	unused				
TIM8 break interrupt and TIM12 global interrupt	unused				
UART4 global interrupt	unused				
UART5 global interrupt	unused				
TIM6 global interrupt, DAC1_CH1 and	unused				
DAC1_CH2 underrun error interrupts					
Ethernet wake-up interrupt through EXTI line 86		unused			
FDCAN calibration unit interrupt		unused			

Interrupt Table	Enable	Preenmption Priority	SubPriority	
USART6 global interrupt	unused			
FPU global interrupt	unused			
USB On The Go FS End Point 1 Out global interrupt	unused			
USB On The Go FS End Point 1 In global interrupt	unused			
USB On The Go FS global interrupt		unused		
HSEM1 global interrupt	unused			
ADC3 global interrupt	unused			

## 8.5.2. NVIC Code generation

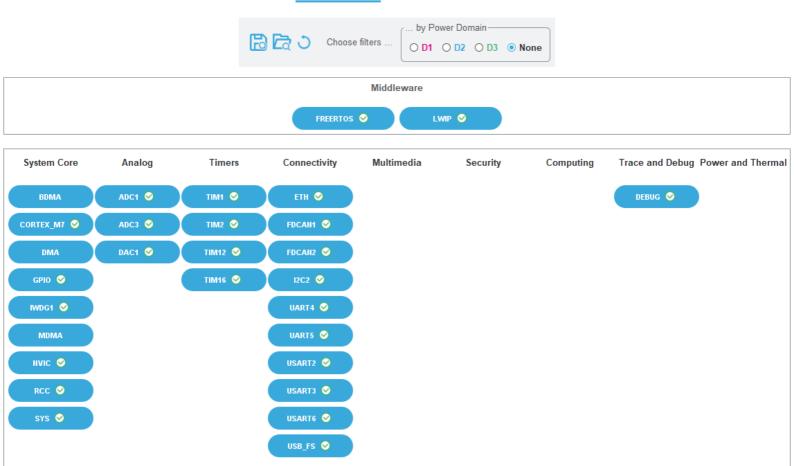
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
Ethernet global interrupt	false	true	true
TIM16 global interrupt	false	true	true
TIM17 global interrupt	false	true	true

<sup>\*</sup> User modified value

# 9. System Views

9.1. Category view

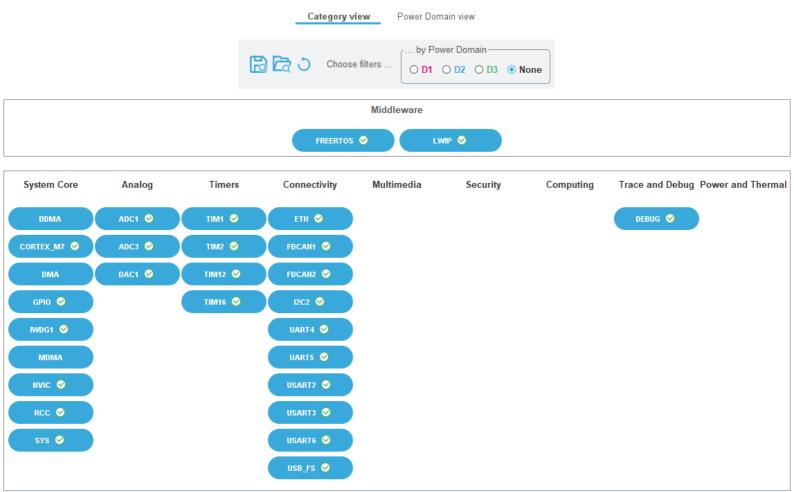
9.1.1. Current



Power Domain view

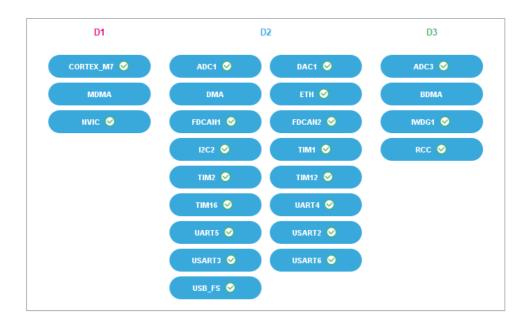
Category view

#### 9.1.2. Without filters



#### 9.2. Power Domain view

Category view Power Domain view



### 10. Docs & Resources

Type Link

Presentations https://www.st.com/resource/en/product\_presentation/microcontrollers\_st

m32h7\_series\_product\_overview.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

stm8\_embedded\_software\_solutions.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32\_eval-

tools\_portfolio.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32\_stm8\_functi

onal-safety-packages.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

stm8\_software\_development\_tools.pdf

Training Material https://www.st.com/resource/en/sales\_guide/sg\_sc2154.pdf

Training Material https://www.st.com/resource/en/training\_certification/faecp\_stm32h7\_dual

core\_edr.pdf

Training Material https://www.st.com/resource/en/training\_certification/faecp\_stm32h7\_edr.

pdf

Brochures https://www.st.com/resource/en/brochure/brstm32h7.pdf

Brochures https://www.st.com/resource/en/brochure/brstm32h7vl.pdf

Flyers https://www.st.com/resource/en/flyer/flnucleolrwan.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32trust.pdf

Flyers https://www.st.com/resource/en/flyer/flpowerstbd.pdf

Application Notes https://www.st.com/resource/en/application\_note/an1181-electrostatic-

discharge-sensitivity-measurement-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an2606-stm32-

microcontroller-system-memory-boot-mode-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an2639-soldering-

recommendations-and-package-information-for-leadfree-ecopack-mcus-

- and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4230-stm32-microcontroller-random-number-generation-validation-using-the-nist-statistical-test-suite-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-

- applications-stmicroelectronics.pdf
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