LAB 3 STRUCTURAL REPORT

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing "yes" at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? <u>Yes</u>

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: <u>N/A</u>

Student Name: Hayden Yu
Student ID: 66185399
Date Completed: 2/19/18
Time Spent: Reviewing Digital Design Material: 2 hours
Design/Preparation Work: 1 hours
VHDL Coding & Debugging: 5 hours

STRUCTURAL OVERVIEW

For this lab, I started with a control word table. In the table, it shows Current States which set the Register File's inputs and outputs, Selector's input for ALU, Shifter, and 2-input Selector, and other output signals. After I completed the table, I watched the corresponding videos for the structural part. The integrator example confused me because the lab 3s' template is completely different than that example. I read other student's questions on the message board, and it cleared some of my confusion. I translated my control word table into the Controller's behavioral code. However, I still spent a long time trying to understand how to implement the controller in the structural code. At first, I followed the integrator's example and tried to come up with equations for each output. Then, I realized that I was making another controller in the structural code. Thus, I connected the signals to corresponding ports for each component. The simulation didn't output what was expected because I didn't connect one of the signals in the Controller component. After I debugged everything, the simulation ran as expected. Therefore, I believe that I 100% completed this lab.

LAB 3 FSMD & CONTROL WORD TABLE
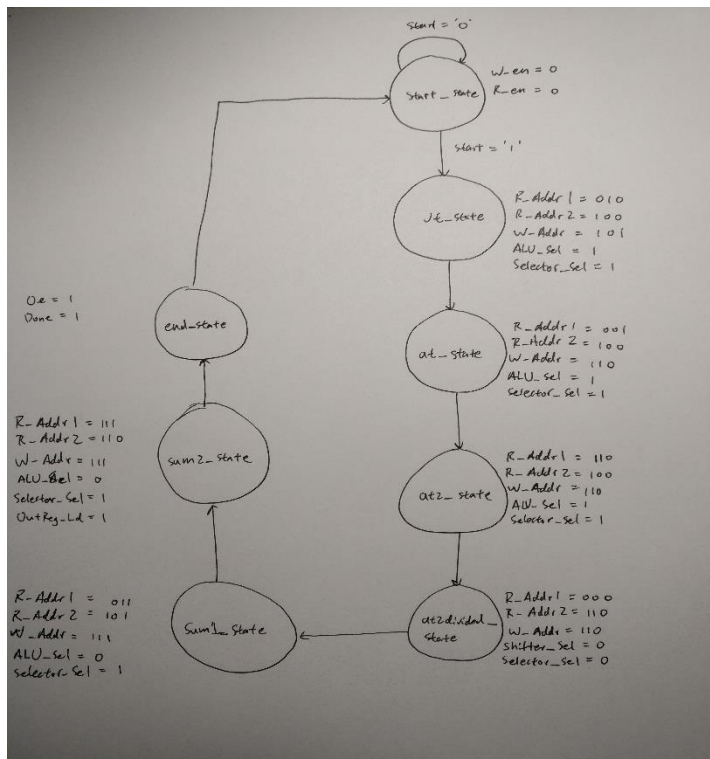
The reason that this FSMD has eight states comparing to the last one which had ten states is the Register File writes the ALU's calculation in the same state. Therefore, it doesn't need an extra state after a calculation.

Control Word Table:

Start	C2	C1	C0		N2	N1	N0		R_EN	W_EN	R_ADDR1	R_ADDR2	W_ADDR	ALU_SEL	SHIF_SEL	SEL_SEL	OUTREG_LD	OE	DONE	
1	0	0	0		0	0	1		0	0	0	0	0	0	0	0	0	0	0	start = 000
0	0	0	1		0	1	0		1	1	010	100	101	1	0	1	0	0	0	vt = 001
0	0	1	0		0	1	1		1	1	001	100	110	1	0	1	0	0	0	at = 010
0	0	1	1		1	0	0		1	1	110	100	110	1	0	1	0	0	0	at2 = 011
0	1	0	0		1	0	1		1	1	000	110	110	0	0	0	0	0	0	at2/2 = 100
0	1	0	1		1	1	0		1	1	011	101	111	0	0	1	0	0	0	sum1 = 101
0	1	1	0		1	1	1		1	1	111	110	111	0	0	1	1	0	0	sum2 = 110
0	1	1	1		0	0	0		0	0	0	0	0	0	0	0	0	1	1	end = 111

LAB 3 MINIMUM CLOCK CYCLE

Minimum clock cyle: 38 ns

StateReg (5 ns) + CombLogic (11 ns) + RegFile (7 ns) + ALU (12 ns) + Selector (3 ns) = 38 ns
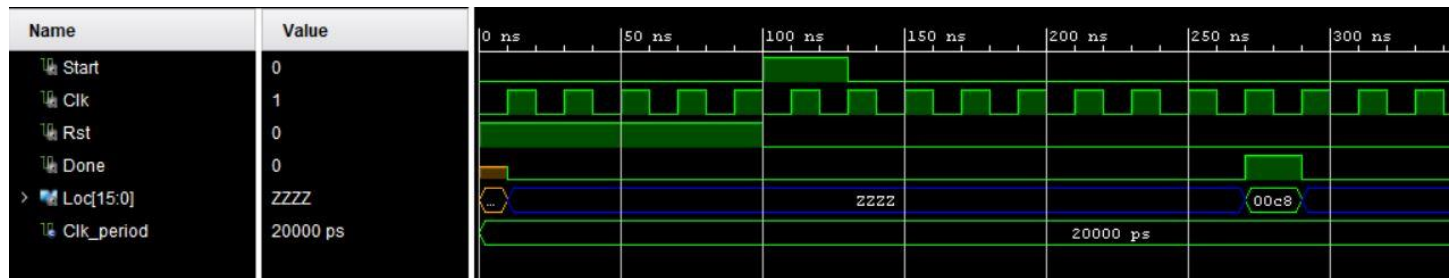
LAB 3 STRUCTURAL SIMULATION GRAPH
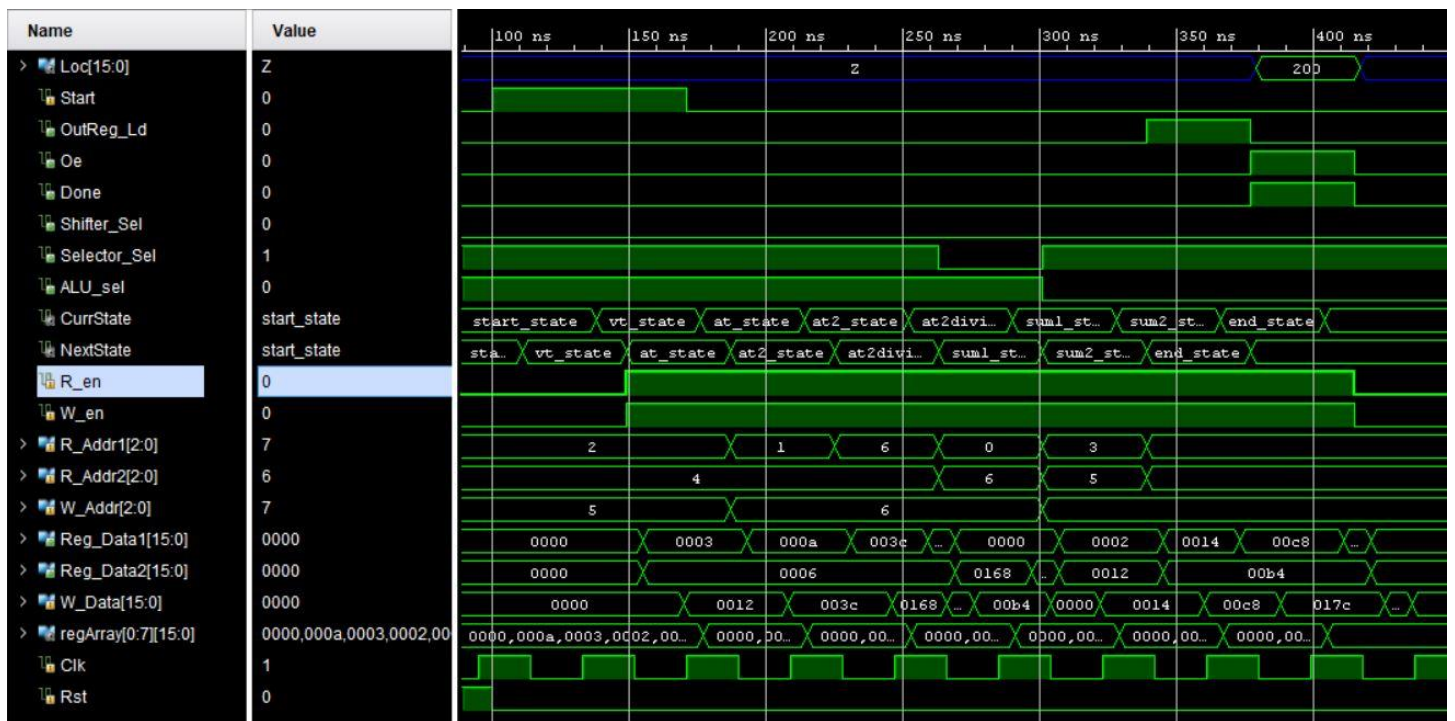
For the testbench, I set the input, 'Start', to '1'. It waits until the next rising edge and, after 20ns, 'Start' will set back to '0'. This will trigger the calculation in the structural architecture. It will first go through the State Register and Controller, and then the calculation from the ALU or Shifter will be stored in the Register File. After it goes through all states, 'Loc' should output 200, and 'Done' and 'Oe' should output '1', which they did. Thus, the simulation ran successfully.
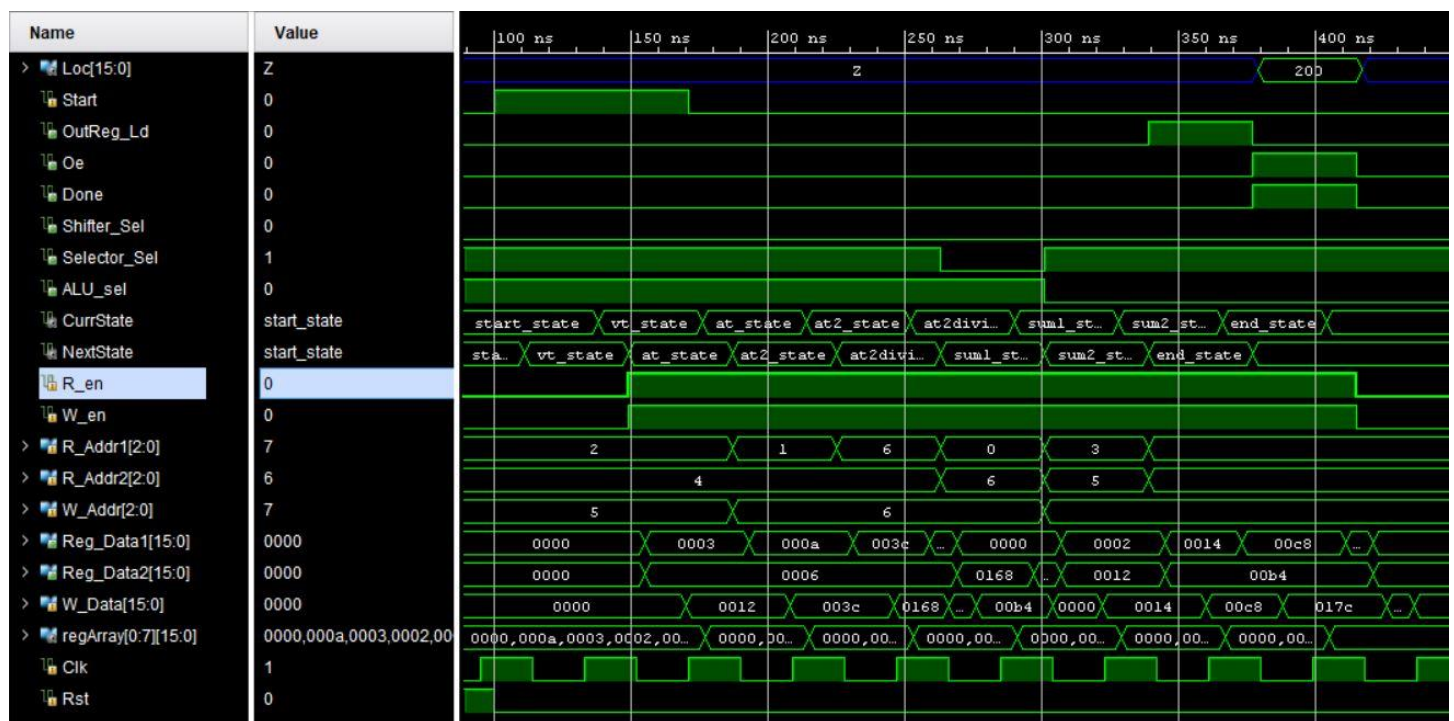
Compare your behavioral & structural graphs here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

Behavioral:

Structural:

The structural simulation took longer to run because the clock cycle needs to account for all delays in each component. In the behavioral simulation, the clock cycle was only an estimation.