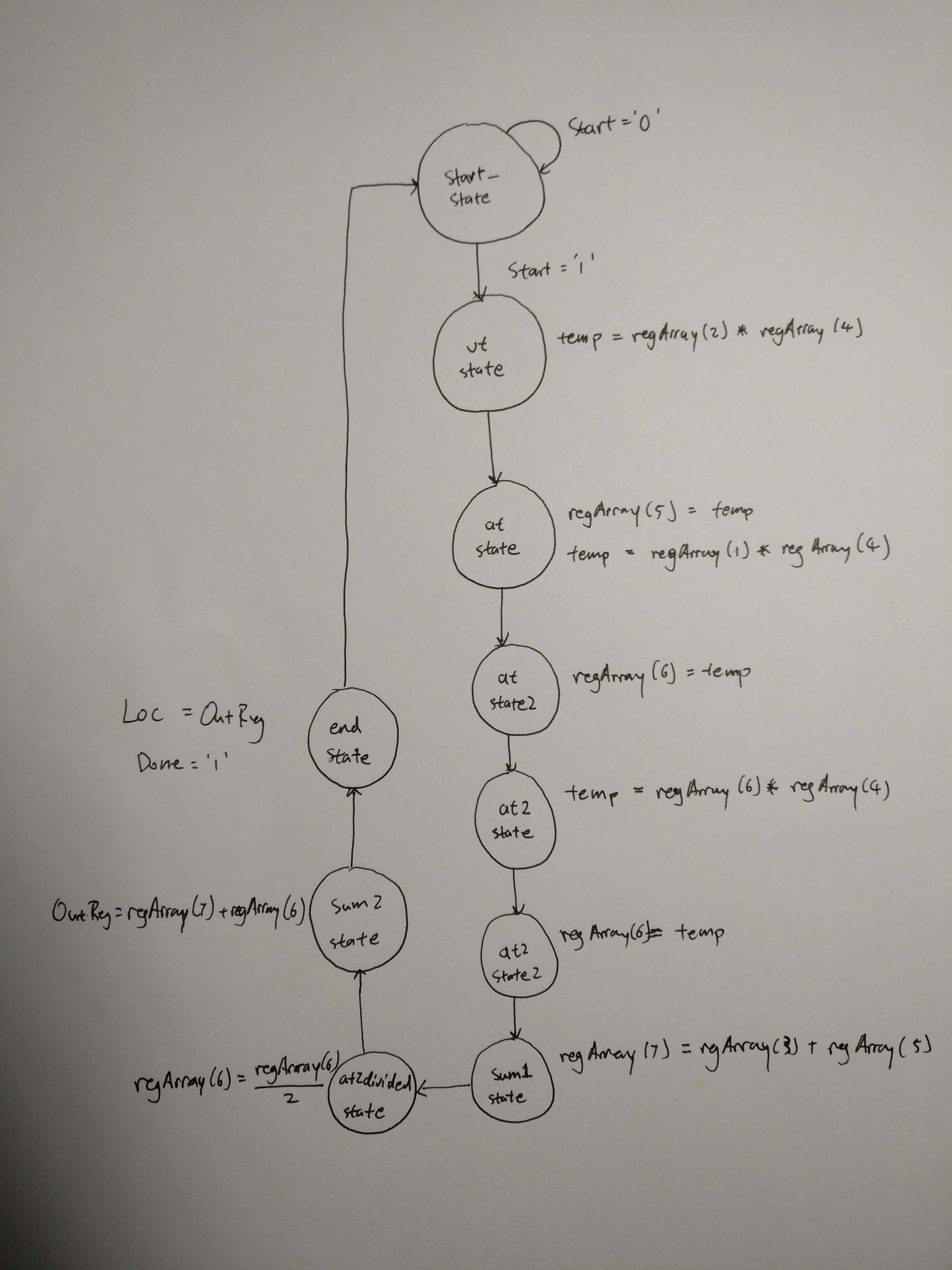
# Lab 3 Behavioral Report

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Date Completed: 2/11/18  
Time Spent: Reviewing Digital Design Material: 1 hour  
 Design/Preparation Work: 1 hour  
 VHDL Coding & Debugging: 3 hours

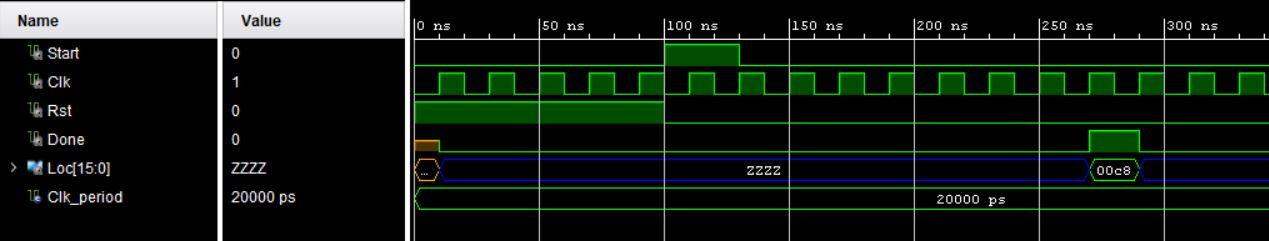
## Behavioral Overview

I started this lab with a rough sketch of the FSMD and a table for the regArray. After I figured out what I want to do in each, I watched the videos corresponded to lab 3. The most helpful one was the Integrator Example, because it explains how to translate the FSMD into Xillinx’s syntax. I also read the message board because the videos didn’t explain those parts. Then, I translated my FSMD, and when I ran the simulation, ‘Loc’ output XXXX. I looked the outputs other each state and I found out that temp is stored in the regArray after one clock cycle. Thus, I added one state after each time I used temp. I ran many simulations, and I finally figured out the correct number of states I needed for this calculation to run successfully. When I obtain my desired result, I redrew my FSMD which in under LAB 3 FSMD. Therefore, I feel that I 100% completed the lab.

## Lab 3 FSMD



## Lab 3 Behavioral Simulation Graph



For the testbench, I set the input, ‘Start’, to ‘1’. It waits until the next rising edge and, after 20ns, ‘Start’ will set back to ‘0’. This will trigger the calculation in the behavioral architecture. Then it will run through the states, and during each state, a certain number will be calculated and stored in the regArray. When it’s done with the calculation, ‘Loc’ will output the result which is 00c8 in hexadecimal and 200 in decimal. If we plug in the same numbers in the equation, the result is also 200. Thus, my testbench ran successfully.