Metropolitan State University

ICS 232 Computer Organization & Architecture
Homework 2 Digital Design 60 points
Due Date: 02/24/2019

Name:

Note: Please post your homework to ICS232 D2L on or before the due date.
If you do not post your homework on or before the due date, please post your late homework when complete (Late Homework: -15% Penalty).

1. (5 pts) Define the following
   a. Combination Logic: It is a combination of inputs which lead to output. Two identical inputs into the two logically identical functions will lead to the same output.
   b. Sequential Logic: It is the same as combinational Logic except that Sequntial Logic has memory.
   c. How are sequential circuits different than combinational circuits? In sequential logic the output is not totally dependent on the input. The output is affected by the memory states.
2. (5 pts) Add the following 8-bit two's complement numbers (i.e. one sign bit and seven data bits) AND indicate "Overflow" if it occurs.

		1110 1100	Carry bits	
Example:		0101 0110		86
	+	0011 0110		+54
Answer:	0	1000 1100	(-116)	140

Overflow: A Positive Number + a Positive number cannot be a Negative number

a. 1111 0111
+ 1101 0101
Answer: 1001100

b. 1111 1111
+ 0111 0101
Answer: 1 1 0100

c. 0110 1111
+ 0101 0101
Answer: 1009100

overflow when adding the two most significant bits

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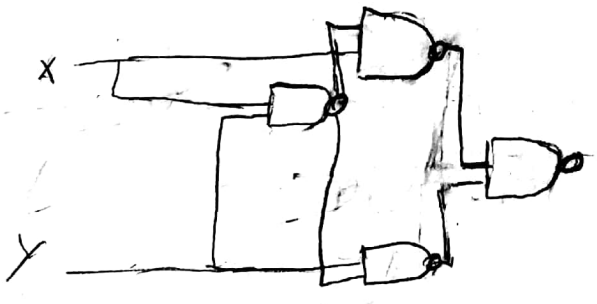
3. (5 pts) Construct a truth table for the following:
   xyz + x(yz)' + x'(y+z) + (xyz)'

x	y	z	F(xyz)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

4. (5 pts) Construct a truth table for the following:
   (x + y')(x' + z')(y' + z')

x	y	z	F(xyz)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

5. (5 pts) Construct the XOR operator using only NAND gates. Hint: x XOR y = ((x' y)' (xy')')'



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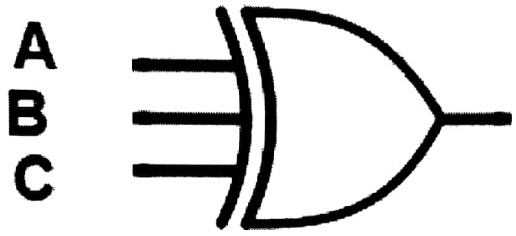
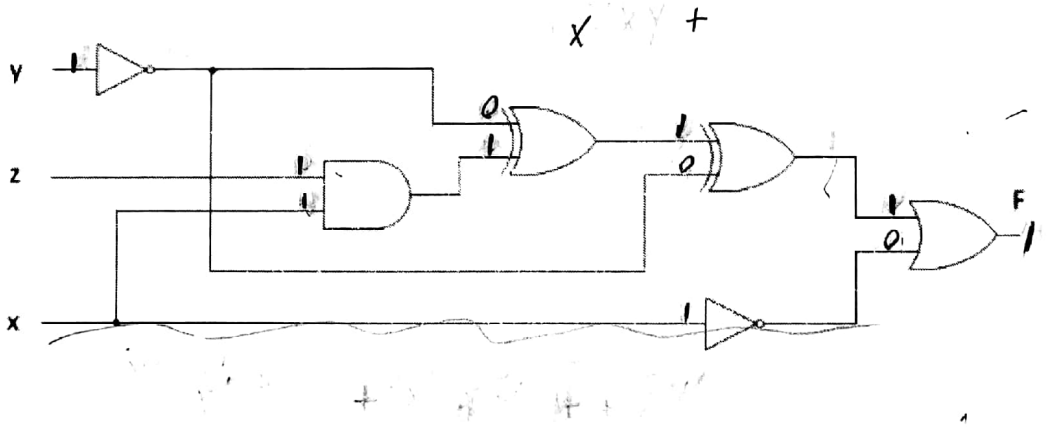
6. (5 points) Construct a truth table for a (3) three input XOR gate.



A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

7. (5 pts) Given the following circuit:



a. Define the boolean equation for the output function F(xyz)

$X' + Z$

b. Define the truth table for the output function F(xyz)

x	y	z	F(xyz)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

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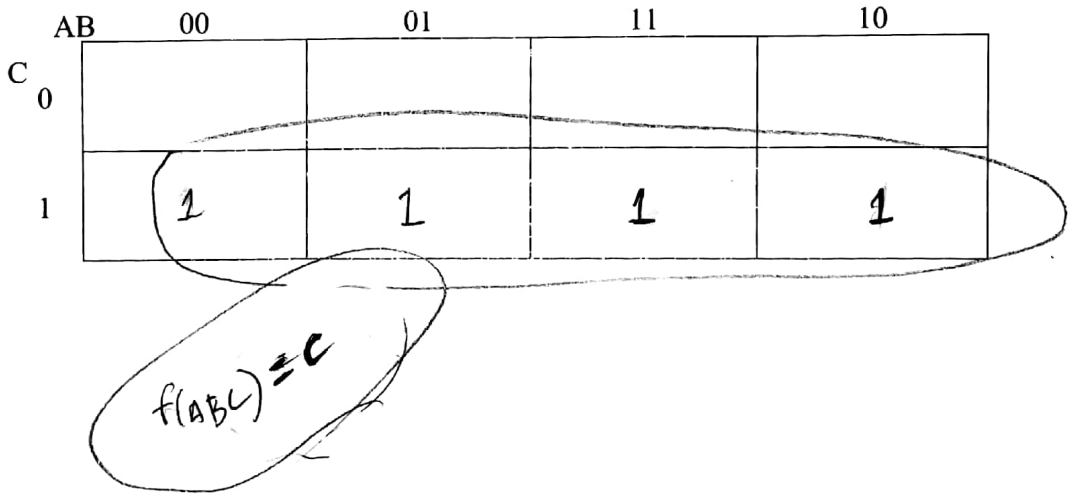
8. (5 pts) Given the truth table below:

A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

a. Write out the SOP (Sum-of-Products) minterm Boolean equation.

$ABC + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}BC$

b. Construct the K-map for this circuit.



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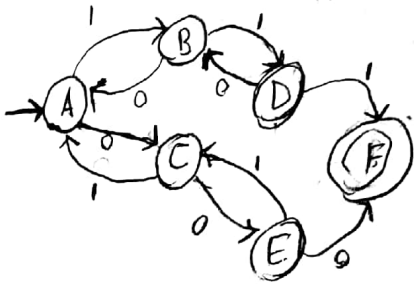
9. (5 points) Define the deterministic finite automata (DFA) computational model and each term in the quintuple M=(Q, S, Σ, δ, F)

DFA model:



Q: {A, B, C, D, E, F}

S: {A}

Σ: 0 or 1

δ:

	0	1
A	C	B
B	A	D
C	E	A
D	B	F
E	F	C

F: ={F}

10. (5 pts) Define the following terms as they pertain to Latches and Flip-Flops.
Note: The book does not cover these definitions very well. Please visit:
https://en.wikipedia.org/wiki/Flip-flop_(electronics)#JK_flip-flop

a. Metastability

the horizontal represents time & the vertical portion represents voltage

When this happens →  instead of this → 

b. Propagation Delay

It is time slot which seperates input time and output time.

c. Setup Time

Amount of time the input data must remain stable. This is necessary to prevent input mix up. This is a tool to segregate inputs

d. Hold Time

Amount of time after clock is active, which the input data must remain stable. This is necessary to segregate inputs into the correct order of being inputted.

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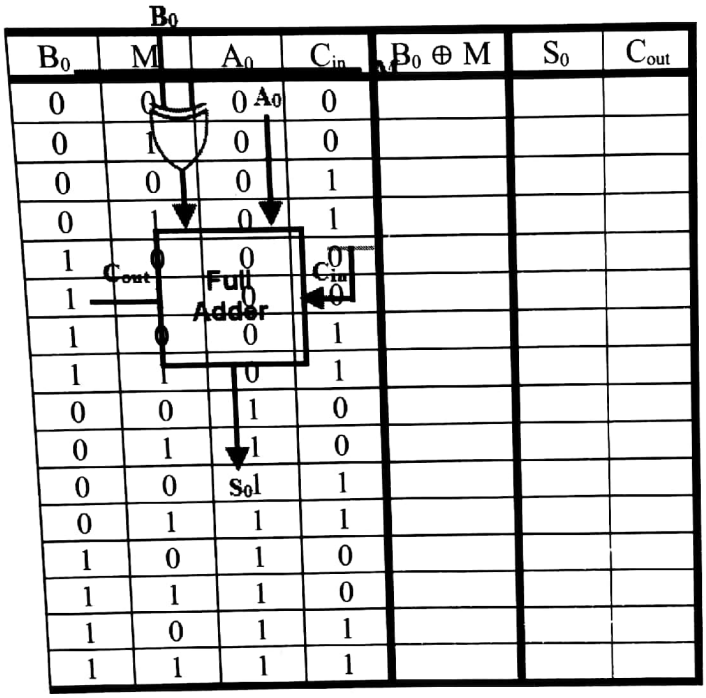
11. (5 pts) Construct the truth table for given the circuit below:



B_0	M	A_0	C_{in}	$B_0 \oplus M$	S_0	C_{out}
0	0	0	0			
0	1	0	0			
0	0	0	1			
0	1	0	1			
1	0	0	0			
1	1	0	0			
1	0	0	1			
1	1	0	1			
0	0	1	0			
0	1	1	0			
0	0	1	1			
0	1	1	1			
1	0	1	0			
1	1	1	0			
1	0	1	1			
1	1	1	1			

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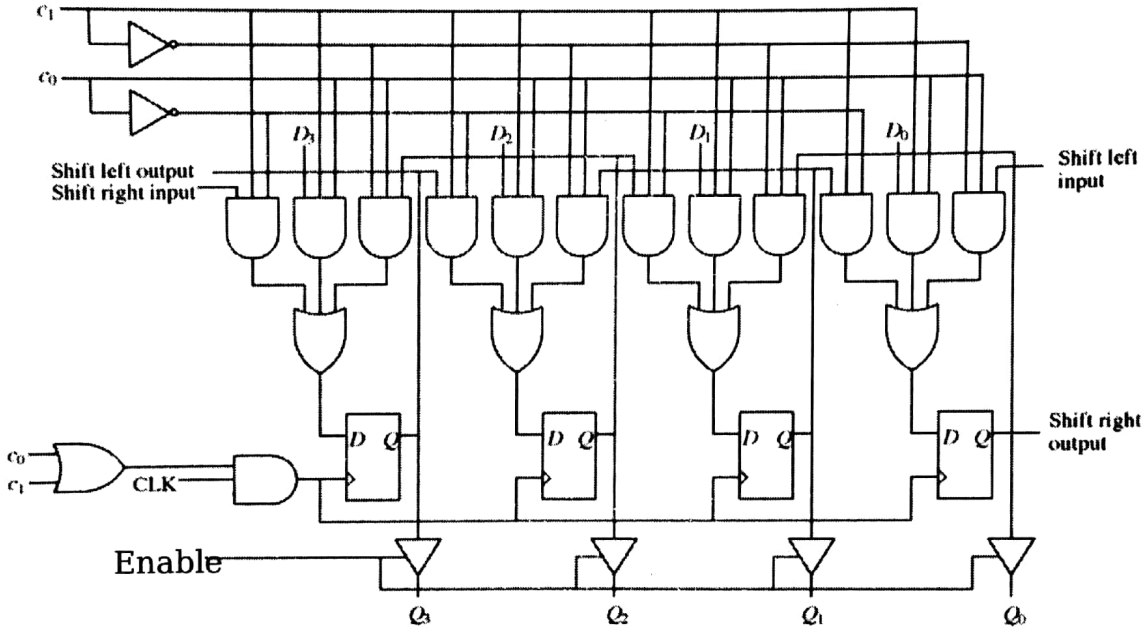
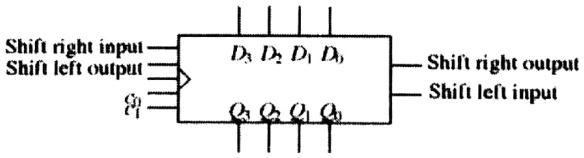
12. (5 pts) Given the left-right shift register shown below answer the following questions. Place an 'x' for don't care conditions on the non-relevant outputs.
Note: Each Control input 'c0 and c1' as listed in the function table is shown twice in the diagram.



Control c_1	Control c_0	Function
0	0	No change
0	1	Shift left
1	0	Shift right
1	1	Parallel load



a. Fill in the shift output table below for the clocks Clk_1-to-Clk_4 given the following parallel load input to the shift register on clock Clk_0. Place an 'x' for don't care conditions on the non-relevant outputs.

Clk_0

D_3	D_2	D_1	D_0	C_1	C_0
1	1	0	1	1	1

Clk_1-to-Clk_4

	Clk_1	Clk_2	Clk_3	Clk_4	c_1	c_0
Shift Right Output					1	0
Shift Left Output						

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b. Fill in the state output of Q_0-to-Q_3 on clock Clk_4 given the input 'Enable=1' AND the following Input serial load of the shift-register in clocks Clk_0-to-Clk_3

Clk_0-to-Clk_3

	Clk_0	Clk_1	Clk_2	Clk_3	C_1	C_0
Shift Right Input	0	1	0	0	1	0
Shift Left Input	1	0	1	1		

Clk_4

Q_3	Q_2	Q_1	Q_0	C_1	C_0	Enable
				0	0	1