1 Introduction

A receiver is a device that receives signals and converts the information to a useable form. The receiver undo the operations done by the transmitter. The receiver chain is shown in figure 1.

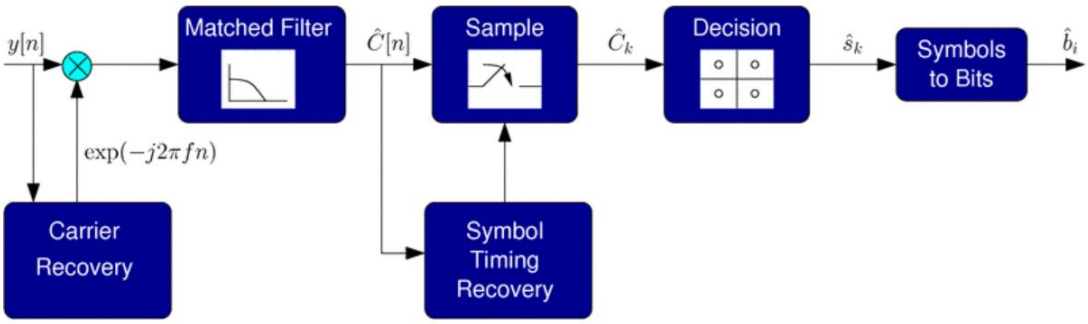


Figure 1: Receiver chain of complex signal

Down conversion

The transmitted signal, which was up converted to a higher frequency, is shifted down to the baseband by multiplying the conjugate of the carrier ($e^{-j2\pi fn}$) to the received signal.

Matched filter

Matched filter is a filter for extracting the desired message from a signal contaminated by noise, hence maximizing signal to noise ratio (SNR). In the receiver, matched filter is applied to reduce noise and remove image at double carrier frequency.

Sample

The wave needs to be sampled at optimal points to get similar I/Q symbol.

Decision

The decision block decides which symbol is more likely to be similar to the original symbol. Decision is needed because there is noise in received signal.

Symbol to bits

The recovered symbol is converted back to bits.

Carrier Recovery

The received and transmitted carrier signal has a frequency difference and a phase offset due to instability of oscillator, Doppler effect, transmission delay, noise and so on. Therefore carrier recovery is needed to correct the phase and frequency offset at the receiver. In Simulink, this can be done by putting a pilot tone' in the transmit signal. Carrier recovery is usually done by using phase-locked loop (PLL).

Symbol timing recovery

The receiver must have the exact symbol timing to have a proper demodulated recovery of signal. This is done by locking PLL to rising and falling edges of the waveforms.

2 Execution/Evaluation

Creating a subsystem

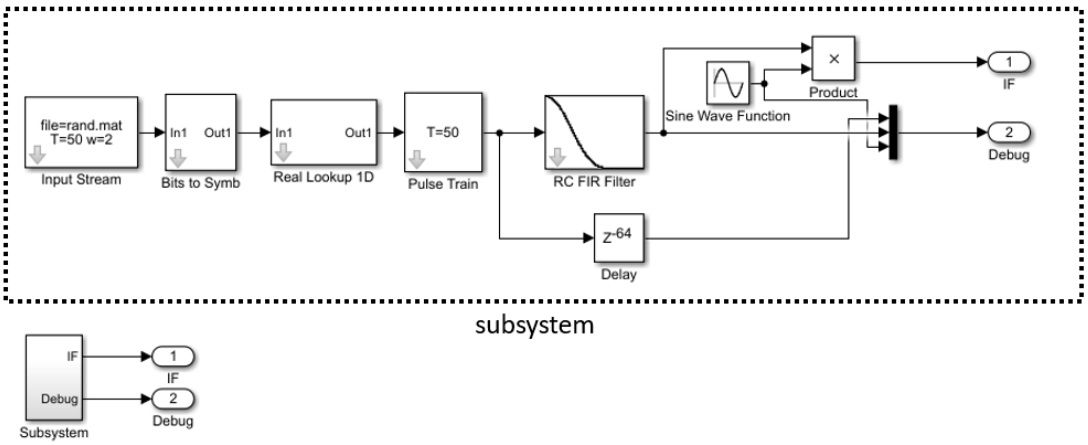


Figure 2: Simulink setup 1

The transmitter part of BPSK is put into a subsystem

Basic BPSK receiver

Check-off 1: The recovered signal has the same shape as the transmitted one, which shows a correct symbol to bits transformation.

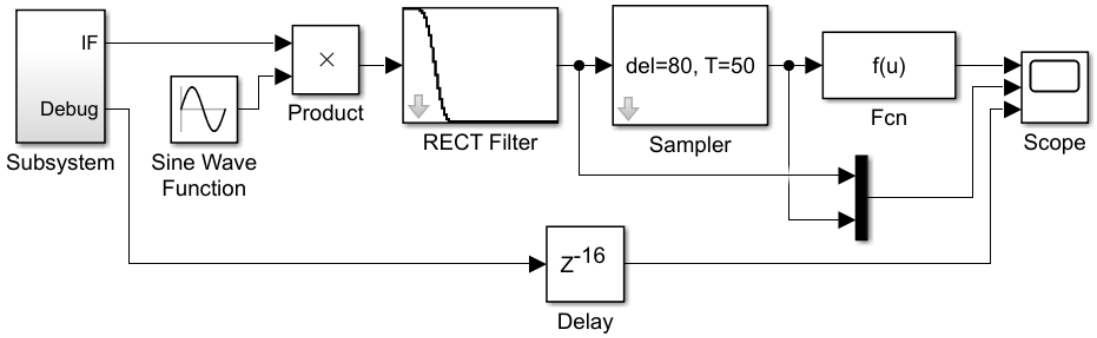


Figure 3: Simulink setup 2

Sine wave has the same frequency ($2 \cdot \pi \cdot 0.1$) of the sine wave of the transmitter. RECT filter has low cut-off of 0, high cut-off of 0.1 and filter taps of 32. The delay was applied because to match the delay produced by RECT filter. The decision block is Fcn block with function of $(u(1) > 0) \cdot 1 + (u(1) \leq 0) \cdot 0$. u(1) represents the input sample, therefore the decision block only returns positive terms.

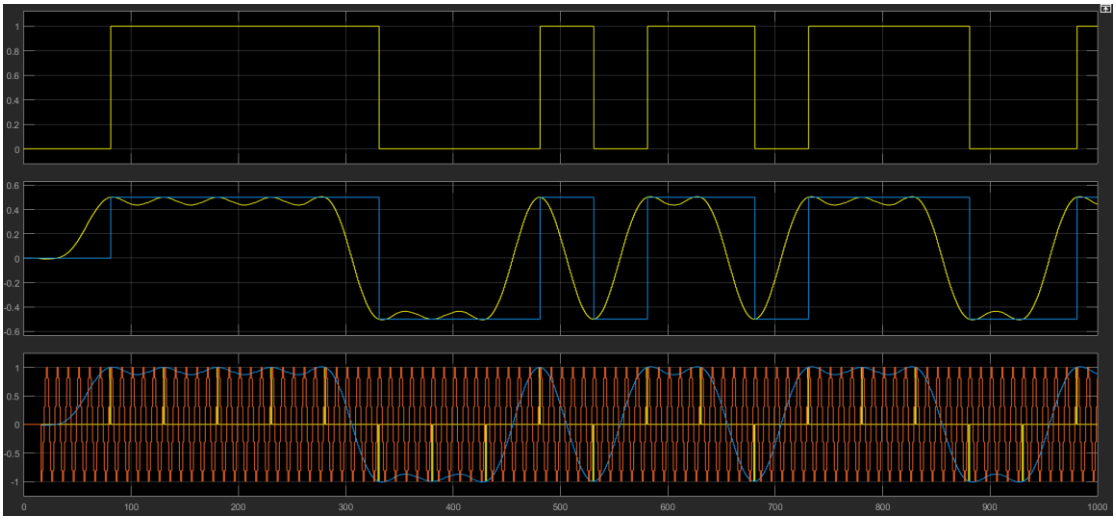


Figure 4: Output setup 2

The upper graph gives the recovered received signal.
The middle graph shows the down converted filtered received baseband signal (yellow) and sampled signal (blue).
The bottom graph shows the transmitted signal
Carrier (red) pulse train (yellow) baseband signal (yellow)

Matched Filtering

The filter block of the receiver was changed to the same one to the transmitter filter block (RC filter)

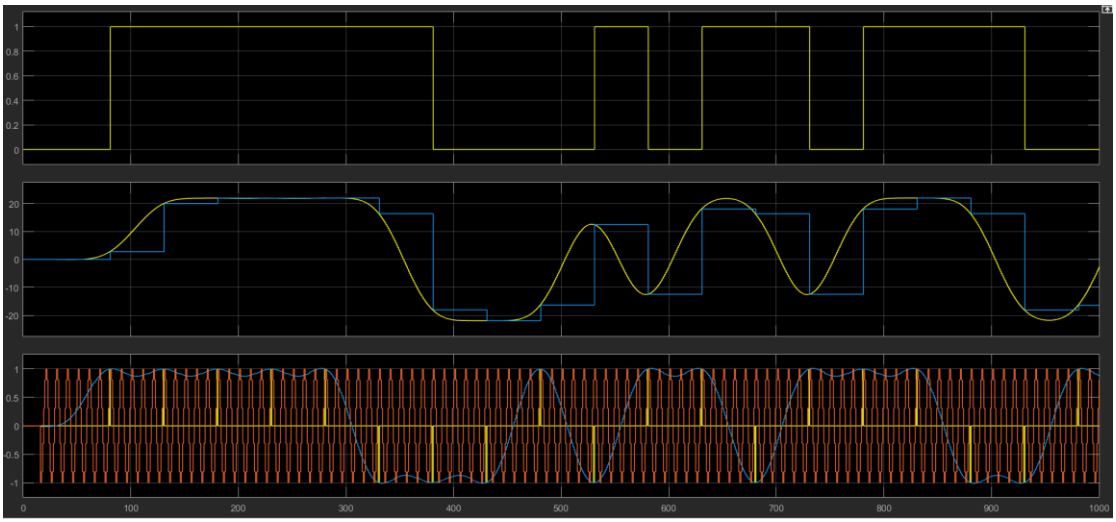


Figure 5: Output with matched RC filter

Root raised-cosine matched filter

The filter in both transmitter and receiver has be set to root raised cosine filter which takes the square root of RC response in frequency domain. Filter taps are set as 512.

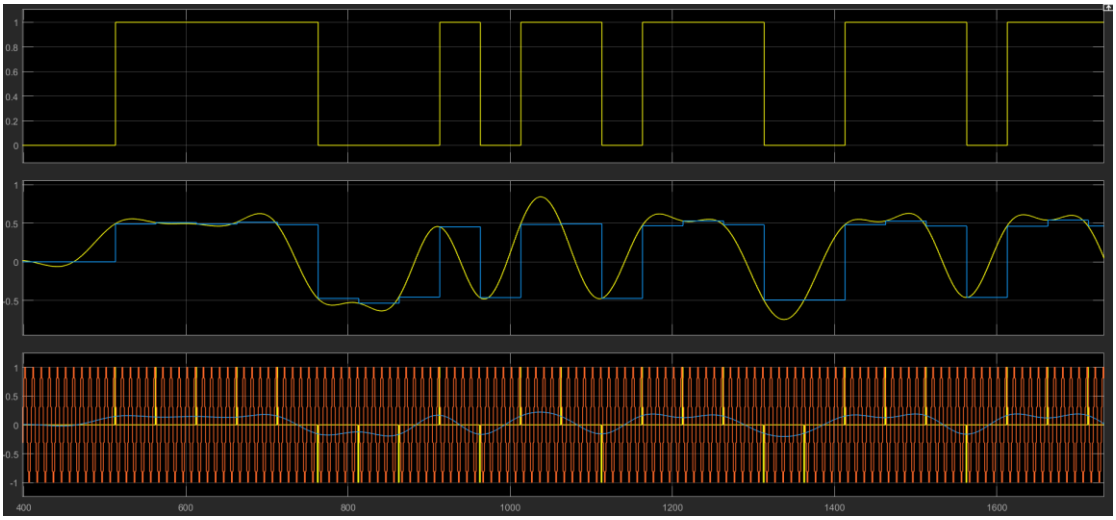


Figure 6: Output with matched RRC filter

By using root RC filter both in transmitter and receiver, the cascade response is a RC filter. Therefore both transmitter and receiver have matched filters.

Carrier Recovery

Check-off 3:

Because the receiver and transmitter oscillator are different in real world, the carrier is different. The transmitter sine block was modified with external time reference and added clock and delay. The pilot tone is added to the transmit signal for easier recovery of the receiver. Pilot tone of sine wave with frequency $2 \cdot \pi \cdot 0.05$, amplitude 0.05, phase 0 is added. To isolate pilot tone in the receiver, RECT filter is added with f0 = 0.03, f1 = 0.08 and 80 taps.

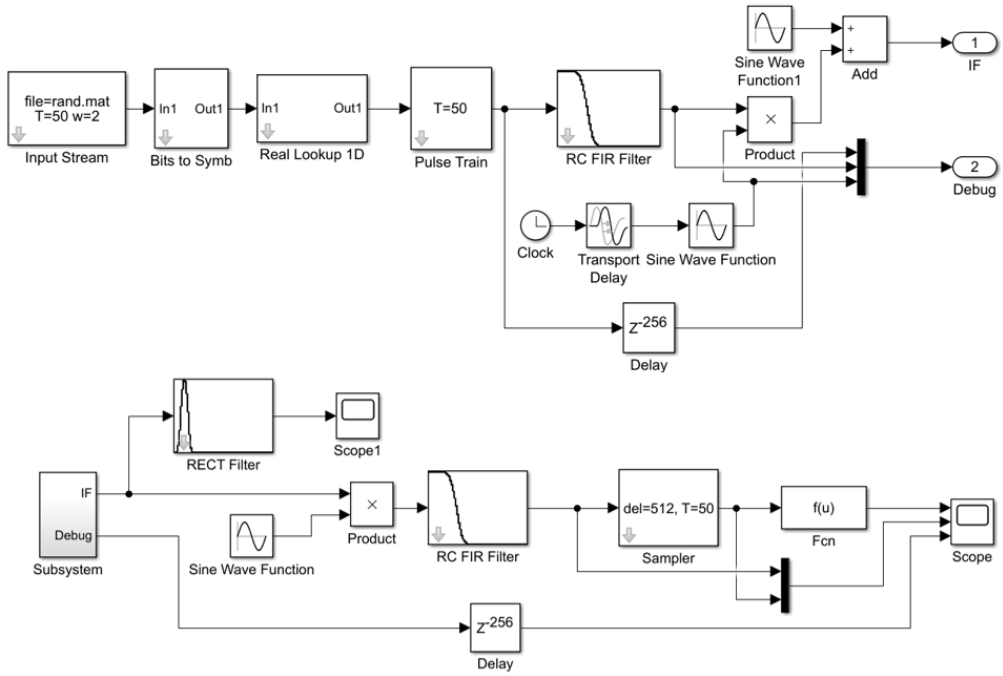


Figure 7: Simulink setup 3

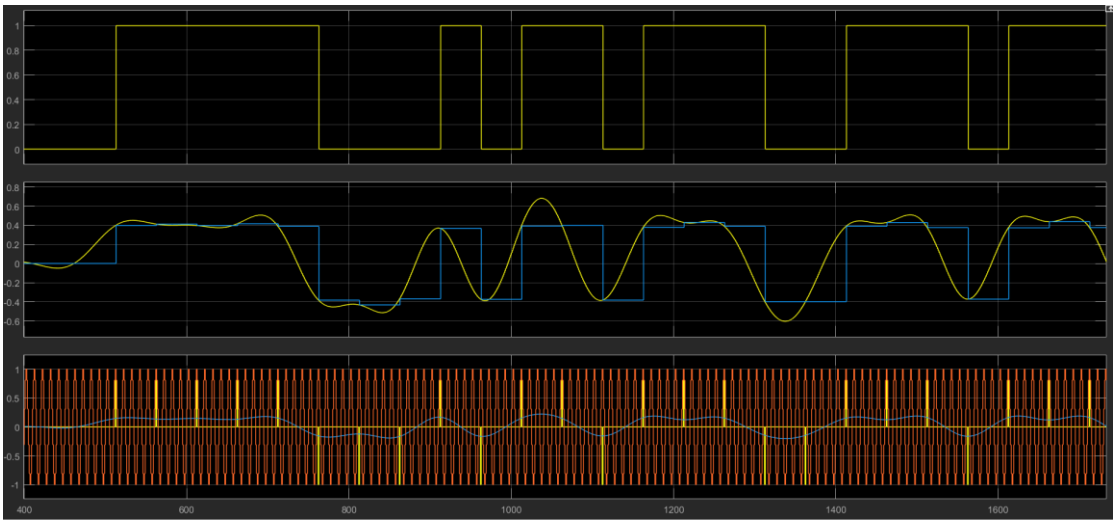


Figure 8: Output setup 3

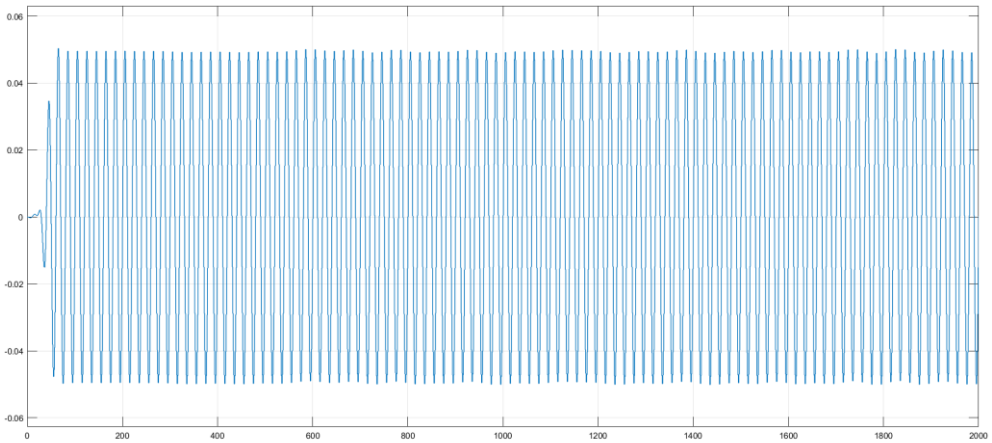


Figure 9: RECT filter scope setup 3

PLL – based Synchronization

Check-off 2: At a frequency of 0.055 Hz (Slightly deviating from 0.05 Hz), a small phase shift can be perceived.

To put the recovered carrier signal to the receiver, PLL is used. PLL generates a output with a phase related to the phase of the input. Here, it takes a sine wave as input and tracks its phase using a loop. The PLL block is set with the following setup:

Input frequency (f_{in}) 0.05, output frequency (f_{out}) 0.05, output amplitude (amp) 1, damping factor (x_i) 1, loop time constant (samples) 500, output phase (phi) 0.

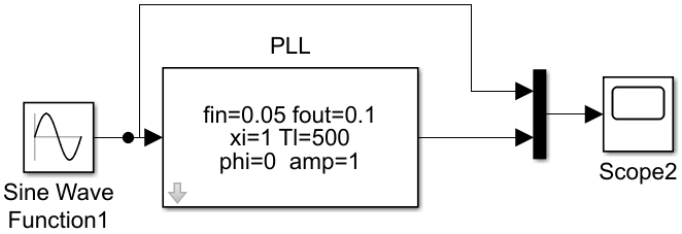


Figure 10 Simulink setup 4 PLL

1) Source frequency of 0.05

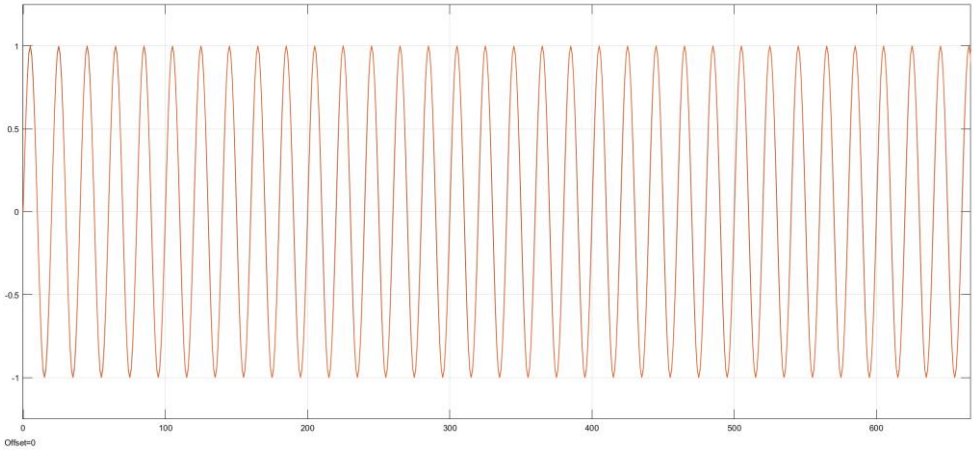


Figure 11: PLL scope setup 1)

Input and output sine wave are the same. (In phase)

2) Amplitude of input source of 2

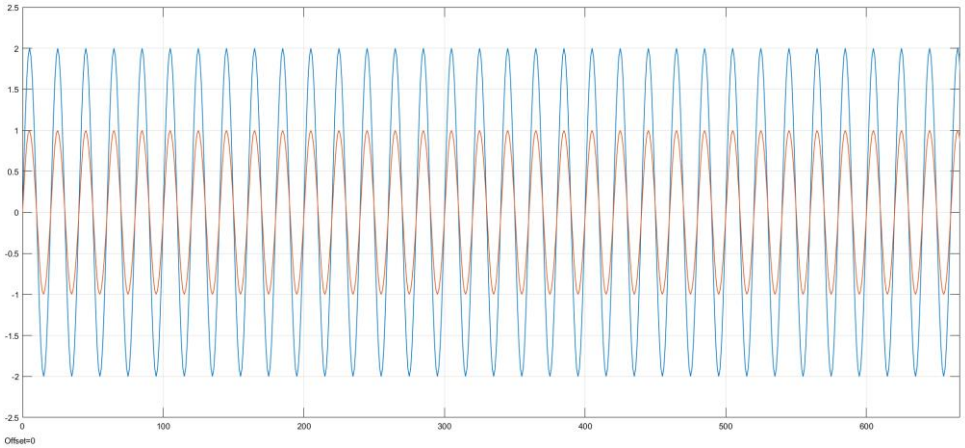


Figure 12: PLL scope setup 2) Blue – input, Red – output

Amplitude didn't affect the output of the PLL because it is in the same phase.

3) Source frequency of 0.055

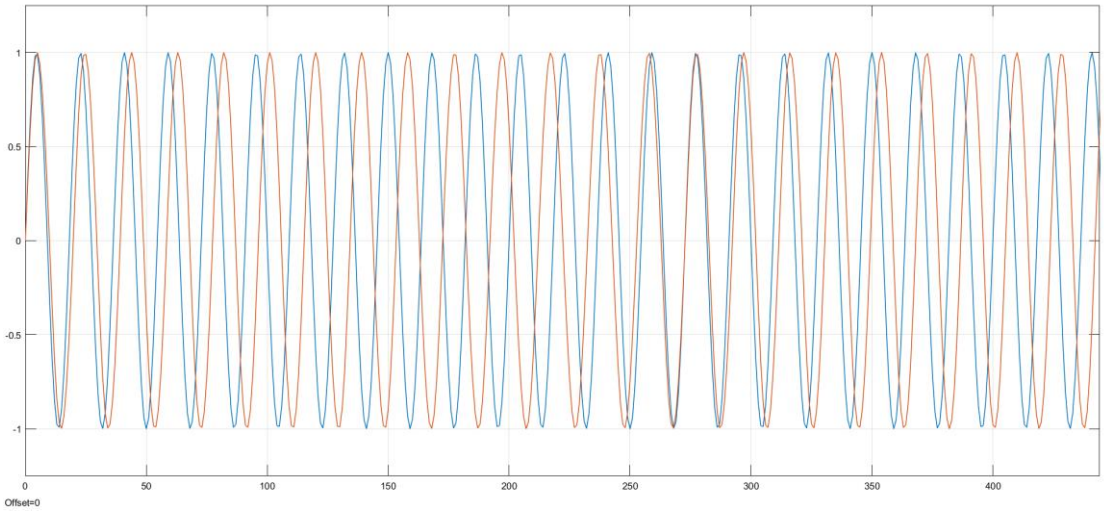
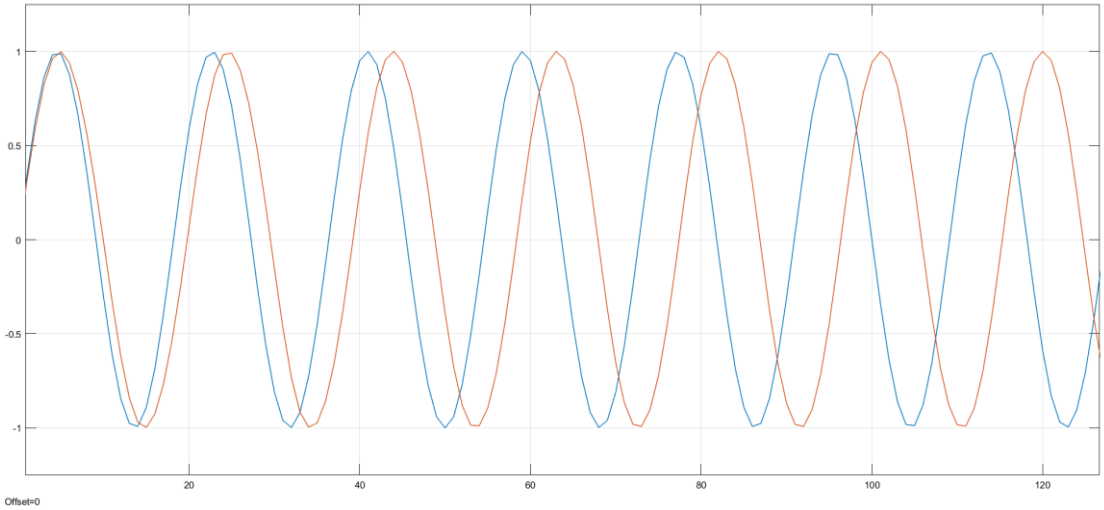


Figure 13: PLL scope setup 3-1) Blue – input, Red – output



Source frequency of 0.45

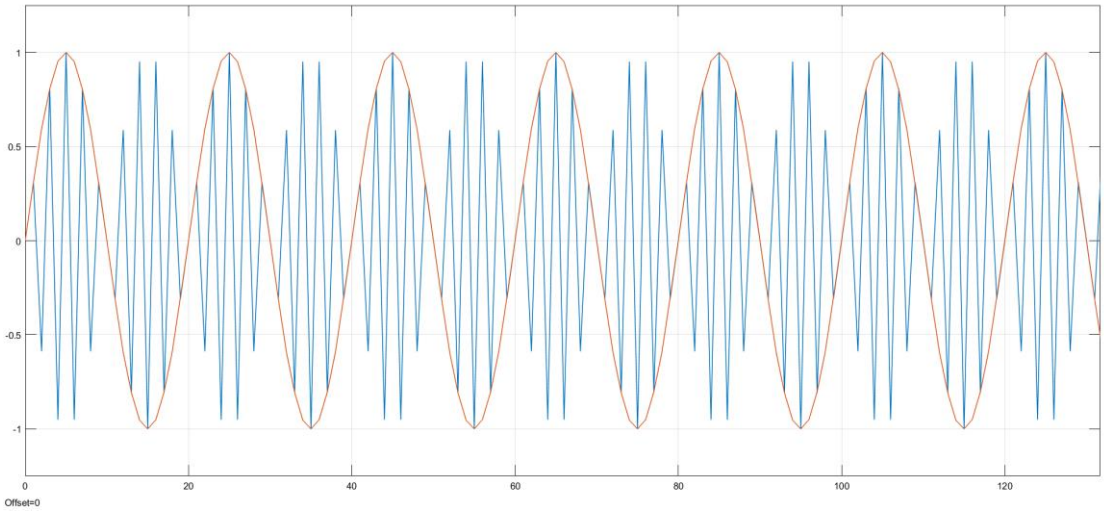


Figure 14: PLL scope setup 3-2) Blue – input, Red – output

4) Output frequency 0.1

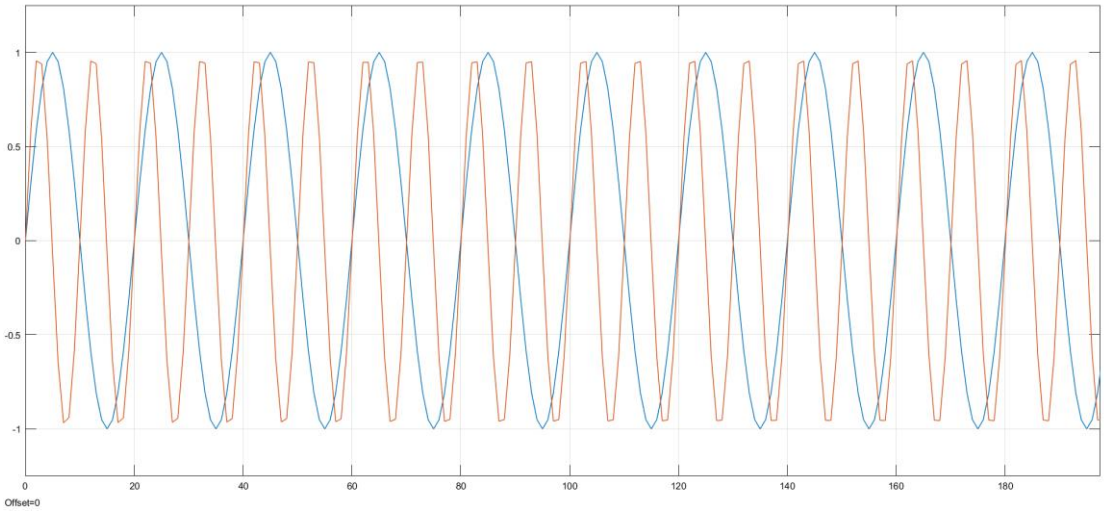


Figure 15: PLL scope setup 4-1) Blue – input, Red – output

Output frequency 0.025

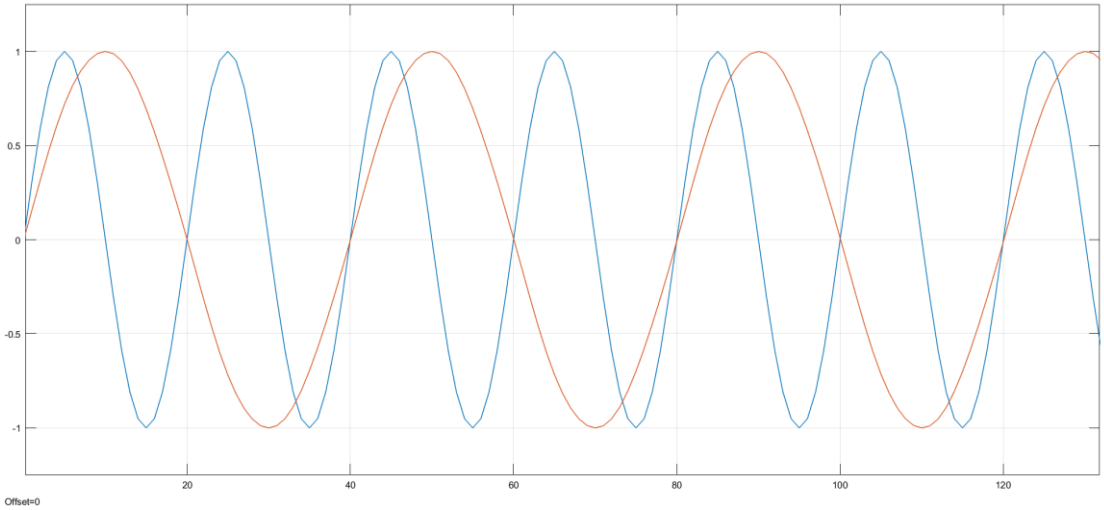


Figure 16: PLL scope setup 4-2) Blue – input, Red – output

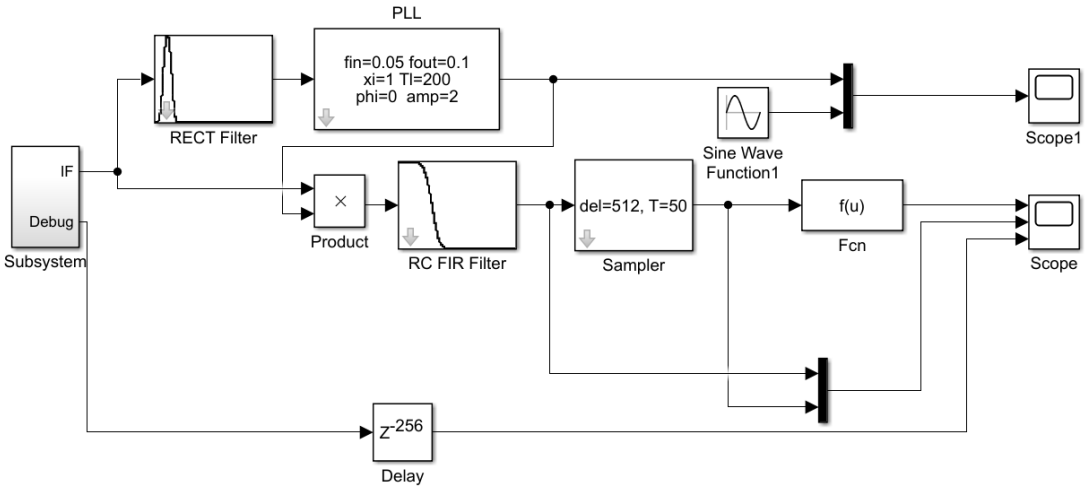


Figure 17: Simulink setup 5

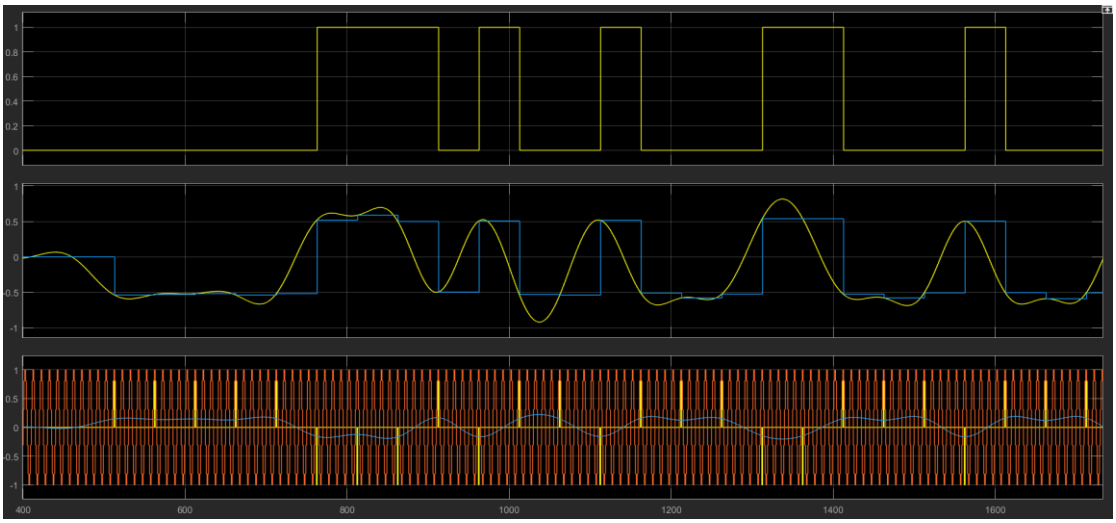


Figure 18: Output setup 5

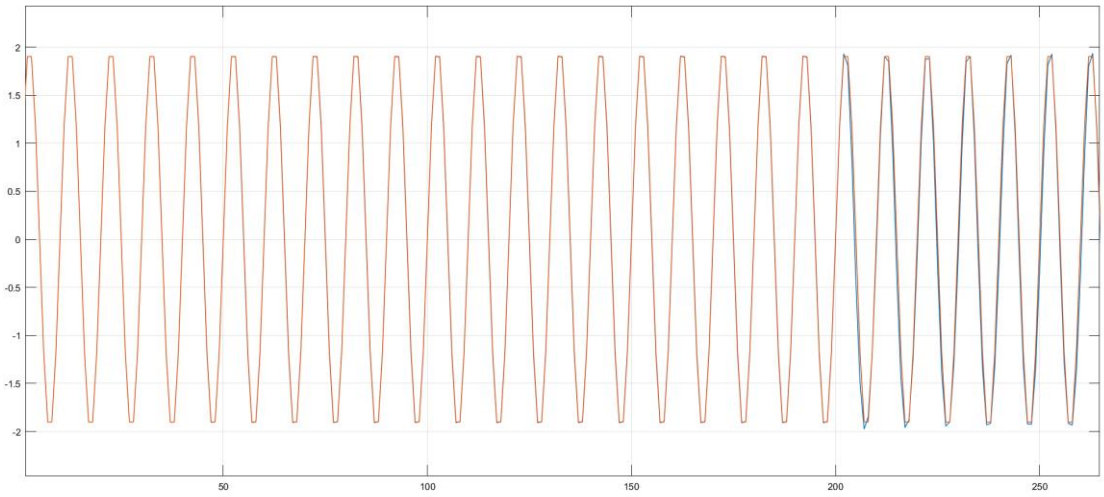


Figure 19: PLL Scope setup 5

Symbol time recovery

Check-off 4: Inside the symbol timing recovery block, there is a PLL that enables us to recover the exact symbol timing.

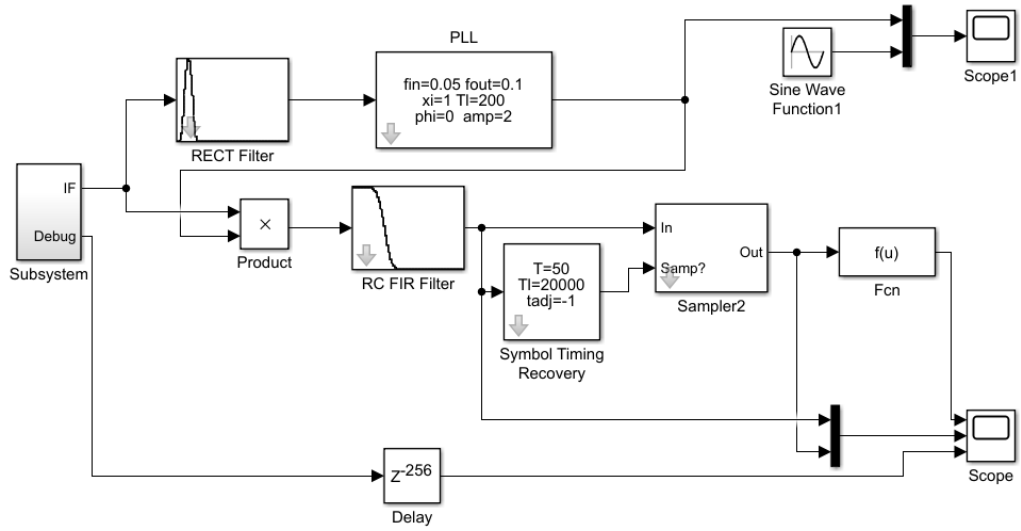


Figure 20: Simulink setup 6

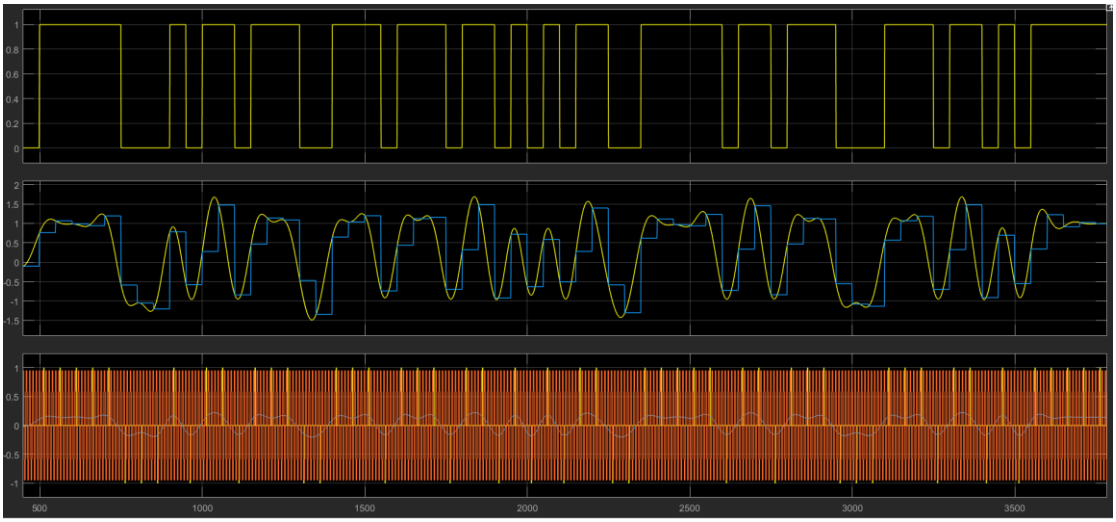


Figure 21: Output setup 6

Noise

There is always unwanted noise in real life communications. Noise level is quantified by signal-to-noise (SNR) ratio, usually values about 10dB or better are required to recover the signal. To consider the noise, the band-limited white noise black had been added. The noise power was set to 0.001, sample time was set to 1 for the noise block parameters – which gives an SNR around 15dB. The graph was shown similar as before, therefore the symbols are decoded properly. When the noise was set to a higher value (i.e. 0.1), the graph was distorted completely and shows a complete different symbol. Shown in figure 24. Therefore if there is too much noise, the signal is distorted and cannot be recovered.

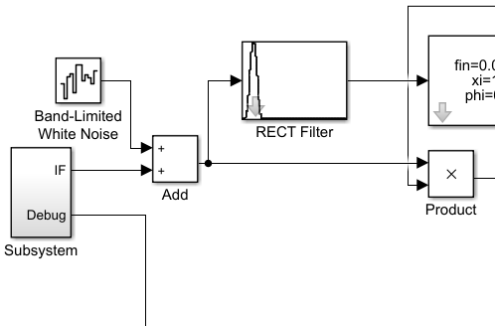


Figure 22: Simulink setup 7 - noise

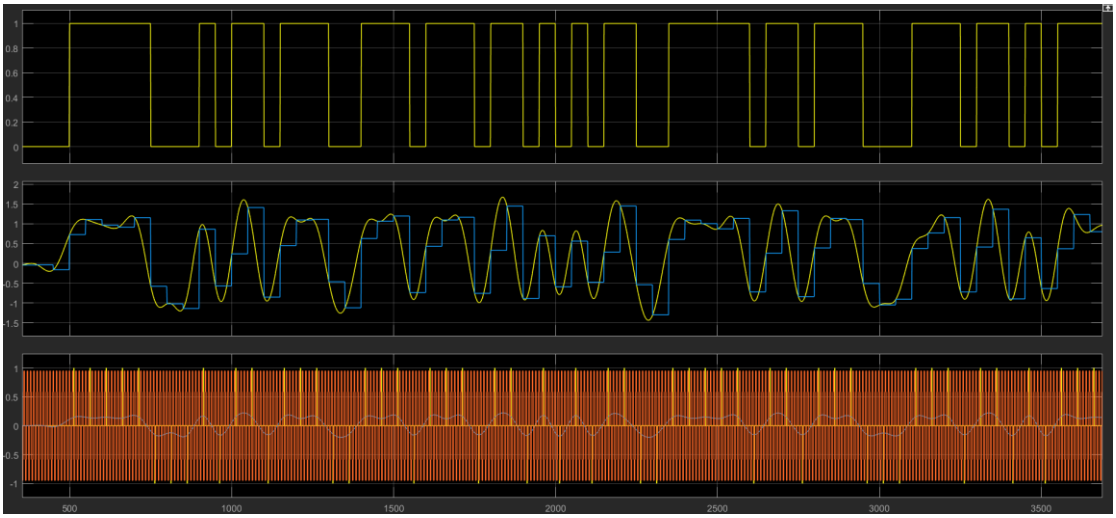


Figure 23: Output setup 7

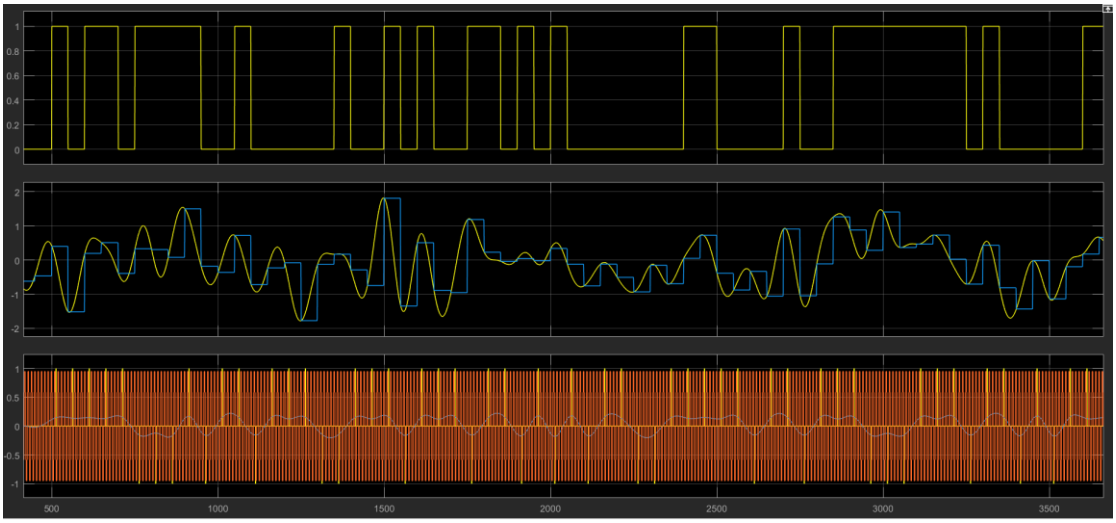


Figure 24: Output with higher noise setup [0.1]

Lab Write up

(1) Explain briefly how the receiver works. Also, please highlight anything that was new that you didn't know before!

Receiver first down converts the received signal to baseband. Down conversion is done by multiplying the conjugate of the carrier used for up conversion. Only the signal in the baseband is kept by filtering the signal by matched filter. Than the signal is sampled at optimal points and the estimation of I/Q symbols are done (decision block). The symbols are mapped back to bits and the signal is fully recovered.

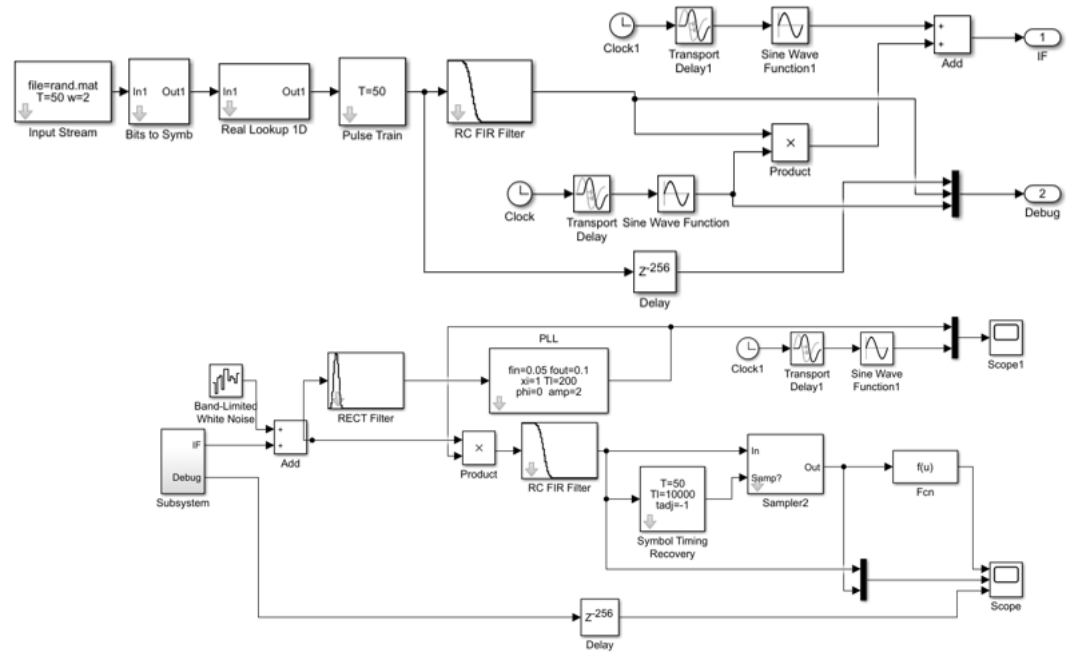
(2) Explain how we can get a RC response by using root filters at the transmit and receive. Explain why this is preferable to using just a single (non root) RC filter somewhere.

The root raised cosine (RRC) filter takes the square root of RC response in frequency domain. Using RRC filter in both transmitter and receiver, the cascade response gives a result of multiplication – giving RC response. Also, this is a matched filter. This method is used because it minimizes the noise of the signal for a desirable zero ISI property.

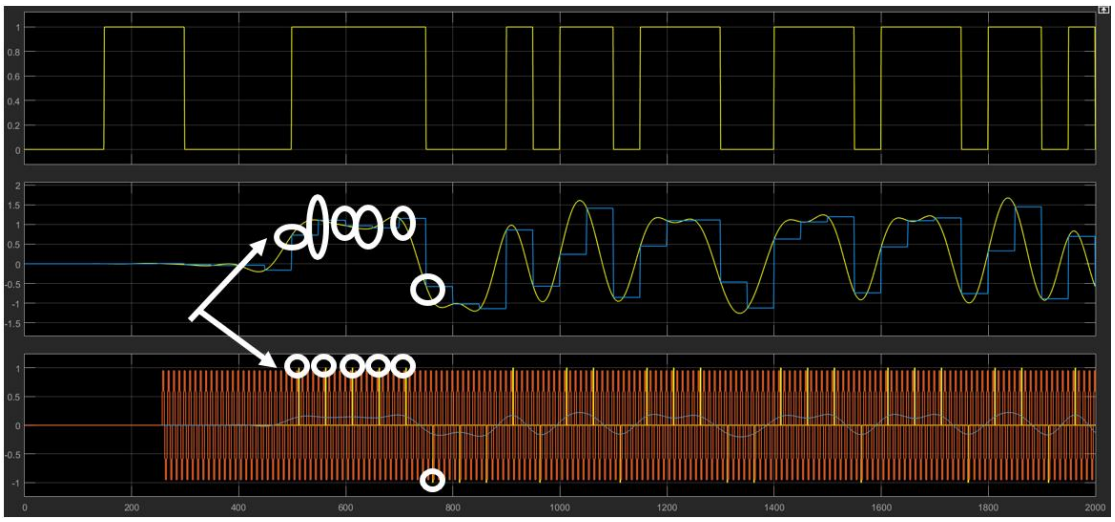
(3) Explain the need for synchronization in communications systems, and how this was accomplished in this lab. Also describe what a PLL is and what it can do. What are carrier and symbol timing recovery for?

Synchronization is needed because phase difference can cause inter symbol interference giving wrong data. Synchronization was done by using phase locked loop.
Phase locked loop (PLL) is a feedback demodulator that gives an output signal with a phase related to the phase of the input signal. PLL has an internal sine wave and tracks the phase of the input wave using a feedback loop. It gives an output proportional to the phase difference.
Carrier recovery recovers the frequency and phase offset of the received signal to that of the transmitted signal. This is done by using PLL.
Symbol timing recovery is needed because the receiver must have the exact symbol timing to have a proper demodulated recovery of signal. It samples the baseband signal the optimal points of samples for symbol to bit conversion. This is done by locking PLL to rising and falling edges of the waveforms.

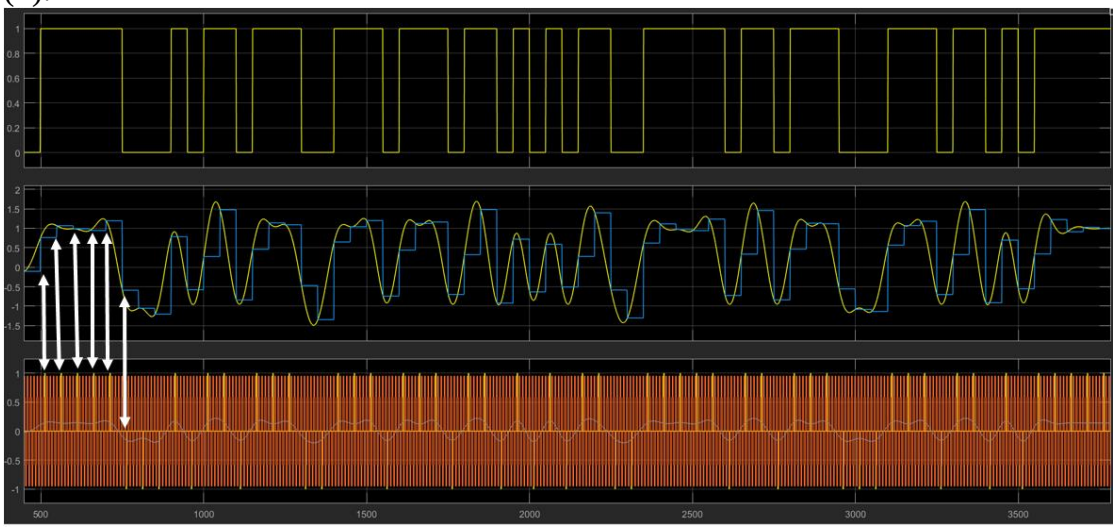
(4) Give plots showing the output of your communications system for two cases: (i) with perfect ideal synchronization, and (ii) with the synchronization blocks. Circle and label points the printout to "prove" to the TA that it is working.


file=rand.mat
T=50 w=2
Input Stream
In1 Out1
Bits to Symb
In1 Out1
Real Lookup 1D
T=50
Pulse Train
RC FIR Filter
Clock1
Transport Delay1
Sine Wave Function1
Add
1
IF
Product
Clock
Transport Delay
Sine Wave Function
2
Debug
z-256
Delay
PLL
fin=0.05 fout=0.1
xi=1 TI=200
phi=0 amp=2
Band-Limited White Noise
RECT Filter
Clock1
Transport Delay1
Sine Wave Function1
Scope1
IF
Debug
Subsystem
Add
Product
RC FIR Filter
T=50
TI=10000
tadj=-1
Symbol Timing Recovery
In
Out
Simp?
Sampler2
f(u)
Fcn
Scope
z-256
Delay

(i):



(ii):



(5) Describe any difficulties you experienced in getting your design to work and how you fixed these problems.

Adapting the external delay block to the different simulation components' delay was not that trivial at first, but analysing and understanding the role of each part of the simulation enabled to adjust the delay block accordingly. Building the circuit in a not so 'complicated' manner was also a challenge that was overcome.

3 **Conclusion**

This experiment successfully met its objective since it enabled to understand the 'uncoded' receiving part of a communication system. The receiving process did not differ that much from the transmission one but was only a mirrored version of it with tools adapted accordingly. We perfectly understood the role of root filters and the effect of synchronization in communication by comparing a perfect synchronization to one done using PLL. Errors in this experiment mainly involved the negligible inaccuracy of the PLL synchronization compared to the perfect synchronization process.

4 **References**

[1] http://dsp-fhu.user.jacobs-university.de/reciversimulinkstudy
[2] Matched filter. (2018, September 13). Retrieved from https://en.wikipedia.org/wiki/Matched_filter
[3] Digital I/Q demodulator carrier recovery using Costas loops. (n.d.). Retrieved from https://www.nutaq.com/blog/digital-iq-demodulator-carrier-recovery-using-costas-loops
[4] Phase-locked loop. (2018, November 24). Retrieved from https://en.wikipedia.org/wiki/Phase-locked_loop