Jacobs University Bremen

Natural Science Laboratory
Electronics Lab

Spring Semester 2019

Lab Experiment 5 – Metal Oxide Field Effect Transistor

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Place of execution	: Research 1 EE Lab 54
Date of execution	: April. 08, 2019

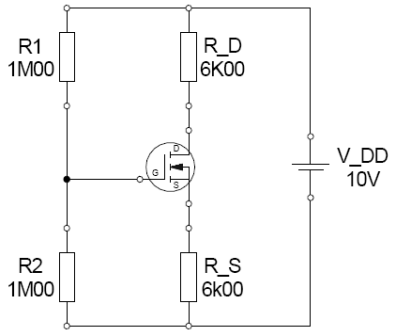
1 Introduction - Prelab

1.1 Problem 1 : Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

(1) Explain the differences between an enhanced and depletion MOSFET.
Enhance MOSFET transistor needs Gate-Source voltage to switch the device 'ON' and the Depletion MOSFET transistor needs Gate-Source voltage to switch the device 'OFF'. In other words, the enhance MOSFET is normally open switch and depletion MOSFET is a normally closed switch.

(2) Explain the differences between an NMOS and PMOS transistor.
NMOS (nMOSFET) is made up of n-type source and drain and a p-type substrate. PMOS (pMOSFET) is made up of p-type source and drain and a n-type substrate.

1.2 Problem 2 : MOSFET as Amplifier



(1) Determine the gate-source and drain-source voltage and the drain current for the MOSFET amplier.
$\mathrm{k} = 0.5\mathrm{mA/V}^2$
$\mathrm{V}_{th} = 1V$
$\mathrm{I_{DS}} = \mu_n C_G \frac{W}{2L}(V_{GS} - V_{th})^2 = k(V_{GS} - V_{th})^2$
Let $\mathrm{I_G} = 0$
$\mathrm{I_D} = I_S = k(V_{GS} - V_{th})^2$
$\mathrm{V_{GS}} = V_G - I_S R_S$
$\mathrm{V_G} = V_{DD} \frac{R_1}{R_1 + R_2} = 10 \cdot \frac{1\mathrm{M}}{1M + 1M} = 5V$
$\mathrm{I_S} = k(V_G - I_S R_S - V_{th})^2 = 0.0005(5 - 6000 I_S - 1)^2$
$\mathrm{I_S} = 0.0005, 0.000888889\ A = \mathrm{I_D}$

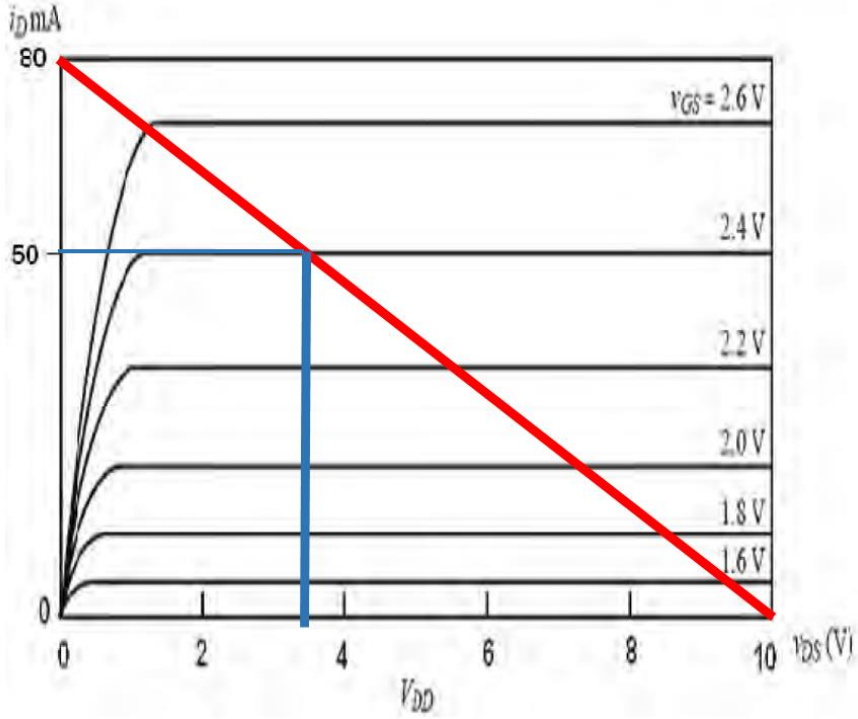
If $\mathrm{I_S} = I_D = 0.000888889$
$\mathrm{V_{GS}} = 5 - 0.000888889 \cdot 6000 = -0.333334$ -> Wrong

If $\mathrm{I_S} = I_D = 0.0005$
$\mathbf{V_{GS}} = V_G - I_S R_S = 5 - 0.0005 \cdot 6000 = 2\mathrm{V}$
$\mathbf{V_{DS}} = V_{DD} - I_D R_D - I_S R_S = 10 - 0.0005 \cdot 6000 - 0.0006 \cdot 6000 = 4V$

(2) Show that the MOSFET indeed operates in the saturation region.
$\mathrm{V_{DS}} > V_{GS} - V_{th}$
Therefore the MOSFET is in the saturation region

1.3 Problem 3: MOSFET as Switch

The MOSFET is used as a switch. The input signal of the circuit varies between 0V and 2.4V. Determine the operating point for both input voltages.
Hint Use the output characteristic below to determine the operating point.



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2 Execution, Evaluation

2.1 Experiment Setup

Used tools and instruments:

- Breadboard, Tools box from workbench
- Oscilloscope Tektronix, Function Generator

2.1.1 Experiment Part 1 : Current/Voltage Characteristic of a MOSFET – Setup

- Objective

Measure current/voltage characteristic of NMOSFET.

2.1.2 Experiment Part 1 – Execution and Results

- Test Circuit:

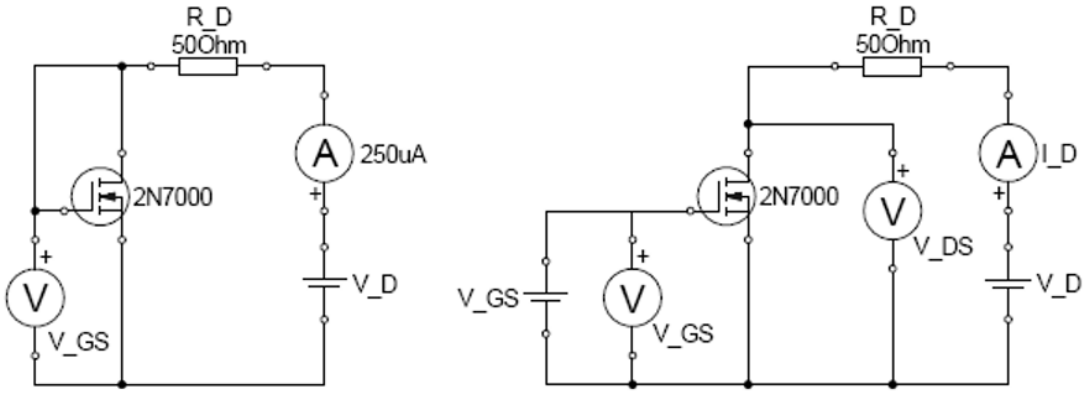


Figure 1 (left) circuit 1, (right) circuit 2

- Description of the measurement procedure.

In question 1, circuit 1 was used and by setting the voltage of V_D such that $I_D = 250\mu A$, U_{th} was measured. In question 2, the transfer characteristic of circuit 2 was determined by changing the gate source voltage from 0 to 3V while keeping $U_{DS} = 5V$. In question 3, the output characteristic was studied by changing the gate source voltage from 2, 2.2, 2.4, 2.6V while the drain source voltage was scanned from 0 to 4 V.

Results:

(1) Use circuit 1 to determine U_{th}.

$$I_D = 258.0\mu A$$
$$U_{th} = U_{GS} = U_{DS} = 2.158V$$

(2) Use circuit 2 to measure the transfer characteristic.

Table 1 Fixed U_{DS} transfer characteristic

U_{GS} [V]	U_{DS} [V]	I_D [A]
0.0	5.006	0.0000003
0.5	5.006	0.0000003
1.0	5.006	0.0000003
1.5	5.006	0.0000004
2.0	4.990	0.0001078
2.2	5.003	0.0029
2.4	5.003	0.0107
2.5	3.006	0.0184
2.7	4.996	0.0356
3.0	4.999	0.0749

(3) Use the circuit from before and measure the output characteristic for gate source voltages of 2V, 2.2V, 2.4V, and 2.6V. The drain source voltage should be scanned from 0V to 4V

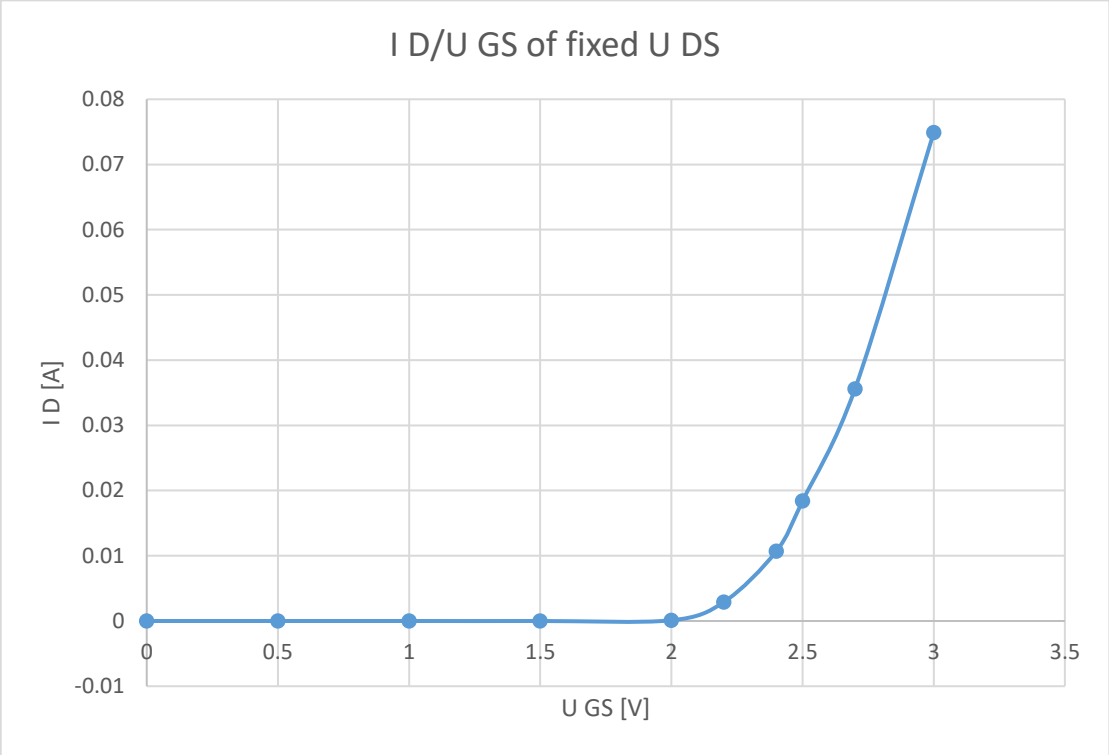
Table 2 Output result of change V_{GS}, V_{DS}[1]

V_{GS} [V]	V_{DS} [V]	I_D [A]	V_{GS} [V]	V_{DS} [V]	I_D [A]
2V	0.004	2.12E-05	2.2V	0	4.38E-05
	0.509	1.81E-04		0.506	1.79E-03
	0.994	1.87E-04		1.013	1.86E-03
	1.496	1.50E-04		1.495	1.89E-03
	2.004	1.50E-04		2.000	1.92E-03
				2.518	1.95E-03
				3.08	1.98E-03
				3.506	2.01E-03
				4	2.04E-03
V_{GS} [V]	V_{DS} [V]	I_D [A]	V_{GS} [V]	V_{DS} [V]	I_D [A]
2.4V	0	5.02E-05	2.6V	0	5.83E-05
	0.522	7.30E-03		0.525	1.16E-02
	1.016	9.66E-03		1.016	1.29E-02
	1.507	1.31E-02		1.538	1.61E-02
	2.014	1.67E-02		2.017	1.97E-02
	2.506	2.05E-02		2.509	2.34E-02
	3.001	2.44E-02		3.002	2.73E-02
	3.500	2.85E-02		3.496	3.13E-02
	4.007	3.27E-02		3.997	3.55E-02

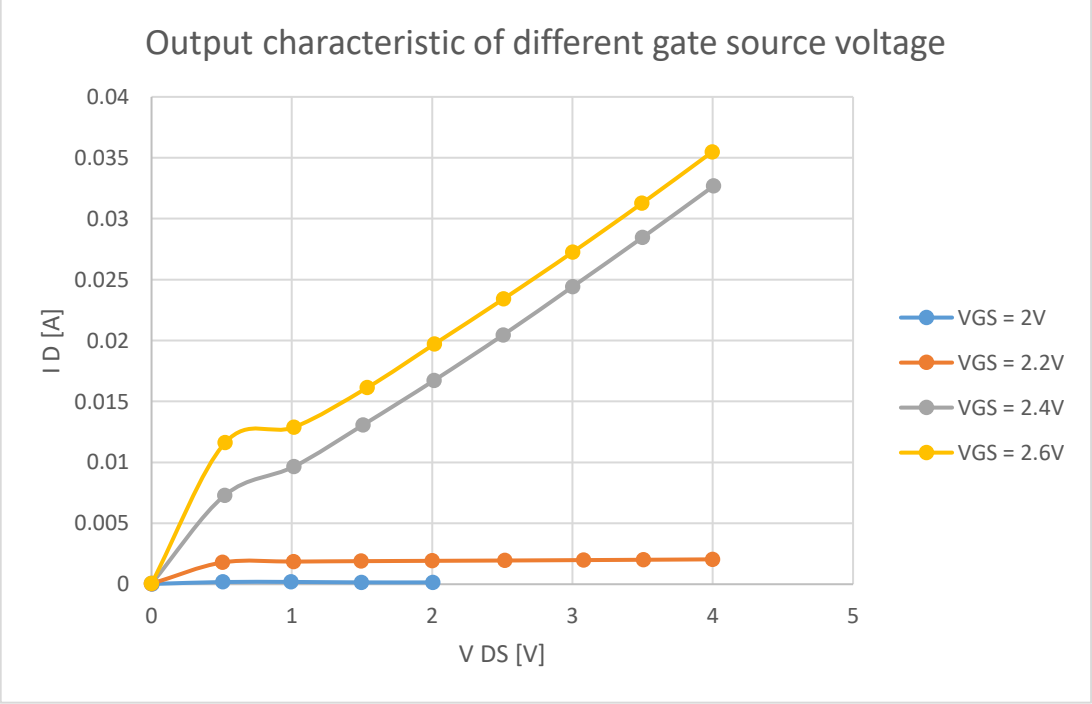
[1] Desar's data is used because of wrong measurement of my group.

In the lab report:

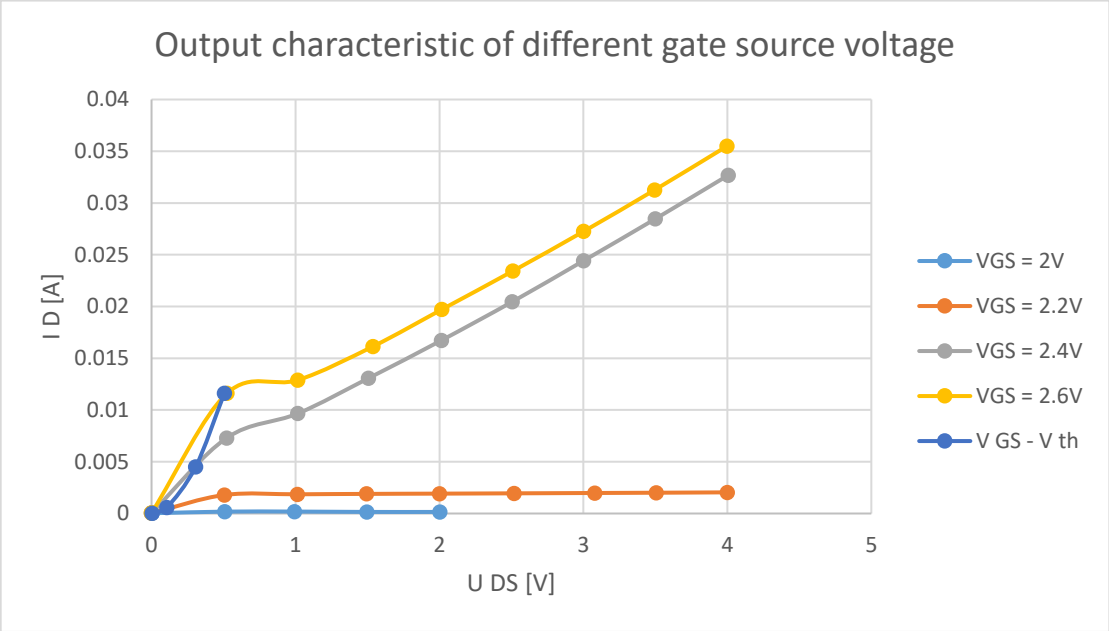
1. Plot the measured transfer characteristic.



2. Plot the measured output characteristic for the different gate source voltages.



3. Insert the $V_{DS} = V_{GS} - V_{th}$ line into the output characteristic.

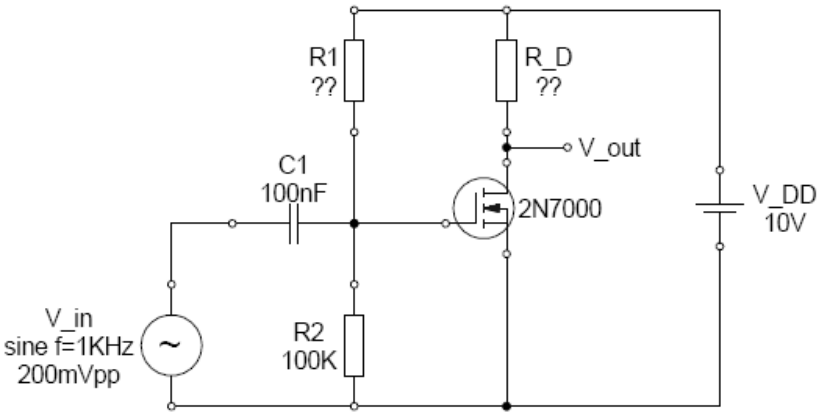


2.1.3 Experiment Part 2 – Setup

- Objective

Design and realize an amplifier circuit by using MOSFET

- Test Circuit:



$V_{GS} = 2.7V$, $V_{DS} = 5V$, $k = 72.2mA/V^2$, U_{th} = use measured value!

Figure 2 Circuit of part 2

2.1.4 Experiment Part 2 – Execution and Results

- Description of the measurement procedure.

Determine the R_1, R_D values and assemble the circuit. Input of 1KHz and amplitude of 100 mV is applied and check the output characteristics.

Results:

(1) R_1, R_D Calculation

$$U_{th} = 2.158V$$

$$R_1 = \frac{V_{DD} - V_{GS}}{V_{GS}} \cdot R_2 = \frac{10 - 2.7}{2.7} \cdot 100000 = 270{,}370\Omega$$

In the circuit, $R_1 = 269.6K\Omega \approx 270\text{K}\Omega$ is used.

$$R_D = \frac{V_{DD} - V_{GS}}{k(V_{GS} - V_{th})^2} = \frac{10 - 5}{0.0722 \cdot (2.7 - 2.158)^2} = 235.7\Omega$$

In the circuit, $R_D = 219.6\Omega \approx 220\Omega$ is used.

(2) Input and output signal result

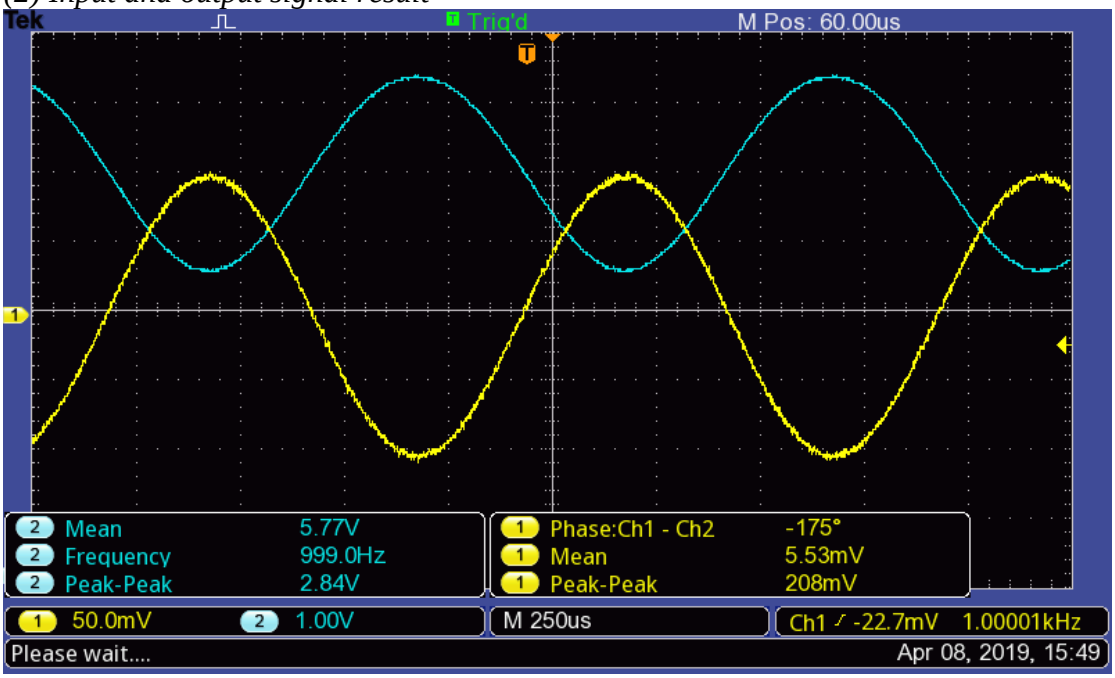


Figure 3 Input and output characteristics of circuit

In the lab report:

1. In which mode (linear or saturation) does the transistor operate during amplification? Provide an explanation.

The transistor operate in the saturation mode during amplification. This is because the $V_{GS} = 2.7V$, which is higher than threshold voltage. In this saturation mode, the MOSFET acts as a voltage-controlled current source, dependent on gate-source voltage.

2. If the amplitude of the sinusoidal input voltage is too large clipping of the output voltage is observed. Determine the largest possible input voltage for which no clipping is observed.

No clipping is observed at 0.542V

$$V_{GS} - V_{in} - V_{th} = 0$$
$$V_{in} = V_{GS} - V_{th} = 2.7 - 2.158 = 0.542$$

3. Provide a mathematical expression for the voltage gain (theoretical voltage gain) of the circuit.

Voltage gain = $\frac{V_{OUT}}{V_{IN}} = \frac{V_{DS}}{V_{IN}} = \frac{V_{DD} - V_{RD}}{V_{IN}}$

4. Determine the measured voltage gain and compare the measured voltage gain with the theoretical voltage gain.

Measured:

$$\frac{V_{out}}{V_{in}} = \frac{5.68}{0.208} = 27.308$$

Theoretical:

$$\frac{V_{OUT}}{V_{IN}} = \frac{10-5}{0.2} = 25$$

5. Explain the phase relation between the input and the output.
As shown in the picture above, there is a phase shift of about 180º. This is due to the capacitor (C1) and the capacitor inside the transistor.

2.1.5 Experiment Part 3: Design a Multiplexer – Setup

- Objective

Understand and design a simple 2-to1 multiplexer using MOFSET.

- Test Circuit:

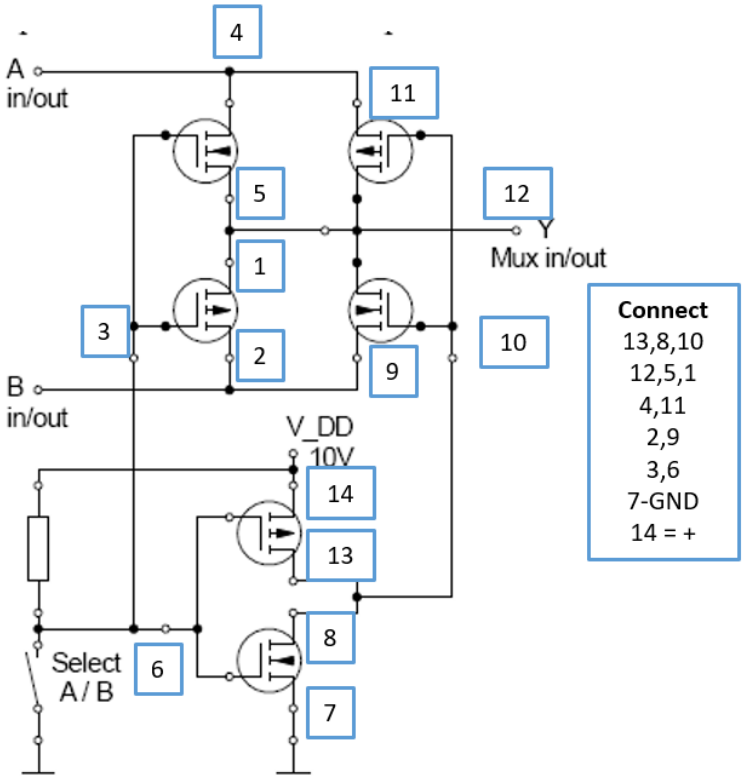


Figure 4 Multiplexer circuit

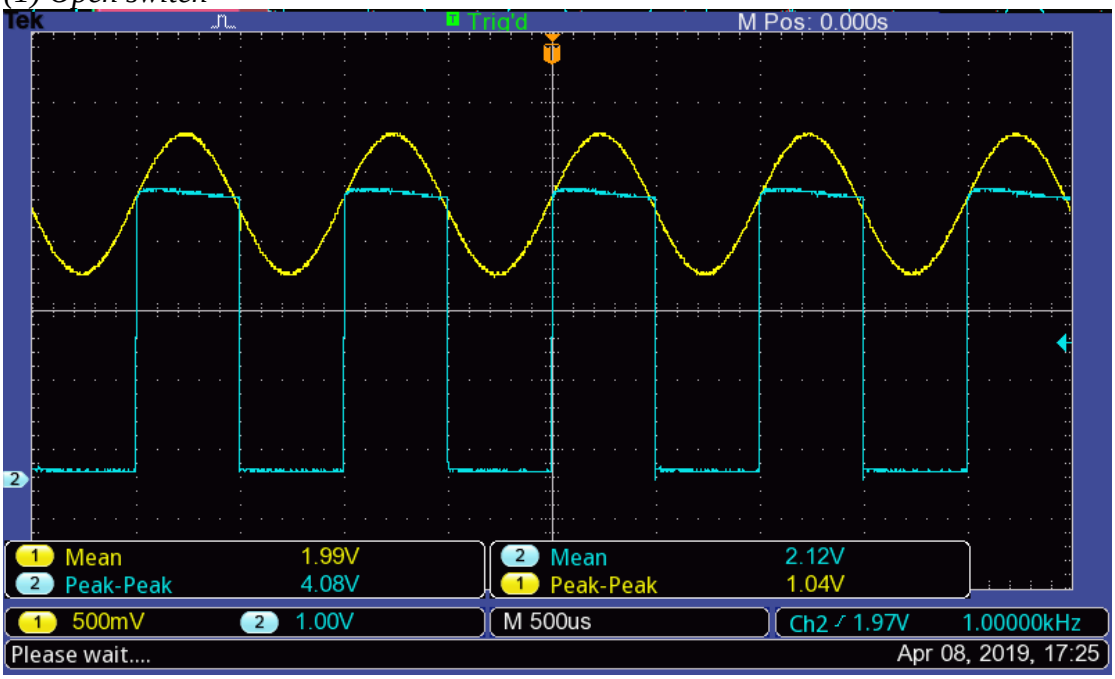
2.1.6 Experiment Part 3 – Execution and Results

- Description of the measurement procedure.

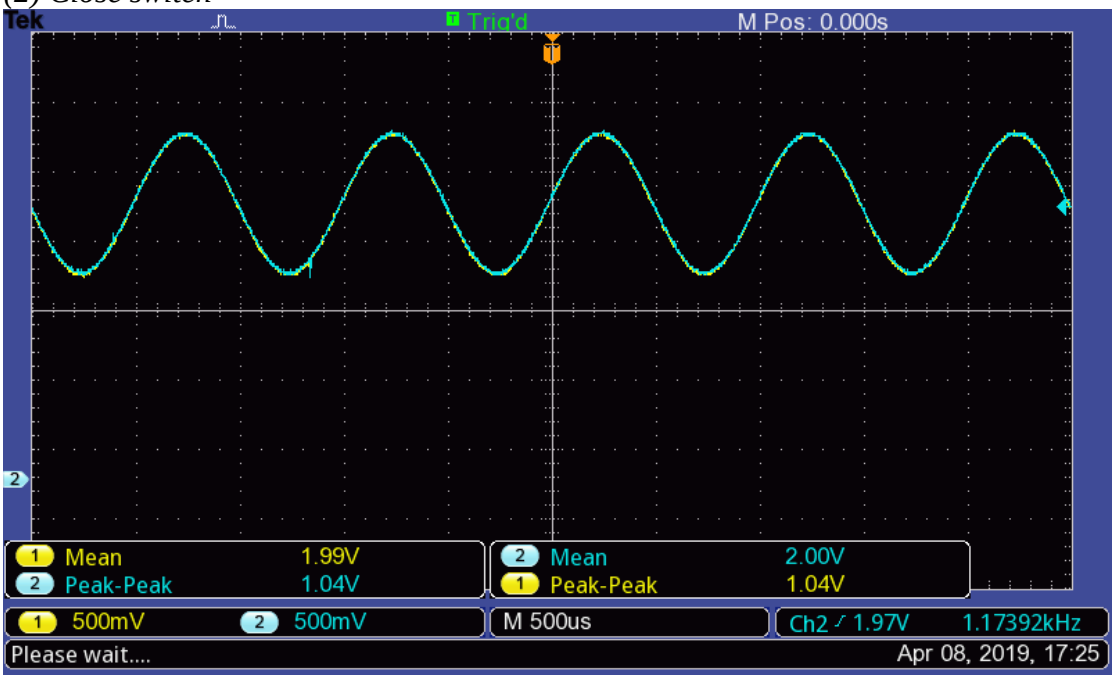
Figure out which pins to connect to make a multiplexer. (Shown in the circuit diagram above). Pin 14 is always connected to the positive supply voltage and pin 7 is always to the negative supply voltage. (In this case, ground) To the input A, a signal of amplitude 1V, offset of 2V and frequency of 1KHZ is applied. And in the sinc function generator is connected to input B. And the output was examined.

Results:

(1) Open switch

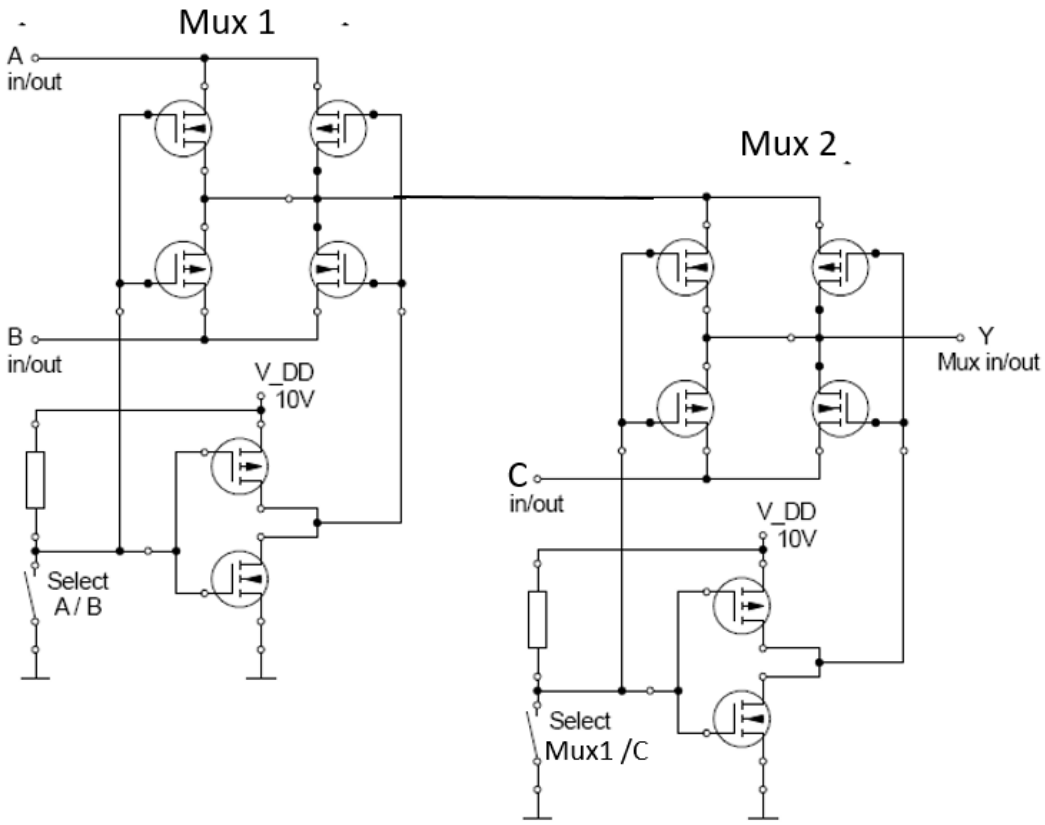


(2) Close switch



In the lab report:
1. Provide the captured hardcopies
Check the figure in result section above.

2. Design a 3 to 1 multiplexer and provide the circuit.



3 Conclusion

In the experiment, Metal Oxide Field Effect Transistor (MOFET) characteristics were observed. U_{th} and transfer characteristic of varying V_{GS}, V_{DS} of a NMOSFET were examined. Graphs are shown in evaluation part 1. The off, sub threshold, linear and saturation region are shown. In part2, MOSFET as an amplifier is shown.The amplification is operatied in the saturation region and the voltage gain was calculated. The measured voltage gain had 27.308 while the theoretical voltage gain was 25, giving 9% of errors. This error is due to the accuracy of the instrument, condition of the MOSFET and circuit element errors. Also, amplifier showed a phase difference of 180º which is due to two capacitors. In part 3, multiplexer was designed by connecting the pins of a MOSFET. The multiplexer operation is shown in results part 3. Also, 3 to 1 multiplexer was designed in evaluation part 3.

5 References

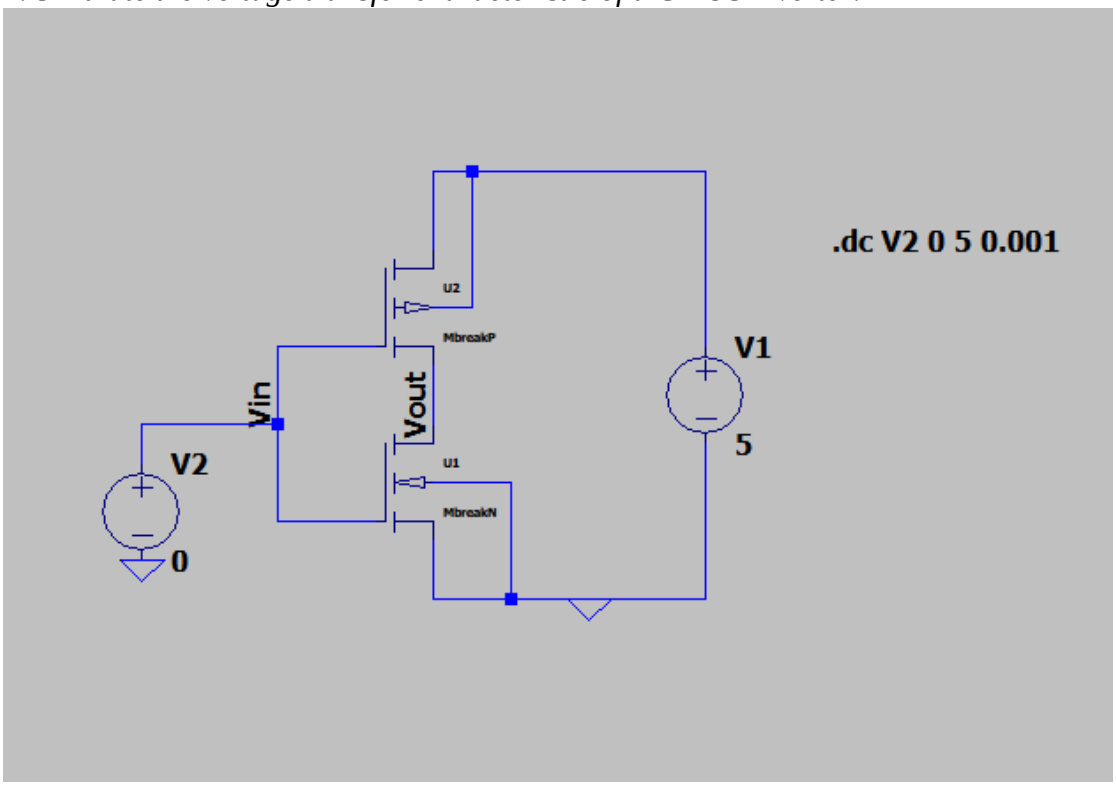
[1] Inst. Uwe Pagel: 'Electronics Lab' (2019), 'Bipolar Junction Transistor', 37-52
[2] What Is the Difference between NMOS, PMOS and CMOS ... www.quora.com/What-is-the-difference-between-NMOS-PMOS-and-CMOS-transistors.
[3] "MOSFET and Metal Oxide Semiconductor Tutorial." Basic Electronics Tutorials, 5 Feb. 2019, www.electronics-tutorials.ws/transistor/tran_6.html.

6 Appendix - Prelab of Experiment 6

6.1 Prelab CMOS Inverters and Logic Gates

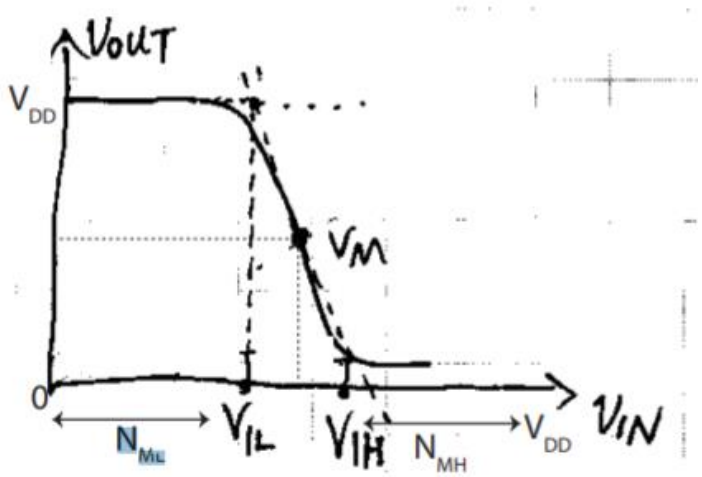
6.1.1 Problem 1: Voltage Transfer Characteristic of a CMOS inverter

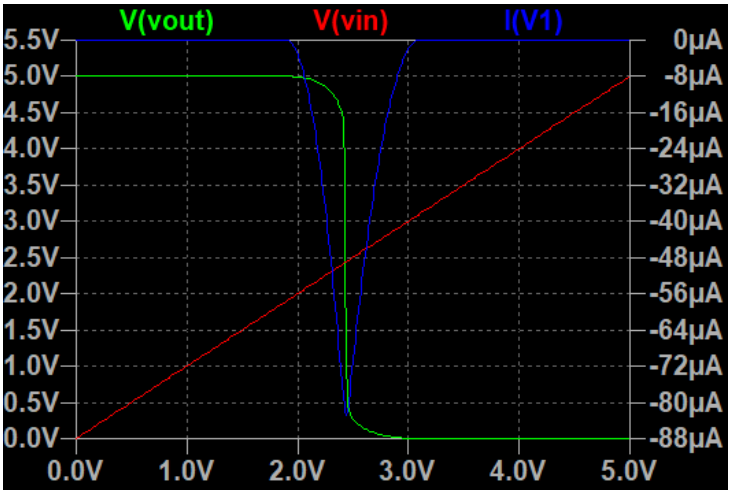
1. Simulate the voltage transfer characteristic of a CMOS inverter.



Note: Use the 'MbreakN' device model for the NMOS transistor and the 'MbreakP' device model for the PMOS transistor from the supplied library. These are the device models for the MOSFETs in the CD4007.

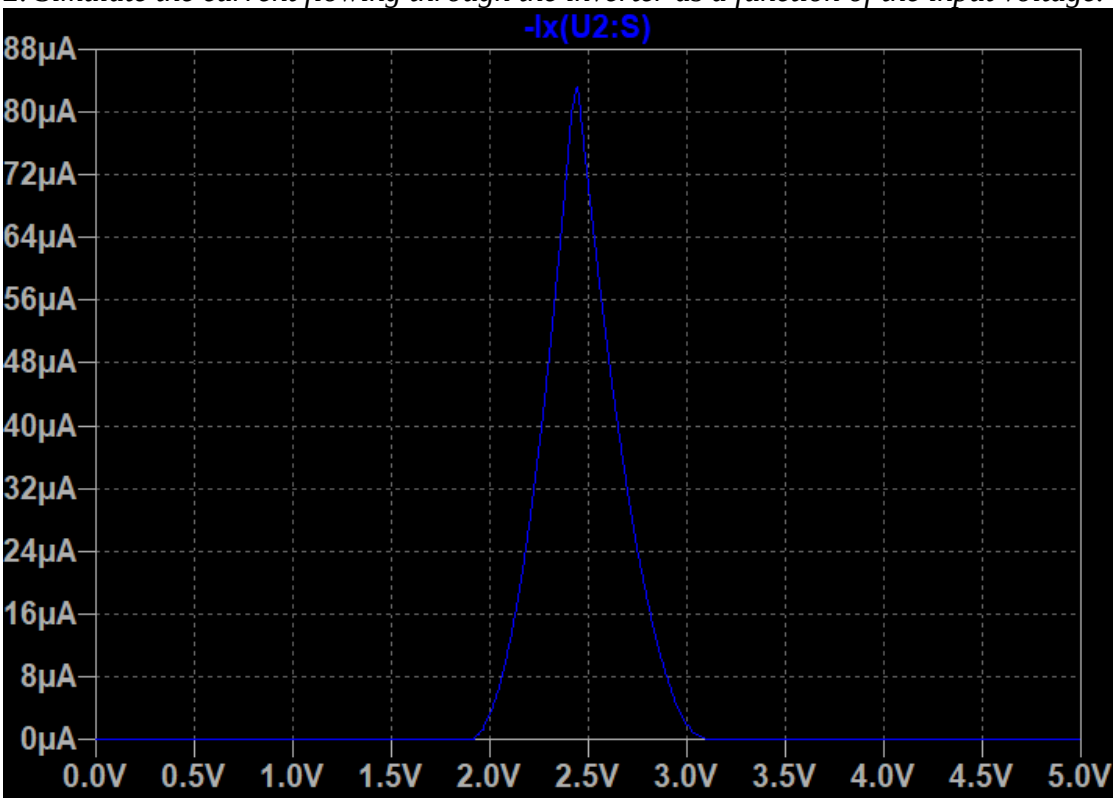
1. Use 5V for the power supply V_{DD}. *Simulate the voltage transfer curve (VTC) of the CMOS inverter and extract the values of* $V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_L, NM_H$ *and* V_{th} . *Hint: Use the d() function of LTSpice to determine* V_{IH}, V_{IL}*!!*





$$V_{OH} = 5V$$
$$V_{OL} = 0V$$
$$V_{IH} = 2.57\ V$$
$$V_{IL} = 2.23\ V$$
$$N_{ML} = V_{IL} - V_{OL} = 2.23\ V$$
$$N_{MH} = V_{OH} - V_{IH} = 2.43V$$
$$V_M = V_{th} = 2.425V$$

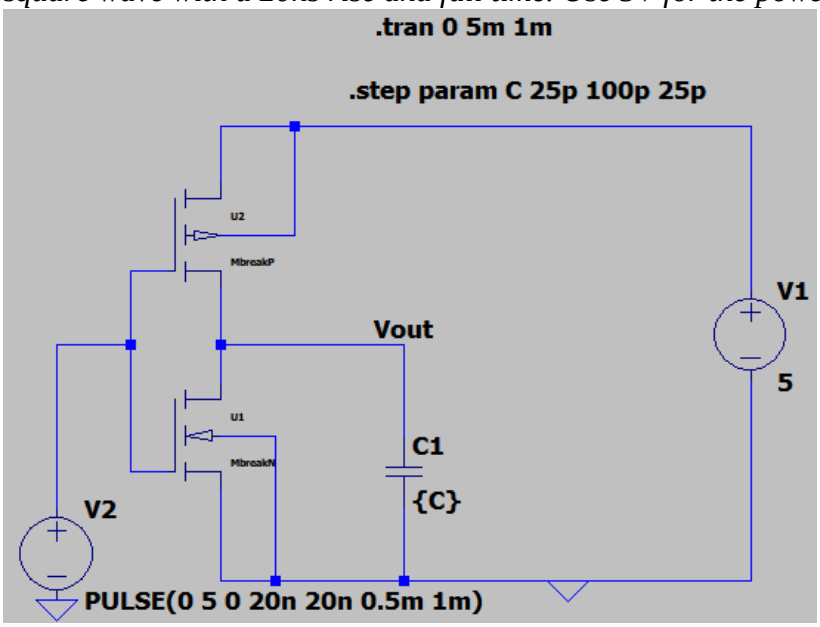
2. Simulate the current flowing through the inverter as a function of the input voltage.

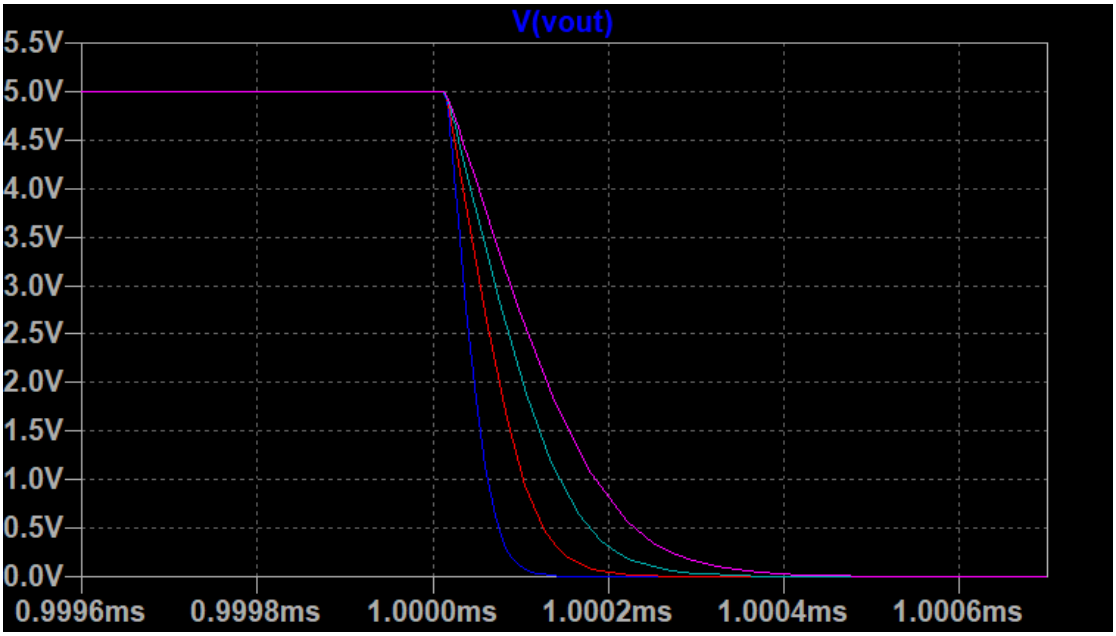


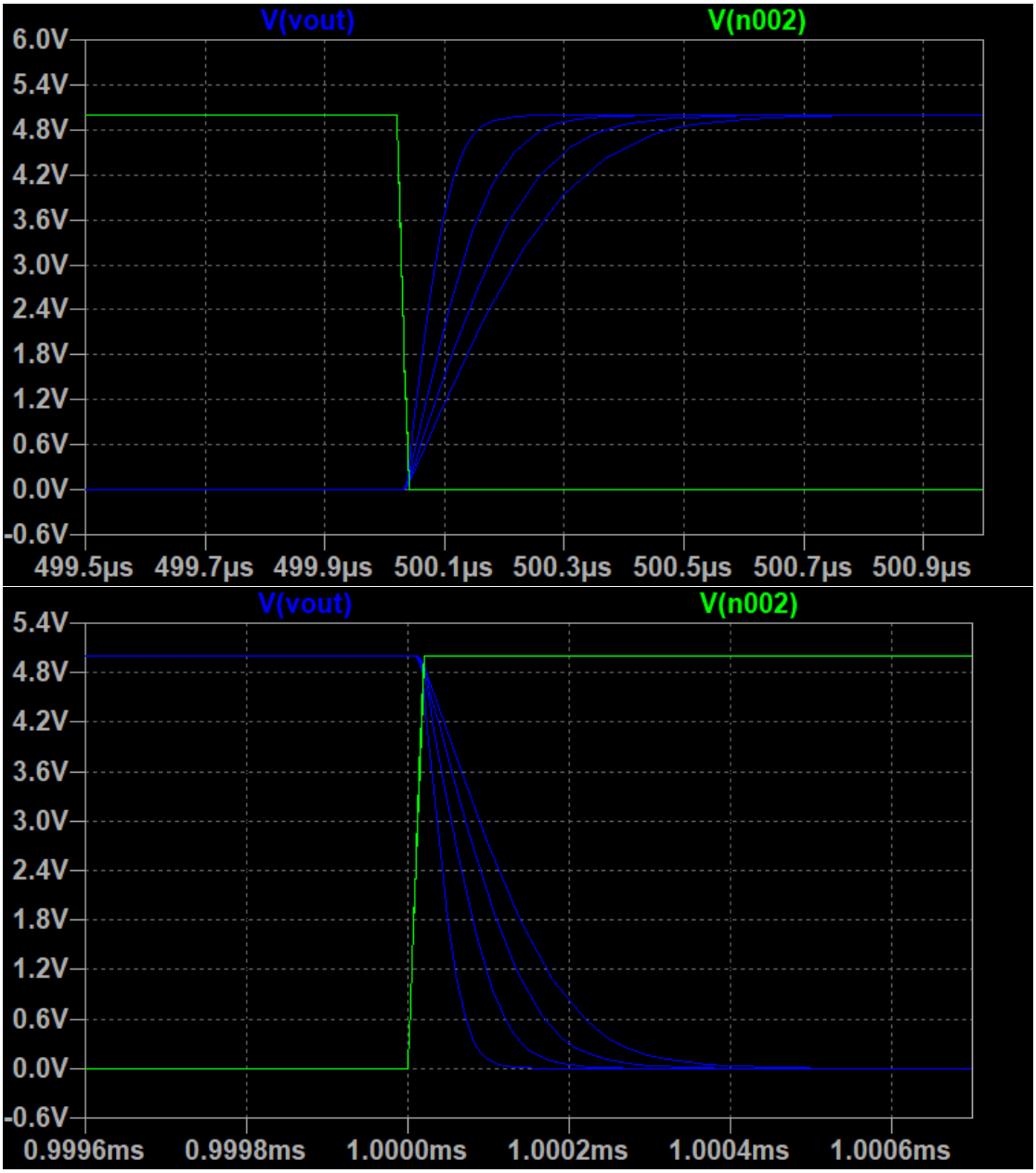
3. For what input level the current reaches its maximum. Provide an explanation.
2.450495V
This is when both NMOS and PMOS is open. Allowing current to flow through its drain-source connection.

6.1.2 Problem 2: CMOS Inverter with Capacitive Load

1. 1. The capacitive load should be varied from 25pF to 100pF in 25pF steps. Determine the propagation delay ($t_{PLH} = t_{PHL}$) if the input signal is given by a 1KHz square wave with a 20ns rise and fall time. Use 5V for the power supply V_{DD}.







C	t_{PLH}
25pF	28.1 ns
50pF	51.1 ns
75pF	74.9 ns
100pF	97.8 ns

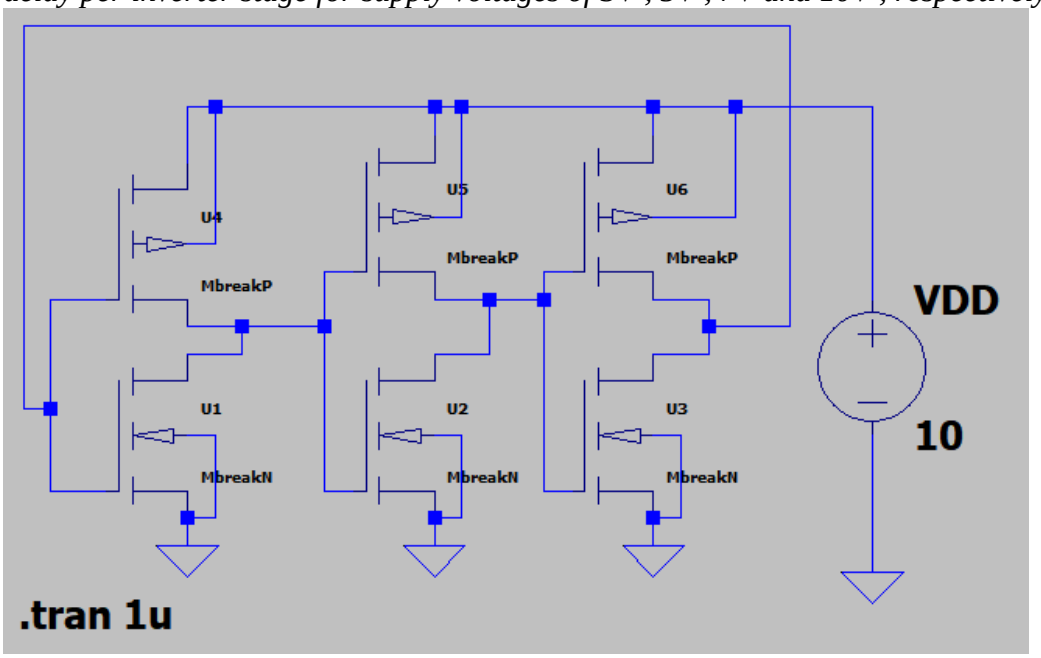
2. Obtain the dynamic power dissipation of the CMOS inverter for the different load capacitors.

$$P_D = f \cdot C \cdot V_{DD}^2$$

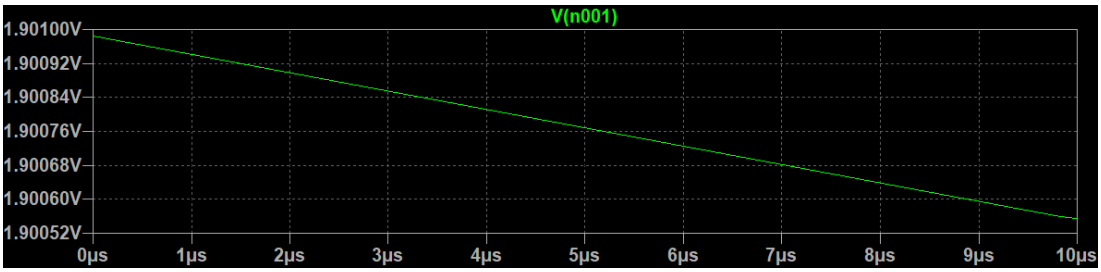
C	$P_D = 1000 \cdot C \cdot 25$
25pF	0.000000625 W
50pF	0.00000125 W
75pF	0.000001875 W
100pF	0.0000025W

6.1.3 Problem 3: Propagation Delay of an Inverter Stage

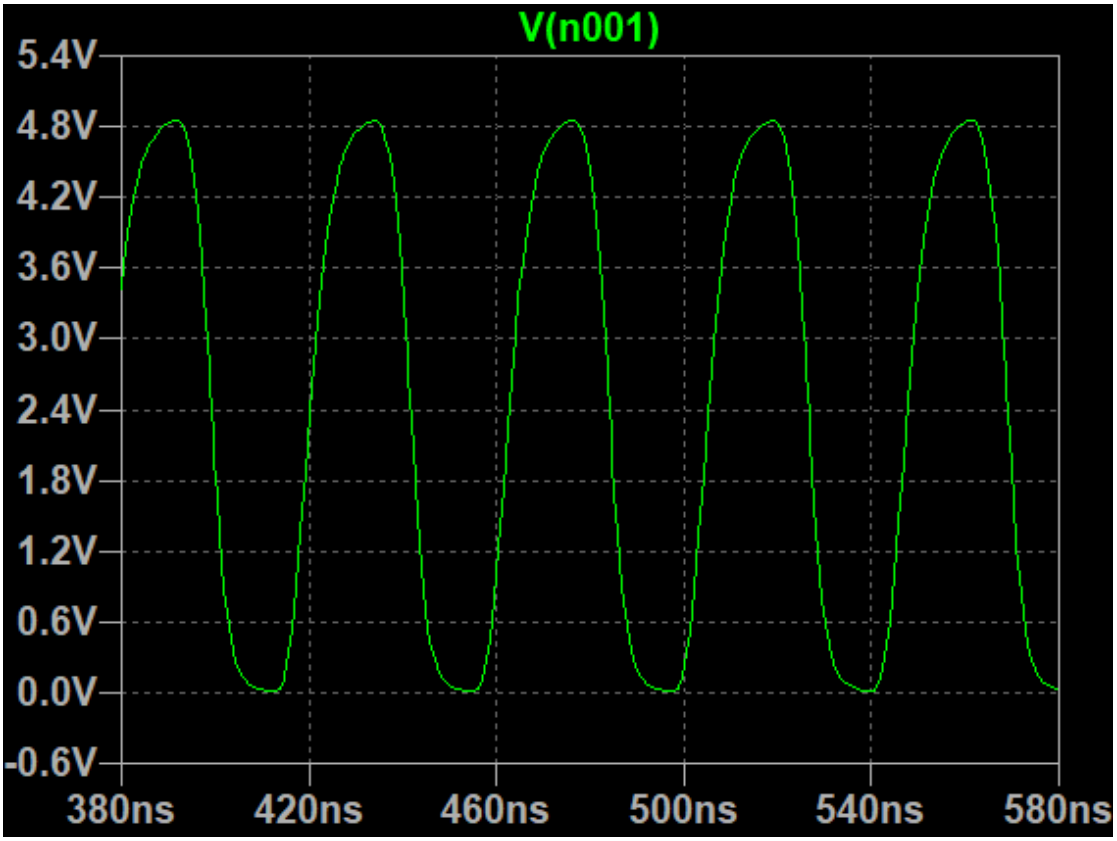
1. Determine the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages of 3V , 5V , 7V and 10V , respectively.



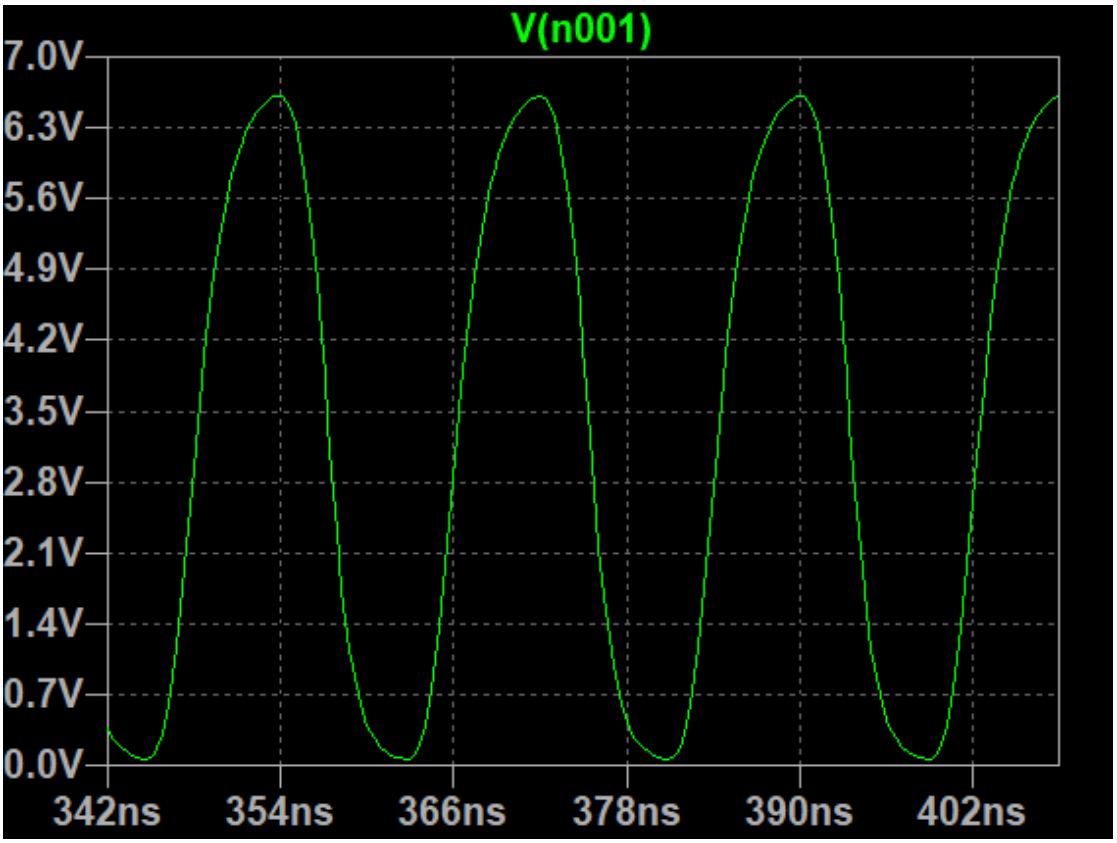
Note: It might be necessary to apply a single pulse to the input of the ring oscillator to start it!



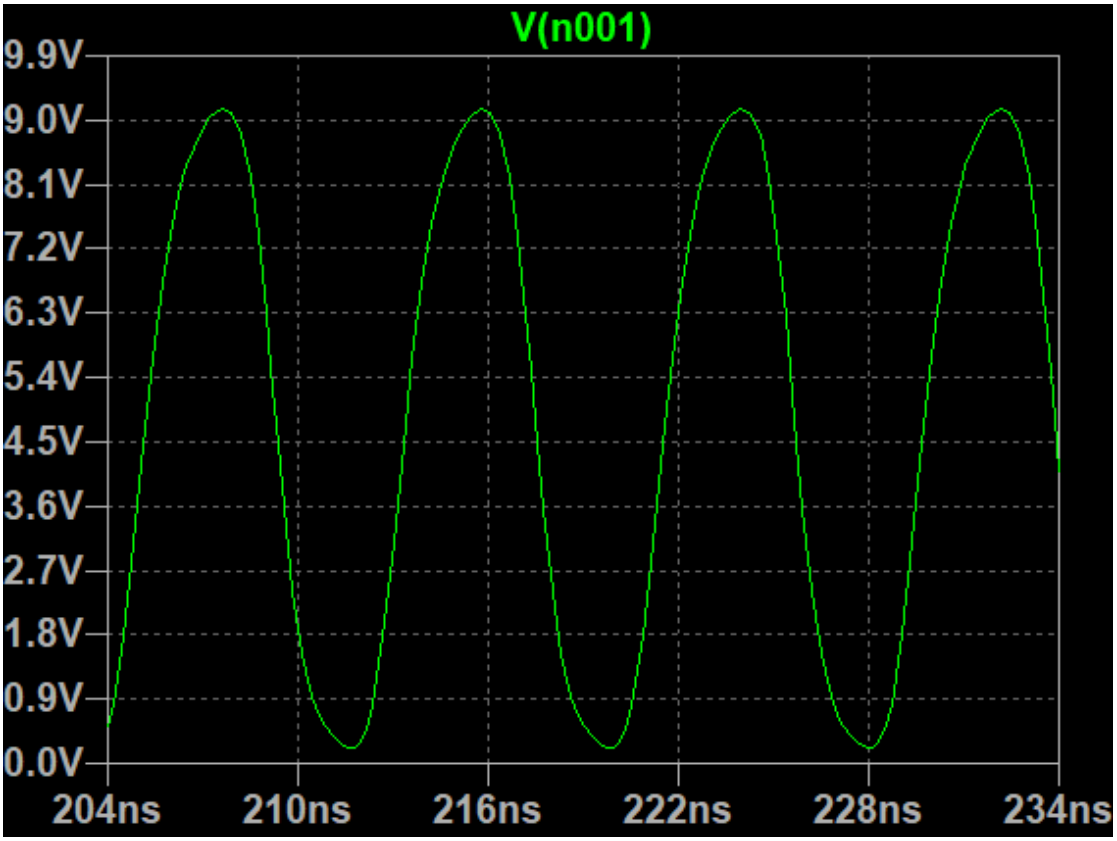
At $V_{DD} = 3V$, no oscillation can be seen.



At $V_{DD} = 5V$



At $V_{DD} = 7V$



At $V_{DD} = 10V$

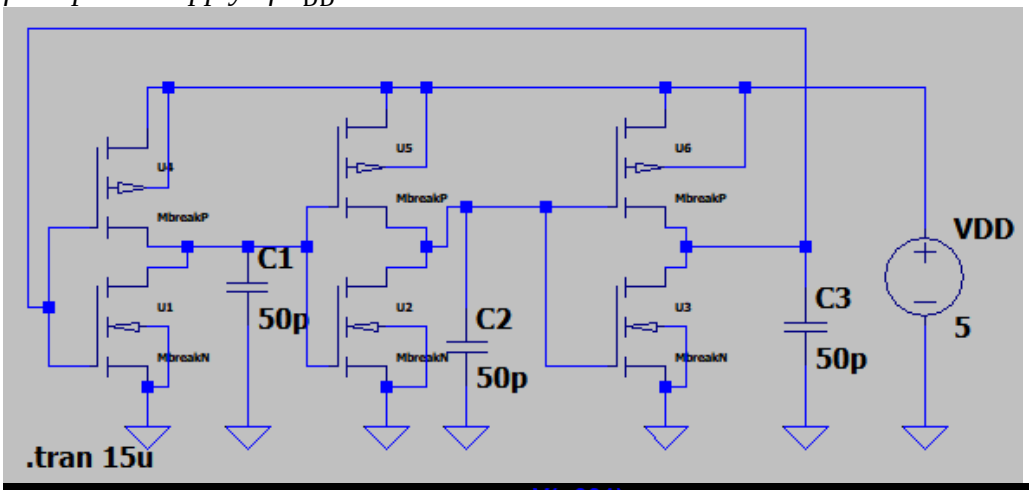
V_{DD} [V]	f	$t_d = \frac{1}{2Nf} = \frac{1}{2 \cdot 3 \cdot f}$
3		
5	24.044266 MHz	6.9 ns
7	54.659806 MHz	3 ns
10	121.37137 MHz	1.37 ns

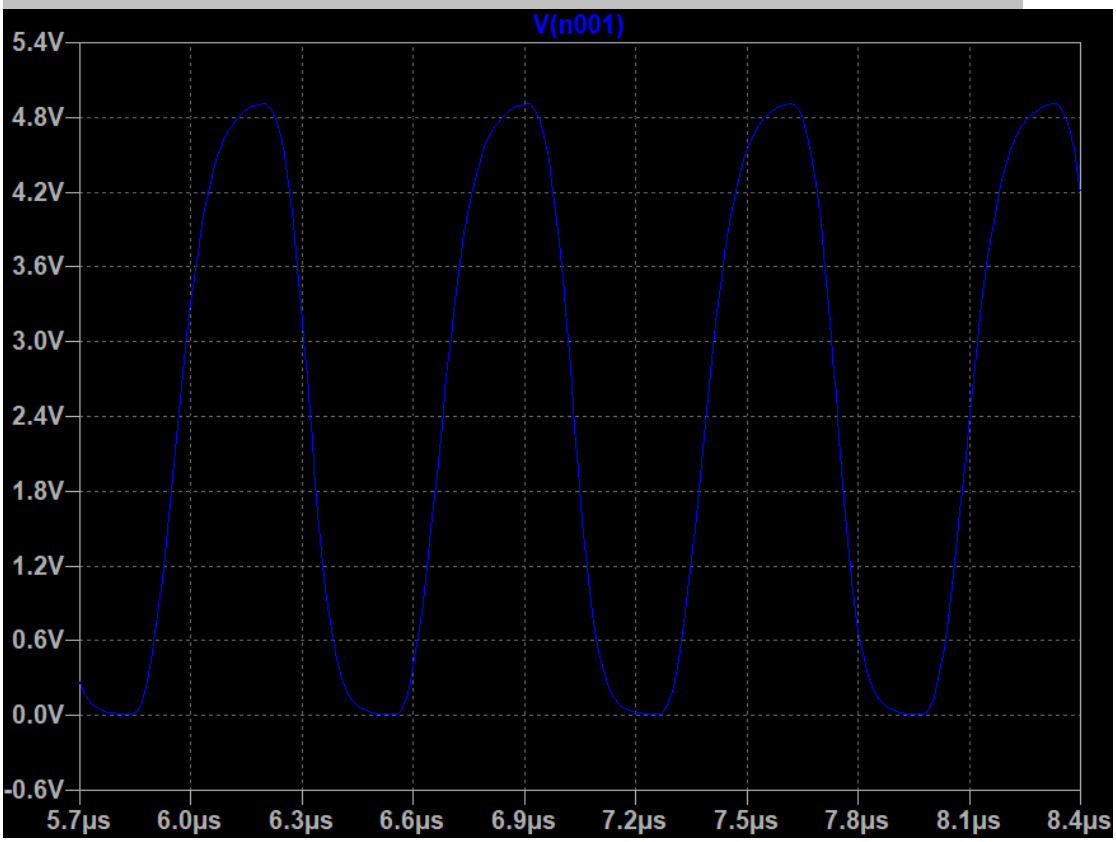
2. Calculate the dynamic power dissipation per inverter stage for the different supply voltages.

$$P = f \cdot C \cdot V_{DD}^2 = f \cdot (10 \cdot 10^{-12}) \cdot V_{DD}^2$$

V_{DD} [V]	f	P
3		
5	24.044266 MHz	0.00601 W
7	54.659806 MHz	0.02679 W
10	121.37137 MHz	0.12137 W

3. Add a 50pF load capacitor to each inverter of the 3-stage ring oscillator and measure the oscillation frequency and determine the propagation delay per inverter for a power supply of V_{DD} *= 5.0V*





f = 1.3880071MHz

$$t_d = \frac{1}{2Nf} = \frac{1}{2 \cdot 3 \cdot 1.388M} = 120.07ns$$

4. What is the effect of the capacitive load on the propagation delay and the oscillation frequency?

Higher the capacitive load, oscillation frequency gets smaller and propagation delay gets larger.

5. What is the effect of the capacitive load and the power supply on the power dissipation?
Higher the capacitive load, increases the power dissipation. Also, when the power supply is increased, the power dissipation increases.

6.1.4 Problem 4: Logic Gate

Design a XOR (exclusive OR) logic gate. The gate should be realized by using a pull-up and a pull-down network. Only if one of the input signals is getting high the output signal is getting high. If both input signals are getting high the output signals is getting low. Use LTSpice to show the circuit. Simulate to verify the function.