BIRZEIT UNIVERSITY

Faculty of Engineering & Technology – Electrical & Computer Engineering Department
Digital Systems ENCS2340

HDL Homework

Due Saturday, June 11, 2022

This project is to be done individually.
1) You need to submit your codes.
2) Write a report for your results by providing the code and the simulation results of every component as well as the whole system.
NOTE:
• The grading of the project will be via discussion.
• This project should be implemented in Verilog HDL using Quartus software DO NOT:
• Give/receive code or proofs to/from other students
• Use Google to find solutions for assignment
DO:
• Meet with other students to discuss the project (it is best not to take any notes during such meetings, and to re-work project on your own)
• Use online resources (e.g. Wikipedia) to understand the concepts needed to solve the project

Q1: Given the following Combinational circuit, Use Verilog HDL on Quartus tool to
a. Implement the 1-bit adder and use it to build 4-bit adder structurally // this module name must be your last name

b. Implement the MUX2x1 and then use it to build the Quad MUX 2x1 structurally. this module name must be your first name

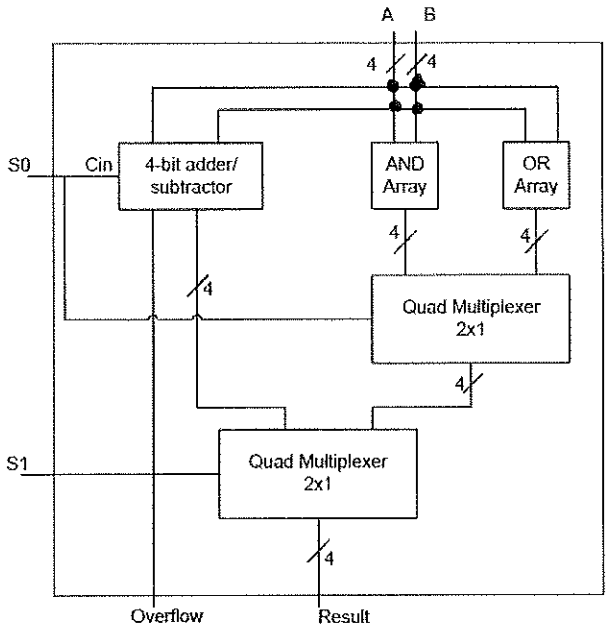
c. Implement the 4-bit OR Array

d. Implement the 4-bit AND Array

e. Use the blocks you implemented in the parts above to build the final system shown in the figure below. // this module name must be your university number

f. You should show simulation results for each of the above parts

AND array = 4 and
OR " = 4 OR



In addition to building the Quartus project, you need to write down one report for **each student** that includes the following items:

1. System Design.
2. Verilog code.
3. Simulation results.

There would be a discussion for each project with date allocated by the instructors.
Note: There is no group work

Note: Screenshot is not allowed in writing the code (copy the code from Quartus software)