University of Leeds
School of Electronic and Electrical Engineering

# ELEC5870M Interim Report

## Fabrication of Enhancement pHEMT Devices via Gate Recession

**Student:** Harry Carless
**Student ID:** 201508537

**Supervisor:** Dr Christopher Wood
**Assessor:** Mr Rob Farr

# Abstract

Abstract goes here

# Contents

# List of Figures

# CHAPTER 1

# Introduction and Technical Background

## 1.1 Motivation and Context

High-electron-mobility transistors (HEMTs) and their pseudomorphic variants (pHEMTs) are fundamental to many modern high-frequency and high-performance electronic systems. Their exceptional electron mobility and low parasitic capacitance make them indispensable in microwave amplifiers, radar receivers, satellite communications, and other circuits requiring high gain and low noise. These advantages arise from the formation of a two-dimensional electron gas (2DEG) within a III–V heterostructure, typically gallium arsenide (GaAs) with an aluminium gallium arsenide (AlGaAs) barrier. The resulting high carrier velocity and low scattering rates allow significantly faster operation than equivalent silicon-based devices.

Although HEMTs dominate within analogue and radio-frequency domains, their use in digital logic has remained limited. The majority of GaAs-based field-effect transistors operate in depletion mode ($D$-mode), meaning that they conduct current at zero gate bias and must be driven negatively to turn off. Logic circuits constructed solely from depletion-mode transistors suffer from high static power dissipation, incomplete switching, and restricted noise margins. Enhancement-mode ($E$-mode) devices, in contrast, remain non-conductive at zero bias and switch on only when a positive gate voltage is applied; these characteristics are desirable for logic implementation, providing defined logic levels and low static power.

To realise efficient GaAs logic, both device types are required. Complementary operation between depletion and enhancement-mode transistors underpins logic families such as direct-coupled FET logic (DCFL) and enhancement/depletion-load logic. The depletion device provides a passive load, while the enhancement device acts as the active pull-down element. Together they enable rail-to-rail voltage swings and reduced power consumption. However, achieving reliable enhancement-mode behaviour within standard GaAs fabrication processes remains challenging.

## 1.2 Rationale for Project Direction

During the early phase of this project, sixteen depletion-mode pHEMTs were fabricated and characterised in the Leeds Nanotechnology Cleanroom. The devices exhibited threshold voltages of approximately $-0.9$ V and peak transconductances of around 3 mS, confirming that the existing process yields high-quality depletion-mode transistors. While these results established a solid baseline, they also highlighted a key limitation: the absence of enhancement-mode devices restricts any exploration of complementary logic structures.

A review of existing literature on GaAs logic indicates that enhancement-mode behaviour can be induced through modification of the barrier region above the 2DEG. Techniques reported include double-recess etching of the AlGaAs barrier[1], platinum gate sinking to locally increase the Schottky barrier height[2], and dielectric interface engineering. Many of these methods depend on epitaxial wafers containing dedicated etch-stop layers or require high-temperature processing beyond the capabilities of the Leeds cleanroom. Consequently, a practical question arises: can enhancement-mode operation be achieved on a standard GaAs pHEMT wafer, without an etch-stop, through precise control of the gate recess process?

This question defines the central motivation of the project. If successful, such a process would offer a low-cost and experimentally accessible route to complementary GaAs logic, broadening the capability of the cleanroom and contributing insight into the relationship between recess depth and threshold voltage.

## 1.3 Device Physics Background

A pseudomorphic HEMT consists of a GaAs channel beneath an AlGaAs donor layer. Electrons transfer from the donor layer into the GaAs, forming a two-dimensional electron gas (2DEG) at the heterojunction. The 2DEG provides a highly conductive channel whose carrier concentration is modulated by the Schottky gate potential. The threshold voltage, $V_{th}$, depends primarily on the gate–channel separation, barrier composition, and surface charge density.

In depletion-mode devices, the 2DEG exists at zero gate bias, and a negative voltage is required to deplete the carriers and switch the device off. In enhancement-mode devices, the 2DEG is fully depleted when $V_G = 0$, and a positive voltage is required to induce conduction. One of the most effective ways to shift the threshold voltage towards positive values is to recess the gate. By carefully etching away a controlled thickness of the AlGaAs barrier, the gate potential gains stronger electrostatic influence over the channel, resulting in a shallower depletion region and a positive shift in $V_{th}$. Excessive etching, however, increases leakage and roughens the surface, whereas insufficient etching yields little or no threshold shift. The process therefore demands precise control at nanometre-scale depths.

[*A cross-section of a pHEMT structure to be included to illustrate the 2DEG formation and the effect of a recessed gate region on the electrostatic profile*]

## 1.4 Project Aim and Significance

The aim of this project is to investigate the feasibility of achieving enhancement-mode behaviour in GaAs-based pHEMTs through controlled gate recessing using the equipment available within the Leeds Nanotechnology Cleanroom. The work involves calibrating etch rates, fabricating transistors with systematically varied recess depths, and evaluating the resulting electrical characteristics. From this, an empirical relationship between recess depth and threshold voltage will be derived.

The broader significance extends beyond the immediate fabrication results. Establishing enhancement-mode operation without an etch-stop would demonstrate a viable route towards complementary GaAs logic using existing cleanroom infrastructure. This would enable the future design and testing of logic cells such as inverters and NAND gates composed of both depletion- and enhancement-mode devices. The findings will also contribute to a deeper understanding of threshold-voltage engineering, surface passivation, and process sensitivity in III–V semiconductor technology.

# CHAPTER 2

# Literature Review

# CHAPTER 3

# Experimental Work to Date

## 3.1 Depletion-Mode HEMT Fabrication and Testing

Summarise the training run and provide a succinct fabrication flow.

# CHAPTER 4

# Reflection and Project Management

# CHAPTER 5

# Plans for Semester 2

## 5.1 Gantt Chart Testing for Timeplan

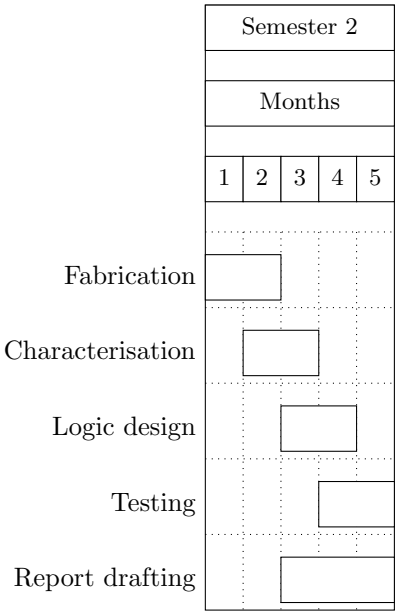


**Figure 5.1:** Indicative Semester 2 plan; adjust dates and scope as milestones firm up.

A high-level plan is shown in Figure 5.1.

# Bibliography

[1] A. Hsieh and Others, “Enhancement-mode algaas/gaas phemts via double-recess structure,” *Journal of Electronic Materials*, 2004. Placeholder entry—update with full bibliographic details.

[2] B. Chu and Others, “Positive-threshold phemts using platinum gate sinking,” *IEEE Transactions on Electron Devices*, 2007. Placeholder entry—update with full bibliographic details.

# APPENDIX A

## Additional Figures

# APPENDIX B

## Code and Process Flow