University of Leeds
School of Electronic and Electrical Engineering

ELEC5870M Interim Report

Fabrication of Enhancement Mode HEMT Devices via Gate Recession

Student: Harry Carless
Student ID: 201508537

Supervisor: Dr Christopher Wood
Assessor: Mr Rob Farr

Abstract

Abstract goes here

Acknowledgements

Abbreviations

2DEG	Two-dimensional electron gas
HEMT	High-electron-mobility transistor

Contents

List of Tables

List of Figures

CHAPTER 1

Introduction

Modern communication, sensing and microwave systems impose increasingly demanding requirements on the semiconductor devices that form their front-end signal paths. Higher operating frequencies, tighter noise constraints and strict linearity targets continue to push transistor technologies beyond the capabilities of many silicon-based platforms. Although silicon processes have made notable progress in recent years, they do not always provide the carrier mobility, noise performance or high-frequency gain required in performance-critical microwave and millimetre-wave applications.

III–V High–Electron–Mobility Transistors (HEMTs) play a central role in addressing these challenges. Their heterostructure–based design creates a highly conductive channel at the interface between two semiconductor layers with different bandgaps. At this interface a two–dimensional electron gas (2DEG) forms, supporting exceptionally high carrier mobility. The resulting strong transconductance, stable high–frequency behaviour and low–noise performance have firmly established HEMTs as core devices throughout microwave and millimetre–wave circuit design.

Research activity within the field has increasingly shifted toward gallium nitride (GaN) HEMTs, driven by the material properties enabled by its wide bandgap. GaN supports high breakdown voltages, strong power–handling capability and robust operation under large electric fields, making it the preferred choice for many high–power and high–linearity applications [cite needed]. Despite this growing dominance, gallium arsenide (GaAs) HEMTs remain one of the most mature and well characterised III–V transistor platforms. Their stability, extensive documentation and long industrial history continue to make them an invaluable system for studying the relationships between heterostructure design, device architecture and electrical behaviour.

For the purposes of this project, GaAs presents clear practical and technical advantages. The Leeds Nanotechnology Cleanroom maintains established, reliable processes for GaAs/AlGaAs heterostructures, and suitable wafers are readily available with reproducible epitaxial quality [1]. This provides a controlled environment in which HEMT structures can be fabricated and analysed systematically. The work undertaken here aims to investigate how variations in device structure influence key electrical characteristics, including threshold voltage, transconductance, leakage behaviour and the overall conduction profile of the device. The intention is to determine how specific structural changes translate into measurable shifts in device performance, building a clear link between fabrication choices and the resulting electrical behaviour.

CHAPTER 2

Technical Background

2.1 Overview of GaAs/AlGaAs HEMTs

In the GaAs/AlGaAs HEMTs used in this project, the interface between the GaAs channel layer and the overlying AlGaAs barrier produces a discontinuity in the conduction band because the two materials have different bandgaps. This offset creates a potential well on the GaAs side of the junction. Electrons supplied by silicon donors in the modulation–doped AlGaAs layer transfer into this well and accumulate to form the 2DEG that serves as the conducting channel. This interfacial 2DEG is the defining feature of the GaAs/AlGaAs HEMT structure [2].

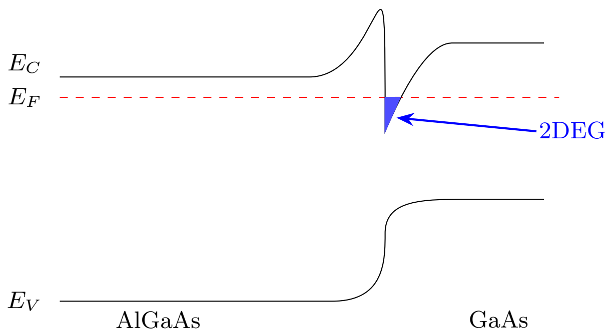

Figure 2.1: Conduction and valence band alignment at the AlGaAs/GaAs interface showing band bending and the resulting two-dimensional electron gas (2DEG) in a quantum well.

2.2 The GaAs/AlGaAs Heterostructure

2.3 Practical Device Layers and Gate Structure

2.4 HEMT Operation

2.5 Summary

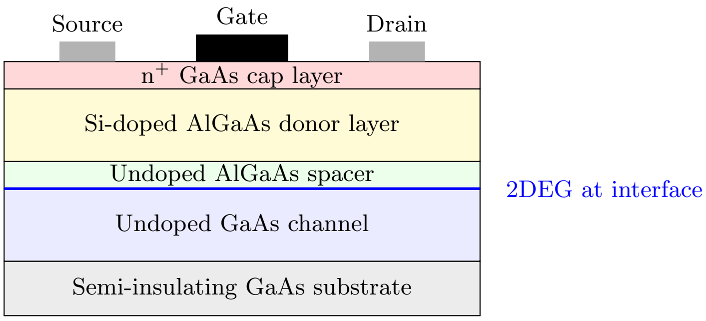

Figure 2.2: Cross-section of the GaAs/AlGaAs HEMT used in this project (not to scale).

CHAPTER 3

Fabrication of Depletion-Mode pHEMT Devices

3.1 Overview of the Fabrication Workflow

3.2 Mesa Definition

3.3 Ohmic Contact Formation

3.4 Gate Metallisation

3.5 Final Device Completion and Inspection

3.6 Summary of Fabricated Devices

3.7 Key Technical Lessons Learned

CHAPTER 4

Electrical Characterisation and Critical Analysis

CHAPTER 5

Exploration of Enhancement-Mode HEMT Devices

CHAPTER 6

Reflection and Project Management

6.1 Summary of Progress

6.2 Challenges and Adaptations

6.3 Skills Developed

6.4 Lessons for Semester Two

CHAPTER 7

Semester Two Plan

7.1 Gantt Chart

7.2 Planned Technical Deliverables

7.3 Risk Mitigation Strategy

Bibliography

[1] The University of Leeds, "Leeds nanotechnology cleanroom process gallery." Avaliable at: https://cleanroom.leeds.ac.uk/.

[2] W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HEMTs.* John Wiley and Sons, 1999.

APPENDIX A

Additional Figures

APPENDIX B

Code and Process Flow