University of Leeds
School of Electronic and Electrical Engineering

ELEC5870M Interim Report

Fabrication of Enhancement Mode pHEMT Devices via Gate Recession

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Abstract

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CHAPTER 1

Introduction

1.1 Context and Motivation

Modern electronic and communication systems impose increasingly demanding requirements on the devices that form their signal paths. Higher carrier frequencies, lower permissible noise levels, stricter linearity constraints and improved power efficiency are now expected. At the device level, these system requirements manifest as targets for cut-off frequency, noise figure, gain and power handling that conventional silicon technologies cannot always achieve.

High-electron-mobility transistors meet many of these system requirements through the use of a carefully engineered heterojunction, which is the interface between two semiconductor materials with different band structures. This band discontinuity causes electrons to collect in a very thin region at the heterojunction, creating a highly mobile sheet of charge carriers known as a two-dimensional electron gas (2DEG). The key advantage of this arrangement is that the 2DEG forms without the need to place donor atoms directly in the conduction path. In contrast to MESFETs, where electrons move through a doped channel, the absence of ionised impurities in a HEMT channel greatly reduces Coulomb scattering [1]. As a result, electrons can move more freely, giving the device high mobility, high transconductance and predictable behaviour at high frequencies. These characteristics allow HEMTs to operate reliably across a broad frequency range, typically from around 1 GHz to beyond 100 GHz [2], making them well suited to low-noise amplifiers, receiver front ends and other high-frequency subsystems.

Within this context, it is necessary to understand how the structure and processing of III–V HEMTs influence their electrical behaviour. Practical device performance is shaped not only by the underlying material system, but also by the fabrication steps used to define the channel, contacts and gate. Engaging directly with these processes provides a clearer view of how device characteristics emerge from both design and implementation. This interim report therefore introduces the key principles that underpin HEMT operation and presents the fabrication and analysis of GaAs-based pseudomorphic III–V HEMT devices produced during the first phase of the project.

1.2 Importance of III–V HEMTs

III–V compound semiconductors play a central role in enabling the performance characteristics associated with HEMT devices. Materials such as GaAs, InP and GaN possess band structures and carrier transport properties that support high-frequency operation, low noise and, in some cases, high power density. [2] Their relatively low effective electron mass and favourable mobility characteristics provide a foundation for transistor behaviour that is difficult to achieve with silicon CMOS or SiGe bipolar processes over the same frequency range. [**?**]

The heterostructure engineering available within III–V systems allows precise control over carrier confinement, channel composition and interface quality. By separating charge carriers from their parent dopants, these structures sustain mobility values that directly translate into high transconductance and improved gain at microwave frequencies. As a result, III–V HEMTs continue to serve key functions in low-noise receivers, high-frequency amplifiers and specialist instrumentation.

1.3 Current Landscape and Relevance

Although silicon RF technologies have progressed significantly, particularly in CMOS and SiGe BiCMOS platforms, III–V HEMTs remain important in domains where the highest noise performance, highest frequency operation or highest power density are required. Their continued use in satellite commu-

nication payloads, microwave backhaul links, scientific instrumentation and radar receivers reflects the practical advantages of III–V material systems in these regimes.

Contemporary research and industry practice continue to refine III–V device structures, epitaxial growth methods and fabrication processes to improve linearity, noise behaviour and frequency response. Even where silicon-based technologies dominate large-volume commercial applications, III–V HEMTs retain a critical role in performance-driven systems that cannot rely solely on silicon.

1.4 Scope and Structure of the Report

This interim report introduces the fundamental operating principles of III–V HEMT devices and describes the fabrication and characterisation work completed during the first phase of the project. The report begins with the physical structure and behaviour of pseudomorphic HEMTs, followed by a summary of the cleanroom fabrication processes used to produce the devices analysed here. Their electrical characteristics are then examined through transfer behaviour, output curves, transconductance and threshold voltage extraction.

The final sections provide a reflection on project management and skills development, before outlining the planned technical work for the second semester.

CHAPTER 2

Technical Background

CHAPTER 3

Fabrication of Depletion-Mode pHEMT Devices

CHAPTER 4

Electrical Characterisation and Critical Analysis

CHAPTER 5

Exploration of Enhancement-Mode HEMT Devices

CHAPTER 6

Reflection and Project Management

CHAPTER 7

Semester Two Plan

Bibliography

[1] F. Ali and A. K. Gupta, *HEMTs and HBTs: Devices, Fabrication and Circuits*. Artech House Microwave Library, 1991.

[2] W. Liu, *Fundamentals of III-V Devices - HBTs, MESFETs, and HEMTs*. John Wiley and Sons, 1999.

APPENDIX A

Additional Figures

APPENDIX B

Code and Process Flow