

University of Leeds
School of Electronic and Electrical Engineering

ELEC5870M Interim Report

**Fabrication of Enhancement Mode HEMT Devices via Gate
Recession**

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Abstract

Abstract goes here

Acknowledgements

Revision History

Version	Date	Notes
0.1	–	Draft skeleton; content to be populated.

Abbreviations

2DEG	Two-dimensional electron gas
HEMT	High-electron-mobility transistor

Contents

Abstract	i
Acknowledgements	ii
Revision History	iii
Abbreviations	iv
1 Introduction	1
2 Technical Background	2
2.1 Overview of GaAs/AlGaAs HEMTs	2
2.2 The GaAs/AlGaAs Heterostructure	2
2.3 Formation and Properties of the Two-Dimensional Electron Gas	3
2.4 Practical Device Layers and Gate Structure	3
2.5 HEMT Operation	3
2.6 Summary	3
3 Fabrication of Depletion-Mode pHEMT Devices	4
3.1 Overview of the Fabrication Workflow	4
3.2 Mesa Definition	4
3.3 Ohmic Contact Formation	4
3.4 Gate Metallisation	4
3.5 Final Device Completion and Inspection	4
3.6 Summary of Fabricated Devices	4
3.7 Key Technical Lessons Learned	4
4 Electrical Characterisation and Critical Analysis	5
4.1 Measurement Setup	5
4.2 Output Characteristics (ID–VD)	5
4.3 Transfer Characteristics (ID–VG)	5
4.4 Gate Leakage Behaviour	5
4.5 Threshold-Voltage Extraction	5
4.6 Variability, Non-Idealities and Interpretation	5
4.7 Implications for Process Control and Device Behaviour	5

5	Exploration of Enhancement-Mode HEMT Devices	6
5.1	Motivation for Enhancement-Mode Operation	6
5.2	Mechanisms for Achieving Enhancement Mode	6
5.3	Challenges of Gate Recessing Without an Etch-Stop Layer	6
5.4	Proposed Fabrication Strategy for Semester Two	6
5.5	Ideal Outcomes and Target Behaviour	6
5.6	Logic Motivation and Stretch Goal	6
6	Reflection and Project Management	7
6.1	Summary of Progress	7
6.2	Challenges and Adaptations	7
6.3	Skills Developed	7
6.4	Lessons for Semester Two	7
7	Semester Two Plan	8
7.1	Gantt Chart	8
7.2	Planned Technical Deliverables	8
7.3	Risk Mitigation Strategy	8
	References	9
A	Additional Figures	10
B	Code and Process Flow	11

List of Tables

List of Figures

2.1	Conduction and valence band alignment at the AlGaAs/GaAs interface showing band bending and the resulting two-dimensional electron gas (2DEG).	2
2.2	Cross-section of the GaAs/AlGaAs HEMT used in this project (not to scale). . .	3

CHAPTER 1

Introduction

Modern communication, sensing and microwave systems impose increasingly demanding requirements on the semiconductor devices that form their front-end signal paths. Higher operating frequencies, tighter noise constraints and strict linearity targets continue to push transistor technologies beyond the capabilities of many silicon-based platforms. Although silicon processes have made notable progress in recent years, they do not always provide the carrier mobility, noise performance or high-frequency gain required in performance-critical microwave and millimetre-wave applications.

III–V High-Electron-Mobility Transistors (HEMTs) play a central role in addressing these challenges. Their favourable material properties, particularly the high electron mobility achievable within modulation-doped heterostructures, enable predictable, low-noise operation across wide frequency ranges [1]. As a result, HEMTs remain fundamental to satellite communication payloads, radar receivers, millimetre-wave backhaul links and a range of scientific and instrumentation systems where stringent performance metrics cannot be met by silicon technologies alone.

Research activity within the field has increasingly shifted toward gallium nitride (GaN) HEMTs [cite needed], driven by their wide bandgap, high breakdown field and strong power-handling capabilities. These characteristics make GaN the preferred option for many high-power and high-linearity applications [cite needed]. Even so, GaAs/AlGaAs HEMTs remain one of the most mature, well-understood and experimentally accessible III–V transistor technologies. Their stability, extensive documentation and long industrial history continue to make them an invaluable platform for studying the fundamental relationships between heterostructure design, device architecture and electrical behaviour.

For the purposes of this project, GaAs presents clear practical and technical advantages. The Leeds Nanotechnology Cleanroom maintains established, reliable processes for GaAs/AlGaAs heterostructures, and suitable wafers are readily available with reproducible epitaxial quality [2]. This provides a controlled environment in which HEMT structures can be fabricated and analysed systematically. The work undertaken here aims to investigate how variations in device structure influence key electrical characteristics, including threshold voltage, transconductance, leakage behaviour and the general conduction profile of the device. By examining how different architectural choices and design modifications affect these metrics, the project seeks to develop a coherent understanding of how HEMTs can be engineered to meet diverse functional requirements within high-frequency systems.

CHAPTER 2

Technical Background

2.1 Overview of GaAs/AlGaAs HEMTs

High-electron-mobility transistors employ a semiconductor heterojunction to create a confined, low-scattering electron channel. In the GaAs/AlGaAs material system used in this project, a discontinuity in the conduction band establishes a potential well at the interface. Electrons supplied by the doped AlGaAs layer accumulate within this well and form a two-dimensional electron gas (2DEG). Because the GaAs channel is undoped, the absence of ionised impurities suppresses Coulomb scattering, leading to high electron mobility and predictable high-frequency behaviour [3].

The epitaxial structure used in this project is a standard, lattice-matched GaAs/AlGaAs heterostructure. Unlike pseudomorphic devices that rely on strained InGaAs channels, this system achieves confinement purely through band offsets, ensuring stable material behaviour without the additional complexity of strain engineering.

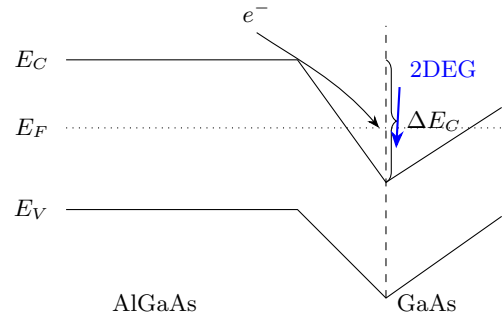


Figure 2.1: Conduction and valence band alignment at the AlGaAs/GaAs interface showing band bending and the resulting two-dimensional electron gas (2DEG).

2.2 The GaAs/AlGaAs Heterostructure

The heterostructure consists of three active layers. The undoped GaAs channel forms the conduction path for the 2DEG. Its crystalline uniformity and lack of intentional impurities suppress scattering and enable high mobility. Above the channel lies the undoped AlGaAs spacer, which physically separates the electrons from the ionised donors in the doped barrier. Its thickness determines the balance between mobility and electrostatic coupling. The Si-doped AlGaAs donor layer then supplies electrons and establishes the conduction band offset needed to form the potential well at the interface.

Together, these layers determine the electron density, mobility and confinement properties that underpin HEMT behaviour.

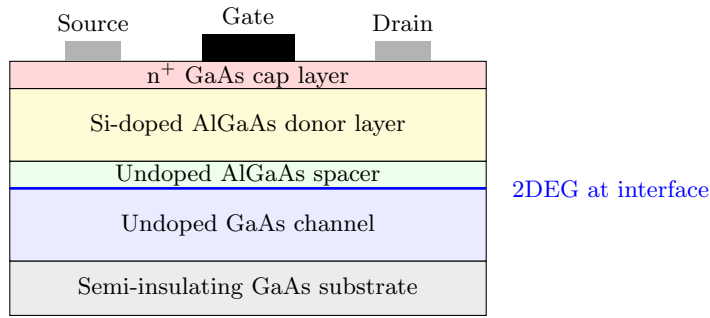


Figure 2.2: Cross-section of the GaAs/AlGaAs HEMT used in this project (not to scale).

2.3 Formation and Properties of the Two-Dimensional Electron Gas

Electrons diffuse from the doped AlGaAs barrier into the undoped GaAs channel until equilibrium is established. The conduction band offset forms a narrow, triangular potential well that confines the carriers to the interface. Because the channel contains no ionised donors, scattering from charged impurities is largely eliminated [1]. Mobility is therefore limited primarily by phonon interactions and interface roughness, both of which are less severe mechanisms. This combination of strong confinement and reduced scattering results in a high-mobility electron sheet that supports strong transconductance and predictable current–voltage behaviour.

2.4 Practical Device Layers and Gate Structure

Above the active heterostructure sits the heavily doped GaAs cap. Its high doping level enables reliable formation of low-resistance ohmic contacts when the AuGe/Ni/Au metallisation stack is alloyed, while also providing a uniform, conductive surface for lithographic patterning.

The Ti/Au Schottky gate controls the depletion region within the AlGaAs barrier. Adjusting the gate bias modifies the electric field beneath the gate and therefore the electron density in the 2DEG. The effective gate-to-channel separation plays a critical role in determining the threshold voltage, transconductance and linearity of the device. Unlike MOSFETs, HEMTs do not employ an insulating oxide; control is achieved purely through depletion of the channel.

2.5 HEMT Operation

HEMT operation is governed by the modulation of the 2DEG by the Schottky gate. A negative gate bias expands the depletion region and reduces channel conductivity. As the drain–source voltage increases, the electric field at the drain side causes local depletion, eventually leading to pinch-off and current saturation. The combination of high channel mobility and strong electrostatic coupling between the gate and channel results in high transconductance, efficient current modulation and favourable high-frequency behaviour.

2.6 Summary

The GaAs/AlGaAs HEMT derives its performance from engineered carrier confinement, spatial separation from ionised donors and the electrostatic control provided by the Schottky gate. These characteristics form the technical foundation for the fabrication and characterisation work presented in the subsequent chapters.

CHAPTER 3

Fabrication of Depletion-Mode pHEMT Devices

- 3.1 Overview of the Fabrication Workflow
- 3.2 Mesa Definition
- 3.3 Ohmic Contact Formation
- 3.4 Gate Metallisation
- 3.5 Final Device Completion and Inspection
- 3.6 Summary of Fabricated Devices
- 3.7 Key Technical Lessons Learned

CHAPTER 4

Electrical Characterisation and Critical Analysis

4.1 Measurement Setup

4.2 Output Characteristics (ID–VD)

4.3 Transfer Characteristics (ID–VG)

4.4 Gate Leakage Behaviour

4.5 Threshold-Voltage Extraction

4.6 Variability, Non-Idealities and Interpretation

4.7 Implications for Process Control and Device Behaviour

CHAPTER 5

Exploration of Enhancement-Mode HEMT Devices

- 5.1 Motivation for Enhancement-Mode Operation
- 5.2 Mechanisms for Achieving Enhancement Mode
- 5.3 Challenges of Gate Recessing Without an Etch-Stop Layer
- 5.4 Proposed Fabrication Strategy for Semester Two
- 5.5 Ideal Outcomes and Target Behaviour
- 5.6 Logic Motivation and Stretch Goal

CHAPTER 6

Reflection and Project Management

6.1 Summary of Progress

6.2 Challenges and Adaptations

6.3 Skills Developed

6.4 Lessons for Semester Two

CHAPTER 7

Semester Two Plan

7.1 Gantt Chart

7.2 Planned Technical Deliverables

7.3 Risk Mitigation Strategy

Bibliography

- [1] F. Ali and A. K. Gupta, *HEMTs and HBTs: Devices, Fabrication and Circuits*. Artech House, 1991.
- [2] The University of Leeds, “Leeds nanotechnology cleanroom process gallery.” Available at: <https://cleanroom.leeds.ac.uk/>.
- [3] W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HEMTs*. John Wiley and Sons, 1999.

APPENDIX A

Additional Figures

APPENDIX B

Code and Process Flow