University of Leeds
School of Electronic and Electrical Engineering

ELEC5870M Interim Report

Fabrication of Enhancement Mode HEMT Devices via Gate Recession

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Abstract

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Acknowledgements

Revision History

Version	Date	Notes
0.1	–	Draft skeleton; content to be populated.

Abbreviations

2DEG	Two-dimensional electron gas
HEMT	High-electron-mobility transistor

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CHAPTER 1

Introduction

1.1 Context and Motivation

Modern communication, sensing and microwave systems place increasing demands on the semiconductor devices that form their front-end signal paths. Higher operating frequencies, lower permissible noise figures and stricter linearity requirements all intensify the performance constraints on transistor technologies. Although silicon-based RF platforms have progressed considerably, they do not always deliver the mobility, noise performance or gain required in performance-driven microwave applications.

III–V high-electron-mobility transistors (HEMTs) continue to address this gap. Their favourable material properties, including high electron mobility and low intrinsic noise, support predictable and efficient operation at microwave and millimetre-wave frequencies [1]. As a result, HEMTs remain essential in systems such as satellite communication payloads, radar receivers, millimetre-wave backhaul links and scientific instrumentation, where stringent noise and frequency requirements cannot be met by silicon alone.

1.2 Relevance of GaAs/AlGaAs HEMTs to This Project

The GaAs/AlGaAs HEMT is one of the most established III–V transistor architectures. Its behaviour is strongly influenced by the quality of the heterostructure and the precision of the fabrication sequence, making it well-suited to a project that aims to evaluate how material properties and process decisions shape device performance. In this work, GaAs/AlGaAs HEMTs are fabricated within the Leeds Nanotechnology Cleanroom to gain practical experience with device definition, assess process reproducibility and examine the electrical characteristics that emerge from the epitaxial structure.

A central motivation is the transition from the depletion-mode operation inherent to the supplied wafer structure toward enhancement-mode behaviour through controlled gate recessing. Achieving enhancement mode requires reducing the effective gate-to-channel separation while maintaining interface quality. This places strict demands on etch controllability, surface integrity and uniformity across devices. Establishing the relationship between recess depth and threshold voltage therefore represents a key technical objective.

1.3 Project Motivation and Aims

The first stage of the project focuses on fabricating and characterising baseline depletion-mode GaAs/AlGaAs HEMTs. These devices provide the necessary framework for assessing the heterostructure, validating the fabrication workflow and establishing the electrical measurement setup. A major aim is to understand how threshold voltage, transconductance and gate leakage

relate to the epitaxial design and the process conditions used to form the contacts and gate.

Building on this foundation, the project then seeks to develop a controlled gate-recess process capable of shifting the threshold voltage into the enhancement regime. This requires a systematic study of etch depth, surface behaviour and process reproducibility. A longer-term motivation is the eventual construction of simple logic elements using enhancement-mode GaAs-based devices, since enhancement-mode operation provides defined switching thresholds and more flexible circuit behaviour appropriate for digital logic.

CHAPTER 2

Technical Background

2.1 Overview of GaAs/AlGaAs HEMTs

High-electron-mobility transistors employ a semiconductor heterojunction to create a confined, low-scattering electron channel. In the GaAs/AlGaAs material system used in this project, a discontinuity in the conduction band establishes a potential well at the interface. Electrons supplied by the doped AlGaAs layer accumulate within this well and form a two-dimensional electron gas (2DEG). Because the GaAs channel is undoped, the absence of ionised impurities suppresses Coulomb scattering, leading to high electron mobility and predictable high-frequency behaviour [2].

The epitaxial structure used in this project is a standard, lattice-matched GaAs/AlGaAs heterostructure. Unlike pseudomorphic devices that rely on strained InGaAs channels, this system achieves confinement purely through band offsets, ensuring stable material behaviour without the additional complexity of strain engineering.

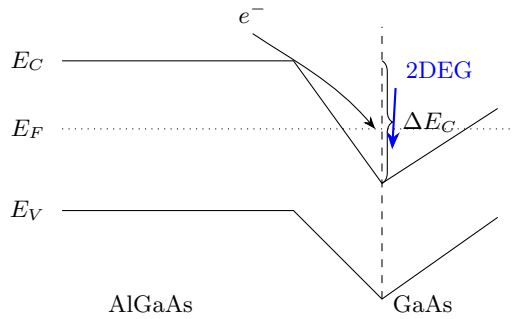

Figure 2.1: Conduction and valence band alignment at the AlGaAs/GaAs interface showing band bending and the resulting two-dimensional electron gas (2DEG).

2.2 The GaAs/AlGaAs Heterostructure

The heterostructure consists of three active layers. The undoped GaAs channel forms the conduction path for the 2DEG. Its crystalline uniformity and lack of intentional impurities suppress scattering and enable high mobility. Above the channel lies the undoped AlGaAs spacer, which physically separates the electrons from the ionised donors in the doped barrier. Its thickness determines the balance between mobility and electrostatic coupling. The Si-doped AlGaAs donor layer then supplies electrons and establishes the conduction band offset needed to form the potential well at the interface.

Together, these layers determine the electron density, mobility and confinement properties that underpin HEMT behaviour.

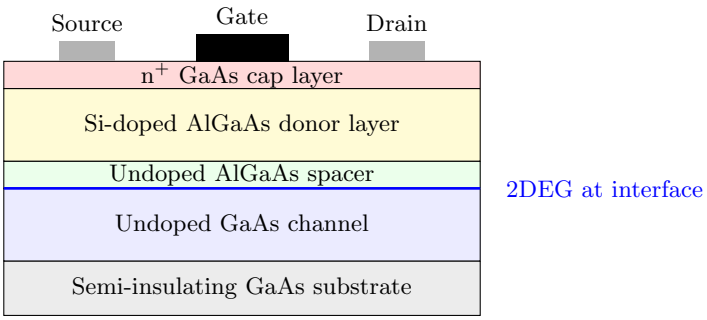

Figure 2.2: Cross-section of the GaAs/AlGaAs HEMT used in this project (not to scale).

2.3 Formation and Properties of the Two-Dimensional Electron Gas

Electrons diffuse from the doped AlGaAs barrier into the undoped GaAs channel until equilibrium is established. The conduction band offset forms a narrow, triangular potential well that confines the carriers to the interface. Because the channel contains no ionised donors, scattering from charged impurities is largely eliminated [1]. Mobility is therefore limited primarily by phonon interactions and interface roughness, both of which are less severe mechanisms. This combination of strong confinement and reduced scattering results in a high-mobility electron sheet that supports strong transconductance and predictable current–voltage behaviour.

2.4 Practical Device Layers and Gate Structure

Above the active heterostructure sits the heavily doped GaAs cap. Its high doping level enables reliable formation of low-resistance ohmic contacts when the AuGe/Ni/Au metallisation stack is alloyed, while also providing a uniform, conductive surface for lithographic patterning.

The Ti/Au Schottky gate controls the depletion region within the AlGaAs barrier. Adjusting the gate bias modifies the electric field beneath the gate and therefore the electron density in the 2DEG. The effective gate-to-channel separation plays a critical role in determining the threshold voltage, transconductance and linearity of the device. Unlike MOSFETs, HEMTs do not employ an insulating oxide; control is achieved purely through depletion of the channel.

2.5 HEMT Operation

HEMT operation is governed by the modulation of the 2DEG by the Schottky gate. A negative gate bias expands the depletion region and reduces channel conductivity. As the drain–source voltage increases, the electric field at the drain side causes local depletion, eventually leading to pinch-off and current saturation. The combination of high channel mobility and strong electrostatic coupling between the gate and channel results in high transconductance, efficient current modulation and favourable high-frequency behaviour.

2.6 Summary

The GaAs/AlGaAs HEMT derives its performance from engineered carrier confinement, spatial separation from ionised donors and the electrostatic control provided by the Schottky gate. These characteristics form the technical foundation for the fabrication and characterisation work presented in the subsequent chapters.

CHAPTER 3

Fabrication of Depletion-Mode pHEMT Devices

CHAPTER 4

Electrical Characterisation and Critical Analysis

CHAPTER 5

Exploration of Enhancement-Mode HEMT Devices

CHAPTER 6

Reflection and Project Management

CHAPTER 7

Semester Two Plan

Bibliography

[1] F. Ali and A. K. Gupta, *HEMTs and HBTs: Devices, Fabrication and Circuits.* Artech House, 1991.

[2] W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HEMTs.* John Wiley and Sons, 1999.

APPENDIX A

Additional Figures

APPENDIX B

Code and Process Flow