University of Leeds
School of Electronic and Electrical Engineering

ELEC5870M Interim Report

Fabrication of Enhancement Mode pHEMT Devices via Gate Recession

Student: Harry Carless
Student ID: 201508537

Supervisor: Dr Christopher Wood
Assessor: Mr Rob Farr

Abstract

The abstract provides a concise overview of the project motivation, methodology, key findings, and the implications of the work. Summaries typically span one paragraph (150–250 words) and should stand alone without references to figures or citations in the main body.

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CHAPTER 1

Introduction and Technical Background

1.1 Motivation and Context

This project investigates the feasibility of achieving enhancement-mode (e-mode) behaviour in GaAs-based pseudomorphic high-electron-mobility transistors (pHEMTs) using controlled gate recessing. While CMOS dominates general-purpose logic, III–V devices retain strong relevance in RF, mixed-signal, and radiation-hard domains owing to high carrier mobility and favourable transport. The central question is whether positive-threshold devices can be realised on GaAs without an explicit etch-stop layer—opening a pathway to logic topologies that leverage compound-semiconductor performance.

1.2 Device Physics Background

A pHEMT typically comprises a GaAs channel and an AlGaAs barrier that forms a two-dimensional electron gas (2DEG) at the heterointerface. A Schottky gate electrostatically modulates the channel. Depletion-mode (d-mode) operation arises when the channel is conductive at zero gate bias (negative threshold), whereas e-mode devices conduct only for positive gate bias. Gate recessing reduces gate-to-channel separation and can shift the threshold voltage, but is highly sensitive to surface states and processing chemistry.

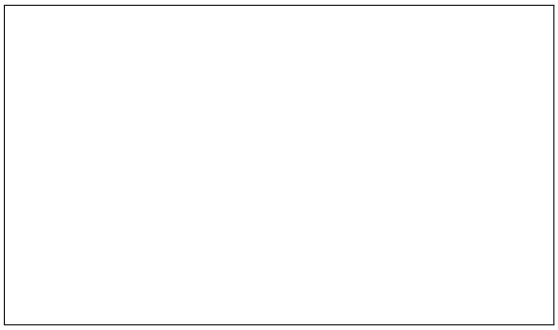

Figure 1.1: Simplified pHEMT cross-section showing gate, barrier, channel, and recess region. Replace with final schematic from your CAD/diagram tool.

1.3 Relevance to Logic

GaAs logic families (e.g., DCFL and e/d-load logic) benefit from devices with a positive threshold voltage. The project aims to fabricate and characterise recessed-gate pHEMTs that enable such topologies, providing an empirical link between recess depth and threshold voltage.

CHAPTER 2

Literature Review

2.1 Enhancement-Mode Methods

Reported routes to e-mode behaviour in AlGaAs/GaAs structures include double recess geometries and metallurgical gate approaches (e.g., Pt sinking). Double recess structures can yield uniform, positive thresholds with careful control of barrier thinning, while gate sinking modifies the effective Schottky barrier. Oxide/dielectric engineering also appears in the literature.

Representative works include [1, 2]. Update and expand this section with additional sources as your reading develops.

2.2 Comparative Analysis

Table 2.1: Comparison of enhancement-mode methods and practical considerations.

Method	Wafer needs	Pros	Cons	Local feasibility
Double recess	Etch control	Uniform V_{th}	Process complexity	High
Gate sinking	Specific metals	Simple flow	Metallurgical risk	Medium
Dielectric eng.	Deposition	Interface tuning	Additional tooling	Low–Med

A template for comparing techniques, wafer requirements, and local feasibility is provided in Table 2.1.

2.3 Identified Gap

There is limited reporting on controlled recessing without an etch-stop using a process flow similar to that available at Leeds. This work targets an empirical map of recess depth versus threshold voltage under those constraints.

CHAPTER 3

Experimental Work to Date

3.1 Depletion-Mode HEMT Fabrication and Testing

Summarise the training run and provide a succinct fabrication flow. Include one representative dataset (transfer and output characteristics) with captions that explain the key features and extracted parameters (e.g., $V_{\mathrm{th}} \approx -0.9\,\mathrm{V}$, $g_m \approx 3\,\mathrm{mS}$).

Figure 3.1: Representative transfer characteristic for d-mode HEMT. Replace with plot from the Python pipeline.

3.2 Python Data-Processing Pipeline

Briefly describe the CSV parsing, plotting, and parameter-extraction stages. Justify the pipeline for reproducibility and efficiency. Add a figure generated by the tool once available.

3.3 Enhancement-Mode Development (pHEMT)

Describe etch-rate calibration (gas mixture, pressure, time) and summarise profilometer measurements.

Table 3.1: Example recess depth calibration (replace with measured data).

Etch time (s)	Depth (nm)	Notes
10	–	calibration
20	–	calibration
30	–	device batch

Table 3.1 will be replaced with the measured relationship between etch time and recess depth. Include representative I–V and transfer curves indicating threshold shift, and discuss trade-offs (surface roughness, leakage). Document any process adjustments (post-etch clean, passivation).

3.4 Discussion

Compare recessed devices with the d-mode baseline, explain the physical origin of threshold shifts, and comment on reproducibility and process sensitivity.

CHAPTER 4

Reflection and Project Management

4.1 Technical Reflection

Summarise key technical learning: etch control, surface sensitivity, data integrity, and the discipline required in the cleanroom. Document challenges (equipment downtime, illness, coordination) and the impact on time management.

4.2 Project Management

Describe the supervision structure and risk management for a 45-credit module.

Table 4.1: Risk register (example fields; update with specifics).

Risk	Impact	Mitigation
Tool downtime	Schedule slip	Alternate slot, simulation fallback
Yield issues	Rework	Extra wafers, design margin

Table 4.1 will be completed with identified risks, impacts, and mitigations.

CHAPTER 5

Plans for Semester 2

5.1 Immediate Next Steps

Complete recessed-gate dataset analysis; derive an empirical relationship between threshold voltage and recess depth; fabricate final optimised devices.

5.2 Logic Demonstration Phase

Plan a DCFL inverter (and optional NAND) using measured device parameters. Outline simulation with extracted models, wire-bonding, and testing.

5.3 Time Plan

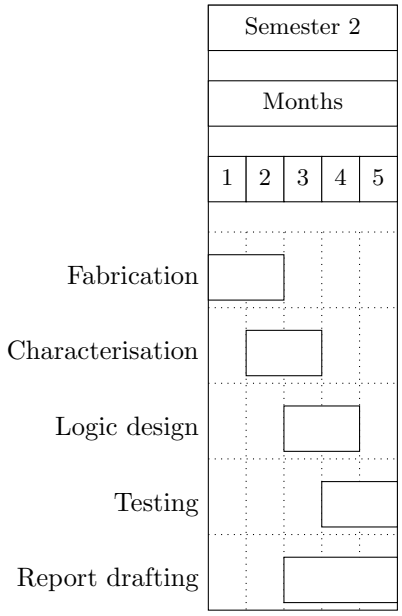

Figure 5.1: Indicative Semester 2 plan; adjust dates and scope as milestones firm up.

A high-level plan is shown in Figure 5.1.

Bibliography

[1] A. Hsieh and Others, “Enhancement-mode algaas/gaas phemts via double-recess structure,” *Journal of Electronic Materials*, 2004, placeholder entry—update with full bibliographic details.

[2] B. Chu and Others, “Positive-threshold phemts using platinum gate sinking,” *IEEE Transactions on Electron Devices*, 2007, placeholder entry—update with full bibliographic details.

APPENDIX A

Additional Figures

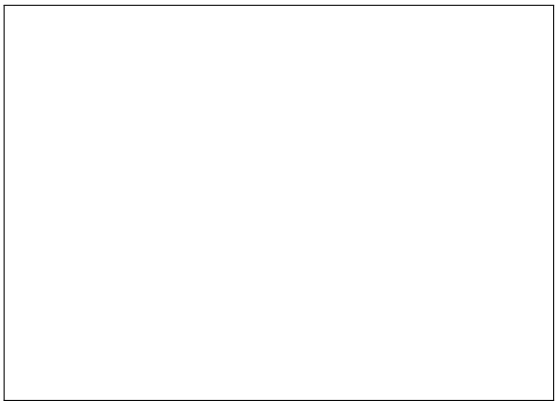

Figure A.1: Supplementary plot. Replace with final figure.

APPENDIX B

Code and Process Flow

B.1 Python Analysis Outline

Brief outline of the analysis pipeline and key scripts. Include code snippets or links to the repository as appropriate.

B.2 Cleanroom Process Summary

Summarise lithography, metallisation, and etch steps with key parameters.