University of Leeds
School of Electronic and Electrical Engineering

ELEC5870M Interim Report

Fabrication of Enhancement pHEMT Devices via Gate Recession

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Abstract

The abstract provides a concise overview of the project motivation, methodology, key findings, and the implications of the work. Summaries typically span one paragraph (150–250 words) and should stand alone without references to figures or citations in the main body.

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CHAPTER 1

Introduction and Technical Background

1.1 Motivation and Context

High-electron-mobility transistors (HEMTs) and their pseudomorphic variants (pHEMTs) are fundamental to many modern high-frequency and high-performance electronic systems. Their exceptional electron mobility and low parasitic capacitance make them indispensable in microwave amplifiers, radar receivers, satellite communications, and other circuits requiring high gain and low noise. These advantages arise from the formation of a two-dimensional electron gas (2DEG) within a III–V heterostructure, typically gallium arsenide (GaAs) with an aluminium gallium arsenide (AlGaAs) barrier. The resulting high carrier velocity and low scattering rates allow significantly faster operation than equivalent silicon-based devices.

Although HEMTs dominate within analogue and radio-frequency domains, their use in digital logic has remained limited. The majority of GaAs-based field-effect transistors operate in depletion mode (D-mode), meaning that they conduct current at zero gate bias and must be driven negatively to turn off. Logic circuits constructed solely from depletion-mode transistors suffer from high static power dissipation, incomplete switching, and restricted noise margins. Enhancement-mode (E-mode) devices, in contrast, remain non-conductive at zero bias and switch on only when a positive gate voltage is applied; these characteristics are desirable for logic implementation, providing defined logic levels and low static power.

To realise efficient GaAs logic, both device types are required. Complementary operation between depletion and enhancement-mode transistors underpins logic families such as direct-coupled FET logic (DCFL) and enhancement/depletion-load logic. The depletion device provides a passive load, while the enhancement device acts as the active pull-down element. Together they enable rail-to-rail voltage swings and reduced power consumption. However, achieving reliable enhancement-mode behaviour within standard GaAs fabrication processes remains challenging.

1.2 Rationale for Project Direction

During the early phase of this project, sixteen depletion-mode pHEMTs were fabricated and characterised in the Leeds Nanotechnology Cleanroom. The devices exhibited threshold voltages of approximately -0.9 V and peak transconductances of around 3 mS, confirming that the existing process yields high-quality depletion-mode transistors. While these results established a solid baseline, they also highlighted a key limitation: the absence of enhancement-mode devices restricts any exploration of complementary logic structures.

A review of existing literature on GaAs logic indicates that enhancement-mode behaviour can be induced through modification of the barrier region above the 2DEG. Techniques reported include double-recess etching of the AlGaAs barrier[1], platinum gate sinking to locally increase the Schottky barrier height[2], and dielectric interface engineering. Many of these methods depend on epitaxial wafers containing dedicated etch-stop layers or require high-temperature processing beyond the capabilities of the Leeds cleanroom. Consequently, a practical question arises: can enhancement-mode operation be achieved on a standard GaAs pHEMT wafer, without an etch-stop, through precise control of the gate recess process?

This question defines the central motivation of the project. If successful, such a process would offer a low-cost and experimentally accessible route to complementary GaAs logic, broadening the capability of the cleanroom and contributing insight into the relationship between recess depth and threshold voltage.

1.3 Device Physics Background

A pseudomorphic HEMT consists of a GaAs channel beneath an AlGaAs donor layer. Electrons transfer from the donor layer into the GaAs, forming a two-dimensional electron gas (2DEG) at the heterojunction. The 2DEG provides a highly conductive channel whose carrier concentration is modulated by the Schottky gate potential. The threshold voltage, V_{th}, depends primarily on the gate–channel separation, barrier composition, and surface charge density.

In depletion-mode devices, the 2DEG exists at zero gate bias, and a negative voltage is required to deplete the carriers and switch the device off. In enhancement-mode devices, the 2DEG is fully depleted when $V_G = 0$, and a positive voltage is required to induce conduction. One of the most effective ways to shift the threshold voltage towards positive values is to recess the gate. By carefully etching away a controlled thickness of the AlGaAs barrier, the gate potential gains stronger electrostatic influence over the channel, resulting in a shallower depletion region and a positive shift in V_{th}. Excessive etching, however, increases leakage and roughens the surface, whereas insufficient etching yields little or no threshold shift. The process therefore demands precise control at nanometre-scale depths.

[*A cross-section of a pHEMT structure to be included to illustrate the 2DEG formation and the effect of a recessed gate region on the electrostatic profile*]

1.4 Project Aim and Significance

The aim of this project is to investigate the feasibility of achieving enhancement-mode behaviour in GaAs-based pHEMTs through controlled gate recessing using the equipment available within the Leeds Nanotechnology Cleanroom. The work involves calibrating etch rates, fabricating transistors with systematically varied recess depths, and evaluating the resulting electrical characteristics. From this, an empirical relationship between recess depth and threshold voltage will be derived.

The broader significance extends beyond the immediate fabrication results. Establishing enhancement-mode operation without an etch-stop would demonstrate a viable route towards complementary GaAs logic using existing cleanroom infrastructure. This would enable the future design and testing of logic cells such as inverters and NAND gates composed of both depletion- and enhancement-mode devices. The findings will also contribute to a deeper understanding of threshold-voltage engineering, surface passivation, and process sensitivity in III–V semiconductor technology.

CHAPTER 2

Literature Review

2.1 Enhancement-Mode Methods

Reported routes to e-mode behaviour in AlGaAs/GaAs structures include double recess geometries and metallurgical gate approaches (e.g., Pt sinking). Double recess structures can yield uniform, positive thresholds with careful control of barrier thinning, while gate sinking modifies the effective Schottky barrier. Oxide/dielectric engineering also appears in the literature.

Representative works include [1, 2]. Update and expand this section with additional sources as your reading develops.

2.2 Comparative Analysis

A template for comparing techniques, wafer requirements, and local feasibility is provided in Table 2.1.

2.3 Identified Gap

There is limited reporting on controlled recessing without an etch-stop using a process flow similar to that available at Leeds. This work targets an empirical map of recess depth versus threshold voltage under those constraints.

Table 2.1: Comparison of enhancement-mode methods and practical considerations.

Method	Wafer needs	Pros	Cons	Local feasibility
Double recess	Etch control	Uniform V_{th}	Process complexity	High
Gate sinking	Specific metals	Simple flow	Metallurgical risk	Medium
Dielectric eng.	Deposition	Interface tuning	Additional tooling	Low–Med

CHAPTER 3

Experimental Work to Date

3.1 Depletion-Mode HEMT Fabrication and Testing

Summarise the training run and provide a succinct fabrication flow. Include one representative dataset (transfer and output characteristics) with captions that explain the key features and extracted parameters (e.g., $V_{\mathrm{th}} \approx -0.9\,\mathrm{V}$, $g_m \approx 3\,\mathrm{mS}$).

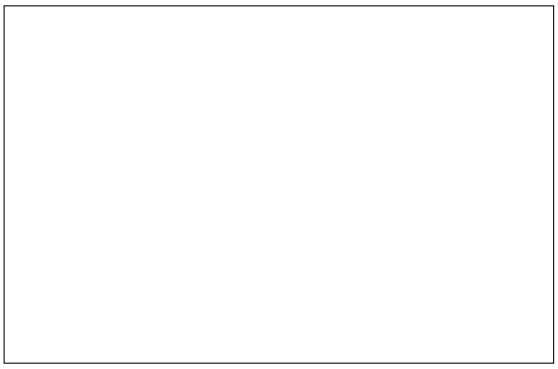

Figure 3.1: Representative transfer characteristic for d-mode HEMT. Replace with plot from the Python pipeline.

3.2 Python Data-Processing Pipeline

Briefly describe the CSV parsing, plotting, and parameter-extraction stages. Justify the pipeline for reproducibility and efficiency. Add a figure generated by the tool once available.

3.3 Enhancement-Mode Development (pHEMT)

Describe etch-rate calibration (gas mixture, pressure, time) and summarise profilometer measurements.

Table 3.1: Example recess depth calibration (replace with measured data).

Etch time (s)	Depth (nm)	Notes
10	–	calibration
20	–	calibration
30	–	device batch

Table 3.1 will be replaced with the measured relationship between etch time and recess depth. Include representative I–V and transfer curves indicating threshold shift, and discuss trade-offs (surface roughness, leakage). Document any process adjustments (post-etch clean, passivation).

3.4 Discussion

Compare recessed devices with the d-mode baseline, explain the physical origin of threshold shifts, and comment on reproducibility and process sensitivity.

CHAPTER 4

Reflection and Project Management

4.1 Technical Reflection

Summarise key technical learning: etch control, surface sensitivity, data integrity, and the discipline required in the cleanroom. Document challenges (equipment downtime, illness, coordination) and the impact on time management.

4.2 Project Management

Describe the supervision structure and risk management for a 45-credit module.

Table 4.1: Risk register (example fields; update with specifics).

Risk	Impact	Mitigation
Tool downtime	Schedule slip	Alternate slot, simulation fallback
Yield issues	Rework	Extra wafers, design margin

Table 4.1 will be completed with identified risks, impacts, and mitigations.

CHAPTER 5

Plans for Semester 2

5.1 Immediate Next Steps

Complete recessed-gate dataset analysis; derive an empirical relationship between threshold voltage and recess depth; fabricate final optimised devices.

5.2 Logic Demonstration Phase

Plan a DCFL inverter (and optional NAND) using measured device parameters. Outline simulation with extracted models, wire-bonding, and testing.

5.3 Time Plan

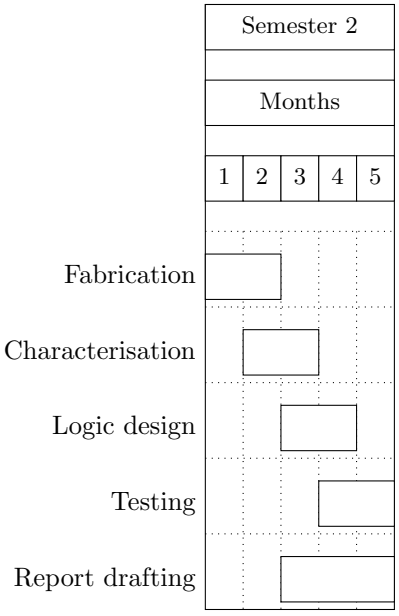

Figure 5.1: Indicative Semester 2 plan; adjust dates and scope as milestones firm up.

A high-level plan is shown in Figure 5.1.

Bibliography

[1] A. Hsieh and Others, “Enhancement-mode algaas/gaas phemts via double-recess structure,” *Journal of Electronic Materials*, 2004. Placeholder entry—update with full bibliographic details.

[2] B. Chu and Others, “Positive-threshold phemts using platinum gate sinking,” *IEEE Transactions on Electron Devices*, 2007. Placeholder entry—update with full bibliographic details.

APPENDIX A

Additional Figures

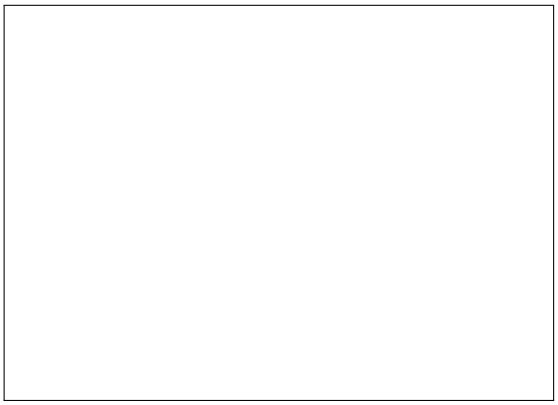

Figure A.1: Supplementary plot. Replace with final figure.

APPENDIX B

Code and Process Flow

B.1 Python Analysis Outline

Brief outline of the analysis pipeline and key scripts. Include code snippets or links to the repository as appropriate.

B.2 Cleanroom Process Summary

Summarise lithography, metallisation, and etch steps with key parameters.