

University of Leeds  
School of Electronic and Electrical Engineering

## **ELEC5870M Interim Report**

### **Fabrication of Enhancement Mode HEMT Devices via Gate Recession**

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# Abstract

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## Acknowledgements

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## Abbreviations

2DEG Two-dimensional electron gas

HEMT High-electron-mobility transistor

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# CHAPTER 1

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## Introduction

Modern communication, sensing, and microwave systems impose increasingly demanding requirements on the semiconductor devices that form their front-end signal paths. Higher operating frequencies, tighter noise constraints and strict linearity targets continue to push transistor technologies beyond the capabilities of many silicon-based platforms. Although silicon processes have made notable progress in recent years, they do not always provide the carrier mobility, noise performance or high-frequency gain required in performance-critical microwave and millimetre-wave applications.

III–V High-Electron-Mobility Transistors (HEMTs) play a central role in addressing these challenges. Their heterostructure-based design creates a highly conductive channel at the interface between two semiconductor layers with different bandgaps. At this interface a two-dimensional electron gas (2DEG) forms, supporting exceptionally high carrier mobility. The resulting strong transconductance, stable high-frequency behaviour and low-noise performance have firmly established HEMTs as core devices throughout microwave and millimetre-wave circuit design.

Research activity within the field has increasingly shifted toward gallium nitride (GaN) HEMTs, driven by the material properties enabled by its wide bandgap. GaN supports high breakdown voltages, strong power-handling capability and robust operation under large electric fields, making it the preferred choice for many high-power and high-linearity applications [cite needed]. Despite this growing dominance, gallium arsenide (GaAs) HEMTs remain one of the most mature and well characterised III–V transistor platforms. Their stability, extensive documentation and long industrial history continue to make them an invaluable system for studying the relationships between heterostructure design, device architecture and electrical behaviour.

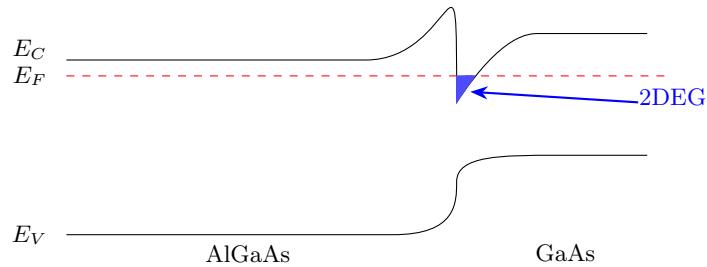
For the purposes of this project, GaAs presents clear practical and technical advantages. The Leeds Nanotechnology Cleanroom maintains established, reliable processes for GaAs/AlGaAs heterostructures, and suitable wafers are readily available with reproducible epitaxial quality [1]. This provides a controlled environment in which HEMT structures can be fabricated and analysed systematically. The work undertaken here aims to investigate how variations in device structure influence key electrical characteristics, including threshold voltage, transconductance, leakage behaviour and the overall conduction profile of the device. The intention is to determine how specific structural changes translate into measurable shifts in device performance, building a clear link between fabrication choices and the resulting electrical behaviour.

# CHAPTER 2

## Technical Background

### 2.1 Overview of GaAs/AlGaAs HEMTs

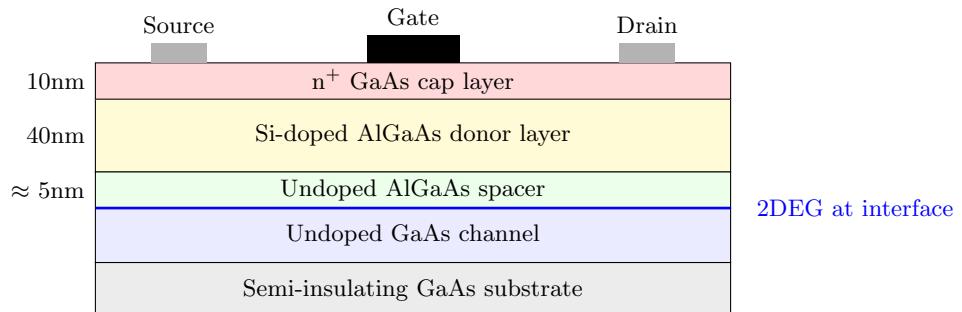
In the GaAs/AlGaAs HEMTs used in this project, the interface between the GaAs channel layer and the overlying AlGaAs barrier produces a discontinuity in the conduction band because the two materials have different bandgaps. This offset creates a potential well on the GaAs side of the junction, as demonstrated in 2.1. Electrons supplied by silicon donors in the modulation-doped AlGaAs layer transfer into this well and accumulate to form the 2DEG that serves as the conducting channel. This 2DEG forming at the interface is the defining feature of the HEMT structure [2].



**Figure 2.1:** Band Structure Diagram of the AlGaAs/GaAs interface demonstrating the resulting Two-Dimensional Electron Gas (2DEG) formed in a Potential Well.

### 2.2 The GaAs/AlGaAs Heterostructure

The HEMTs used in this project are based on a conventional GaAs/AlGaAs heterostructure in which a sequence of epitaxial layers is engineered to create and control a two-dimensional electron gas (2DEG). A schematic cross-section of the structure is shown in Figure 2.2, highlighting the cap, donor, spacer and channel layers that together define the electrical behaviour of the device.



**Figure 2.2:** Cross-section of the GaAs/AlGaAs HEMT used in this project (not to scale).

At the top of the structure lies a thin, highly doped GaAs cap layer. This cap provides a stable surface for forming the Schottky gate contact and prevents oxidation of the underlying AlGaAs. Its high conductivity also assists charge access to the regions adjoining the source and drain contacts.

Beneath the cap is the Si-doped AlGaAs donor layer. Silicon donors in AlGaAs supply electrons that preferentially transfer into the GaAs channel due to the conduction-band discontinuity at the heterointerface. This arrangement is known as modulation doping, as the dopants are placed in the barrier rather than in the channel. The donor concentration and its distance from the interface set the available carrier population for the 2DEG.

A thin undoped AlGaAs spacer layer separates the donor layer from the GaAs channel. Although only a few nanometres thick, it plays a crucial role in determining device performance. By physically separating the 2DEG from the ionised silicon donors, the spacer suppresses Coulomb scattering and allows carriers to move through the channel with significantly higher mobility. This benefit becomes particularly pronounced at cryogenic temperatures, where phonon scattering is reduced, and impurity scattering would otherwise dominate. The spacer thickness therefore influences both the electrostatic coupling to the gate and the mobility of carriers within the 2DEG.

The GaAs channel beneath the spacer hosts the 2DEG. Electrons accumulate at the AlGaAs/GaAs interface, where the conduction-band offset creates a quantum-well-like potential that confines carriers to a narrow region within the GaAs. This interfacial channel is responsible for the high-mobility transport behaviour characteristic of GaAs/AlGaAs HEMTs.

Together, these layers define the depth, density and confinement of the 2DEG, providing the structural basis for the electrical behaviour analysed later in this report.

### 2.3 HEMT Operating Principles

The electrical behaviour of the GaAs/AlGaAs HEMTs used in this project is governed by the interaction between the Schottky gate contact and the two-dimensional electron gas (2DEG) formed within the heterostructure. When a metal is deposited on the GaAs surface, a Schottky barrier is formed, giving rise to a depletion region beneath the gate. Applying a gate voltage modulates this depletion region and enables electrostatic control of the 2DEG at the AlGaAs/GaAs interface.

A negative gate voltage widens the depletion region and reduces the electron density within the underlying 2DEG. As the voltage becomes more negative, the carrier concentration continues to fall until the 2DEG is fully depleted; the corresponding gate voltage defines the threshold voltage of the device.

When a drain voltage is applied, electrons flow laterally through the 2DEG from source to drain. At low drain voltages the channel remains uniformly accumulated, resulting in a linear relationship between drain current and drain voltage. As the drain voltage increases, the channel near the drain becomes progressively depleted, leading to pinch-off. Beyond this point the drain

current saturates, with the saturation level determined primarily by the gate voltage.

The sensitivity of the drain current to changes in gate voltage is expressed through the transconductance,  $g_m = \partial I_D / \partial V_G$ . High values of  $g_m$  arise from strong electrostatic coupling between the gate and the 2DEG, together with the high intrinsic mobility of carriers within the channel.

The Schottky gate introduces a finite leakage current, particularly at large negative gate biases where thermionic emission and tunnelling processes become more significant. The magnitude of this leakage depends on the quality of the gate interface, the barrier height and the condition of the semiconductor surface.

Together, these electrostatic and transport processes describe how a GaAs/AlGaAs HEMT functions as a field-effect transistor and provide the basis for the electrical characterisation presented later in this report.

# CHAPTER 3

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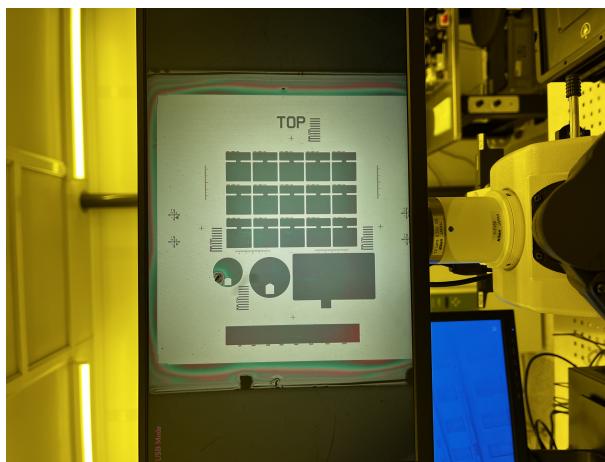
## Fabrication of Depletion-Mode HEMT Devices

### 3.1 Overview of the Fabrication Workflow

The depletion-mode HEMTs characterised in this report were fabricated using the standard III-V device process established within the Leeds Nanotechnology Cleanroom. The workflow follows the routine sequence used for GaAs/AlGaAs transistors in this facility, comprising mesa definition, ohmic contact formation, contact annealing and Schottky-gate metallisation. This well-established procedure was followed without modification and carried out over four full-day laboratory sessions. The devices produced through this workflow provide a reliable baseline against which the behaviour of devices with different structures and dimensions can be compared.

### 3.2 Mesa Definition and Isolation Etch

The fabrication process began with the electrical isolation of individual device regions through mesa etching. Prior to lithography, the GaAs wafer was cleaned sequentially in acetone, iso-propanol (IPA) and deionised water (DI) to remove organic residues and ensure good photoresist adhesion. A positive photoresist (S1803) was then spun onto the sample at 3000rpm, soft-baked at approximately 115°C, and then patterned with exposure from the Heidelberg MLA 150 - Maskless Aligner (MLA).



**Figure 3.1:** Mesa lithography mask used for defining isolated device regions. (Post-Development)

Following development, the mesa pattern was transferred into the wafer using a sulphuric acid, hydrogen peroxide and water wet-etch solution (160:8:1 ratio). This etchant is well suited to GaAs/AlGaAs mesa formation because it produces a controllable, moderately fast isotropic etch (typically a few nanometres per second) that removes the active layers uniformly. Its rate

is slow enough to time accurately for a shallow  $\approx 200\text{ nm}$  recess, yet fast enough to be practical for routine device isolation.

To calibrate the process, a 30 s pilot etch was performed, and the depth measured using the Alpha-Step profilometer, giving an initial etch rate of approximately  $3.8\text{ nm s}^{-1}$ . Using this value, the main mesa etch was timed to reach the target recess. During the second etch, the measured rate decreased to around  $2.9\text{ nm s}^{-1}$ , most likely due to cooling of the etchant after mixing. Since the reaction rate of this chemistry is temperature dependent, a lower solution temperature reduces its reactivity and therefore slows the etch.

This variation highlighted the sensitivity of the process to temperature and timing. For future wet-etching, the etchant temperature will be monitored before and during etching, and the solution will be used promptly after mixing to ensure consistent reactivity.

### 3.3 Ohmic Contact Formation

When a metal is deposited directly onto the GaAs cap, the interface would naturally form a Schottky barrier, which behaves like a diode and restricts carrier injection into the channel. Ohmic contacts are used to avoid this; during annealing the AuGe layer alloys with the GaAs and creates a heavily doped region beneath the metal, thinning the barrier sufficiently for current to enter the 2DEG with low resistance.

To pattern these contacts cleanly, a dual-layer resist stack of LOR beneath S1803 was used. A single resist layer develops near-vertical sidewalls, causing the evaporated metal to form a continuous film across both the wafer surface and the resist edges. This continuity makes lift-off unreliable and often leaves metallic flakes or fences around the contact perimeter.

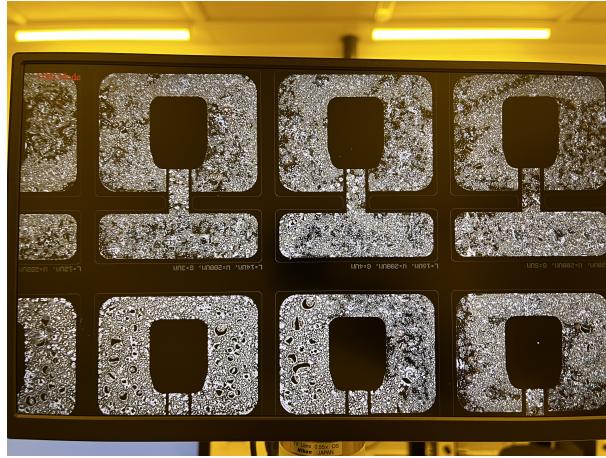
The dual-layer stack overcomes this by exploiting the higher developer solubility of LOR. During development, the LOR recedes laterally more than the S1803 above it, producing the undercut profile shown in Figure 3.2. This undercut breaks the continuity of the deposited metal so the film on top of the resist is physically separated from the metal inside the opening. When the LOR dissolves during lift-off, the unwanted metal lifts away cleanly, leaving sharply defined contact openings ready for metallisation.



**Figure 3.2:** Dual-layer LOR/S1803 resist stack after development showing the wider LOR opening that creates an undercut for clean metal lift-off.

A AuGe/Ni/Au metallisation stack was then deposited by thermal evaporation to form the ohmic contacts. During the subsequent anneal the AuGe alloys with the GaAs to create the heavily doped contact region required for a linear, low-resistance interface. After deposition, solvent-based lift-off removed the excess metal, leaving well defined pads with smooth edges and

good adhesion, as shown in Figure 3.3.



**Figure 3.3:** Ohmic contacts after lift-off.

### 3.4 Contact Annealing and Gate Patterning

The sample was annealed to activate the AuGe/Ni/Au contacts and form a low-resistance alloyed interface with the GaAs surface. The annealing process promotes the diffusion of germanium into the GaAs, increasing the local doping concentration and thereby reducing the contact resistance.

With the ohmic contacts established, a second lithography step was performed to define the gate electrode. As before, a dual-layer resist stack was used to ensure reliable lift-off. The gate was aligned centrally between the source and drain to modulate the 2DEG formed at the AlGaAs/GaAs interface. Following development, Ti/Au was evaporated to form the Schottky gate metal stack, with titanium acting as an adhesion layer and gold providing a stable Schottky barrier and low-resistance gate conductor.

### 3.5 Final Lift-Off, Cleaning and Inspection

After gate metallisation, the resist was removed using solvent lift-off to reveal the final device structure. A small number of lift-off defects, primarily isolated metallic particles, were observed under the microscope and removed using brief, gentle ultrasonic cleaning. These artefacts can cause electrical short circuits, particularly around the gate edges, so their removal was essential for device reliability.

The completed devices were inspected using optical microscopy. The mesas exhibited clean sidewalls, ohmic pads were well defined and the gate electrodes showed sharp, uninterrupted edges with no bridging or residual flakes. The overall process yielded a high-quality array of depletion-mode HEMTs suitable for electrical testing.

### 3.6 Initial Electrical Verification

Electrical characterisation was performed using the Keysight Semiconductor Device Parameter Analyser. For each device, output characteristics ( $I_D - V_D$ ), transfer characteristics ( $I_D - V_G$ ) and

gate-leakage ( $I_G$ - $V_G$ ) curves were recorded. Channel resistance was extracted from the low-bias linear region of the output characteristics.

Of the 15 planar transistors in the array, 14 exhibited strong depletion-mode behaviour with clear pinch-off, monotonic current increase with less negative gate voltage and well-defined threshold voltages. This confirmed that the ohmic contacts, gate metallisation and mesa isolation were all functioning as intended. Two of the four Corbino-type devices did not operate correctly; inspection suggested that this was due to short circuits caused by small metallic residues remaining after gate lift-off. Their failure highlighted the sensitivity of circular devices to surface debris, underscoring the importance of careful cleaning following metallisation.

# CHAPTER 4

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# CHAPTER 7

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7.2 Planned Technical Deliverables

7.3 Risk Mitigation Strategy

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- [1] The University of Leeds, “Leeds nanotechnology cleanroom process gallery.” Available at: <https://cleanroom.leeds.ac.uk/>.
- [2] W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HEMTs*. John Wiley and Sons, 1999.

## APPENDIX A

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### Additional Figures

## APPENDIX B

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### Code and Process Flow