CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: _____ACDC_____

Team Members: _____Colton Hazlett_____

_____Dustin Heims_____

_____Austin Collins_____

Course Goals:

- To run instructions on the MIPS processor.
- Understand the computer architecture about the processor.
- To further my knowledge in hardware design
- To get an A in the course

Team Expectations:

- **Conduct:** General manners and communicate efficiently
- **Communication:** Teams Meetings, GroupMe. GitHub to save our project.
- **Group conventions:** Comment majority of the code and file comment about the file, naming for ports (output → o_Data, input → i_Data, signal → s_iData), organize into steps, and maybe .do file.
- **Meetings:** Group meeting Monday 12-1/2pm and lab Thursday 10am – 12am. Plus any extra meetings that are needed (Saturday). Work together online using teams and individually on assigned responsibilities.
- **Peer Evaluation Criteria:** Responsiveness, time towards project, completed work, and respectfullness.

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part	Estimated Time	Design		Test	
		Lead	Timeline	Lead	Timeline
High-level design	1 hr	Austin	March 7th	Dustin	March 14th
Test programs	4 hr	Dustin	March 26th	Austin	March 28th
Control logic *test bench*	2 hr	Colton	March 5th	Austin	March 14th
Fetch logic *test bench*	3 hr	Austin	March 7th	Colton	March 14th
Barrel shifter *test bench*	2 hr	Dustin	March 7th	Austin	March 14th
ALU integration + Misc updates	2 hr	Colton	March 14th	Dustin	March 18th
High-level integration	4 hr	Colton	March 19th	Dustin	March 23rd
Synthesis (human effort)	1.5 hr	Dustin	March 27th	Colton	March 27th

Run Quartus prime synthesis on personal computer

Integrity of Work: We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature _____Colton Hazlett_____ **Date** ____2/25/2021_____

Student Signature _____Dustin Heims_____ **Date** _____2/25/2021____

Student Signature _____Austin Collins_____ **Date** _____2/25/2021_____