

The World Leader in High Performance Signal Processing Solutions



Understanding & Optimizing Sampled Data Systems





Outline

- What happens when an analog signal enters the Sampled/Quantized/Digital domain
 - Sampling/Quantization/Digitization
 - Domains
 - Continuous vs Discrete Time
 - Time vs Frequency
 - Analog vs Digital
 - Sampling & Quantizing Impacts
 - Noise
 - Aliasing
 - Under & Over-Sampling
 - Distortion
 - ADC's, DAC's & Switched Cap Filters
 - Impacts, Solutions & Application



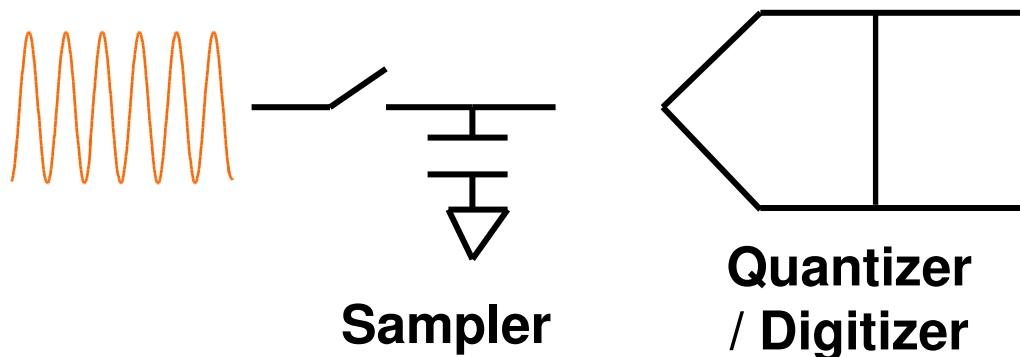
Many Sampled Data Systems

- ◆ **Analog to digital converters**
- ◆ **Digital to analog converters**
- ◆ **Sample and hold amplifiers**
- ◆ **Peak detectors**
- ◆ **Comparators**
- ◆ **Switched cap filters**

- ◆ **Samples a continuous signal**
- ◆ **Domain conversion**
 - **Analog to digital**
 - **Digital to analog**
 - **Continuous time to discrete time**
 - **Continuous frequency to discrete frequency**
- ◆ **Sampling rate**
 - **Continuous, discontinuous**

Sampling, Quantization & Digitization

The Differences have Importance



Sometimes handy to think of the A/D converter in terms of different functional blocks— each with a set of specifications

May Be Combined

- **Sampler** – moves from the continuous to the discrete-time domain
 - Sample & Hold, Peak Detector, Switched Cap Filter
- **Quantizer** – moves from the continuous value to the discrete value domain (non-continuous).
 - Comparator
- **Digitizer** – Moves Continuous or Discrete value to coded digital value
 - SAR Register, Decimation Filter

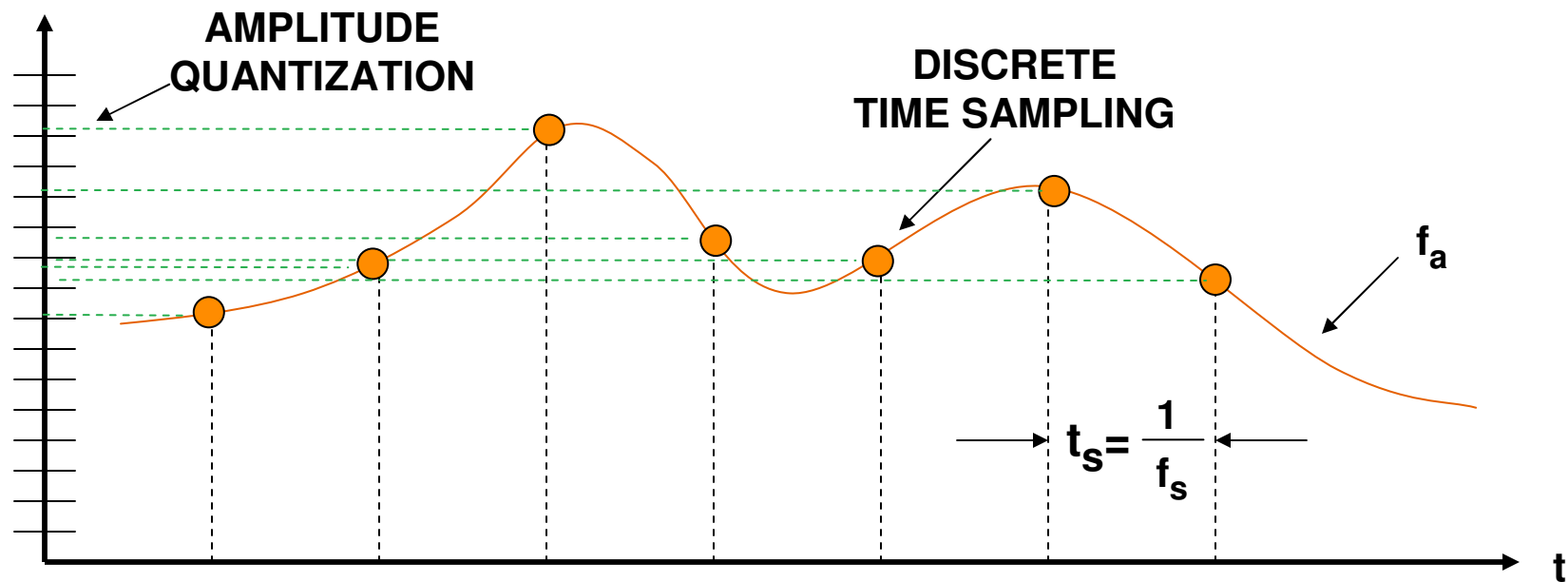
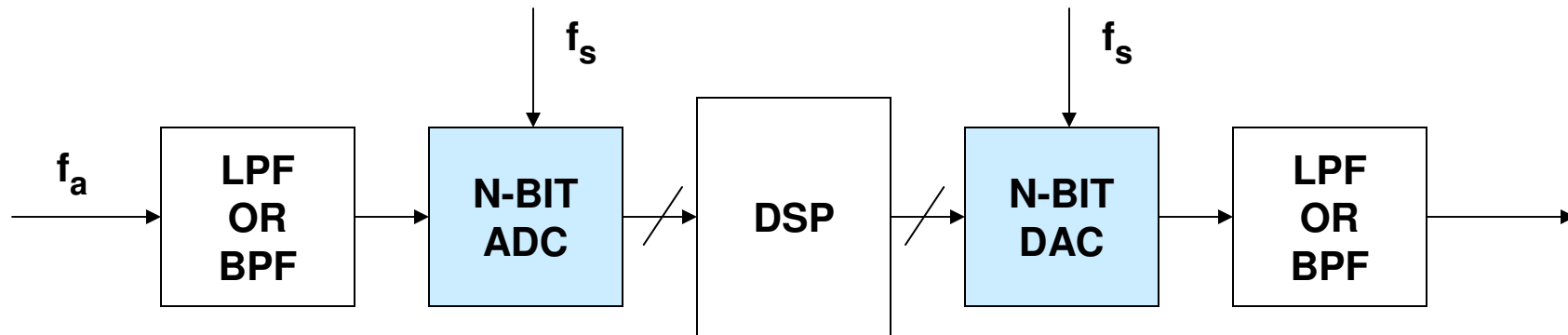


Which Domain are You Operating In?

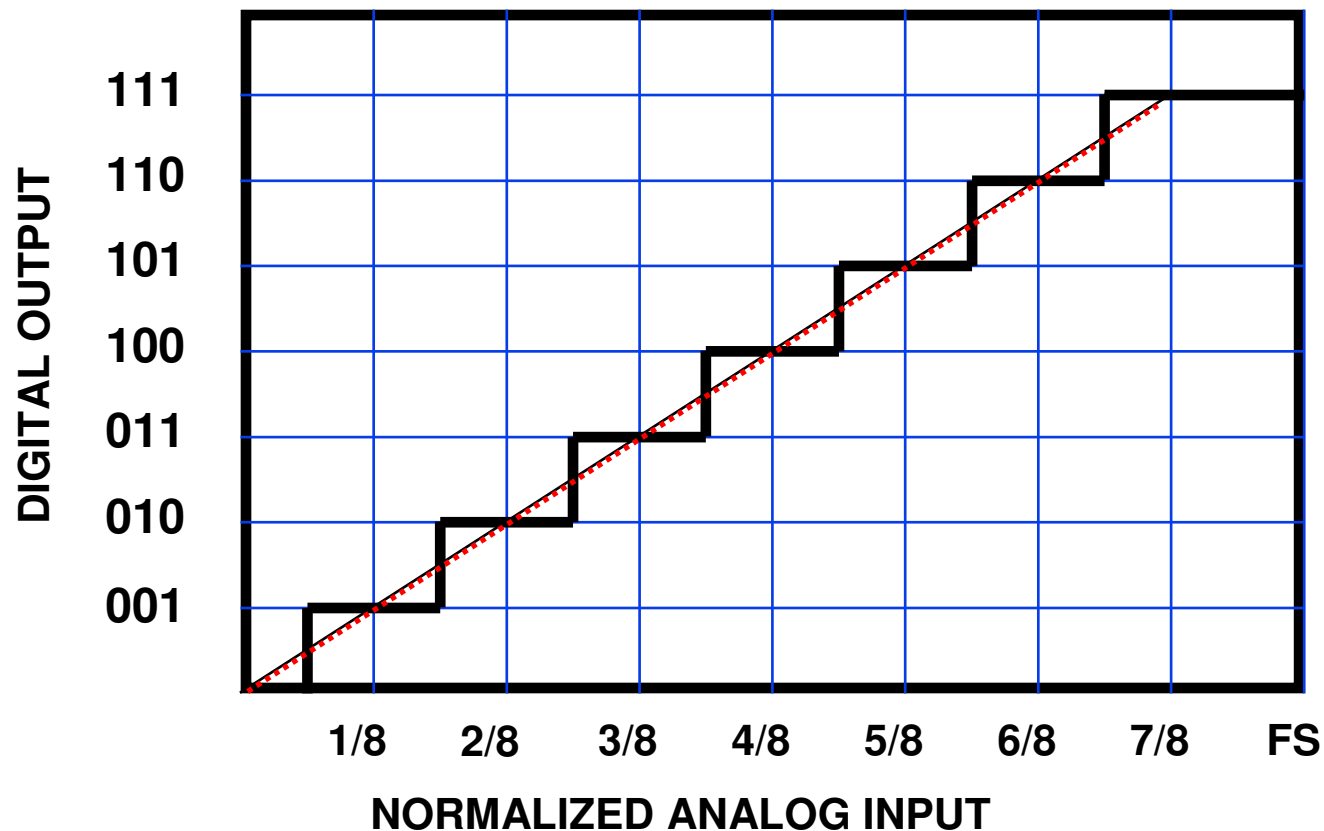
- ◆ Transfer Function: Signal Out vs. Signal In (crossplot)
- ◆ Continuous time domain, analog (oscilloscope)
- ◆ Continuous frequency domain, analog (spectrum analyzer)
 - Amplitude vs. Power
- ◆ Discrete time, analog (switched capacitor, z-domain)
- ◆ Discrete time, digital, time domain (sequence of bytes)
- ◆ Discrete time, digital, frequency domain (FFT output)
- ◆ “Real” signals vs. complex (quadrature) signals

Each domain may have its own set of specifications. We need to be aware of the artifacts associated with transition between these domains--even in the “ideal” world--in addition to “real world” non-idealities.

Sampled Data System: Sampling and Quantization



Quantization & Quantization Noise

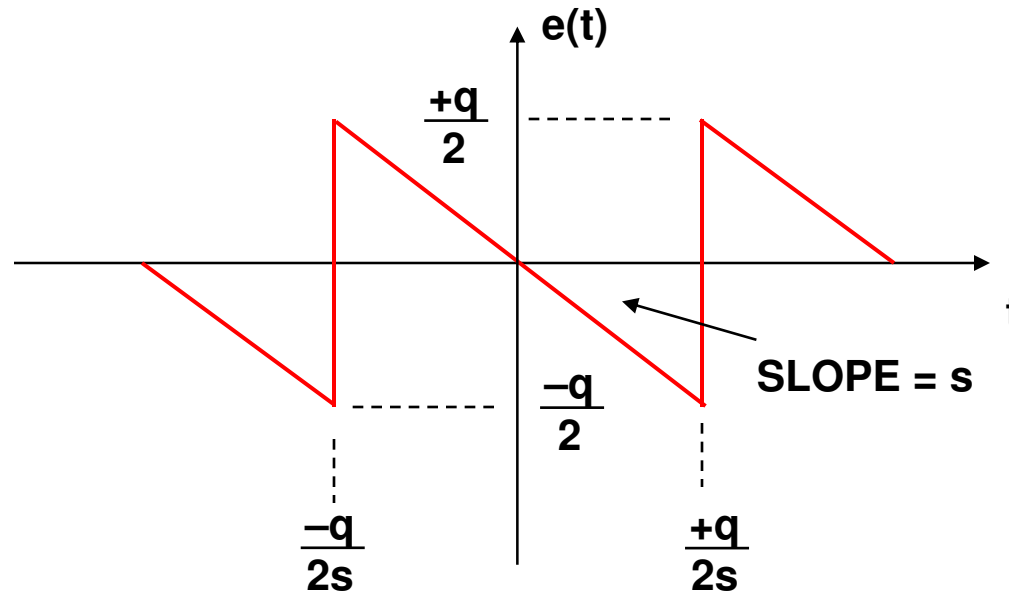


Quantization Error
Function



quantization noise error: RMS value is $\text{LSB}/3.464$

Quantization Noise as a Function of Time

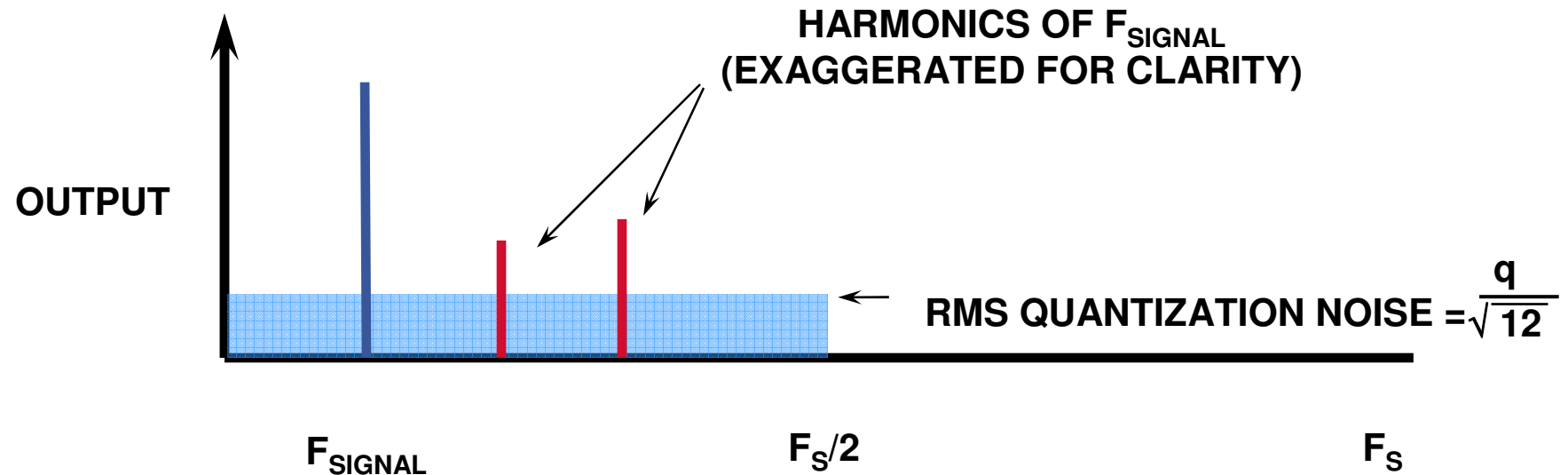


◆ ERROR = $e(t) = st$, $-\frac{q}{2s} < t < \frac{q}{2s}$

◆ MEAN-SQUARE ERROR = $\overline{e^2(t)} = \frac{s}{q} \int_{-q/2s}^{+q/2s} (st)^2 dt = \frac{q^2}{12}$

◆ ROOT-MEAN-SQUARE ERROR = $\sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}}$

Quantization Noise (con't)



If the Quantization Noise Is Uncorrelated With the AC Input Signal,
The Noise Will Be Spread Evenly Over the **Nyquist Bandwidth of $F_s/2$** . (approx. white)
This places a limit to the Dynamic Range of the system.



Theoretical Signal-to-Quantization Noise Ratio of an Ideal N-Bit Converter

◆ FS INPUT = $v(t) = \left[\frac{q 2^N}{2} \right] \sin(2\pi f t)$

◆ RMS Value of FS Sinewave = $\frac{q 2^N}{2\sqrt{2}}$

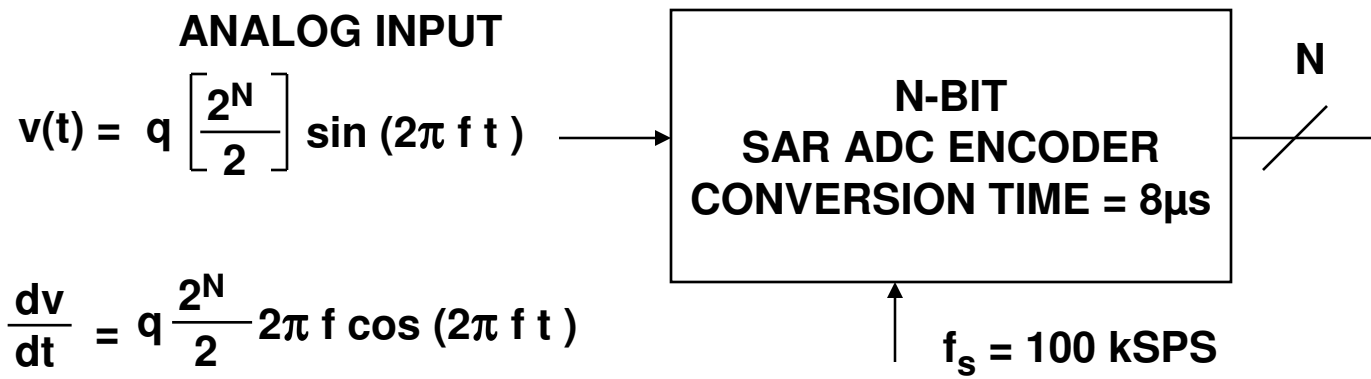
◆ RMS Value of Quantization Noise = $\frac{q}{\sqrt{12}}$

◆ $SNR = 20 \log_{10} \left[\frac{\text{RMS Value of FS Sinewave}}{\text{RMS Value of Quantization Noise}} \right] = 20 \log_{10} 2^N + 20 \log_{10} \sqrt{\frac{3}{2}}$

$$SNR = 6.02N + 1.76\text{dB}$$

(Measured over the Nyquist Bandwidth : DC to $f_s/2$)

Input Frequency Limitations of Non-Sampling ADC (Encoder)



$$\frac{dv}{dt} = q \frac{2^N}{2} 2\pi f \cos(2\pi f t)$$

$$\left. \frac{dv}{dt} \right|_{\max} = q 2^{(N-1)} 2\pi f$$

$$f_{\max} = \frac{\left. \frac{dv}{dt} \right|_{\max}}{2^{(N-1)} 2\pi q}$$

$$f_{\max} = \frac{\left. \frac{dv}{dt} \right|_{\max}}{q\pi 2^N}$$

EXAMPLE:

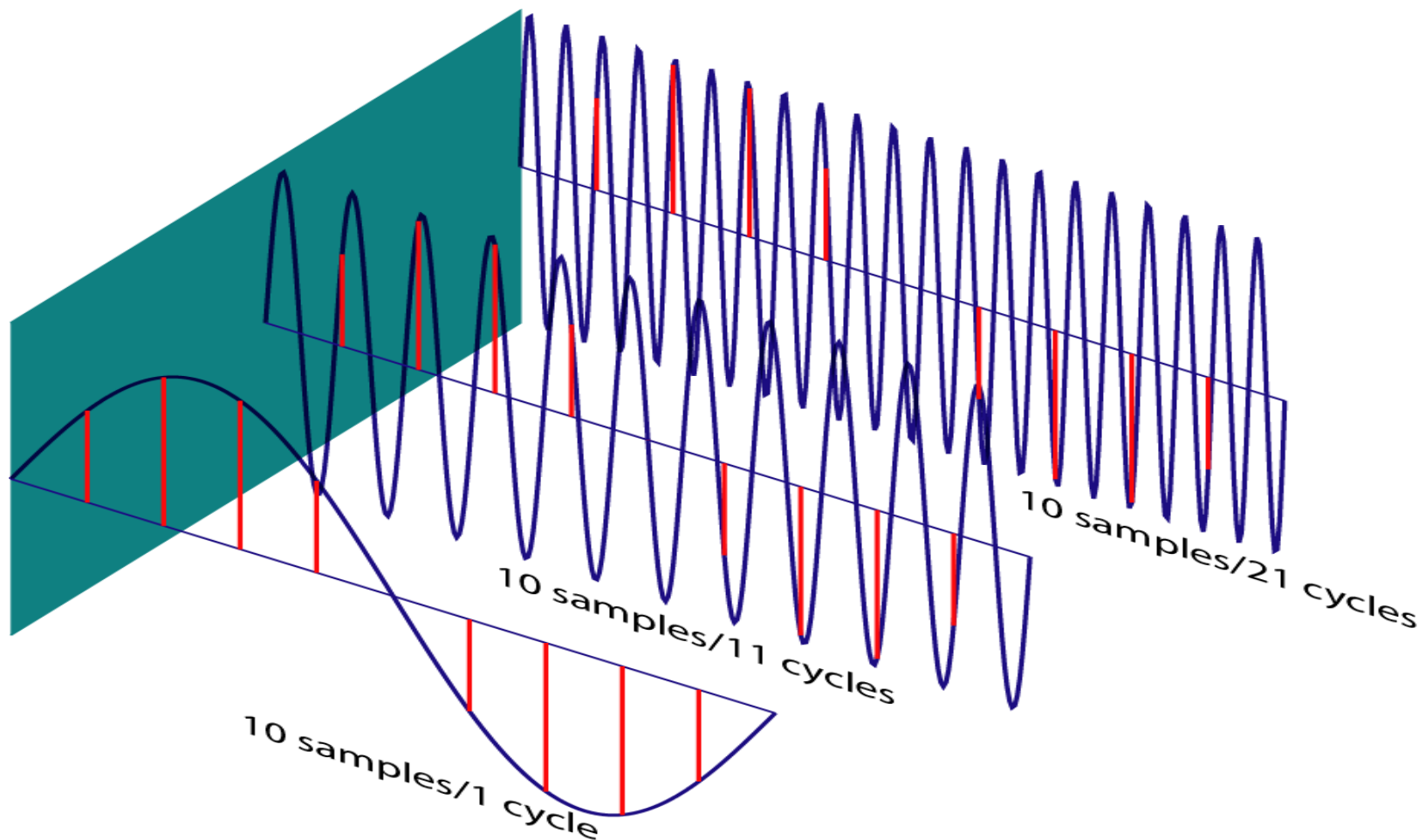
$$dv = 1 \text{ LSB} = q$$

$$dt = 8\mu\text{s}$$

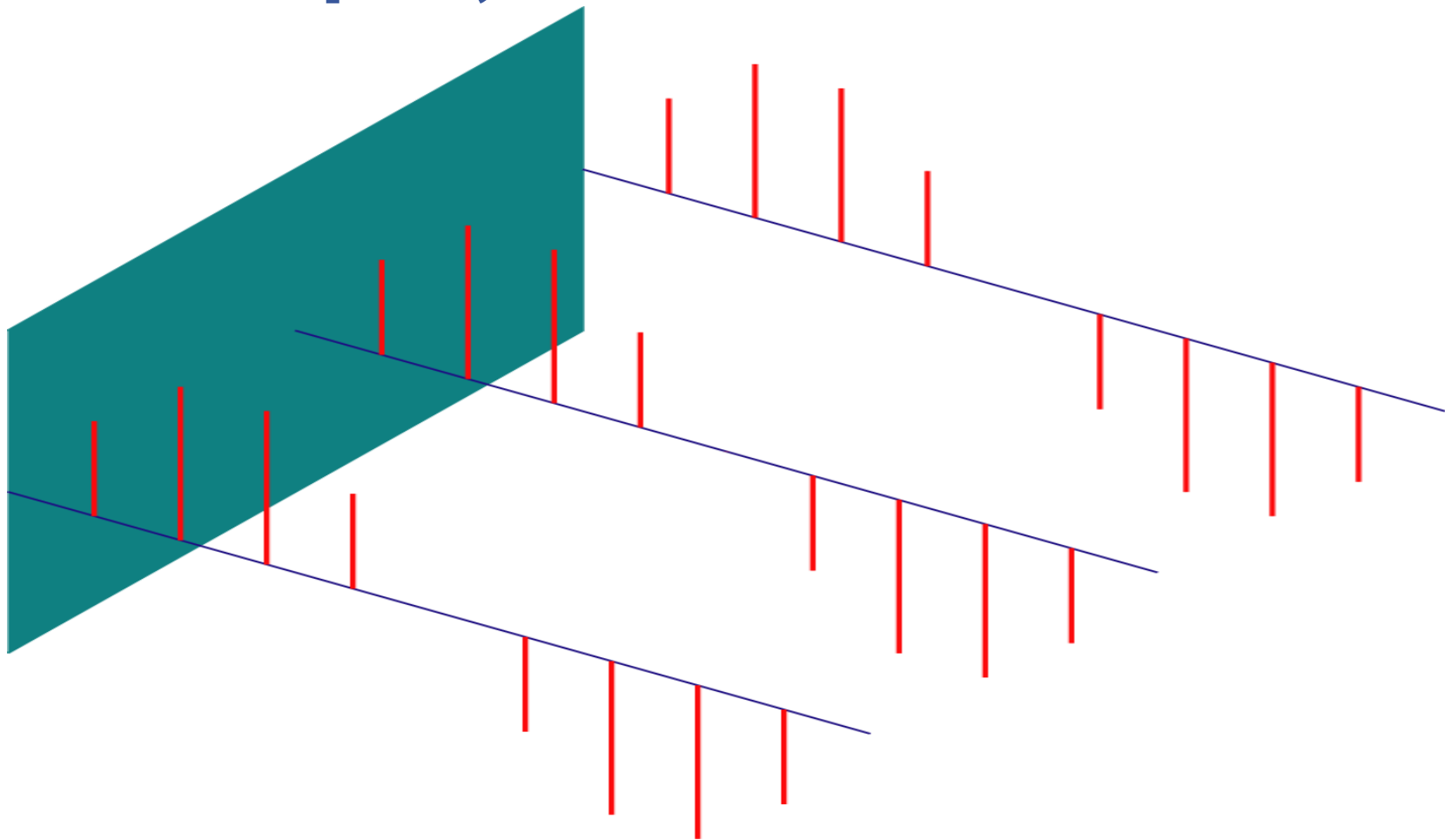
$$N = 12, \quad 2^N = 4096$$

$$f_{\max} = 9.7 \text{ Hz}$$

Ideal ADC Sampling 3 Different Frequencies, Sampled the Same



Ideal ADC Sampling Once Sampled, Information is Lost

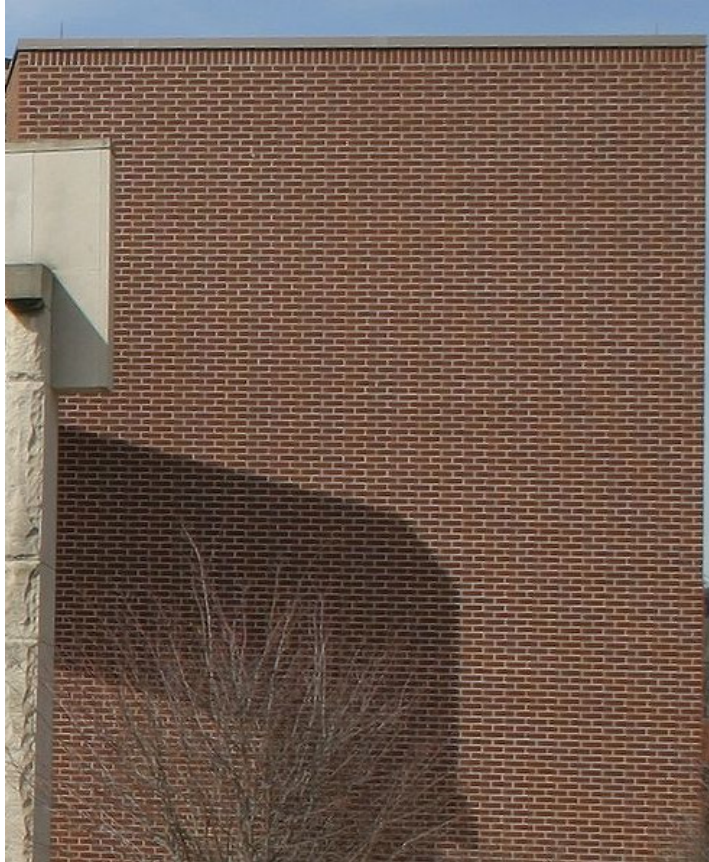




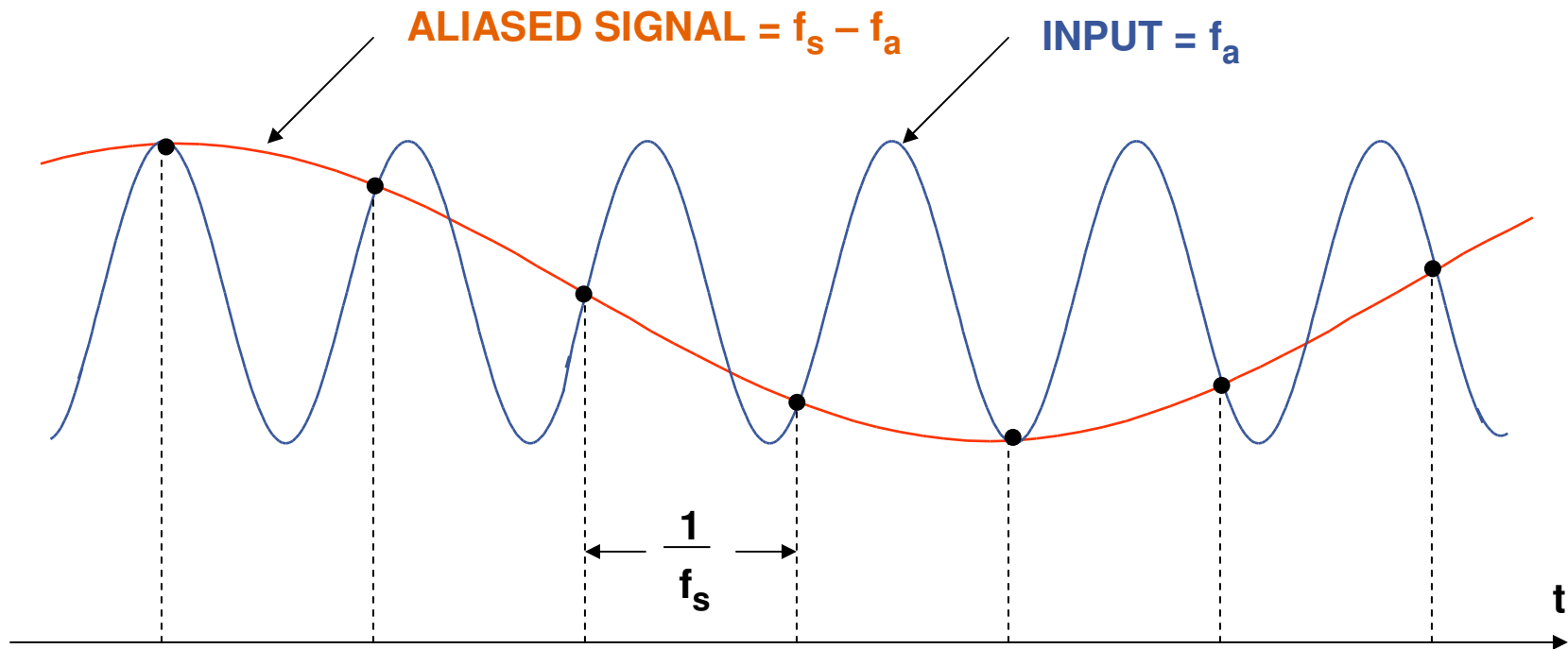
Nyquist's Criteria

- ◆ A signal with a *maximum frequency* f_a must be sampled at a rate $f_s > 2f_a$ or information about the signal will be lost because of aliasing.
- ◆ Aliasing occurs whenever $f_s < 2f_a$
- ◆ A signal which has frequency components between f_a and f_b must be sampled at a rate $f_s > 2(f_b - f_a)$ in order to prevent alias components from overlapping the signal frequencies
- ◆ The concept of aliasing is widely used in communications applications such as direct IF-to-digital conversion.

Aliasing occurs in Many Domains Spatial, Temporal, etc.



Sampling & Aliasing in the Time Domain

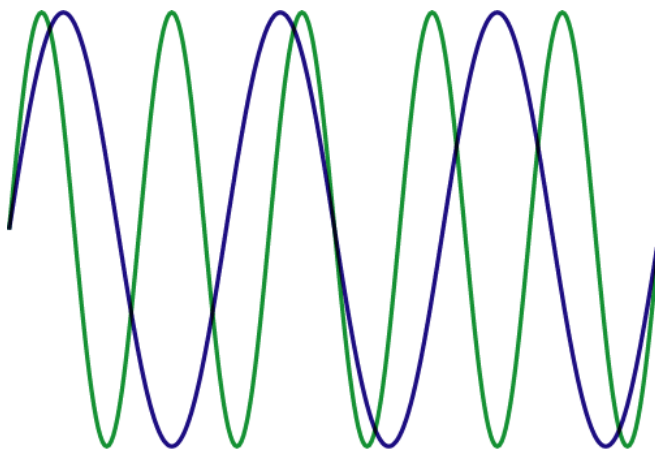


NOTE: f_a IS SLIGHTLY LESS THAN f_s

Very Quick Fourier Reminder

FFT Basics

- Fourier showed us that any periodic signal can be broken down into discrete frequencies.
- The DFT and FFT (Discrete and Fast Fourier Transforms) allow us to separate the sampled signal into the discrete frequencies



$$a(f)_{\text{real}} = \int_0^{\infty} a(t) \cos \omega t$$

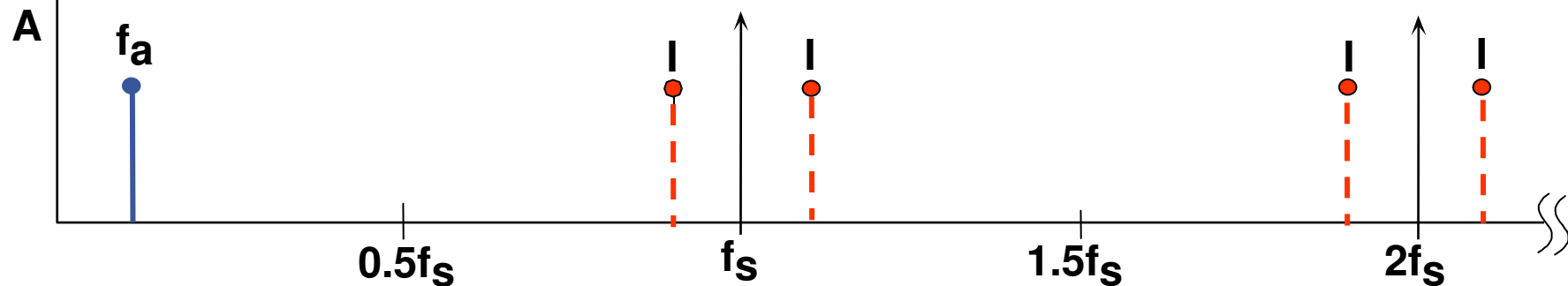
$$a(f)_{\text{imag}} = \int_0^{\infty} a(t) \sin(\omega t)$$

$$a(f)_{\text{mag}} = (a(f)_{\text{real}}^2 + a(f)_{\text{imag}}^2)^{\frac{1}{2}}$$

Sampling & Aliasing in the Frequency Domain

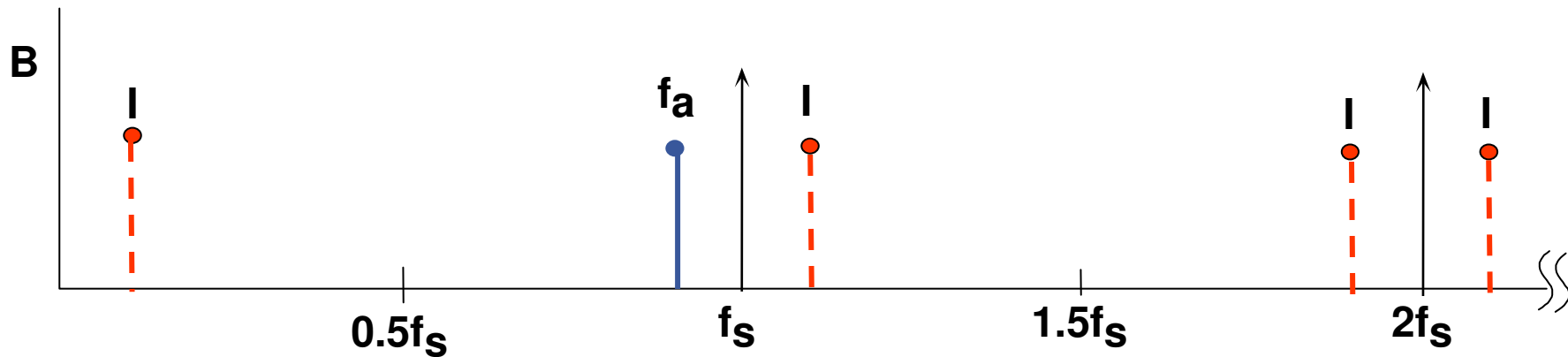
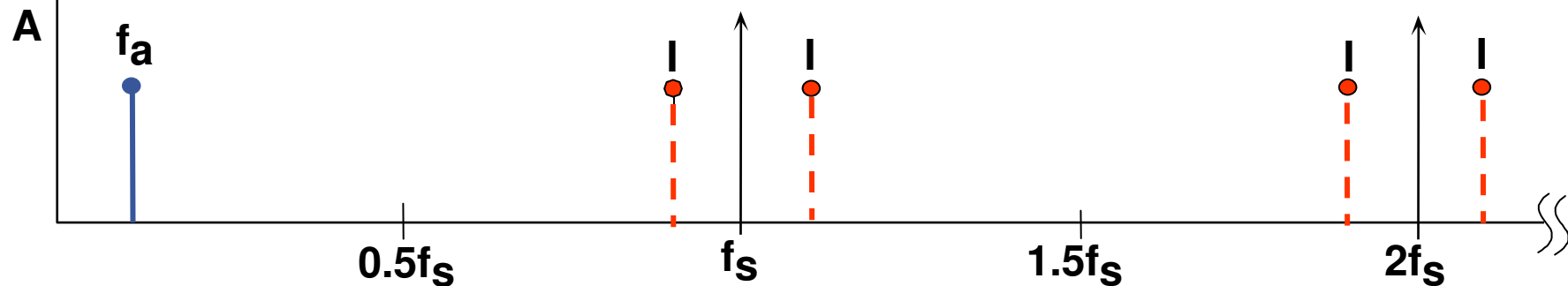
Analog Signal f_a Sampled @ f_s Using Ideal Sampler

Has Images (Aliases) at $|\pm Kf_s \pm f_a|$, $K = 1, 2, 3, \dots$



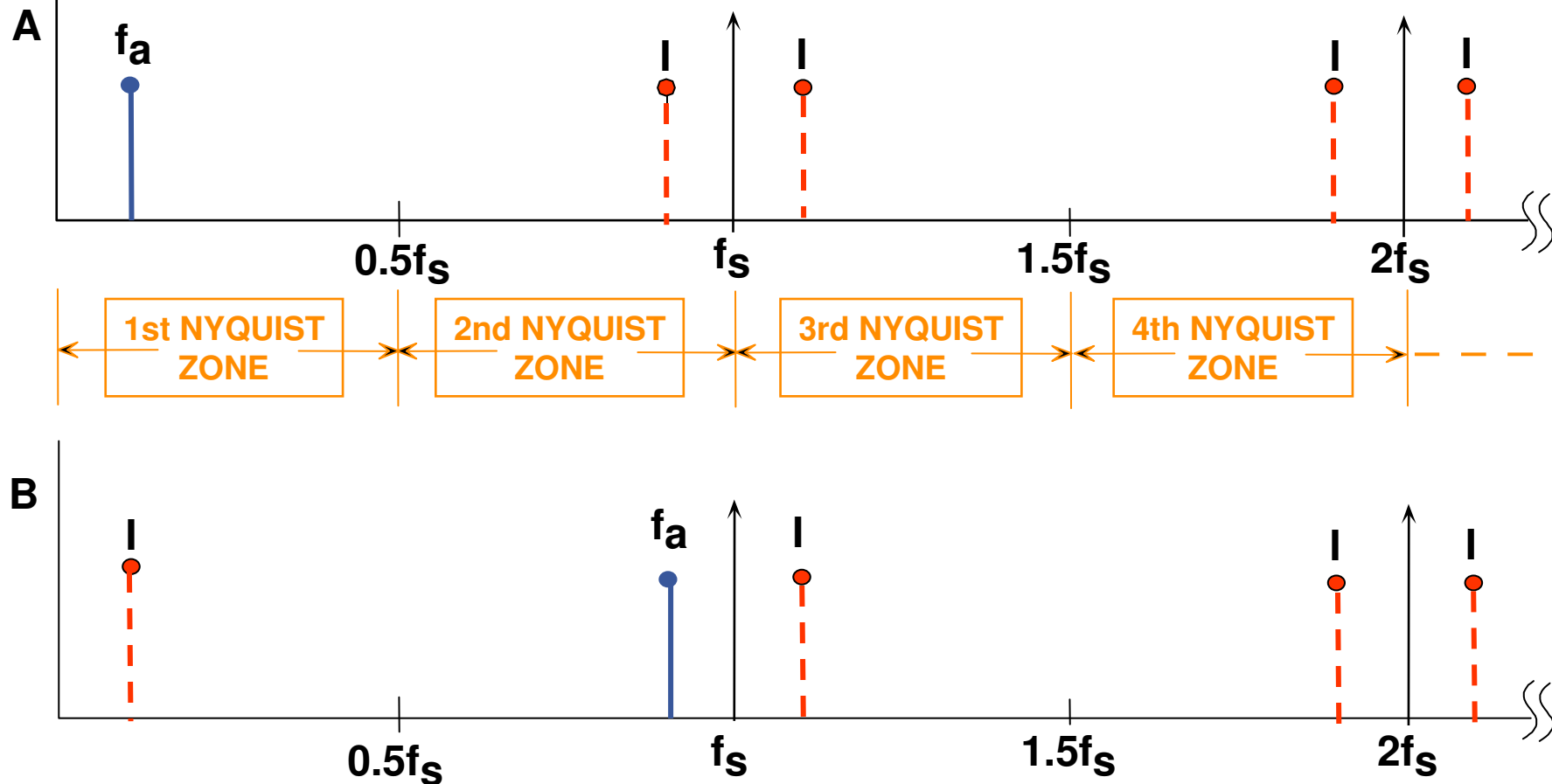
Sampling & Aliasing in the Frequency Domain

Analog Signal f_a Sampled @ f_s Using Ideal Sampler
Has Images (Aliases) at $|\pm Kf_s \pm f_a|$, $K = 1, 2, 3, \dots$



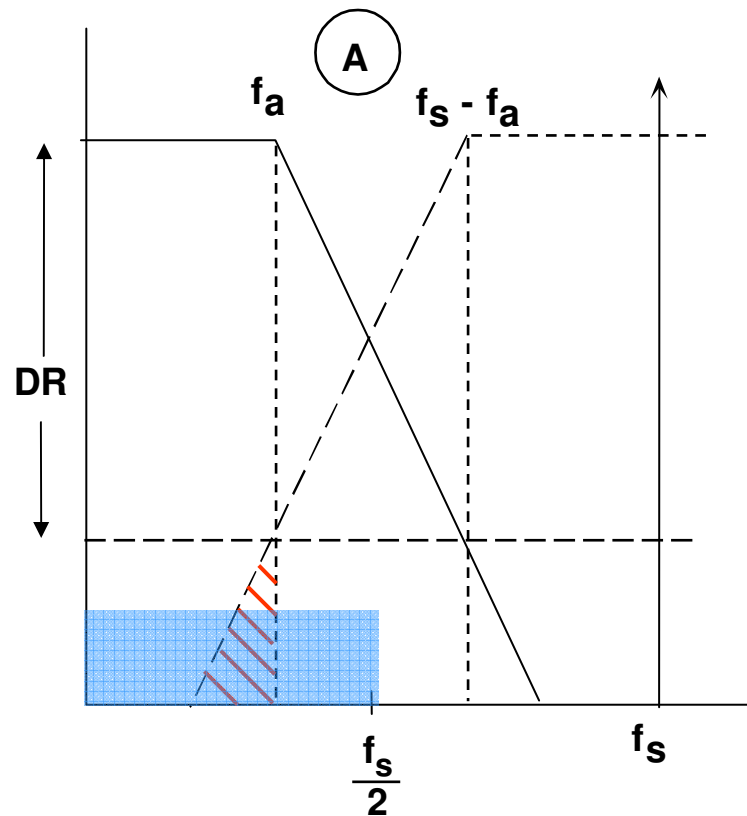
Sampling & Aliasing in the Frequency Domain

Analog Signal f_a Sampled @ f_s Using Ideal Sampler
Has Images (Aliases) at $|\pm Kf_s \pm f_a|$, $K = 1, 2, 3, \dots$



Undersampling: Aliasing is generally a problem, but sometimes is used as a signal processing technique

Baseband Antialiasing Filter Requirements



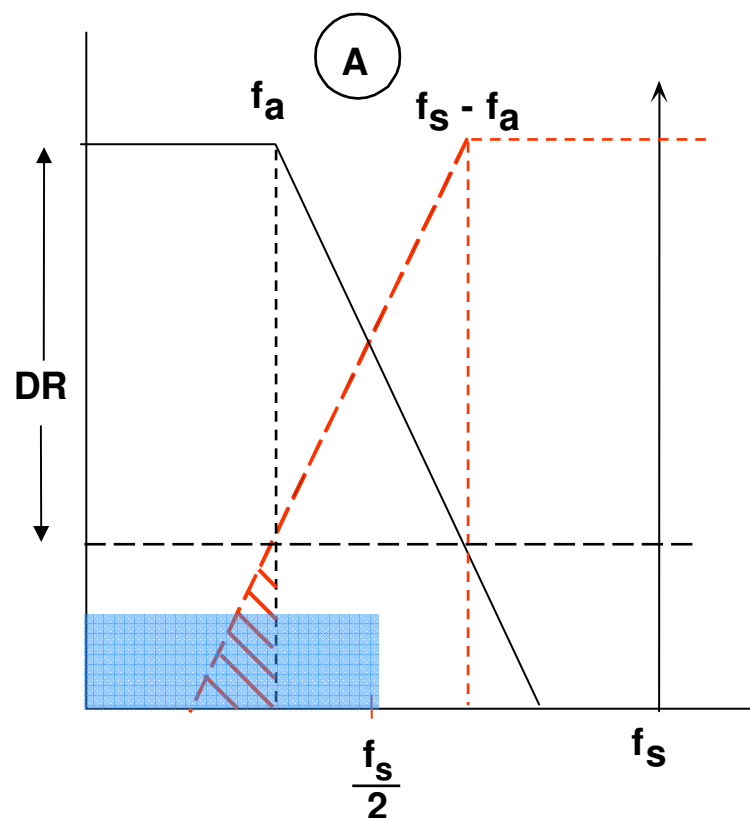
STOPBAND ATTENUATION = DR
 TRANSITION BAND: f_a to $f_s - f_a$
 CORNER FREQUENCY: f_a

**Anti-Alias Filter Prevents Aliasing
 Contributes to Dynamic Range**

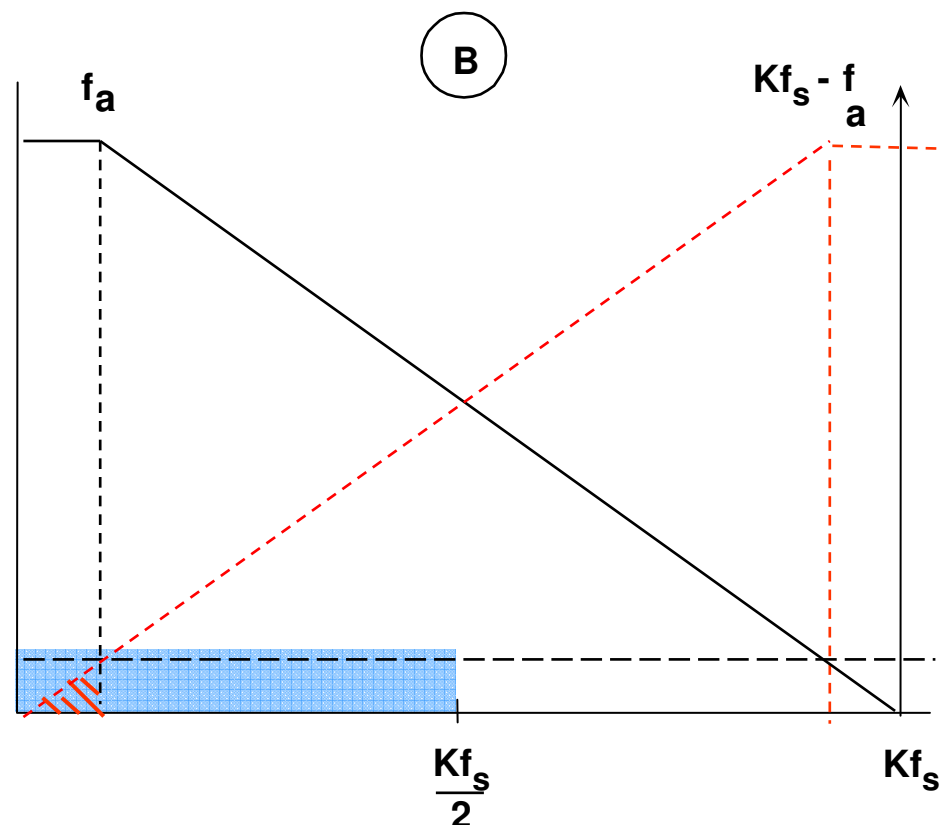
Anti-Alias Filter Objectives

- **Brick Wall (Steep/Deep Rolloff)**
- **Linear Passband**
- **Linear Phase**

Oversampling Relaxes Requirements on Baseband Antialiasing Filter

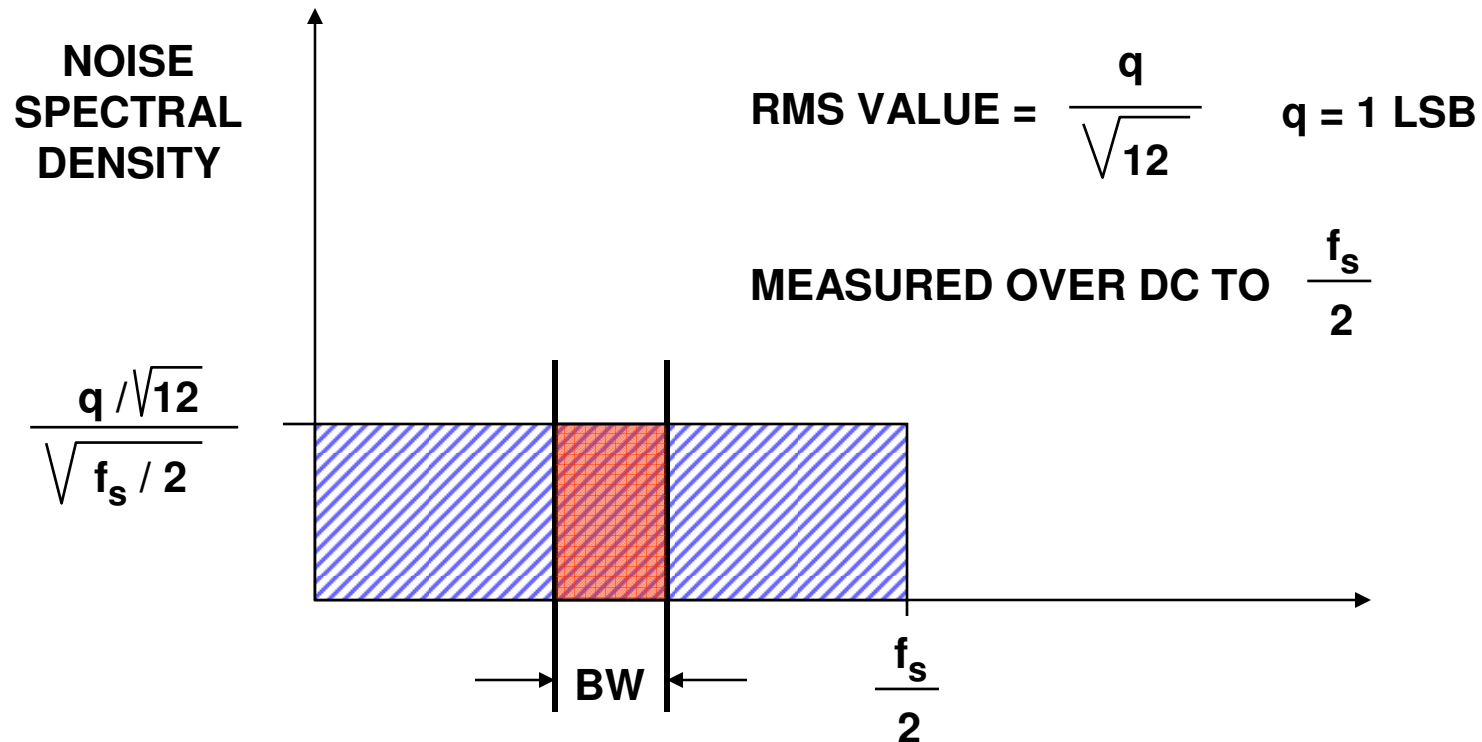


STOPBAND ATTENUATION = DR
 TRANSITION BAND: f_a to $f_s - f_a$
 CORNER FREQUENCY: f_a



STOPBAND ATTENUATION = DR
 TRANSITION BAND: f_a to $Kf_s - f_a$
 CORNER FREQUENCY: f_a

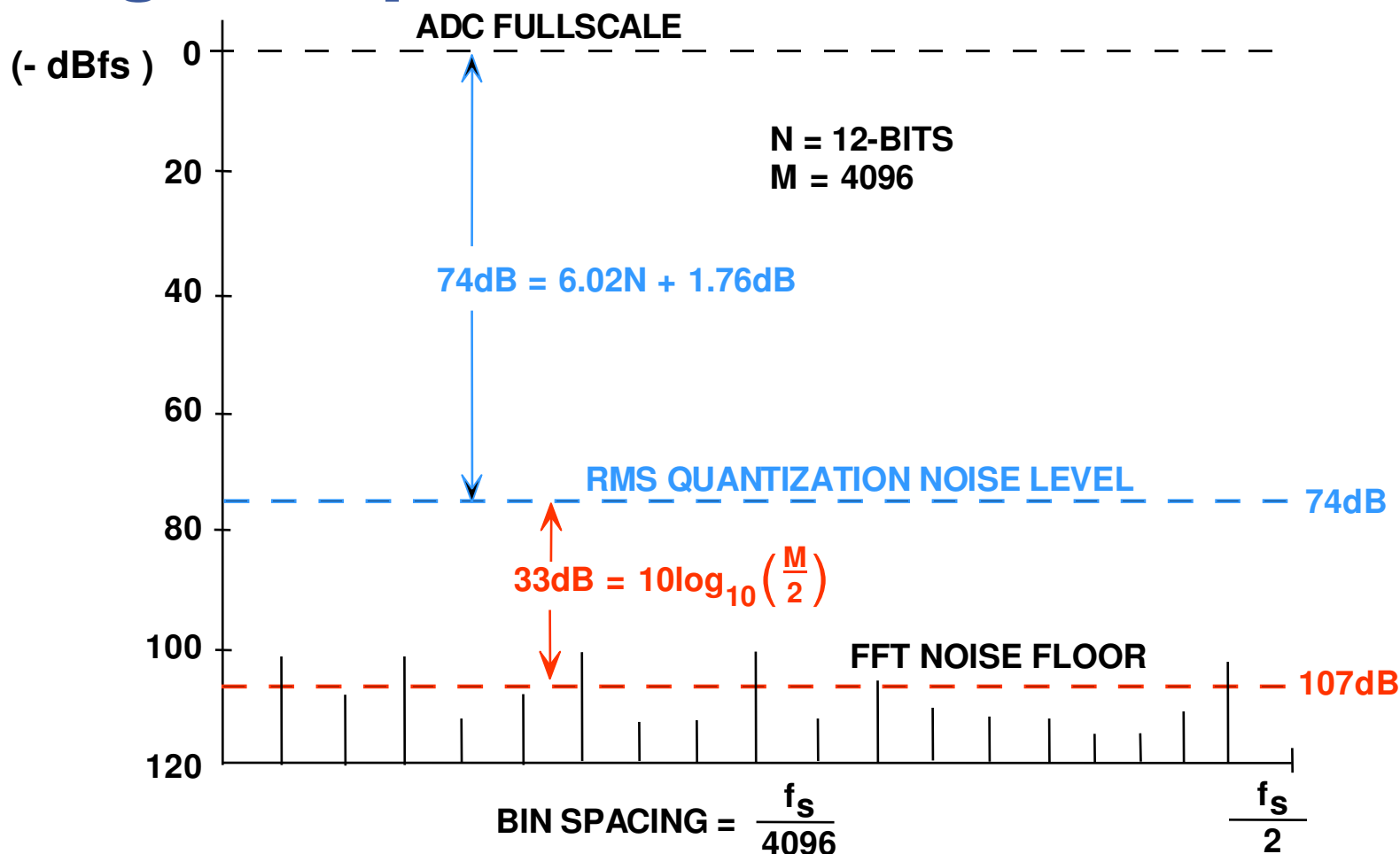
Quantization Noise Spectrum Obtaining Process Gain



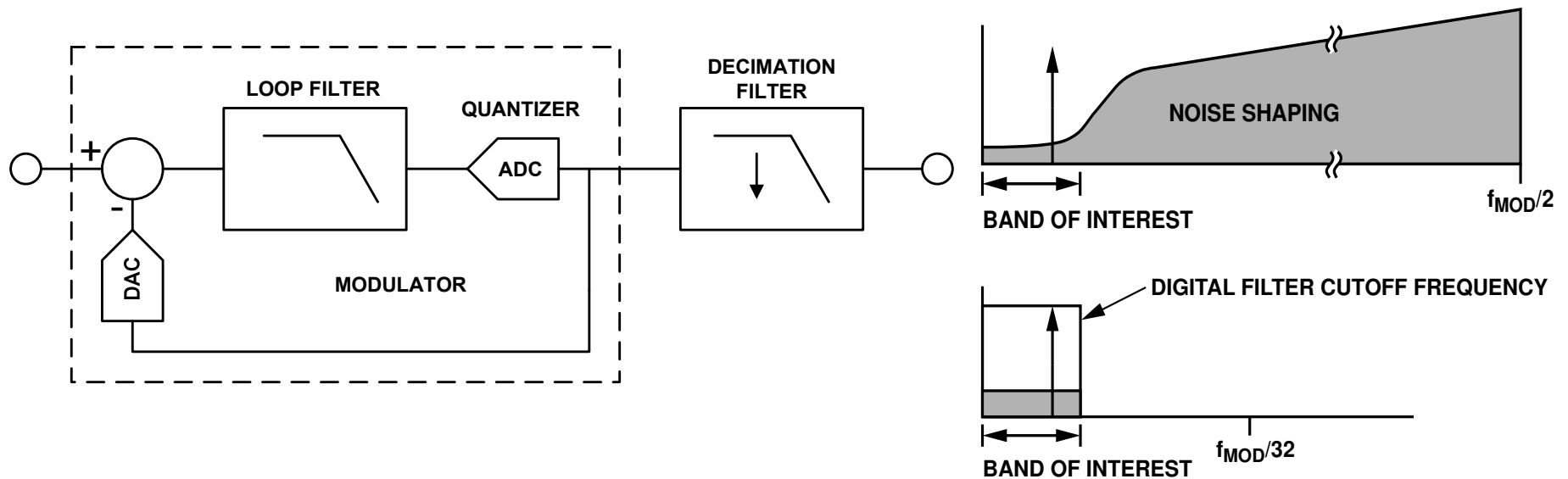
$$\text{SNR} = 6.02N + 1.76\text{dB} + 10\log_{10} \frac{f_s}{2 \cdot \text{BW}} \quad \text{FOR FS SINEWAVE}$$

Process Gain

Noise Floor for an Ideal 12-bit ADC Using 4096-point FFT

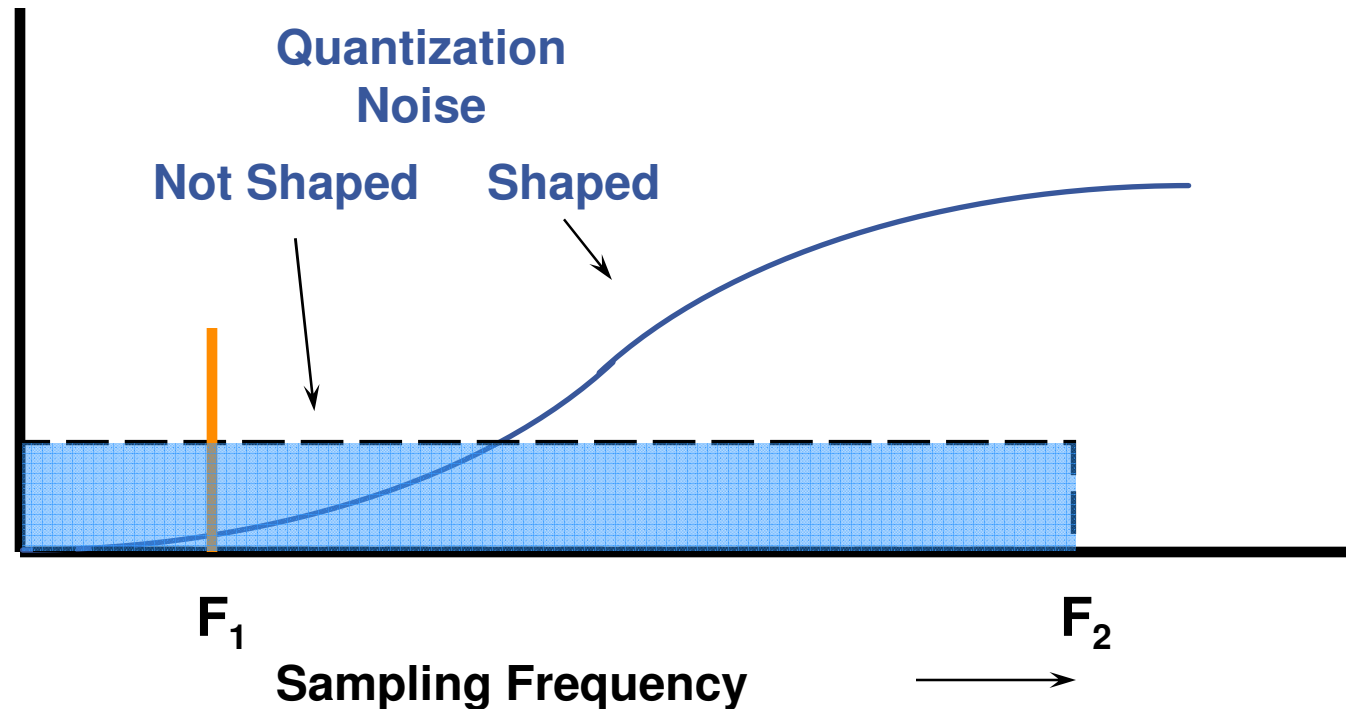


What is a Delta Sigma?



- ◆ Oversampled coarse quantizer feeds back to cancel input (Δ)
 - Quantizer has low quantization noise density in signal band
- ◆ Loop filter shapes Δ error noise out of signal band (Σ)
 - Further reduces in-band quantization noise
- ◆ Decimation filter rejects out of band noise

Noise Shaping: the Key to Sigma-Delta Modulator Processing gains



Noise Shaping Redistributes the Quantization Noise Outside the Passband



Processing Gain & Oversampling

For white noise spectrum:

Processing Gain = $10 \log (\text{Sample rate}/2 * \text{channel BW})$

→ 3dB/ Octave

For “shaped” noise spectrum,
depends on order of modulator:

→ ^{*}/ Octave

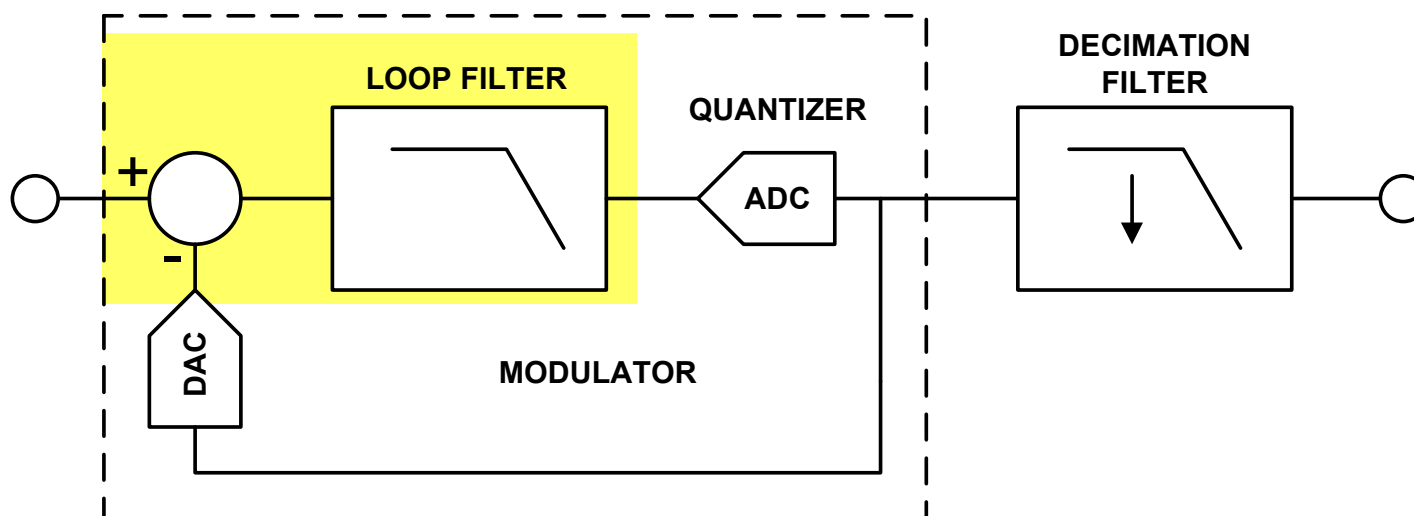
Depends on Order of Modulator:

1st Order: 9dB/ Octave

2nd Order: 15dB/ Octave

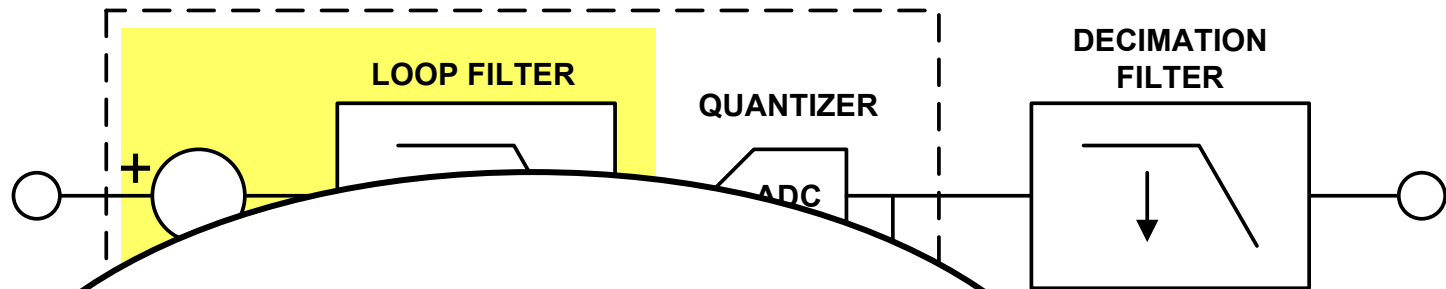
$3*(2*L+1)$ approx. For loop order L

Discrete versus Continuous Time $\Delta\Sigma$



- ◆ Discrete time $\Delta\Sigma$ samples the input directly
 - Sampling takes place @ Input structure – Separate from Quantizer
 - ◆ same as Nyquist rate pipeline ADC, switched cap
 - Loop filter is discrete time, $H(z)$ – switched cap poles and zeros
- ◆ Continuous time $\Delta\Sigma$ samples after the loop filter
 - Input structure is passive and Doesn't sample
 - Loop filter is continuous time, $LF(f) \rightarrow$ “real” poles and zeros, generally need tuning
 - Sampling takes place at Quantizer – Allows for deep rejection of Aliases
- ◆ Either loop filter can be lowpass or bandpass

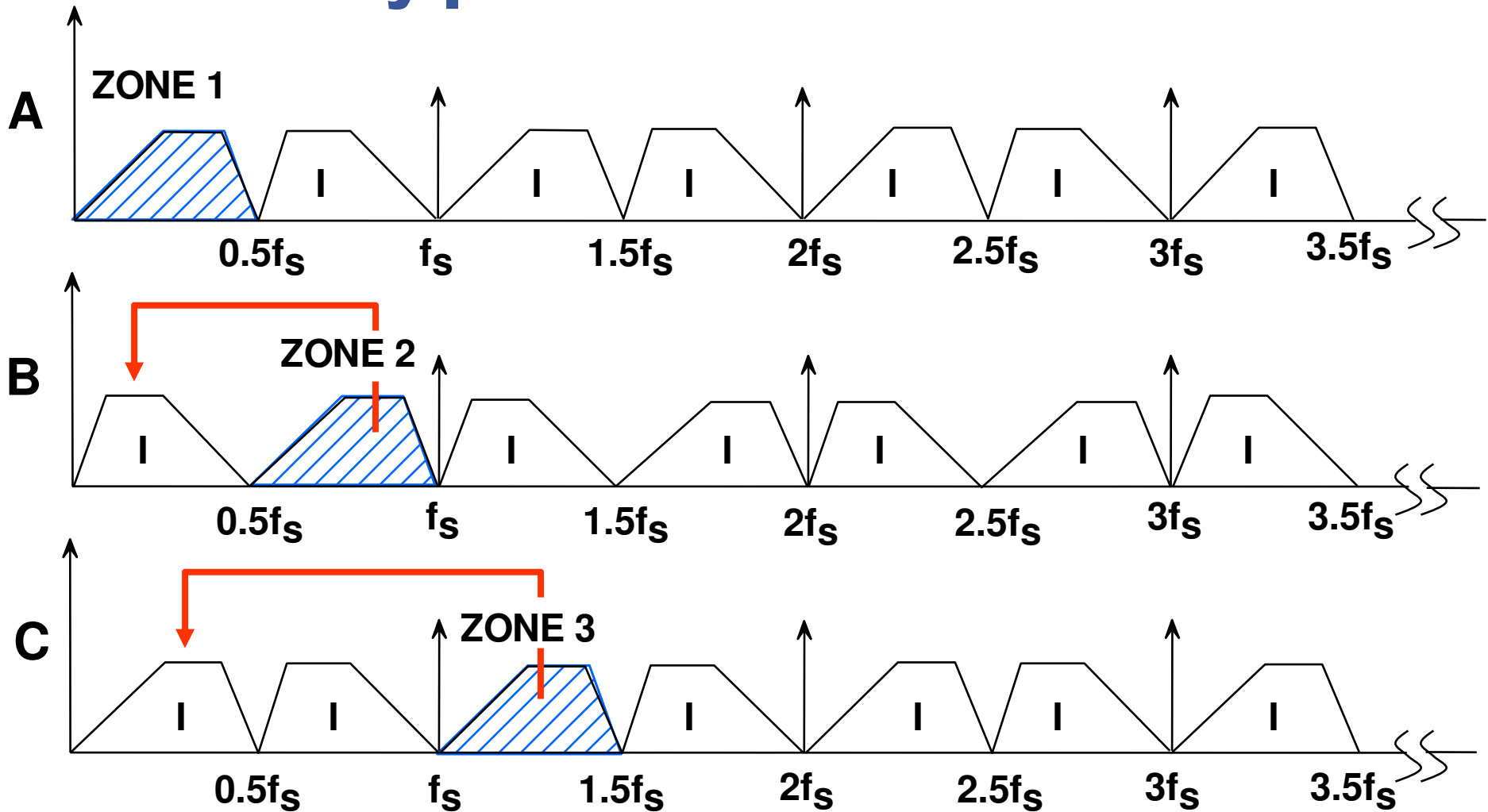
Discrete versus Continuous Time $\Delta\Sigma$



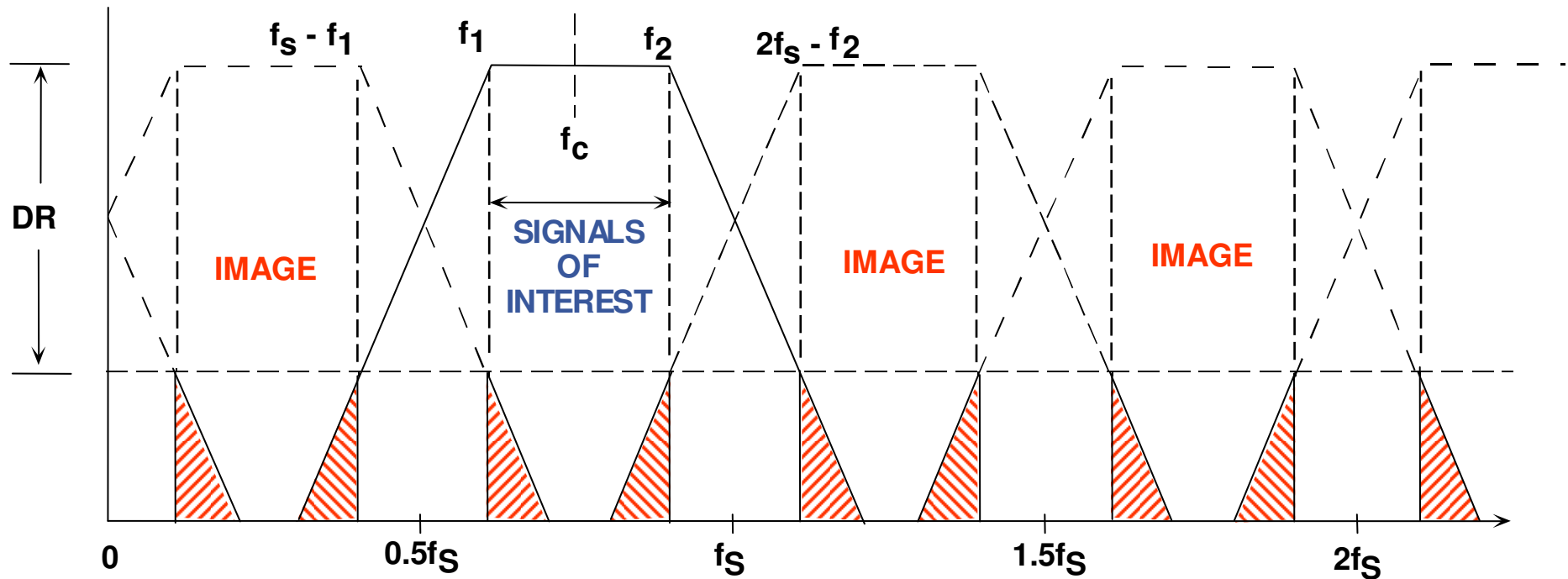
**We'll come back to this
and More in Part 2 . . .**

- ◆ Discrete time
 - Sampling rate
 - ◆ same as Nyquist
 - Loop filter is discrete
- ◆ Continuous time $\Delta\Sigma$ samples after the loop filter
 - Input structure is passive and Doesn't sample
 - Loop filter is continuous time, $LF(f) \rightarrow$ "real" poles and zeros, generally need tuning
 - Sampling takes place at Quantizer – Allows for deep rejection of Aliases
- ◆ Either loop filter can be lowpass or bandpass

Undersampling and Frequency Translation Between Nyquist Zones



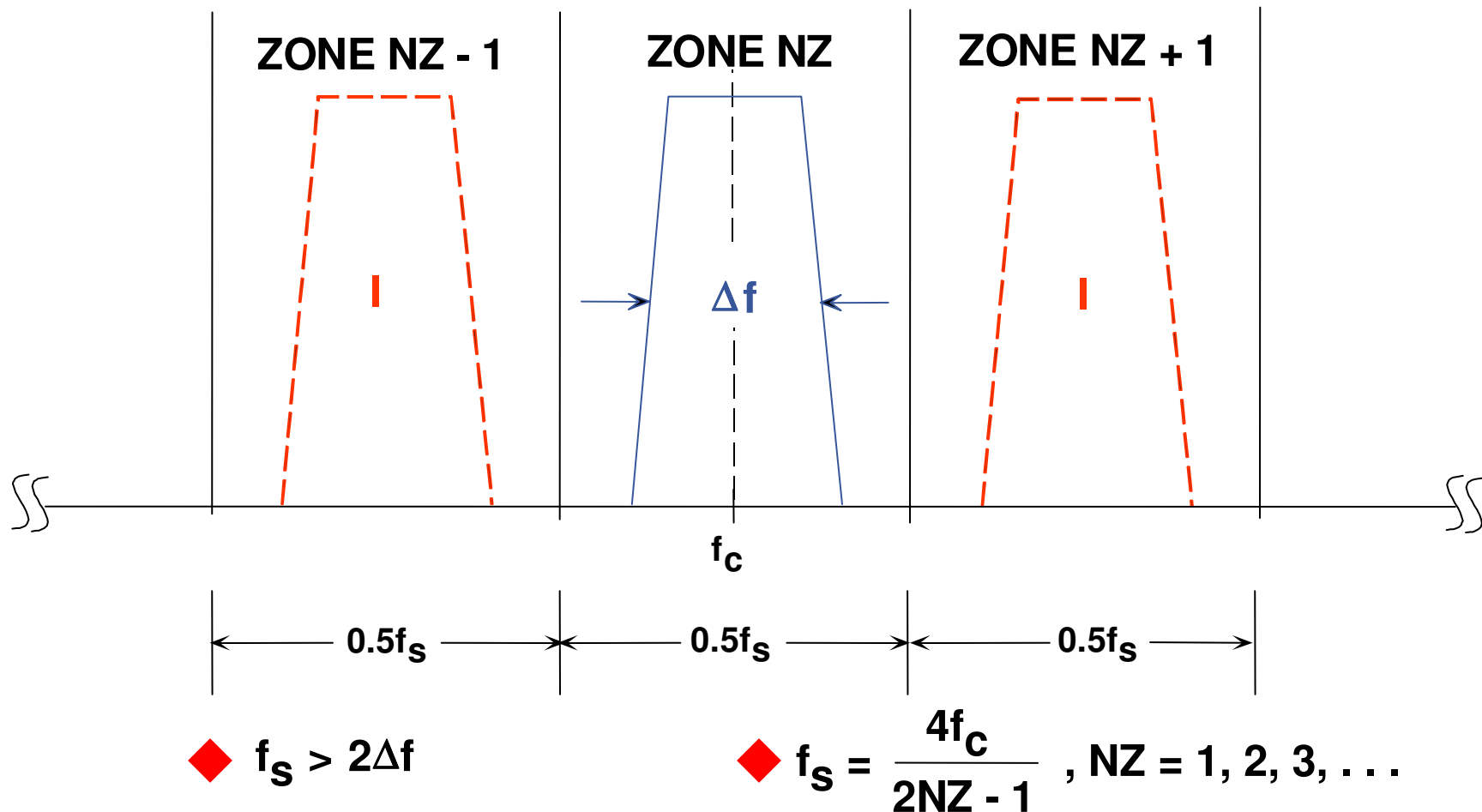
Antialiasing Filter for Undersampling



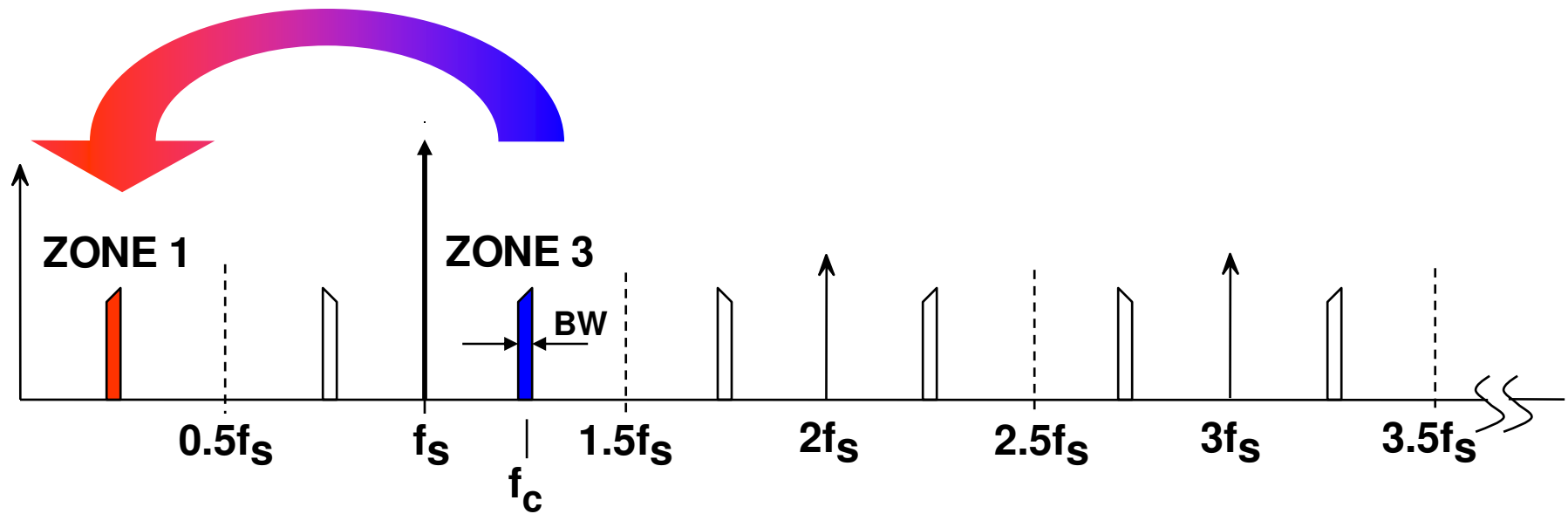
BANDPASS FILTER SPECIFICATIONS:

STOPBAND ATTENUATION = DR
TRANSITION BAND: f_2 TO $2f_s - f_2$
 f_1 TO $f_s - f_1$
CORNER FREQUENCIES: f_1, f_2

Centering an Undersampled Signal within a Nyquist Zone



Undersampling and Oversampling Combined Results in Process Gain

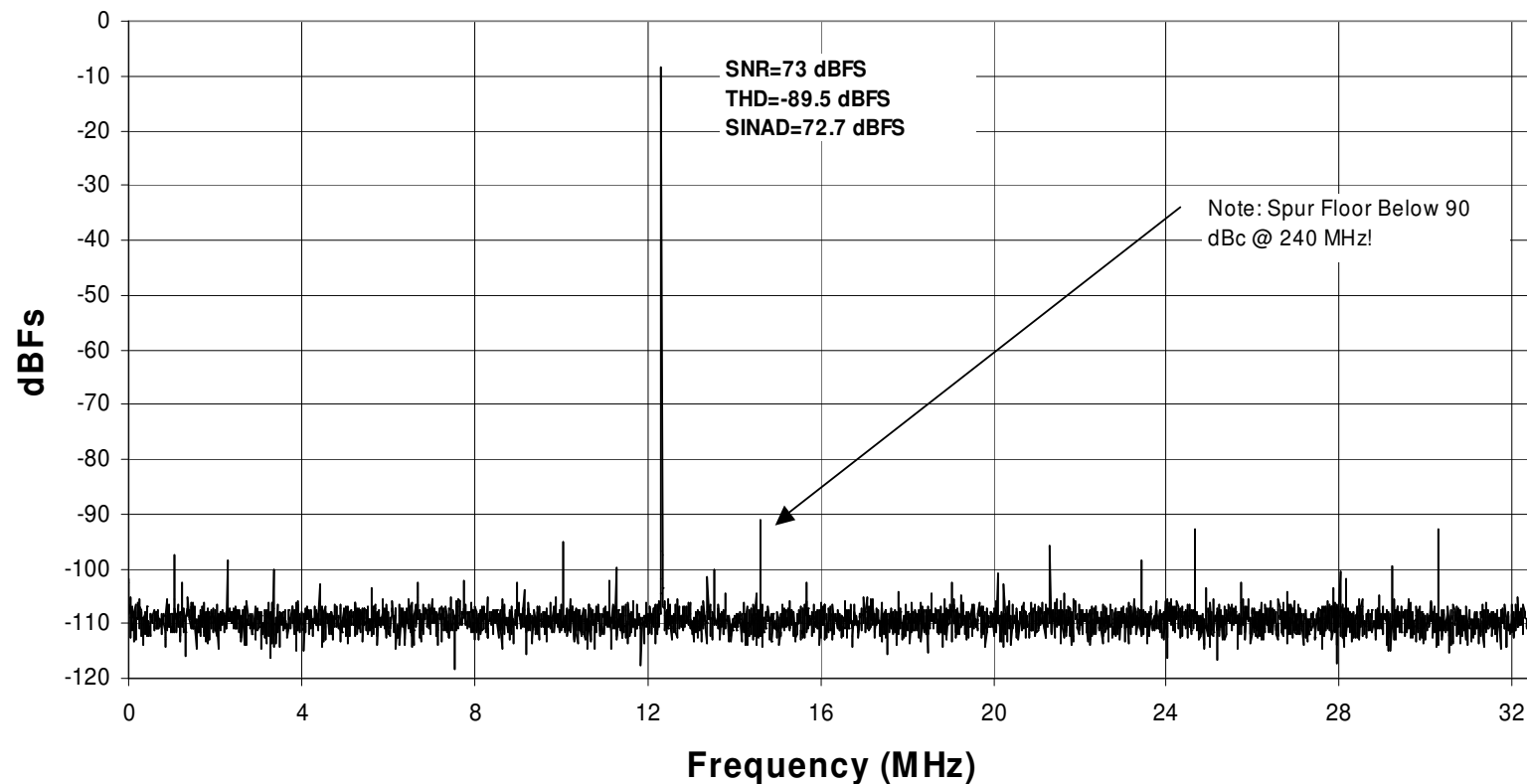


$$\text{SNR} = 6.02N + 1.76\text{dB} + 10\log_{10} \left[\frac{f_s}{2 \cdot BW} \right] \text{ FOR FS SINEWAVE}$$

Process Gain

Measurement of ADC in Undersampling Application



AD9244 with $F_{IN}=240$ MHz and $F_{CLK}=65$ MSPS
(2 V Input Span-Differential, $A_{in}=-8.5$ dBFS)



ADI Design Tools @ ANALOG.COM

The screenshot displays the Analog Devices website interface. At the top, a navigation bar features colorful icons for various product categories: Amplifiers, Power Management, Processors, DSP, MEMS, and Converters. Below this, the Analog Devices logo is accompanied by the tagline "World leader in high performance signal processing". A search bar with a "GO" button and links for "Parametric search" and "Replacement parts search" is located on the left. A large banner on the right reads "ADI in Industry and Aerospace" with an image of an airplane. Below the banner, a welcome message says "Welcome. [Log in](#) to access your preferences." The main content area is divided into three columns. The first column, "Find the Right Products", lists "MEMS and Sensors", "Amplifiers and Comparators", and a "Show All" link. The second column, "Explore Applications", lists "Video & Imaging Solutions", "Medical Solutions", "Audio Solutions", and a "Show All" link. The third column, "Use Design Tools Get Support", is circled in orange and contains the text "If you need help, contact Technical Support". Below these columns, there are three main sections: "Design Tools" (listing ADIsim, Amplifier Error Budget Analysis, DAC Harmonic Analyzer, Design Calculators, I/O Subsystem Software Tools, Input Stage and Filter Design, Multisim SPICE Program Download, Power Management, Software Configurable Products, Symbols & Footprints, and Utilities and Conversions), "Evaluation Boards & Kits", and "Simulation Models" (listing BSDI Files, IBIS Models, SABER Models, Simulink Models, and SPICE Models). To the right of these sections, there are links for "Circuits from the Lab", "Technical Library" (including ADI (Pb) Lead Free, Analog Dialogue, Application Notes, Code Examples, Design Handbooks, FAQs, Glossary of EE Terms, IC Anomalies, Manuals, Packages Index, Reference Design, Solutions Bulletins, Technical Articles, Technical Documentation, User Guides, and White Papers), "Training & Tutorials" (including Seminars & Webcasts, Training, and Tutorials), "Embedded Processing & DSP" (including Development Tools, Knowledge Base, Learning and Development (Beginner's Guide to DSP, Training Publications, University Programs, Visual Learning & Development (VLD), and Workshops), "Software & Reference Designs" (including Code Examples, Software Development Kits (SDKs), Software Modules, Starter Kits, and Third Party Reference Designs), and "VisualDSP++ 90-Day Test Drive".


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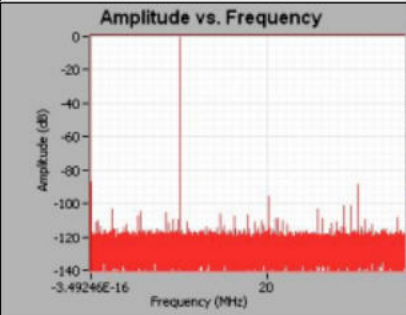

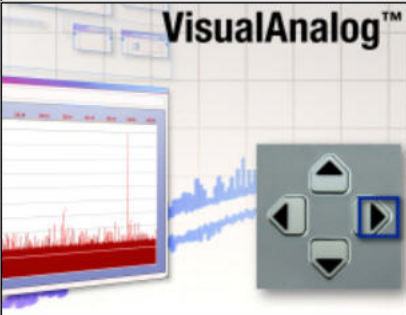
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High Speed ADC Evaluation Board Software and Behavioral Models

ADI has created [3 videos](#) that describe the features and benefits of VisualAnalog™ and how to interface VisualAnalog™ to an evaluation board.

Analyze ADC Performance Online	Configure Eval Boards and Predict ADC Performance	Customize Input Waveforms and ADC Analysis
		

ADIsimADC™ accurately models the typical performance characteristics of many of our High Speed Converters. There are three tools that use these models, giving designers consistent results at different stages of the design and evaluation process. [More info](#)

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AD9461

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STEP 1: Select an ADC Part

Select from Available (Modeled) Parts

16 Bit, 130 MSPS, AD9461-130

-- OR --

Perform a Part Search

Encode Rate: MSPS

(optional)

of Bits

SNR dB

SFDR dB

Suggested Parts (Best Fit)

STEP 2: Enter Operating Conditions

FFT Type: Single Tone

Amplitude: -0.5 dBFS output

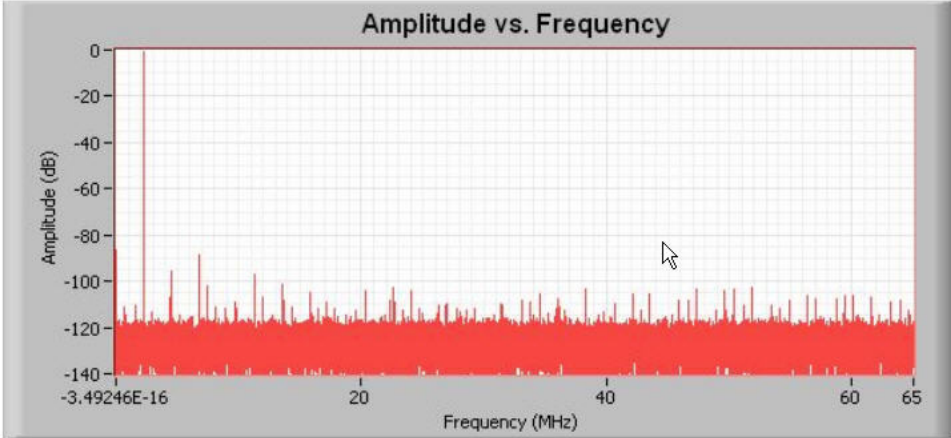
Frequency: 2.23 MHz

Encode Rate: 130 MSPS

Encode Jitter: 0.06 pSec

STEP 3: Run Model

Amplitude vs. Frequency



Amplitude (dB)

Frequency (MHz)

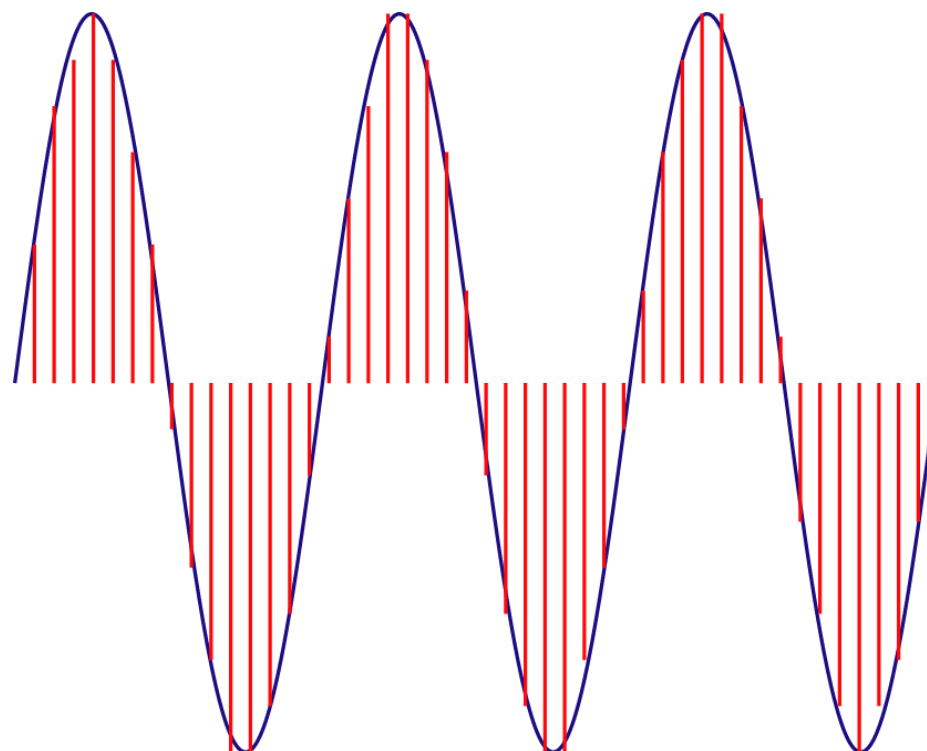
Results:

SNR:	78.17 dB	Fund:	-0.50 dBFS	Worst Other:	-101.81 dBc
SFDR:	88.02 dBc	2nd:	-94.92 dBc	Noise Floor:	-123.83 dBc
SINAD:	77.59 dBc	3rd:	-88.02 dBc		
THD:	86.58 dBc	4th:	-115.20 dBc		
ENOB:	12.60 Bits	5th:	-96.71 dBc		

Log:

No Messages

Quantization Error



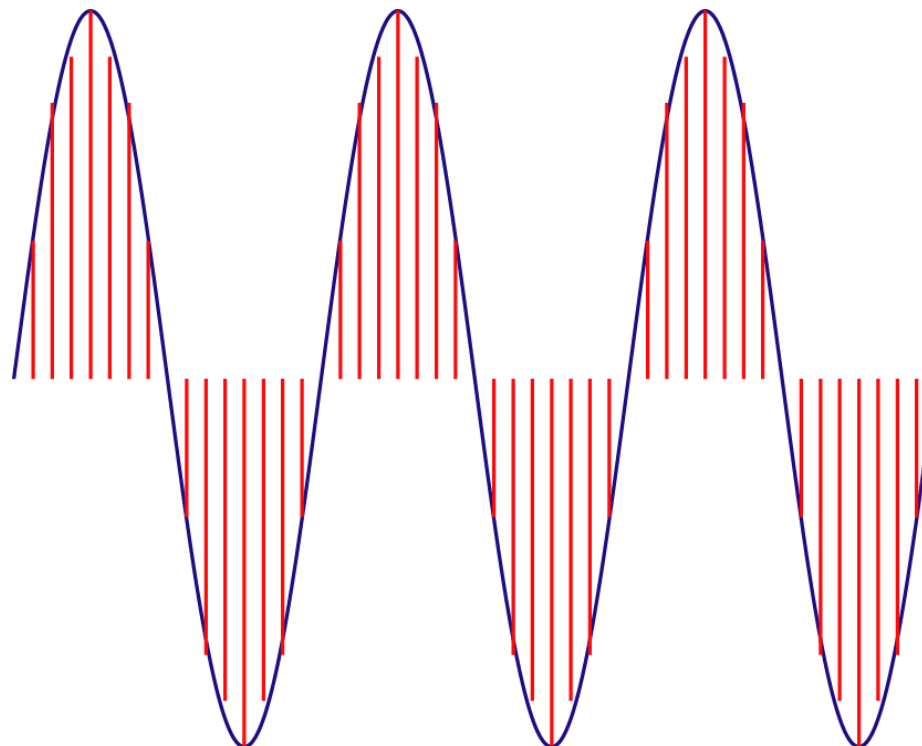
Note – 3 cycles, 47 samples, so error signal is not periodic, looks random, has noise like characteristics

Real Time and Discrete Time Digitized Signals (four bits resolution)



Quantization Error (noise) for Signal Above, scaled to 5x

Quantization Error



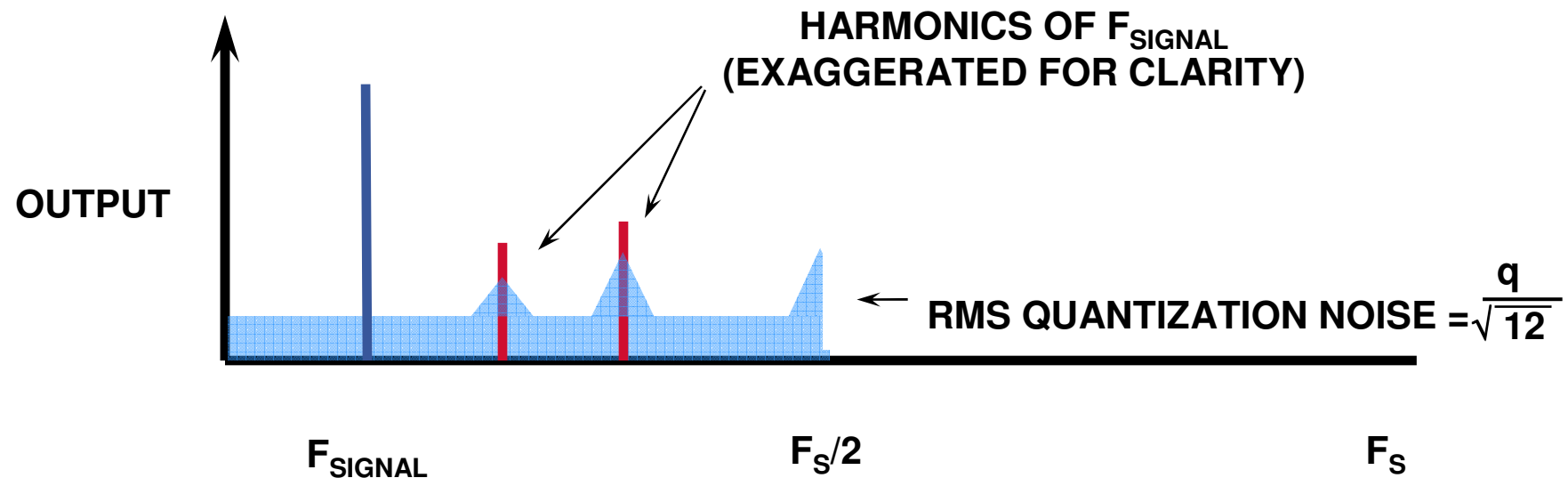
Note – 3 cycles, 48 samples, so error signal is periodic, quantization error will not be noise like, may have strong spectral components

Real Time and Discrete Time Digitized Signals (four bits resolution)




Quantization Error (periodic) for Signal Above, scaled to 5x

Quantization Noise in Correlated Sampling



If the Quantization Noise Is Uncorrelated With the AC Input Signal,
The Noise Will Be Spread Evenly Over the Nyquist Bandwidth of $F_s/2$. (approx. white)
If, however, the Input Signal Is Locked to a Sub-multiple of the Sampling Frequency,
The Quantization Noise Will No Longer Appear Uniform, but As Harmonics of the
Fundamental Frequency (becomes “colored”)

Problem – Correlated Sampling



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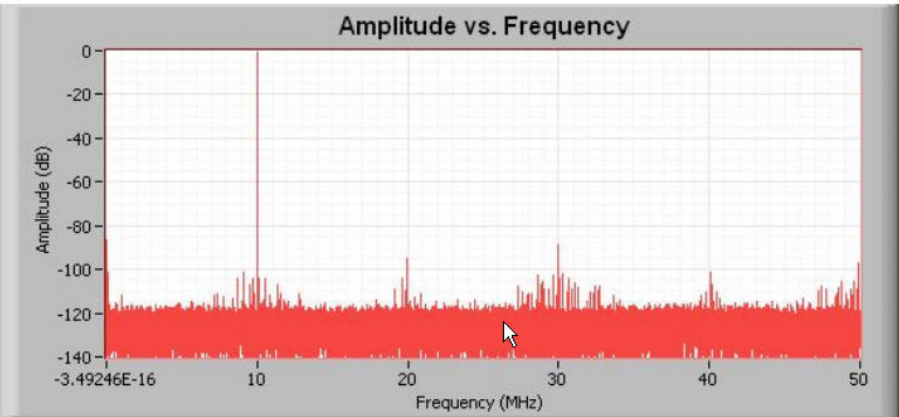
STEP 1: Select an ADC Part
Select from Available (Modeled) Parts
16 Bit, 130 MSPS, AD9461-130
-- OR --
Perform a Part Search
Encode Rate: MSPS
(optional)
of Bits:
SNR: dB
SFDR: dB

Suggested Parts (Best Fit)

STEP 2: Enter Operating Conditions
FFT Type: Single Tone
Amplitude: -0.5 dBFS output
Frequency: 10 MHz
Encode Rate: 100 MSPS
Encode Jitter: 0.06 pSec

STEP 3: Run Model

Amplitude vs. Frequency



Amplitude (dB) vs. Frequency (MHz)

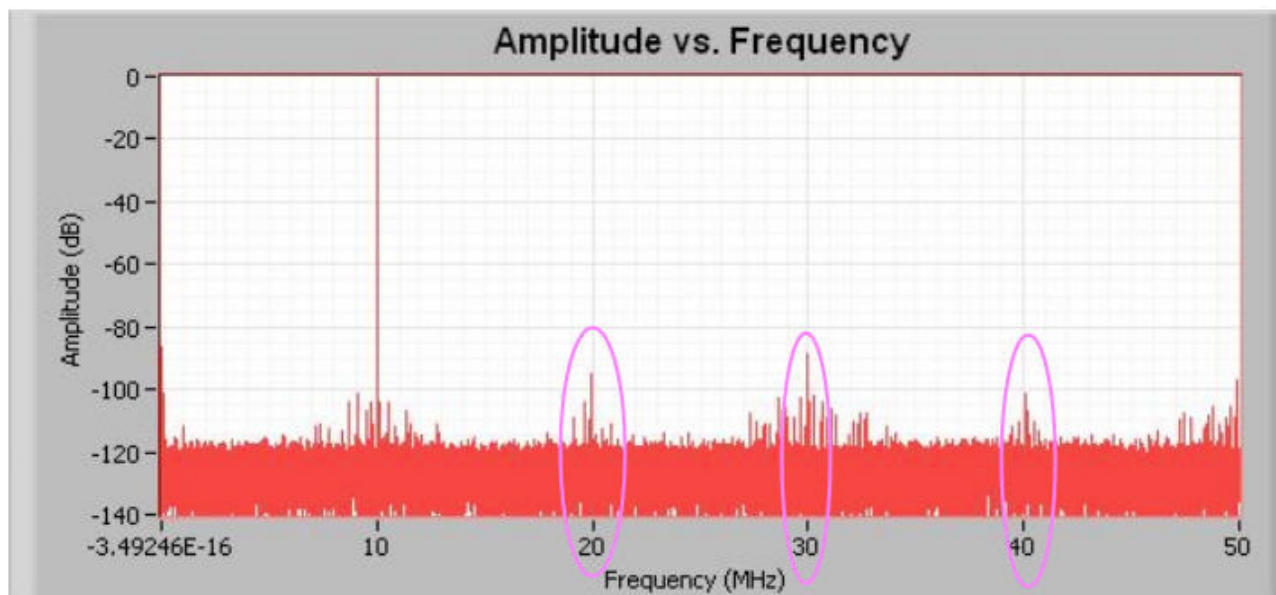
Results:

SNR:	78.14 dB	Fund:	-0.50 dBFS	Worst Other:	-101.03 dBc
SFDR:	88.15 dBc	2nd:	-94.59 dBc	Noise Floor:	-123.80 dBc
SINAD:	77.57 dBc	3rd:	-88.15 dBc		
THD:	86.64 dBc	4th:	-123.30 dBc		
ENOB:	12.59 Bits	5th:	-96.91 dBc		

Log:

The specified encode rate is an integer multiple of the entered signal frequency. This relationship leads to degraded performance and should be avoided. The quantization noise tends to be concentrated at harmonics of the fundamental leading to dramatically reduced SFDR. For better performance choose an encode rate that does not have an integer relationship to the signal frequency.

Correlated Sampling

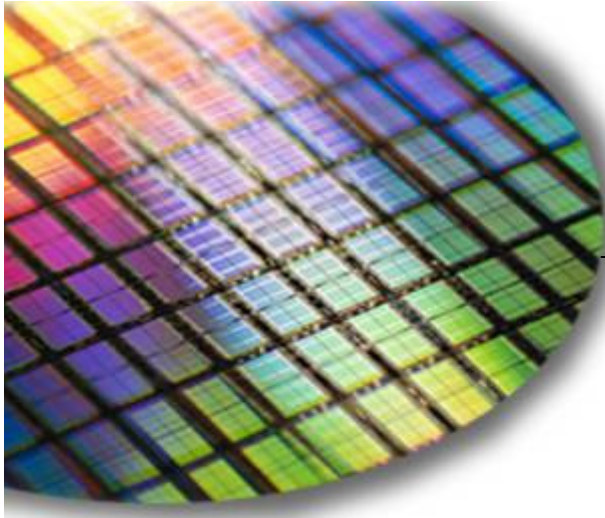


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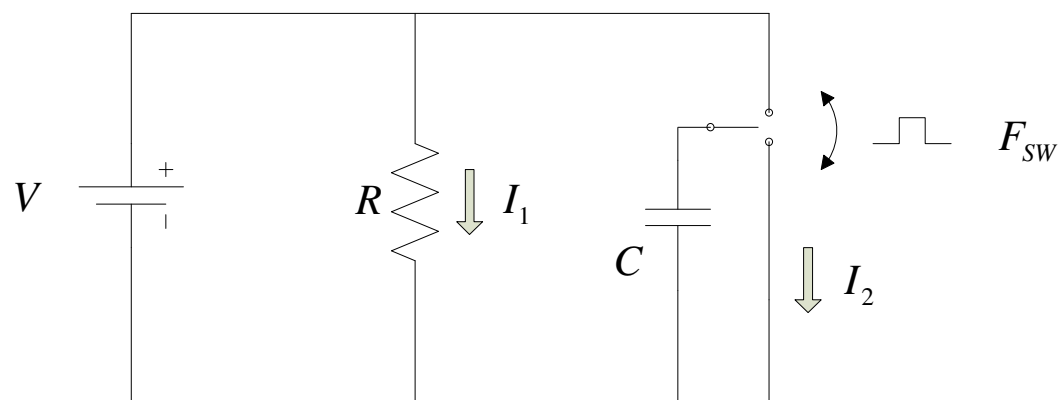
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Switched Cap Filters

Not all Sampled Data Systems are Converters

Switched Cap Filter Operation



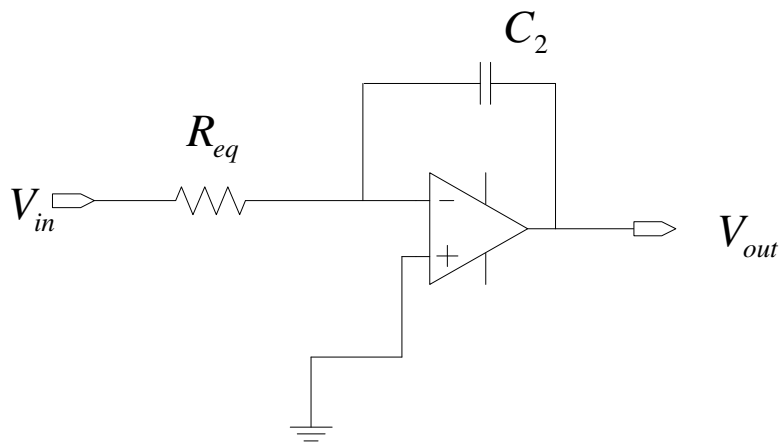
$$I_1 = V/R$$

$$Q = CV$$

$$QF_{SW} = CVF_{SW} = I_{2Avg}$$

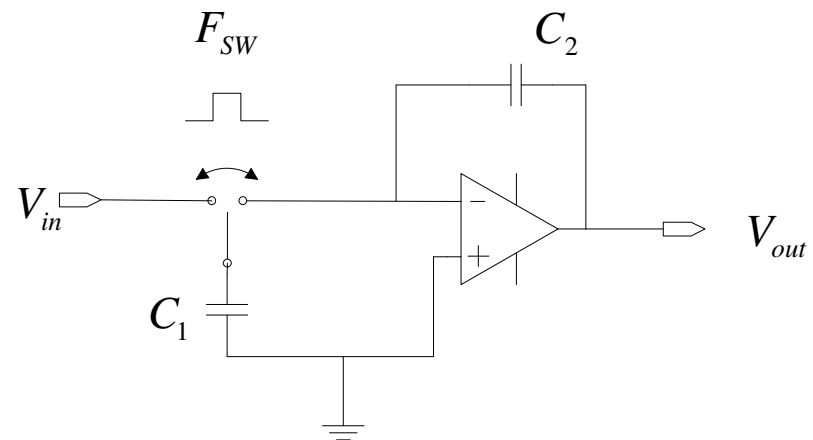
$$R_{eq} = \frac{I_{2Avg}}{V} = \frac{1}{CF_{SW}}$$

Filters : Linear vs Switched Cap



Linear integrator

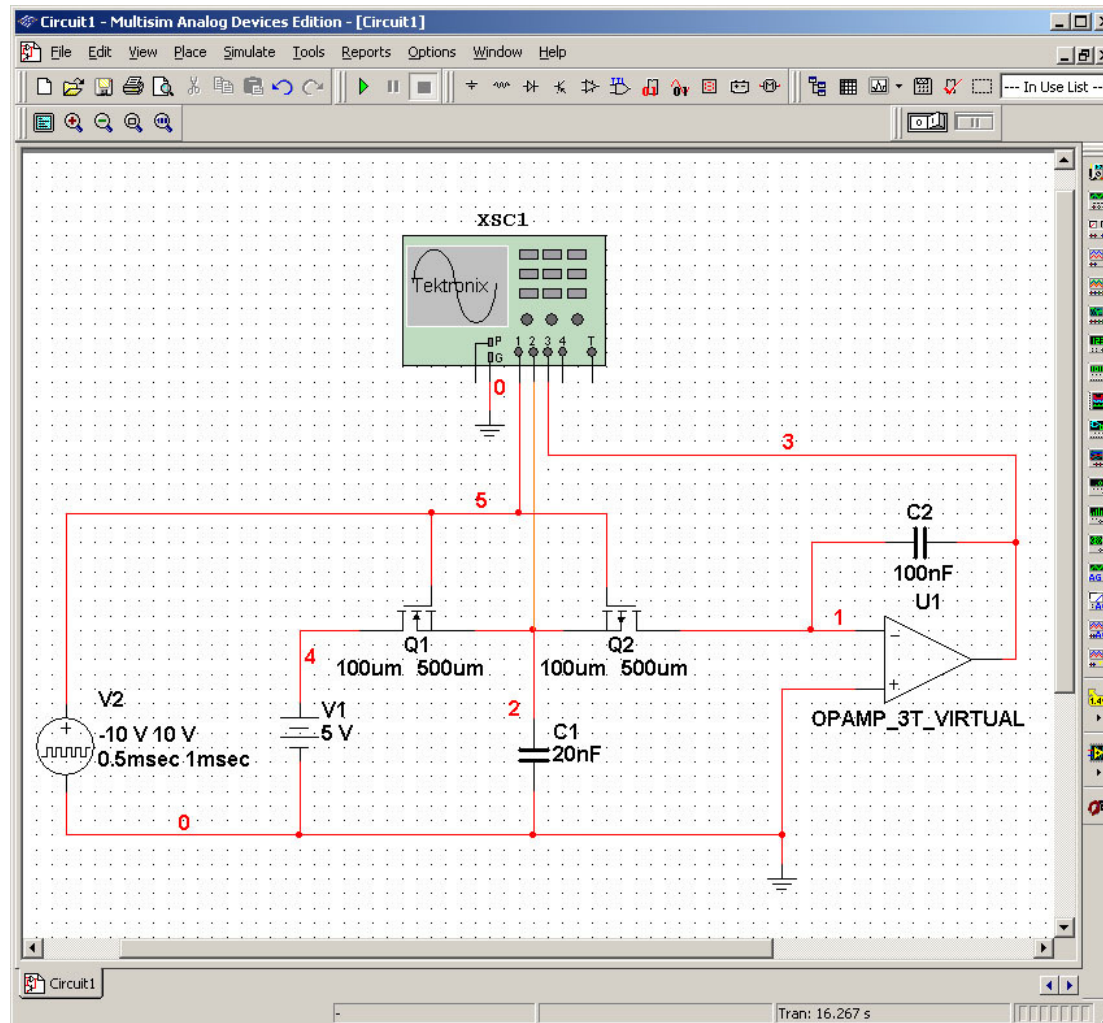
$$V_{out} = \frac{-1}{R_{eq} C_2} \int V_{in} dt$$



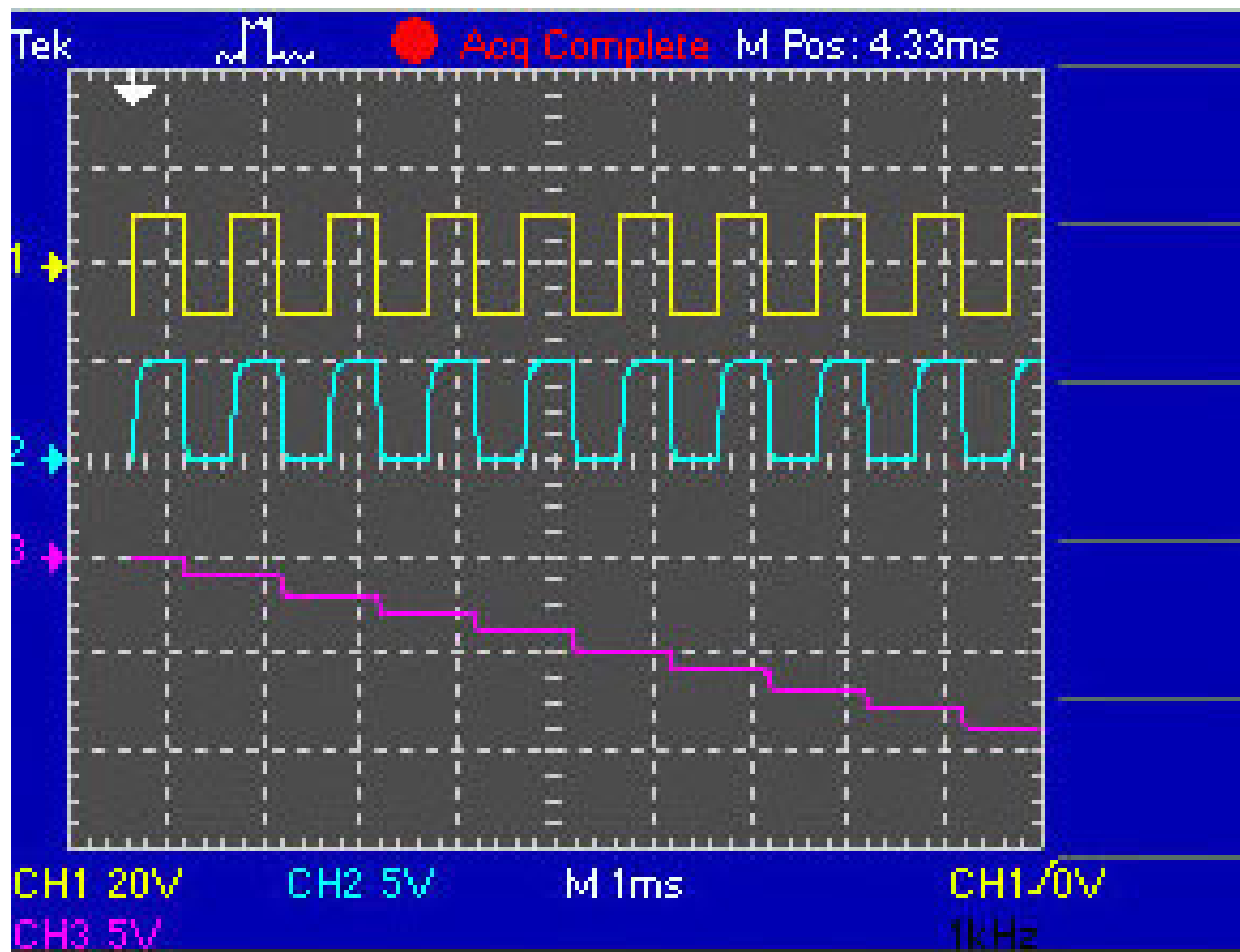
Switched cap integrator

$$V_{out} = \frac{-1}{\left(\frac{1}{F_{sw} C_1} \right) C_2} \int V_{in} dt$$

Switched Cap Simulation



Switched Cap Filters needs Filtering



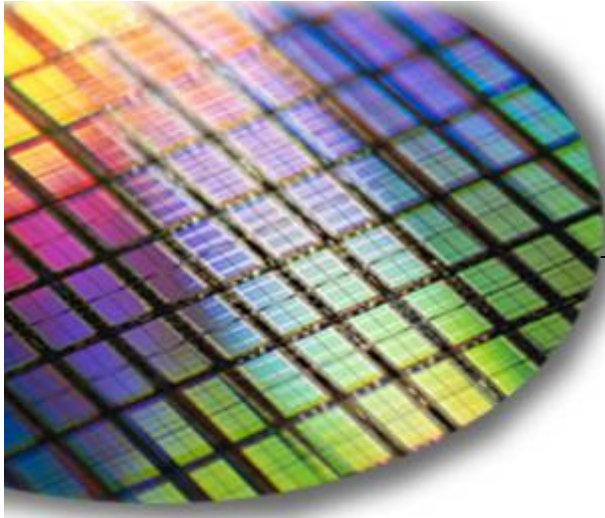
Switched Cap Filters Pro/Con

◆ Pros

- Complex analog filters can be built on chip
- Can adjust filter parameters by varying input clock

◆ Cons

- Needs antialiasing & reconstruction filters
- More limited function than equivalent ADC+DSP+DAC signal chain
- Limited bandwidth

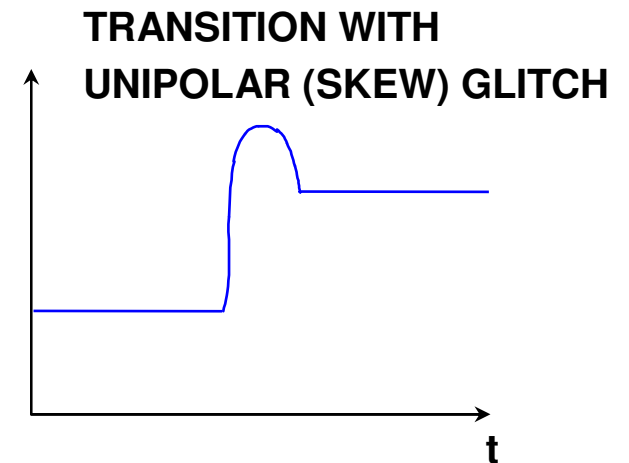
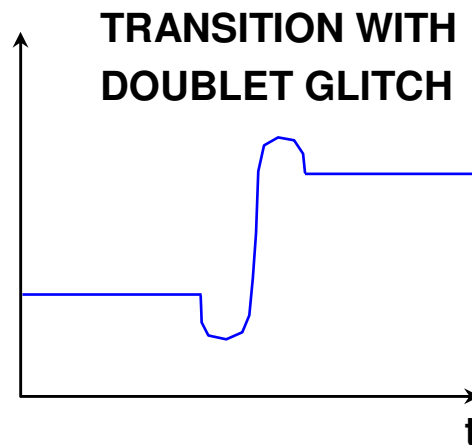
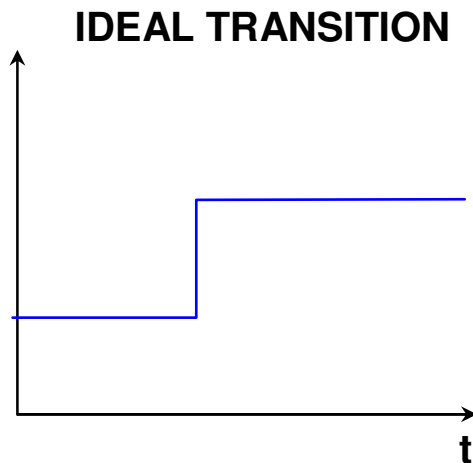
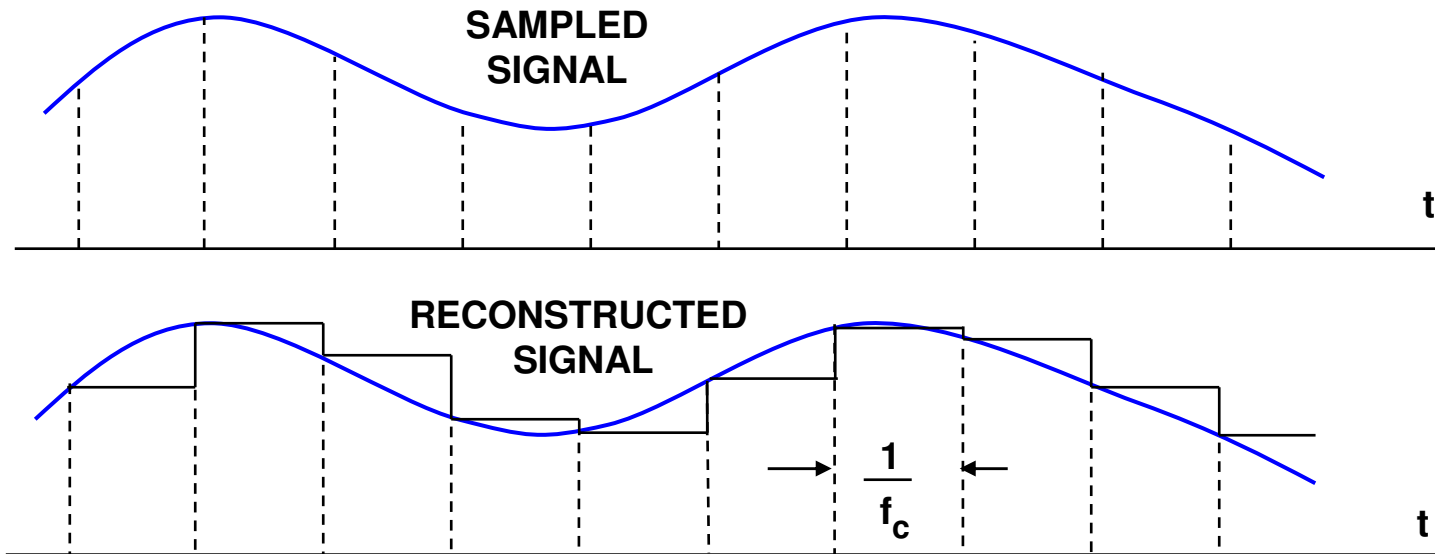


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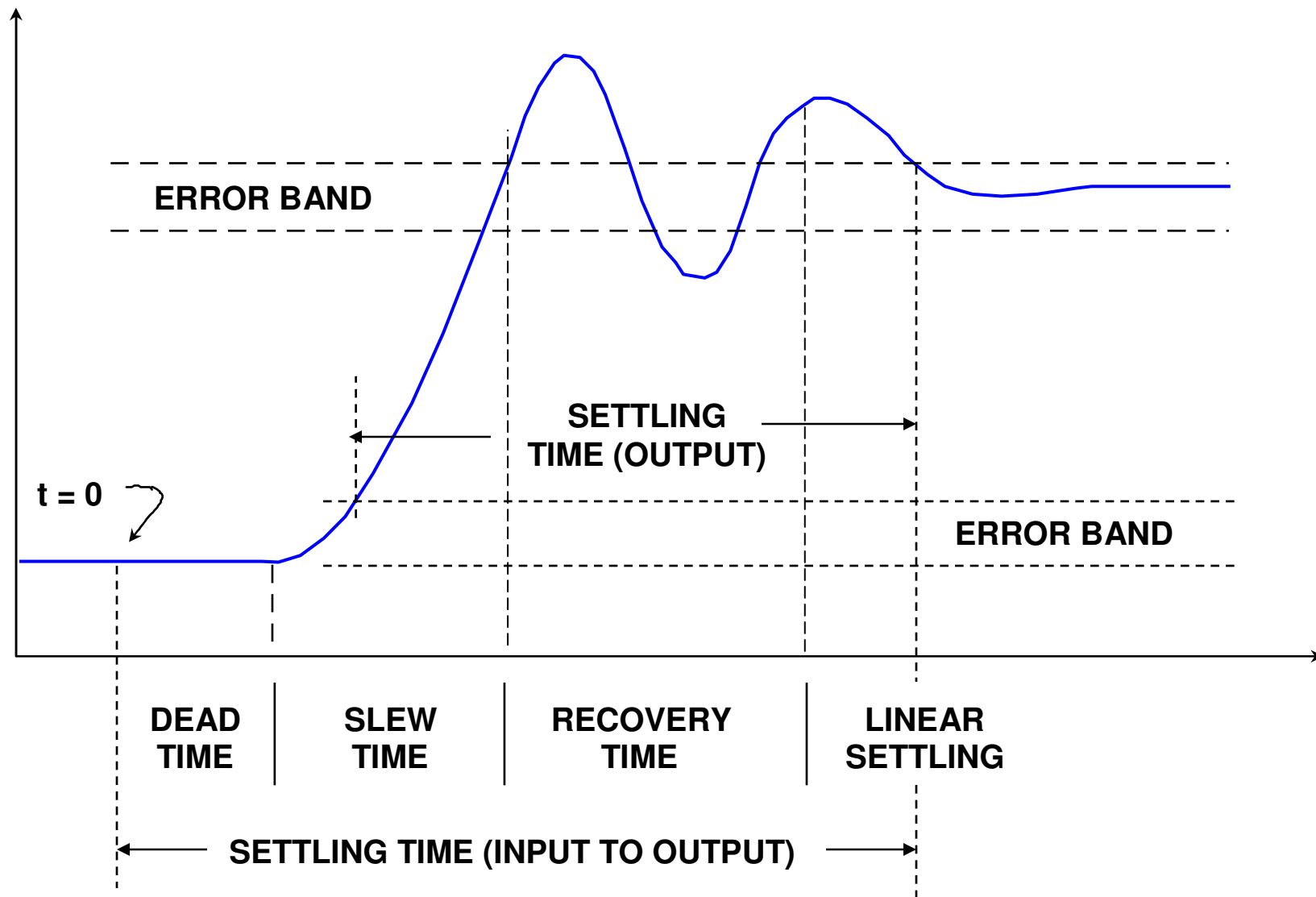


Digital to Analog Converters

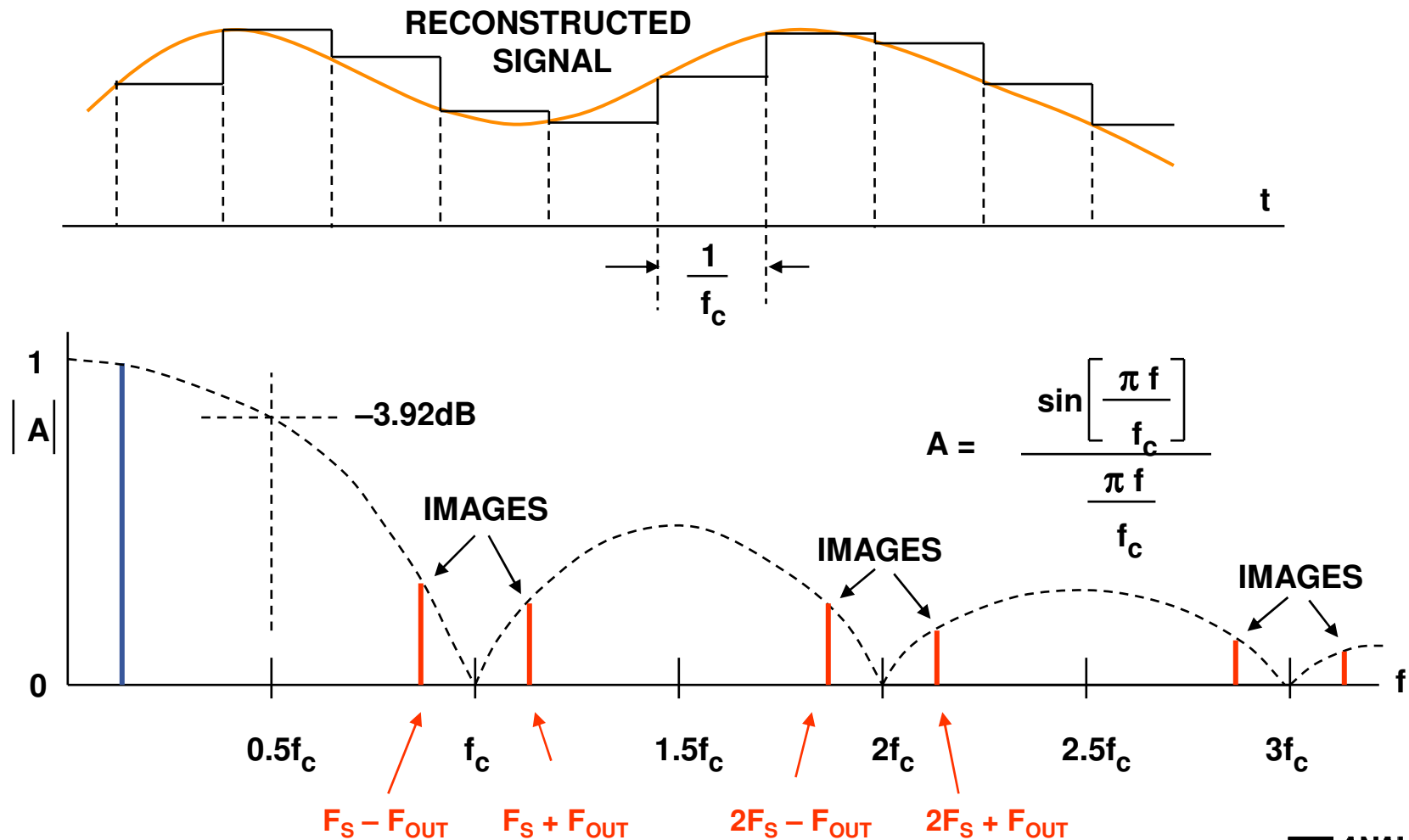
DAC Signal Construction



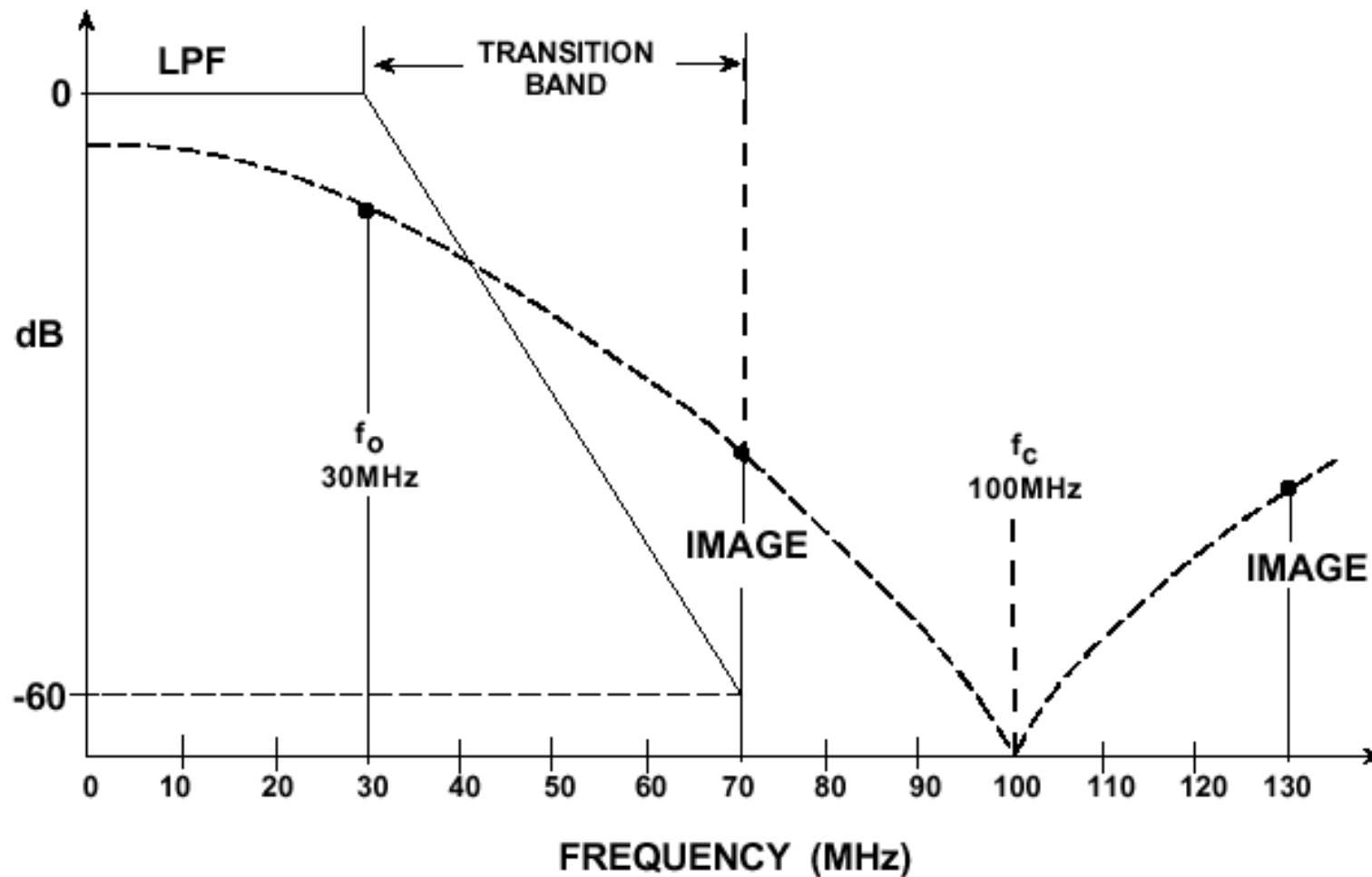
DAC Settling Time



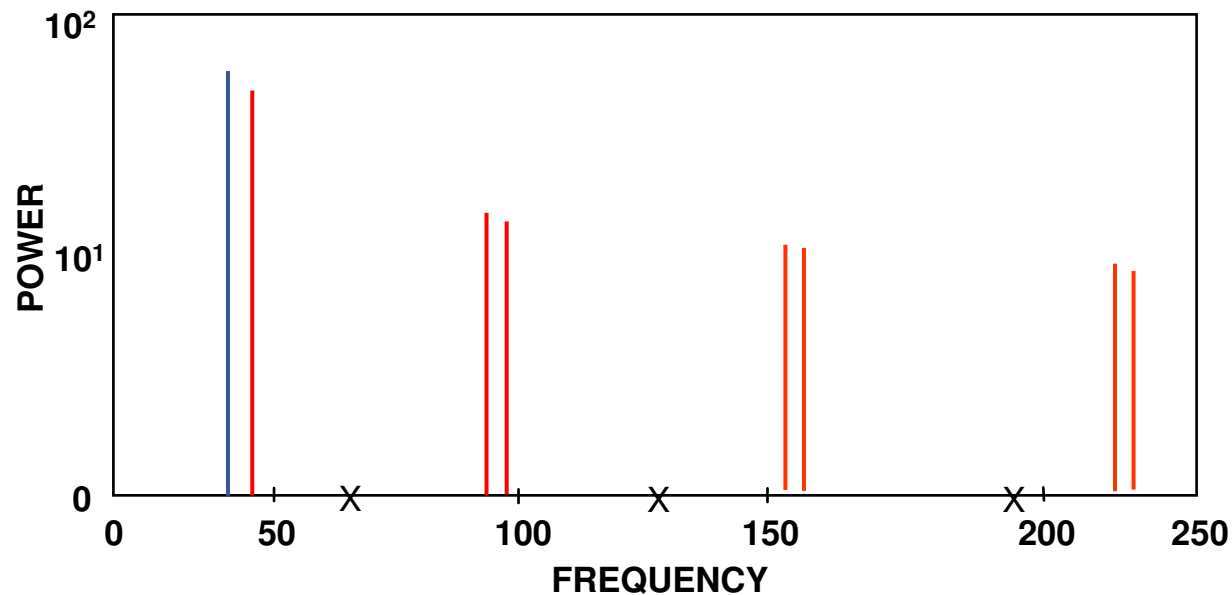
DAC sin x/x Roll Off (Amplitude Normalized)



LPF Required to Reject Image Frequency



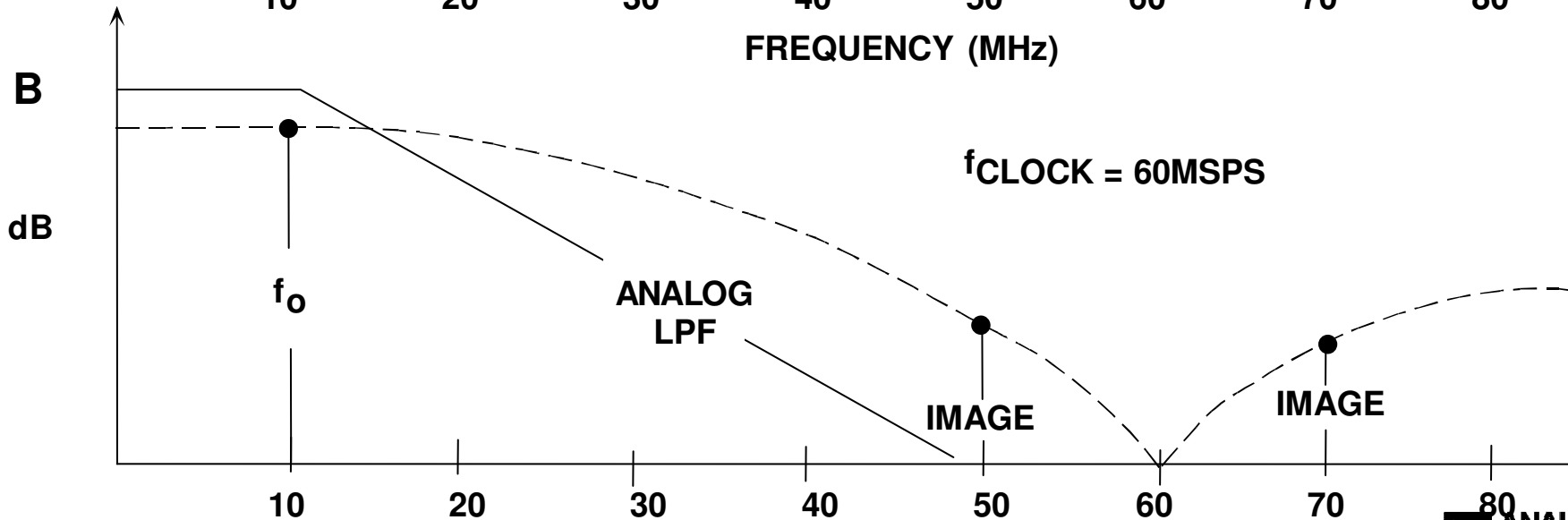
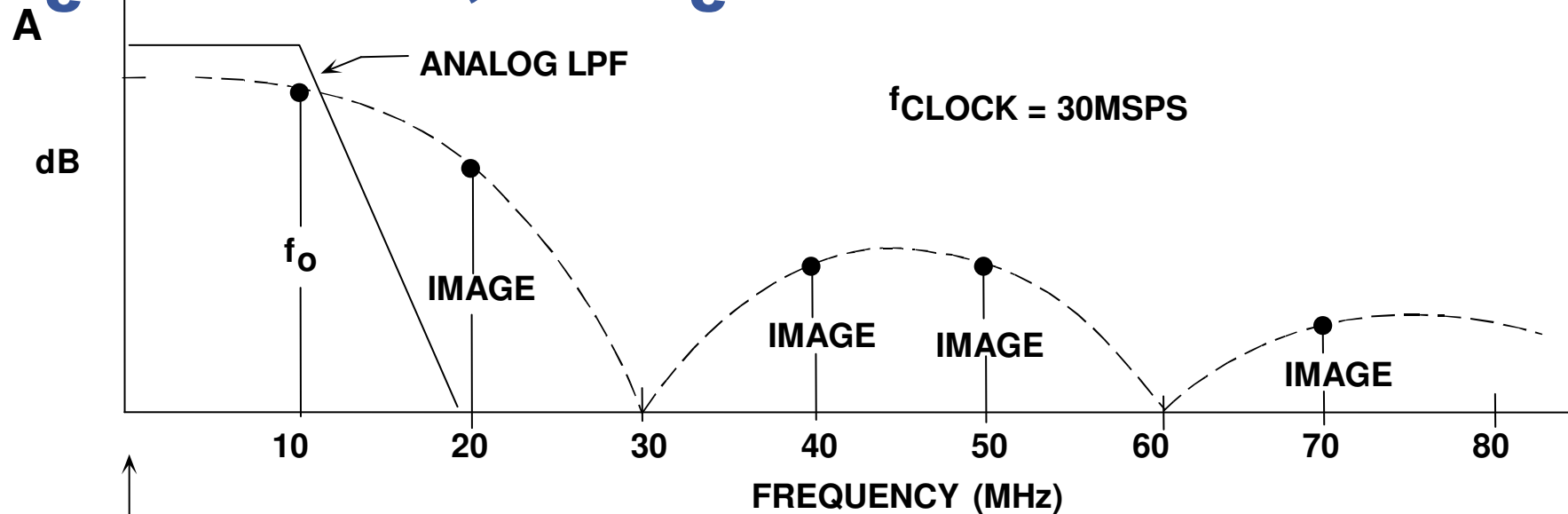
DAC Images (continued)



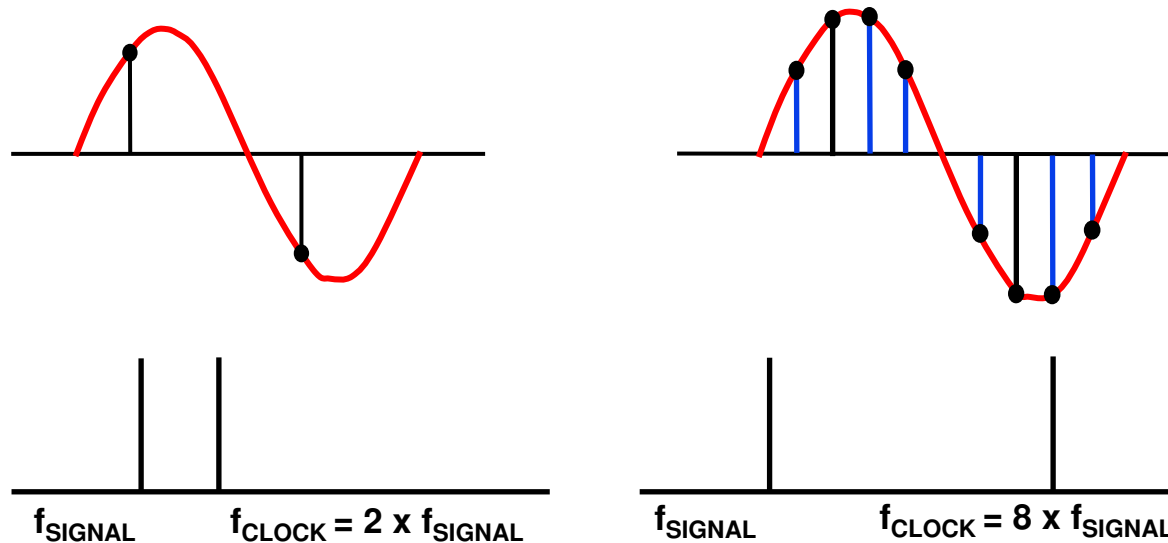
In the above example, $F_{OUT} = 0.453 F_s$

As the DAC output (F_{OUT}) approaches Nyquist frequency, the images come closer together, making it extremely difficult to filter the image from the signal.

Analog Filter Requirements for $f_o = 10\text{MHz}$: $f_c = 30\text{MSPS}$, and $f_c = 60\text{MSPS}$

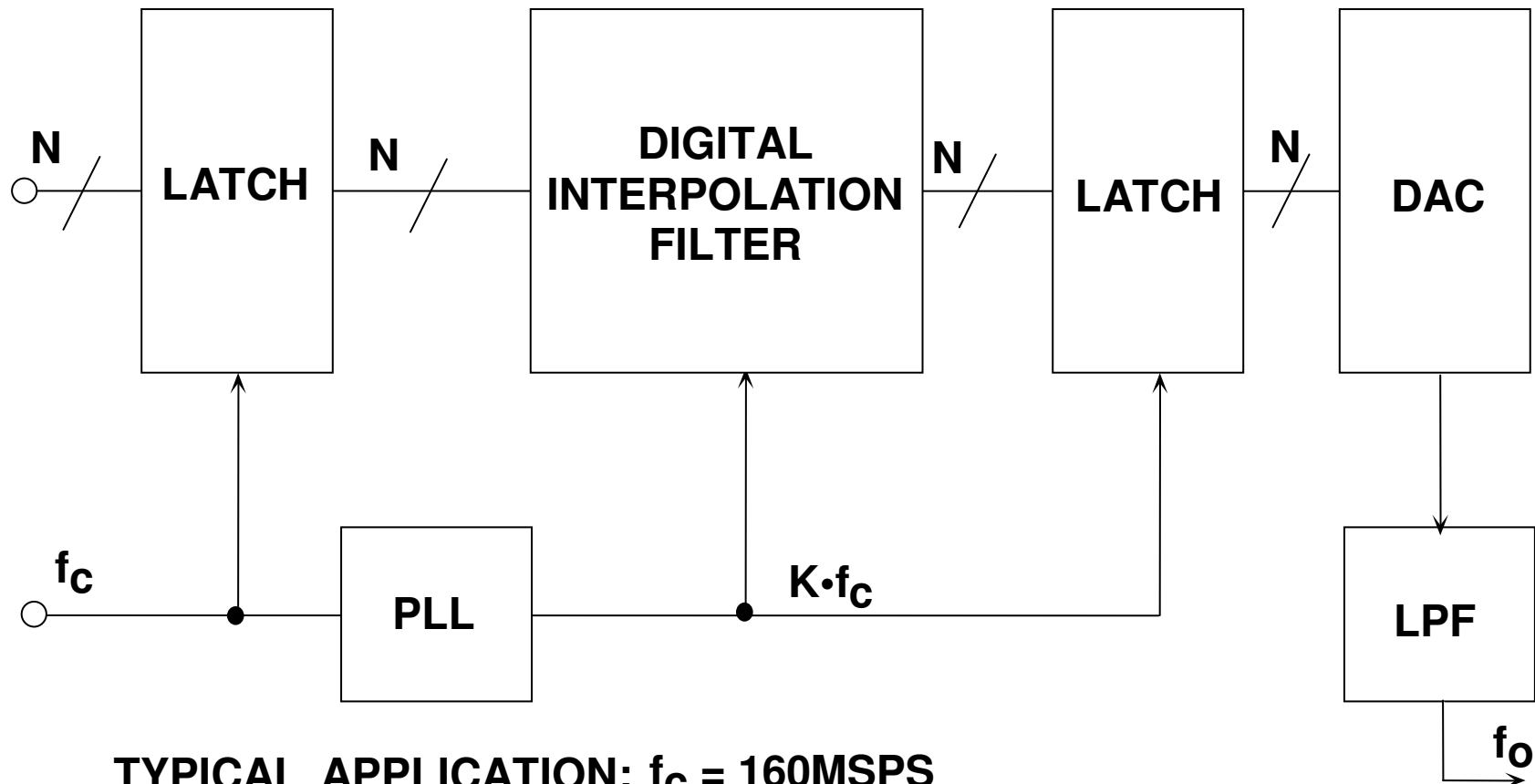


Interpolation



- Maximum Output Frequency of Standard DAC is $F_{\text{CLOCK}} \div 2$ (Nyquist Rate).
- In an Interpolating D/A Converter, Digital Interpolation Filters and a PLL Clock Multiplier are Used to Multiply the Input Data Rate to the DAC by a Factor of x Times the Clock Rate.
- Produces an Image at x Times F_{SIGNAL} , Smoothing the Sine Function and Simplifying the Filter Requirements and digital interface.

Oversampling Interpolating Txdac™ Simplified Block Diagram



TYPICAL APPLICATION: $f_c = 160\text{MSPS}$

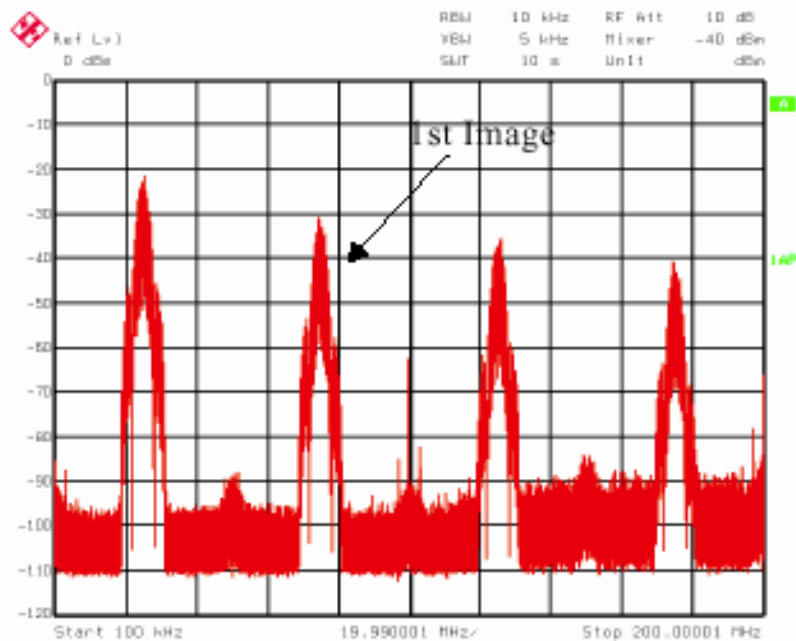
$f_o = 50\text{MHz}$

$K = 2$

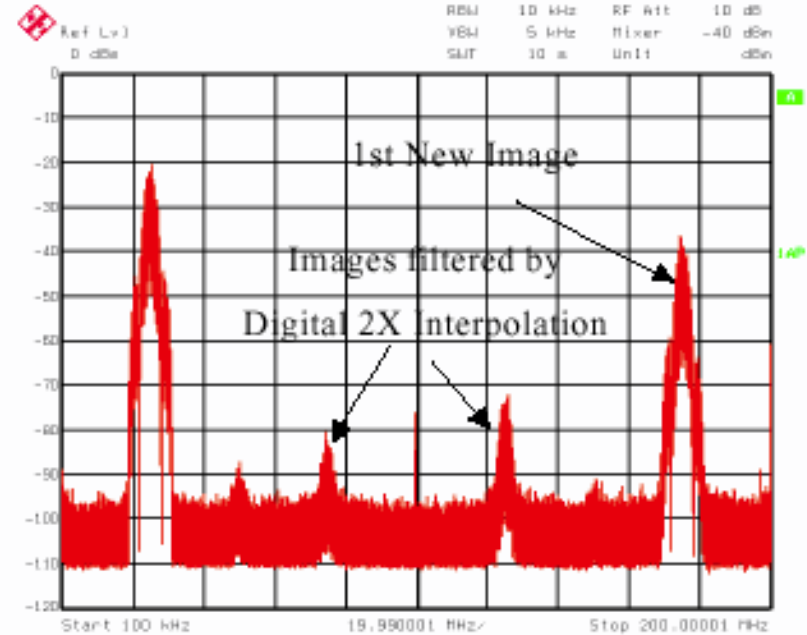
Image Frequency = $320 - 50 = 270\text{MHz}$

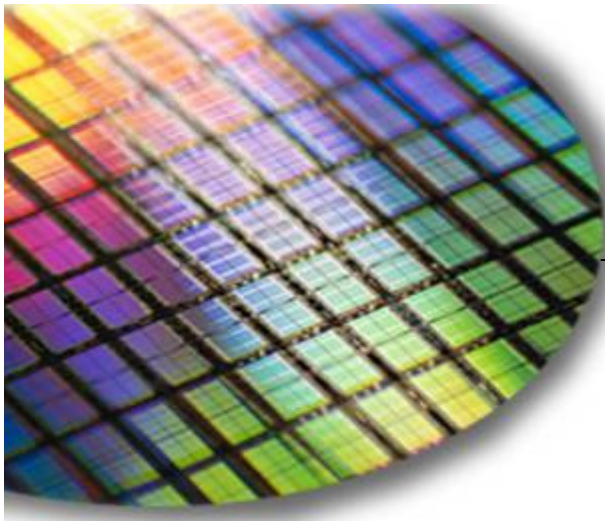
AD9772: 2X interpolation versus Nyquist DAC

Nyquist DAC



AD9772 DAC

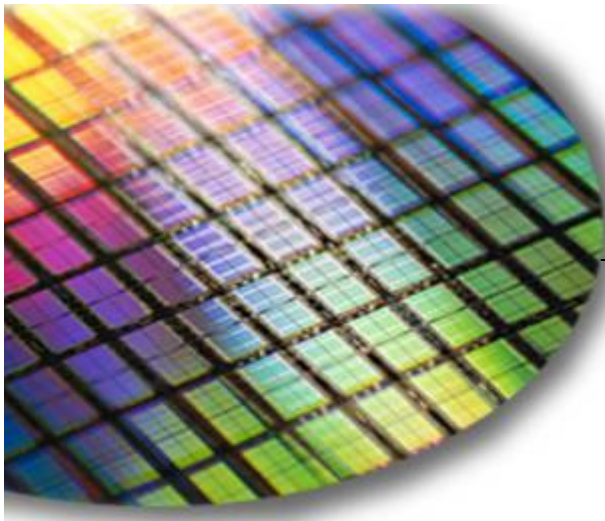




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Next Time (Part 2): Architectural Considerations Linearity, Distortion, Noise Care & Feeding (Application) Tips



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Much More to come in Part 2

For more information

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