ATtiny3224/3226/3227

Silicon Errata and Data Sheet Clarifications

The ATtiny3224/3226/3227 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002345), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny3224/3226/3227 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002345) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A
ADC	2.2.1 Low Latency Mode Must Be Set Before Changing ADC Configuration	X
ADC	2.2.2 The PGA Initialization Delay Does Not Work Outside Low Latency Mode	X
CCL	2.3.1 The CCL Must be Disabled to Change the Configuration of a Single LUT	X
TCB	2.4.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.5.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 ADC - Analog-to-Digital Converter

2.2.1 Low Latency Mode Must Be Set Before Changing ADC Configuration

If using the low latency mode in the ADC, the initialization delay does not start for settings configured before the Low Latency (LOWLAT) bit in the Control A (ADCn.CTRLA) register. This may result in a conversion starting before the initialization time has ended and give a corrupt result.

Work Around

Enable the low latency bit (LOWLAT) in the Control A (ADCn.CTRLA) register at the start of ADC initialization before configuring any other register in the ADC.

Affected Silicon Revisions

Rev. A
X

2.2.2 The PGA Initialization Delay Does Not Work Outside Low Latency Mode

The initialization delay for the PGA does not start when the LOWLAT bit is '0'. This may cause a corrupt conversion when the PGA is the module with the slowest initialization time. When using the internal references, this is not an issue because of a slower initialization delay.

Work Around

Set the ADC in low latency mode by setting the Low Latency (LOWLAT) bit in the Control A (CTRLA) register to '1'.

Affected Silicon Revisions

Rev. A
X

2.3 CCL - Configurable Custom Logic

2.3.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None

Affected Silicon Revisions

Rev. A
X

2.4 TCB - 16-Bit Timer/Counter Type B

2.4.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A
X

2.5 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.5.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This results in the Start-of-Frame Detector being triggered and falsely detecting the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in the Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A
X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002345).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
A	09/2021	Initial document release

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