ACA 2016

Contributed Talk, Poster & Exhibition Session

摘要集（Poster 部分）

8 月 23 日

1. Micro-architectural Features for Malware Detection

Huicheng Peng, Jizeng Wei and Wei Guo
Tianjin Advanced Network Key Lab

Abstract: As the variety and complexity of attacks continue to increase, software-based malware detection can impose significant performance overhead. Recent works have demonstrated the feasibility of malware detection using hardware performance counters. Therefore, equipping a malware detector to collect and analyze micro-architecture features of CPUs to recognize malware at running time has become a promising method. In comparison to the software-based malware detection, hardware-based malware detection not only reduces the cost of system performance, but also possesses better detection capacity. However, hundreds of micro-architecture events can be monitored by hardware performance counters (HPCs) which are widely available in prevailing CPUs, such as Intel, ARM and so on. In this paper, we take Intel ivy bridge i3 processor as an example and examine most of these micro-architectural features. Instead of relying on experience, the Lasso algorithm is employed to reduce the dimensionality of feature vector to 6 elements. Furthermore, 4 classification methods based on supervised learning are applied for the selected features. We improve the classification accuracy rate of 15% on average. The results show that the micro-architectural features of this paper can reveal the behaviors of malware better.

2. H-TDMS: A System for Traffic Big Data Management

Xingcheng Hua, Jierui Wang, Li Lei, Bin Zhou, Xiaolin Zhang and Peng Liu
Zhejiang University

Abstract: Massive traffic data is produced constantly every day, causing problems in data integration, massive storage, high performance processing when applying conventional data management approaches. We propose a cloud computing based system H-TDMS (Hadoop based Traffic Data Management System) to capture, manage and process the traffic big data. H-TDMS designs a configurable tool for data integration, a scalable data scheme for data storage, a secondary index for fast search query, a computing framework for data analysis, and a web-based user-interface with data visualization service for user interaction. Experiments on actual traffic data show that H-TDMS achieves considerable performance in traffic big data management.

3. 集成 IO 硬件压缩加速器的 Hadoop 系统结构

雷力，钱斌海，郭俊，顾雄礼，刘鹏
浙江大学

摘要：随着大数据的发展，Hadoop 系统成为了大数据处理中的重要工具之一。在实际应用中，Hadoop 的 I/O 操作制约系统性能的提升。通常 Hadoop 系统通过软件压缩数据来减少 I/O

操作，但是软件压缩速度较慢，因此使用硬件压缩加速器来替换软件压缩。Hadoop 运行在 Java 虚拟机上，无法直接调用底层 I/O 硬件压缩加速器。通过实现 Hadoop 压缩器/解压缩器类和设计 C++动态链接库来解决从 Hadoop 系统中获得压缩数据和将数据流向 I/O 硬件压缩加速器两个关键技术，从而将 I/O 硬件压缩加速器集成到 Hadoop 系统框架。实验结果表明，I/O 硬件压缩加速器的每赫兹压缩速度为 15.9Byte/s/Hz，集成 I/O 硬件压缩加速器提升 Hadoop 系统性能 2 倍。

4. GLDA: Parallel Gibbs Sampling for Latent Dirichlet Allocation on GPU

Pei Xue, Tao Li, Kezhao Zhao, Qiankun Dong, Wenjing Ma
Nankai University

Abstract: With the development of the general computing ability of GPU, more and more algorithms are being run on GPU, to enjoy much higher speed. In this paper, we propose an approach that uniformly accelerate Gibbs sampling for LDA (Latent Dirichlet Allocation) Algorithm on GPU, which makes the data load to the cores of GPU evenly to avoid the idle waiting for GPU, and improves the utilization of GPU. We use three text mining datasets to test the algorithm. Experiments show that our parallel methods can achieve about 30x speedup over sequential training methods with similar prediction precision. Furthermore, the idea that uniformly partitioning the data bases on GPU can also be applied to other machine learning algorithms.

5. OPTAS: Decentralized Flow Monitoring and Scheduling for Tiny Tasks

Ziyang Li, Yiming Zhang, Dongsheng Li and Yuxing Peng
National University of Defense Technology

Abstract: Task-aware flow schedulers collect task information across the data center to optimize task-level performance. However, the majority of the tasks, which generate short flows and are called tiny tasks, have been largely overlooked by current schedulers. The large number of tiny tasks brings significant overhead to the centralized schedulers, while the existing decentralized schedulers are too complex to fit in commodity switches.In this paper we present OPTAS, a lightweight, commodity-switch-compatible scheduling solution that efficiently monitors and schedules flows for tiny tasks with low overhead. OPTAS monitors system calls and buffer footprints to recognize the tiny tasks, and assigns them with higher priorities than larger ones. The tiny tasks are then transferred in a FIFO manner by adjusting two attributes, namely, the window size and round trip time, of TCP. We have implemented OPTAS as a Linux kernel module, and experiments on our 37-server testbed show that OPTAS is at least 2.2× faster than fair sharing, and 1.2× faster than only assigning tiny tasks with the highest priority.

6. A Model for Evaluating and Comparing Moving Target Defense Techniques based on Generalized Stochastic Petri Net

Guilin Cai, Baosheng Wang, Yuebin Luo, Wei Hu
National University of Defense Technology

Abstract: Moving Target Defense has been proposed as a way to alter the asymmetric situation of attacks and defenses, and there has been given a great number of related works. Currently, the performance evaluation of these works has largely been empirical, but lacks the application of theoretical models. Further, the evaluation is usually for a specific approach or a category of MTD approaches, and few work has been taken to compare different MTD techniques. In this paper, we consider a Web server as a deployment scenario for the three typical kinds of MTD techniques, and develop a generalized abstract performance evaluation and comparison model for existing MTDs through using generalized stochastic Petri Net (GSPN). We also take a case study to describe the usage of the model. The model enables us to analyze and understand the benefits and costs of an MTD approach, and can be viewed as an attempt to fill the gap of MTD comparison.

7. A Dynamic Latency-aware Load-Balancing Strategy In 2.5D NoC Architecture

Chen Li
National University of Defense Technology

Abstract: As the 3D stacking technology still faces several challenges, the 2.5D stacking technology gains better application prospects nowadays.With the silicon interposer, the 2.5D stacking can improve the bandwidth and capacity of the memory system. To satisfy the communication requirements of the integrated memory system, the free routing resources in the interposer should be explored to implement an additional network. Yet, the performance is strongly limited by the unbalanced loads between the CPU-layer network and the interposer-layer network. In this paper, to address this issue, we propose a dynamic latency-aware load-balancing (DLL) strategy. Our key innovations are detecting congestion of the network layer via the average latency of recent packets and making the network layer selection at each source node. We leverage the free routing resources in the interposer to implement a latency propagation ring.With the ring, the latency information tracked at destination nodes is propagated back to source nodes. We achieve loadbalance by using these information. Experimental results show that compared with the baseline design, a destination-detection strategy and a buffer-aware strategy, our DLL strategy achieves 45%, 14.9% and 6.5% of average throughput improvements with minor overheads.

8. Overcoming and Analyzing the Bottleneck of Interposer Network in 2.5D NoC Architecture

Chen Li, Zicong Wang, Lu Wang, Sheng Ma*, Yang Guo
National University of Defense Technology

Abstract: As there are still a lot of challenges on 3D stacking technology, 2.5D stacking technology seems to have better application prospects. With the silicon interposer, the 2.5D stacking can improve the bandwidth and capacity of memory. Moreover, the interposer can be explored to make use of unused routing resources and generates an additional network for communication. In this paper, we conclude that using concentrated Mesh as the topology of the interposer network faces the bottleneck of edge portion, while using Double-Butterfly can overcome this bottleneck. We analyze the reasons that pose the bottleneck, compare impacts of different topologies on bottlenecks and propose design goals for the interposer network.

9. High Performance Stencil Computations for Intel Xeon Phi Coprocessor

Luxia Feng, Yushan Dong, Chunjiang Li and Hao Jiang
National University of Defense Technology

Abstract: Stencil computations are a class of computational kernels which update array elements according to some stencil patterns, and they have drawn more attentions recently. The Intel Xeon Phi coprocessor, which is designed for high performance computing, has not been fully evaluated for stencil computations. In this paper, we present a series of optimizations to accelerate the 3-D 7-point stencil code on Intel Xeon Phi coprocessor. We focus on how to exploit the performance potential of many cores and wide-vector unit in each core. In order to exploit data locality, we use loop tiling and we propose a method for calculating the block size while tiling. The achieved performance brings a speedup of 211.6 in comparison with the serial code.

10. Coarse Granularity Data Migration Based Power Management mechanism for 3D DRAM Cache

Litiao Qiu, Lei Wang, Hongguang Zhang, Zhenyu Zhao , Qiang Dou
National University of Defense Technology

Abstract: 3D-stacked technology is a promising solution to improve the performance of on-chip memory system. In our work, a 3D DRAM Cache with high density and wide bandwidth is utilized as the Last Level Cache (LLC). With the same Cache area, a 3D DRAM Cache shows superior capacity, bandwidth, cost performance ratio to a SRAM Cache. However, 3D DRAM storage has a problem of high power consumption. The power consumption of die-stacked DRAM is 5x compared to plane DRAM. In order to solve this problem, we proposed a power management mechanism for 3D DRAM Cache in this paper. The core idea of our mechanism is closing the infrequent accessed banks for saving power consumption. We design and implement a trace-driven 3D DRAM Cache simulator based on DRAMSim2. Experiment result of SPEC CPU2006 shown that for most applications, some banks have little access during execution. We proposed a coarse granularity data migration based power management mechanism. Compared with the system without power management mechanism, the static power consumption of some

application decreased to 0.75x, a portion of application reach to 0.375x

11. A Novel Hybrid Last Level Cache Based on Multi-Retention STT-RAM Cells

Zhang Hongguang, Zhang Minxuan, Zhao Zhenyu, Tian Shuo
National University of Defense Technology

Abstract: Spin-transfer torque random access memory (STT-RAM) is one of the most promising substitutes for universal main memory and cache due to its excellent scalability, high storage density and low leakage power. A much larger cache capacity in the same die footprint can be implemented with STT-RAM because its area is only 1/9 to 1/3 that of SRAM. However, the non-volatile STT-RAM also has some drawbacks, such as long write latency and high write energy, which limit its application in cache design. To solve the two problems, we relax the retention time of STT-RAM to optimize its write performance and energy, and propose a novel multi-retention STT-RAM hybrid last level cache (LLC) architecture, which is realized with three different kinds of cells. In addition, we design the data migration scheme to manage its block allocation, thus improving overall system performance further. The experiment results show that our multi-retention hybrid LLC reduces the total power consumption by as much as 96.6% compared with SRAM LLC, while having almost the same (at 99.4%) instruction per cycle (IPC).

12. 一种解决访存调度问题的改进蚁群优化算法

田烁，窦强，王勇，张洪广，周朝兵，李石明
国防科学技术大学

摘要：存储器的访问调度策略是复杂的，不仅仅要考虑具体的电路时序参数，还有访存节拍数。在分析 DRAM 的特点以及访存调度策略的基础上，考虑 DDR3 时序规范，提出一种改进的蚁群优化访问调度策略。采用不同的 trace 作为测试，同贪婪式调度算法作比较，该算法可以有效降低平均总延迟、提高带宽利用率。

13. 高阶路由器结构研究综述

杨文祥，董德尊，雷斐，李存禄，吴际，孙凯旋
国防科学技术大学

摘要：随着高性能网络规模的增，高阶路由器结构设计成为高性能计算中研究的重点和热点。使用高阶路由器，网络能实现更低的报文传输延迟、网络构建成本和网络功耗，同时高阶路由器的应用还可以提高网络可靠性。过去十年是高阶路由器发展最快的时期，对近年高阶路由器的研究进行了综述，并对未来发展趋势进行了预测，主要介绍了以 YARC 为代表的经典

结构化设计以及“network within a network”等近年来涌现的新型设计方法。未来的研究重点是解决高阶路由器结构设计中遇到的缓存和仲裁等各种问题，并利用光互连等技术设计性能更好的结构。

14. An Energy Efficient Algorithm for Virtual Machine Allocation in Cloud Datacenter

Ahmad Ali, Yanmin Zhu, Li Lu and Jiadi Yu
Shanghai Jiao Tong University

Abstract: In cloud datacenters, virtual machine (VM) allocation in a power efficient way remains a critical research problem. There are a number of algorithms for allocating the workload among different machines. However, existing works do not consider more than one energy efficient host, thus they are not efficient for large scale cloud datacenters. In this paper, we propose a VM allocation algorithm to achieve higher energy efficiency in large scale cloud datacenters. Simulation result shows that, compared with BRS, RR and MPD algorithms, our algorithms can achieve 23%, 23% and 9% more power efficiency in large scale cloud environment.

15. Power Attack Defense: Securing Battery-Backed Data Centers

Chao Li, Xiaofeng Hou, Zhenhua Wang, Haopeng Chen, Xiaoyao Liang and Minyi Guo
Shanghai Jiao Tong University

Abstract: Battery systems are crucial components for mission-critical data centers. Without secure energy backup, existing under-provisioned data centers are largely unguarded targets for cyber criminals. Particularly for today’s scale-out servers, power oversubscription unavoidably taxes a data center’s backup energy resources, leaving very little room for dealing with emergency. Besides, the emerging trend towards deploying distributed energy storage architecture causes the associated energy backup of each rack to shrink, making servers vulnerable to power anomalies. As a result, an attacker can generate power peaks to easily crash or disrupt a power-constrained system. This study aims at securing data centers from malicious loads that seek to drain their precious energy storage and overload server racks without prior detection. We term such load as Power Virus (PV) and demonstrate its basic two-phase attacking model and characterize its behaviors on real systems. The PV can learn the victim rack’s battery characteristics by disguising as benign loads. Once gaining enough information, the PV can be mutated to generate hidden power spikes that have a high chance to overload the system. To defend against PV, we propose power attack defense (PAD), a novel energy management patch built on lightweight software and hardware mechanisms. PAD not only increases the attacking cost considerably by hiding vulnerable racks from visible spikes, it also strengthens the last line of defense against hidden spikes. Using Google cluster traces we show that PAD can effectively raise the bar of a successful power attack: compared to prior arts, it increases the data center survival time by 1.6~11X and provides better performance guarantee. It enables modern data centers to safely exploit the benefits that power oversubscription may provide, with the slightest

cost overhead.

16. An Energy Efficient Algorithm for Virtual Machine Allocation in Cloud Datacenters

Ahmad Ali,Li Lu, Yanmin Zhu and Jiadi Yu
Shanghai Jiao Tong University

Abstract: In cloud datacenters, virtual machine (VM) allocation in a power efficient way remains a critical research problem. There are a number of algorithms for allocating the workload among different machines. However, existing works do not consider more than one energy efficient host, thus they are not efficient for large scale cloud datacenters. In this paper, we propose a VM allocation algorithm to achieve higher energy efficiency in large scale cloud datacenters. Simulation result shows that, compared with BRS, RR and MPD algorithms, our algorithms can achieve 23%, 23% and 9% more power efficiency in large scale cloud environment.

17. 同时多线程架构下核内资源动态划分方法

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中科院计算所

摘要：受到数据中心应用复杂并且需求多变特征的影响，传统体系结构中的部分硬件部件固定功能的设计不能很好的满足这些混合多应用的场景需求。此外，如何在保持延迟敏感型应用服务质量同时有效地改善资源利用率也为数据中心服务器设计带来巨大的挑战。
为了解决这一挑战，许多研究工作提出资源划分技术，其通过在为目标应用构筑资源敏感模型的基础上对共享资源（例如，末级缓存）实施按需划分，从而在多类应用混合部署环境下为目标应用提供资源隔离，带来性能保证。但是，已提出的资源划分技术是基于核间共享资源，而在同步多线程场景下，如何对核内共享资源进行划分依旧是一个颇具挑战的开放问题。在本文中，首先通过在真实系统下对同时多线程应用进行性能干扰点分析，发现对于两个同步多线程应用，对 SMT 干扰敏感的核内资源主要为指令队列、保留站、存储队列，而分支预测器等对 SMT 干扰不敏感。在此基础上，本文提出一种核内资源可编程机制，使得核内资源可根据应用需求由使用者通过资源需求语义标签进行分配；提供一套基于采样的资源监控回收机制，在低开销的成本下实现资源有效利用，避免资源分配不均。其结果表明，该方法未对系统性能带来严重的影响，只使用有限的资源即可为硬件增加更为灵活的可编程能力，在提高资源利用率的同时保障了同时多线程场景下目标应用的 QoS 需求。

18. 一种面向 FPGA 异构计算的高效能 KV 加速器

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中科院计算所

摘要：网络功能虚拟化等新兴应用的蓬勃发展对 Key-Value 查询的能效提出了更高要求。传统的解决方法要么采用基于软件 Hash 表，要么采用专用的三态内容可寻址存储器（TCAM）

芯片进行加速。其中，软件方法实现成本低，但是在数据冲突较高时会导致查表性能急速下降；硬件 TCAM 方法具有优良的时间特性，但其价格昂贵、耗能巨大。目前，随着基于现场可编程门阵列 FPGA 的异构计算技术的高速发展，利用系统已经提供的 FPGA 资源对基于软件实现的 Hash 表结构进行加速成为一种性价比更佳的解决方案。探讨如何利用 FPGA 上的 RAM 资源来实现一种具有高扩展性和高能效比的 TCAM 逻辑。与传统的 TCAM 结构不同，提出的架构支持查表范围的动态缩放，从而可以有效减少查表功耗!为了验证方案的有效性，利用 Virtex-7 系列 FPGA 对本文方案进行实现和评估，并与软件查表的性能进行详细比较。实验表明，本文方案吞吐量可达到 234Mpps，查表延迟为 25.56ns。相比软件的方法，吞吐量提高 780 倍，延迟降低 240 倍。

19. 及时局部组和一种支持渗透计算的缓存模型

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Beijing Jiaotong University, Chinese Academy of Science

摘要：良好的数据及时局部性环境保证了处理器能够迅捷获取其所需要的数据。为了营造数据及时局部性环境，学术界、工业界提出了渗透计算的思想。一些研究结果已经表明片上存储层次中形成的数据及时局部性对于多核乃至高通量处理器的性能提升至关重要。为了进一步挖掘片上存储层次中的数据及时局部性，我们提出了及时局部组的概念，明确定义了何为渗透数据以及何为非渗透数据，为渗透计算的开展提供了理论依据。其次，我们提出了以泉吸和泉涌为主要构件的渗透缓存组成原理以及相应的以冷渗透和热渗透为主要手段的渗透数据迁移策略，为渗透计算的开展提供了物质基础。此外，我们采用 Verilog 语言和 ModelSim 仿真工具搭建了一个踪迹驱动的模拟仿真平台，通过注入 WordCount、Cholesky 等测试用例的访存地址序列，可以得到缓存命中率等性能输出结果。我们对渗透缓存和传统缓存进行了大量的对比实验，结果表明，我们提出的渗透缓存以及渗透数据迁移策略能够有效提高缓存命中率。

20. Fork Path: Improving Efficiency of ORAM by Removing Redundant Memory Accesses

Xian Zhang, Guangyu Sun, Chao Zhang, Weiqi Zhang, Yun Liang, Tao Wang, Yiran Chen and Jia Di
Peking University

Abstract: Oblivious RAM (ORAM) is a cryptographic primitive that can prevent information leakage in the access trace to untrusted external memory. It has become an important component in modern secure processors. However, the major obstacle of adopting an ORAM design is the significantly induced overhead in memory accesses. Recently, Path ORAM has attracted attentions from researchers because of its simplicity in algorithms and efficiency in reducing memory access overhead. However, we observe that there exist a lot of redundant memory accesses during the process of ORAM requests. Moreover, we further argue that these redundant memory accesses can be removed without harming security of ORAM. Based on this observation, we propose a novel Fork Path ORAM scheme. By leveraging three optimization techniques, namely, path merging, ORAM request scheduling, and merging-aware caching, Fork

Path ORAM can efficiently remove these redundant memory accesses. Based on this scheme, a detailed ORAM controller architecture is proposed and comprehensive experiments are performed. Compared to traditional Path ORAM approaches, our Fork Path ORAM can reduce overall performance overhead and power consumption of memory system by 58% and 38%, respectively, with negligible design overhead.

21. Programmable Two-Particle Bosonic-Fermionic Quantum Simulation System

Yang Wang, Junjie Wu, Yuhua Tang, Huiquan Wang, Dongyang Wang
National University of Defense Technology

Quantum computing promises to outperform its classical counterpart substantially. In the past decades, there has been tremendous progress. However, few previous researches have involved programmable systems. Quantum computing is mainly implemented in physics laboratories. This paper proposes a programmable structure. Using the entangled states of photon pairs, we have constructed the whole programmable system including a classical host, constructed with computer and circuits, and a quantum “coprocessor”, used for two-particle quantum simulations. A quantum “program” with both classical statements and quantum statements is executed for a certain computation task. The experiment shows high similarity of 95.2% to theoretical result in boson simulation and 97.1% in fermion simulation, which demonstrates the feasibility of our programmable system.

22. An Introduction to All-optical Quantum Controlled-NOT Gates

Hongjuan He, Junjie Wu and Xuan Zhu
National University of Defense Technology

Quantum computer promises to outperform classical computer fundamentally, due to its quantum superposition. Any operations to N qubits can be decomposed into several single-qubit operations and two-qubit controlled-NOT (CNOT) operations in theory. Linear optical quantum computing (LOQC) is one of the most prominent physical quantum systems, which has the advantage of long coherent time and convenience in implementing single qubit operations. However, the realization of two-qubit CNOT gate is the greatest challenge for LOQC, because two photons cannot directly interact with each other by nature. KLM protocol proves the feasibility of LOQC and spurs quantity of research on schematic design and experimental demonstration of CNOT gates by using linear quantum optics system. These researches are very important and nontrivial for LOQC, and this paper gives an overview of different schemes of the proposed CNOT gates and the experimental demonstration.

23. Computing Permanents for Boson Sampling on Tianhe-2 Supercomputer

Junjie Wu, Liu Yong, Baida Zhang, Xianmin Jin and Xuejun Yang
National University of Defense Technology

Abstract: Boson sampling [1], a specific quantum computation problem, is widely regarded to be one of the most achievable fields in which quantum machine will outperform the most powerful classical computer in the near term, although up to now no upper-bound of how fast the classical computers can compute matrix permanents, the core problem of Boson sampling, has been reported. Here we test the computing of the matrix permanent on Tianhe-2 [2], a supercomputer retaining its position as the world's No. 1 system for six times since June 2013. We arrived at the time (about 77.41~112.44 minutes) to compute the permanent of a 50×50 matrix in an acceptable precision. In addition, we have found that Ryser's algorithm will produce an unacceptable error with the increase of problem scale, compared to Balasubramanian-Bax/Franklin-Glynn's algorithm in the same complexity. The precision issue suggests carefully check in future research of Boson sampling, and comprehensive comparison between quantum computer and classical computer. More details: arXiv1606.05836. [1] Aaronson, S. and Arkhipov, A. The computational complexity of linear optics. In Proceedings of the Forty-third Annual ACM Symposium on Theory of Computing, STOC '11, 333-342 (ACM, New York, NY, USA, 2011). [2] Liao, X et al., MilkyWay-2 supercomputer: system and application. Front. Comput. Sci. 8(3), 345-356, June (2014).

24. 基于量子漫步概率幅调控的算法设计与优化

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国防科学技术大学

摘要：量子漫步是经典随机漫步的量子化版本，是具有量子特性的粒子在一定空间内游走的物理过程。研究表明，量子漫步的许多非经典特性能够对计算过程产生加速效果，因此，量子漫步已被作为构建量子算法的重要计算模型。2010 年，英国布里斯托大学展示了在光波导芯片上有效地执行量子漫步基本操作（Science 329, 1500 (2010)），使得量子漫步模型在物理实现上也展示出了其特有优势。但由于量子漫步模型与人们熟知的以门操作为基础的计算模型之间存在较大的差异，且量子特性常常违背人们的常规思维，所以如何基于量子漫步模型构建量子算法一直缺乏有效的方法论指导。当前基于量子漫步模型的算法针对的应用领域不多，且这些算法的设计方法基本上属于“从量子漫步过程的特殊物理性质过渡到对应的特定问题的解”这样一种自下而上的方法，这样的方法使得算法的设计极大地依赖于对量子漫步物理性质的研究。本海报展示了我们对基于量子漫步模型进行量子算法设计与优化的一系列研究。首先介绍了一种从计算模型出发的自上而下的量子算法设计与优化方法，然后使用该方法对当前基于量子漫步模型的两个主要应用进行了显著优化，以及对量子漫步算法在量子计算中的应用进行了拓展。

25. RLDRPSO: An Efficient Heuristic Algorithm for Task Partitioning

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Abstract: Task partitioning is the critical step in the co-design of reconfigurable embedded system. Particle Swarm Optimization (PSO) has been used for fast task partitioning. However, PSO has the problems of local extremum and low precision, leading to the poor partitioning quality and unsatisfied performance. In this paper, Reverse Learning Dynamic Radius Particle Swarm Optimization (RLDRPSO) task partitioning algorithm was proposed to solve these problems. Firstly, the fitness function was designed according to the system model. Then, DRPSO was proposed to extend the solution space and improve the accuracy. Finally, reverse learning strategy was proposed to degenerate solution periodically and solve the problem of local extremum. Experimental results show that RLDRPSO increases the partitioning quality by 20%~45% and the average performance of system by 7%~9%.

26. A Fine-Granular Programming Scheme for Irregular Scientific Applications

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Abstract: HPC systems are widely used for accelerating calculation-intensive irregular applications, e.g., molecular dynamics (MD) simulations, astrophysics applications, and irregular grid applications. As the scalability and complexity of current HPC systems keeps growing, it is difficult to parallelize these applications in an efficient fashion due to irregular communication patterns, load imbalance issues, dynamic characteristics, and many more. This paper presents a fine granular programming scheme, on which programmers are able to implement parallel scientific applications in a fine granular and SPMD (single program multiple data) fashion. Different from current programming models starting from the global data structure, this programming scheme provides a high-level and object-oriented programming interface that supports writing applications by focusing on the finest granular elements and their interactions. Its implementation framework takes care of the implementation details e.g., the data partition, automatic EP aggregation, memory management, and data communication. The experimental results on SuperMUC show that the OOP implementations of multi-body and irregular applications have little overhead compared to the manual implementations using C++ with OpenMP or MPI. However, it improves the programming productivity in terms of the source code size, the coding method, and the implementation difficulty.

27. Research on Virtual Machine cluster Deployment Algorithm in Cloud Computing Platform

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HuNan normal University

Abstract: To address the virtual machine cluster deployment issues in cloud computing environment, a novel MCSA (Min-cut segmentation algorithm) of virtual machine cluster is

proposed with resource and communication bandwidth constraints. In this paper, the basic idea is based on the fully consideration on the CPU, memory, hard-disk and other resource constraints between virtual machine cluster and physical host, as well as the communication bandwidth constraints between the virtual machine. We quantified the virtual machine cluster constructed an undirected graph. In the undirected graph, the nodes represent the virtual machine, so the weight of a node represents the value of resources, and the edges represent the communication bandwidth, so the weight of the edge represents the value of communication bandwidth. Base on the above transformations, the resources and bandwidth constrained optimization problem is transformed into the graph segmentation problem. Next we segment the undirected graph by minimum cut algorithm, and computing the matching degree of physical machines. Last we obtained the approximate solution. To validate the effectiveness of the new algorithm, we carried out extensive experiments based on the CloudSim platform.

28. An OS-level Data Distribution method in DRAM-PCM Hybrid Memory

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Abstract: Hybrid memory composed of DRAM and PCM has gained substantial research recently. Compared to each other, DRAM has lower read/write latency and higher endurance, and Phase Change Memory (PCM) has higher density and consumes less energy. Hybrid memory has been proposed to exploit the benefits of both these technologies, while at the same time mitigating their disadvantages. The data distribution methods of state of art approaches were managed by either hardware or compiler, which had some shortcomings. The disadvantage of hardware based approaches is that it need large storage, and the required data swapping degrades overall performance, which is not suitable for certain program which has poor locality. While the compiler based technique requires dynamic program analysis, thus increasing run time overhead and also requires programmer's help, thus making it a cumbersome approach. We present an OS-level Data Distribution(OSDD) method, in which data sections that have respective read/write features in virtual address space were assigned to different memory medium by memory management module of operating system. Since our approach needs no input from programmer, thus making it transparent. The OSDD based hybrid memory put appropriate data to corresponding memory medium at system level in page granularity and gained better performance and energy saving than former methods, with less overhead. The experiment showed that on average our method get 52% energy saving at 6% performance overhead than uniform DRAM memory.

29. 基于关键列分组排序的列存储结构

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清华大学

摘要：磁盘作为海量数据的主要存储介质，具有容量大、成本低的优点，但是磁盘 IO 带宽

远远落后于数据增长速度，日益成为大数据管理系统的性能瓶颈。因此，优化存储结构，提高读写效率是大数据时代管理系统面临的重要挑战。提出了一种基于关键列分组排序的混合列存储结构 KCGS-Store，根据关键列分组将关系表划分为存储池，确保池内所有记录在关键列上的取值或取值范围相同，然后逐列进行池合并#合并后的关键列，以池为单位有序排列，执行条件查询时能够有效过滤无关列值，减少数据读取量，提升查询性能。同时利用池号索引，以少量时间空间代价完成记录重组。实验数据表明，与 ORCFile、Parquet 存储结构相比，KCGS-Store 在存储空间、数据加载、SQL 查询等方面都有不同程度的优化。

30. 利用多维分级 Cache 替换策略减少对 PCM 内存写回量

阮深沉，王海霞，汪东升
清华大学

摘要：寻找新型存储材料代替 DRAM 内存是当前的一个研究热点。相变存储 PCM 因其具有低功耗、高存储密度和非易失性的优点受到广泛的关注，然而 PCM 的可擦写次数有限，要用作内存必须考虑如何减少对其的写操作。针对该问题，一种有效的解决方法是优化 Cache 替换策略，减少 Cache 中脏块被替换出的数量。现有研究主要通过在插入和访问命中时给脏块设定较高的保护优先级来达到给脏块额外保护的目的，但是在降级过程中不再对脏块与干净块进行区分，这导致 Cache 可能在存在大量干净块的情况下仍然先替换脏块。提出一种新型的 Cache 替换策略 MAC，它通过一个多维分级结构在脏块与干净块之间设置了不可逾越的界限，使得脏块能得到更有力的保护。模拟实验表明，相对 LRU 替换策略，MAC 以较低的硬件开销代价平均减少约 25.12%的内存写，同时对程序运行性能基于没有影响。

31. Subway timetable adjusting method research of bi-directional trains arriving at a station asynchronously

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Abstract: Metro transmits, as the backbone of urban public transit, plays an important role in alleviating congested traffic and shaping low-carbon and comfortable trip mode. With the rapid development of urban rail transit, the traffic of the city cannot be separated from the subway; however, large passenger flow triggers heavy traffic accident easily and reduces the degree of comfort greatly, especially when up and down trains arriving at the same station simultaneously. To implement urban railway transit system optimization and to achieve the goal of up and down trains arrive at a station asynchronously, situations of trains arriving at the platform are studied, and a quantitative analysis of different time periods and different types of platforms are completed. The definition of the train conflict time of arriving at a station simultaneously is given. Through the derivation and calculation of the total use of the subway conflict time, to identify the key variables that affect the conflict time, a solution of using greedy algorithm to adjust conflict time is proposed. Simulation through Visual C++ platform demonstrates that the algorithm can provide optimal railway timetables while satisfying operational constraints.

Comparative analysis of the results showed that: if passenger flow is considered, departure time, interval time and dwell time are invariant, only adjusting the morning peak-hours is 19.76% superior than the unadjusted state, while adjusting the morning and evening peak-hours is 34.85% prior. The models can be further expanded to develop models and algorithms for estimating the conflict time of up and down trains and reduce the conflict time.

32. Performance Analysis of Sliding Window Network Coding in MANET

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Abstract: Network coding (NC) enables us to mix two or more packets into a single coded packet at relay nodes and improve performances in mobile ad hoc networks (MANETs). Sliding window network coding is a variation of NC that is an addition to data packet streaming and improves the data delay on MANETs. In this paper, we propose a Sliding Window Network Coding in MANETs (SWNCM). SWNCM preserves the degree distribution of the encoded data packets through the recombination at the nodes. SWNCM enables to control the decoding complexity of each sliding window independently from the data packets received and recover the original data. The performance of the SWNCM is studied using NS2 and evaluated in terms of the network throughput, encoding overhead, decoding delay, packet transmission rate when data packet is transmitted. The simulations result shows that the SWNCM with our proposition can significantly improve the network throughput and achieves higher diversity order.

33. 一种基于最小二乘优化的快速压缩感知算法

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摘要：压缩感知方法可以以远低于传统采样定理规定的采样率对信号采样。针对压缩感知重构信号的时间较长且随信号增大以极高速率快速增长的问题，提出了面向图像信号的快速压缩感知算法 FBWRFI。FBWRFI 基于最小二乘方法实现信号的优化重构，利用新定义的整体相关性度量参数选择针对图像信号的最相关原子，引入分块重构理论并重新设计分块大小和测量矩阵，有效降低了重构操作的计算复杂度和计算规模!实验结果表明 FBWRFI 算法可以显著降低信号的重构时间，并使随信号增大而高速增长的重构时间的增长趋势变为线性，证明了算法的有效性

34. 嵌入式系统可信虚拟化技术的研究与应用

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摘要：嵌入式系统在生活中的应用日益广泛，传统的安全增强手段已无法有效应对各种安全问题，增强嵌入式系统的安全性成为目前亟需解决的问题。为提高嵌入式系统及其应用程序的安全性，结合嵌入式系统的虚拟化技术与可信计算技术，设计并实现基于虚拟 TCM 的可信计算平台框架，实现了虚拟 TCM 和基于虚拟 TCM 的可信增强技术，提出并实现了一个基于虚拟 TCM 的会话认证方法，将信任链从硬件操作系统层扩展到了虚拟域的应用软件层。实验结果表明，虚拟 TCM 与物理 TCM 相结合能够有效保证嵌入式系统、虚拟域和应用程序的安全可信。

35. 一种基于 Spark 在线 Web 服务的高效低延迟调度资源算法

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摘要：Spark 作为流行的分布式数据处理框架，其资源的调度方式和资源的利用率直接关系到集群计算处理的效率和速度。针对 Spark 资源调度问题，在 Spark 自身考虑的资源因素内存和空余核数下，提出新的调度算法。算法通过实时监视工作节点资源利用情况，增加对节点 CPU 处理速度和 CPU 剩余利用率的考虑，重新调度与分配资源，为 Spark 作 Web 服务高并发请求、低延迟响应提供优化，还可以减少传统方式没有考虑的资源因素导致出现的资源利用倾斜现象，提高资源的利用率。实验表明，改进的资源调度算法有较好的效果。

36. 云环境中基于分解的多目标工作流调度算法

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摘要：云服务提供商在给用户提供海量虚拟资源的同时，也面临着一个现实的问题，即怎样调度这些资源，以最小的代价（完工时间、执行费用、资源利用率等）完成工作流的执行、针对 IaaS 环境下的工作流调度问题，以完工时间和执行费用作为目标，提出了一种基于分解的多目标工作流调度算法。该算法结合了基于列表的启发式算法和多目标进化算法的选择过程，采用一种分解方法，将多目标优化问题分解为一组单目标优化子问题，然后同时求解这些单目标子问题，使得调度过程更为简单有效。算法利用天马项目发布的现实世界中的工作流进行实验，结果表明，和 MOHEFT 算法以及 NSGA-II*算法相比较，所提出的算法能得到更优的 Pareto 解集，同时具有更低的时间复杂度。

37. 基于动态松弛时间回收的开销敏感节能实时调度算法

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摘要：为适应实际系统中任务集的不断变化以及不可忽视状态切换开销的要求，针对多核多处理器系统中常见的周期任务模型，提出一种基于动态松弛时间回收的开销敏感节能实时调

度算法 DSROM 在每个 TL 面的初始时刻，任务提前完成时刻实现节能调度及动态松弛时间回收，在不违反周期任务集可调度性的基础上，达到实时约束与能耗节余之间的合理折衷。模拟实验结果表明 DSROM 算法不仅保证了周期任务集的最优可调度性，而且当任务集总负载超过某一个值后，其节能效果整体优于现有方法，最多可节能近 20%。

38. 面向嵌入式穿戴医疗的快速经验模态分解方法

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摘要：智能照护系统通过人体感知智慧衣实时采集心电(ECG)等生理数据，却不可避免地混入运动伪影造成信号失去形态学特征。经验模态分解算法(EMD)通过获得本征函数分量去除非静态、非线性信号，去除 ECG 信号中的运动伪影。但是，传统 EMD 算法计算量大，不适用于低功耗的嵌入式移动设备。提出一种 Fast-EMD 算法，通过采用不同的运动状态来控制相应迭代次数的方式取代计算复杂边界值 SD。实验结果表明，该方法既简化了算法执行流程，又提高了 R 点捕获准确率，有效提升了嵌入式设备上滤波处理性能。

39. Android 智能电视测试用例生成方法及应用研究

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摘要：相比传统电视，由于增加上网浏览、音视频文件播放、下载各种应用软件等多种功能，智能电视系统软硬件变得异常复杂，用户使用相对繁琐，这种大批量消费类产品的可靠性是目前智能电视厂家面临的主要问题。提出根据系统设计规格书对智能电视的操作行为采用 AutoStar 进行层次化状态迁移矩阵（STM）建模，进而转化为具有记忆功能的正则表达式，同时根据正则表达式圈复杂度来递归确定正则表达式中包含所有闭包循环的次数，并生成测试用例，自动转成 Python 脚本，通过 Android 提供的 ADB 接口发送给 Android 智能电视，最后设计实现 Android 智能电视测试平台，该平台应用于国内智能电视的测试。

40. 一种面向三维众核微处理器的新型 NoC 拓扑结构

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摘要：三维微处理器具有集成度高、全局互连线短及连接部件多的优势，但是传统的三维拓扑结构在大规模系统中无法充分利用垂直方向上低延时高带宽的特性，很难满足大规模众核微处理器低直径、高带宽、高扩展性的需求。针对三维 NoC 网络直径大、可扩展性要求高以及路由端口多的问题，提出了一种基于多级垂直域的三维拓扑结构—V-Spidergon，其在水平层上采用 Spidergon 结构，在垂直方向上采用多级垂直域扩展结构，域内及域间均实现全互连#实验数据表明。在 8 层，16 层和 32 层堆叠下 V-Spidergon 结构的延时较 3D-Mesh 分别

降低 15.1%、28.5%和 55.7%，较 NoC-Bus 分别降低 11.5%、32.7%和 77.6%；在 15%和 100%负载率注入情形下, V-Spidergon 的平均延时表现出与水平层数增加不相关的特性。

41. 二元域大型稀疏矩阵向量乘的 FPGA 设计与实现

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摘要：作为 Wiedemannn 算法的核心部分，稀疏矩阵向量乘是求解二元域上大型稀疏线性方程组的主要步骤。提出了一种基于 FPGA 的二元域大型稀疏矩阵向量乘的环网硬件系统架构，为解决 Wiedemannn 算法重复计算稀疏矩阵向量乘，提出了新的并行计算结构。实验分析表明，提出的架构提高了 Wiedemannn 算法中稀疏矩阵向量乘的并行性，同时充分利用了 FPGA 的片内存储器和吉比特收发器，与目前性能最好的部分可重构计算 PR 模型相比，实现了 2.65 倍的加速性能。

42. “绑定中测试”“多绑一测”方式对于测试过程的影响

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摘要：随着半导体工艺水平的不断发展，3D 芯片技术已成为一大研究热点。“绑定中测试”环节的提出对于芯片的测试流程有了新的要求。但是，“绑定中测试”“一绑一测”的特点会使部分裸片被重复测试，从而带来测试时间的增加。从“绑定中测试”的过程出发，协同考虑测试功耗与“理论制造成本”对于“绑定中测试”的影响，提出“多绑一测”的测试流程。在此基础上提出相应的广度优先遍历算法，结合，ITC’02 电路的相关参数，体现本文思想在实际生产制造中的现实意义。

43. 云计算弹性评测模型的研究与实现

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摘要：当前，越来越多的企业开始将自己的核心业务与数据迁移到云上，其中很多业务需要相应的弹性服务来应对负载的实时变化，因此对弹性的评测正变得越来越重要，然而当前缺少一种较为全面的弹性评测方法。为解决以上问题，从资源分配、QoS、资源配置时间等多个角度，对云计算的弹性进行较为全面的分析，提出适用于供应商和用户两个角度的评测方法。在已有基础上，提出资源分配、资源配置时间两个方面的计算模型，并对现存的罚金模型进行改进。最后，在 CloudStark 云平台上，使用 auto-scaling 和 scale-out 两种弹性扩展策略，以 TPC-W 为负载验证了所提方法的有效性。

44. 基于加速收敛蜂群算法的资源感知调度器

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摘要：为了能有效处理海量数据，进行关联分析、商业预测等，Hadoop 分布式云计算平台应运而生。但随着 Hadoop 的广泛应用，其作业调度方面的不足也显现出来，现有的多种作业调度器存在参数设置复杂、启动时间长等缺陷。借助于人工蜂群算法的自组织性强、收敛速度快的优势，设计并实现了能实时检测 Hadoop 内部资源使用情况的资源感知调度器。相比于原有的作业调度器，该调度器具有参数设置少、启动速度快等优势。基准测试结果表明，该调度器在异构集群上，调度资源密集型作业比原有调度器快 10%~20%左右。

45. 一种基于种族分类进化的 QoS 异构组播路由机制

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摘要：随着新型网络应用的大量涌现，传统的网络技术已无法满足当前应用在带宽、延迟及出错率等方面的需求，IP over DWDM 光互联网以其独特性能优势成为研究热点。基于种族分类进化算法，提出了一种 IP over DWDM 光互联网服务质量 QoS 异构组播路由机制。具体地，利用概率论方法处理网络状态参数信息的不确定性；引入模糊数学方法，确定用户对 QoS 的需求并提供柔性 QoS 支持；综合考虑网络提供方和用户方的利益，设计公平的带宽定价方法。仿真结果表明，该路由机制获得了良好的综合性能指标，可以有效地解决 IP over DWDM 光互联网中的柔性 QoS 异构组播路由选择问题。