

H BHARATH BHAT

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hbharathbhat.github.io

Experience

Indian Institute of Science, Bengaluru

September 2024 - Ongoing

Research Intern

Hybrid

- Currently working under the guidance of **Prof. Sumit Kumar Mandal** on the Hardware Implementation of **Cussen's Algorithm** which involves **Matrix Multiplication using only Addition**. This technique uses Sorting and Addition over Multiplication, hence expected to reduce Execution Time and Area.

November 2023 - April 2024

Research Intern

Onsite

- Worked on **Energy-Efficient Hardware Accelerators for Machine Learning Algorithms** in the **Future Computing Systems (FIST)** group within the **Computer Science and Automation Department, IISc, Bengaluru**.
- My work also includes contributions to literature on **Communication-aware Heterogeneous 2.5D Systems for Energy-efficient LLM Execution at Edge** published at the IEEE Journal on Emerging and Selected Topics in Circuits and Systems
- Skills Enhanced:** Verilog · C · RTL Design · Python · Cadence
- <https://www.csa.iisc.ac.in/~skmandal/bharat.html>

Education

JSS Academy of Technical Education, Bengaluru

2021 - Present

Visvesvaraya Technological University (VTU)

Aggregate: 8.6 CGPA

Bachelor of Engineering in Electronics and Communication Engineering

Projects

Hardware Implementation of Minimally Biased Multipliers | Verilog

June 2024

- This project involves Hardware Implementation of **Minimally Biased Multipliers for Approximate Integer Multiplication** using **Verilog**.
- This project also involves synthesis of the algorithm using **tsmc90** technology library on **Cadence Genus Tool** to analyze area, power and speed.
- github.com/hbharathbhat/minimally_biased_multipliers.git

Tech Fusion Cruiser | Embedded C

January 2024

- This project was developed on **ARIES V3.0** Development Board as a part of Inter-branch workshop conducted at **JSS Academy of Technical Education, Bengaluru**.
- Won the 1st prize in the contest held post the workshop.
- github.com/hbharathbhat/cdac_vega_tech_fusion_cruiser.git

Hardware Implementation of Systolic Array | Verilog · RTL Design · Python

August 2023

- This project involves Hardware Implementation of **nxn Systolic Array integrated with Softmax Model** using **Verilog**, which was later synthesized using Cadence Design Tool.
- This project was developed during the internship period at Indian Institute of Science, Bengaluru.

Collection of RTL Codes | Verilog · RTL Design

June 2023

- This hobby project includes a collection of RTL codes, featuring components such as flip-flops, adders, latches, multiplexers, encoders, ALUs, counters, RAMs, ROMs, and more.
- github.com/hbharathbhat/rtl_codes.git

Technical Skills

Languages: Verilog · C · Python · HTML/CSS

Hardware Design & Synthesis: Xilinx Vivado/ISE · Cadence Genus · Cadence Design Tools

Software Development: VS Code · Git · Jupyter Notebook · Spyder · Code Blocks

Development Boards: Vega Processors: Aries V2.0 and V3.0 · Arduino UNO

Operating Systems: Linux(Ubuntu) · Windows

Technologies/Frameworks: Multisim · Tina-Ti · Cedar · Matlab · Arduino IDE

Major Courses

Introduction to Programming in C, IIT Kanpur
Hardware Modeling Using Verilog, IIT Kharagpur
Digital Design with Verilog, IIT Guwahati
Programming, Data Structures and Algorithms using Python, IIT Madras
C Programming Bootcamp, Udemy

Workshops

Present and Future Computing Systems, CSA, IISc, Bengaluru
Semiconductor Technology and Microfabrication, CeNSE Summer School, IISc, Bengaluru
Vega Processor and its Applications, JSSATE, Bengaluru

Extra Curricular

Carnatic Music

2017

Junior *Karnataka State Board*

- Has cleared Karnataka Music (Vocal) Junior Examination.

Trekking · Cycling