Name	Register address	Width	Access	Type	Default Value	Description
GLOBAL_MODULE (module address 0x00)						
GLOBAL_CONTROL	0x01	32	W	STAT	0x00	Not in use
GLOBAL_STATUS	0x02	32	R	STAT	0x00	Not in use
GLOBAL_WRITE	0x03	32	W	STAT	0x00	Writes data to every com_module in the system. [31] R/$\overline{W}$ bit towards PCU [30..24] Not in use [23..16] PCU reg address [12..0] Data to PCU
GLOBAL_RESET	0x05	32	W	CMD	0x00	Resets all modules except the global_module
COM_ENABLE_0	0x08	32	R/W	STAT	0xFFFFFFFF	These 32 bits enable com_modules[1→32] '1' = ENABLED Bit[n] controls com _module_[1 + n]
COM_ENABLE_1	0x09	32	R/W	STAT	0xFFFFFFFF	These 32 bits enable com_modules[33→64] '1' = ENABLED Bit[n] controls com _module_[33 + n]
SYSTEM CLOCK SPEED	0x06	32	R/W	STAT	0x1D905C0	The speed of the clock used by the com_modules. This is used to calculate the baud rate towards the PCUs. Default: 31Mhz (clock from IPbus)
PSU BAUD RATE	0x07	32	R/W	STAT	0x1C200	The baud rate to use towards the PCUs
COM_MODULE (module address 0x01 – 0x40)						
CONTROL	0x01	32	W	STAT	0x00	Not in use
STATUS	0x02	32	R	STAT	0x00	Not in use
WRITE	0x03	32	W	STAT	0x00	Writes data to the corresponding PCU. [31] R/$\overline{W}$ bit towards PCU [30..24] Not in use [23..16] PCU reg address [12..0] Data to PCU
READ	0x04	32	R	STAT	0x00	Reads a 32-bit vector from the corresponding PCU. [31] R/$\overline{W}$ bit towards PCU [30..24] Not in use [23..16] PCU reg address [12..0] Data to PCU
RESET_FIFO	0x05	32	W	CMD	0x00	Resets both TX and RX FIFO to clear them.
DUMMY_MODULE (module address 0x43)						
WRITE	0x03	32	W	STAT	0x00	Write anything to store a new value
READ	0x04	32	R	STAT	0xDEADBEEF	Read back the stored value