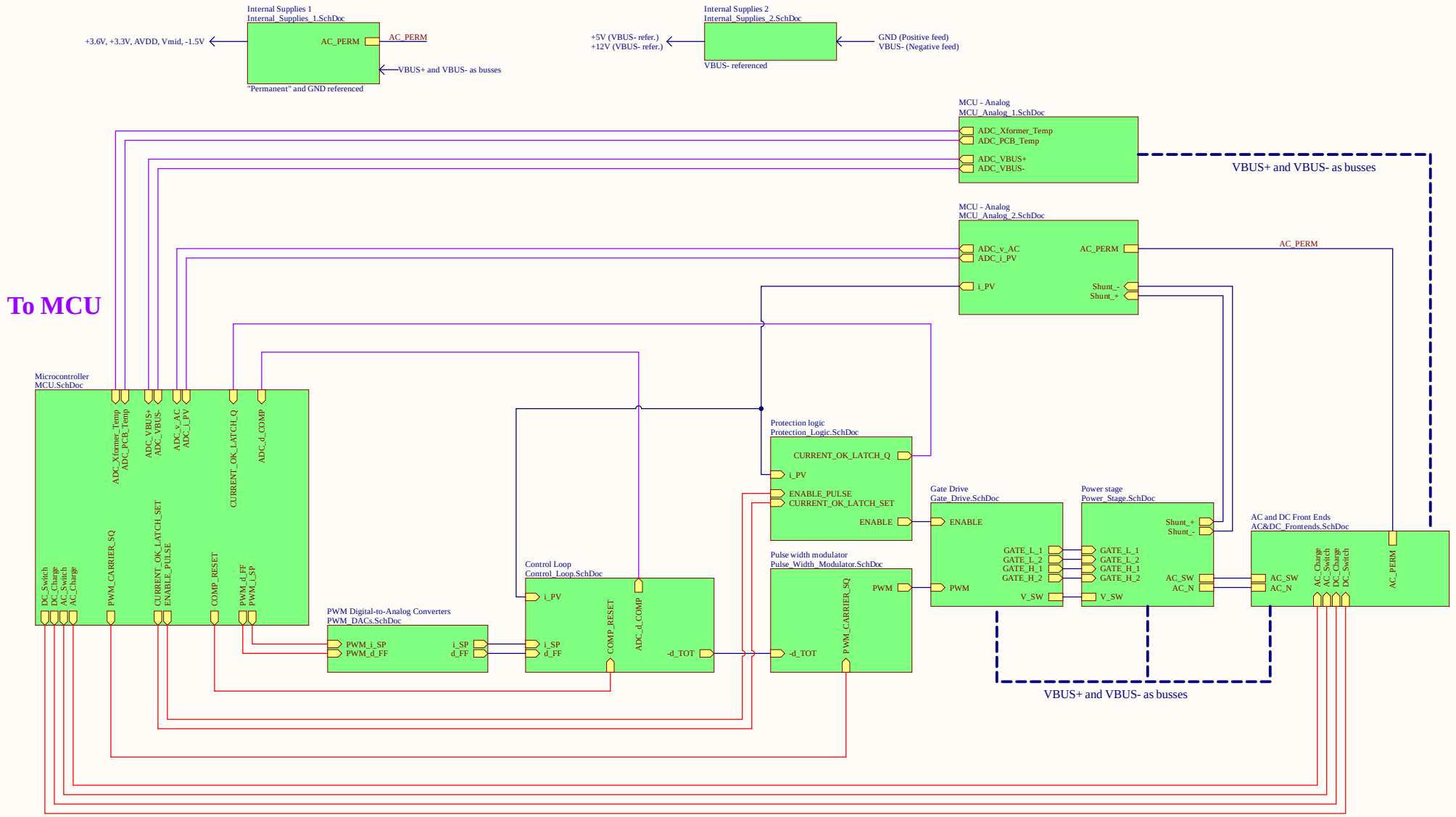
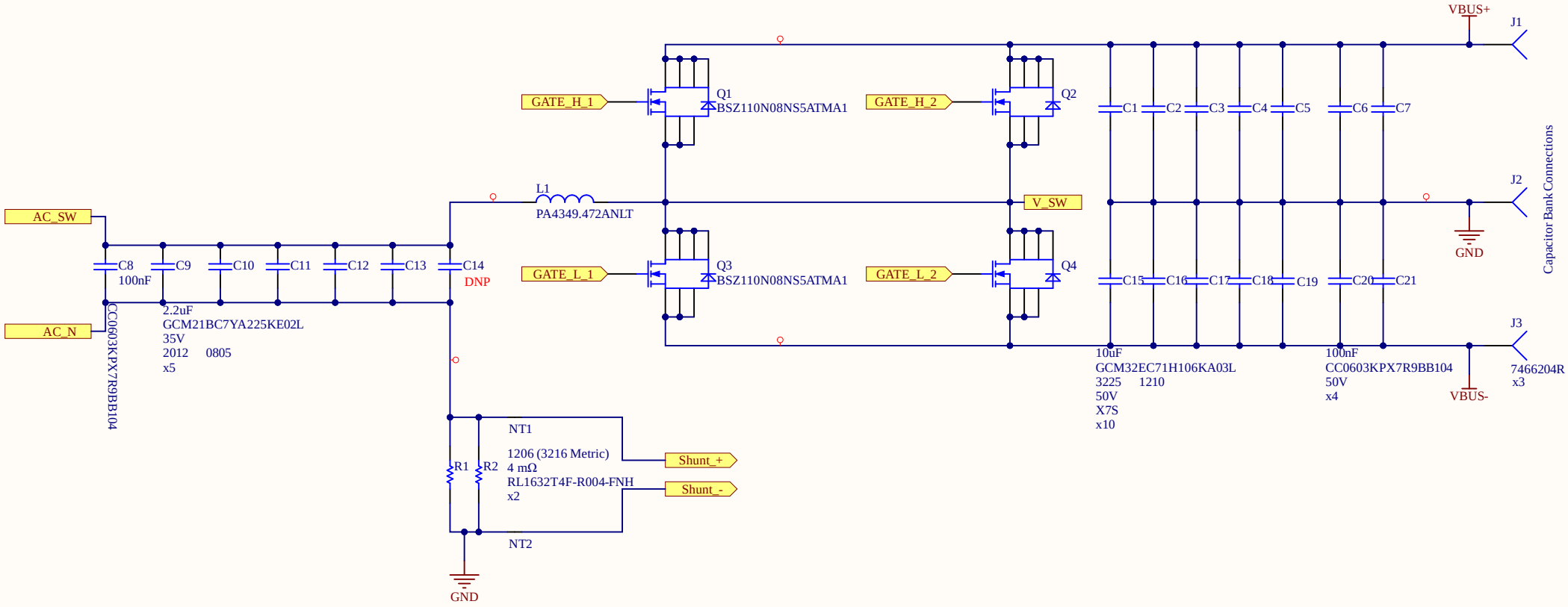


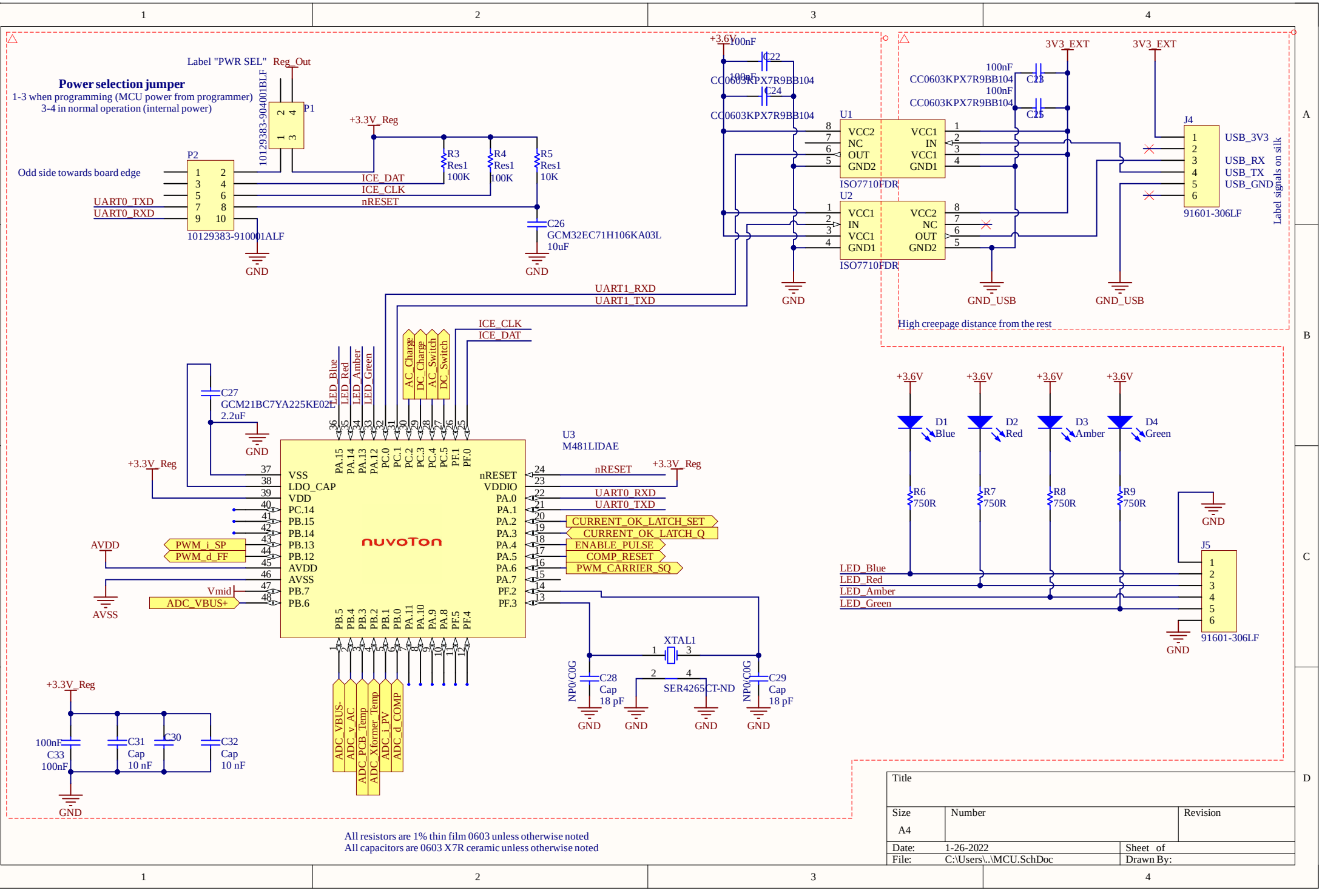
TODO: Make this more readable.

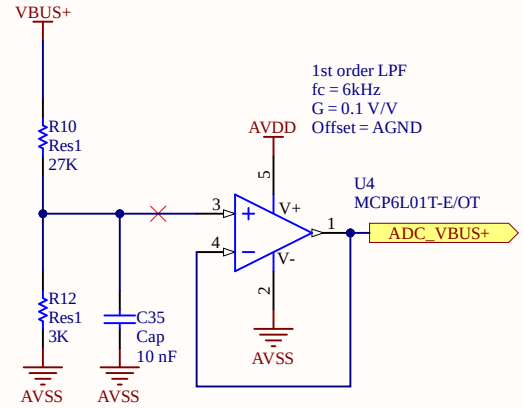
Title		
Size: Tabloid	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\Main_sheet_Top.SchDoc		Drawn By:

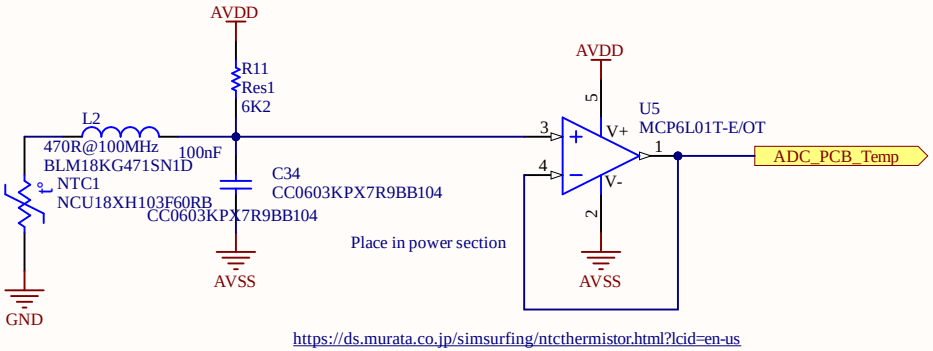


All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

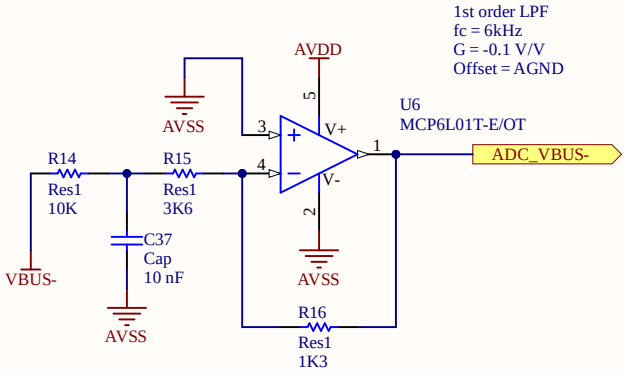
Title		
Size A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\Power_Stage.SchDoc		Drawn By:

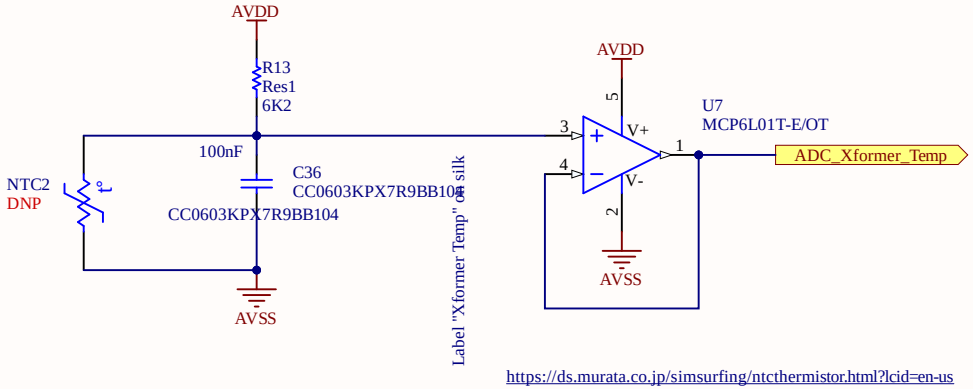

Power selection jumper
1-3 when programming (MCU power from programmer)
3-4 in normal operation (internal power)
Label "PWR SEL"
Reg_Out
10129383-904001BLF
P1
P2
Odd side towards board edge
10129383-910001ALF
+3.3V_Reg
R3 Res1 100K
R4 Res1 100K
R5 Res1 10K
ICE_DAT
ICE_CLK
nRESET
UART0_TXD
UART0_RXD
C26 GCM32EC71H106KA03L 10uF
GND
+3.6V
C22 100nF
C24 100nF
CC0603KPX7R9BB104
U1
ISO7710FDR
U2
ISO7710FDR
3V3_EXT
C23 100nF
C25 100nF
J4
91601-306LF
USB_3V3
USB_RX
USB_TX
USB_GND
Label signals on silk
GND_USB
High creepage distance from the rest
UART1_RXD
UART1_TXD
C27 GCM21BC7YA225KE02L 2.2uF
LED_Blue
LED_Red
LED_Amber
LED_Green
AC_Charge
DC_Charge
AC_Switch
DC_Switch
U3
M481LIDAE
nuvoTon
VSS
LDO_CAP
VDD
PC.14
PB.15
PB.14
PB.13
PB.12
AVDD
AVSS
PB.7
PB.6
nRESET
VDDIO
PA.0
PA.1
PA.2
PA.3
PA.4
PA.5
PA.6
PA.7
PF.2
PF.3
PWM_i_SP
PWM_d_FF
Vmid
ADC_VBUS+
CURRENT_OK_LATCH_SET
CURRENT_OK_LATCH_Q
ENABLE_PULSE
COMP_RESET
PWM_CARRIER_SQ
XTAL1
SER4265CT-ND
C28 Cap 18 pF
C29 Cap 18 pF
NP0/C0G
D1 Blue
D2 Red
D3 Amber
D4 Green
R6 750R
R7 750R
R8 750R
R9 750R
J5
91601-306LF
C33 100nF
C31 Cap 10 nF
C30
C32 Cap 10 nF
ADC_VBUS-
ADC_v_AC
ADC_PCB_Temp
ADC_Xformer_Temp
ADC_i_PV
ADC_d_COMP
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size A4
Number
Revision
Date: 1-26-2022
Sheet of
File: C:\Users\..\MCU.SchDoc
Drawn By:



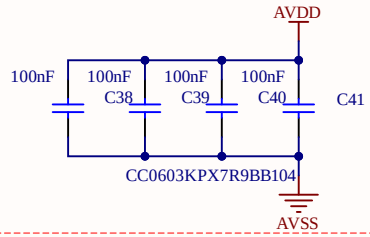


https://ds.murata.co.jp/simsurfing/ntcthermistor.html?lcid=en-us



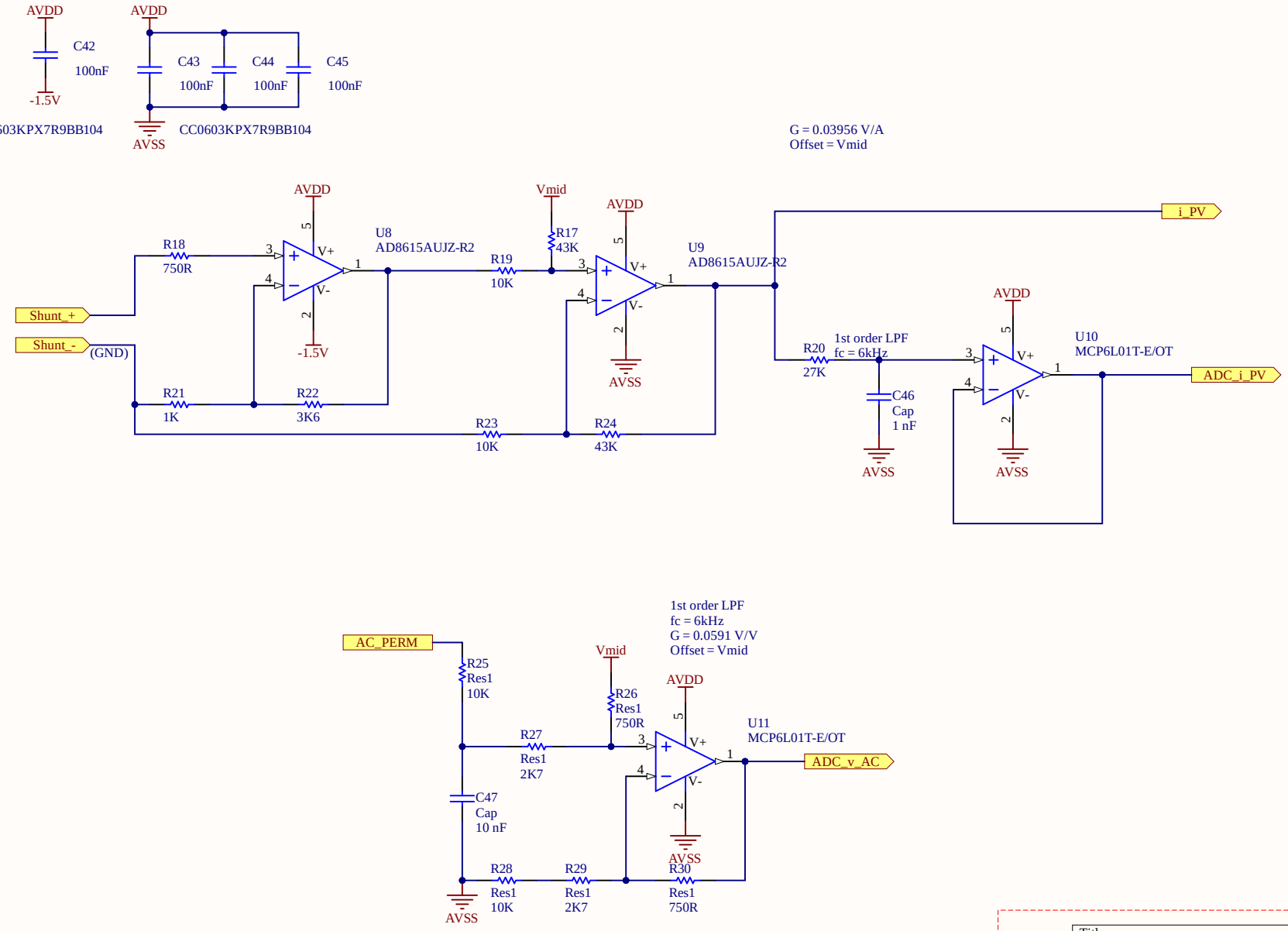


https://ds.murata.co.jp/simsurfing/ntcthermistor.html?lcid=en-us



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

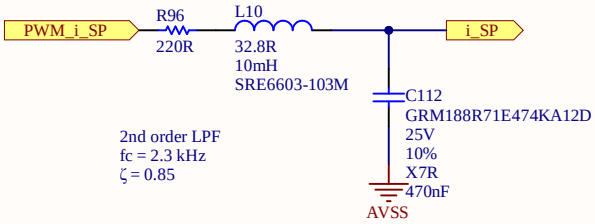
Title		
Size A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\MCU_Analog_1.SchDoc		Drawn By:



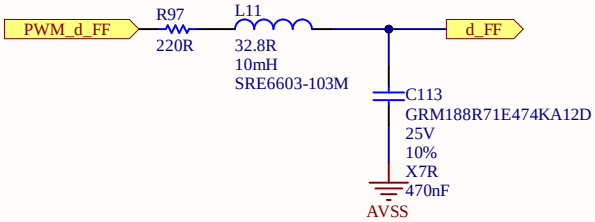
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

Title		
Size: A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\MCU_Analog_2.SchDoc		Drawn By:

11-bit PWM DAC
f_in = 93.7 kHz

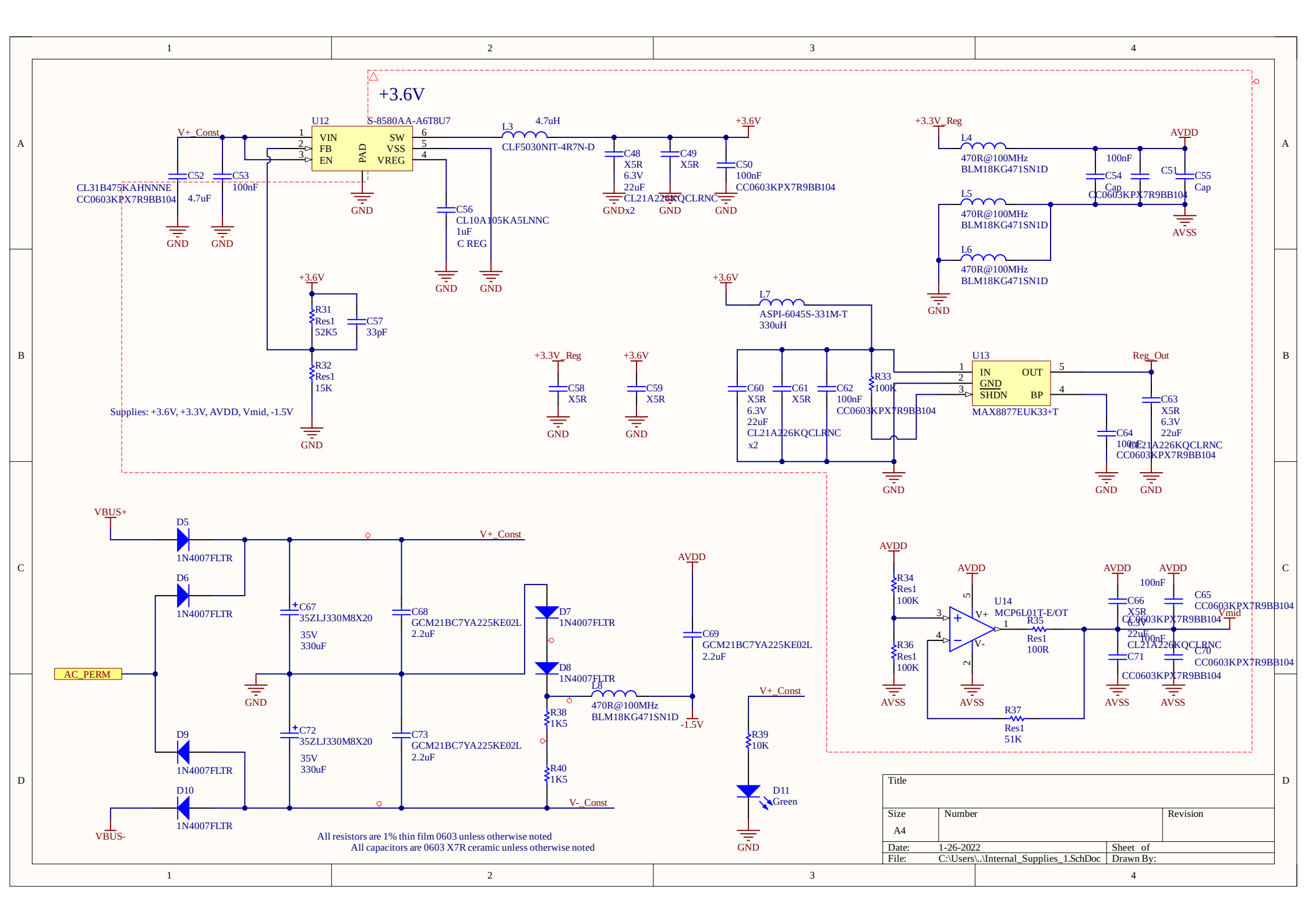


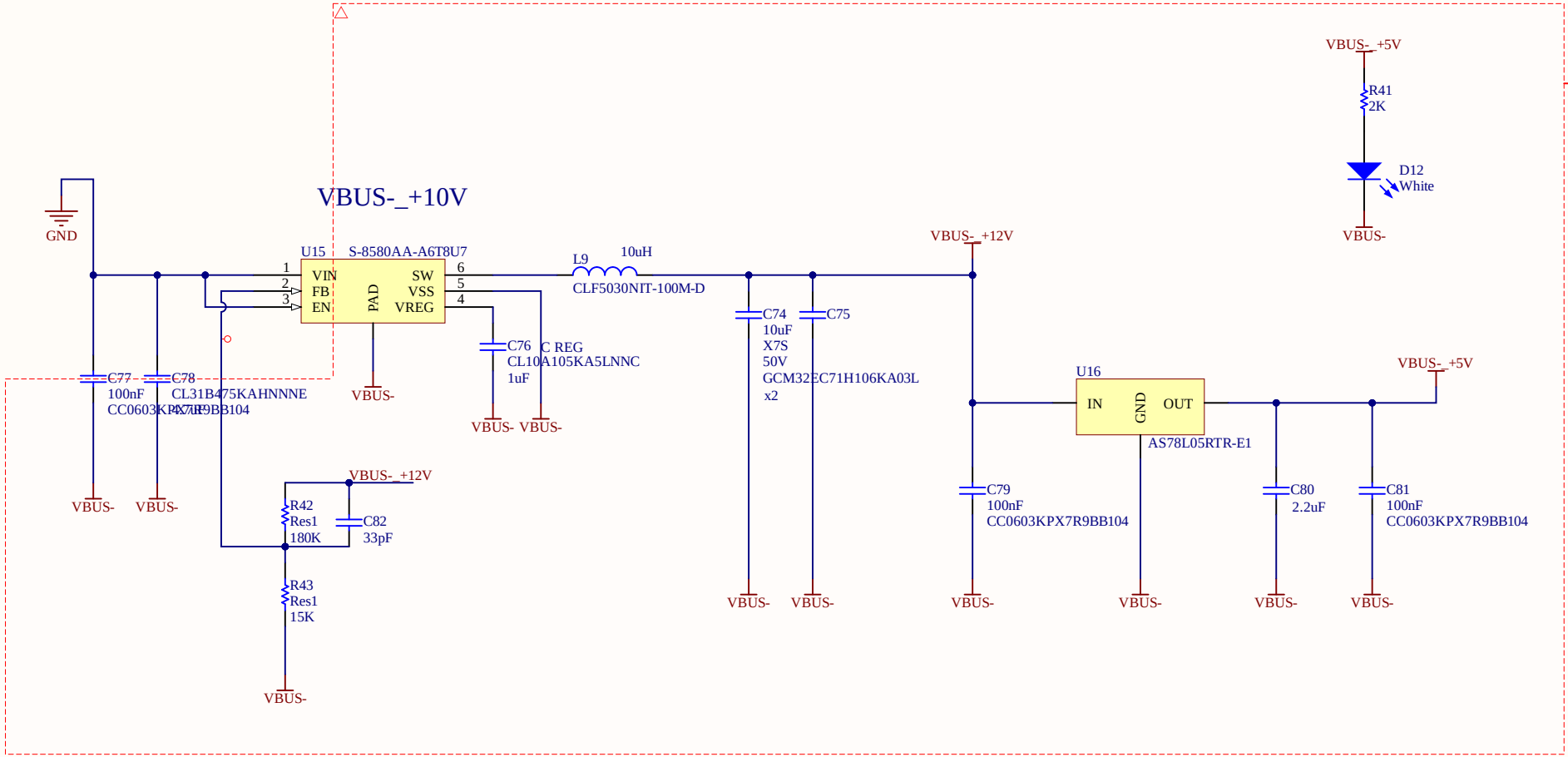
2nd order LPF
fc = 2.3 kHz
ζ = 0.85



This circuit is implemented because I could not get the DACs to work properly.
Obviously it is not necessary with correctly working DACs.

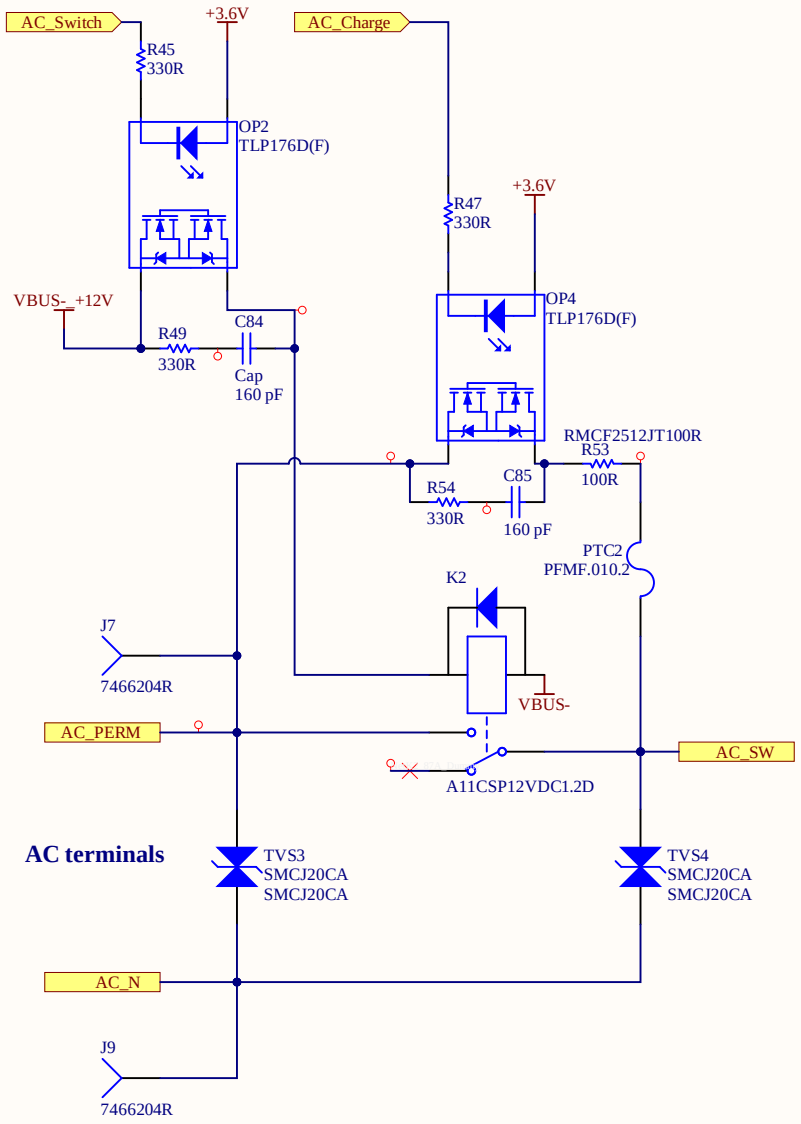
Title		
Size: A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\PWM_DACs.SchDoc		Drawn By:

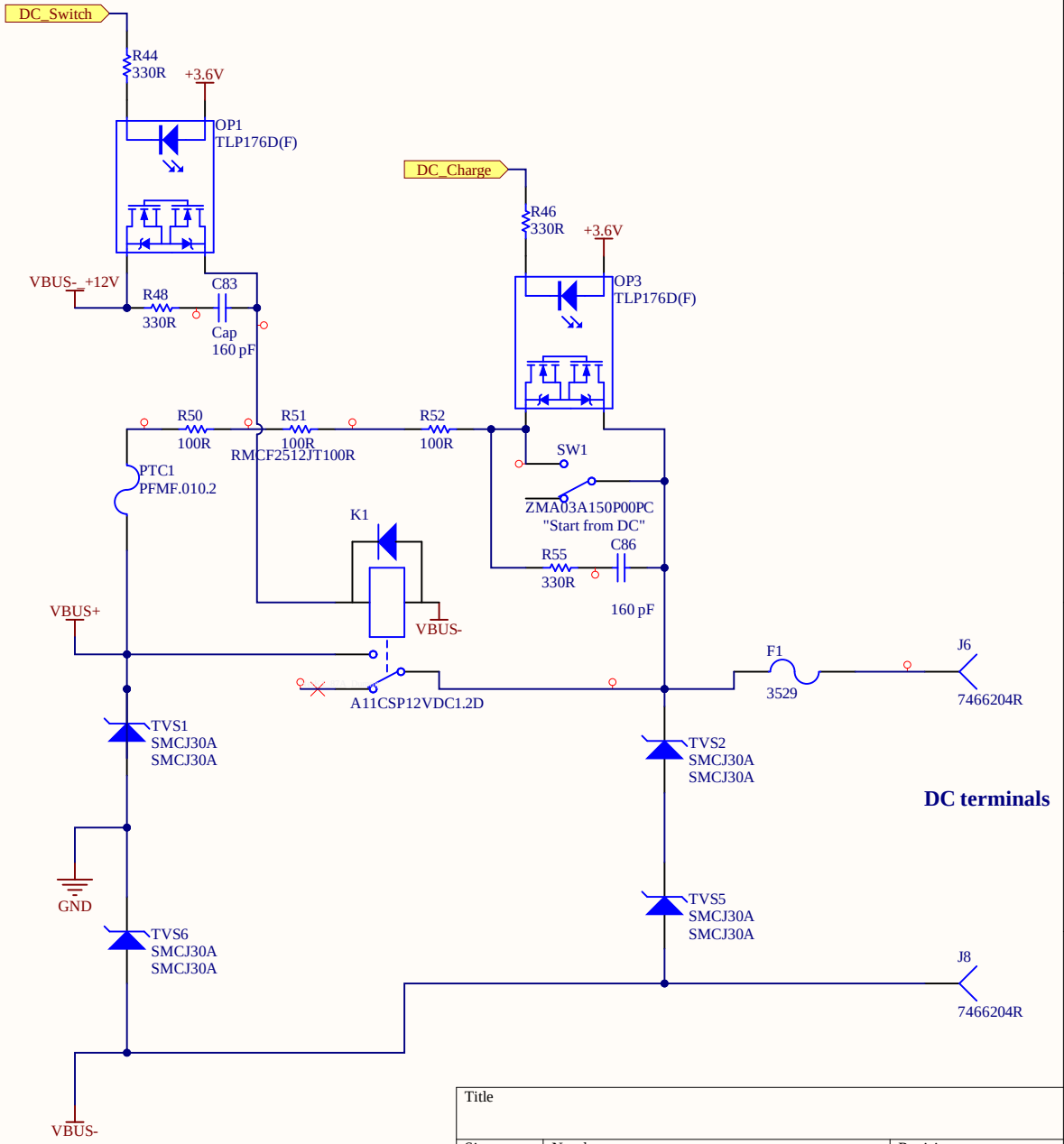

+3.6V
U12
S-8580AA-A6T8U7
VIN
FB
EN
SW
VSS
VREG
PAD
V+_Const
L3
4.7uH
CLF5030NIT-4R7N-D
C48
X5R
6.3V
22uF
CL21A226KQCLRNC
C49
X5R
C50
100nF
CC0603KPX7R9BB104
C52
4.7uF
CL31B475KAHNNNE
CC0603KPX7R9BB104
C53
100nF
C56
CL10A105KA5LNNC
1uF
C REG
GND
GNDx2
+3.3V_Reg
L4
470R@100MHz
BLM18KG471SN1D
L5
L6
C54
Cap
CC0603KPX7R9BB104
C51
C55
Cap
AVDD
AVSS
R31
Res1
52K5
C57
33pF
R32
Res1
15K
Supplies: +3.6V, +3.3V, AVDD, Vmid, -1.5V
L7
ASPI-6045S-331M-T
330uH
C58
X5R
C59
X5R
C60
X5R
6.3V
22uF
CL21A226KQCLRNC
x2
C61
X5R
C62
100nF
CC0603KPX7R9BB104
R33
100K
U13
IN
GND
SHDN
OUT
BP
MAX8877EUK33+T
Reg_Out
C63
X5R
6.3V
22uF
CL21A226KQCLRNC
C64
100nF
CC0603KPX7R9BB104
VBUS+
VBUS-
D5
D6
D9
D10
1N4007FLTR
AC_PERM
C67
35ZLJ330M8X20
35V
330uF
C68
GCM21BC7YA225KE02L
2.2uF
C72
C73
D7
D8
L8
470R@100MHz
BLM18KG471SN1D
C69
-1.5V
R38
1K5
R40
V-_Const
R39
10K
D11
Green
R34
Res1
100K
R36
U14
MCP6L01T-E/OT
V+
V-
R35
Res1
100R
R37
Res1
51K
C66
X5R
6.3V
22uF
CL21A226KQCLRNC
C65
C70
C71
Vmid
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size
A4
Number
Revision
Date:
1-26-2022
Sheet of
File:
C:\Users\..\Internal_Supplies_1.SchDoc
Drawn By:



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

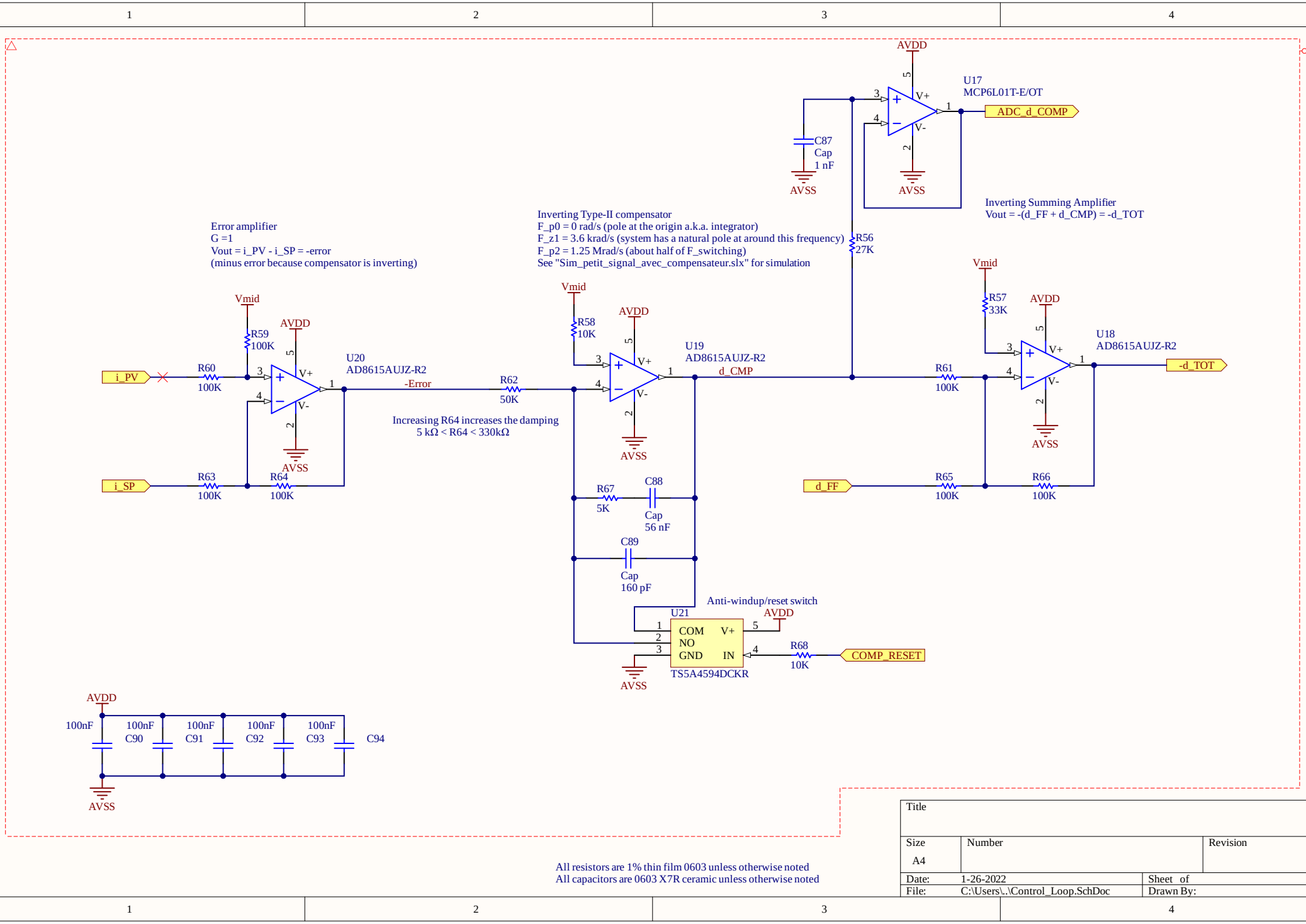
Title		
Size A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\Internal_Supplies_2.SchDoc		Drawn By:

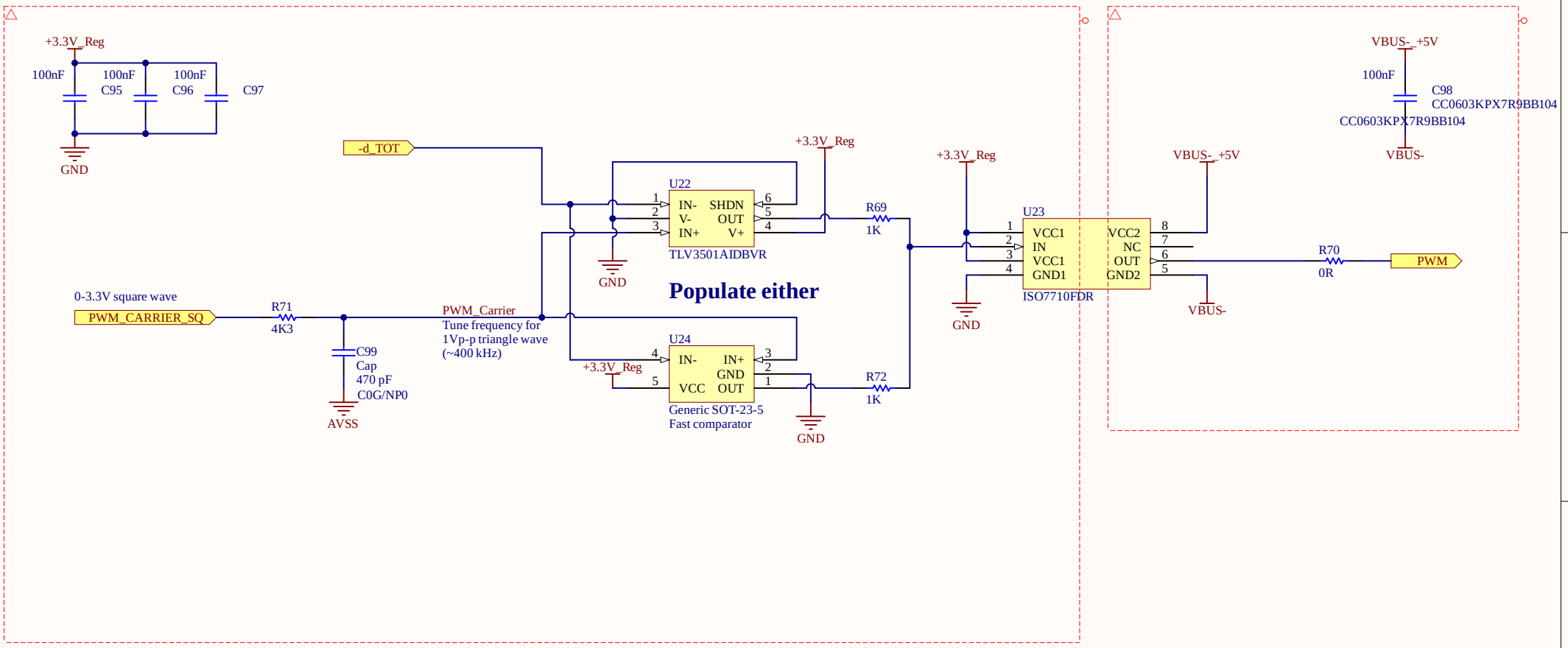




All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

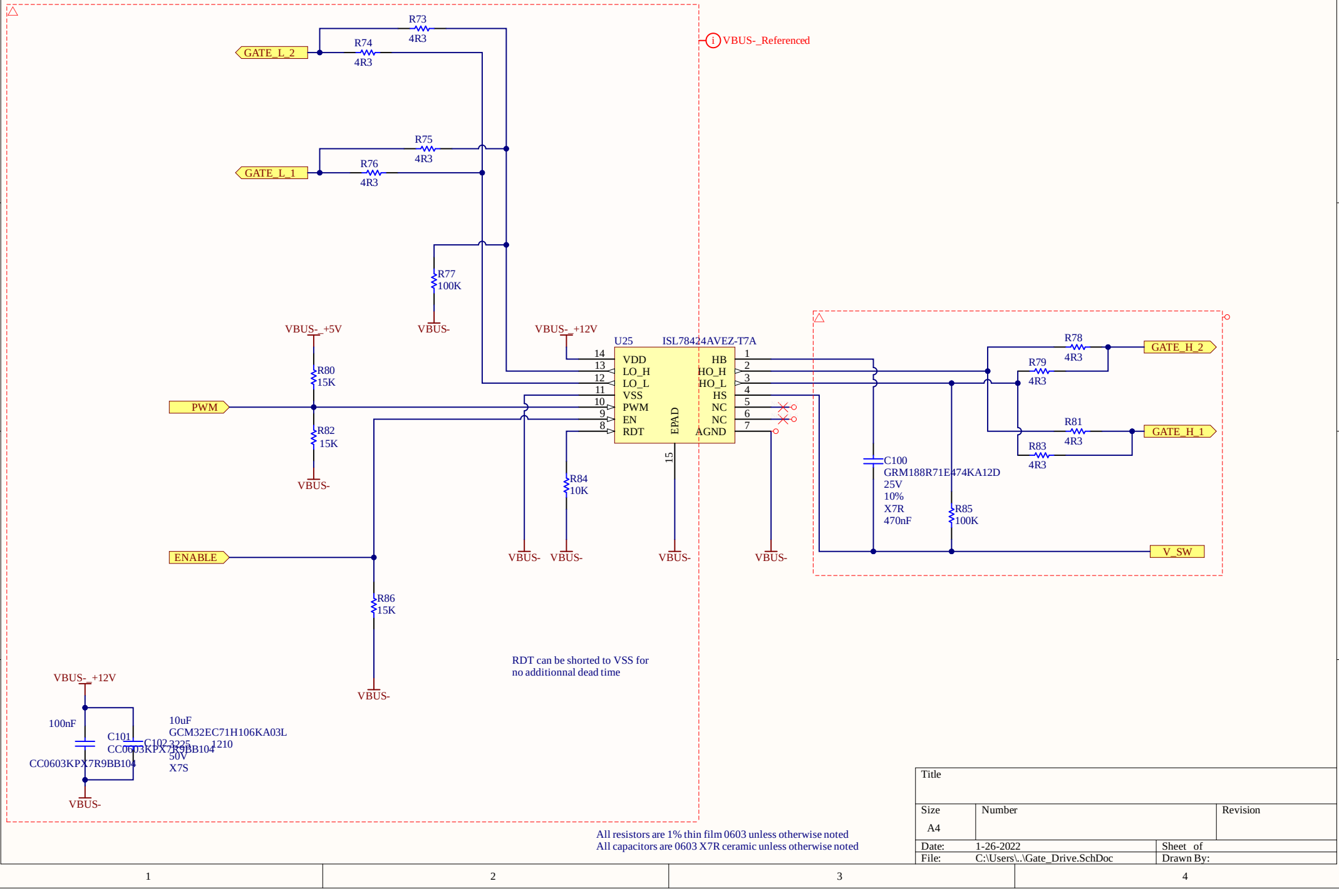
Title		
Size A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\AC&DC_Frontends.SchDoc		Drawn By:


AVDD
U17
MCP6L01T-E/OT
ADC_d_COMP
C87
Cap
1 nF
AVSS
Inverting Summing Amplifier
Vout = -(d_FF + d_CMP) = -d_TOT
Error amplifier
G =1
Vout = i_PV - i_SP = -error
(minus error because compensator is inverting)
Inverting Type-II compensator
F_p0 = 0 rad/s (pole at the origin a.k.a. integrator)
F_z1 = 3.6 krad/s (system has a natural pole at around this frequency)
F_p2 = 1.25 Mrad/s (about half of F_switching)
See "Sim_petit_signal_avec_compensateur.slx" for simulation
R56
27K
Vmid
R59
100K
R58
10K
R57
33K
U18
AD8615AUJZ-R2
-d_TOT
i_PV
R60
100K
U20
AD8615AUJZ-R2
-Error
R62
50K
U19
AD8615AUJZ-R2
d_CMP
R61
100K
i_SP
R63
100K
R64
100K
Increasing R64 increases the damping
5 kΩ < R64 < 330kΩ
d_FF
R65
100K
R66
100K
R67
5K
C88
Cap
56 nF
C89
Cap
160 pF
Anti-windup/reset switch
U21
COM
NO
GND
V+
IN
TS5A4594DCKR
R68
10K
COMP_RESET
100nF
C90
C91
C92
C93
C94
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size
A4
Number
Revision
Date:
1-26-2022
Sheet of
File:
C:\Users\..\Control_Loop.SchDoc
Drawn By:



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

Title		
Size: A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\Pulse_Width_Modulator.SchDoc		Drawn By:



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

Title		
Size A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\Gate_Drive.SchDoc		Drawn By:

+3.3V_Reg

100nF C103 100nF C104 100nF C105 100nF C106 C107

CC0603KPX7R9BB104

GND

VBUS-_Referenced

VBUS-_+5V

100nF C108 CC0603KPX7R9BB104

VBUS-

Rising edge at most every 100 µs
to enable gate driver.

Trigger on rising edge
100 µs pulse duration
Retriggerable

ENABLE_PULSE

ENABLE_PULSE has to be LOW when the latch is set, otherwise trigerring will occur.

U27

SN74LVC1G123DCTR

R89 100K

C109 Cap 1 nF

R90 10K

R87 1K

U26

ISO7710FDR

R88 0R

ENABLE

To gate driver

i_PV

AVDD

C110 100nF R92 15K

IN-

R93 300K

IN+

C111 100nF R94 15K

AVSS

U28 MAX9140EUK+T

U30 MAX9140EUK+T

Window Comparator

Current OK Latch

CURRENT_OK_LATCH_RESET

U29

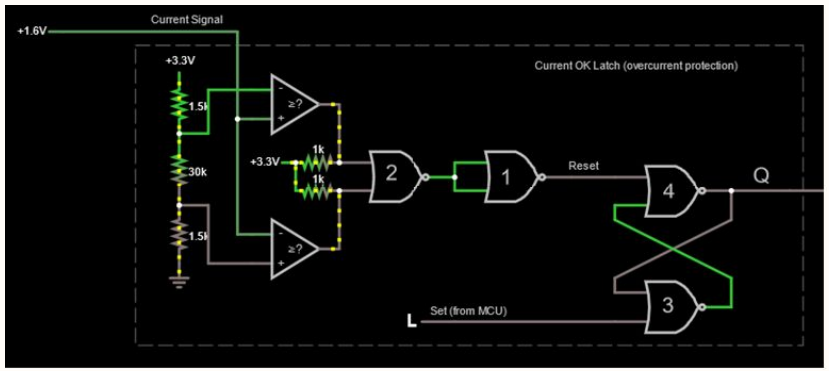
SN74LVC02APW

CURRENT_OK_LATCH_SET

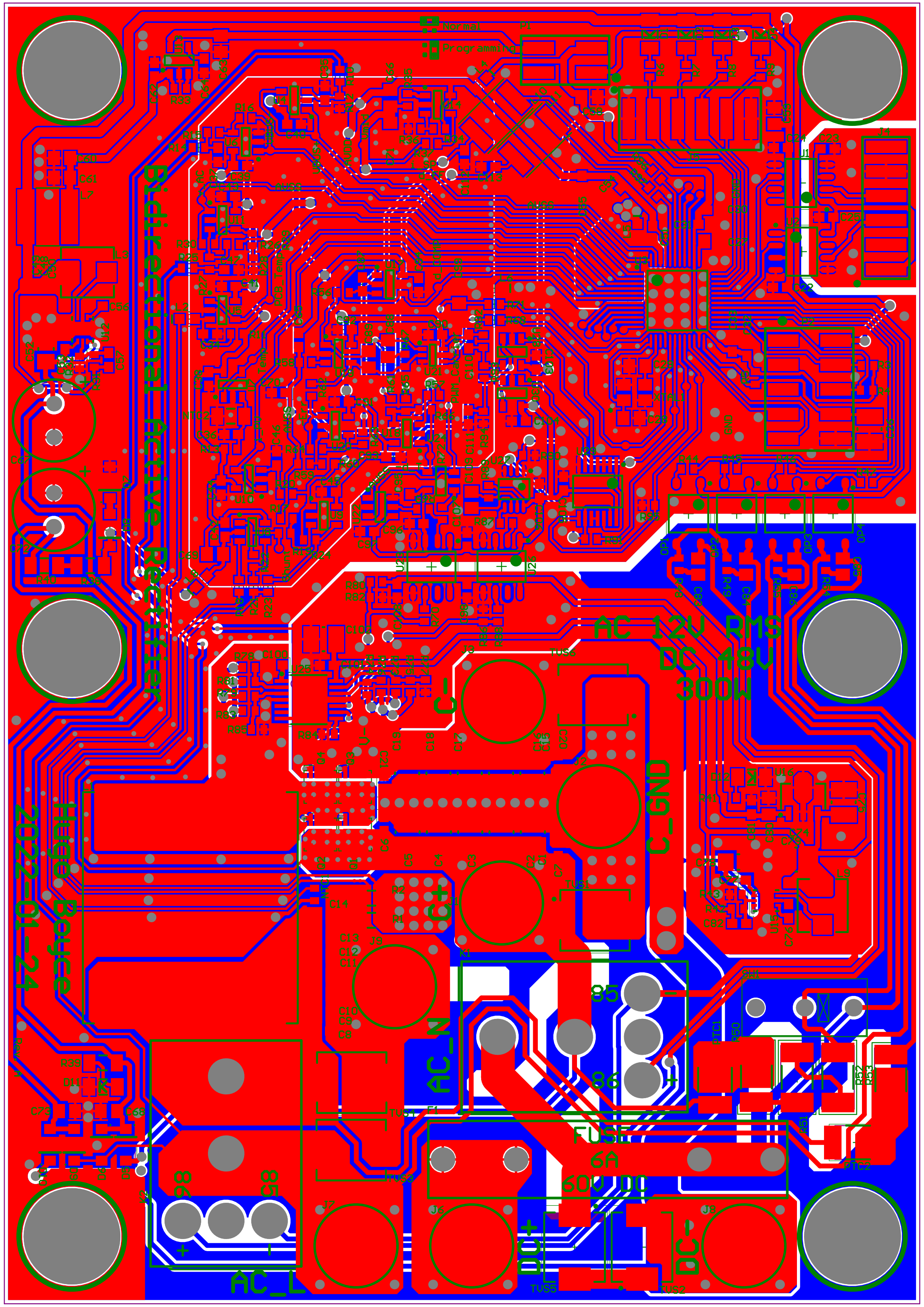
R95 15K

R91 15K

CURRENT_OK_LATCH_Q



Title		
Size A4	Number	Revision
Date: 1-26-2022		Sheet of
File: C:\Users\..\Protection_Logic.SchDoc		Drawn By:



AC 12V RMS
DC 48V
300W
C_GND
C-
C+
AC_N
AC_L
DC+
DC-
FUSE
6A
600 DC
85
86

Board Stack Report