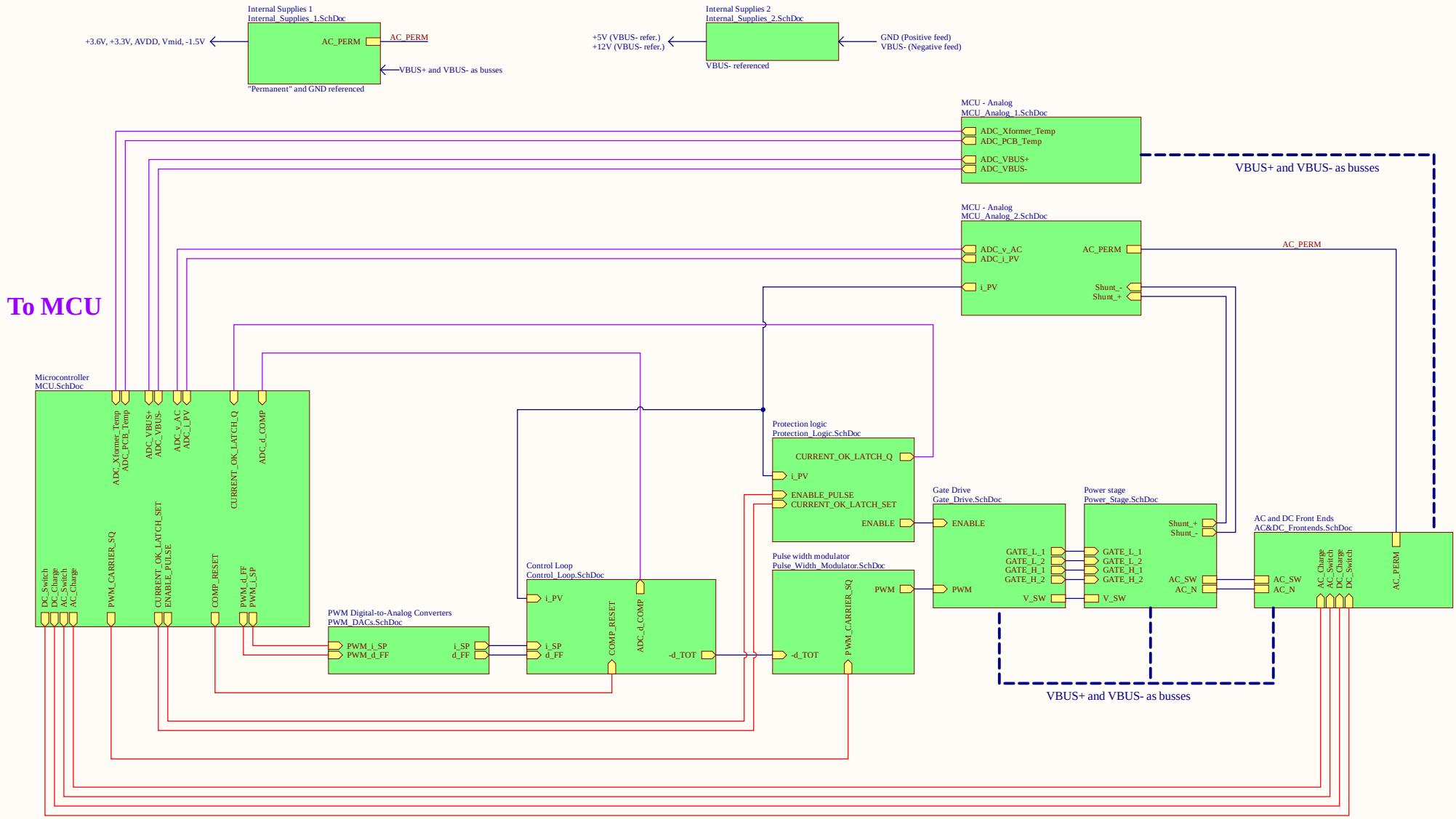
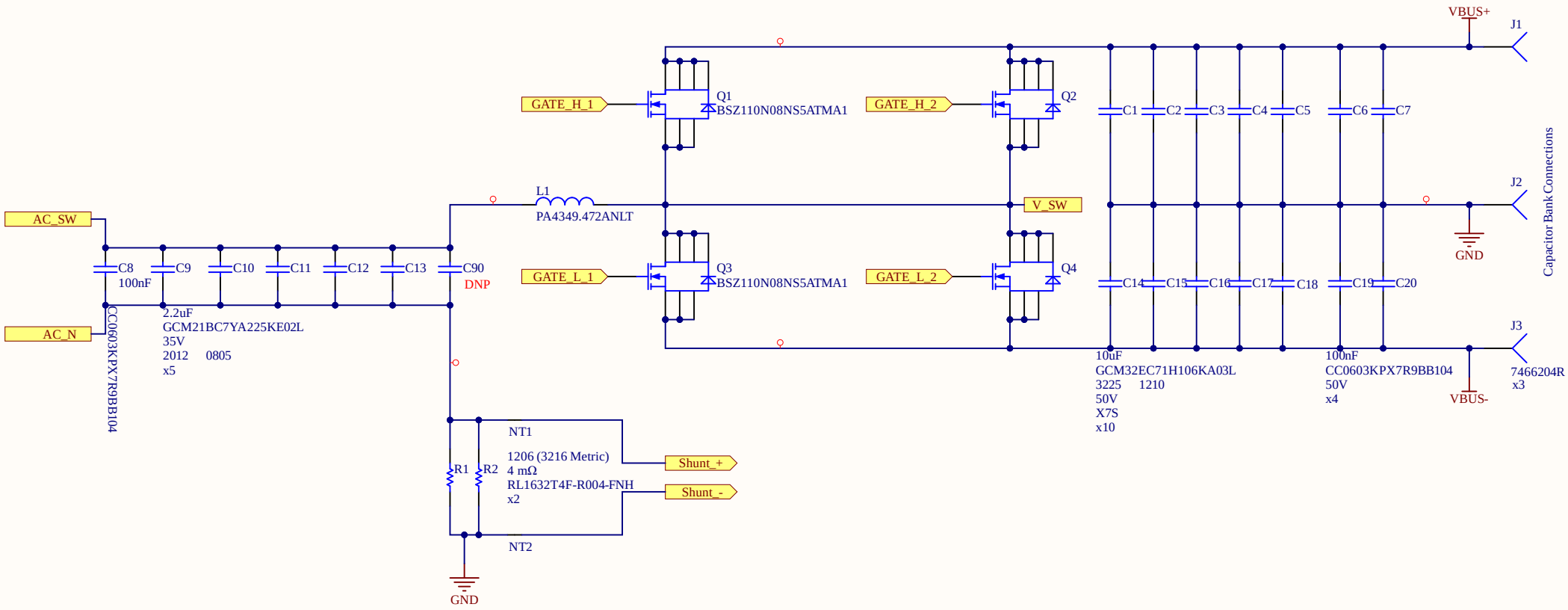


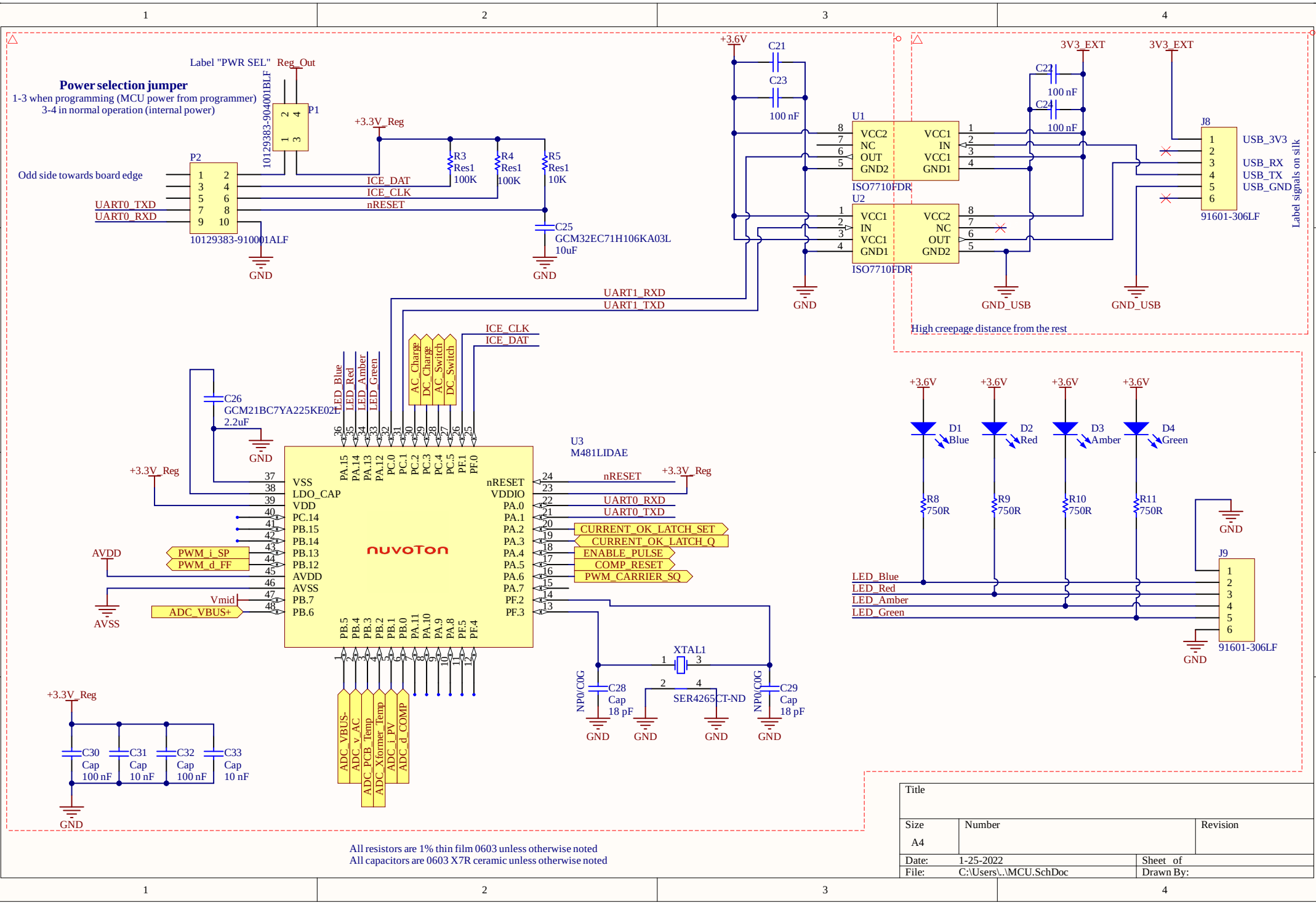
TODO: Make this more readable.

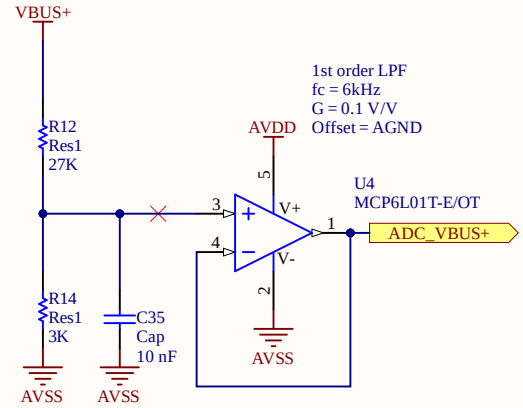
Title		
Size: Tabloid	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\Main_sheet_Top.SchDoc		Drawn By:

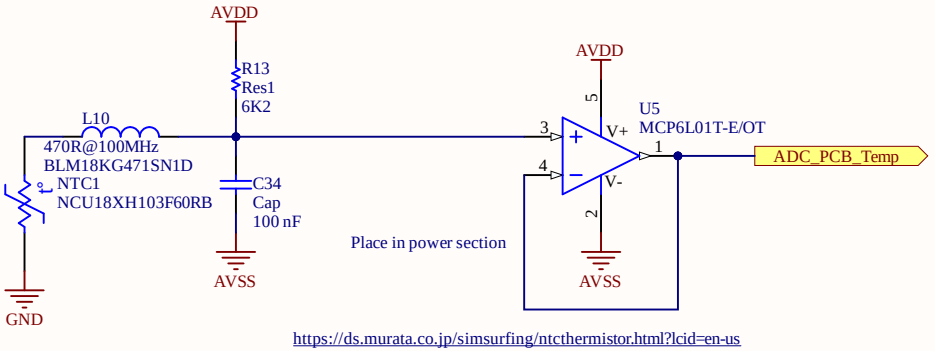


All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

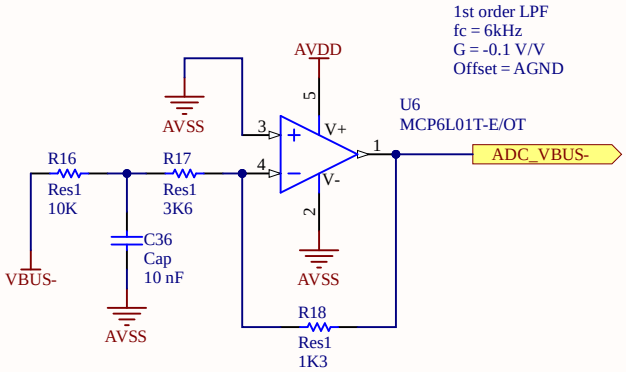
Title		
Size A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\Power_Stage.SchDoc		Drawn By:

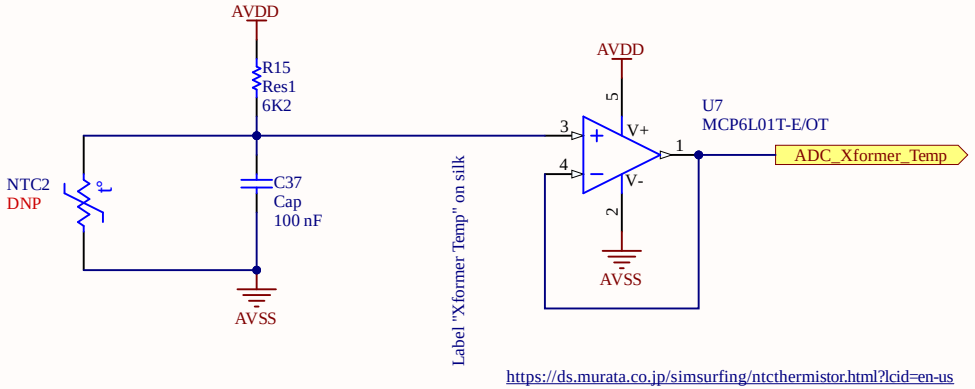

Power selection jumper
1-3 when programming (MCU power from programmer)
3-4 in normal operation (internal power)
Label "PWR SEL"
Reg_Out
10129383-904001BLF
P1
P2
Odd side towards board edge
10129383-910001ALF
+3.3V_Reg
ICE_DAT
ICE_CLK
nRESET
UART0_TXD
UART0_RXD
R3 Res1 100K
R4 Res1 100K
R5 Res1 10K
C25 GCM32EC71H106KA03L 10uF
GND
+3.6V
C21
C23
100 nF
U1
ISO7710FDR
U2
ISO7710FDR
C22
C24
3V3_EXT
J8
91601-306LF
USB_3V3
USB_RX
USB_TX
USB_GND
Label signals on silk
GND_USB
High creepage distance from the rest
UART1_RXD
UART1_TXD
C26 GCM21BC7YA225KE02L 2.2uF
LED_Blue
LED_Red
LED_Amber
LED_Green
AC_Charge
DC_Charge
AC_Switch
DC_Switch
U3
M481LIDAE
nuvoTon
VSS
LDO_CAP
VDD
PC.14
PB.15
PB.14
PB.13
PB.12
AVDD
AVSS
PB.7
PB.6
nRESET
VDDIO
PA.0
PA.1
PA.2
PA.3
PA.4
PA.5
PA.6
PA.7
PF.2
PF.3
PWM_i_SP
PWM_d_FF
Vmid
ADC_VBUS+
CURRENT_OK_LATCH_SET
CURRENT_OK_LATCH_Q
ENABLE_PULSE
COMP_RESET
PWM_CARRIER_SQ
AVDD
AVSS
XTAL1
SER4265CT-ND
C28 Cap 18 pF
C29 Cap 18 pF
NP0/C0G
D1 Blue
D2 Red
D3 Amber
D4 Green
R8 750R
R9 750R
R10 750R
R11 750R
J9
91601-306LF
C30 Cap 100 nF
C31 Cap 10 nF
C32 Cap 100 nF
C33 Cap 10 nF
ADC_VBUS-
ADC_v_AC
ADC_PCB_Temp
ADC_Xformer_Temp
ADC_i_PV
ADC_d_COMP
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size A4
Number
Revision
Date: 1-25-2022
Sheet of
File: C:\Users\..\MCU.SchDoc
Drawn By:



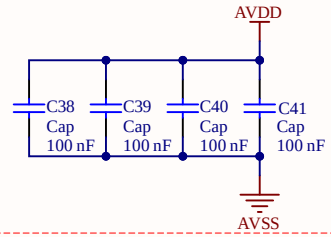


https://ds.murata.co.jp/simsurfing/ntcthermistor.html?lcid=en-us



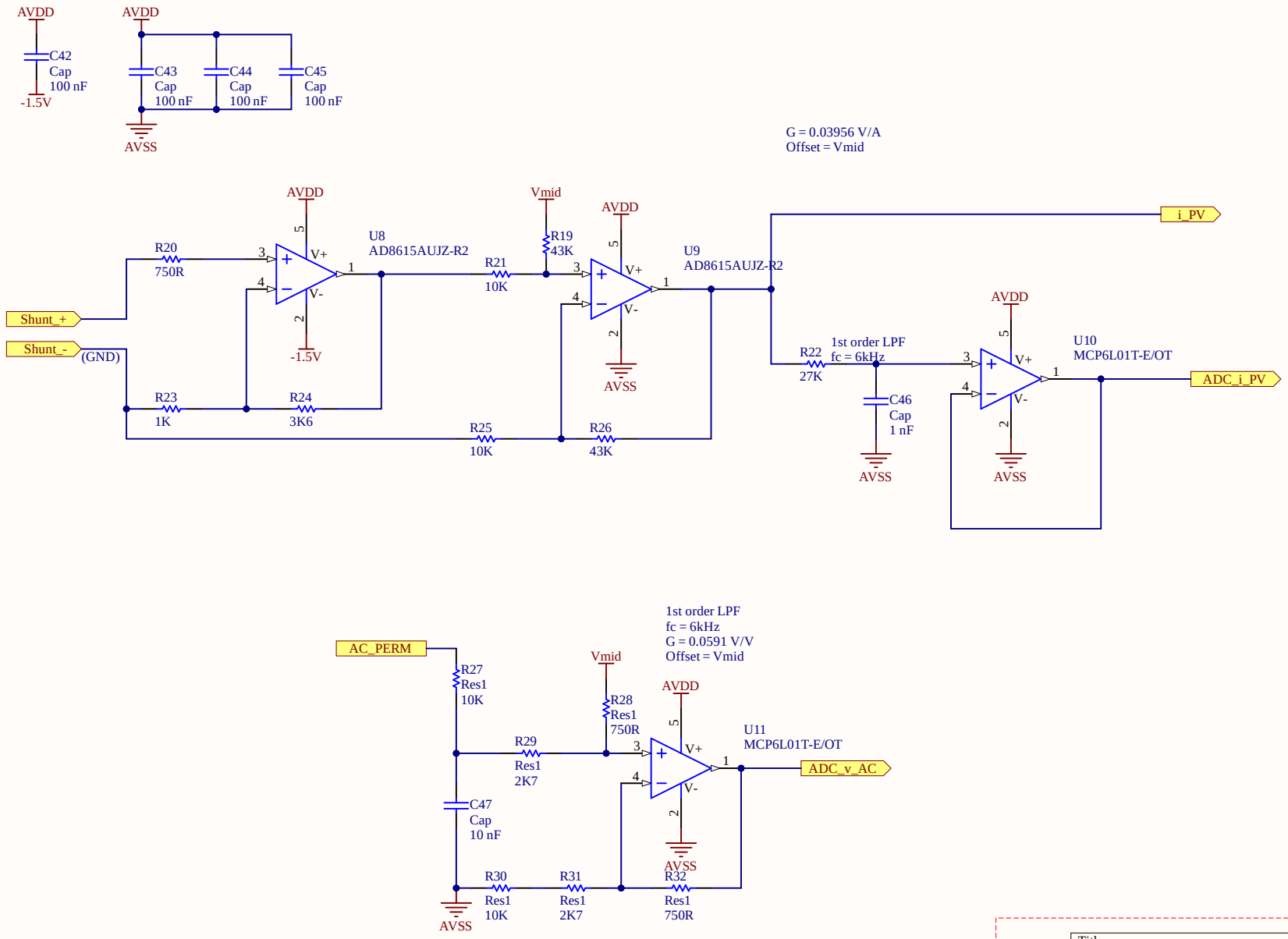


https://ds.murata.co.jp/simsurfing/ntcthermistor.html?lcid=en-us



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

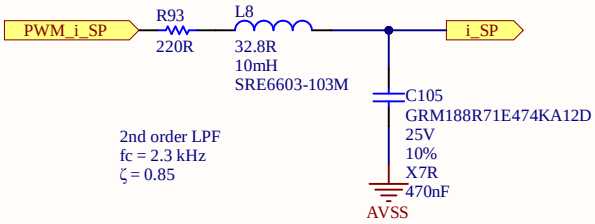
Title		
Size: A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\MCU_Analog_1.SchDoc		Drawn By:



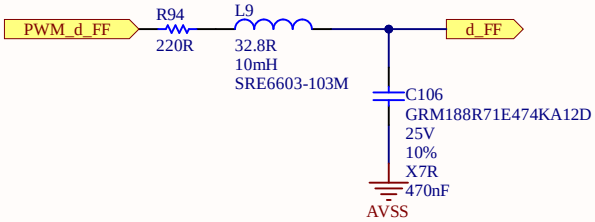
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

Title		
Size A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\MCU_Analog_2.SchDoc		Drawn By:

11-bit PWM DAC
f_in = 93.7 kHz

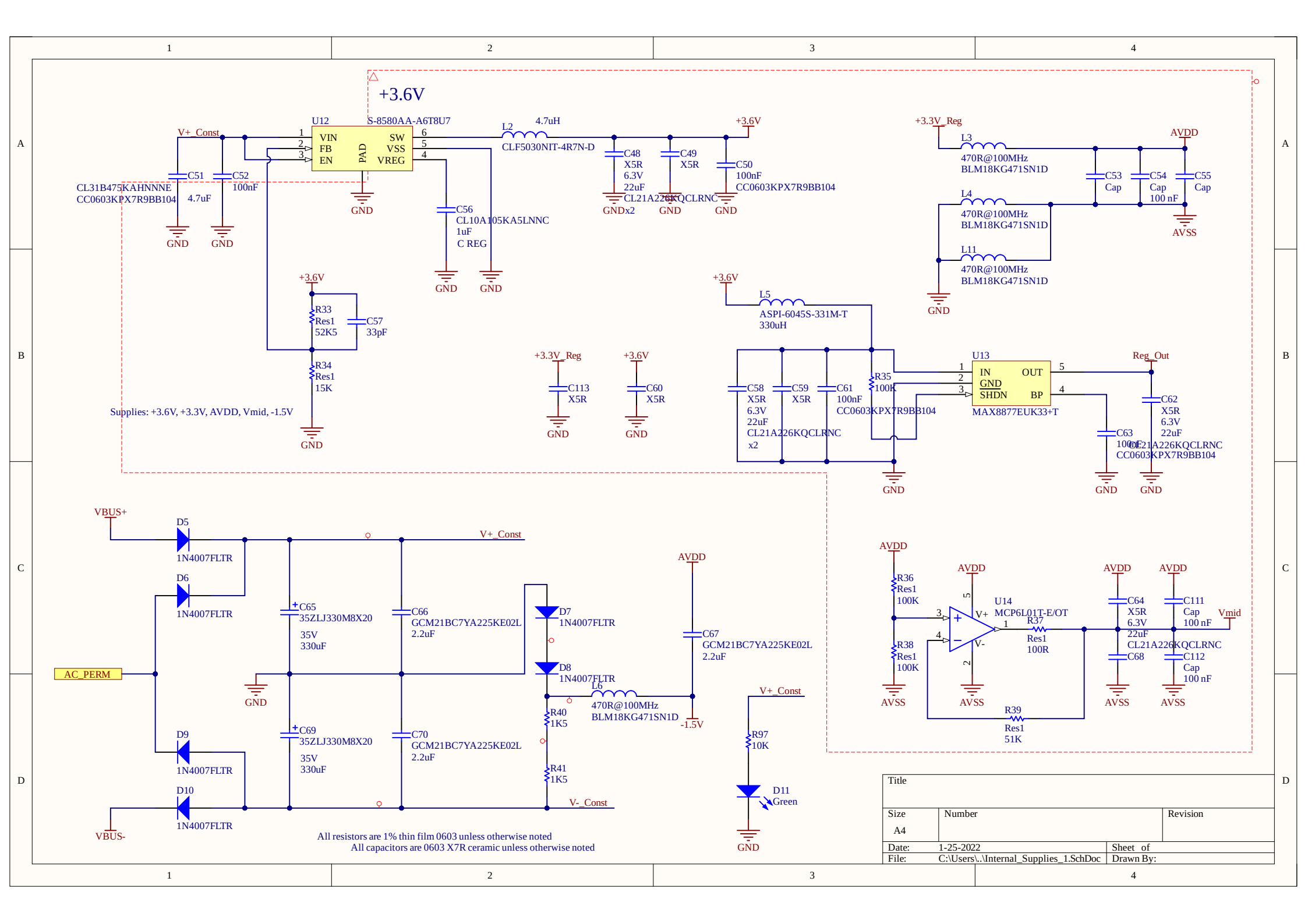


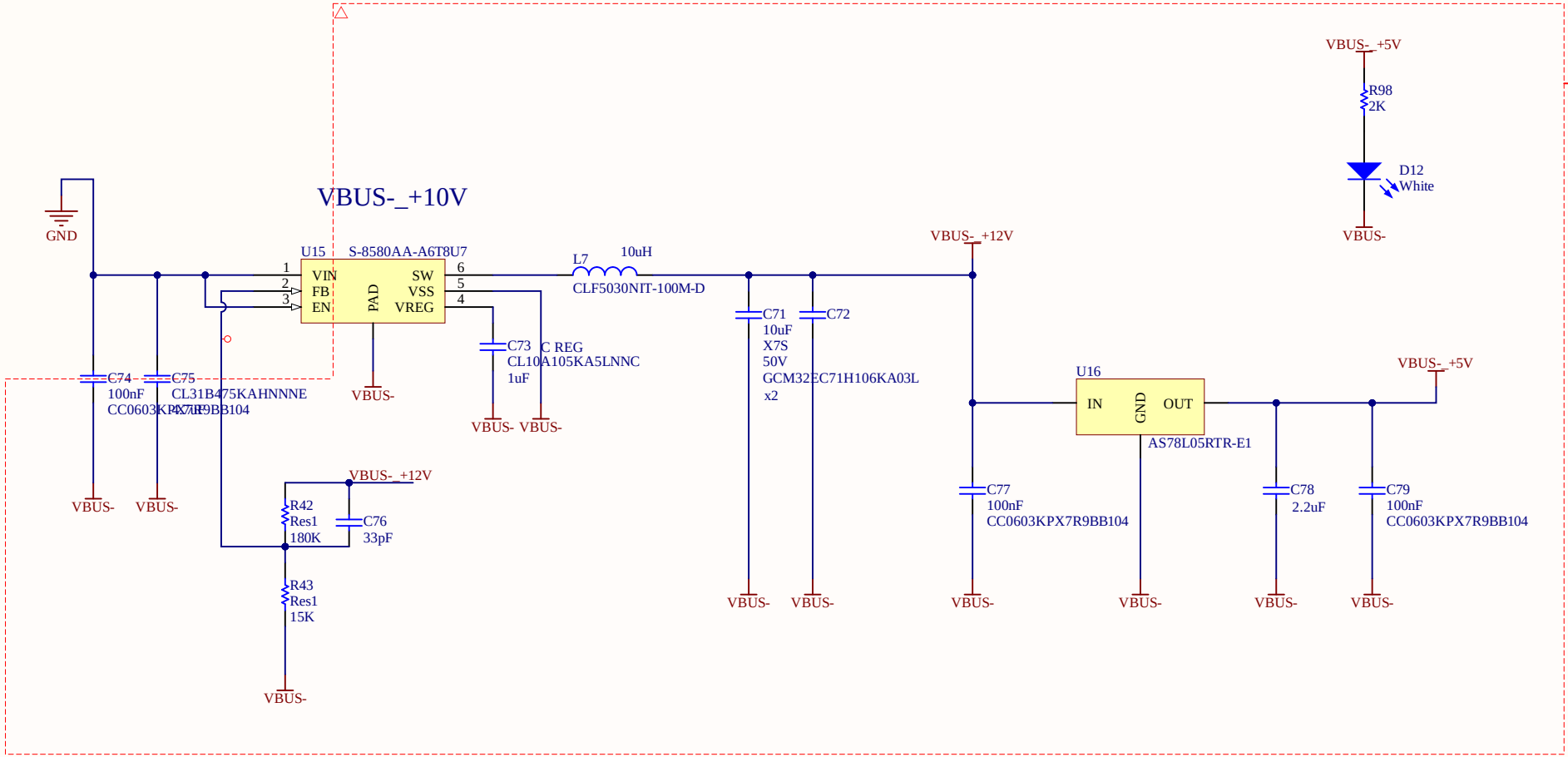
2nd order LPF
fc = 2.3 kHz
ζ = 0.85



This circuit is implemented because I could not get the DACs to work properly.
Obviously it is not necessary with correctly working DACs.

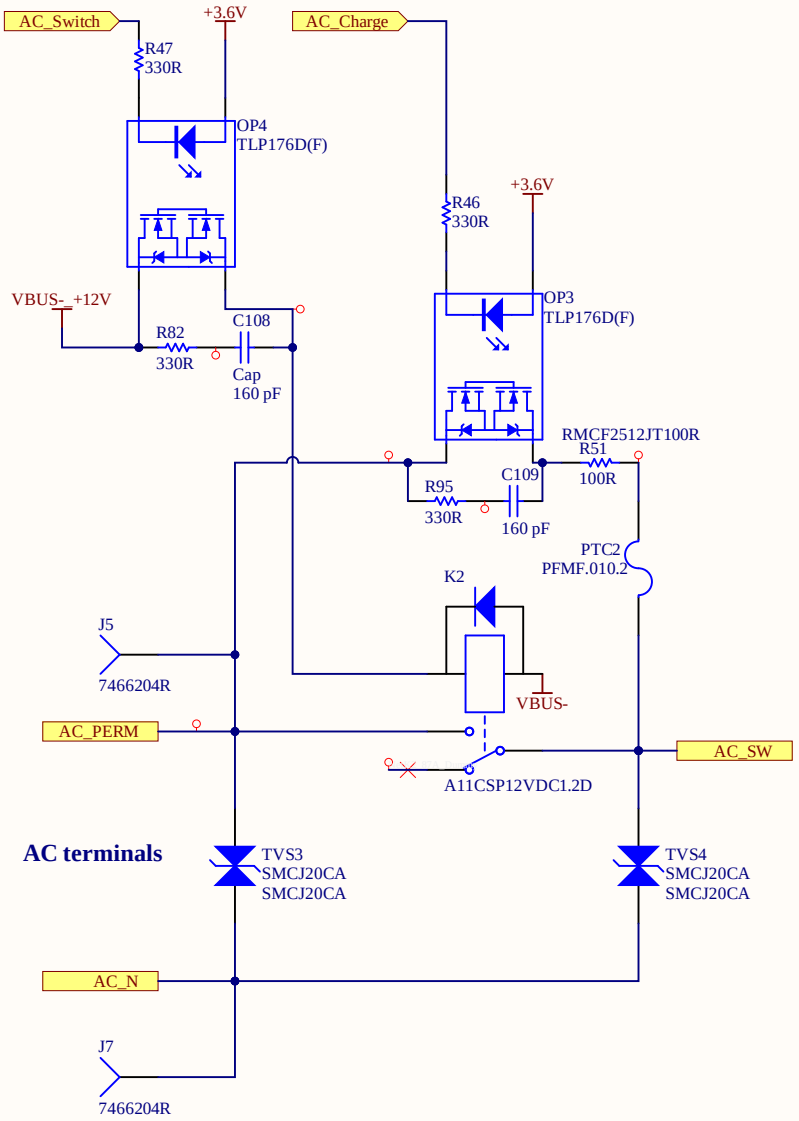
Title		
Size: A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\PWM_DACs.SchDoc		Drawn By:

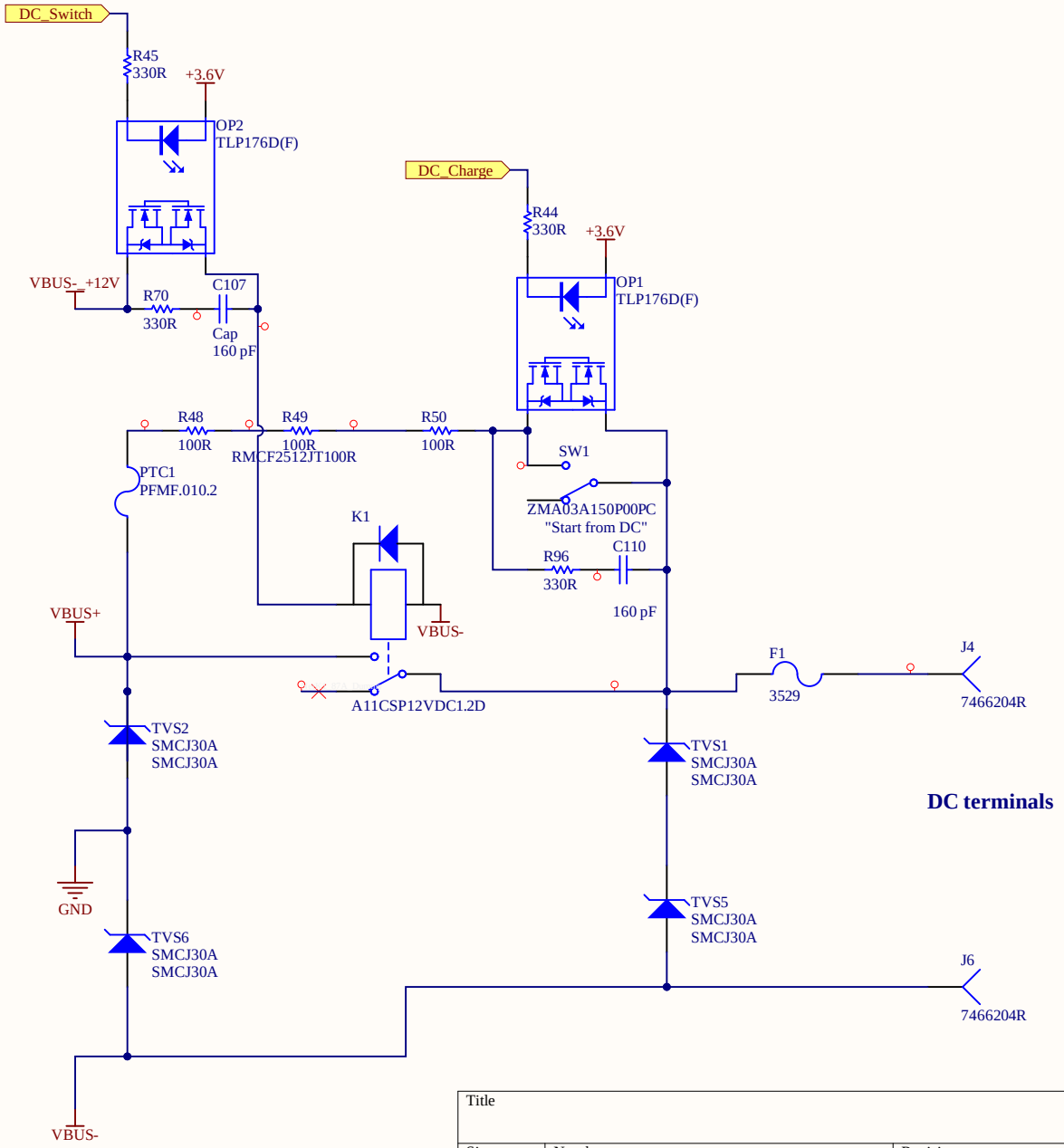

+3.6V
U12
S-8580AA-A6T8U7
VIN
FB
EN
SW
VSS
VREG
PAD
V+_Const
L2
4.7uH
CLF5030NIT-4R7N-D
C48
X5R
6.3V
22uF
CL21A226KQCLRNC
C49
X5R
C50
100nF
CC0603KPX7R9BB104
C51
CL31B475KAHNNNE
CC0603KPX7R9BB104
4.7uF
C52
100nF
C56
CL10A105KA5LNNC
1uF
C REG
GND
GNDx2
+3.3V_Reg
L3
470R@100MHz
BLM18KG471SN1D
L4
L11
AVDD
AVSS
C53
Cap
C54
Cap
100 nF
C55
Cap
R33
Res1
52K5
C57
33pF
R34
Res1
15K
Supplies: +3.6V, +3.3V, AVDD, Vmid, -1.5V
C113
X5R
C60
X5R
L5
ASPI-6045S-331M-T
330uH
C58
X5R
6.3V
22uF
CL21A226KQCLRNC
x2
C59
X5R
C61
100nF
CC0603KPX7R9BB104
R35
100K
U13
IN
GND
SHDN
OUT
BP
MAX8877EUK33+T
Reg_Out
C62
X5R
6.3V
22uF
CL21A226KQCLRNC
C63
100nF
CC0603KPX7R9BB104
VBUS+
VBUS-
D5
D6
D9
D10
1N4007FLTR
V+_Const
V-_Const
AC_PERM
C65
35ZLJ330M8X20
35V
330uF
C66
GCM21BC7YA225KE02L
2.2uF
C69
C70
D7
D8
C67
L6
470R@100MHz
BLM18KG471SN1D
-1.5V
R40
1K5
R41
1K5
R97
10K
D11
Green
R36
Res1
100K
R38
Res1
100K
U14
MCP6L01T-E/OT
V+
V-
R37
Res1
100R
R39
Res1
51K
C64
X5R
6.3V
22uF
CL21A226KQCLRNC
C68
C111
Cap
100 nF
C112
Cap
100 nF
Vmid
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size
A4
Number
Revision
Date:
1-25-2022
Sheet of
File:
C:\Users\..\Internal_Supplies_1.SchDoc
Drawn By:



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

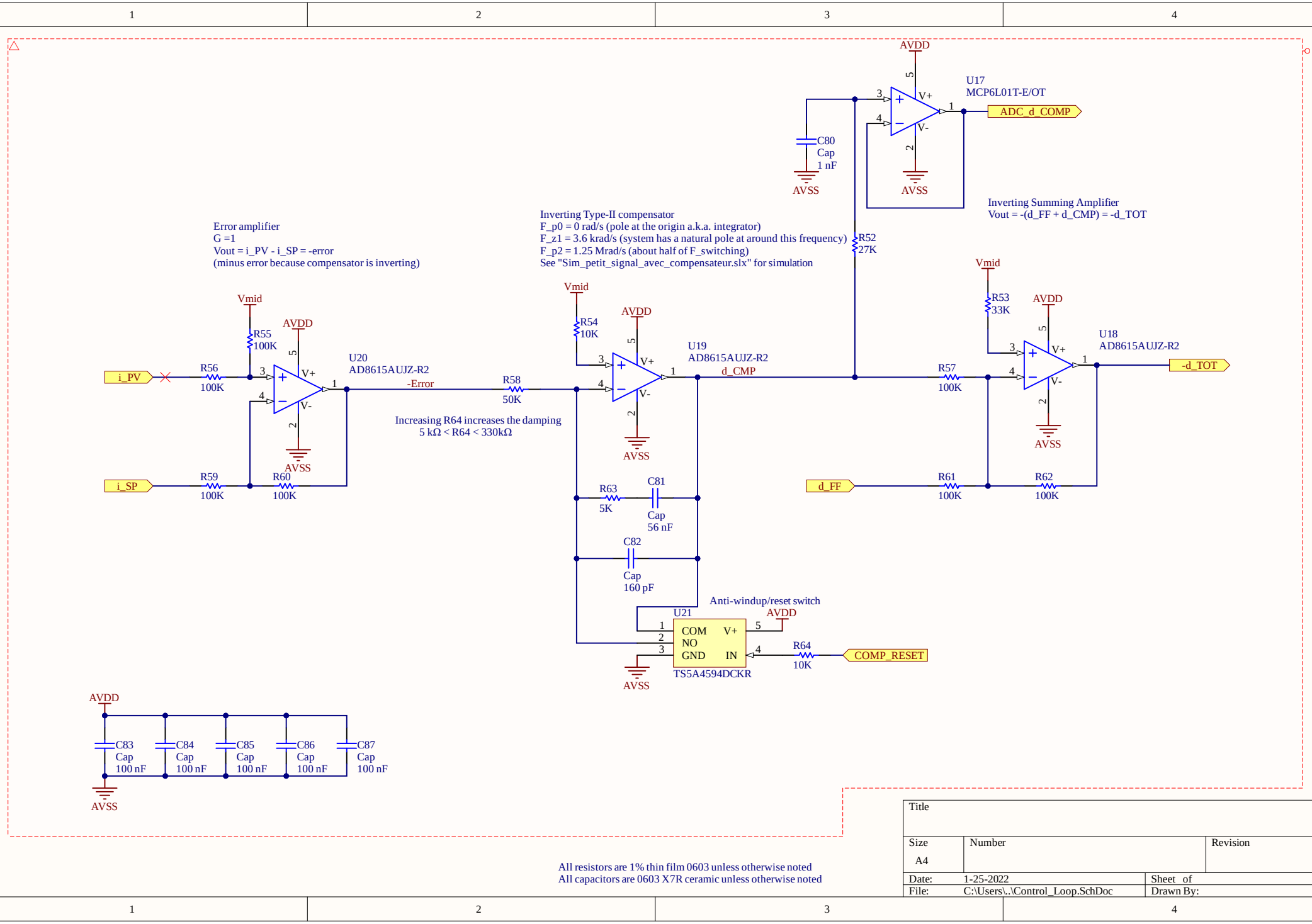
Title		
Size: A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\Internal_Supplies_2.SchDoc		Drawn By:

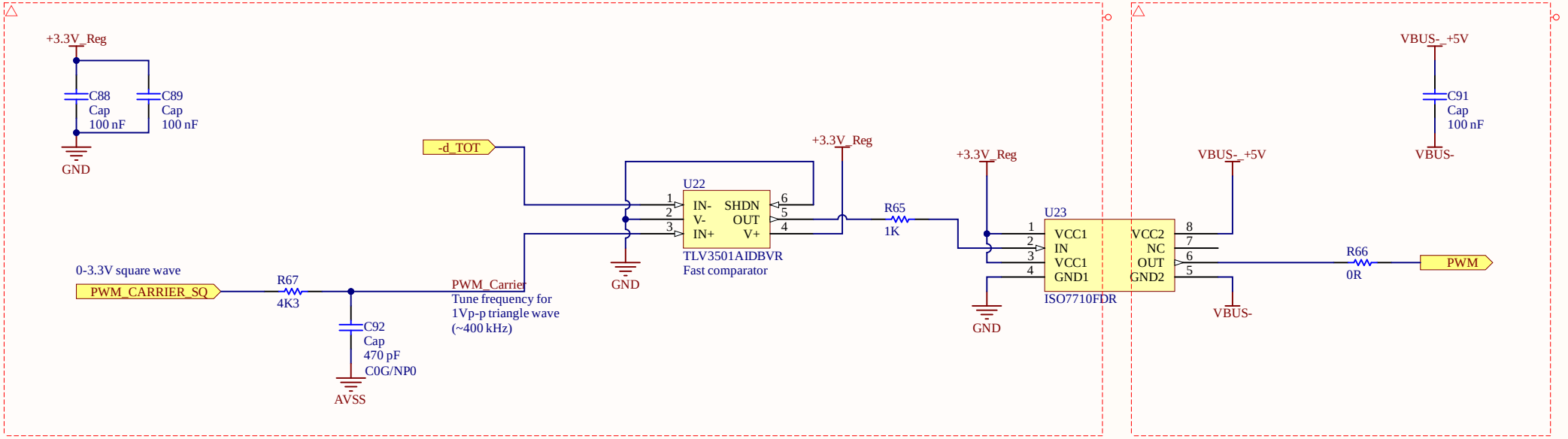




All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

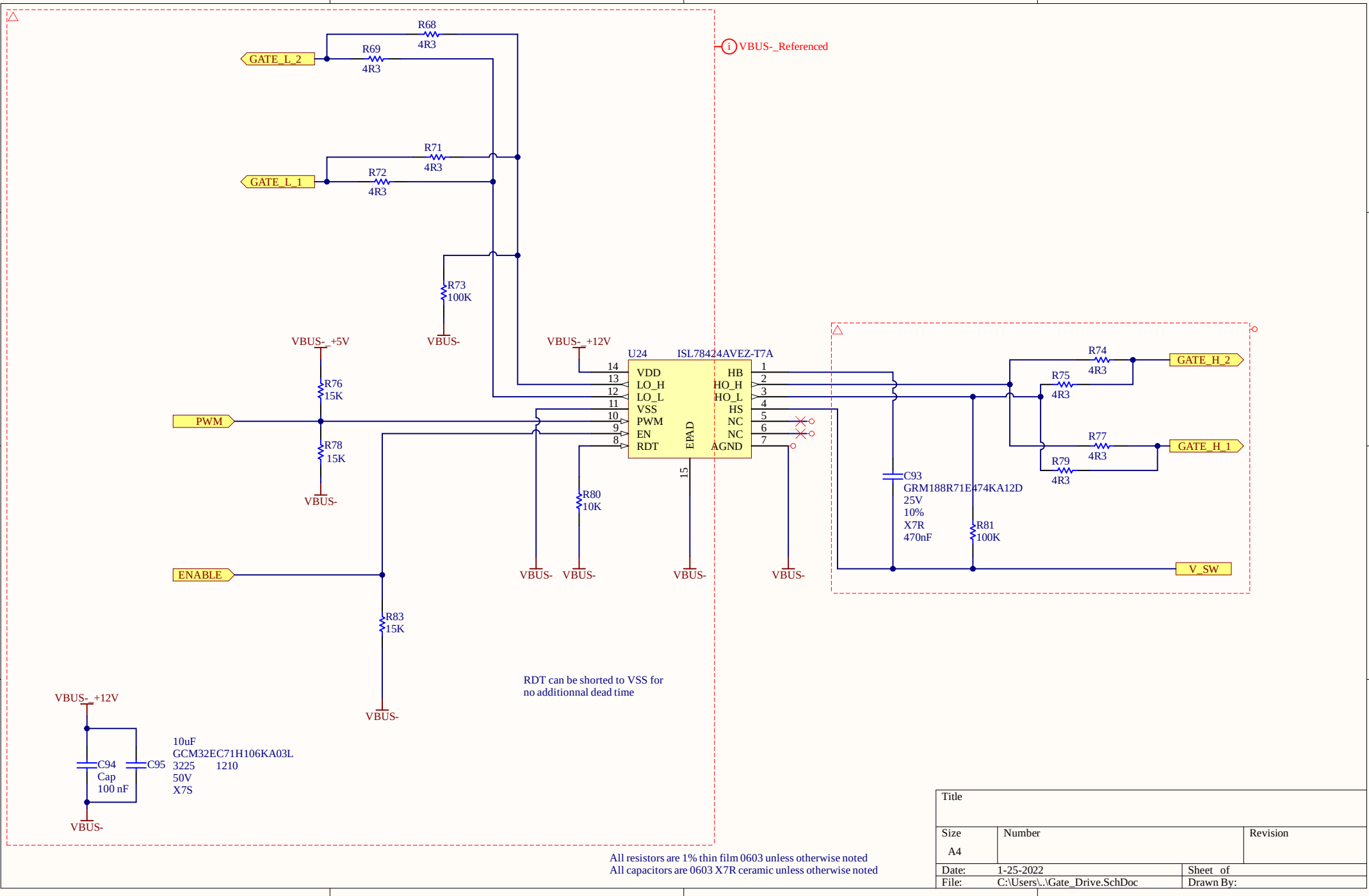
Title		
Size: A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\AC&DC_Frontends.SchDoc		Drawn By:


AVDD
U17
MCP6L01T-E/OT
ADC_d_COMP
C80
Cap
1 nF
AVSS
Inverting Summing Amplifier
Vout = -(d_FF + d_CMP) = -d_TOT
Error amplifier
G =1
Vout = i_PV - i_SP = -error
(minus error because compensator is inverting)
Inverting Type-II compensator
F_p0 = 0 rad/s (pole at the origin a.k.a. integrator)
F_z1 = 3.6 krad/s (system has a natural pole at around this frequency)
F_p2 = 1.25 Mrad/s (about half of F_switching)
See "Sim_petit_signal_avec_compensateur.slx" for simulation
R52
27K
Vmid
R55
100K
R54
10K
R53
33K
i_PV
R56
100K
U20
AD8615AUJZ-R2
-Error
R58
50K
U19
AD8615AUJZ-R2
d_CMP
R57
100K
U18
AD8615AUJZ-R2
-d_TOT
Increasing R64 increases the damping
5 kΩ < R64 < 330kΩ
i_SP
R59
100K
R60
100K
R63
5K
C81
Cap
56 nF
C82
Cap
160 pF
d_FF
R61
100K
R62
100K
Anti-windup/reset switch
U21
COM
NO
GND
V+
IN
TS5A4594DCKR
R64
10K
COMP_RESET
C83
Cap
100 nF
C84
Cap
100 nF
C85
Cap
100 nF
C86
Cap
100 nF
C87
Cap
100 nF
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size
A4
Number
Revision
Date:
1-25-2022
Sheet of
File:
C:\Users\..\Control_Loop.SchDoc
Drawn By:



All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted

Title		
Size: A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\Pulse_Width_Modulator.SchDoc		Drawn By:


R68
4R3
GATE_L_2
R69
4R3
R71
4R3
GATE_L_1
R72
4R3
R73
100K
VBUS-
VBUS-_Referenced
VBUS-_+5V
VBUS-_+12V
U24
ISL78424AVEZ-T7A
VDD
LO_H
LO_L
VSS
PWM
EN
RDT
EPAD
HB
HO_H
HO_L
HS
NC
NC
AGND
R76
15K
PWM
R78
15K
VBUS-
R80
10K
VBUS-
VBUS-
VBUS-
R74
4R3
GATE_H_2
R75
4R3
R77
4R3
GATE_H_1
R79
4R3
C93
GRM188R71E474KA12D
25V
10%
X7R
470nF
R81
100K
V_SW
ENABLE
R83
15K
VBUS-
RDT can be shorted to VSS for
no additionnal dead time
VBUS-_+12V
C94
Cap
100 nF
C95
10uF
GCM32EC71H106KA03L
3225
1210
50V
X7S
VBUS-
All resistors are 1% thin film 0603 unless otherwise noted
All capacitors are 0603 X7R ceramic unless otherwise noted
Title
Size
A4
Number
Revision
Date:
1-25-2022
Sheet of
File:
C:\Users\..\Gate_Drive.SchDoc
Drawn By:

+3.3V_Reg

C96 Cap 100 nF
C97 Cap 100 nF
C98 Cap 100 nF
C99 Cap 100 nF
C100 Cap 100 nF

GND

VBUS-_Referenced

VBUS-_+5V

C101 Cap 100 nF

VBUS-

Rising edge at most every 100 µs to enable gate driver.

Trigger on rising edge
100 µs pulse duration
Retriggerable

+3.3V_Reg

U26

A
B
CLR
GND
Vcc
Cext/Rext
Cext
Q

SN74LVC1G123DCTR

R86 100K

C102 Cap 1 nF

ENABLE_PULSE

ENABLE_PULSE has to be LOW when the latch is set, otherwise trigerring will occur.

R87 10K

GND

+3.3V_Reg

R84 1K

U25

VCC1
IN
VCC1
GND1
VCC2
NC
OUT
GND2

ISO7710FDR

VBUS-_+5V

R85 0R

ENABLE

To gate driver

VBUS-

R88 15K

CURRENT_OK_LATCH_Q

i_PV

AVDD

C103 Cap 100 nF

R89 15K

R90 300K

C104 Cap 100 nF

R91 15K

AVSS

Window Comparator

U27

IN-
V-
IN+
SHDN
OUT
V+

TLV3501AIDBVR

U29

TLV3501AIDBVR

+3.3V_Reg

Current OK Latch

CURRENT_OK_LATCH_RESET

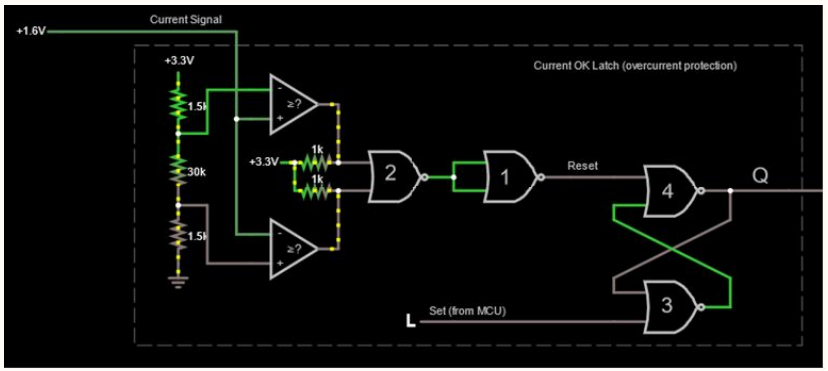
U28

1Y
1A
1B
2Y
2A
2B
GND
QUAD NOR
Vcc
4Y
4B
4A
3Y
3B
3A

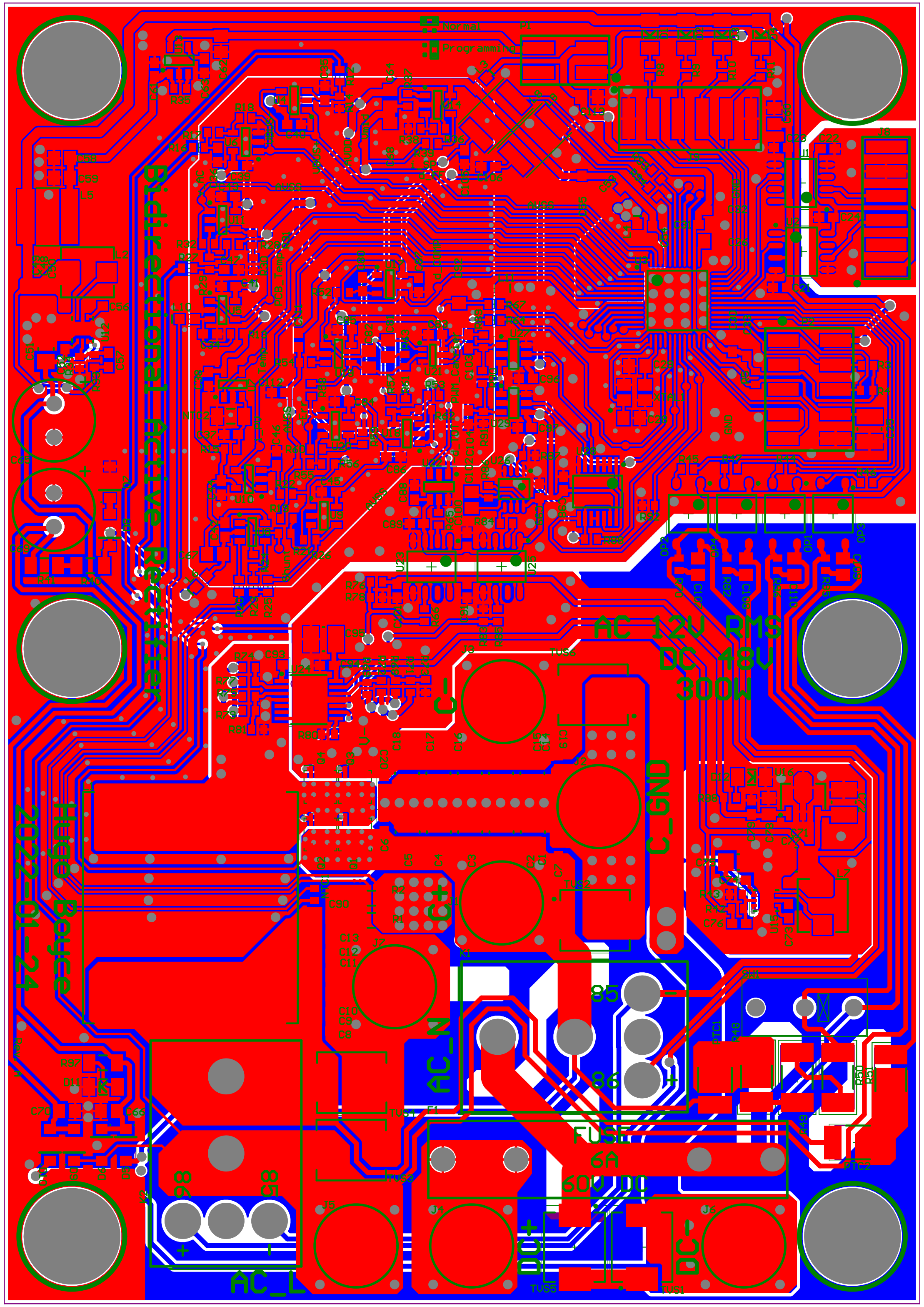
SN74LVC02APW

CURRENT_OK_LATCH_SET

R92 15K



Title		
Size A4	Number	Revision
Date: 1-25-2022		Sheet of
File: C:\Users\..\Protection_Logic.SchDoc		Drawn By:



AC 12V RMS
DC 48V
300W
C_GND
AC_N
AC_L
FUSE
6A
DC+
DC-
85
86

Board Stack Report