Problem:
Optimal Wiring Topology for Electromigration Avoidance
2015 ICCAD/SIGDA CADathlon Training in Taiwan

Table of Contents

1. Introduction

As technology advancing, the shrinking feature size results in the increasing current density. When the current density of a wire exceeds the process limitation, a mass of atoms inside of the metal are forced to migrate along the direction of the current, and the gradual transport eventually causes a permanent failure (e.g., open- or short-circuit defect). This phenomenon is referred to as electromigration (EM). In modern analog and mixed-signal designs, EM has become a prevalent reliability issue for signal or power lines. To diminish the EM risk, a thin wire should be widened according to its current density. If a good wiring topology with EM consideration is applied to a router, we may immune EM with much fewer routing resources, i.e., smaller wire area. Consider an instance as shown in Fig. 1(a), where a signal net has three current sources and four current sinks. The flow of each current source/sink is indicated by a positive/negative value. In this example, we normalize the maximum allowable flow in a unit width wire to 1. If the minimum wirelength routing is applied, followed by EM fixing by widening wires at post-layout, Fig. 1(b) depicts the result of wire area 182. (The value/arrow beside each wire segment indicates its flow/direction.) Considering EM during routing instead, we may find an optimal routing solution of wire area 142 (Fig. 1(c)(d)). In this problem, the contestants are asked to design an optimal wiring topology for EM avoidance (e.g., Fig. 1(c) for Fig. 1(a)).

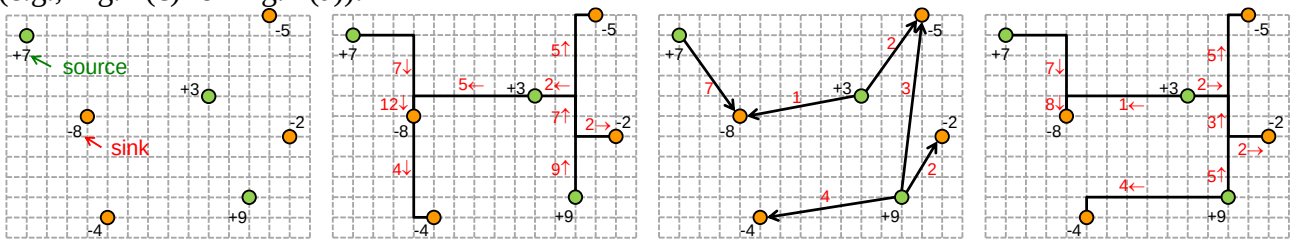

Fig. 1. EM routing. (a) An instance with 3 current sources and 4 current sinks. (b) A routing of minimum wirelength: area 182, wirelength 33. (c) Optimal wiring topology. (d) A routing of minimum area 142.

2. Problem statement

2.1. Brief description

The Wiring Topology for Electromigration Avoidance Problem: Given a set $S = \{s_1, s_2, \ldots, s_m\}$ of m current sources, a set $T = \{t_1, t_2, \ldots, t_n\}$ of n current sinks, each current source i (sink j) is associated with its flow f_{s_i} (f_{t_j}), construct a wiring topology to connect all current sources and sinks in S+T, such that the total wire area is minimized and electromigration is avoided. Assume that both the maximum tolerable flow for a unit width wire and the minimum feasible wire width are 1. In all testcases, the flows of sources/sinks are integers.

2.2. Wirelength and wire area

For rectilinear routing, only vertical and horizontal lines are allowed. Hence, as depicted in Fig. 2(a), the wirelength (Manhattan distance) $l(p_1, p_2)$ between two arbitrary points $p_1(x_1, y_1, f_1)$ and $p_2(x_2, y_2, f_2)$ can be computed as follows.

$$l(p_1, p_2) = l_x + l_y = |x_1 - x_2| + |y_1 - y_2|.$$

It can be seen that each possible practical route between arbitrary two sources/sinks can be abstracted by the slant wire segment of length equal to their Manhattan distance. Moreover, due to coordinate independence, l_x and l_y are considered separately.

Typically, the consumed routing resource can be computed as the total wire area. For practical routes, if two wire segments overlap, as shown in Fig. 2(b), the overlapped parts can be *superpositioned*, i.e., *additive* considering current directions. Based on superposition, a current can be split into pieces, planned individually, and then combined together. As revealed by [1], the optimal wiring topology contains only source-to-sink connections, and the wire area estimated by the optimal wiring topology is equal to that at detailed routing. Moreover, the optimal wiring topology can be obtained by constructing a flow network for an arbitrary EM-free wiring topology and then removing all negative cycles in the flow network.

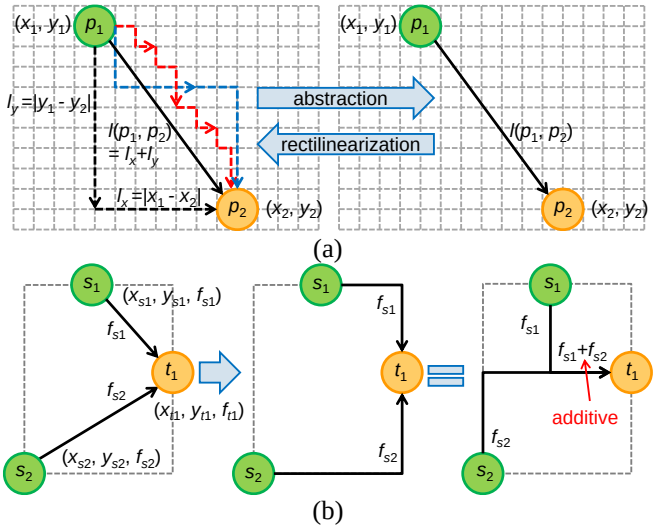

Fig. 2. (a) Wirelength in the rectilinear system. (b) Wire segments can be superpositioned.

2.3. Input/output specification

In order to test your program, you are asked to add the following command-line parameters to your program (e.g., ./em inp1.in inp1.out):

./em [input file name] [output file name]

- Input

The input file describes the current source S and sink T information. The first line describes the total number sources and sinks (m+n). In the following (m+n) lines, each line indicates the x-coordinate, y-coordinate, and flow of a current source or sink. A source/sink is associated with a positive/negative flow. The input file of the example shown in Fig. 1(a) is listed as follows.

Sample input

```
7
1 10 +7          // a current source at (1, 10) with flow 7; the "+" sign may be omitted.
4 6 -8
5 1 -4
10 7 +3
12 2 +9
14 5 -2
13 11 -5
```

- Output

The program first prints the optimal total wire area. Then, the following lines describe the optimal wiring topology. Each line indicates the *x*-coordinate and *y*-coordinate of a source, the *x*-coordinate and *y*-coordinate of a sink, and the corresponding wire width. The output file of the example shown in Fig. 1 is listed as follows.

Sample output

```
142                    // total wire area
1 10 4 6 7             // a connection from source (1, 10) to sink (4, 6) of width 7
10 7 4 6 1
10 7 13 11 2
12 2 5 1 4
12 2 13 11 3
12 2 14 5 2
```

3. Evaluation

You need to submit the following materials: (1) source codes, (2) executable binaries, and (3) a text readme file (readme.txt) stating how to build and use your programs. Please check these items before submission. Each case is individually evaluated by

- Time bound: 30 mins for each case.
- (10%) The correctness of wiring topology: A correct wiring topology fully assigns the flows from sources to sinks.
- (60%) The optimality of wiring topology: An optimal wiring topology is a correct wiring topology of minimum wire area. The optimality score is obtained only if a correct wiring topology is obtained. $\text{Optimality score} = \frac{\text{optimal wire area}}{\text{wire area}} * 60$.
- (30%) Runtime (30%). The running time score is obtained only if the optimal wiring topology is obtained. $\text{Runtime score} = \frac{\text{fast runtime of optimal solution reported by all contestants}}{\text{runtime}} * 30$.

4. References

[1] Iris Hui-Ru Jiang, Hua-Yu Chang, and Chih-Long Chang, "WiT: Optimal wiring topology for electromigration avoidance," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 20, no. 4, Apr. 2012, pp. 581—592. Also see in *Proc. 19th ACM International Symposium on Physical Design (ISPD-2010)*, San Francisco, CA, Mar. 2010, pp. 177—184. Slides [Online] Available: http://www.ispd.cc/slides/slides10/8_05.pdf

[2] Jing-Wei Lin, Tsung-Yi Ho, and Iris Hui-Ru Jiang, "Reliability-driven power/ground routing for analog ICs," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 17, no. 1, Jan. 2012, pp. 6:1—6:26.