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Computer Architecture HW (4) (memory)

Ans:

5.4

5.4.1

L2 cache 有較大的 write miss penalty，而 L1 的 write miss penalty 較小。所以我們應該在 L1 和 L2 之間設置一個 write buffer 來隱藏 L2 的 write miss latency。當將替換掉 dirty block 時，buffer 對於 L2 有助益，因為在將 dirty block 寫入 memory 之前新的 block 的可被 read in。

5.4.2

在 L1 write miss 時，word 直接寫入 L2 而不將其 block 帶入 L1。如果這導致 L2 miss，則必須將其 block 帶入 L2，這可能會替換掉必須先寫入 memory 的 dirty block。

5.4.3

在 L1 write miss 後，block 將留在 L2 中而不是 L1。對同一 block 的後續 read miss 會需要 L2 block 被寫回 memory，並被傳送到 L1，最後在 L2 中失效。

5.4.4

Instruction bandwidth: (.003 * 64) * 0.5 = 0.096 bytes/cycle.
Data read bandwidth: 0.02 * (0.13 + 0.050) * 64 = 0.23 bytes/cycle.
Total read bandwidth: 0.33 bytes/cycle.
Data write bandwidth: 0.05 * 4 = 0.2 bytes/cycle.

5.4.5

Instruction bandwidth: (.003 * 64) * 0.5 = 0.096 bytes/cycle.
Data read bandwidth: 0.02 * (0.13 + 0.050) * 64 = 0.23 bytes/cycle.
Total read bandwidth: 0.33 bytes/cycle.
Data write bandwidth: 0.02 * 0.30 * (0.13 + 0.050) * 64 = 0.069 bytes/cycle.

5.4.6

Instruction bandwidth: (0.0030 * 64) * 0.67 = 0.13 bytes/cycle.
Data read bandwidth: 0.02 * (0.17 +0.067) *64 = 0.22 bytes/cycle.
Total read bandwidth: 0.35 bytes/cycle.
Data write bandwidth: 0.067 * 4 = 0.27 bytes/cycle.
Write-back cache, the data write bandwidth: 0.02 * 0.30 * (0.17+0.067) * 64 = 0.091 bytes/cycle.

ANS:

5.6

5.6.1

P1: 1.52GHz; P2: 1.11GHz

5.6.2

P1: 6.31ns; P2: 5.11ns

5.6.3

P1: 12.64 CPI, 8.34 ns/instr; P2: 7.36 CPI, 6.63 ns/inst

P2 is faster.

5.6.4

6.5ns, worse

5.6.5

13.04

5.6.6

P1 AMAT = .66 +.08 * 70 = 6.26ns

P2 AMAT = .90 +.06 * (5.62+.95*70) = 5.23ns

P2 is faster.

So P1 need to match P2’s performance.

5.23 = .66 +MR*70

MR = 6.5%

5.11

5.11.1

Address	Virtual Page	TLB H/M	TLB			
			Valid		Tag	Physical Page
			Value	Last access		
4669	1	TLB miss	1		11	12
		PT hit	1		7	4
		PF	1		3	6
			1	0	1	13
2227	0	TLB miss	1	1	0	5
		PT hit	1		7	4
			1		3	6
			1	0	1	13
13916	3	TLB hit	1	1	0	5
			1		7	4
			1	2	3	6
			1	0	1	13
34587	8	TLB miss	1	1	0	5
		PT hit	1	3	8	14
		PF	1	2	3	6
			1	0	1	13
48870	11	TLB miss	1	1	0	5
		PT hit	1	3	8	14
			1	2	3	6
			1	4	11	12
12608	3	TLB hit	1	1	0	5
			1	3	8	14
			1	5	3	6
			1	4	11	12
49225	12	TLB miss	1	6	12	15
		PT miss	1	3	8	14
			1	5	3	6
			1	4	11	12

5.11.2

Address	Virtual Page	TLB H/M	TLB			
			Valid		Tag	Physical Page
			Value	Last access		
4669	0	TLB miss	1		11	12
		PT hit	1		7	4
			1		3	6
			1	0	0	5
2227	0	TLB hit	1		11	12
			1		7	4
			1		3	6
			1	1	0	5
13916	0	TLB hit	1		11	12
			1		7	4
			1		3	6
			1	2	0	5
34587	2	TLB miss	1	3	2	13
		PT hit	1		7	4
		PF	1		3	6
			1	2	0	5
48870	2	TLB hit	1	4	2	13
			1		7	4
			1		3	6
			1	2	0	5
12608	0	TLB hit	1	4	2	13
			1		7	4
			1		3	6
			1	5	0	5
49225	3	TLB hit	1	4	2	13
			1		7	4
			1	6	3	6
			1	5	0	5

說明：較大的 page size 會降低 TLBmiss rate，但會導致更高的 fragmentation 和更低的 utilization of the physical memory。

5.11.3

Two-way set associative

Address	Virtual Page	Tag	Index	TLB H/M	TLB				
					Valid		Tag	Physical Page	Index
					Value	Last access			
4669	1	0	1	TLB miss	1		11	12	0
				PT hit	1		7	4	1
				PF	1		3	6	0
					1	0	0	13	1
2227	0	0	0	TLB miss	1	1	0	5	0
				PT hit	1		7	4	1
					1		3	6	0
					1	0	0	13	1
13916	3	1	1	TLB hit	1	1	0	5	0
				PT hit	1	2	1	6	1
					1		3	6	0
					1	0	1	13	1
34587	8	4	0	TLB miss	1	1	0	5	0
				PT hit	1	2	1	6	1
				PF	1	3	4	14	0
					1	0	1	13	1
48870	11	5	1	TLB miss	1	1	0	5	0
				PT hit	1	2	1	6	1
					1	3	4	14	0
					1	4	5	12	1
12608	3	1	1	TLB hit	1	1	0	5	0
					1	5	1	6	1
					1	3	4	14	0
					1	4	5	12	1
49225	12	6	0	TLB miss	1	6	6	15	0
				PT miss	1	5	1	6	1
					1	3	4	14	0
					1	4	5	12	1

Direct mapped

Address	Virtual Page	Tag	Index	TLB H/M	TLB				
					Valid		Tag	Physical Page	Index
					Value	Last access			
4669	1	0	1	TLB miss	1		11	12	0
				PT hit	1		0	13	1
				PF	1		3	6	2
					0		4	9	3
2227	0	0	0	TLB miss	1		0	5	0
				PT hit	1		0	13	1
					1		3	6	2
					0		4	9	3
13916	3	0	3	TLB miss	1		0	5	0
				PT hit	1		0	13	1
					1		3	6	2
					1		0	6	3
34587	8	2	0	TLB miss	1		2	14	0
				PT hit	1		0	13	1
				PF	1		3	6	2
					1		0	6	3
48870	11	2	3	TLB miss	1		2	14	0
				PT hit	1		0	13	1
					1		3	6	2
					1		2	12	3
12608	3	0	3	TLB miss	1		2	14	0
				PT hit	1		0	13	1
					1		3	6	2
					1		0	6	3
49225	12	3	0	TLB miss	1		3	15	0
				PT miss	1		0	13	1
					1		3	6	2
					1		0	6	3

所有 memory references 必須對 page table 交叉參照，並且 TLB 允許在沒有 access off-chip memory 的情況下執行此般操作。另外，如果沒有 TLB，memory access time 會顯著增加。

5.11.4

假設 half the memory available

The tag size is 32 - lg(8192) = 19 bits.

All five page tables would require 5 * (2^19/2 * 4) bytes = 5 MB

5.11.5

Each of the second-level tables contain 2^(19-8) = 2048 entries, requiring 2048 * 4 = 8 KB

Covering 2048 * 8 KB = 16 MB (2^24) of the virtual address space.

Minimum amount:

The second-level tables: 5 * (2^31 /2^24) * 8 KB = 5 MB.

The first-level tables would require an additional: 5 * 128 * 6 bytes = 3840 bytes.

Maximum amount:

The second-level tables: 5 * 256 * 8 KB =10 MB

The first-level tables: 7680 bytes

5.11.6

16 KB direct-mapped cache

2-words per block

⇨ 8-byte blocks

⇨ 16 KB / 8 bytes = 2048 blocks

Index field would span address bits 13 to 3

11 bits to index

1 bit word off set

2 bit byte off set

⇨ The tag LSB of the cache tag is address bit 14.

使用 cache 2-way associative to 增加 its size to 16 KB.

5.12

5.12.1

Worse case = 2^31 entries

需要 2^31 * 4 bytes = 8 GB

5.12.2

Each level of the page table to fit in one page, so 4 KiB/4B = 1 K entries, using 10 bits each. So, there are 31 bits of virtual page number, requiring 4 levels of page tables. Each address translation will take 4 memory accesses.

5.12.3

在 inverted page table 中，PTE 的數量可以減少到 hash table 的大小加上 collisions 的成本。

在這種情況下，提供 TLB miss 需要 extra reference 來比較存儲在 hash table 的一個或多個 tags。

舉例來說：3 or fewer PTEs will be required to store the page table as there are only 3 valid entry-ids.

5.12.4

Paged out to disk

5.12.5

TLB miss

The software can pre-fetch TLB entries

5.12.6

Interrupt would be generated because the page is marked as read only.

5.14

5.14.1

Shadow page table：

（1）VM 創建 page table，hypervisor 更新 Shadow page;

（2）None

（3）hypervisor 攔截 page fault，創建新的 mapping，並使 TLB 中的舊 mapping 無效;

（4）VM 通知 hypervisor 使進程的 TLB 條目無效。

Nested page table：

（1）VM 創建新的 page table，hypervisor 在 PA 到 MA 表中添加新的 mapping。

（2）硬件遍歷兩個 page table 以將 VA 轉換為 MA;

（3）VM 和 hypervisor 更新其 page table，hypervisor 使過時的 TLB 條目無效;

（4）與 Shadow page table 相同。

5.14.2

Native: 4; NPT: 24 (instructors can change the levels of page table)

By Native: L; NPT: L*(L+2)

5.14.3

Shadow page table: page fault rate.

NPT: TLB miss rate.

5.14.4

Shadow page table: 1.03

NPT: 1.04

5.14.5

Combining multiple page table updates

5.14.6

NPT caching (similar to TLB caching)