
STM32
CubeMX

1. Description

1.1. Project

Project Name	Robot_Car_RTOS_
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 6.1.1
Date	05/24/2021

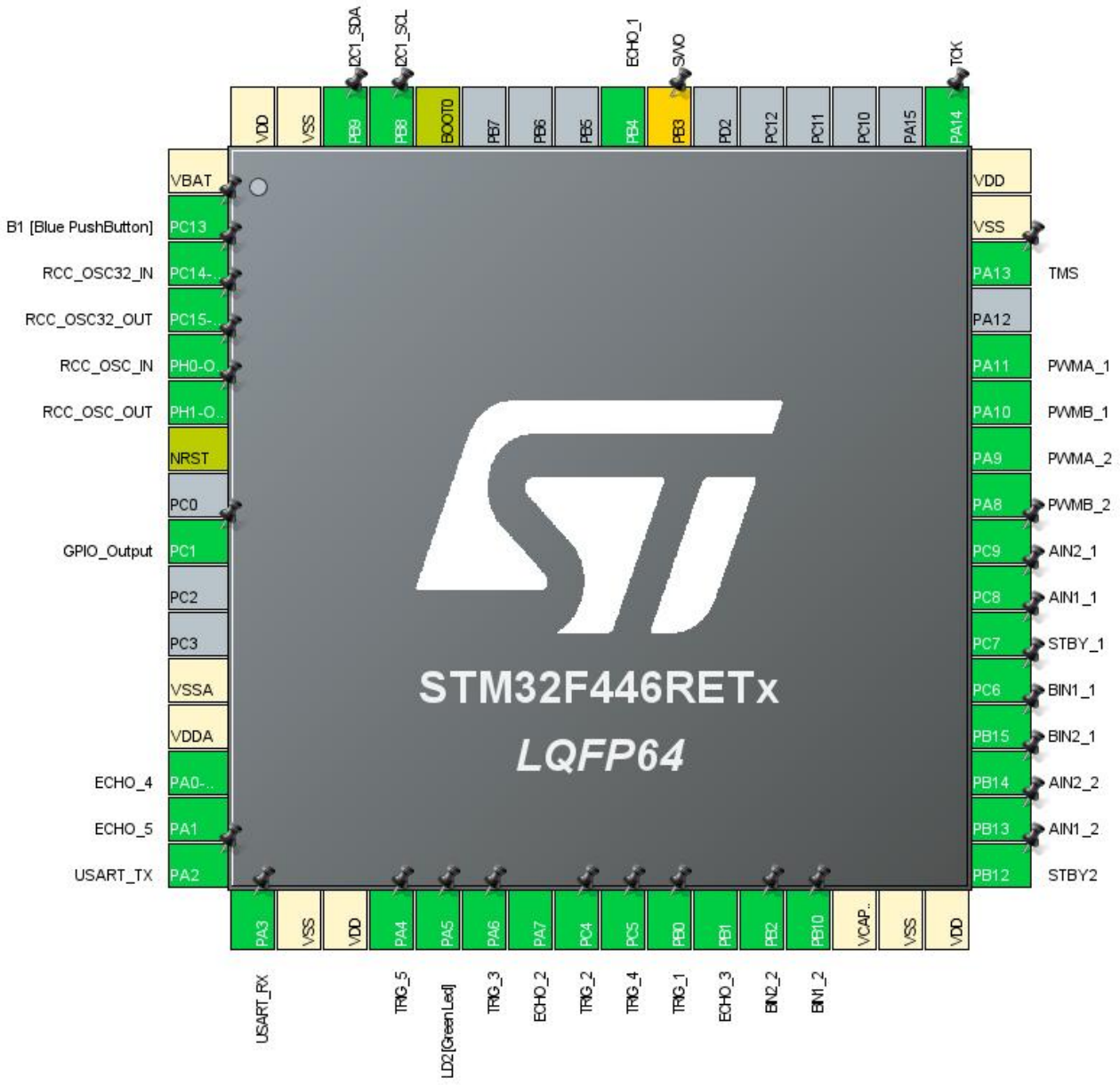
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

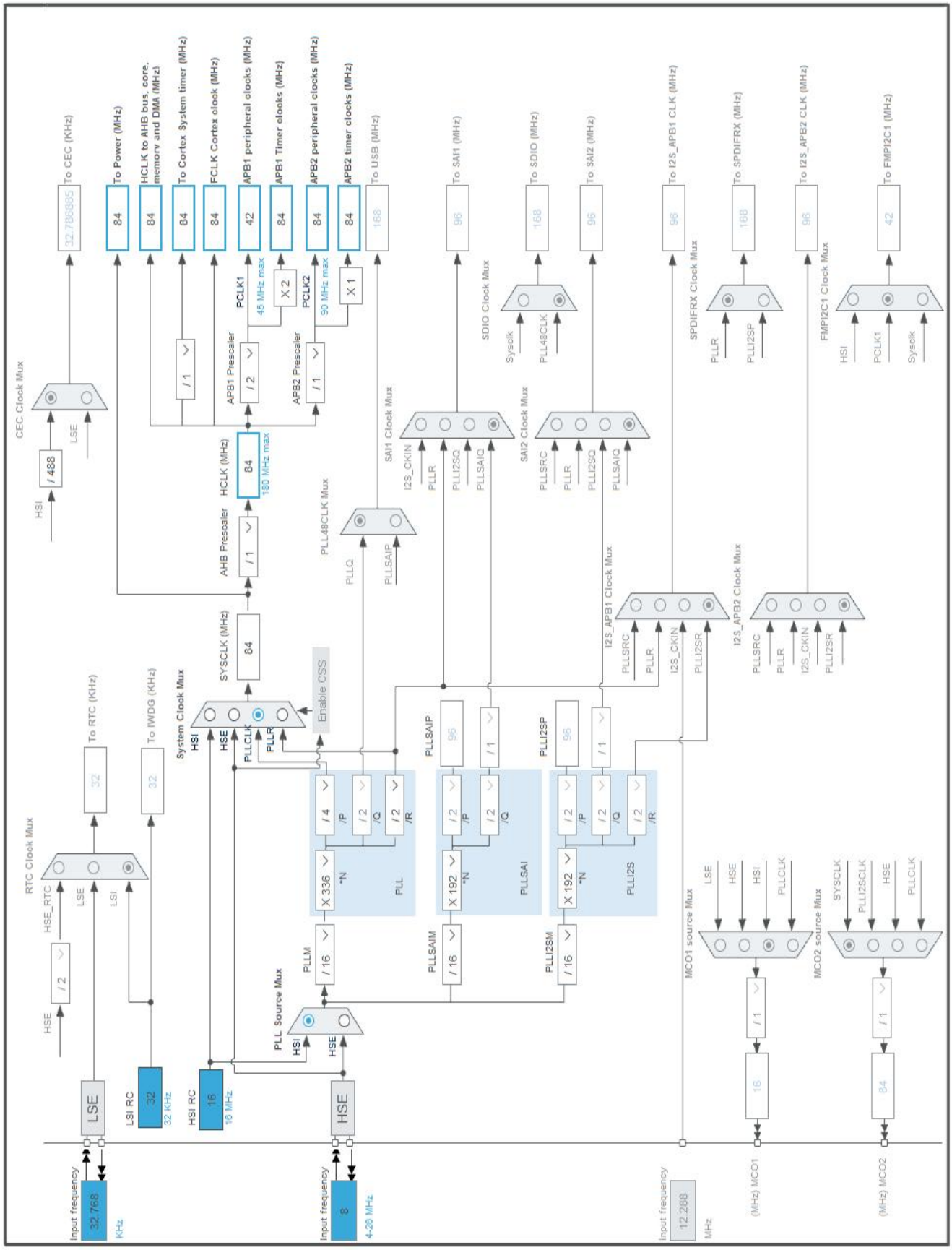
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
9	PC1 *	I/O	GPIO_Output	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM5_CH1	ECHO_4
15	PA1	I/O	TIM5_CH2	ECHO_5
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	TRIG_5
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6 *	I/O	GPIO_Output	TRIG_3
23	PA7	I/O	TIM3_CH2	ECHO_2
24	PC4 *	I/O	GPIO_Output	TRIG_2
25	PC5 *	I/O	GPIO_Output	TRIG_4
26	PB0 *	I/O	GPIO_Output	TRIG_1
27	PB1	I/O	TIM3_CH4	ECHO_3
28	PB2 *	I/O	GPIO_Output	BIN2_2
29	PB10 *	I/O	GPIO_Output	BIN1_2
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	STBY2
34	PB13 *	I/O	GPIO_Output	AIN1_2
35	PB14 *	I/O	GPIO_Output	AIN2_2
36	PB15 *	I/O	GPIO_Output	BIN2_1
37	PC6 *	I/O	GPIO_Output	BIN1_1
38	PC7 *	I/O	GPIO_Output	STBY_1
39	PC8 *	I/O	GPIO_Output	AIN1_1

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PC9 *	I/O	GPIO_Output	AIN2_1
41	PA8	I/O	TIM1_CH1	PWMB_2
42	PA9	I/O	TIM1_CH2	PWMA_2
43	PA10	I/O	TIM1_CH3	PWMB_1
44	PA11	I/O	TIM1_CH4	PWMA_1
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
56	PB4	I/O	TIM3_CH1	ECHO_1
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Robot_Car_RTOS_
Project Folder	C:\Users\henca\git\Robot_Car_RTOS_\Robot_Car_RTOS_
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM1_Init	TIM1
4	MX_USART2_UART_Init	USART2
5	MX_TIM4_Init	TIM4
6	MX_I2C1_Init	I2C1
7	MX_TIM3_Init	TIM3
8	MX_TIM5_Init	TIM5

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

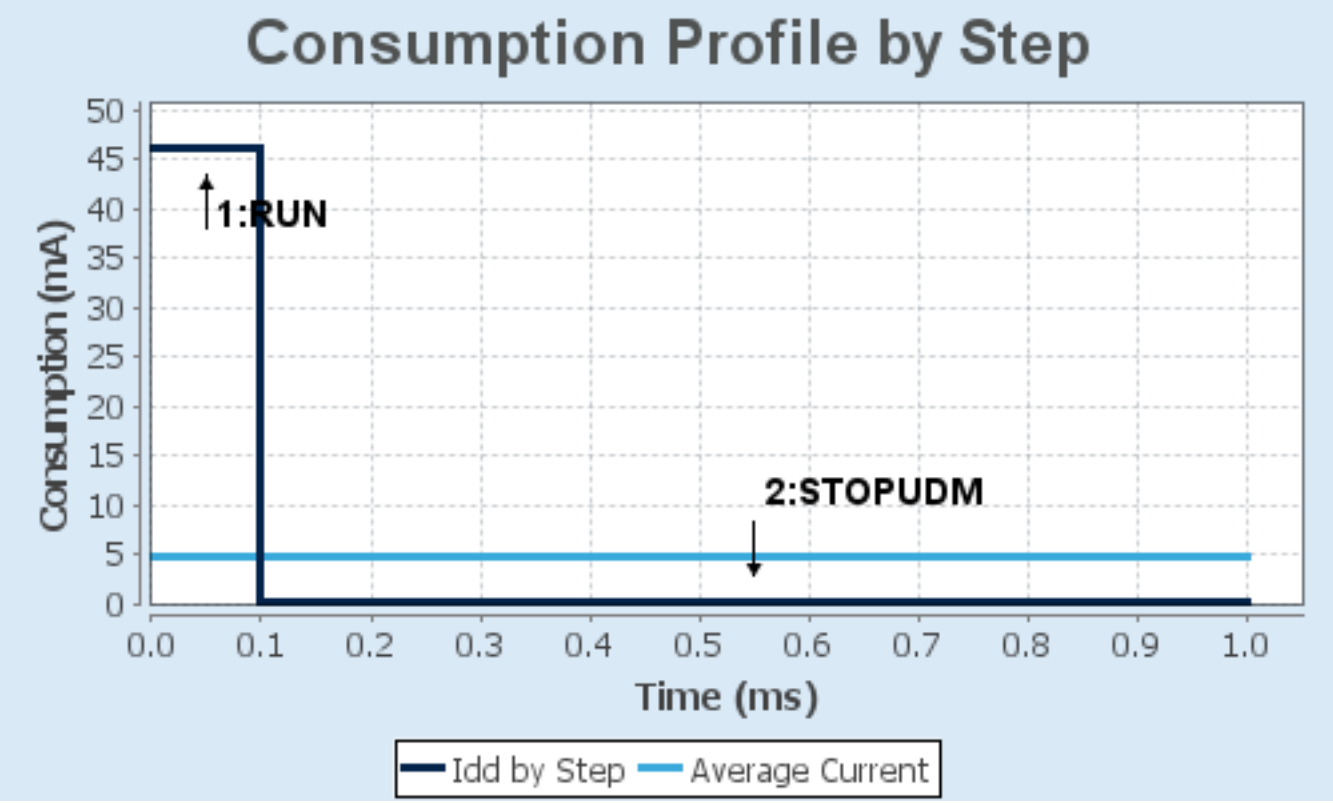
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/PREFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 3
Power Over Drive	Disabled

7.3. SYS

Debug: Serial Wire

Timebase Source: TIM2

7.4. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1292 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**255 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**2000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**2000 ***

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**2000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**2000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.5. TIM3

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel4: Input Capture direct mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	**Both Edges ***
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

Input Capture Channel 2:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

Input Capture Channel 4:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

7.6. TIM4
mode: Clock Source
7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.7. TIM5
Channel1: Input Capture direct mode
Channel2: Input Capture direct mode
7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**65535 ***

Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

Input Capture Channel 2:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

7.8. USART2

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.9. FREERTOS

Interface: CMSIS_V1

7.9.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.9.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.9.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	PWMB_2
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	PWMA_2
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	PWMB_1
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	PWMA_1
TIM3	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ECHO_2
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	ECHO_3
	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ECHO_1
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ECHO_4
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ECHO_5
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_RX
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG_5
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG_3
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG_2
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG_4
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG_1
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BIN2_2
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BIN1_2
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STBY2
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AIN1_2
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AIN2_2
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BIN2_1
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BIN1_1
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STBY_1
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AIN1_1
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AIN2_1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false

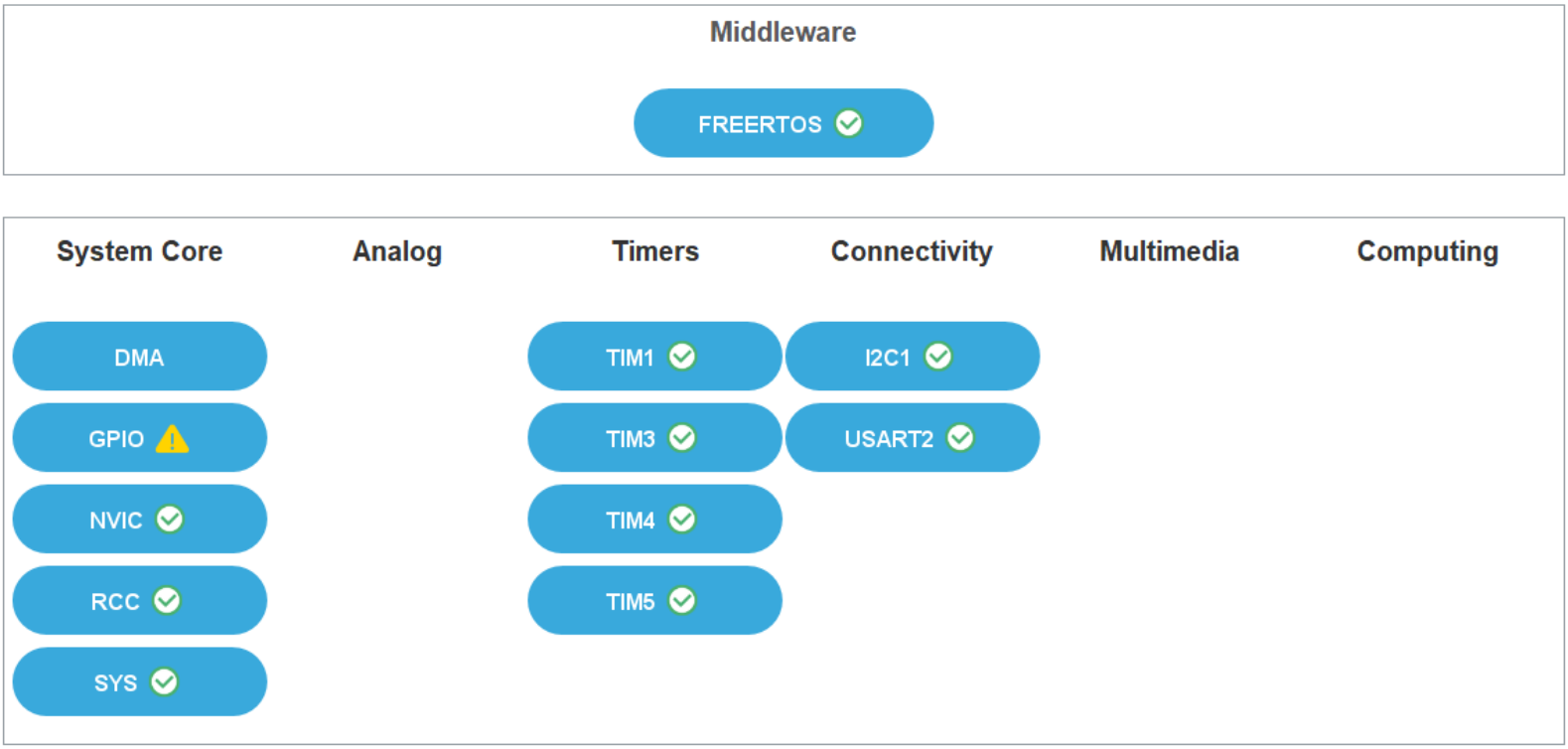
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00141306.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00135183.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00155929.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00161778.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf