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INTUITIVE



BRKARC-2003

# Cisco ASR 9000 System Architecture

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# Agenda

- ASR9000 Products Introduction
- ASR9000 System Hardware Architecture
- ASR9000 Distributed Control Plane
- Data Packet Processing & QoS
- ASR9000 TCAM Architecture and Partition
- IOS-XR & IOS-XR 64 Bit
- Conclusion

# ASR 9000 Products

## Introduction

# Cisco ASR 9000 System Comprehensive Portfolio

Compact & Powerful Access/Aggregation	Flexible Service Edge	High Density Service Edge and Core				
<ul style="list-style-type: none"><li>Small footprint with full IOS-XR for distributed environments</li></ul>	<ul style="list-style-type: none"><li>Optimized for ESE and MSE with high M-D scale for medium to large sites</li></ul>	<ul style="list-style-type: none"><li>Scalable, ultra high density service routers for large, high-growth sites</li></ul>				
<b>One Platform, One OS, One Family</b>						
nV Satellites ASR 9000v, NCS5000 	ASR 9006 ASR 9006 (highlighted)  4 LC/10RU 7 Tbps	ASR 9912 ASR 9912 (highlighted)  20 LC/44RU 160 Tbps				
ASR 9901  456Gbps ASR 9001  Fixed 2RU 240 Gbps	ASR 9004  2 LC/6RU 16 Tbps	ASR 9006 ASR 9006 (highlighted)  4 LC/14RU 32 Tbps	ASR 9910 ASR 9910 (highlighted)  8 LC/21RU 14 Tbps	ASR 9910 ASR 9910 (highlighted)  8 LC/21RU 64 Tbps	ASR 9922  10 LC/30RU 80 Tbps	
MSE	E-MSE	Peering	P/PE	CE	Mobility	Broadband

# ASR 9000 Switch Fabric Overview

Integrated fabric/RP/LC



9901 2RU, 45G

Fabric is integrated on RSP



9904  
RSP880: 1.4T/slot  
RSP5: 3.6T/slot



RSP880: 800G/slot  
RSP5: 1.8T/slot

Integrated + Separated Fabric  
6+1 redundancy



9906  
RSP880+SFC2: 1.4Tb/slot  
RSP5+SFC3: 4.2T/slot



Separated fabric card

6+1 redundancy



9912

RSP880+SFC2: 1.4Tb/slot  
RSP5+SFC3: 4.2T/slot

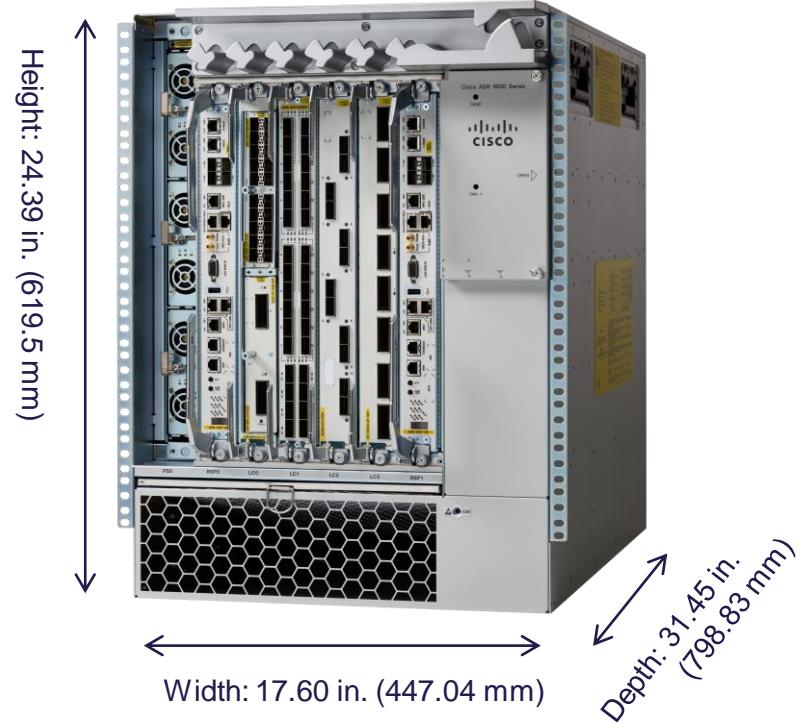


9922

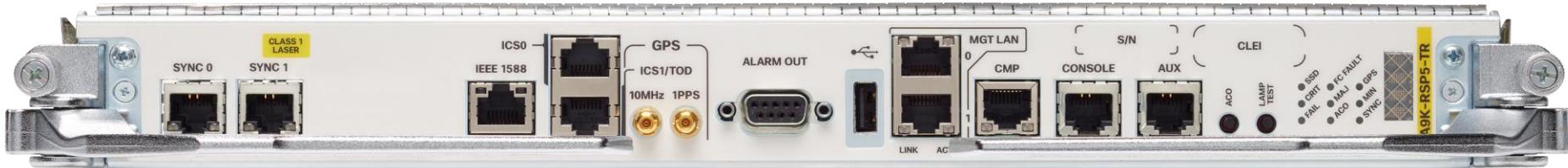
# Cisco ASR 9906 Overview



Feature	Description
Total Capacity	>32T
Capacity per Slot	>4T
Slots	6 slots - 4 Line Cards and 2 RSPs
Rack size	14RU, with native front-to-back airflow. Note: the ASR 9006 is (10RU), but with baffle it is approximately 14RU also.
Power	1 Power Tray 4.4 KW DC supplies (max 4) 6.0 KW AC supplies (max 3)
Fan	Front-to-Back Airflow 2 Fan Trays, FRU
RSPs	Integrated Fabric, 1+1 Redundancy
Fabric Cards	5 Fabric cards on rear of chassis for additional capacity 230G per FC at FCS Up to 6+1 Redundancy using RSP's integrated fabric
Line cards	Tomahawk Lightspeed Service Card: VSM with 32-bit XR support only



# RSP5/RP3 Front Panel Configuration



- 2x BITS ports on RJ-45
- 100Mbps, 1588 port – RJ-45
- TOD – RJ-45
- 10Mhz on SMA
- 1x CMP
- 1PPS on SMA
- Alarm output serial port
- USB
- 2x Management ports on RJ-45
- AUX & Console on RJ-45 connectors
- LED's for major/critical and normal oper alarms or states

# Route Switch Processors and Route Processors

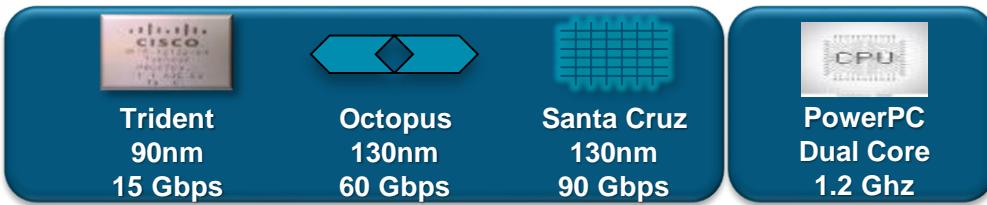
RSP used in ASR9910/9906/9904/9006/9010, RP in ASR9922/9912

	RSP880 A99-RSP	RP2	RSP5	RP3
Description	3 <sup>rd</sup> Gen RP and Fabric ASIC		4 <sup>th</sup> Gen RP and Fabric ASIC	
Switch Fabric Bandwidth	800G/slot (9006/9010) 1.4T/slot (9904) 1.4T/slot (9906/9910)	1.4T/slot (separated fabric card) (9912/9922)	1.8T/slot (9006/9010) 3.6T/slot (9904) 4.2T/slot (9906/9910)	4.2T/slot (separated fabric card) (9912/9922)
Processor	Intel x86 (Ivy Bridge EP) 8 Core 2GHz		Intel x86 (Skylake EP) 8 Core 2GHz	
RAM	-TR: 16GB -SE: 32GB		-TR: 16GB -SE: 40GB	
SSD	2 x 32GB Slim SATA		2 x 128GB Slim SATA	
Punt BW	40GE		40GE	

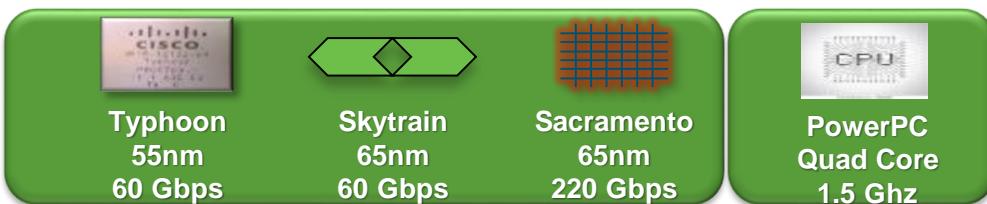
# ASR9000 Edge Linecard Silicon Evolution



1<sup>st</sup> Gen  
Trident 120G



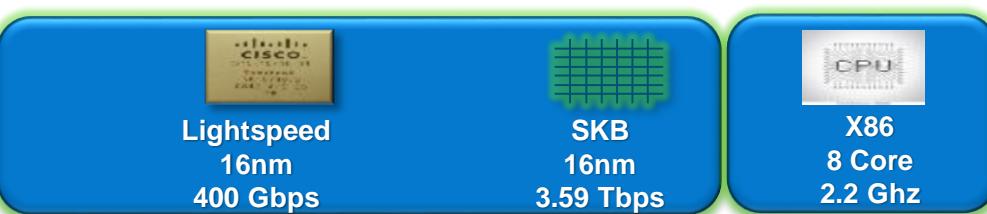
2<sup>nd</sup> Gen  
Typhoon 360G



3<sup>rd</sup> Gen  
Tomahawk 1.2T



4<sup>th</sup> Gen  
Lightspeed 3.2T



# ASR 9000 3rd Ethernet Line Card Overview



MPAs  
20x1GE  
2x10GE  
4x10GE  
1x40GE  
2x40GE

MPAs  
1x100GE  
2x100GE  
20x10GE



MPA  
32x1GE



3<sup>rd</sup> gen LC  
Tomahawk NPU:  
240Gbps,  
~150Mpps



A9K-4x100GE

A9K-8x100GE  
A99-12x100GE

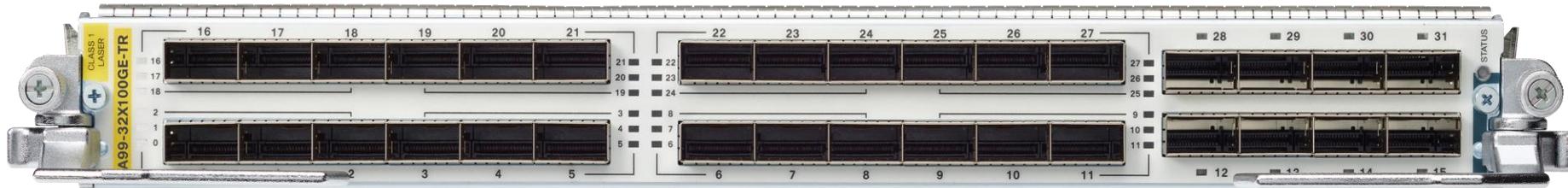


-TR, -SE

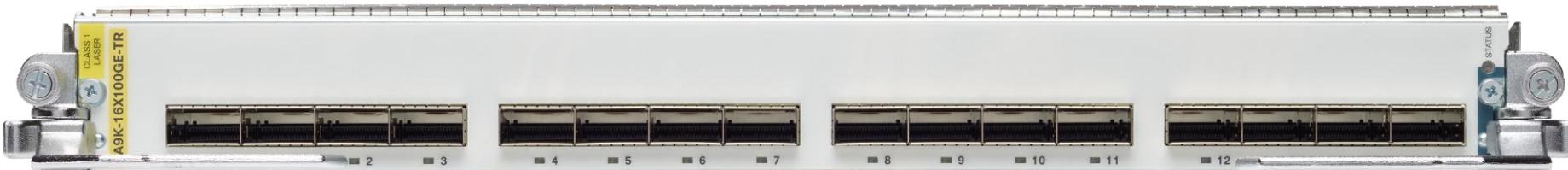
A9K-48X10GE-1G

MOD400/MOD200  
A9K-400G-DWDM

# ASR9000 4<sup>th</sup> Generation Line Card Overview



A99-32X100GE-TR



A9K-16X100GE-TR

# Pop Quiz ????

What is the difference between RP3 and RSP5?

- The same
- RSP5 can only be used in ASR9000 Chassis
- RP3 can only be used in ASR9900 Chassis
- RSP5 is integrated with switch fabric but RP3 is not.

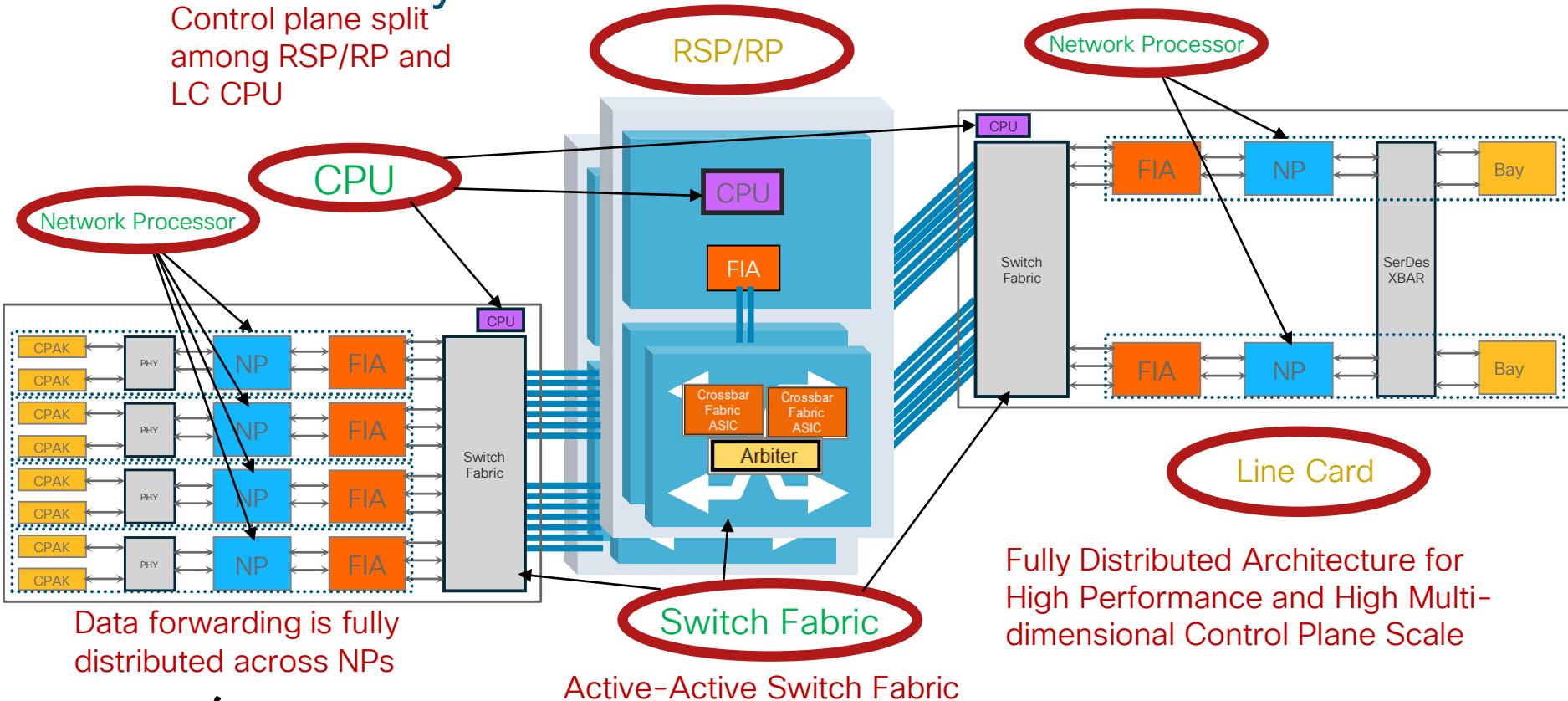


# ASR9000 Hardware Architecture



# ASR 9000 System Architecture “At-a-Glance”

Control plane split  
among RSP/RP and  
LC CPU



# A99-32x100G-TR – Preparing for Zettabyte Era

## Innovation

Cisco NPU 4 in 1 (16nm): Integrated NPU, PHY, FIA, Memory

Native support for 10/25/40/100/400G

Integrated 100GE FEC

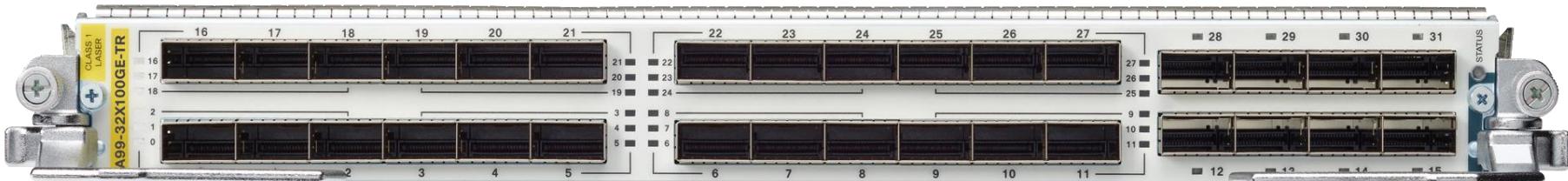
## Leading the Market

4 x capacity increase per system

10GE, 40GE, 100GE and 400GE densities w/ rich features

Hitless FPD upgrade possible (no LC reload)

Sub Sec ISSU



## Lower TCO

Low OPEX:

- Drastically lower power profile: ~ .5W/GE
- Improvement over Tomahawk w/ power down capability of the complete slice path including NP

Low CAPEX - Vortex and PAYG

## Scale

Ultra high control plane scale with eXR

HW acceleration for L2 classification, hashing, prefix lookup, ACL range compression, header re-write, flow ordering, statistics, policers, WRED

# ASR9000 32x1G MPA



- 16 x 1GE Ports with SFP

With SFPs in all slots															
SFP0	SFP1	SFP2	SFP3	SFP4	SFP5	SFP6	SFP7	SFP8	SFP9	SFP10	SFP11	SFP12	SFP13	SFP14	SFP15
0 1	2 3	4 5	6 7	8 9	10 11	12 13	14 15	16	17	18	19	20	21	22	23
▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲
31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15	14	13	12	11	10	9	8
SFP15	SFP14	SFP13	SFP12	SFP11	SFP10	SFP9	SFP8	SFP7	SFP6	SFP5	SFP4	SFP3	SFP2	SFP1	SFP0

32/16 x 1GE (CSFP/ SFP Optics)

MOD 200 & MOD 400 Linecards

32 Bit & 64 Bit IOS-XR



## 32 x 1GE Ports With CSFP

With all CSFP optics

CSFP0	CSFP1	CSFP2	CSFP3	CSFP4	CSFP5	CSFP6	CSFP7
0 1	2 3	4 5	6 7	8 9	10 11	12 13	14 15
▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲	▲▼▲▼▲
31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
CSFP15	CSFP14	CSFP13	CSFP12	CSFP11	CSFP10	CSFP9	CSFP8

CSFP – Dual Channel BiDi SFP – 2 ports per SFP Slot

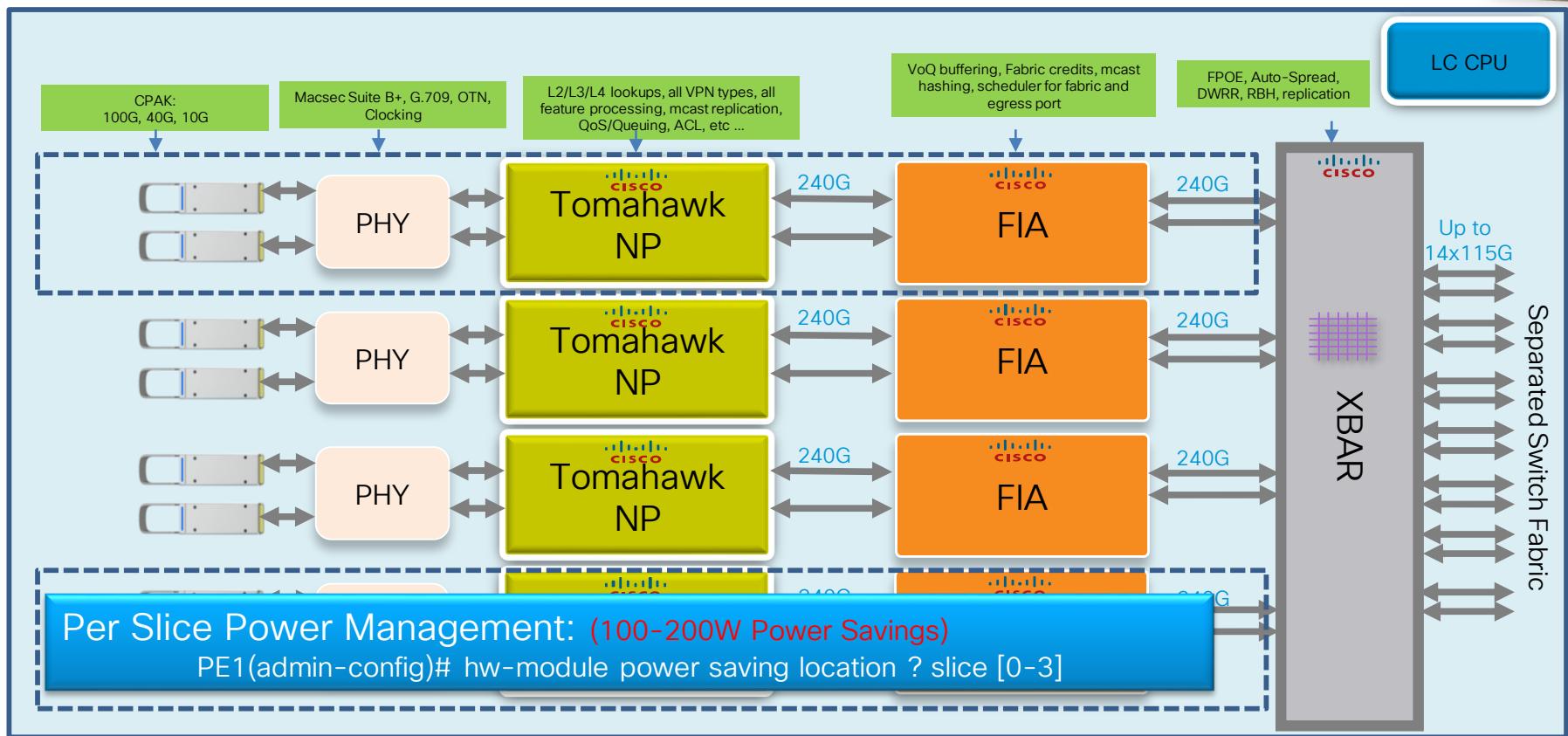
MAC-SEC

SyncE | 1588

AES128/256 Encryption

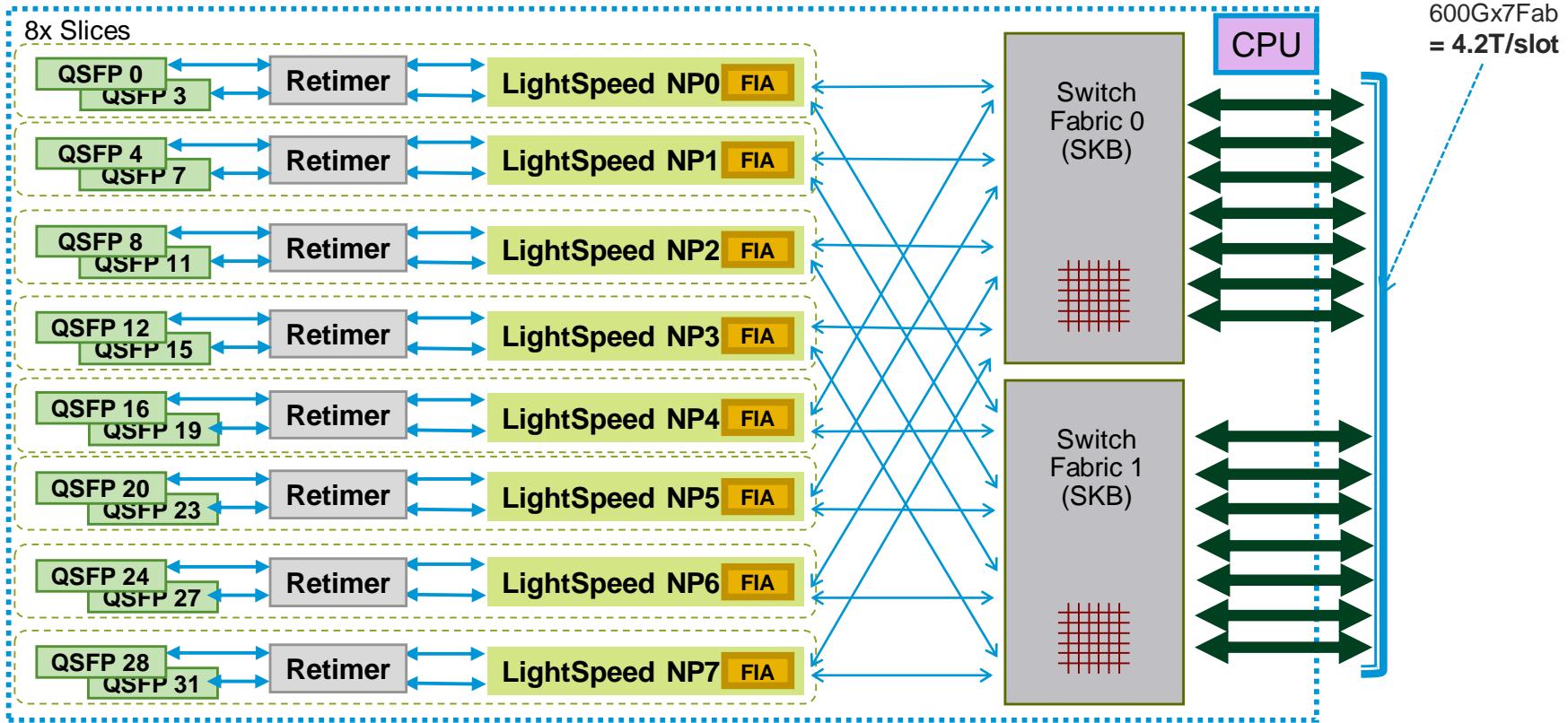
Combination of SFP and CSFP allowed

# ASR9000 Linecard Slice Based Architecture



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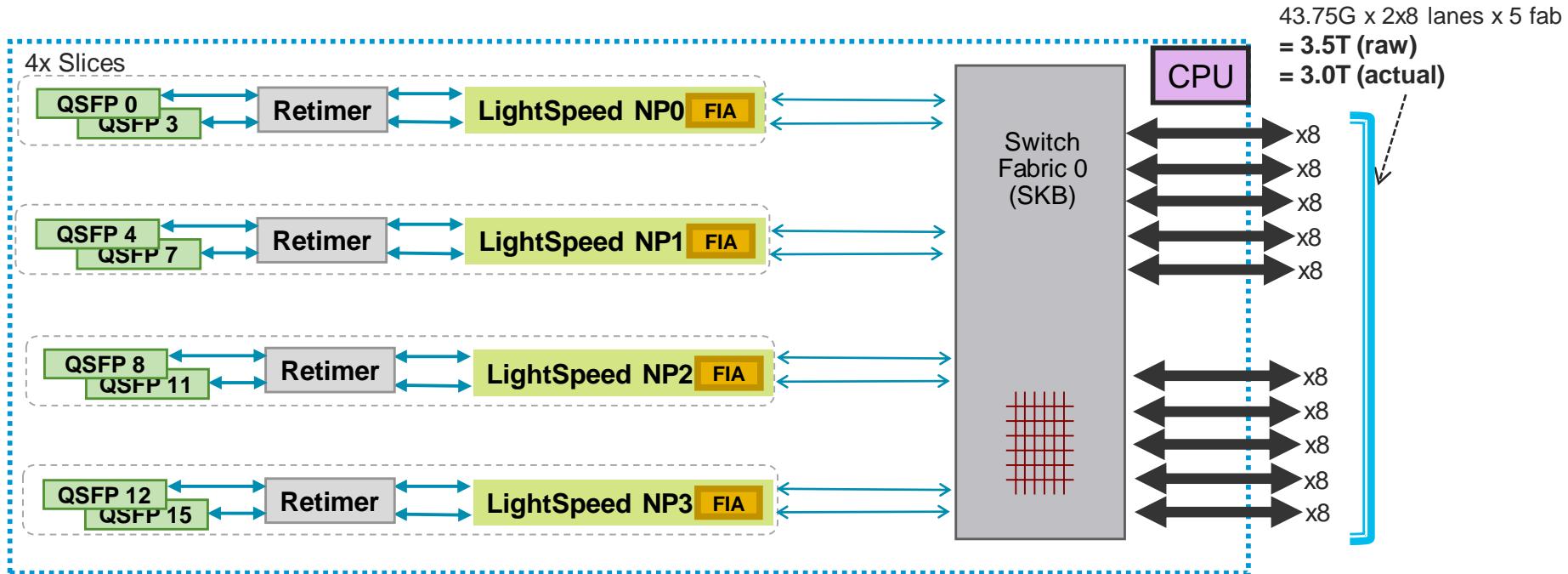
# 32x100GE (7-fabric) Linecard Architecture



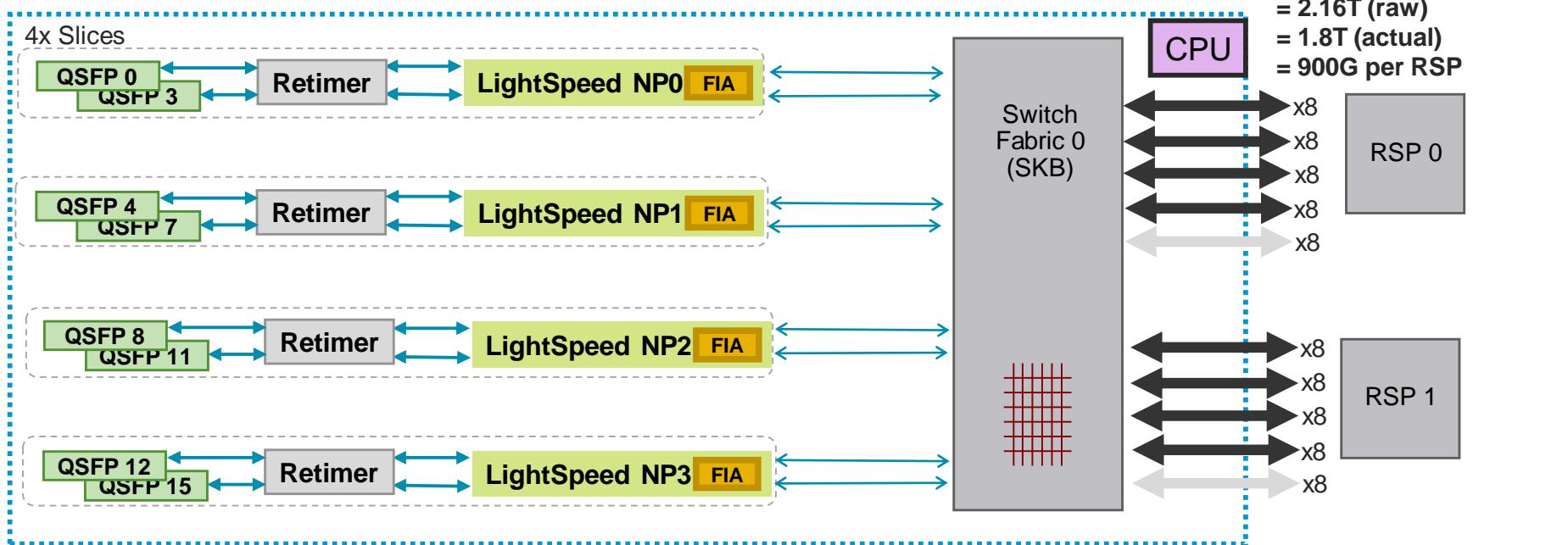
# 32x100GE (7-fabric) Linecard Architecture

- 3.2T linerate QSFP28 TR LAN linecard
- No hardware support for OTN, MACsec and FlexE
- 7-Fabric card
  - Works in 9922, 9912, 9910, 9906 & 9904 chassis
- Requires LightSpeed commons
  - RP3
  - SFC3
  - RSP5
- Linecard Performance
  - ASR 9922, 9912, 9910 & 9906 chassis
    - 3.2T linerate with fabric redundancy
  - ASR 9904 chassis
    - 3.2T linerate with dual RSP5
    - 1.8T throughput with single RSP5

# 16x100GE (5-fabric) Linecard Architecture (when used in 9922, 9912, 9910 & 9906)



# 16x100GE (5-fabric) Linecard Architecture (when used in 9010 & 9006)



# 16x100GE (5-fabric) Linecard Architecture

- 1.6T linerate QSFP28 TR LAN linecard
- 5-Fabric card
  - Works in all ASR9k modular chassis
- Linecard Performance with LightSpeed commons
  - ASR 9922, 9912, 9910 & 9906 chassis
    - 1.6T linerate with fabric redundancy
  - ASR 9904 chassis
    - 1.6T linerate with dual RSP5
    - 1.4T throughput with single RSP5
  - ASR 9010 & 9006 chassis
    - 1.6T linerate with dual RSP5
    - 900G throughput with single RSP5

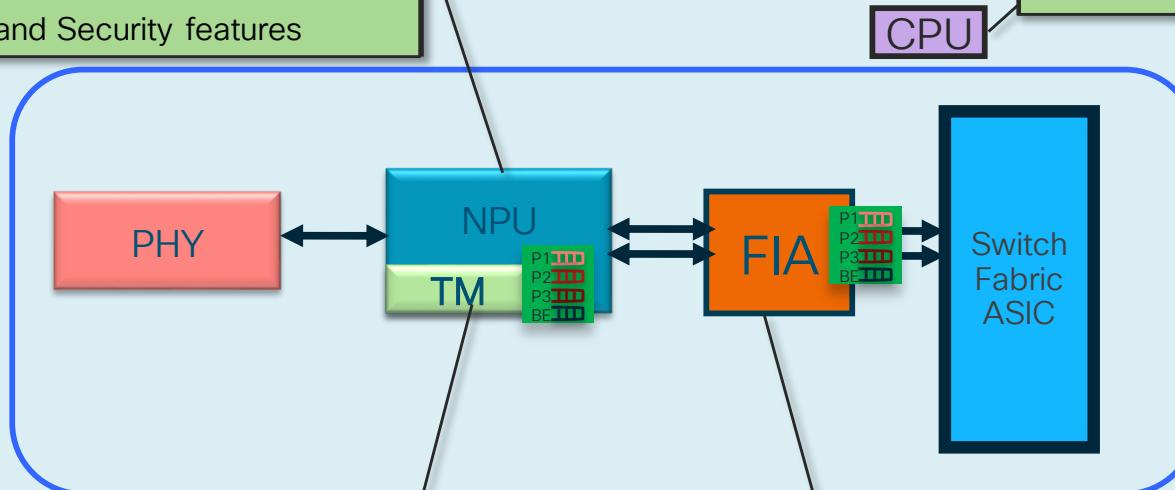
# Line Card Components

Main forwarding engine L2 and L3 lookups  
Multicast replication toward Optics  
User level QoS and Security features

Runs distributed control plane protocols for increased scale

BFD, CFM, ARP

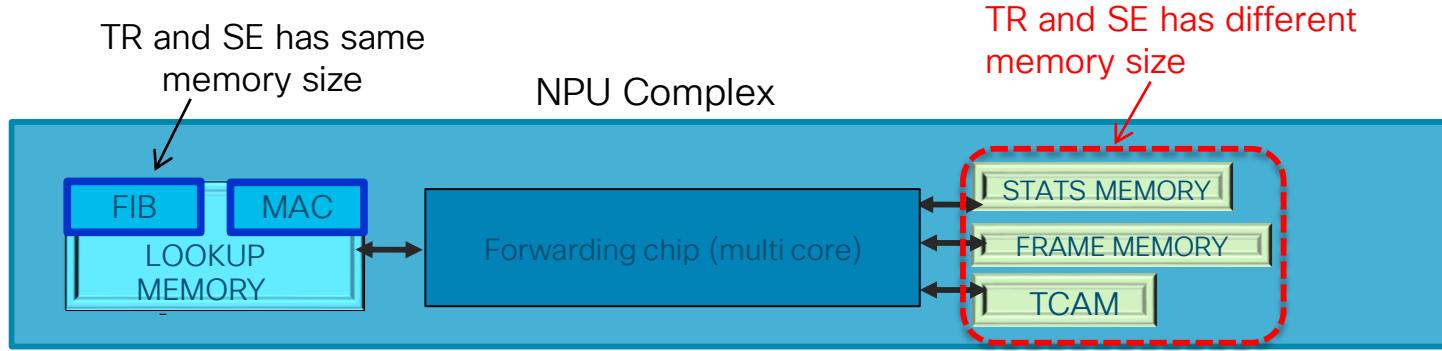
Receive FIB table from RP and program hardware forwarding table



Dedicated queue ASIC - TM (traffic manager) per NPU for QoS functions  
User Configurable Queue on TM.  
Default Port Queue Always Created.

Provides data connection to switch fabric  
Manage VoQ, Superframe and loadbalancing data traffic across switch fabric  
Mccast replication table for replication toward NPs

# Network Processor Architecture Details



- TCAM: VLAN tag, QoS and ACL classification
- Stats memory: interface statistics, forwarding statistics etc
- Frame memory: buffer, Queues
- Lookup Memory: forwarding tables, FIB, MAC, ADJ
- TR/SE
  - Different TCAM/frame/stats memory size for different per-LC QoS, ACL, logical interface scale
  - Same lookup memory for same system wide scale mixing different variation of LCs doesn't impact system wide scale

-TR: transport optimized, -SE: Service edge optimized

# ASR 9900 Switch Fabric High-Level Architecture

- 3-Stage Non-Blocking Fabric (Separate Unicast and Multicast Crossbars)

Fabric frame format:

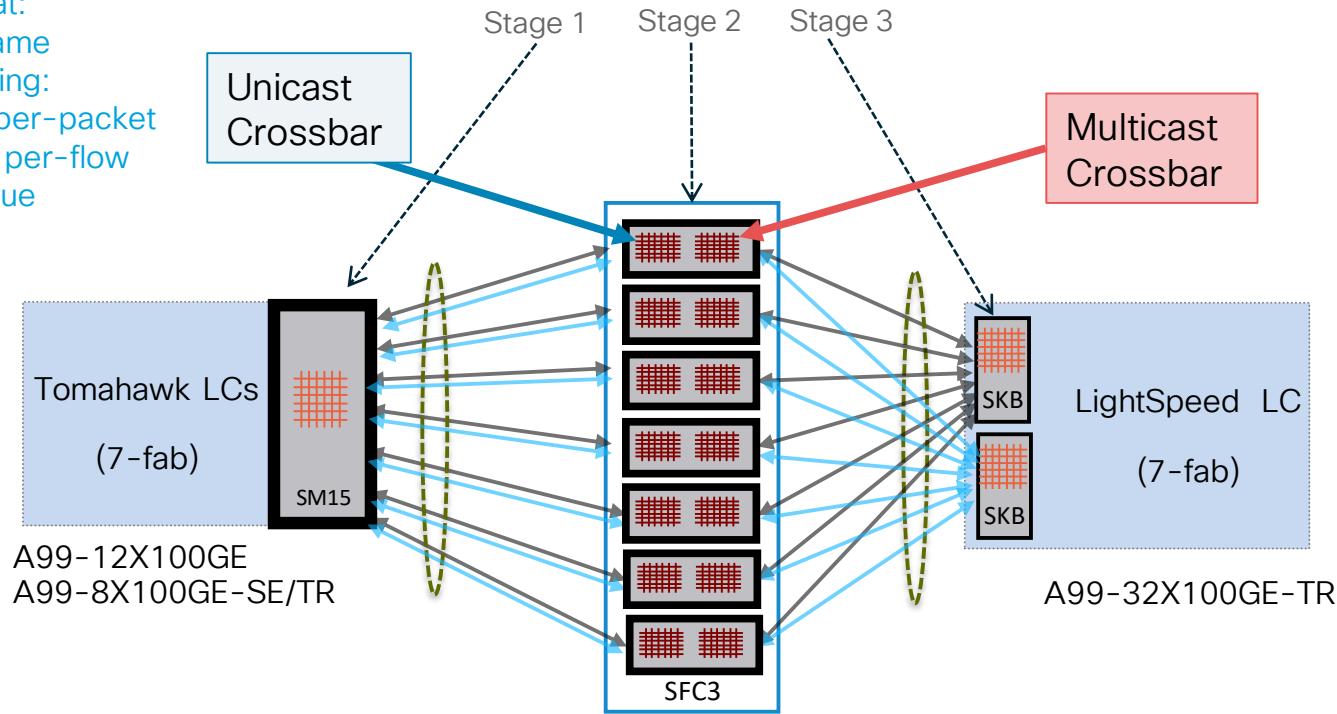
- Super-frame

Fabric load balancing:

- Unicast per-packet
- Multicast per-flow

Virtual Output Queue

Arbitration



# ASR 9000 Switch Fabric High-Level Architecture

- 3-Stage Non-Blocking Fabric (Separate Unicast and Multicast Crossbars)

Fabric frame format:

Super-frame

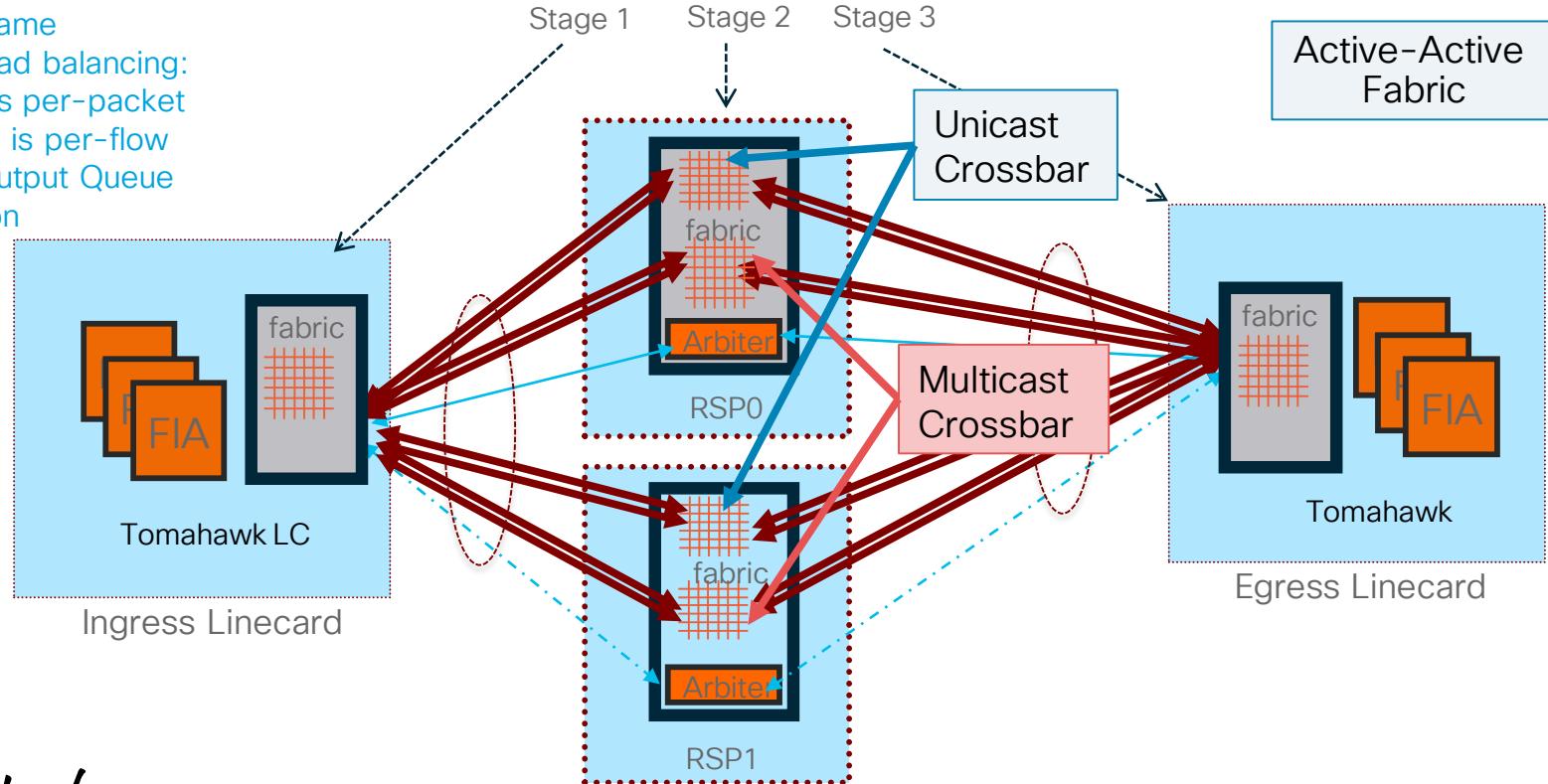
Fabric load balancing:

Unicast is per-packet

Multicast is per-flow

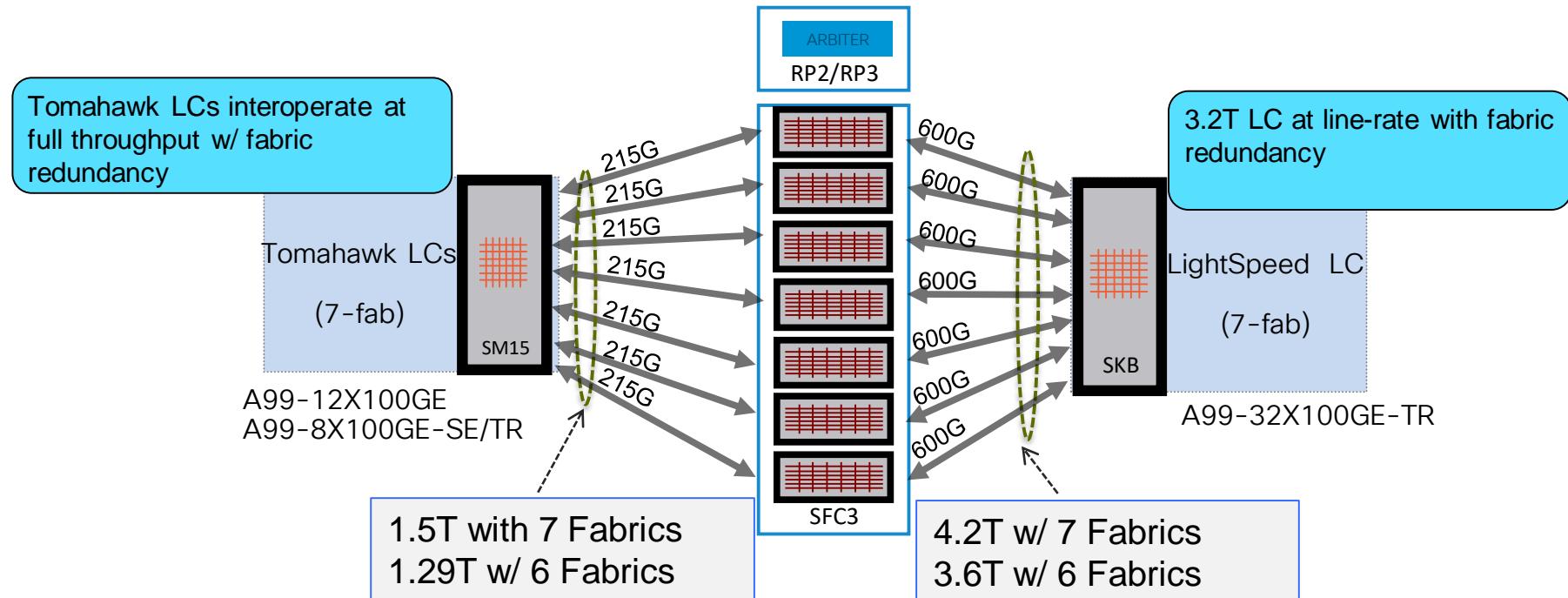
Virtual Output Queue

Arbitration



# ASR9922/12: 7-fabric System w/ LightSpeed and Tomahawk

- 7-fabric LCs use all 7 fabrics if all other LCs in the system are 7 fabric
- All LightSpeed and Tomahawk LCs in this mode interoperate at full BW



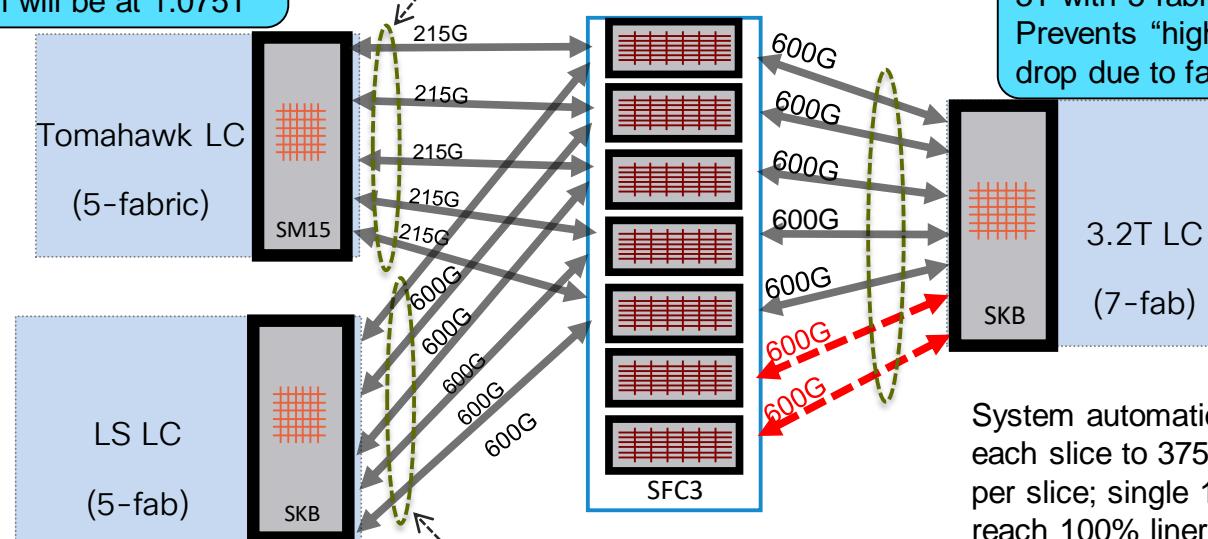
# ASR99xx: 5-fabric System w/ LightSpeed and Tomahawk

- 7-fabric LC uses 5 fabrics if there is a 5-fab LightSpeed or Tomahawk LCs in system

All Tomahawk LCs interoperate at full throughput w/ fabric redundancy; except for 12x100GE LC, which will be at 1.075T

1.0T with 5 fabrics  
860G w/ 4 fabrics

3T with 5-fabrics  
Prevents “high priority” packet drop due to fabric congestion



System automatically rate-limits each slice to 375G (93.75% linerate per slice; single 100G port can reach 100% linerate)

For 100G linerate on all ports:

- Shut down one slice

# Pop Quiz ????

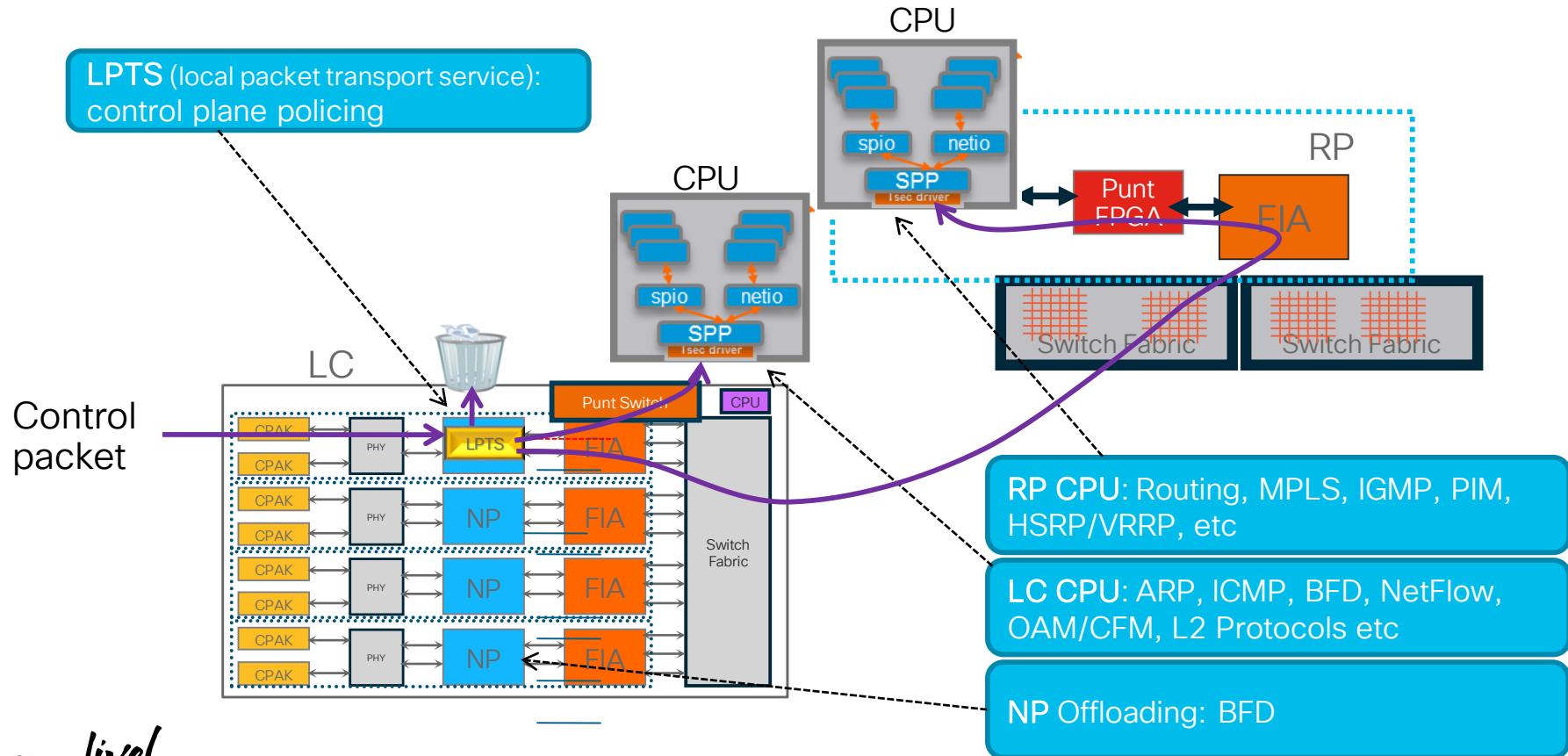
In a ASR9912 chassis with one A99-32x100G-TR and one A9K-16x100G-TR and seven SFC3 switch fabric running, what is the total switch fabric bandwidth available for the A99-32x100G-TR card?

- 4.2T
- 3.0T
- 1.0T

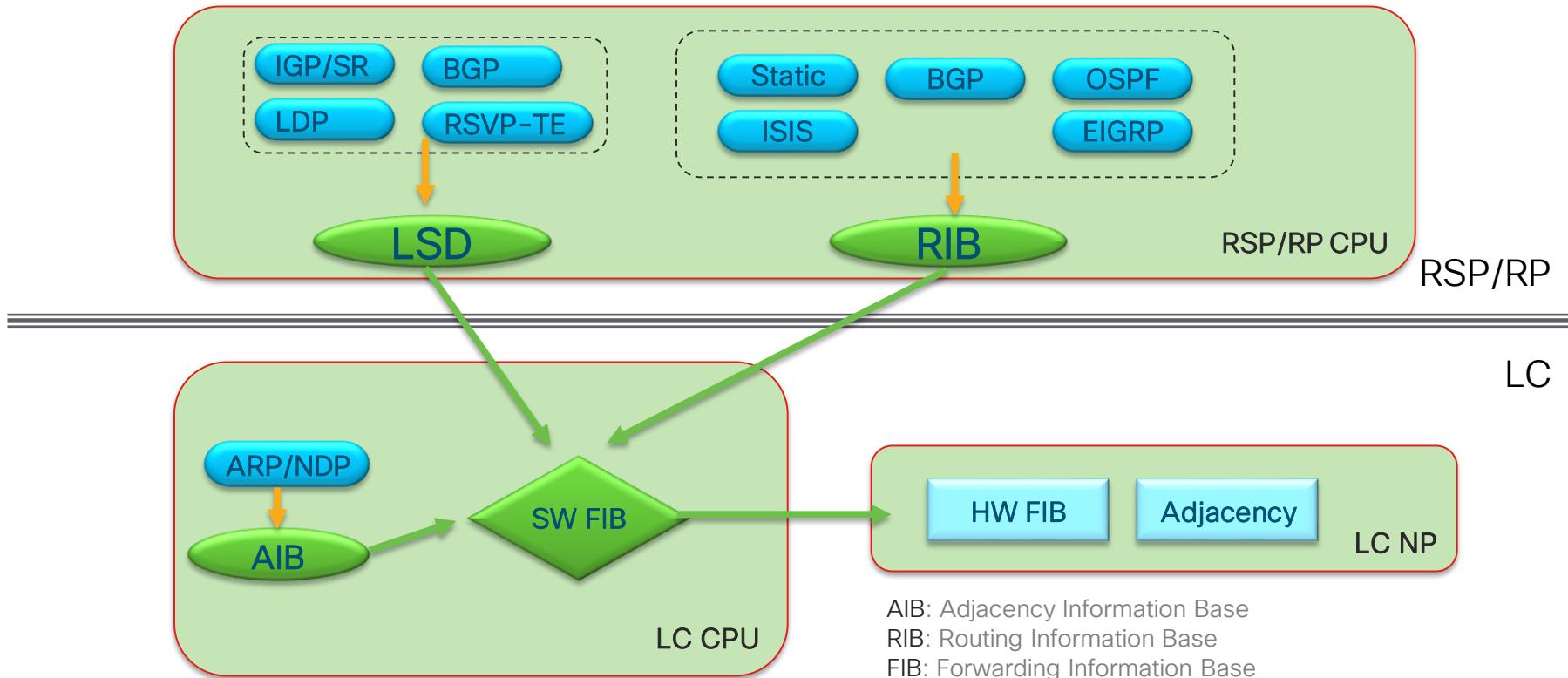


# ASR9000 Distributed Control Plane

# ASR9000 Fully Distributed Control Plane



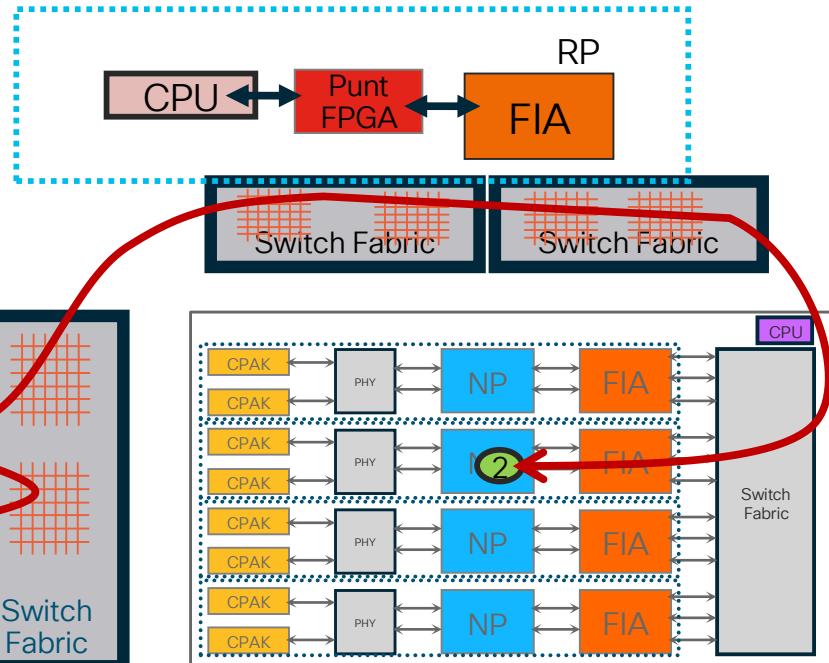
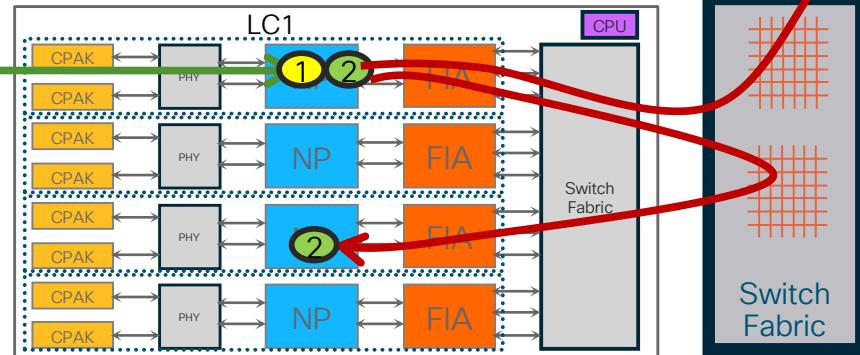
# L3 Control Plane Architecture



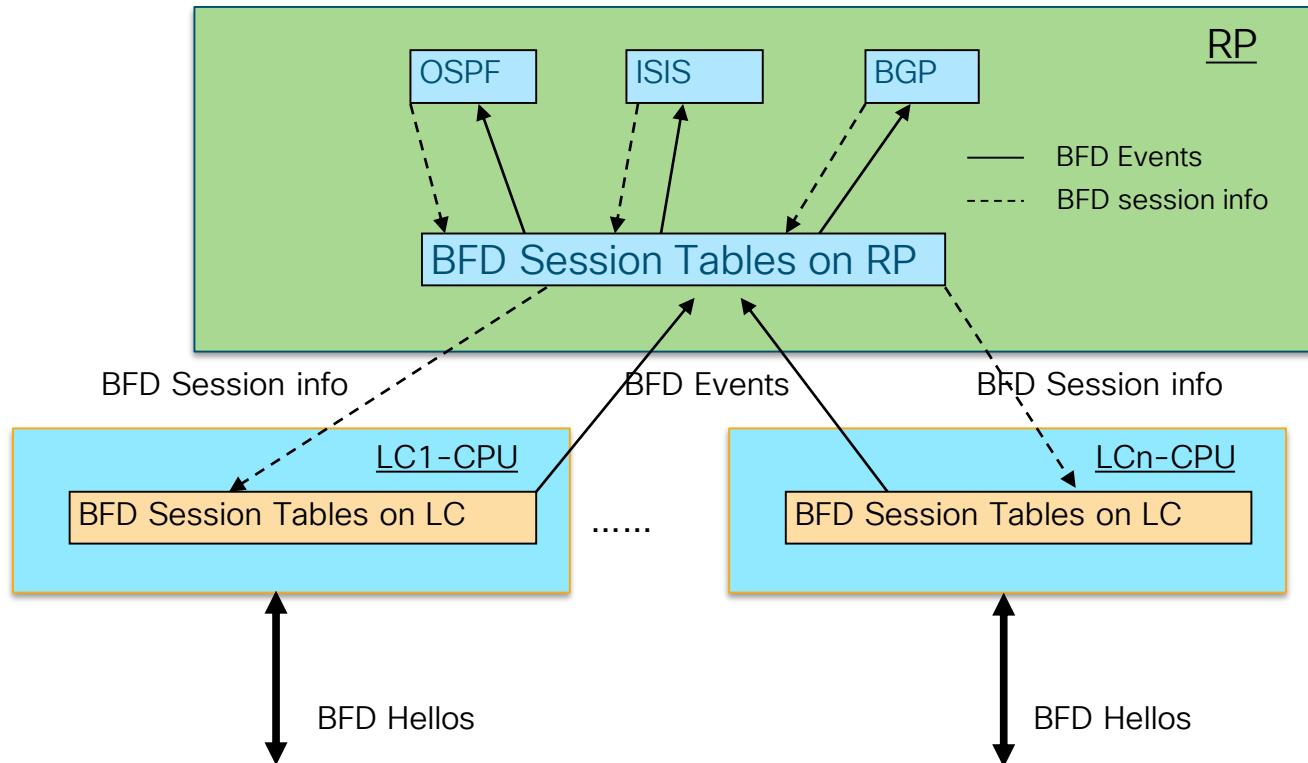
# MAC Learning and Sync

- ① NP learn MAC address in hardware (around 4M pps)
- ② NP flood MAC notification (data plane) message to all other NPs in the system to sync up the MAC address system-wide. MAC notification and MAC sync are all done in hardware

Hardware based MAC learning: ~4Mpps/NP

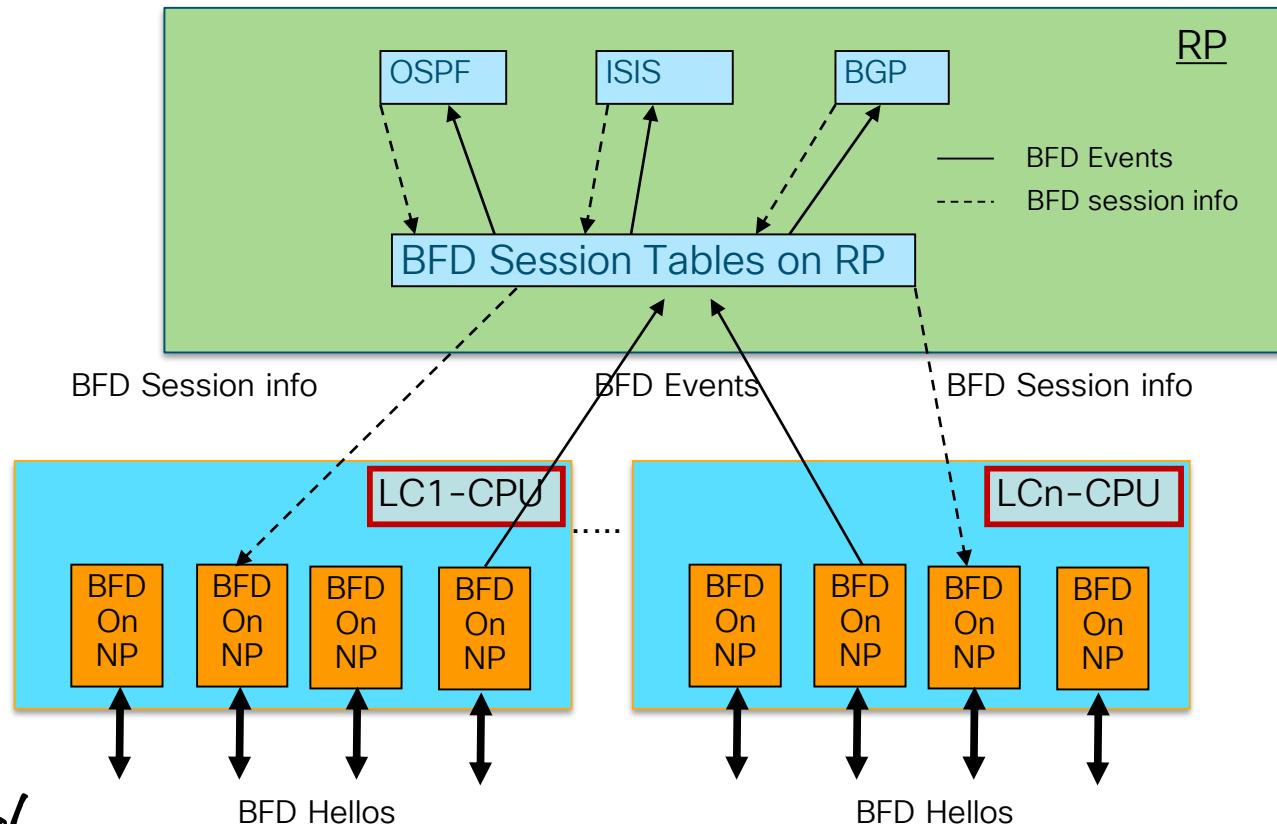


# Distributed BFD Architecture



# HW-offloaded BFD

```
hw-module bfd-hw-offload enable location 0/0/CPU0
```



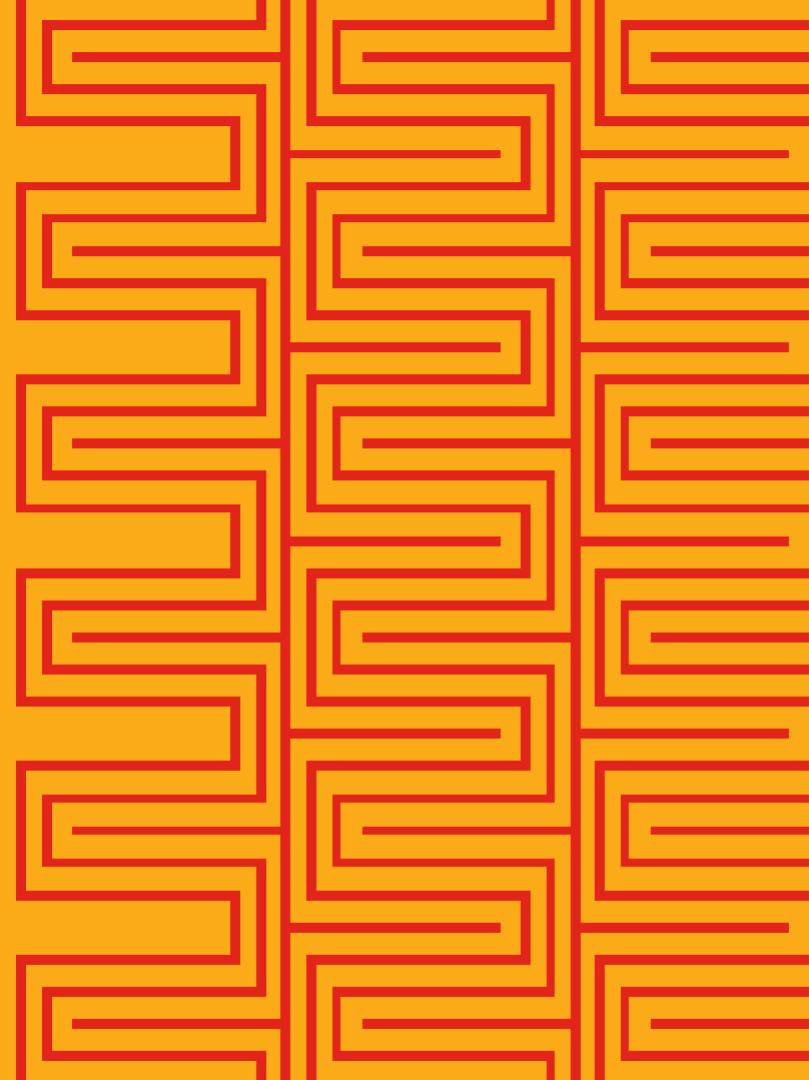
# Pop Quiz ????

In an ASR9906 system which has 2 RSP, 4 linecards and 5 switch fabric cards, how many total CPUs are available to host ASR9000 control-plane functionalities?

- 2
- 4
- 6
- 11

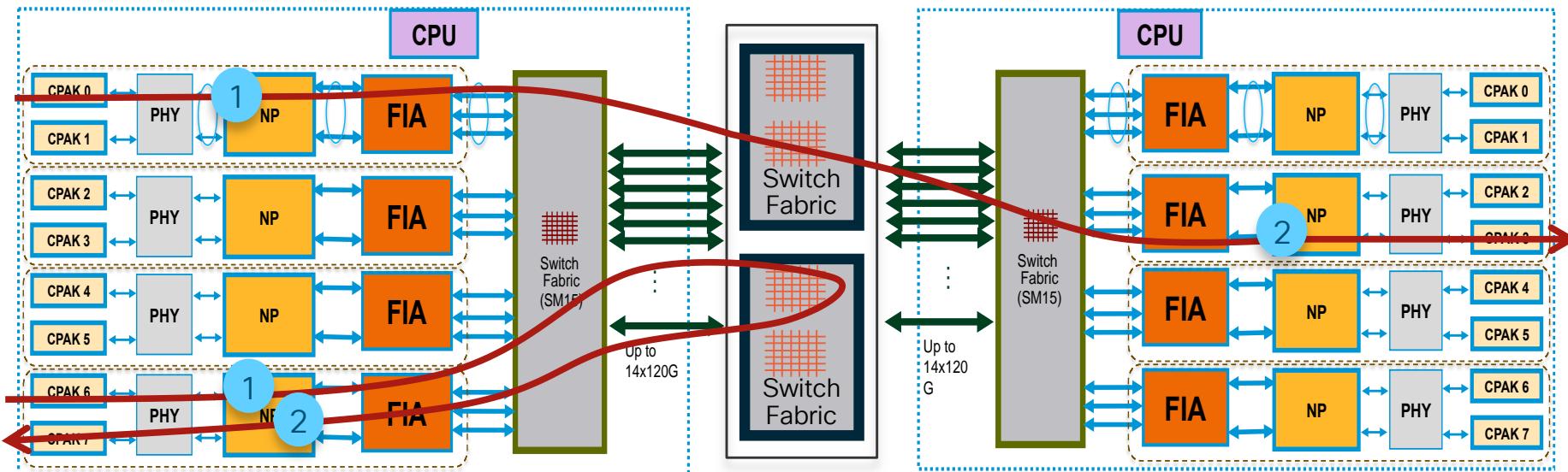


# Data Packet Processing & QoS



# Distributed Two-Stage Packet Processing

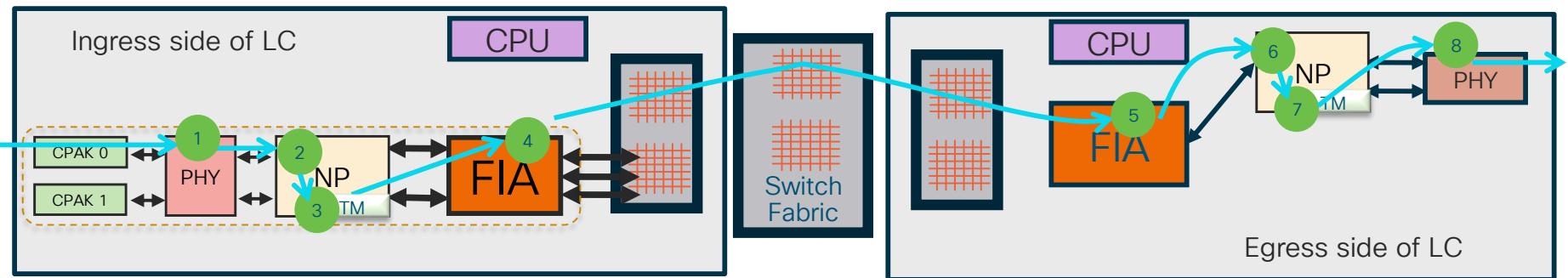
- Ingress lookup yields packet egress port and applies ingress features
- Egress lookup performs packet-rewrite and applies egress features



Uniform packet flow for simplicity and predictable

# ASR9000 Life of a Packet - Tomahawk LC

- 2 • Ingress L2/L3 FIB lookup, ACL/QoS lookup
  - Ingress PBR/ABR, ACL, uRPF
  - Ingress QoS: classification, marking, policing
  - Packet Punting
  - Ingress ECMP/LAG hashing
- 4 • Buffering packet from NP
  - Requesting fabric credit
  - Manage superframe and load-balancing packet across fabric
  - Manage system VoQ
- 6 • Egress L2/L3 FIB lookup, ACL/QoS lookup
  - Egress PBR/ABR, ACL, uRPF
  - Egress QoS: classification, marking, policing, shaping
  - Incomplete Adj Packet Punting
  - Egress ECMP/LAG hashing
- 8 • MACSEC Encryption
  - G.709/OTN/WAN-PHY/LAN-PHY
  - Line Clocking



1 • MACSEC Decryption

- G.709/OTN/WAN-PHY/LAN-PHY
- Line Clocking

3 • Ingress Queuing Processing

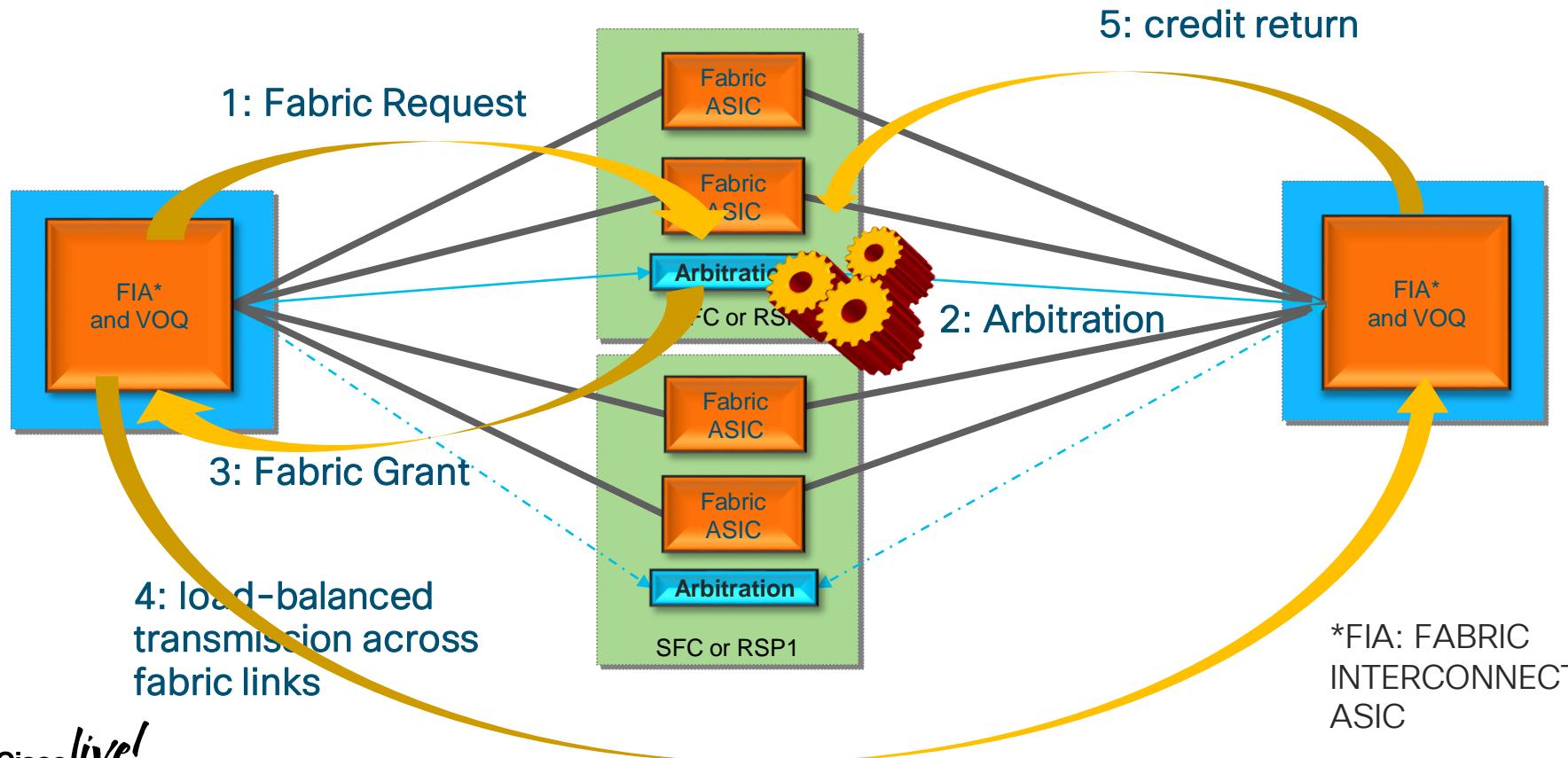
- Bypassed in case no ingress queuing support

5 • Re-assembling packets from superframe

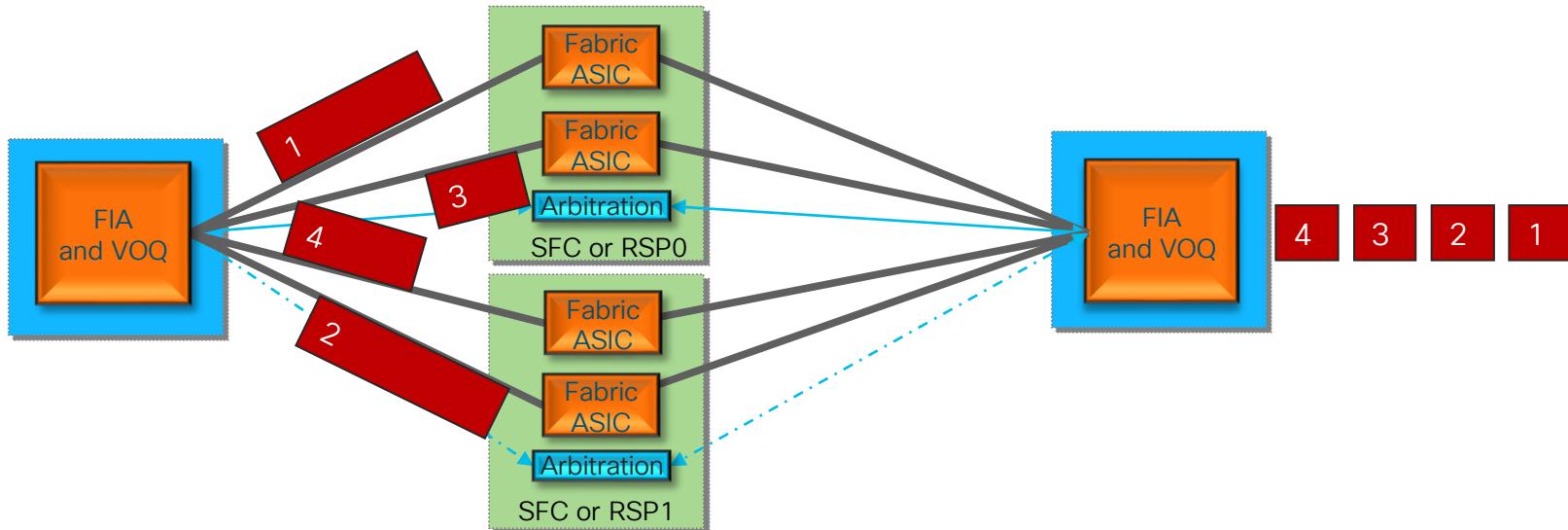
- Send packet to corresponding NP
- Release buffer and fabric credit

7 • Egress Queuing Processing

# Switch Fabric Arbitration

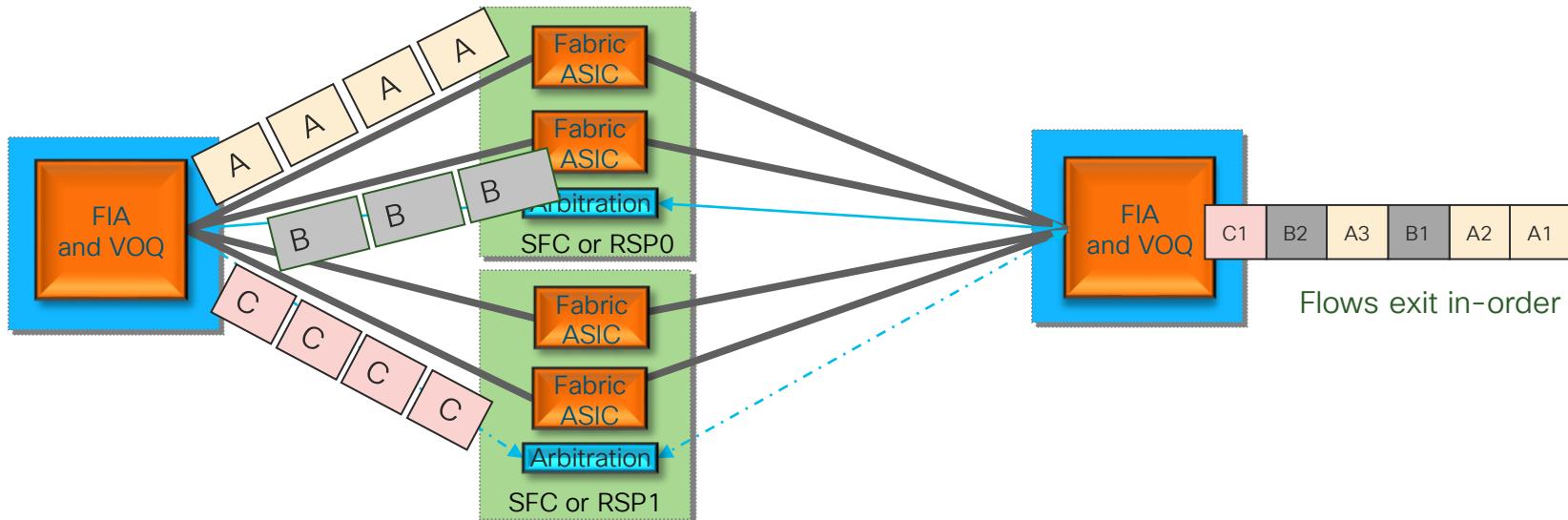


# Fabric Load Balancing – Unicast



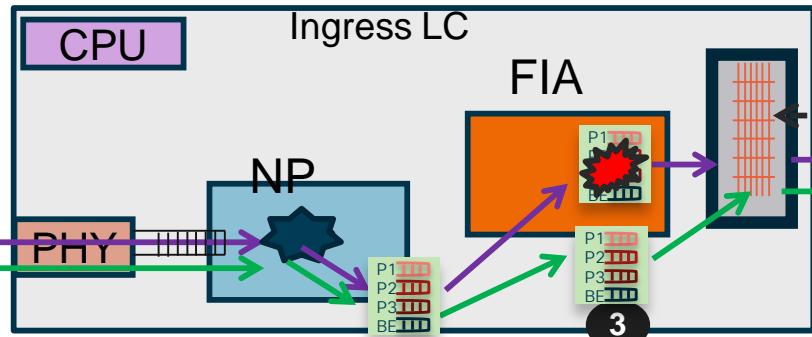
- Unicast traffic sent across first available fabric link to destination (maximizes efficiency)
- Each frame (or super frame) contains sequencing information
- All destination fabric ASIC have re-sequencing logic
- Additional re-sequencing latency is measured in nanoseconds

# Fabric Load Balancing – Multicast

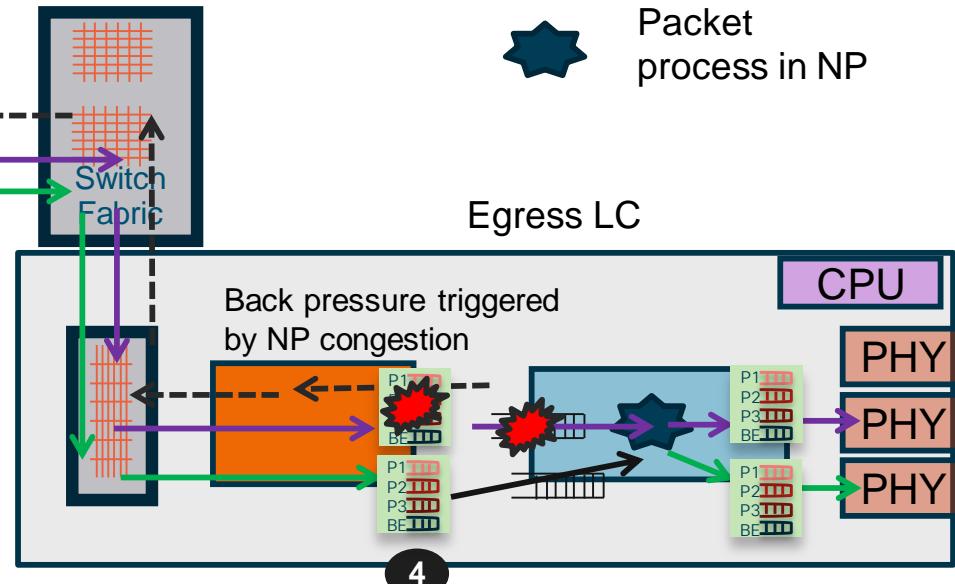


- Multicast traffic hashed based on (S,G) info to maintain flow integrity
  - Very large set of multicast destinations preclude re-sequencing
- Multicast traffic is non arbitrated – sent across a different fabric plane

# Internal QoS: Back Pressure and VoQ

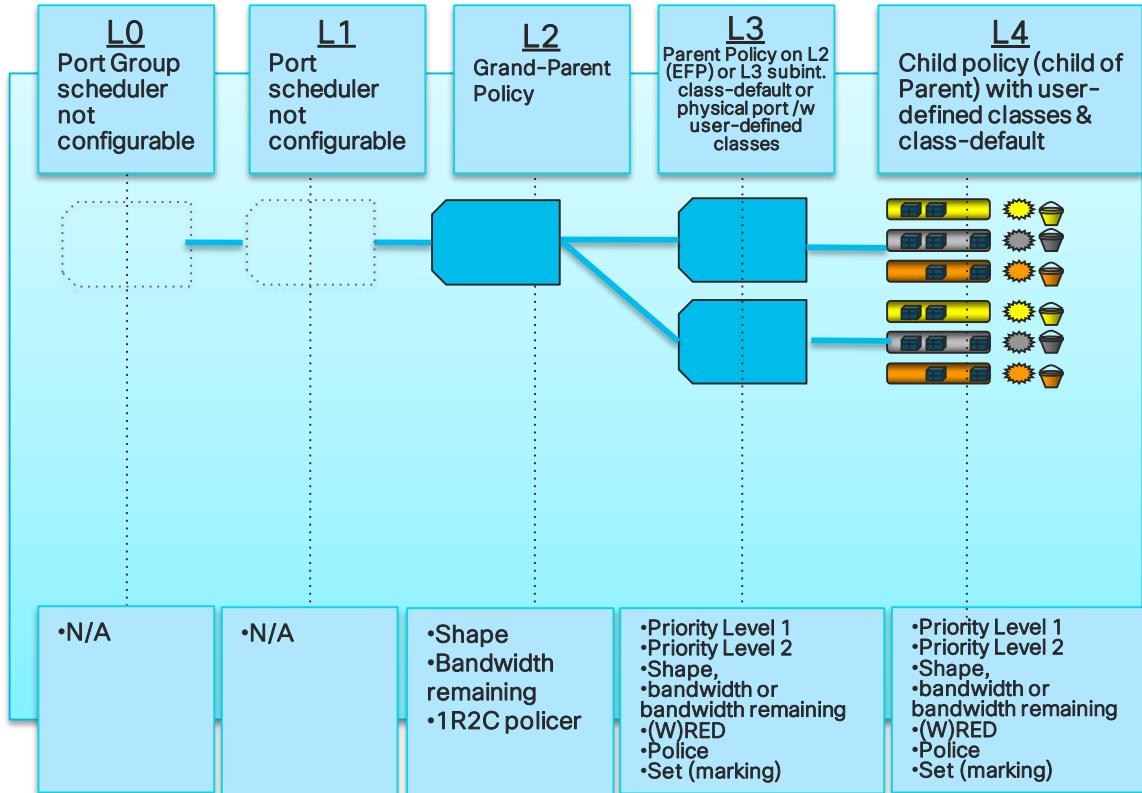


- Per egress NP input q backpressure to egress FIA DQ
- Per egress FIA priority DQ backpressure to switch fabric, then to the same priority VoQs on all ingress FIAs
- **No Head of Line Blocking** between different ports or between different priority VoQs for the same SFP/VQI
- Per Tomahawk FIA: 2k x4 VoQs, 96 x4 DQs



- **100G singe flow!**
  - Per Tomahawk FIA VoQ (3) or DQ (4) 100G, 40G or 10G single flow line-rate

# 3-Layer Hierarchical QoS (H-QoS)



```

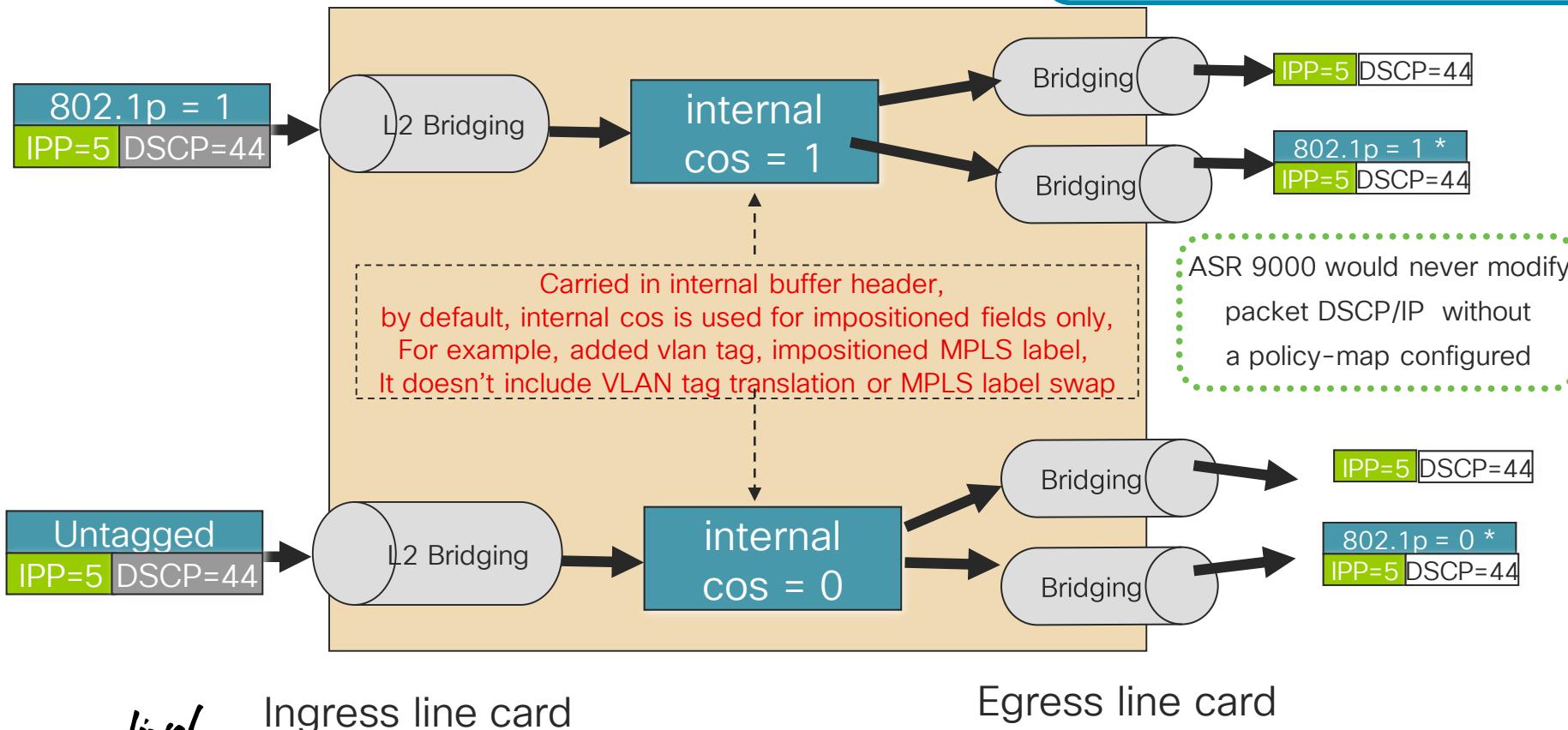
policy-map child
  class Pr1
    police rate 64 kbps
    priority level 1
  class Pr2
    police rate 10 mbps
    priority level 2
  class C13
    bandwidth 3 mbps
  class C14
    bandwidth 1 mbps
  !
policy-map parent
  class parent1
    shape average 100 mbps
    service-policy child
  class parent2
    shape average 25 mbps
    service-policy child
  class class-default
  !
policy-map grand-parent
  class class-default
    shape average 500 mbps
    service-policy parent
  
```

# ASR9000 QoS Classification Criteria

	L2 Header Fields	L3 Header Fields	Internal Marking
L2 Interfaces/EFPs  Or L3 Interfaces	Inner/outer COS, inner/outer vlan, DEI Source/Destination MAC address* match all/match any	Outer EXP DSCP/TOS TTL, TCP flags, Source/destination L4 ports Protocol Source/Destination IPv4 address*	Discard-class Qos-group
Notes:	<ul style="list-style-type: none"><li>- Support match all or match any</li><li>- Max 8 match statements per class, max 8 match entries per match statement</li><li>- Not all header fields can be used in one MQC policy-map, see details next</li><li>- No "Deny" statement if access-list used.</li></ul>		

# Default Implicit Trust Model

L2 IF: trust outer Cos  
L3 IF: trust DSCP  
L3 MPLS: trust outer EXP

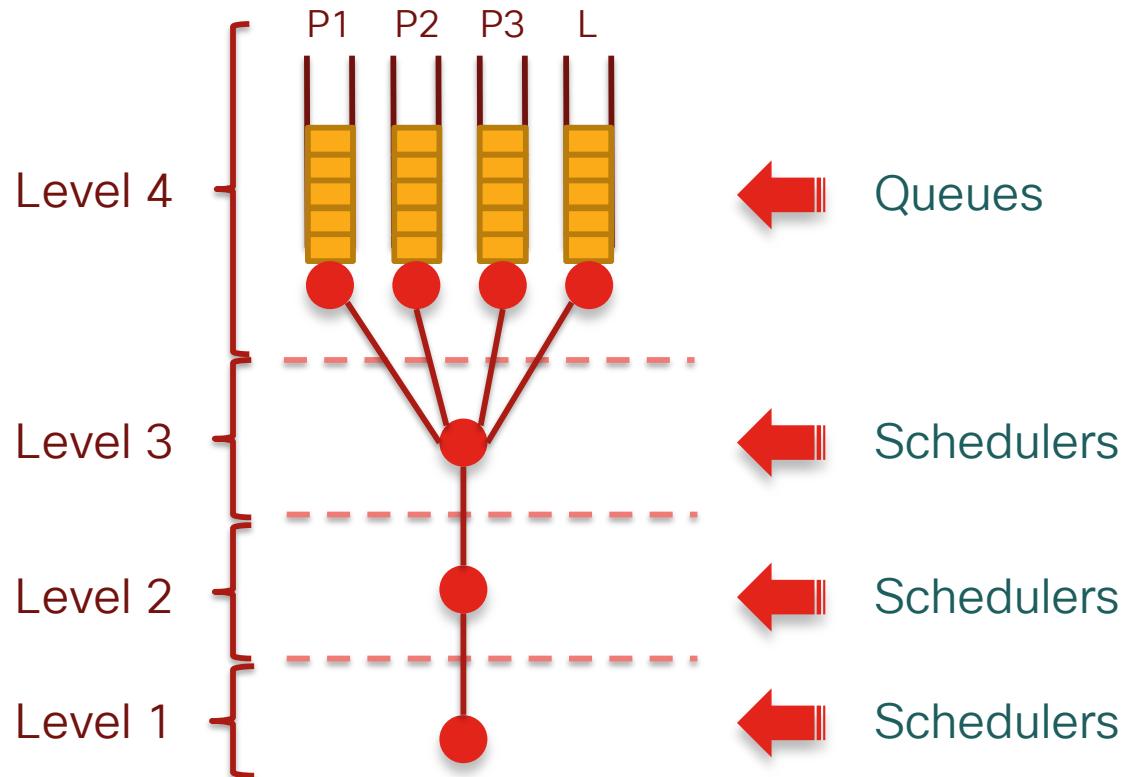


# Queueing

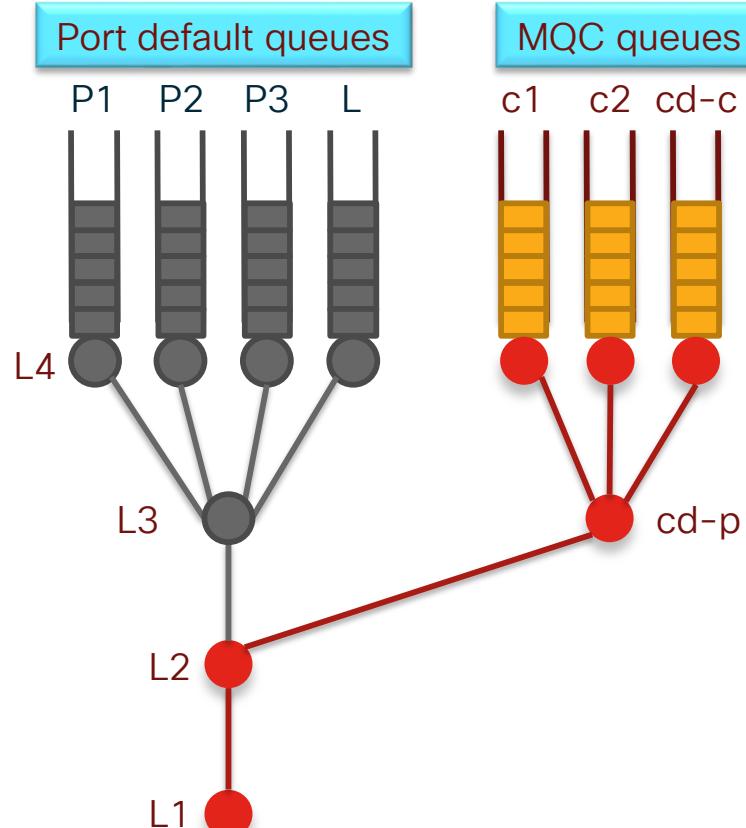
	Queueing Action	Ingress	Egress	Comments
1	shape	Yes	Yes	Supported on all interfaces. Rate configuration supported in percent and absolute terms. Burst configuration not supported.
2	bandwidth	Yes	Yes	Supported on all interfaces. Rate configuration supported in percent and absolute terms.
3	bandwidth-remaining	Yes	Yes	Supported on all interfaces. Configuration supported in percent and ratio, although only one type can be used in a policy.
4	priority	Yes	Yes	Two priority levels supported on all interfaces. Priority class should be always constrained by a policer.
5	queue-limit	Yes	Yes	Supported on all interfaces. Can be specified in packets, bytes and time-based units.
6	WRED	Yes	Yes	WRED based on prec/DSCP/EXP are supported on L3 interfaces. WRED based on discard-class is supported on L2 and L3 interfaces.

❖ Not all LCs support ingress queueing

# Default Interface Queues

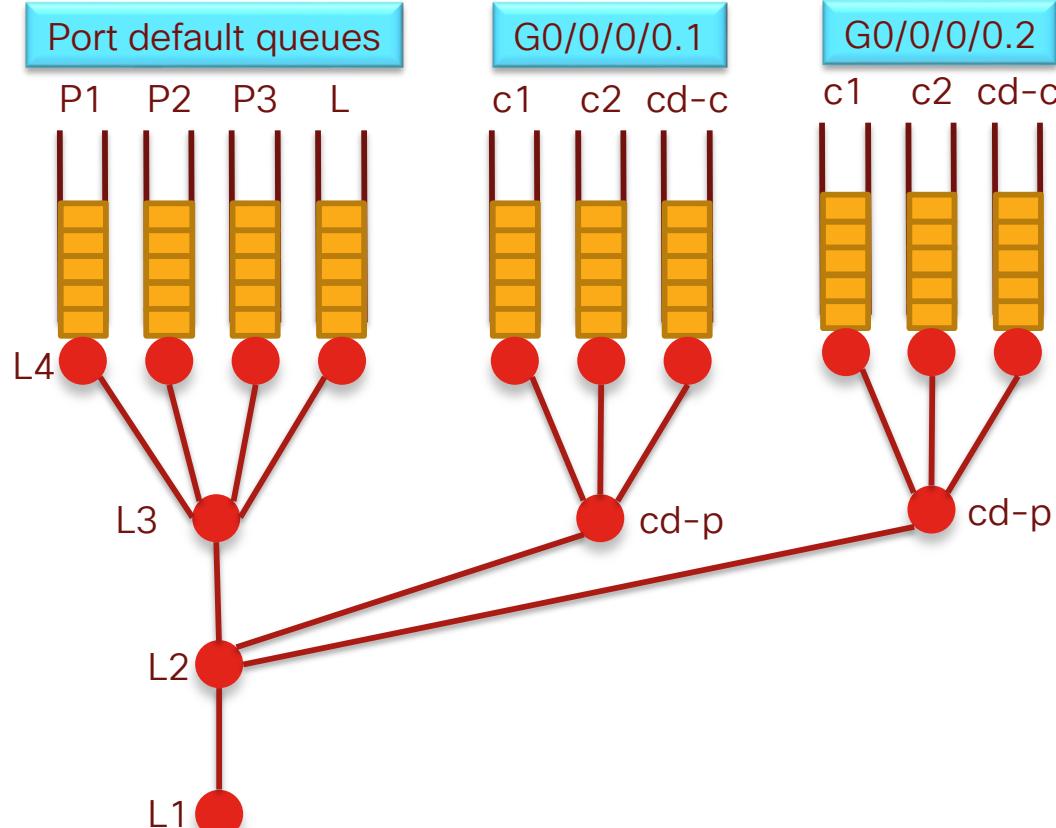


# MQC Hierarchy in Queuing ASIC



```
policy-map child
  class c1
    priority level 1
    police rate 640 kbps
  class c2
    bandwidth 20 mbps
  class class-default cd-c
    bandwidth 1 mbps
!
policy-map parent
  class class-default cd-p
    shape average 35 mbps
    service-policy child
!
interface GigabitEthernet0/0/0/0
  service-policy output parent
```

# MQC Hierarchy in Queuing ASIC



```
policy-map child
  class c1
    priority level 1
    police rate 640 kbps
  class c2
    bandwidth 20 mbps
  class class-default      cd-c
    bandwidth 1 mbps
!
policy-map parent
  class class-default
    shape average 35 mbps
    service-policy child
!
interface GigabitEthernet0/0/0/0.1
  service-policy output parent
!
interface GigabitEthernet0/0/0/0.2
  service-policy output parent
```

- Inactive entity (Grey circle)
- Active entity (Red circle)

# Pop Quiz ????

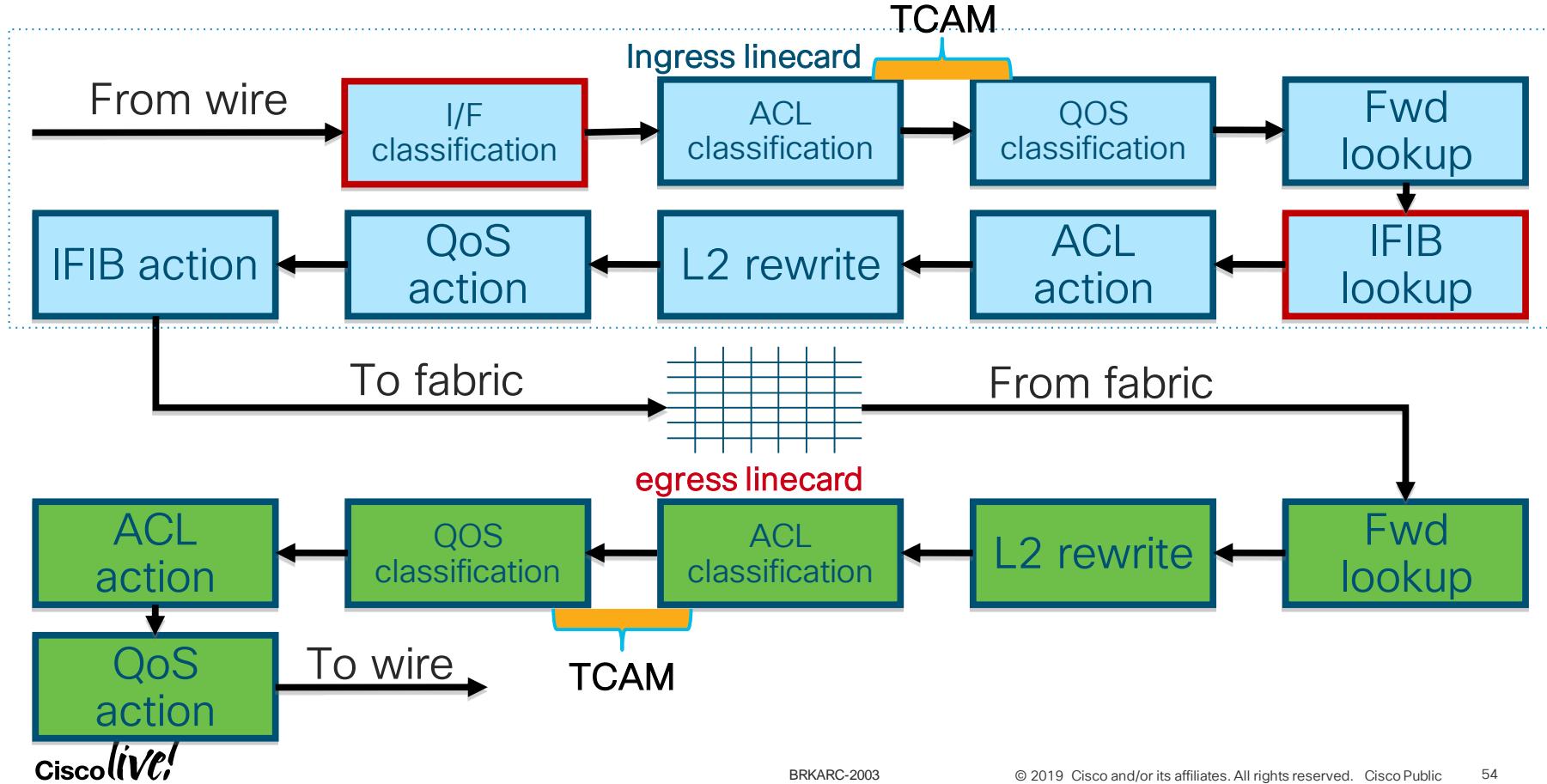
For an incoming **untagged** layer 2 frame, what is the priority value used when the frame is processed inside ASR9000?

- 2
- COS bit
- 802.1p Value
- 0

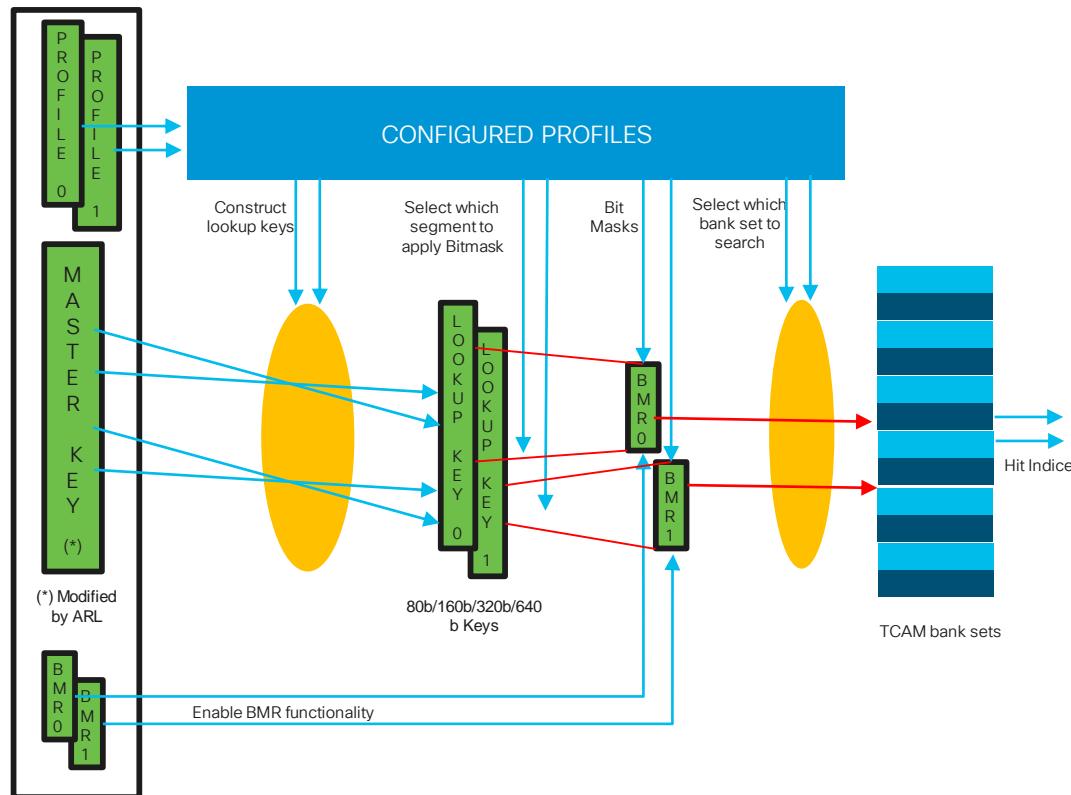


# ASR9000 TCAM Architecture and Usage

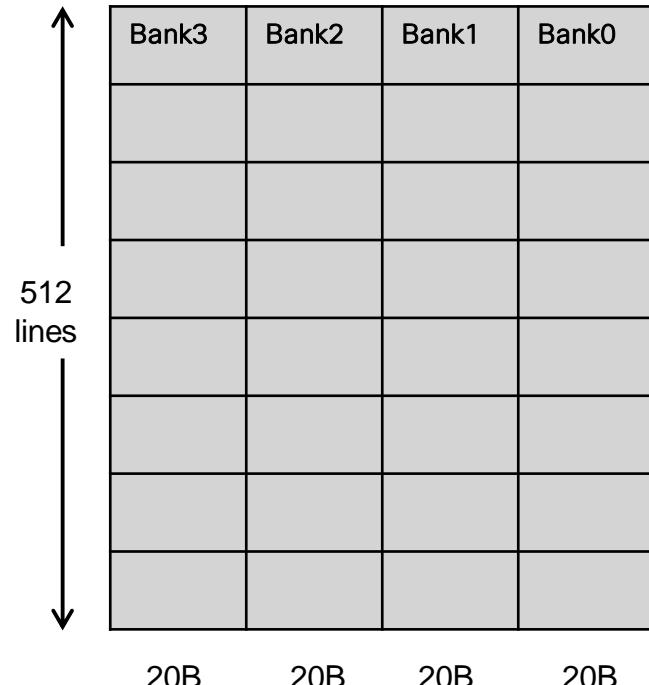
# TCAM Used for Traffic Classification



# 4th Generation LC TCAM Loopup Process



# 4th Generation LC TCAM Bank Sets



- TCAM organized into bank sets, with 4 arrays in each bank set.
- Each array composed of 512x160b entries or 128x640b entries
- Entries can be arranged as 20B/80B wide and can span multiple lines/blocks
- LPTS on 4<sup>th</sup> Generation LC uses hash table instead of iTCAM which saves iTCAM usage

# TCAM Partitions for Different Linecards

TCAM Regions		3 <sup>rd</sup> Generation LC	4 <sup>th</sup> Generation LC
L2 Partition	Physical Ports, Bundles	Reserved Partition for each type	N/A, L2 classification does not require TCAM resource
	Encap Default		
	Encap Untagged, Encap Any		
	Single VLAN, PWHE		
	Double VLAN, BVI		
ODS2 (160 bit entries)	ODS2 iFIB	Reserved Partition for iFIB (IPv4 LPTS)	N/A, LPTS does not require TCAM resource
	Common	Reserved Partition for all ODS2 features	Reserved Partition for all ODS2 features
ODS8(640 bit entries)	ODS8 iFIB	Reserved Partition for iFIB (IPv6 LPTS)	N/A, LPTS does not require TCAM resource
	Common	Reserved Partition for all ODS8 features	Reserved Partition for all ODS8 features

# Lightspeed TCAM Feature Lookup Region

TCAM Region	Features sharing resources	Search mode
160-ING	L2-ACL IPV4-ACL IPv4-QOS PBR-IPV4 PBR-MPLS PBR-L2 IPV4-LI	160 bits
160-EGR	L2-ACL IPV4-ACL IPv4-QOS	160 bits
640-ING	IPV6-ACL IPv6-QOS PBR-IPV6 IPV6-LI EDPL BGP Flowspec	640 bits
640-EGR	IPV6-ACL IPv6-QOS	640 bits

# TCAM Partition Example - 3<sup>rd</sup> Generation LC

```
show prm server tcam summary all all np0 location 0/0/CPU0
  Node: 0/0/CPU0:
-----
TCAM summary for NP0:

  TCAM Logical Table: TCAM_LT_L2 (1)
    Partition ID: 0, priority: 2, valid entries: 2, free entries: 2046
    Partition ID: 1, priority: 2, valid entries: 0, free entries: 2048
    Partition ID: 2, priority: 0, valid entries: 0, free entries: 2048
    Partition ID: 3, priority: 0, valid entries: 8, free entries: 24568
    Partition ID: 4, priority: 0, valid entries: 5, free entries: 67579
  TCAM Logical Table: TCAM_LT_ODS2 (2), free entries: 89710, resvd 128
    ACL Common Region: 448 entries allocated. 448 entries free
    Application ID: NP_APP_ID_IFIB (0)
      Total: 1 vmr_ids, 8005 active entries, 8005 allocated entries.
    Application ID: NP_APP_ID_QOS (1)
      Total: 5 vmr_ids, 13 active entries, 13 allocated entries.
    Application ID: NP_APP_ID_ACL (2)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
    Application ID: NP_APP_ID_AFMON (3)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
    Application ID: NP_APP_ID_LI (4)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
    Application ID: NP_APP_ID_PBR (5)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
  TCAM Logical Table: TCAM_LT_ODS8 (3), free entries: 15200, resvd 128
    ACL Common Region: 448 entries allocated. 448 entries free
    Application ID: NP_APP_ID_IFIB (0)
      Total: 1 vmr_ids, 603 active entries, 603 allocated entries.
    Application ID: NP_APP_ID_QOS (1)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
    Application ID: NP_APP_ID_ACL (2)
      Total: 1 vmr_ids, 5 active entries, 5 allocated entries.
    Application ID: NP_APP_ID_PBR (5)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
    Application ID: NP_APP_ID_EDPL (6)
      Total: 0 vmr_ids, 0 active entries, 0 allocated entries.
```

Note: "show controllers rm tcam summary all all np X location X/X/X" for 4<sup>th</sup> Generation LC

# TCAM Usage Summary

- IPv4-ACL/QoS support on both ingress/egress
- IPv6-ACL/QoS support on both ingress/egress
- IPv4-ACL/QoS search mode use 160bits, IPv6-ACL/QoS search mode use 640bits
- PBR/Lawful Interception(LI) are both ingress features
- BGP FlowSpec (both v4 and v6) uses 640 bit TCAM format, and only in the ingress direction

# Pop Quiz ????

As we discussed, most of IPv4 related features use ODS2 partition and most of IPv6 related features use ODS8 partition. When BGP flowspec is configured for IPv4 traffic and rules has been pushed, in which TCAM region are the rules programmed?

- L2 Partition
- ODS8 Common
- ODS2 Common
- ODS2 iFIB

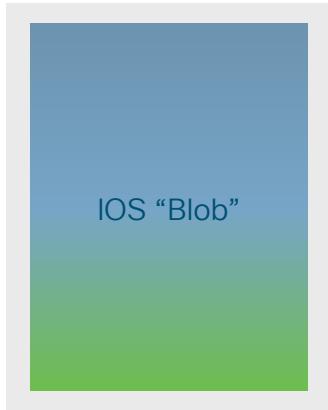


# IOS-XR & IOS-XR 64 Bit

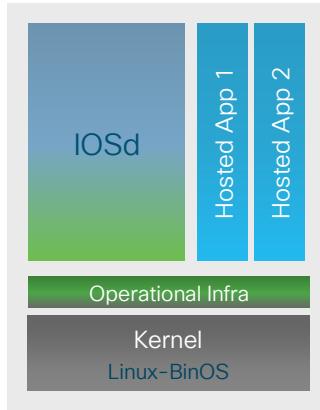


# Cisco IOS - A Recap

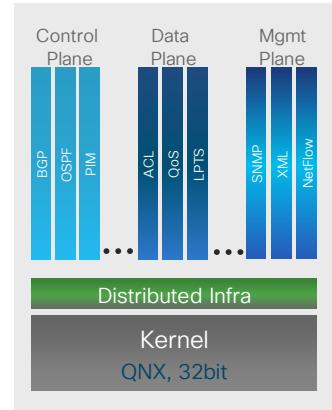
Cisco IOS



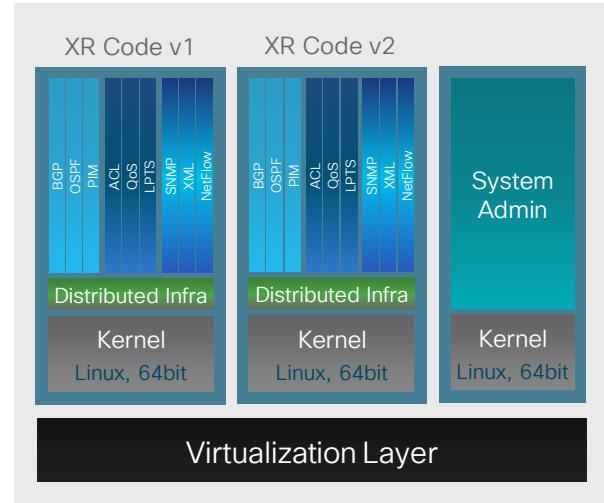
Cisco IOS-XE



Classic IOS-XR



IOS-XR 64 Bit



1990s



2000s



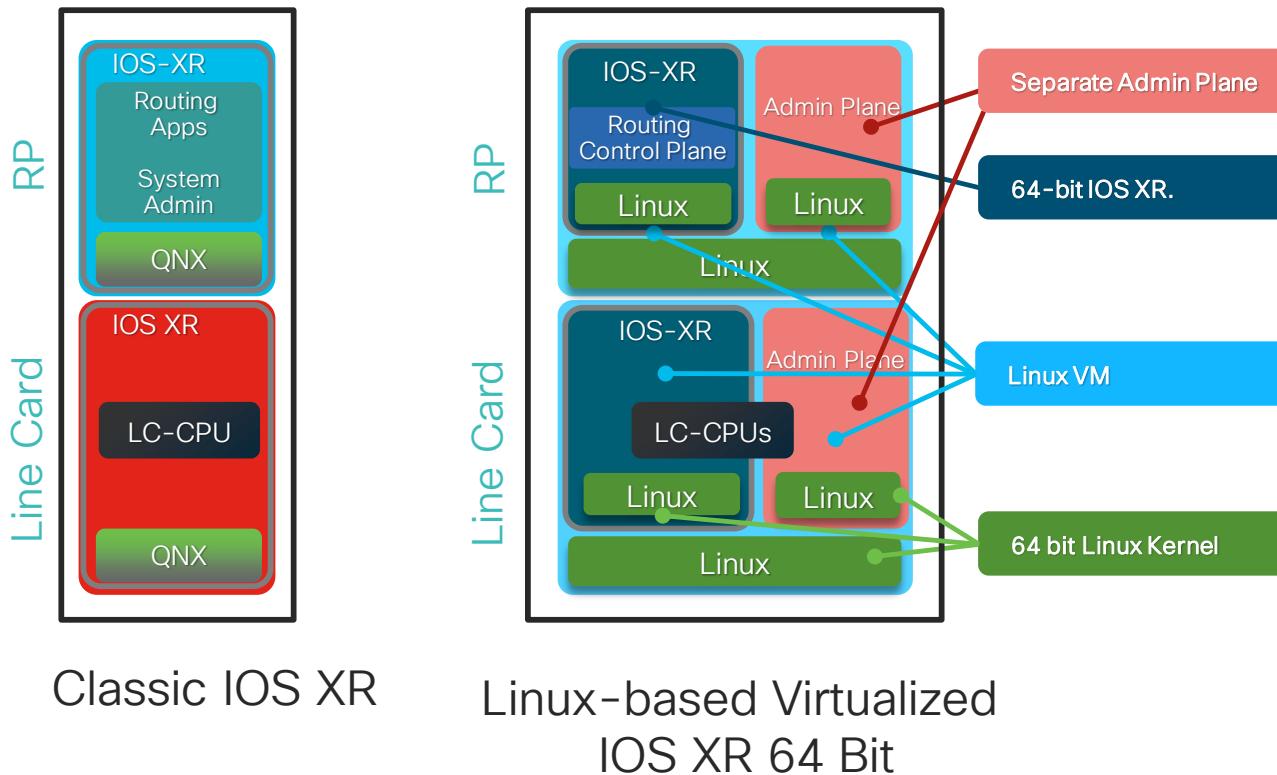
2003-04



Present Day

Incremental Development, with Industry leading investment protection

# IOS XR Evolution: XR 64 bit Architecture



# IOS XR 64 Bit Golden ISO - GISO

- GISO is a customized iso which is built as per individual customer needs.
- GISO contains Mini ISO + rpms + SMUs + config

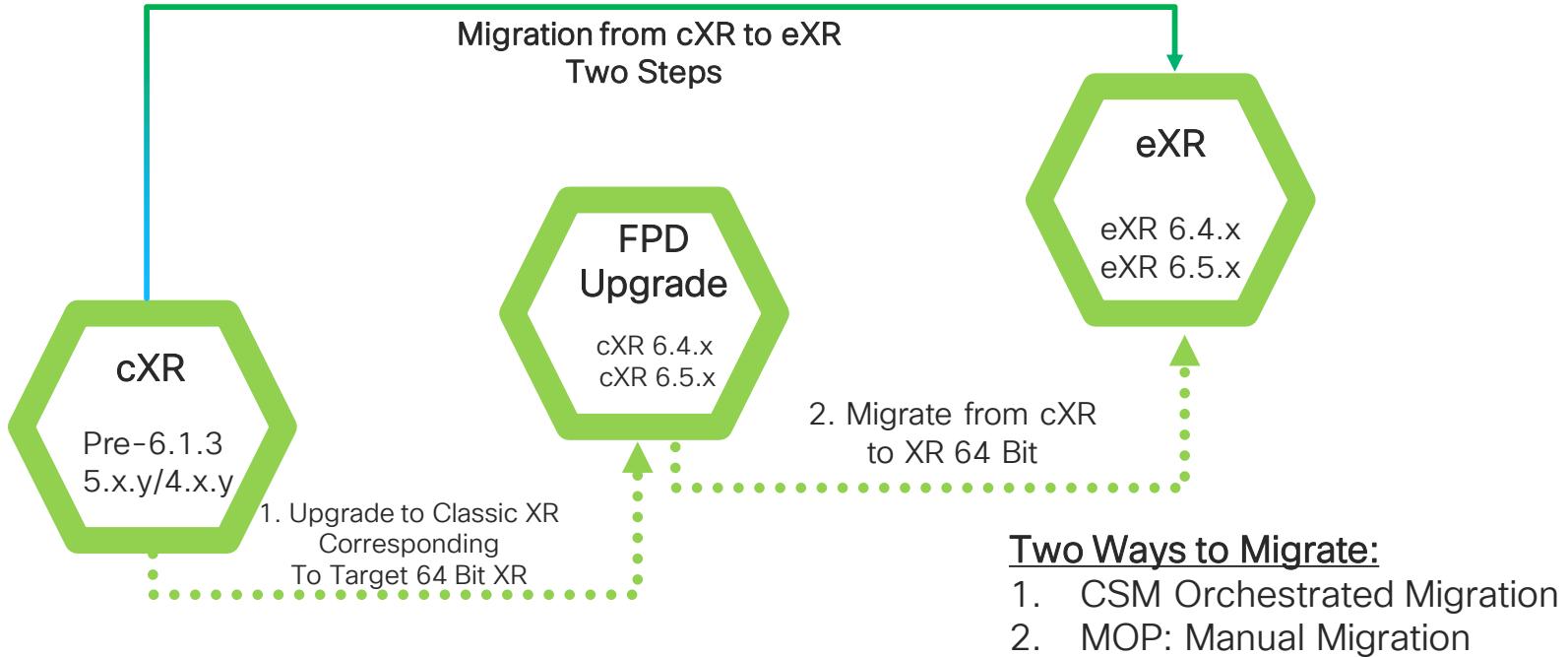
How to build GISO: use tool provided on the router at /pkg/bin/gisobuild.py in XR domain.

Usage: gisobuild.py [-h] -i BUNDLE\_ISO [-r RPMREPO] [-c XRCONFIG] [-l GISOLABEL] [-m] [-v]

Example: gisobuild.py -i asr9k-mini-x.iso -r . -c config-file -l v1

Script Parameter	Expansion	Explanation	Required/optional
-i	BUNDLE_ISO	Path to mini ISO	Required
-r	RPMREPO	Path to RPM repo	Optional
-c	XRCONFIG		Optional
-l	GISOLABEL	GISO Label	Optional
-m	migration	To build migration tar for ASR9K only.	Optional
-v	version	Print script version and exit	Optional
-h	help	Print help menu	N/A

# Migrating Classic XR to IOS XR 64 Bit



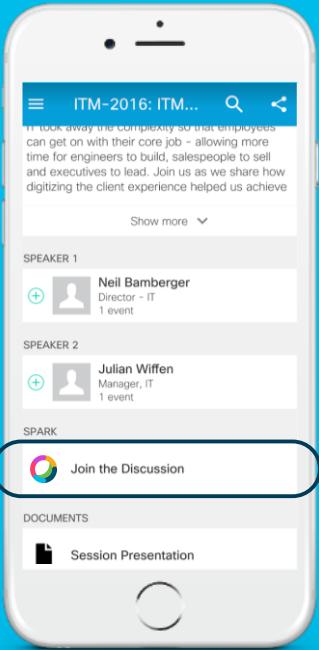
Follow below link for details:

[https://www.cisco.com/c/en/us/td/docs/routers/asr9000/migration/guide/b-migration-to-ios-xr-64-bit/b-migration-to-ios-xr-64-bit\\_chapter\\_011.html](https://www.cisco.com/c/en/us/td/docs/routers/asr9000/migration/guide/b-migration-to-ios-xr-64-bit/b-migration-to-ios-xr-64-bit_chapter_011.html)



# Migration Pre-requisites

HW Component Check	Upgrade cXR	Operational Status	Backup cfg to External Server (Calvados, XR)
<ul style="list-style-type: none"><li>All hardware components, Chassis, RSP/RP, LC, FC, FAN and PEM, should be supported in ASR9K 64 bit. Any unsupported hardware may fail to boot after migration</li></ul>	<ul style="list-style-type: none"><li>Any pre-6.1.3 release needs to be upgraded to classic XR corresponding to the target IOS XR 64 Bit version</li></ul>	<ul style="list-style-type: none"><li>All hardware components must be in operational state before migration</li></ul>	<ul style="list-style-type: none"><li>Back up admin/XR configuration to external server</li></ul>



# Cisco Webex Teams



## Questions?

Use Cisco Webex Teams (formerly Cisco Spark) to chat with the speaker after the session

## How

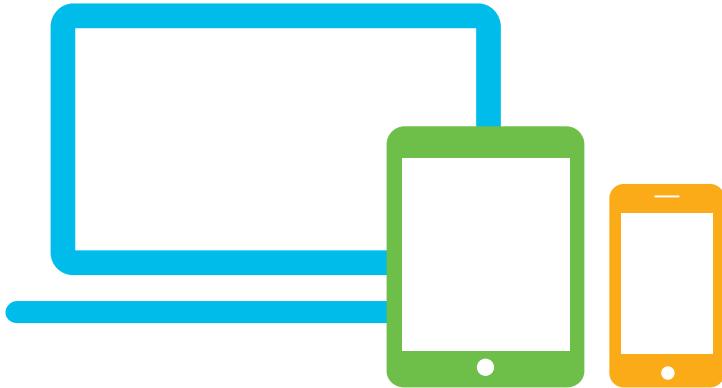
- 1 Find this session in the Cisco Events Mobile App
- 2 Click “Join the Discussion”
- 3 Install Webex Teams or go directly to the team space
- 4 Enter messages/questions in the team space

[cs.co/ciscolivebot#BRKARC-2003](https://cs.co/ciscolivebot#BRKARC-2003)

# Complete your online session survey

- Please complete your Online Session Survey after each session
- Complete 4 Session Surveys & the Overall Conference Survey (available from Thursday) to receive your Cisco Live T-shirt
- All surveys can be completed via the Cisco Events Mobile App or the Communication Stations

Don't forget: Cisco Live sessions will be available for viewing on demand after the event at [ciscoalive.cisco.com](https://ciscoalive.cisco.com)



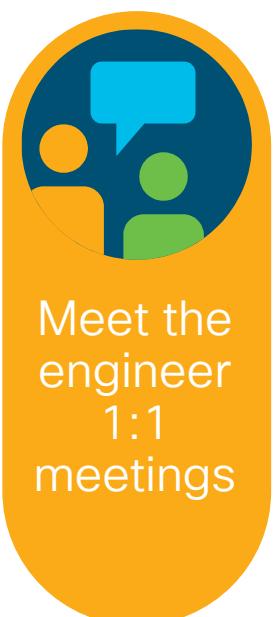
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