SystemC & Behavior Coding

Assignment 6, 2024-12-11

Abstract

Remodel the Exercise 1 timer module with `SC_CTHREAD`.

Please read carefully. All outputs required are described in the text. Five (5) points will be taken for each bug, missing the required output and behavior.

The `SC_CTHREAD` timer module

Description

1. Remodel the Exercise 1 timer module with `SC_CTHREAD`, where `clock` pin is a positive-triggered clock port, and `start` pin is a synchronous active-high reset port.

sc_main

Description

1. Reuse the `main.cpp` implemented in Assignment 5.
2. Create a trace file named `RESULT.vcd`. And trace ports and the register `count` as follows:
   - `clock`
   - `count`
   - `start`
   - `timeout`

makefile

Description

A `makefile` must be provided with proper modifications to your environment.

Using Generative AI

It is encouraged to use Generative AI (GAI) to solve the problem as in earlier assignments. If you use GAI to solve the problem, please compose a prompt to ask the GAI to create another `timergai` module and name it `timergai.h` and `timergai.cpp` plus its `sc_main()` i.e., the test bench, and call it

`gai_main.cpp`, to test the correctness of the `timergai` module. This `timergai` module is a `SC_CTHREAD` one that uses a negative-triggered `clock` with an asynchronous active-low `reset`. Note that the new `sc_main()` needs to design a new waveform, and name the output waveform file `RESULTgai.vcd`. Turn in two prompts you composed and `timergai.h`, `timergai.cpp`, and `gai_main.cpp` thus generated as well. Note that the `makefile` has to include the compilation of this new `timergai` module as well.

Please turn in the source codes and `makefile` only. Do not turn in the executable and waveforms.

Due date
3:00 PM, December 18, 2024

Score weight (towards the final grade) 5%