```
----------------------------------------
Test function of multiplication...
Multiplication task correct
Test function of division...
Division task correct
Test function of AND...
AND task correct
Test function of OR...
OR task correct
----------------------------------------
-    Success!! You passed the simulation    -
----------------------------------------
```

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
alu_in_reg	Flip-flop	32	Y	N	Y	N	N	N	N
shreg_reg	Flip-flop	64	Y	N	Y	N	N	N	N
state_reg	Flip-flop	3	Y	N	Y	N	N	N	N
counter_reg	Flip-flop	5	Y	N	Y	N	N	N	N