HENRY CRUTE

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EDUCATION

University of Texas at Austin *August 2015 - May 2017*
M.S. in Electrical & Computer Engineering
Academic Focus in Architecture, Computer Systems, and Embedded Systems

University of California, Santa Cruz *September 2011 - June 2015*
B.S. in Computer Engineering
Minor in Computer Science
Member of Tau Beta Pi Engineering Honor Society
Dean's Undergraduate Research Award: May 2015
Dean's Honors: Fall 2013 - Spring 2014

EXPERIENCE

Qualcomm May 2016 - August 2016
Modem Firmware Intern *San Diego, CA*

- Implemented a UE Specific Regerence Signal Interference Cancellation and Equalization algorithm.
- Used a proprietary SIMD VLIW singnal processing architecture.
- The final product accomplished matrix inverse approximations using an optimized combination of the Gauss-Seidel method, Cholesky decomposition, and backwards substitution over large non-sparse matrices of complex numbers.
- Verified and validated the algorithms using Matlab, and C. Finally partially optimized in assembly.

UC Santa Cruz June 2014 - June 2015
Research Assistant *Santa Cruz, CA*

- Wrote PIC32 firmware for intermediate data flow control and processing between the MCP3912 sigma delta ADC and wifi/usb controllers.
- Wrote firmware for the ESP8266-03 to store and http POST wattage data to a test server.
- The ESP8266-03 firmware includes the use of an ad hoc chip configuration network as well as regular station mode to connect to the server end point.
- Maintained MSP430 firmware for high speed voltage and current sampling.
- Wrote data visualization software for big data with MATLAB and Python.

CITRIS/ITI June 2014 - January 2015
Technical Assistant *Santa Cruz, CA*

- Served in technical support for equipment in CITRIS conference rooms, experimental classrooms and videoconferencing facilities, for their audio-visual and teleconferencing equipment.
- Helped manage conferences, research symposiums, classes, job fairs, and other events requesting CITRIS space.

TECHNICAL SKILLS

Computer Languages	C/C++, Embedded C, Python, Assembly, Java, Matlab, Verilog, Perl
Communication & Networking	TCP & UDP IPs, PAM-N & QAM-N Transceivers
Tools & Platforms	Git, Mercurial, gem5, Code Composer, Eclipse, MPLAB, NP++, Geany, FDATool, VCS

ADDITIONAL EXAMPLE PROJECTS

x86 Processor - Designed a processor with an x86 instruction set specified by the IA-32 Intel Architecture Software Developer's Manual in a team of four engineers. Built using only structural Verilog. The micro-architecture included a 7 stage pipeline, simple two level branch predictor, and i-cache, d-cache, DMA, I/O controllers sharing a 32 bit bus. The micro-architecture also handled interrupts, and precise exceptions.

SRRIP Replacement Policy - Built using C++ and Python. Added the Static Re-Reference Interval Prediction policy in C++ to gem5 and compared it to the already implemented LRU policy. Statistics of cache misses for different associativity and sizes were obtained using python and SPEC CPU 2006 test benches.

Compiler - Built using C++, Flex, and Bison. The compiler scans, parses, type checks, and outputs appropriately translated assembly code. The language is a subset of C, and includes structs, loops, variables, if statements, scope, functions, and more.

Foobar Challenges - Built using python. Documented and solved numerous coding challenges in the topics of algorithms, data structures, low-level representation, math, and cryptography.