User's Manual

飞凌嵌入式 FORLINX EMBEDDED

FETMX6UL-C
OKMX6UL-C

ARM Cortex-A7

Embedded Development Platform

Hardware Manual

Forlinx Embedded Technology Co. Ltd. www.forlinx.net

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Address: 2699 Xiangyang North Avenue, Baoding, Hebei, China. TEL:0312-3102663 FAX:0312-3112651

Product Features

1. NXP i.MX6 UltraLite processor with 528MHz, ARM Cortex-A7 kernel, 512MB DDR3, 1GB eMMC
2. Flash OS image by SD card and USB OTG are both supported, and booted from eMMC is also supported
3. Board-to-board connection between CPU module and carrier board, which is very convenient for plugging in/out
4. Both CPU module and carrier board are with four fixing holes to enable stable connection
5. With on-board dual CAN port, WIFI&BT module, ESAM and dual fast Ethernet

Attentions

MUST READ BEFORE WORKING WITH i.MX6UL

Product Operation Environment:

Power Supply: DC 5V
Working Temperature: 0 - 85℃
Humility: 10–95%（Non-condensing）

- Hot-plug of CPU module and peripheral modules is strictly prohibited.
- Please follow all the warnings and instructions marked on the product.
- Please keep the product dry. Once splashed or immersed by any liquid, cut off the power and dry it out immediately.
- Please store and operate the product in ventilating conditions to avoid damages brought by over high temperature.
- Please do not use or store the product in dusty or untidy conditions.
- Please do not use or store the product in alternate cold and hot conditions to avoid condensing which will damage components.
- Please do not treat the product rudely. Any falling-off, knocking and violate shaking may cause destruction to circuit and components.
- Please do not clean the product with organic solvents or corrodible liquids.
- Please do not dismantle or repair the product by yourself. Contact us when the product malfunctions.
- Please do not modify the product by yourself or use fittings unauthorized by us. Otherwise, the damage caused by that will be on your part and not included in guarantee terms.

Any questions please feel free to contact Forlinx Technical Service Department..

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Copyright Announcement

Updating Record

Date	Manual Version	CPU Module Version	Base Board Version	Updated
July, 2017	V1.5	V1.1	20160926	1. added spec. about CPU module frequency, interface rate 2. CPU module pin definition updated and added with GPIO ball NO., pin level, I/O information
Oct.21, 2016	V1.4	V1.1	20160926	1. carrier board updated 2. USB OTG circuit description
Oct.10, 2016	V1.3	V1.1	20160526	1. new support to NAND Flash 2. carrier board DIP settings about NAND Flash
Aug.11, 2016	V1.2	V1.1	20160526	1. new description of 4G eMMC ROM
Jun.14, 2016	V1.1	V1.1	20160526	1schematic updates 1. added external RTC chipset to avoid RTC battery power consumption too fast 2. delete LED1 and LED4 3. to avoid booting effected by LCD, we added a buffer chipset between LCD and CPU 4. new design of 4.3'' LCD fixing hole 5. updated PCB silkprint
Mar.7, 2016	V1.0	V1.0	20160301	First edition

Technical Support and Innovation

1. Technical Support

1.1 information about our company's software and hardware
1.2 problems related to our software and hardware manual
1.3 after-sale technical support for OEM and ODM
1.4 requirement of source code and other info which is lost or updated
1.5 failure diagnose and other after-sale service

2. Range of Technical Discussion (non-compulsory)

2.1 modification and comprehension of source code
2.2 how to implant OS
2.3 software and hardware problems occured in self-modifying and programming

3. Accesses to Technical Support

3.1 Tel (non-instant messenger): 0312-3119192
3.2 Email address (non-instant messenger) :
3.2.1. About Linux: linux@forlinx.com
3.2.2. About WinCE: wince@forlinx.com
3.2.3. About Android: android@forlinx.com
3.3 Forum (non-instant): http://bbs.witech.com.cn

4. Timetable for Technical Support

9:00am to 11:30am, 13:30pm to 17:00pm, Monday to Friday

Support will not be available on public holidays. Please send your questions to the email addresses above or Column Technical Support in forum. We'll reply as soon as we are back.

5. Access to Materials

Log in "bbs.witech.com.cn". Click "*materials for development board*" and download what you need.

Contents

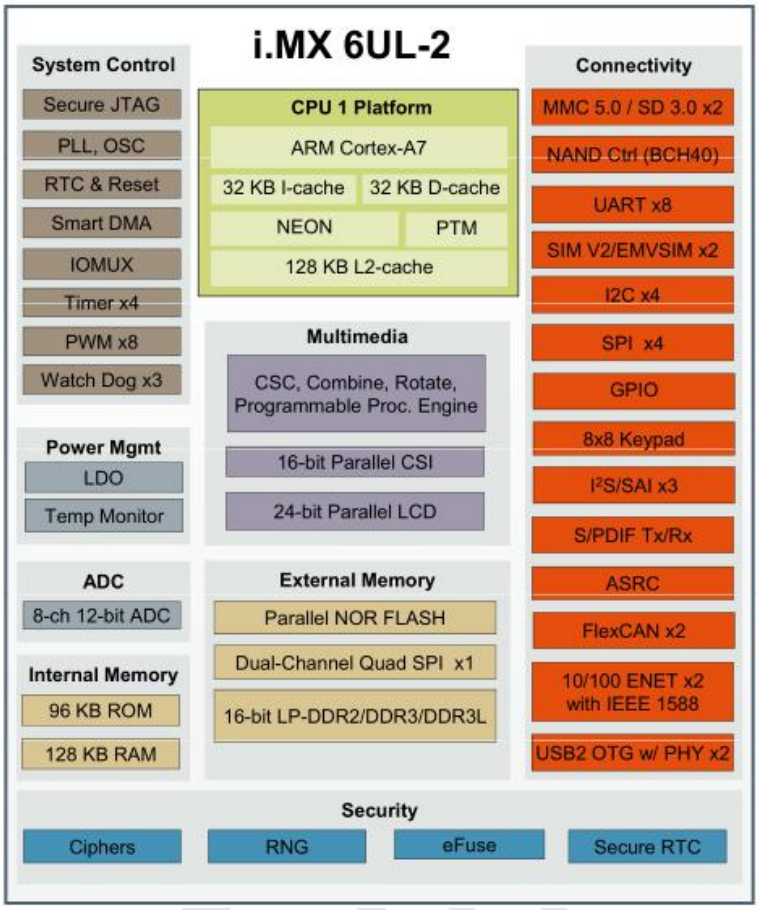
Chapter 1 Overview of Freescale iMX6Ultra Lite

Expanding the i.MX 6 series, the i.MX 6UltraLite is a high performance, ultra-efficient processor family featuring an advanced implementation of a single ARM® Cortex®-A7 core, which operates at speeds up to 528 MHz. The i.MX 6UltraLite applications processor includes an integrated power management module that reduces the complexity of external power supply and simplifies power sequencing. Each processor in this family provides various memory interfaces, including 16-bit LPDDR2, DDR3, DDR3L, raw and managed NAND flash, NOR flash, eMMC, Quad SPI and a wide range of other interfaces for connecting peripherals such as WLAN, Bluetooth™, GPS, displays and camera sensors.

Freescale i.MX6UltraLite

Target Applications

• Automotive telematics
• IoT Gateway
• HMI
• Home energy management systems
• Smart energy concentrators
• Intelligent industrial control systems
• Electronics POS device
• Printer and 2D scanner
• Smart appliances
• Financial payment systems



i.MX 6ULTRALITE DEVICE OPTIONS

- Red indicates change from column to the left

Feature	MCIMX6G0	MCIMX6G1	MCIMX6G2	MCIMX6G3
Speed	528 MHz	528 MHz	528 MHz	528 MHz
Cache	32 KB-I, 32KB-D	32 KB-I, 32KB-D 128 KB L2	32 KB-I, 32KB-D 128 KB L2	32 KB-I, 32KB-D 128 KB L2
OCRAM	128 KB	128 KB	128 KB	128 KB
DRAM	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L
eFuse for Customer	512-bit	1024-bit	1536-bit	2048-bit
NAND (BCH40)	Yes	Yes	Yes	Yes
Parallel NOR/EBI	Yes	Yes	Yes	Yes
Ethernet	10/100 MB x 1	10/100 MB x 1	10/100 MB x 2	10/100 MB x 2
USB with PHY	OTG, HS/FS x 1	OTG, HS/FS x 2	OTG, HS/FS x 2	OTG, HS/FS x 2
CAN	0	1	2	2
Security	Basic	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES with DPA/TDES/SHA/RSA), Secure Boot, Tamper Monitor, PCI4.0 pre-certification, OTF DRAM Encryption
Graphic	None	None	PxP	PxP
CSI	None	None	24-bit Parallel CSI	24-bit Parallel CSI
LCD	None	None	24-bit Parallel LCD	24-bit Parallel LCD
Quad SPI	1	1	1	1
SDIO	2	2	2	2
UART	4	8	8	8
I²C	2	4	4	4
SPI	2	4	4	4
I²S/SAI	1	3	3	3
S/PDIF	1	1	1	1
Timer/PWM	Timer x2, PWM x4	Timer x4, PWM x8	Timer x4, PWM x8	Timer x4, PWM x8
12-bit ADC	1x8ch	1x8ch	2x8ch	2x8ch

The i.MX 6UltraLite applications processor includes an integrated power management module that reduces the complexity of external power supply and simplifies power sequencing. Each processor in this family provides various memory interfaces, including 16-bit LPDDR2, DDR3, DDR3L, raw and managed NAND flash, NOR flash, eMMC, Quad SPI and a wide range of other interfaces for connecting peripherals such as WLAN, Bluetooth®, GPS, displays and camera sensors. The i.MX 6UltraLite is supported by discrete component power circuitry.

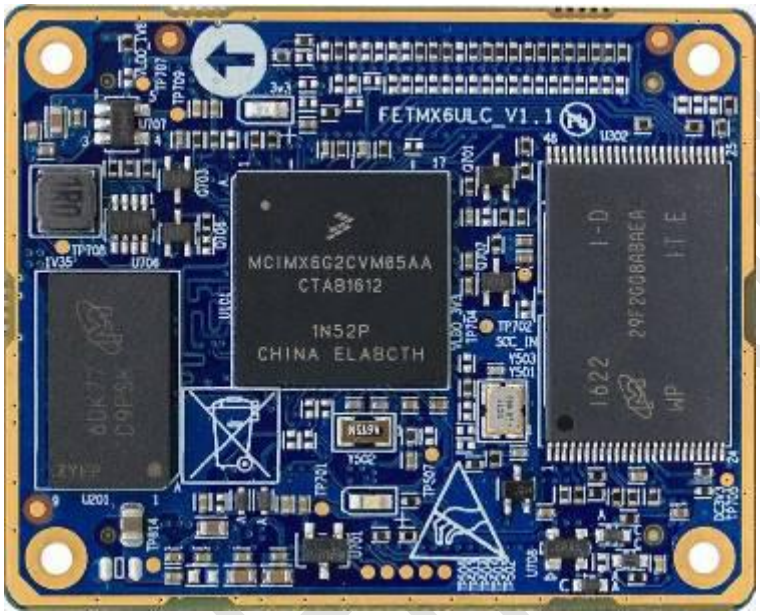
To view more details, please visit Freescale official website

http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-6-processors/i.mx6qp/i.mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?uc=true&lang_cd=en

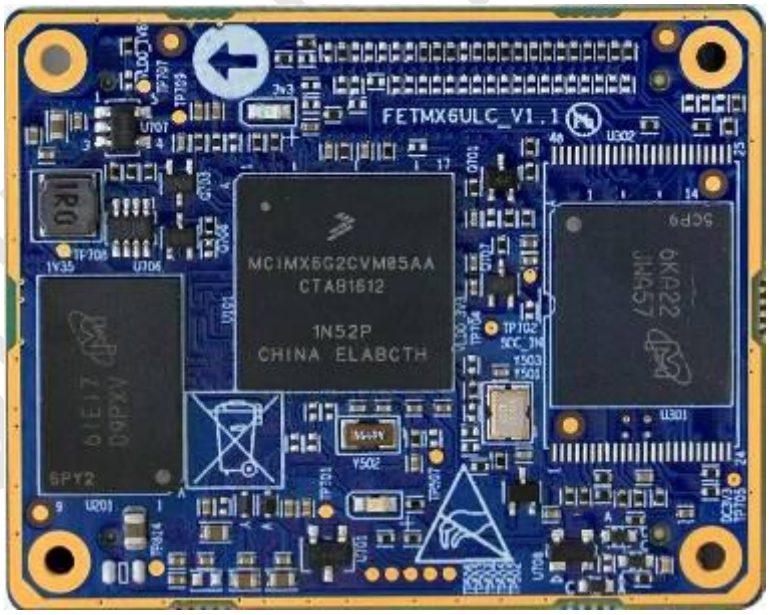
Chapter 2 i.MX6UL CPU Module Introduction

2.1 CPU Module Overview

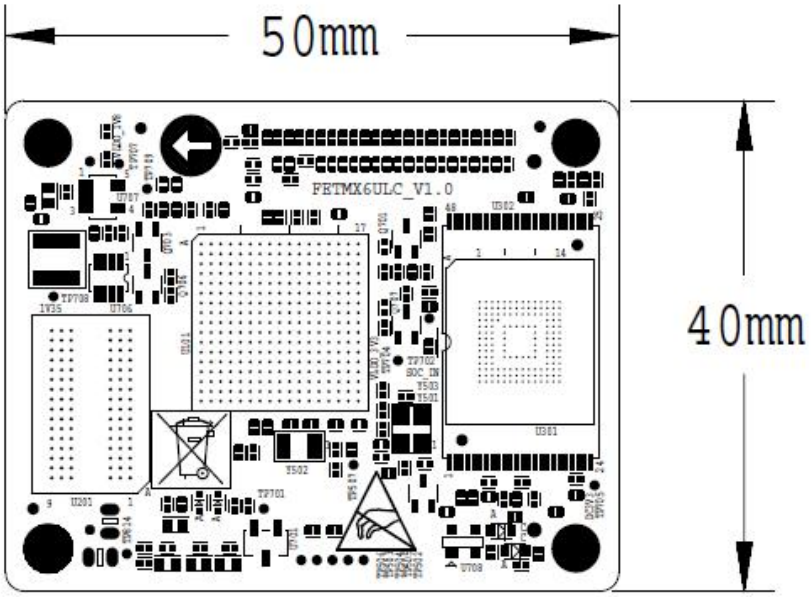
NAND Flash version

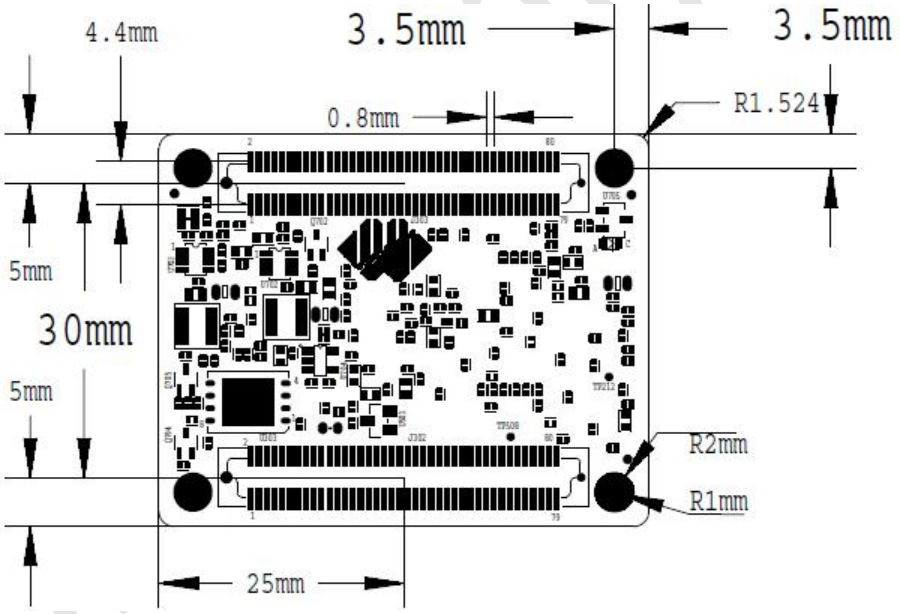


EMMC Version



2.2 FETMX6UL CPU Module Dimension





Dimension: 40mm x 50mm, tolerance ±0.15mm

Craftwork: thickness: 1.15mm, 6-layer PCB

Connectors: 2x 0.8mm pins, 80pin board-to-board connectors, **CPU module connector model**: ENG_CD_5177984, **Carrier board connector model:** ENG_CD_5177983, datasheet please refer to appendix

2.2 CPU Module Features

Hardware Item	Spec.	Model	Description
CPU	528MHz	MCIMX6G2DVM05AA	14mm x 14mm
RAM	512MB	MT41K256M16HA-125:E	LvDDR3 1600（32Meg×16×8banks）
ROM	4GB	MTFC4GACAAAM-1M WT	e.MMC
	8GB	MTFC8GACAAAM-1M WT	e.MMC

2.3 Power Supply Mode

Function	Pin	Value				Spec.
		Minimum	Classic	Maximum	Unit	
Main Power Supply	DC5V	4.5	5	5.5	V	Power adapter: 5V 2A

2.4 Working Environment

Item	Mode	Value				Spec.
		Minimum	Classic	Maximum	Unit	
Working Environment Temp	Working Environment	0	25	+70	℃	Commercial grade
	Storage environment	-40	25	+125	℃	
	Working Environment	-40	25	+85	℃	Industrial grade
	Storage environment	-40	25	+125	℃	
Humidity	Working Environment	10	—	90	%RH	None-condensing
	Storage environment	5	—	95	%RH	

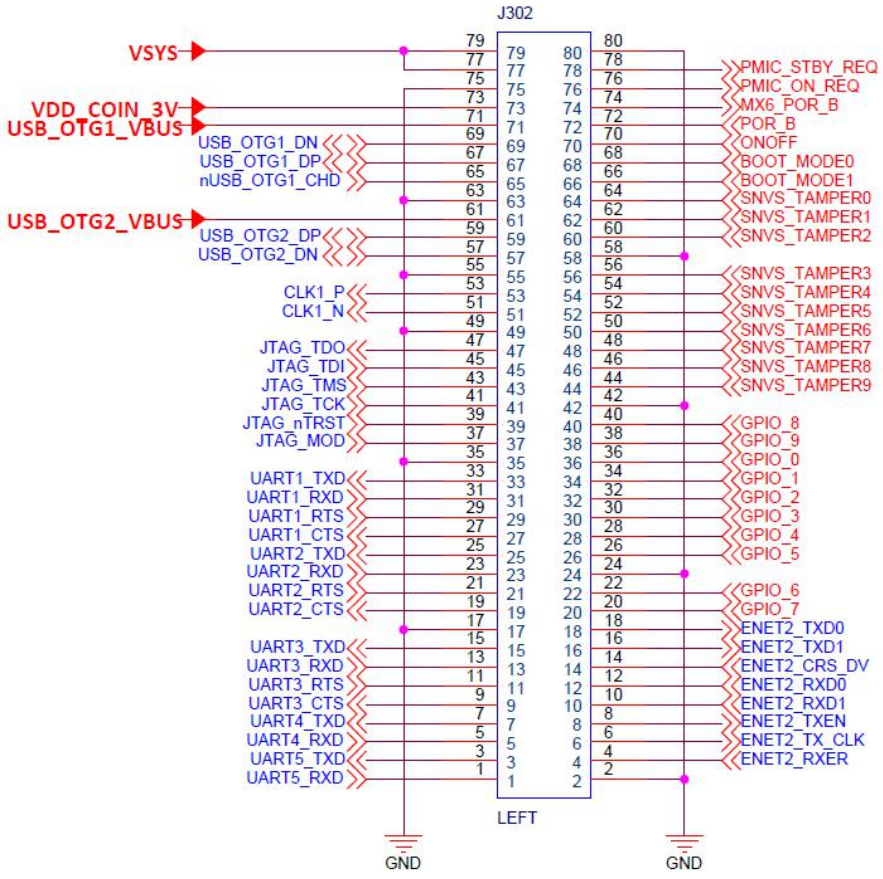
2.5 CPU Module Interface

Function	QTY	Spec.
LCD	1	RGB888, 24-bit, at up to WXGA(1366x 768) (60 Hz)
Camera	1	8-bit parallel interface (DVP), at up to 5-Megapixel
SD/MMC/SDIO	≤2	At up to UHS-I SDR104 SD and SDIO card with 1-bit or 4-bit transferring standard (up to 104MB/s)
USB	2	USB2.0 (up to 480Mbps), with integrated HS USB Phy
SAI	≤3	Supports 3x IIS audio at most
SPDIF	1	

UART	≤8	Each up to 5.0 Mbps
eCSPI	≤4	Full duplex enhanced sync. Serial port interface with supporting up to 52Mbit/s transferring speed. It could be configured to be both host/device mode with four chip selection to support multiple devices
IIC	≤4	
Ethernet	≤2	10/100Mbps
PWM	≤8	16-bit
JTAG	Supported	
Keypad Port	Supported	8*8
QSPI	1	
CAN	≤2	CAN 2.0B
ADC	≤10	2x 12-bit ADC, supports up to 10 input channels
ISO07816-3	≤2	
EBI	1	16-bit parallel bus

2.6 CPU Module Pin Definition

2.6.1 CPU module schematic



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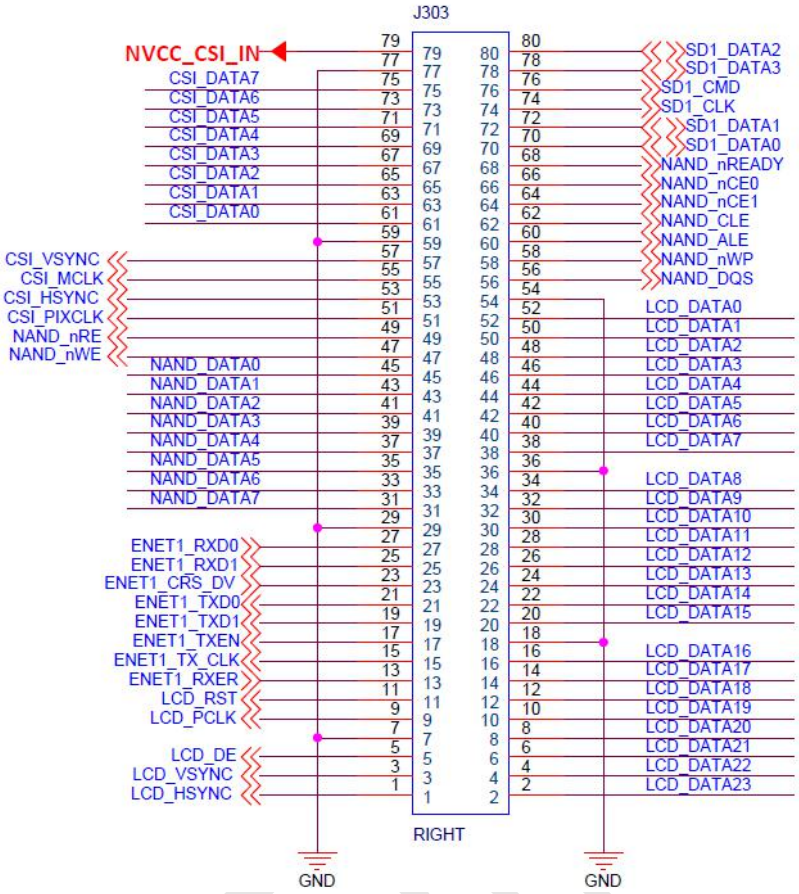


2.6.2 CPU Module FETMX6UL-C Pin Definition

LEFT(J302) connector interface (odd)

Num.	Ball	Signal	GPIO	Vol	Spec.	Function
L_1	G13	UART5_RXD	gpio1.IO[31]	3.3V	UART5 receiving	IIC2_SDA
L_3	F17	UART5_TXD	gpio1.IO[30]	3.3V	UART5 sending	IIC2_SCL
L_5	G16	UART4_RXD	gpio1.IO[29]	3.3V	UART4 receiving	IIC1_SDA
L_7	G17	UART4_TXD	gpio1.IO[28]	3.3V	UART4 sending	IIC1_SCL
L_9	H15	UART3_CTS	gpio1.IO[26]	3.3V	UART3 clear to send	CAN1_TX
L_11	G14	UART3_RTS	gpio1.IO[27]	3.3V	UART3 request to send	CAN1_RX
L_13	H16	UART3_RXD	gpio1.IO[25]	3.3V	UART3 receiving	UART3_RXD
L_15	H17	UART3_TXD	gpio1.IO[24]	3.3V	UART3 sending	UART3_TXD
L_17	-	GND				GND
L_19	J15	UART2_CTS	gpio1.IO[22]	3.3V	UART2 clear sending	CAN2_TX
L_21	H14	UART2_RTS	gpio1.IO[23]	3.3V	UART2 request to send	CAN2_RX
L_23	J16	UART2_RXD	gpio1.IO[21]	3.3V	UART2 receiving	UART2_RXD
L_25	J17	UART2_TXD	gpio1.IO[20]	3.3V	UART2 sending	UART2_TXD
L_27	K15	UART1_CTS	gpio1.IO[18]	3.3V	UART1(debug port) clear sending	UART1_CTS
L_29	J14	UART1_RTS	gpio1.IO[19]	3.3V	UART1(debug port) request to	UART1_RTS

					send	SD1_CD
L_31	K16	UART1_RXD	gpio1.IO[17]	3.3V	UART1(debug port) receive data	UART1_RXD
L_33	K14	UART1_TXD	gpio1.IO[16]	3.3V	UART1(debug port) send data	UART1_TXD
L_35	-	GND				GND
L_37	P15	JTAG_MOD	gpio1.IO[10]	3.3V	JTAG mode selection	JTAG_MOD
L_39	N14	JTAG_nTRST	gpio1.IO[15]	3.3V	JTAG test reset	JTAG_nTRST SAI2_TXD
L_41	M14	JTAG_TCK	gpio1.IO[14]	3.3V	JTAG test clock	JTAG_TCK SAI2_RXD
L_43	P14	JTAG_TMS	gpio1.IO[11]	3.3V	JTAG testing mode selection	JTAG_TMS SAI2_MCLK
L_45	N16	JTAG_TDI	gpio1.IO[13]	3.3V	JTAG test data input	JTAG_TDI SATI2_BCLK
L_47	N15	JTAG_TD0	gpio1.IO[12]	3.3V	JTAG test data output	JTAG_TD0 SAI_SYNC
L_49	-	GND		-		GND
L_51	P16	CLK1_N				CLK1_N
L_53	P17	CLK1_P				CLKI_P
L_55	-	GND				GND
L_57	T13	USB_OTG2_D-			USB host data-	USB_OTG2_D-
L_59	U13	USB_OTG2_D+			USB host data+	USB_OTG2_D+
L_61	U12	USB_OTG2_VBUS			USB host power	USB_OTG2_VBUS
L_63		GND				GND
L_65	U16	nUSB_OTG1_CHD			USB charging control terminal	USB_OTG1_CHD
L_67	U15	USB_OTG1_D+			USB OTG data+	USB_OTG1_D+
L_69	T15	USB_OTG1_D-			USB OTG data-	USB_OTG1_D-
L_71	T12	USB_OTG1_VBUS			USB OTG power	USB_OTG1_VBUS
L_73	-	VDD_COIN_3V			RTC input	BAT1
L_75	-	GND			ground	GND
L_77	-	VSYS		5V	5V power of CPU module	VDD_5V
L_79	-	VSYS		5V		VDD_5V

LEFT(J302) connector interface (even)

Num.	Ball	Signal	GPIO	Vol	Spec.	Function
L_2	-	GND	-	-	ground	GND
L_4	D16	ENET2_RXER	gpio2IO[15]	3.3V	ENET2 RMII error	ENET2_RXER
L_6	D17	ENET2_TX_CLK	Gpio2.IO[14]	3.3V	ENER2 RMII reference clock	ENET2_TX_CLK
L_8	B15	ENET2_TXEN	Gpio2.IO[13]	3.3V	ENET2 RMII sending enable	ENET2_TXEN
L_10	C16	ENET2_RXD1	Gpio2.IO[9]	3.3V	ENET2 RMII receive data1	ENET2_RXD1
L_12	C17	ENET2_RXD0	Gpio2.IO[8]	3.3V	ENET2 RMII receive data 2	ENET2_RXD0
L_14	B17	ENET2_CRS_DV	Gpio2.IO[10]	3.3V	Ethernet2 receive data enable	ENET2_CRS_DV

L_16	A16	ENET2_TXD1	gio2.IO[12]	3.3V	ENET2 RMII send data 1	ENET2_TXD1
L_18	A15	ENET2_TXD0	gio2.IO[11]	3.3V	ENET2 RMII send data 0	ENET2_TXD0
L_20	L16	GPIO_7	gpio1.IO[7]	3.3V	GPIO	ENET2_MDC
L_22	K17	GPIO_6	gpio1.IO[6]	3.3V	GPIO	ENET2_MDIO
L_24	-	GND	-	-	ground	GND
L_26	M17	GPIO_5	gpio1.IO[5]	3.3V	GPIO (don't use on base board	GPIO_5
L_28	M16	GPIO_4	gpio1.IO[4]	3.3V	GPIO	GPIO_4
L_30	L17	GPIO_3	gpio1.IO[3]	3.3V	GPIO	GPIO_3
L_32	L14	GPIO_2	gpio1.IO[2]	3.3V	GPIO	GPIO_2
L_34	L15	GPIO_1	gpio1.IO[1]	3.3V	GPIO	GPIO_1
L_36	K13	GPIO_0	Gpio1.IO[0]	3.3V	GPIO	USB_OTG1_ID
L_38	M15	GPIO_9	gpio1.IO[9]	3.3V	GPIO	LED3 SD1_NRST
L_40	N17	GPIO_8	gpio1.IO[8]	3.3V	GPIO	BLP_PWM
L_42	-	GND	-	-	ground	GND
L_44	R6	SNVS_TAMPER9	gpio5.IO[9]	3.3V	SNVS TAMPER input 9	LED2 LCD_DISP
L_46	N9	SNVS_TAMPER8	gpio5.IO[8]	3.3V	SNVS TAMPER input 8	SHIFT_NOE
L_48	N10	SNVS_TAMPER7	gGpio5.IO[7]	3.3V	SNVS TAMPER input 7	SHIFT_STCP
L_50	N11	SNVS_TAMPER6	gpio5.IO[6]	3.3V	SNVS TAMPER input 6	E
L_52	N8	SNVS_TAMPER5	Gpio5.IO[5]	3.3V	SNVS TAMPER input 5	ENET1_NINT
L_54	P9	SNVS_TAMPER4	Gpio5.IO[4]	3.3V	SNVS TAMPER input 4	AUD_INT
L_56	P10	SNVS_TAMPER3	Gpio5.IO[3]	3.3V	SNVS TAMPER input 3	SNVS_TAMPER3
L_58	-	GND		3.3V	ground	GND
L_60	P11	SNVS_TAMPER2	Gpio5.IO[2]	3.3V	SNVS TAMPER input 2	PERI_PWREN
L_62	R9	SNVS_TAMPER1	Gpio5.IO[1]	3.3V	SNVS TAMPER input 1	TP_INT
L_64	RI0	SNVS_TAMPER0	Gpio5.IO[0]	3.3V	SNVS TAMPER input 0	ACC_INT
L_66	UI0	BOOT_MODE1	Gpio5.IO[11]	3.3V	Booting mode select 1	SHIFT_SHCP BOOT_MODE1
L_68	T10	BOOT_MODE0	Gpio5.IO[10]	3.3V	Booting mode select 1	SHIFT_SDI BOOT_MODE0
L_70	R8	ONOFF	-	-	Power switch, if users do not need it, just hang it	ONOFF
L_72	P8	POR_B	-	-	Reset pin, if not need, hang it	POR_B
L_74	-	MX6_POR_B	-	-	CPU module power off reset, low level valid	MX6_POR_B
L_76	T9	PMIC_ON_REQ			Control GEN_5V and GEN_3.3V on carrier board, high level valid	PMIC_ON_REQ
L_78	U9	PMIC_STBY_REQ	-	-	PMIC Standby signal, used for VDD_SOC_IN voltage (do not use it for carrier board)	PMIC_STBY_REQ

L_80	-	GND	-	-	ground	GND

RIGHT (J303) connector (odd) pin definition

Num.	Ball	Signal	GPIO	Vol	Spec.	Function
R_2	D9	LCD_HSYNC	Gpio3.IO[2]	3.3V	RGB horizontal sync. signal	LCD_HSYNC
R_3	C9	LCD_VSYNC	Gpio3.IO[3]	3.3V	RGB vertical sync. signal	LCD_VSYNC
R_5	B8	LCD_DE	Gpio3.IO[1]	3.3V	RGB data enable signal	LCD_DE
R_7	-	GND		OV	ground	GND
R_9	A8	LCD_PCLK	Gpio3.IO[0]	3.3V	RGB pixel clock signal	LCD_PCLK
R_11	E9	LCD_RST	Gpio3.IO[4]	3.3V	RGB reset signal (inavailable)	LCD_RST
R_13	D15	ENET1_RXER	Gpio2.IO[7]	3.3V	ENETI RMII frame error	ENET1_RXER
R_15	F14	ENET1_TX_CLK	gio2.IO[6]	3.3V	ENET1 RMII reference clcok	ENET1_TX_CLK
R_17	F15	ENET1_TXEN	gio2.IO[5]	3.3V	ENET1 RMII send enable	ENET1_TXEN
R_19	E14	ENET1_TXD1	Gpio2.IO[4]	3.3V	ENET1 RMII send data 1	ENET1_TXD1
R_21	E15	ENET_TXDO	Gpio2.IO[3]	3.3V	ENET1 RMII send data 0	ENET1_TXD0
R_23	E16	ENET1_CRS_DV	-gpio2.IO[2]	3.3V	ENET1 RMII RX_EN, CRS	ENET1_CRS_DV
R_25	E17	ENET1_RXD1	Gpio2.IO[1]	3.3V	ENET1 RMII receive data 1	ENET1_RXD1
R_27	F16	ENET1_RXD0	Gpio2.IO[0]	3.3V	ENET1 RMII receive data 0	ENET1_RXD0
R_29	-	GND			GND	GND
R_31	A5	NAND_DATA7	Gpio4.IO[9]	3.3V	NAND data 7 (not for carrier board	NAND_DATA7
R_33	A6	NAND_DATA6	Gpio4.IO[8]	3.3V	NAND data 6(not for carrier board)	NAND_DATA6
R_35	B6	NAND_DATA5	Gpio4.IO[7]	3.3V	NAND data 5(not for carrier board)	NAND_DATA5
R_37	C6	NAND_DATA4	Gpio4.IO[6]	3.3V	NAND data 4(not for carrier board)	NAND_DATA4
R_39	D6	NAND_DATA3	Gpio4.IO[5]	3.3V	NAND data 3(not for carrier board)	NAND_DATA3
R_41	A7	NAND_DATA2	Gpio4.IO[4]	-	NAND data 2(not for carrier board)	NAND_DATA2
R_43	B7	NAND_DATA1	Gpio4.IO[3]	3.3V	NAND data 1(not for carrier board)	NAND_DATA1
R_45	D7	NAND_DATA0	Gpio4.IO[2]	3.3V	NAND data 0(not for carrier board)	NAND_DATA0
R_47	C8	NAND_nWE	gGpio4.IO[1]	3.3V	NAND write (not for carrier board)	NAND_nWE
R_49	D8	NAND_nRE	Gpio4.IO[0]	3.3V	NAND read control (not for carrier board)	NAND_nRE
R_51	E5	CSI_PIXCLK	Gpio4.IO[18]	3.3V	Digital camera pixel clock in	CSI_PIXCLK
R_53	E3	CSI_HSYNC	Gpio4.IO[20]	3.3V	Digital camera horizontal sync. input	CSI_HSYNC
R_55	F5	CSI_MCLK	Gpio4.IO[17]	2.7V	Digital camera main clock input	CSI_MCLK

R_57	F2	CSI_VSYNC	Gpio4.IO[19]	2.73V	Digital camera vertical sync. input	CSI_VSYNC
R_59		GND				GND
R_61	E4	CSI_DAT0	Gpio4.IO[21]	2.7V	8bit digital camera data0 input	CSI_DAT0
R_63	E3	CSI_DAT1	Gpio4.IO[22]	2.7V	8bit digital camera data1 in	CSI_DAT1
R_65	E2	CSI_DAT2	Gpio4.IO[23]	2.7V	8bit digital camera data2 in	CSI_DAT2
R_67	E1	CSI_DAT3	Gpio4.IO[24]	2.7V	8bit digital camera data 3 in	CSI_DAT3
R_69	D4	CSI_DAT4	Gpio4.IO[25]	2.7V	8bit digital camera data 4 in	CSI_DAT4
R_71	D3	CSI_DAT5	Gpio4.IO[26]	2.7V	8bit digital camera data 5 in	CSI_DAT5
R_73	D2	CSI_DAT6	Gpio4.IO[27]	2.7V	8bit digital camera data 6 in	CSI_DAT6
R_75	D1	CSI_DAT7	Gpio4.IO[28]	2.7V	8bit digital camera data 7 in	CSI_DAT7
R_77		GND	-	-		GND
R_79	-	NVCC_CSI_IN	-	-	CPU internal camera power	NVCC_CSI_IN

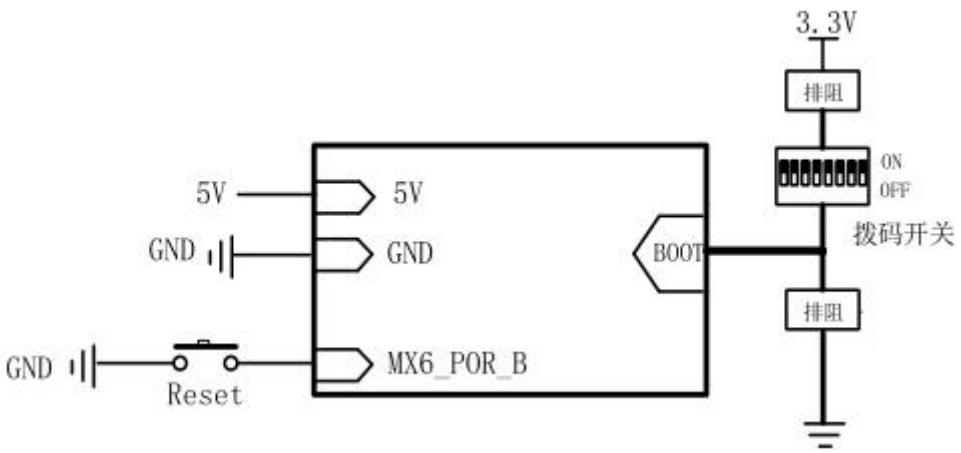
RIGHT(J303) connector interface (even)

Num.	Ball	Signal	GPIO	Vol	Spec.	Function
R_2	B16	LCD_DATA23	Gpio3.IO[28]	3.3V	Red data bit 7(high)	LCD_DATA23
R_4	A14	LCD_DATA22	Gpio3.IO[27]	3.3V	Red data bit 6	LCD_DATA22
R_6	B14	LCD_DATA21	Gpio3.IO[26]	3.3V	Red data bit 5	LCD_DATA21
R_8	C14	LCD_DATA20	Gpio3.IO[25]	3.3V	Red data bit 4	RCD_DATA20
R_10	D14	LCD_DATA19	Gpio3.IO[24]	3.3V	Red data bit 3	RCD_DATA19
R_12	A13	LCD_DATA18	Gpio3.IO[23]	3.3V	Red data bit 2	RCD_DATA18
R_14	B13	LCD_DATA17	Gpio3.IO[22]	3.3V	Red data bit 1	RCD_DATA17
R_16	C13	LCD_DATA16	Gpio3.IO[21]	3.3V	Red data bit 0 (low)	RCD_DATA16
R_18		GND		OV		GND
R_20	D13	LCD_DATA15	Gpio3.IO[4]	3.3V	Green data bit 7(high)	LCD_DATA15
R_22	A12	LCD_DATA14	Gpio3.IO[19]	3.3V	Green data bit 6	LCD_DATA14
R_24	-	LCD_DATA13	Gpio3.IO[18]	3.3V	Green data bit 5	LCD_DATA13
R_26	M17	LCD_DATA12	Gpio3.IO[17]	3.3V	Green data bit 4	LCD_DATA12
R_28	M16	LCD_DATA11	Gpio3.IO[16]	3.3V	Green data bit 3	LCD_DATA11
R_30	R17	LCD_DATA10	Gpio3.IO[15]	3.3V	Green data bit 2	LCD_DATA10
R_32	R14	LCD_DATA9	Gpio3.IO[14]	3.3V	Green data bit 1	LCD_DATA9
R_34	R15	LCD_DATA8	Gpio3.IO[13]	3.3V	Green data bit 0 (low)	LCD_DAT8
R_36		GND				GND
R_38	D11	LCD_DATA7	Gpio3.IO[12]	3.3V	Blue data bit 7(high)	LCD_DATA7
R_40	A10	LCD_DATA6	Gpio3.IO[11]	3.3V	Blue data bit 6	LCD_DATA6
R_42	B10	LCD_DATA5	Gpio3.IO[10]	3.3V	Blue data bit 5	LCD_DATA5
R_44	C10	LCD_DATA4	Gpio3.IO[9]	3.3V	Blue data bit 4	LCD_DATA4
R_46	D10	LCD_DATA3	Gpio3.IO[8]	3.3V	Blue data bit 3	LCD_DATA3
R_48	E10	LCD_DATA2	Gpio3.IO[7]	3.3V	Blue data bit 2	LCD_DATA2
R_50	A9	LCD_DATA1	Gpio3.IO[6]	3.3V	Blue data bit 1	LCD_DATA1

R_52	B9	LCD_DATA0	Gpio3.IO[5]	3.3V	Blue data bit 0(low)	LCD_DATA0
R_54		GND				GND
R_56	E6	NAND_DQS	Gpio4.IO[16]	3.3V	NAND mode selection	NAND_DQS
R_58	D5	NAND_nWP	Gpio4.IO[11]	3.3V	NAND write protection (only for emmc version module)	NAND_nWP
R_60	B4	NAND_ALE	Gpio4.IO[10]	3.3V	NAND address lock enable (only for emmc version module)	NAND_ALE
R_62	A4	NAND_CLE	Gpio4.IO[15]	3.3V	NAND command lock enable (only for emmc version module)	NAND_CLE
R_64	B5	NAND_nCE1	Gpio4.IO[14]	3.3V	NAND chip select signal 1	NAND_nCE1
R_66	C5	NAND_nCE0	Gpio4.IO[13]	3.3V	NAND chip select signal 0(only for emmc version)	NAND_nCE0
R_68	A3	NAND_nREADY	Gpio4.IO[12]	3.3V	NAND busy signal (only for emmc version module)	NAND_nREADY
R_70	B3	SD1_DATA0	Gpio4.IO[18]	3.3V	SD/MMC1 data 0	SD1_DATA0
R_72	B2	SD1_DATA1	Gpio4.IO[19]	3.3V	SD/MMC data 1	SD1_DATA1
R_74	C1	SD1_CLK	Gpio4.IO[17]	3.3V	SD/MMC1 clock	SD1_CLK
R_76	C2	SD1_CMD	Gpio4.IO[16]	3.3V	SD/MMC1 command signal	SD1_CMD
R_78	A2	SD1_DATA3	Gpio4.IO[21]	3.3V	SD/MMC1 data 3	SD1_DATA3
R_80	B1	SD1_DATA2	Gpio4.IO[20]	3.3V	SD/MMC1 data 2	SD1_DATA2

2.7 CPU Module Design

FETMX6UL-C CPU module is integrated with power, reset circuit, memory, available for minimum OS, system just need 5V power, reset, boot mode setting.



we kindly recommend users to connect the module with peripheral devices such as debug power, otherwise, we could not assure whether system booted.

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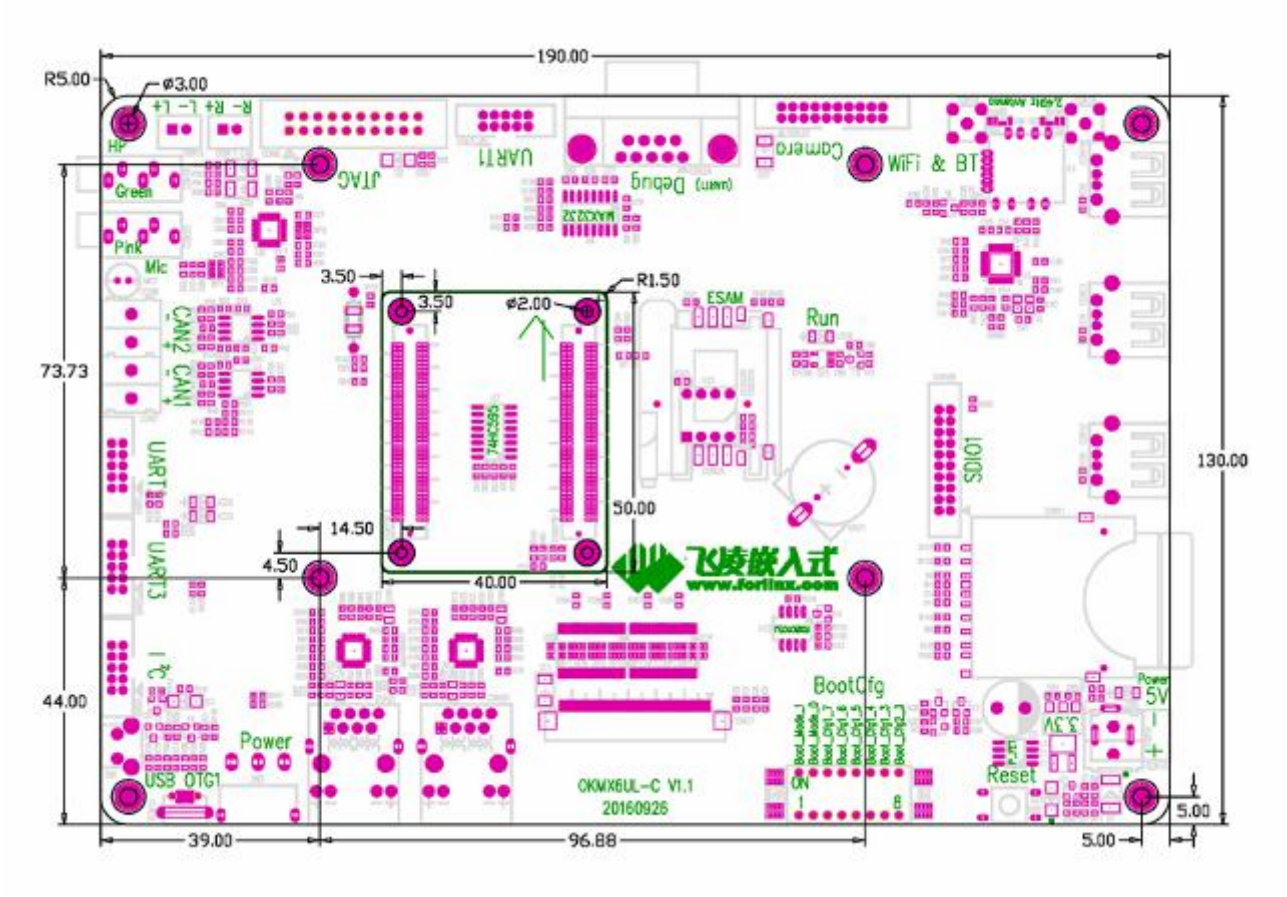
Chapter 3 i.MX6UR Development Platform Overview

3.1 Overview of single board computer i.MX6UR

3.2 Carrier Board Dimension



Dimensions: 130mm×190mmrectangRe PCB

Mounting hole: space: 120mm x 180mm, pad diameter: 5mm, pore diameter: 3mm.

Manufacture: thickness of 1.6mm, 4-Rayer full hole PCB and other Revel oil hole.

Power supply: DC5V

3.3 Base board resource:

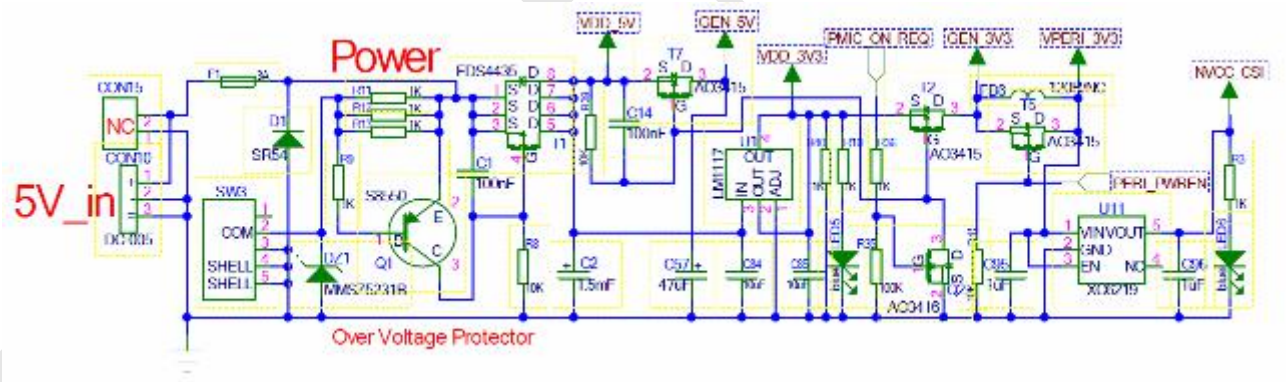
Item	QTY	Spec.
RCD	1	RGB888, WXGA at up to 1366x 768 (60Hz)
Camera	1	8-bit parallel interface (DVP), at up to 5.0 Megapixel: OV5640
Audio	1	1x MIC, 1x Phone, 2x Speaker
USB Host	3	Expanded by hub, USB 2.0 (up to 480Mbps)
USB OTG	1	Micro USB 2.0 OTG (up to 480Mbps)
Ethernet	2	10/100Mbps, RJ45
WIFI	1	RL-UM02WBS-8723BU-V1.2
BT	1	

SD card	1	Compatible with SD, SDHC, SDXC (UHS-I)
SDIO	1	2mmx 20pin, multi-plexed with memory card port
RED	2	
PWM	1	RCD backlight
ADC	4	For resistive touching
IIC	2	
CAN	2	CAN2.0B, DG128-2P
UART	2	5-wire serial port, all are 3.3V power Revel, each at up to 5.0 Mbps
UART Debug	1	RS232, DB9 port
JTAG Debug		

3.4 i.MX6UR Base Board Introduction

3.4.1 Base Board Power

The DC5V power was drew by the DC-005 jack or DC128-5.0 green terminal. This power adapter go through (Self-) Resettable fuse, anti reverse diode and circuit over-voltage protection, then through RM1117 to reduce to 3.3V, neither of these two powers are under control, and their network names are VDD_5V and VDD_3.3V. VDD_5V and VDD_3.3V. are controlled by PMIC_ON_REQ pin, and could be output GEN_5V and GEN_3V3. GEN_3V3 controlled by PERI_PWREN pin to output VPERI_3V3, and output NVCC_CSI from XC6219, to supply power to CPU internal camera circuit. ARR on-board circuits are supplied power by the above power.



3.4.2 Power Switch

SW1 on left bottom corner of base board is the power switch key.

3.4.3 Reset Key

SW2 on right bottom corner of base board is the reset key.

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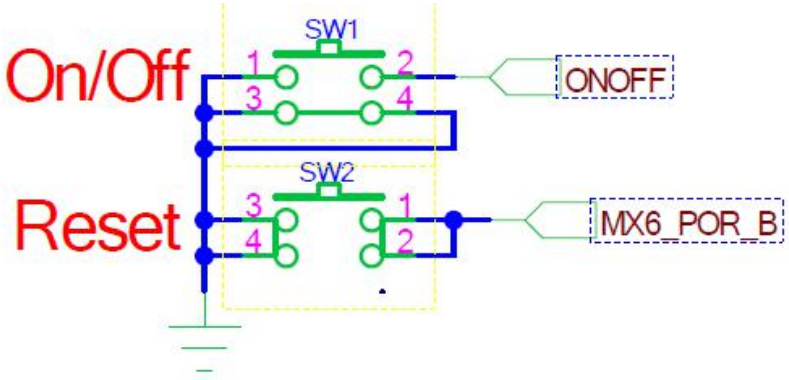


3.4.4 Boot Configuration

Different file flashing and booting modes are available for i.MX6UR,. the booting configuration pins are BOOT_MODE0、BOOT_MODE1、LCD_DATA3~LCD_DATA7、

BOOT_MODE0, BOOT_MODE1 are pins for BOOT_TYPE selection

BMODE[1：0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot(Development)
11	Reserved

RCD_DATA3~RCD_DATA7 and RCD_DATA11 are pins for Boot_Device selection

Boot Device	LCD_D7	LCD_D6	LCD_D5	LCD_D4	LCD_D3	LCD_D11
QSPI	0	0	0	1	x	x
WEIM	0	0	0	0	Memory Type: 0-NOR-Flash 1-OneNAND	x
Serial-ROM	0	0	1	1	x	x
SD/eSD	0	1	0	x	x	0-SDHC1 1-SDHC2
MMC/eMMC	0	1	1	x	x	
NAND	1	x	x	x	x	x

SDHC1 port on base board is for SD card, and SDHC2 interface if for eMMC on CPU module, SW4 is a configuration key for single board computer booting. Below modes are available

1. Flash OS image via SD card: On(up)1, 4

   Off(down) 2, 3, 5, 6, 7, 8

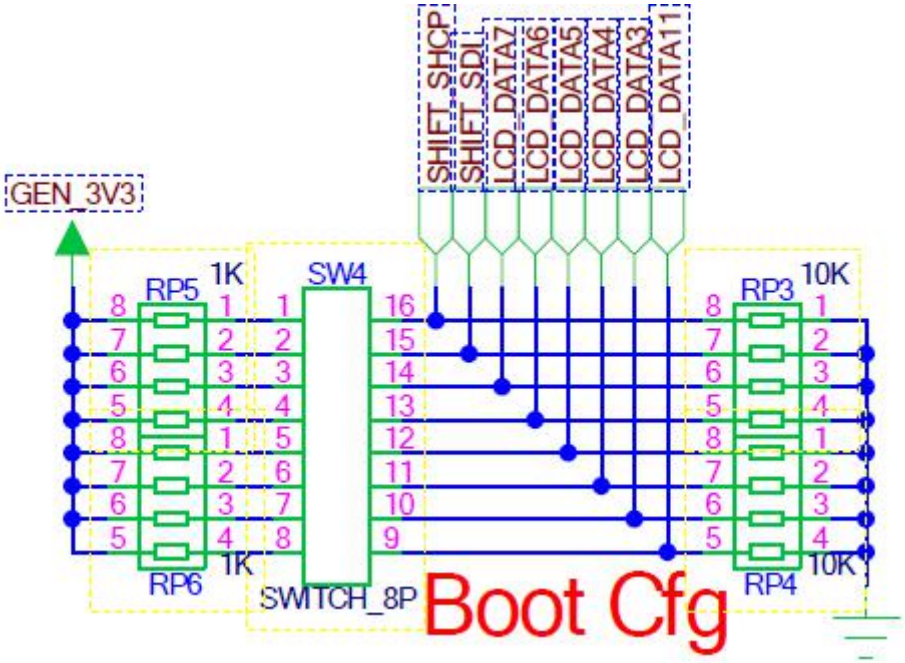
2. Flash OS image via USB OTG: key 1 off, others are all to off,

3. Boot from eMMC: On: 1, 4, 5, 8

   Off: 2, 3, 6, 7

3. Boot from NAND Flash: on: 1, 3

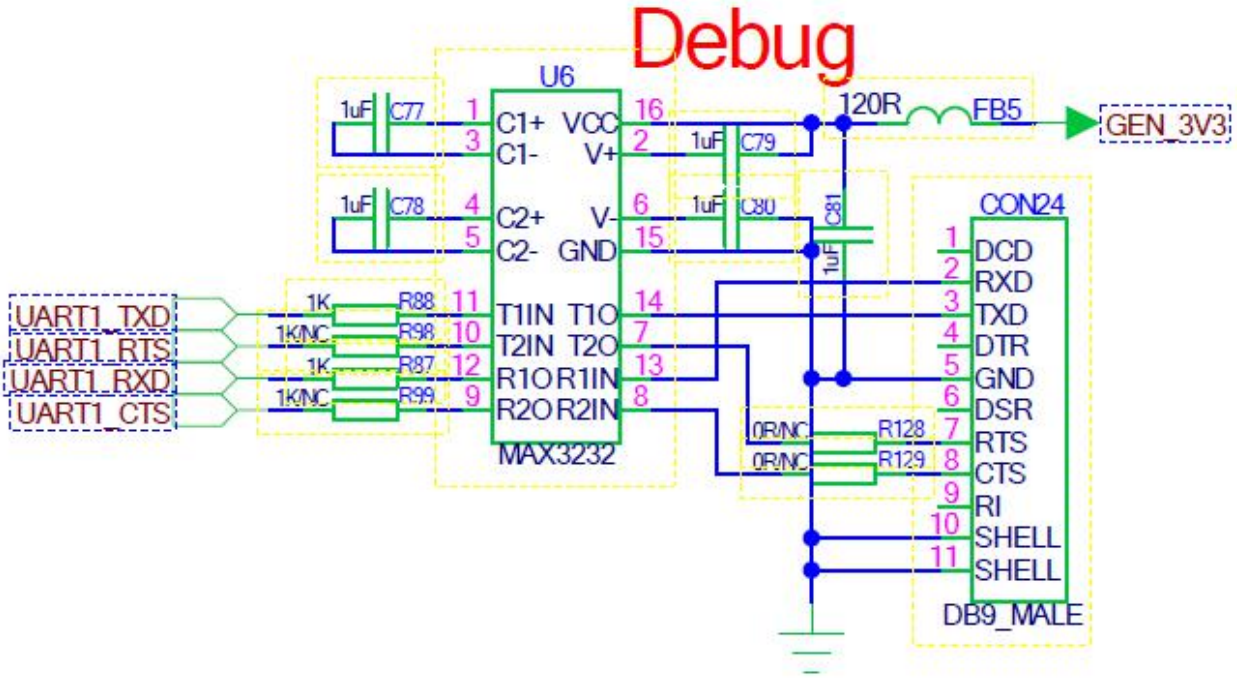
   Off: 2, 4, 5, 6, 7, 8



3.4.5 Serial Port (Debug Port)

The debug port is a standard RS232 port with 9 pins, could be connected to PC via a DB9 male connector. If without serial port on PC, it could be connected via USB-to-RS232 cable.

The UART1 is a debug port with 5-wire and 3.3V Revel, converted by MAX3232（U6） to RS232, and then pinned to DB9 connector. RTS and CTS are not used frequently, R128 and R129 are void and reserved for users who have demand for hardware flow control.



Besides, UART1 was directly pinned out by connector with 20-p and 2mm pitch (CON3), is not recommended to

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be used

As a general serial port for below reasons:

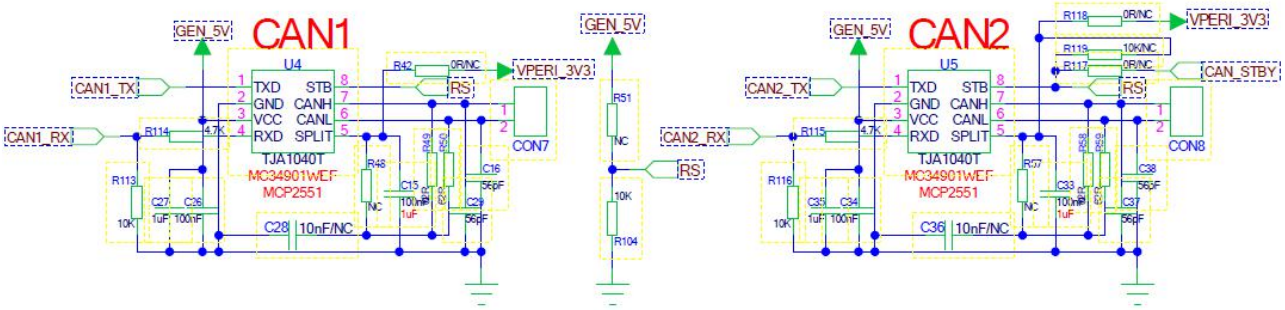
1. R87 have to be removed to avoid effect of U6
2. Software change is also need to configure it to be a general serial port

3.4.6 General Serial Port

Both UART2 and UART3 are 5-wired serial port with 3.3V Revel, and are pinned out by CON4 and CON5. They could be used matched with Forlinx module, to convert 3.3V Revel to RS232 and RS485.

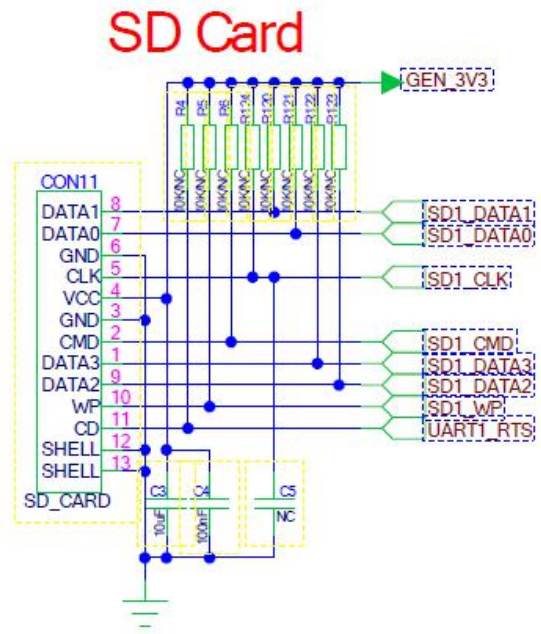
3.4.7 CAN

Two CAN ports are available on base board, both are pinned out by DC128-5.0 green terminal and numbered asCON7 and CON8. Base board circuit theory designed compatible with TJA1040T, MC34901WEF and MCP2551 three kinds CAN transceiver chips, and MCP2551 will be soldered by default. As the MCP2551 output RX is 5V, it my effect the CPU module 3.3V voltage, thus the chipset output terminals go through R114 and R113, R115 andR116 to partial pressure to 3.3V, then input to CAN1_RX and CAN2_RX of the CPU.



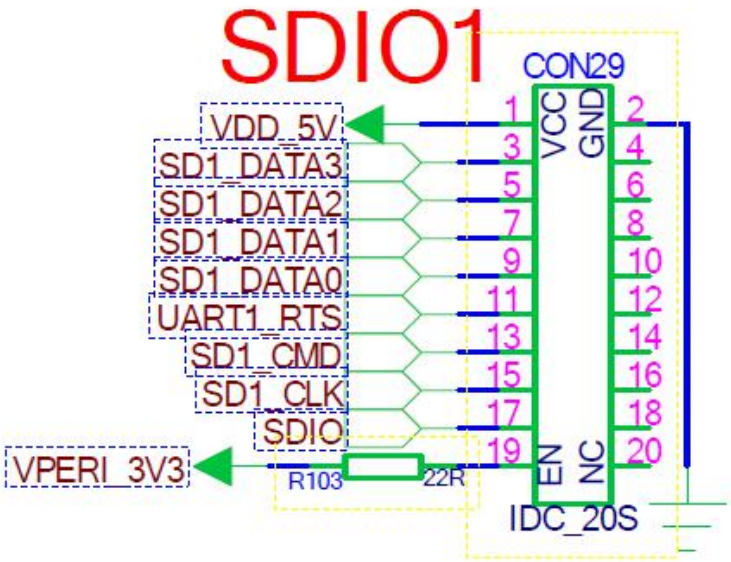
3.4.8 SD Card Slot

CON11 is the SD card slot, it's from SDHC1 port of CPU, users could set system file flashing from SD card by settings of DIP switch. This port is available for SD card, SDHC card and SDXC(UHS-A) card. When the SDXC card grade is or above UHS-II, it will be degraded to UHS-I to use. Because new data pins(compared with USB3.0) are added begin from UHS-II.



3.4.9 SDIO Port

SDIO shares the same SDHC1 port with SD card slot, and it could be matched with Forlinx SDIO WIFI module RTR8189ES. This port was pinned out by a 20-pin 2mm pitch(CON29) connector



3.4.10 RTC Battery

The CPU is with RTC and it also supports external RTC. We selected to use external RTC considering CPU RTC power consumption. The battery model is CR1220

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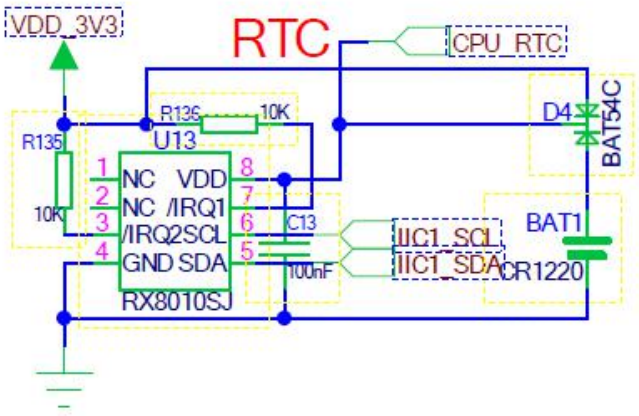
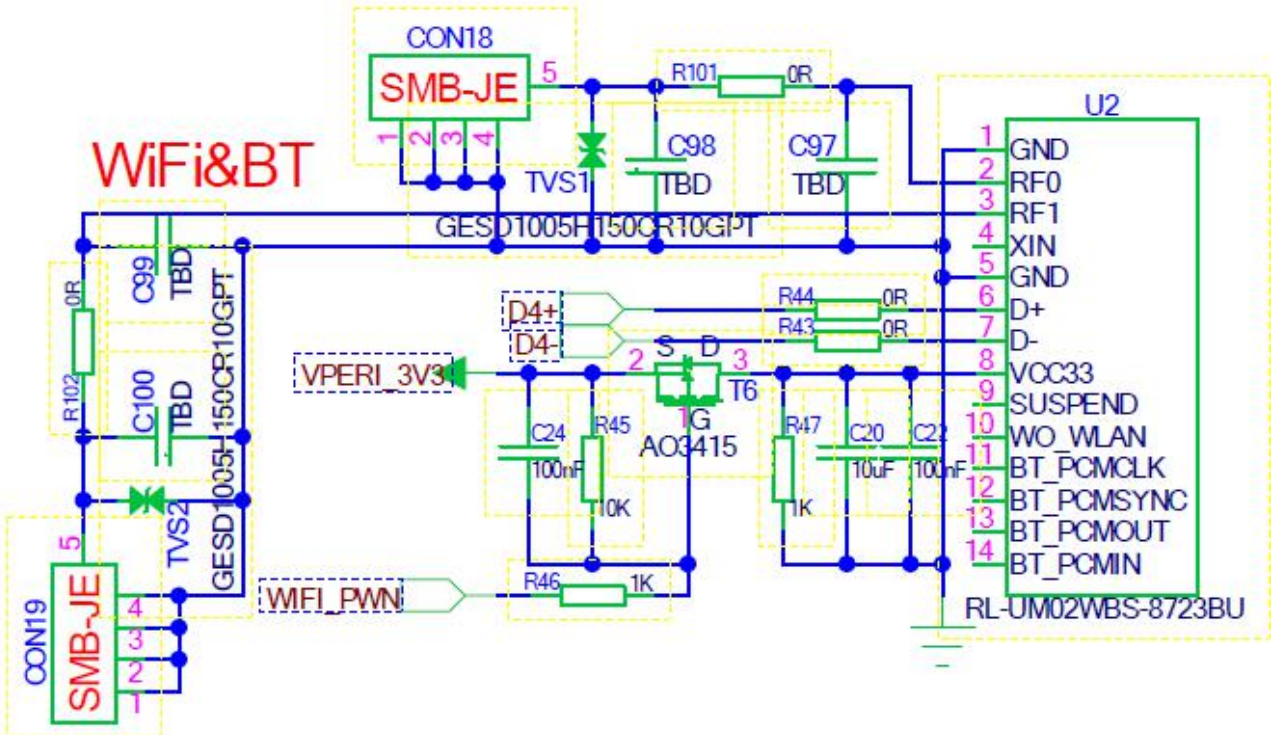


3.4.11 WIFI/Bluetooth

The WIFI&BT coexistence model is RR-UM02WBS-8723BU-V1.2，IEEE 802.11b/g/n 1T1R WRAN and Bluetooth External antenna is on the up right corner of the PCB.



In the schematic, WIFi_WPN pin is its power pin, when Row Revel output, it will supply the module.
This module has host and vice two antennas, the host antenna could send and receive data, the vice antenna could only used for data receiving

3.4.12 Digital Camera Interface

Digital camera port was pinned out from CON23 with 20-p, 2.0mm pitch

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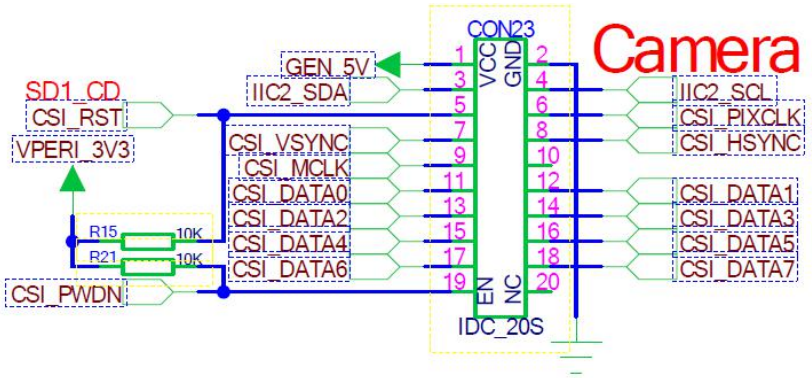
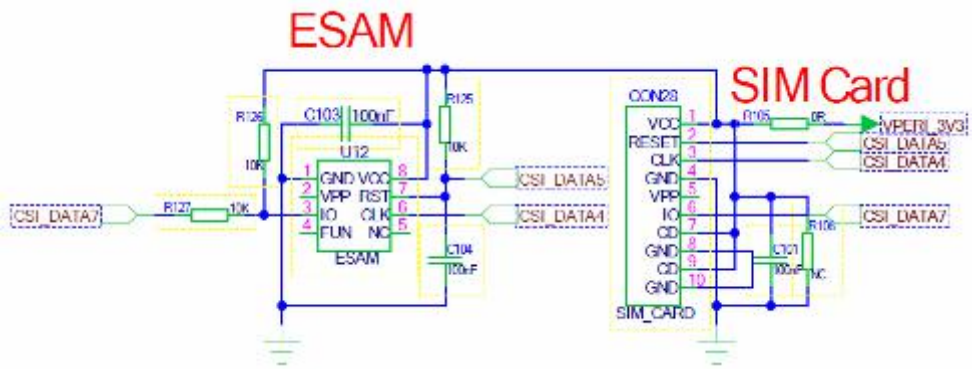


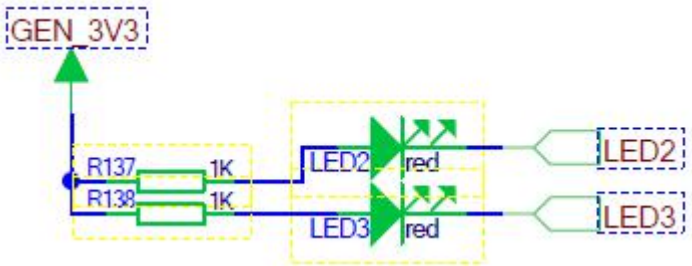
3.4.13 ESAM Interface

One ISO7816 is available on single board computer i.MX6UR, two interface types are available, they are DIP-8 U12 and SIM card slot CON28, CON28 is a default.



3.4.14 RED

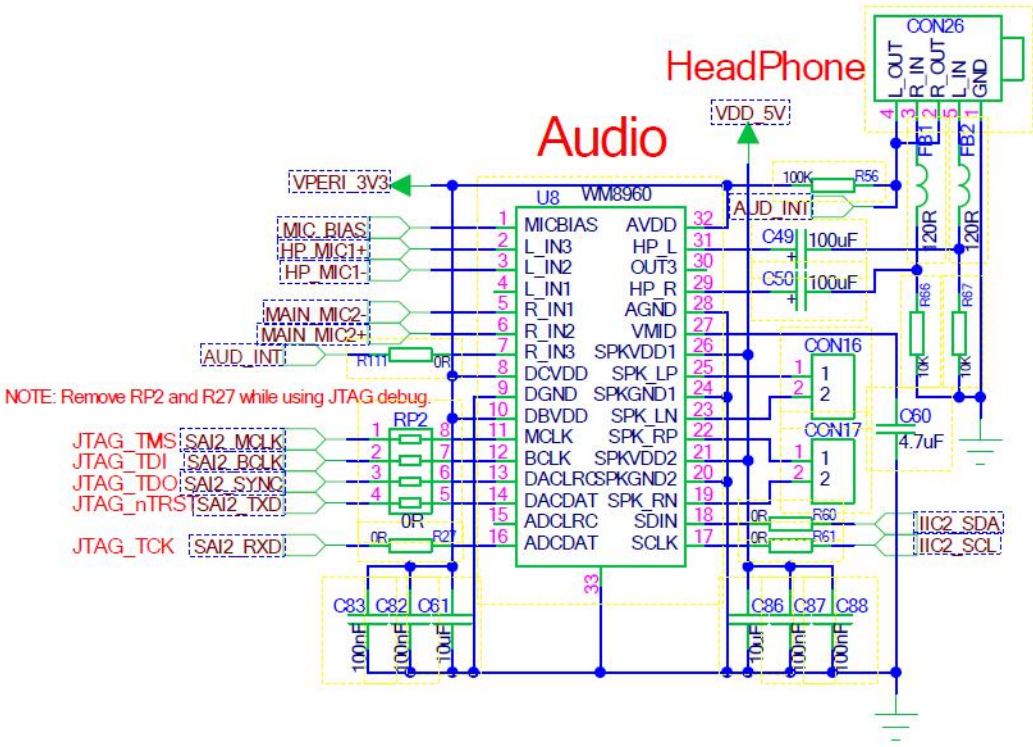
2x RED are available on single board computer i.MX6UR, they are RED2 and RED3, to use RED, users should configure the pin(s) to GPIO, when output Rower power Revel, the RED will be lightened, while when output a high power Revel, the RED will be closed



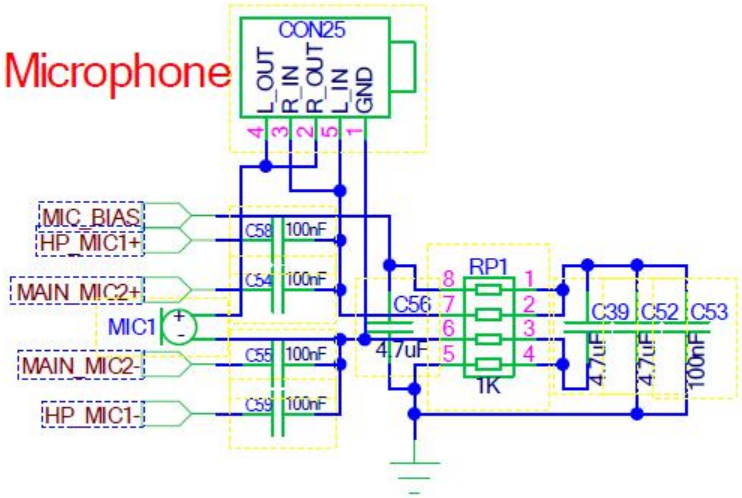
3.4.15 Audio

Two 3.5mm standard stereo audio jacks are avaiRabRe on base board, earphone output(CON26, green) and

micphone input(CON25, red), besides, another two XH2.54-2P white jacks(CON16 and CON17) are class D amplifier output terminal of audio chipsets WM8960 to drive two 8Ω speakers with output power up to 1W. Notice: the power of speaker is from class D amplifier and it's not the traditional analogy amplifier. Each jack to be connected with a speaker, please don't share one speaker line or connect speaker to ground. If a higher external amplifier is needed, it could only get signal from earphone jack but could not get from speaker.



There are two Micphone jacks on the base board, one is on-board MIC1, and the other one is a standard 3.5mm stereo audio jack CON25. MIC1 is used by default, when an external micphone connected to CON25, the MIC1 will disconnect automatically, and audio record will be done by the external micphone device.



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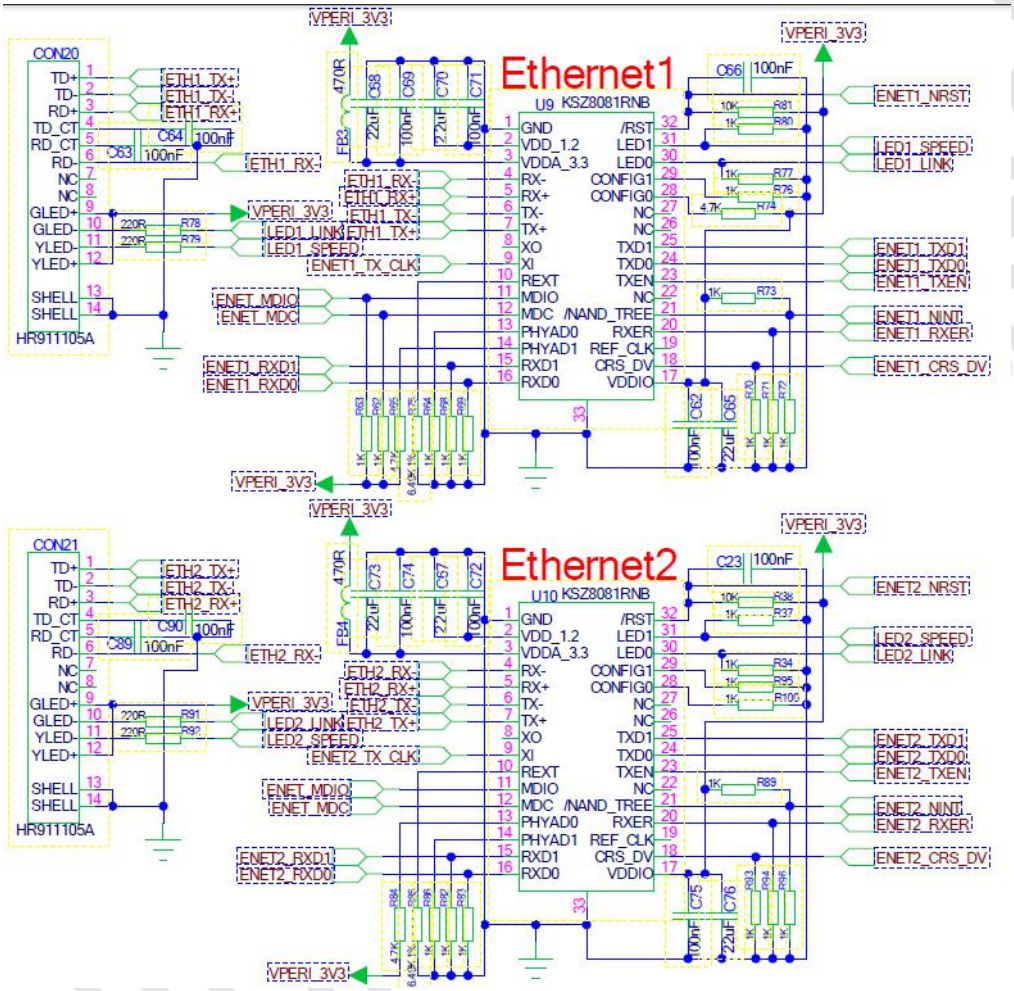
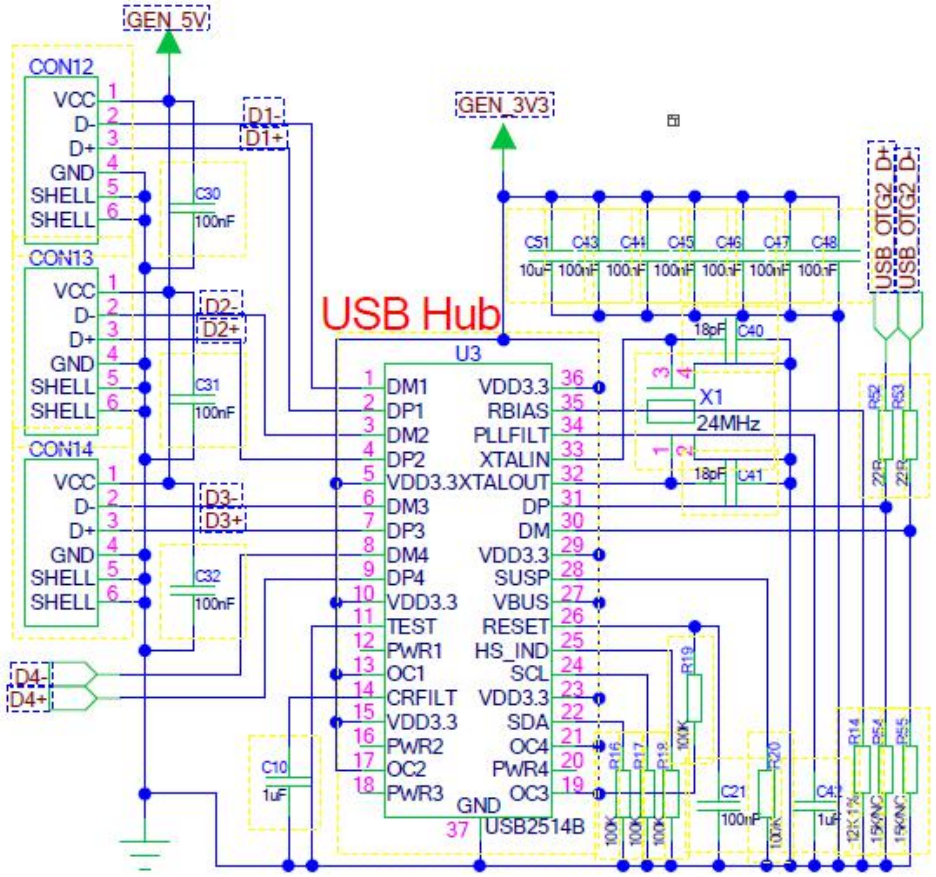
3.4.16 Dual Hundred Ethernet Ports

Two Ethernet ports are available on base board, and both are connected with PHY chipset KSZ8081 via RMII. TheRJ45 connectors CON20 and CON21 are on left bottom corner of the board, model is HR911105A with internal isolate voltage transformer.



3.4.17 USB Host

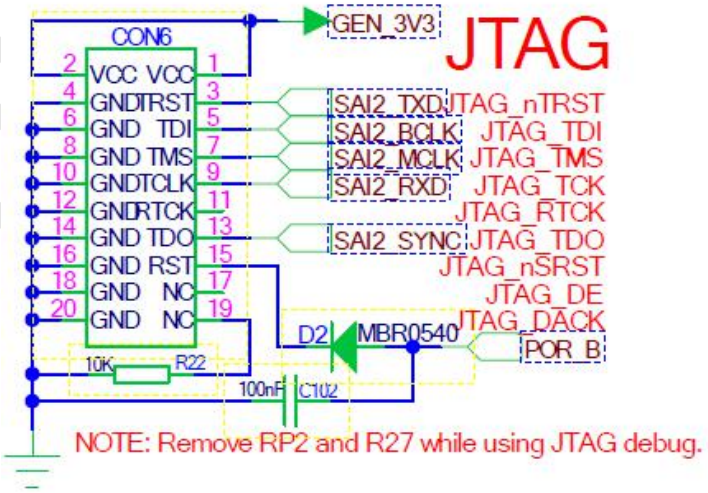
The USB-OTG2 on i.MX6UR was designed to expand the board with 3x USB host 2.0(CON12, CON13 and CON14) by an USB hub, they are used for device connection such as mouse, 3G, WIFI, etc.



3.4.18 JTAG Debug Port

This board is with JTAG port (CON6), which is convenient for users to do emulator debug the board.

Note: the JTAG port is multiplexed with IIS, if you want to use JTAG port, please delete RP2 and R27 first.



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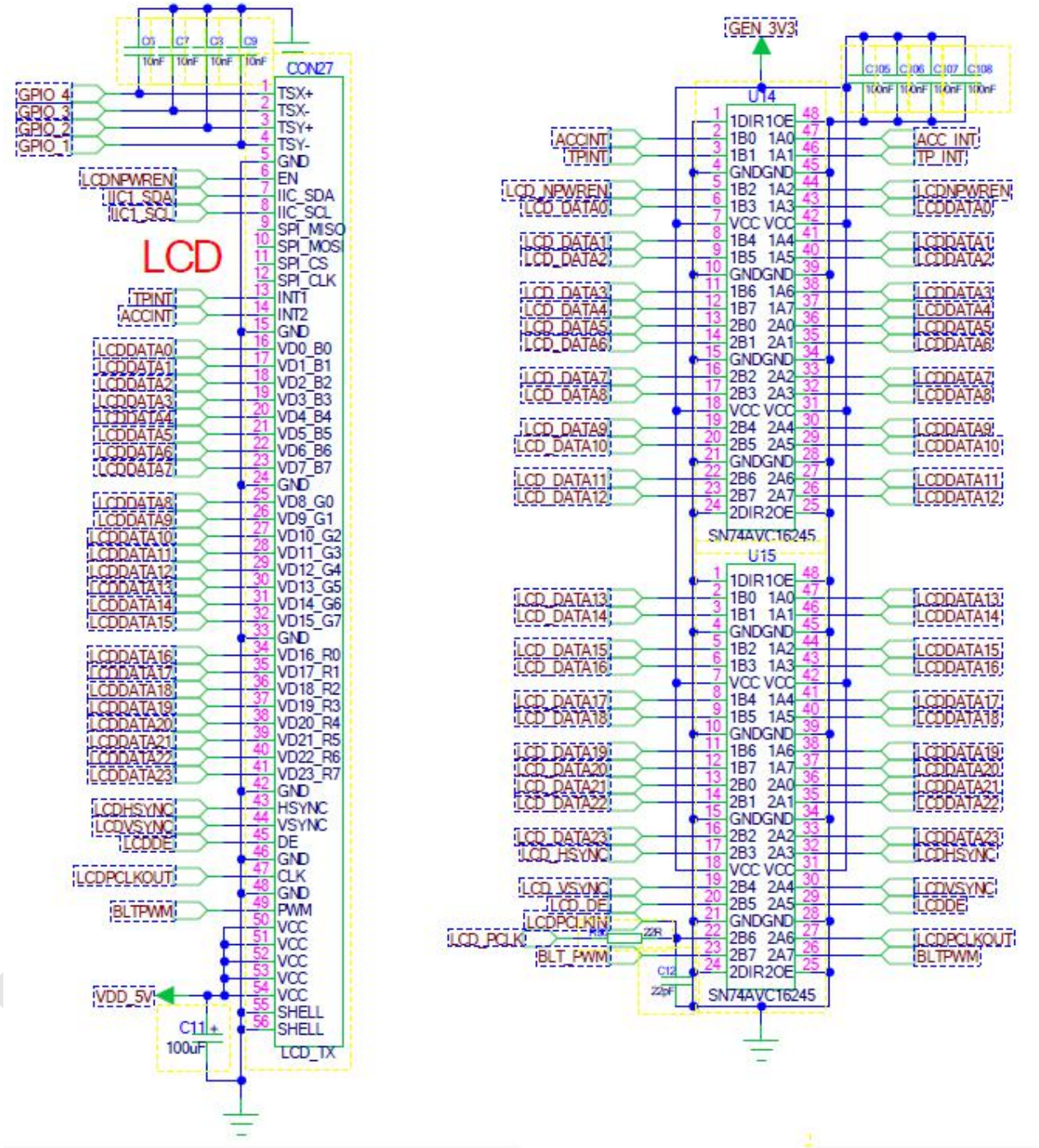
3.4.19 RCD Connector

The board is with a general RCD interface, it's pinned out by a FPC connector(CON27) with 54-pin and 0.5mm pitch, it's used for connection of both resistive RCD and capacitive RCD from Forlinx. This display port is RGB888 24-bit



Note:1. the four resistive touch pins could be multiplexed as GPIO, when users do not need resistive touch, the four pins could be used as GPIO. The four pins are pinned out from IIC, UART1, UART2 and UART3

2. we kindly recommend users to attach a buffer chip between RCD and CPU, chipset SN74AVC16245 is specified

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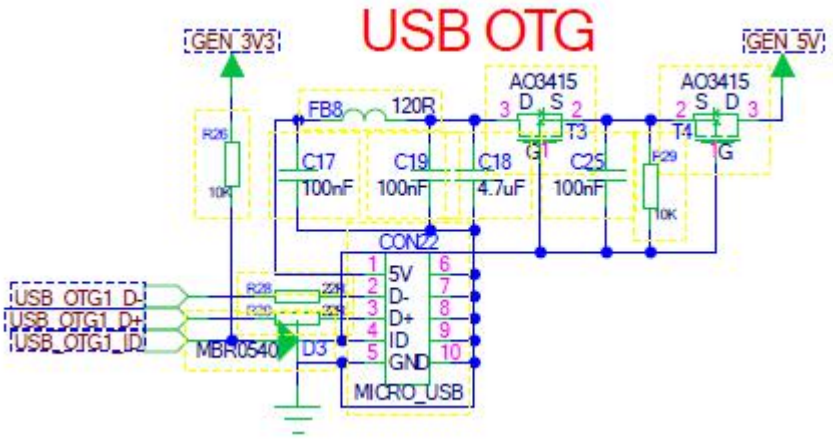
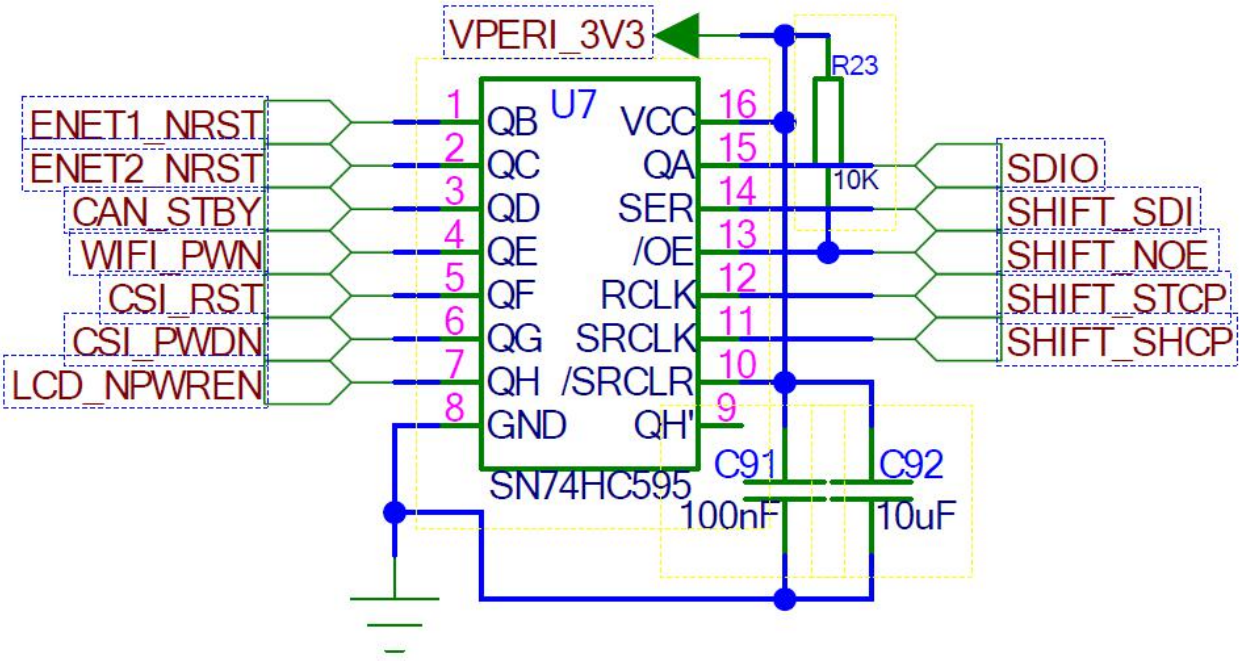
3.4.20 USB OTG

USB OTG is short for USB on-the-go. Briefly, when an USB OTG device (rg. i.MX6UR) is connected to an USB host device (eg. PC), the i.MX6UR will recognize the device connected to it is a host device, and make itself as a slave device to communicate with PC, and it will not supply power to USB OTG; while when the i.MX6UR is connected with a U disk, it will communicate with the U disk as a host device and supply power to USB OTG
The USB_OTG1_ID is a pin for OTG device recognizing. In this circuit, it's also a control pin for the 5V power supply direction.
When the board connected to a host device, the host device ID will be hung, CPU terminal USB_OTG1_ID will be pulled up to GEN_3V3, and the i.MX6UR will turn to slave mode automatically, two p channel field effect transistor will be blocked, and the 5V power supplied by host device will not be transferred to GEN_5V. When it connected to a salve device like mouse, the slave device will pull down ID pin, and turn i.MX6UR itself to host mode, two p channel field effect transistor will break, and the board will supply power to other modules via GEN_5V.
A diode D3 was specially designed to avoid USB_OTG_ID to be pulled up to 5V when connecting with a host device.



3.4.21 Serial/Parallel Convert Circuit

GPIO from the CPU module is limited, the board was designed with a chipset of SN74HC595 integrated a serial in and parallel out convert circuit.
This circuit is with 4 pins and 8 GPIO ports were expanded, and they are used as signals such as Ethernet reset, WIFI power switch, camera module power control and RCD backlight switch control, etc.



Appendix 1 Hardware Design Guideline

1. boot settings

Users could select different methods to flash OS to the board and boot system by different boot settings. Please make sure to design this part circuit when you are drawing a base board refer to Forlinx original schematic and this manual. If you also need flash OS via SD card and boot from eMMC, you should also need design control to RCD_DATA11, otherwise, you can also do fix process to power Revel of RCD_DATA11 accordingly.

2. PMIC_ON_REQ drive capability issue

Both GEN_5V and GEN_3V3 on base board are all controlled and got from PMIC_ON_REQ, current driving capability of PMIC_ON_REQ is too weak and needs voltage control oriented component, AO3416 was used as N channel field effect transistor, meanwhile, the gate of this filed effect transistor should to be designed with a pull-down resistor, otherwise the transistor could not be powered off.

3. IIC was designed with pull-up resistor

When designing a new base board, the IIC bus should have to be designed with pull-up resistor, otherwise, it may cause the IIC bus unavailable. The current two IIC buses on base board were both pulled up to 3.3V via 10k resistors.

4. USB1-1 error during debug process

To work with USB port, both USB_OTG1_VBUS and USB_OTG2_VBUS should have to be connected to 5V, otherwise, errors may appear.

Currently, these two pins are both connected to GNE_5V via a 0Ω resistor.

5. Earphone testing pin

Pin 7 of audio chipset WM8960 is for earphone testing pin and it need to be connected to pin AUD_INT on CPU module to avoid unrecognizable of earphone.

6. Power Revel output by RX of CAN circuit

MCP2551 was used for CAN transceiver chipset for the board, RX output power Revel of this chipset is 5V, while

the Revel of this pin on CPU is 3.3V, to avoid effect of CPU internal 3.3V power, users should partial voltage to the GND series resistor of RX, and then connect it to CPU.

7. SDIO design

The value of series resistor R7 on the SD card clock wire was approved to be 33Ω, and it should be designed near CPU module connectors.

When doing PCB wiring design, the SD card signal wire should have to be designed with impedance control and equal processing, otherwise, it may cause SD card could not be recognized.

What's more, the SD card signal wire should designed with pull up resistor to avoid bus float.

8. Pin CTS and pin RTS of debug port

if connecting RTS and CTS of debug port with DB9 port and power on for communication, the CTS pin of PC serial port would supply power to GEN_3V3 via MAX3232 after powering off the board, this voltage may cause SD card reset abnormal that SD card could not be recognized. Currently, on the board, the two pins were separated by two 0Ω resistor. Users could use a 3-wire debug port when designing a new base board.

9. How to avoid the board connected to Micro USB when powering, to make PC to supply power to the board

Please refer to USB OTG chapter of this manual.

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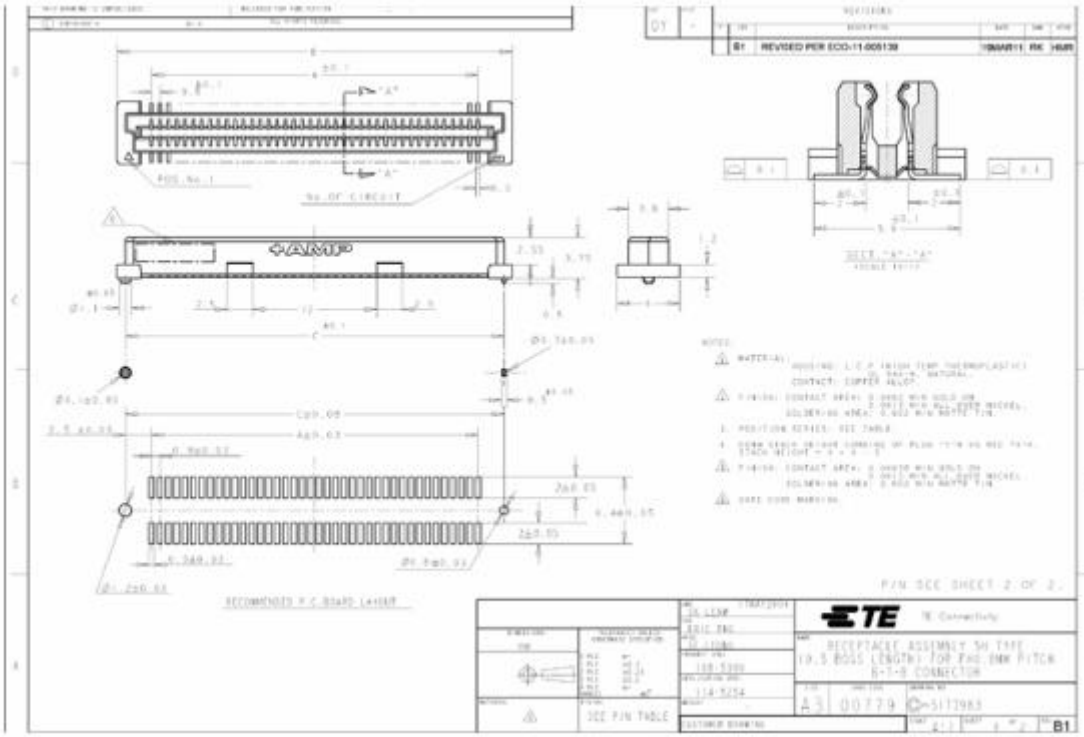
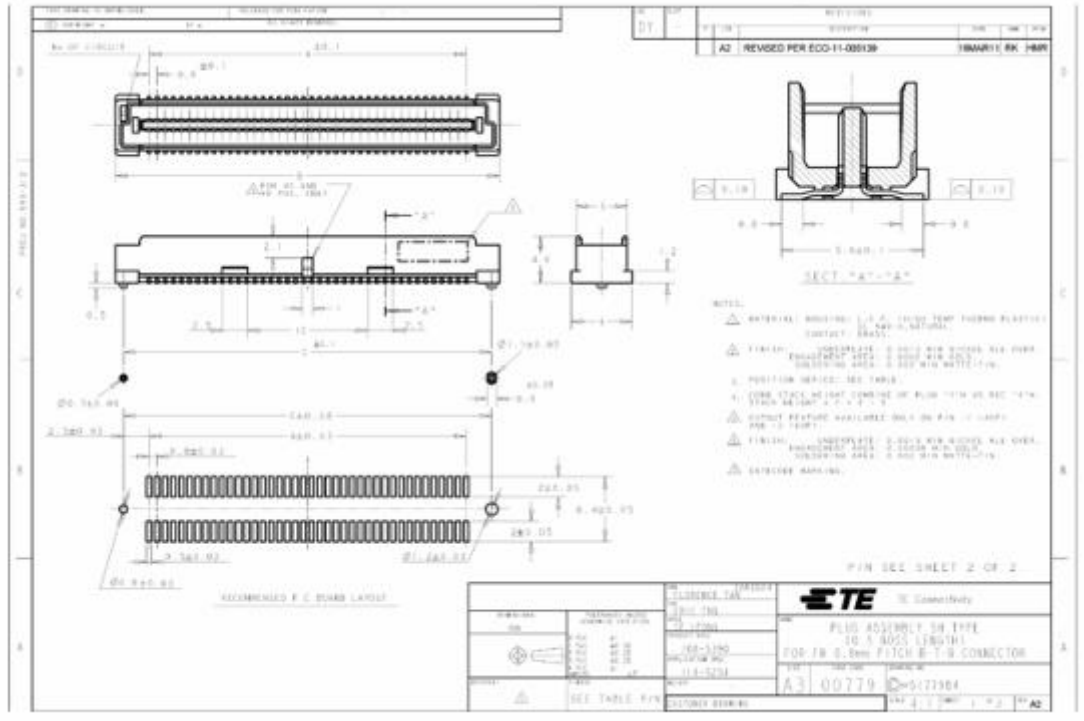
Appendix 2 connector dimension





Thank you!